WHITE PAPER

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Data Retention Performance of 130-nm nvSRAM

Abstract

The nvSRAM (Nonvolatile static random access memory) combines Cypress's industry leading SRAM technology with best-in-class SONOS nonvolatile technology. Cypress's nvSRAM provides infinite read/ write endurance, 1-million STORE cycles on power loss, high-speed read/write access, and nonvolatile data retention.

This white paper provides a brief overview of the data retention performance of the 130-nm nvSRAM.

Introduction

This document provides the data retention performance of Industrial and Automotive grade nvSRAM memory products in 130-nm (0.13-µ) process technology. Data retention is the ability of the SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) cell to retain charge over time. Various factors determine the retention lifetime including flash macro design, fab process technology, and the end-product application. This paper focuses only on one aspect of the end product application and that is *temperature*.

The flash macro can utilize the SONOS cell in many ways. Cells can contain a single SONOS transistor or a pair of transistors operating as a differential pair. Cells can be written one byte at a time or an entire row at a time. Depending on the design, different disturb mechanisms come into play. All these factors can affect the retention lifetime. In the case of nvSRAM, the entire array is written at one time.

The fab process technology affects how much charge is retained in the nitride layer. The stoichiometry, the thickness of the oxide and nitride films, and the degree of ion implantation into the silicon beneath the ONO layer are important for data retention.

Factors of the end application such as the number of times the cell has been programmed and the storage temperature of the device affect the retention lifetime. It is known that the loss of charge is accelerated at higher temperatures. Charge is stored in the nitride layer that is sandwiched between two layers of oxide. Higher temperatures lower the effective barrier to charge de-trapping, thereby reducing the retention lifetime.

Model Description

The Arrhenius model typically used for nonvolatile charge loss does not fit the data for SONOS very well. The poor fit is especially noticeable at lower temperatures where the Arrhenius model provides higher data retention compared to the experimental data. Therefore, Cypress uses the “Temperature model or T-model” instead, which fits the measured data.

$$t_R = t_0 * e^{-\frac{T}{T_0}}$$

where,

$\boldsymbol{t_R}$ is data retention time in sec

$\boldsymbol{t_0}$ is a constant

$\boldsymbol{T}$ is the junction temperature in K, and

$\boldsymbol{T_0}$ is a characteristic temperature of data retention in K

nvSRAM Data Retention

Based on the accelerated and the extended stress experiments, the T-model for the current family of nvSRAM devices in the 130-nm process is as shown below:

$$t_R = (1.551 * 10^{23}) * e^{-\frac{T}{11.256}}$$

Figure 1 shows the data retention time (in years) across various junction temperatures (in °C), where:

$$Junction\ Temperature\ (T)\ in\ K = Junction\ Temperature\ in\ °C + 273.15$$

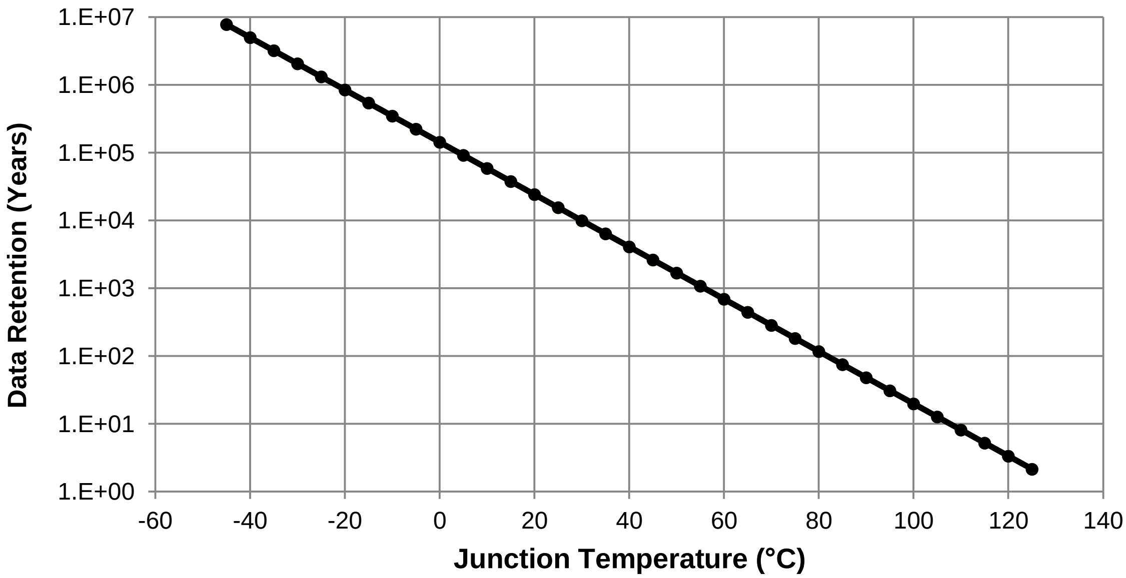

Figure 1. Retention Time of nvSRAM at Various Temperatures

As can be seen, the retention time increases exponentially as temperature decreases.

Summary

The white paper provides an overview of the data retention performance of nvSRAM in 130-nm process and provides the model (T-model) to help in determining the data retention across operating temperatures.

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