200 W dual output 48 V-to-PoL single step converter with XDPP1100 digital controller

Non-isolated buck and half-bridge current-doubler

Scope and purpose

This document describes the reference design (REF_XDP_48V_to_PoL) of a non-isolated hybrid architecture 48 V DC to 12 V DC buck and 48 V DC to 1 V DC half-bridge current-doubler (HB-CD) point-of-load (PoL) solution with a single XDPP1100 digital controller. The following reference design provides fully programmable and configurable dual-outputs with an efficiency up to 97 percent and a voltage accuracy up to ±0.5 percent over the full temperature range from -40°C to 125°C. It has fast line- and load-transient performance using non-linear response, and best-in-class hardware-based feed-forward (FF) response. Moreover, PMBus and I^2C communication is integrated to facilitate system configuration, control and monitoring with telemetry. REF_XDP_48V_to_PoL performance and test results are presented according to each feature, which is described in this document. The design can be used as a basis for the user's further PoL development.

Intended audience

This document would be useful for power supply design engineers who wish to evaluate XDPP1100-Q040 and design their own PoL solutions with buck and half-bridge topologies.

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Abbreviations

HB-CD	Half-bridge current-doubler
MVPoL	Medium-voltage point-of-load
VMC	Voltage mode control
PCMC	Peak current mode control
P2P	Peak-to-peak
V_{IN}	Input voltage
V_{OUTB}	Output voltage of the buck
I_{OUTB}	Output current of the buck
V_{OUTHB}	Output voltage of the HB-CD
I_{OUTHB}	Output current of the HB-CD
OCP	Overcurrent protection
OPP	Overpower protection
OVP	Overvoltage protection
FF	Feed-forward
FW	Firmware

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1 Abstract

PoL converters solve the challenge of high peak current demands and low noise margins, required by high-performance semiconductors such as microcontrollers or ASICs, by placing individual power supply regulators (linear or DC-DC) close to their point of use, where circuits require low voltages of 3.3 V and below. The demand for these types of voltage levels stems from the requirement for lower core voltages, and it is obvious that the current capability for these converters will increase even if the overall power level remains the same, because the output voltage of PoL converters that feeds the core continues to decrease for newer processors. Conventional data center distributed power architectures include an intermediate conversion stage 48 V to 12 V, and 12 V-to-PoL conversion that is distributed to downstream, as shown in **Figure 1**.

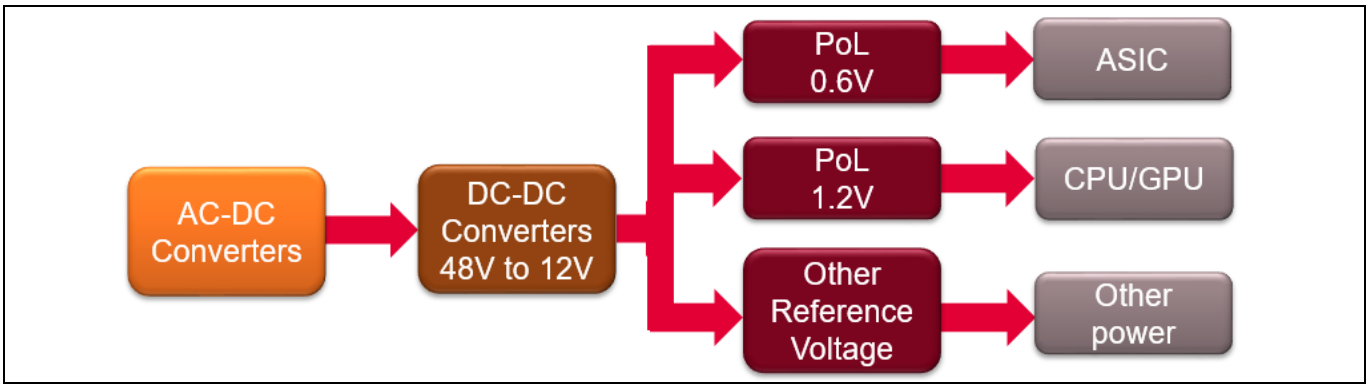


Figure 1 Typical data center power distribution for 48 V

In recent years we have seen a growing trend toward a single-stage conversion, which allows contemporary low-voltage, high-current CPUs, GPUs, ASICs and DDR memory to be powered from a 48 V distribution bus. This technique of down-conversion enables unprecedented power density, conversion efficiency and low power system distribution loss. Today, new topologies and new technologies such as current-doublers and digital control loops are enabling the design of direct-to-chip power architectures, even with IC voltages as low as 1 V, as shown in **Figure 2**.

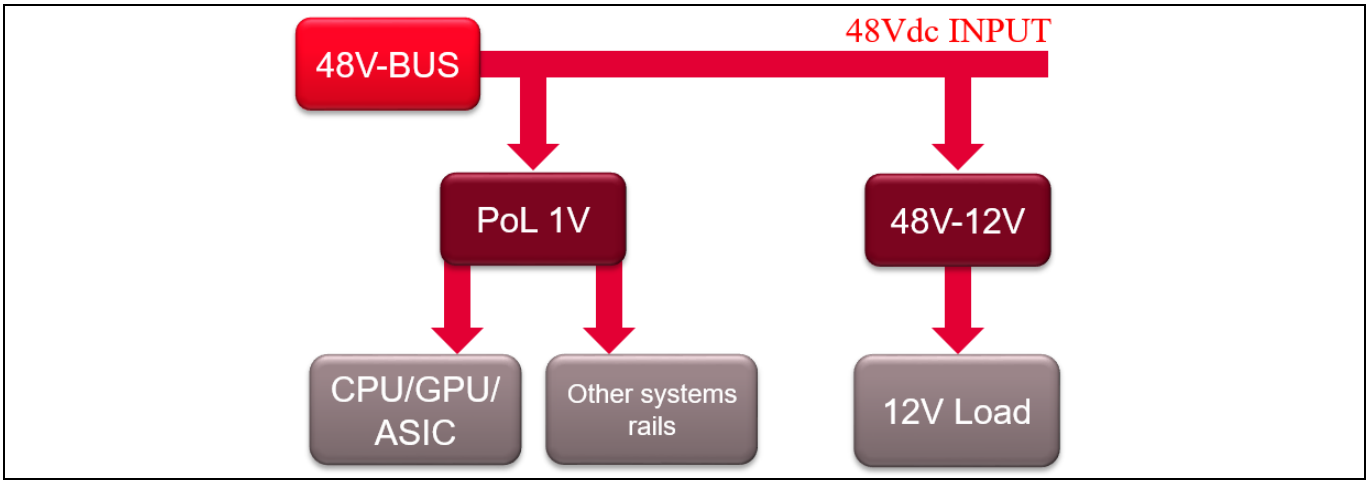


Figure 2 48 V-to-PoL direct architecture

Abstract

In its turn, another interesting example is the telecom radio. These applications require reliable and efficient step-down converters, which have typical 48 V to 12 V isolation. Historically 12 V was used for LDMOS RFPA. Nowadays most of the PAs have been converted to GaN, and that requires a 28 V bus instead. In many countries isolation is not a regulatory requirement, so the system designers can take the 48 V rail and convert it down to lower voltages like 28 V directly using a non-isolated topology.

On the other hand, factors such as cost or legacy issues may determine the point at which some equipment manufacturers consider implementing direct conversion. With direct conversion and traditional modules available side-by-side in the market, designers will also have the freedom to conceive hybrid architectures that combine intermediate bus and direct conversion topologies to deliver the best of both worlds.

2 Background

Some of the notable power supply challenges in telecom infrastructure and data center applications include growing operational costs and thermal management due to increasing power levels, along with shrinking board space due to additional processors, ASICs and FPGAs. Typical early power distribution strategies utilized multiple isolated quarter-brick or eighth-brick converters to convert from initial input voltage rails (usually 48 V) to 12 V bus, which is further converted to the required lower supply voltages 2.5 V, 1.8 V or even 1 V, at the point of load, for example in digital ICs such as MCUs, FPGAs, ASICs and ASSPs.

An intermediate bus converter (IBC) down-converts the nominal 48 V DC from the front-end power supply to a 12 V rail that is distributed to the PoL converters. The PoLs then convert the 12 V input into regulated voltages as needed by onboard ICs. Although many of today's IBC and PoL converters can achieve efficiency in the region of 95 to 96 percent for the IBC, and 90 percent for a typical 12 V to 1 V PoL at a particular load, the cumulative energy loss from both stages of conversion can reduce overall efficiency to a little over 86 percent (**Figure 3**). To take full advantage of switching to 48 V, it is necessary to be able to directly convert from a 48 V supply to a low voltage in a single stage. If a single converter can generate the required IC supply voltage with efficiency, say 89 percent for the same load used in the above example, the overall conversion efficiency can be increased by several percentage points (**Figure 4**).

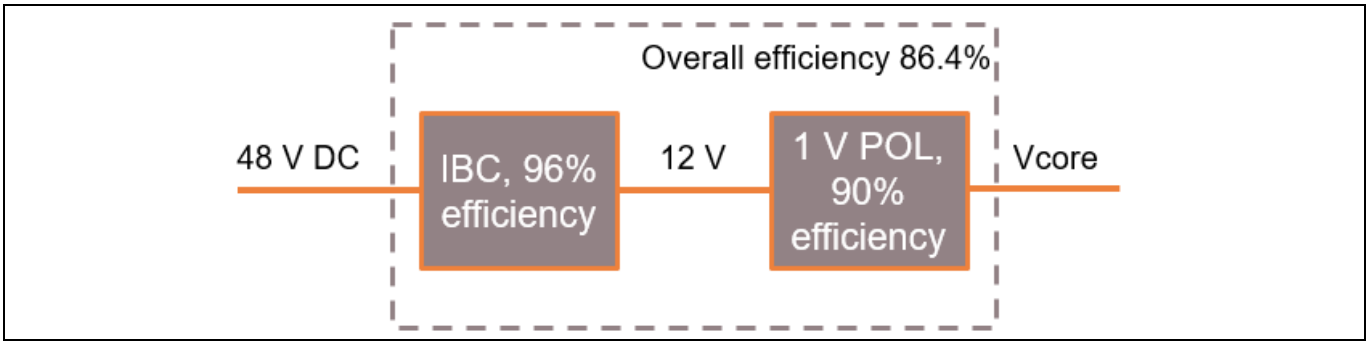


Figure 3 Conventional two-stage 48 V-to-core voltage conversion

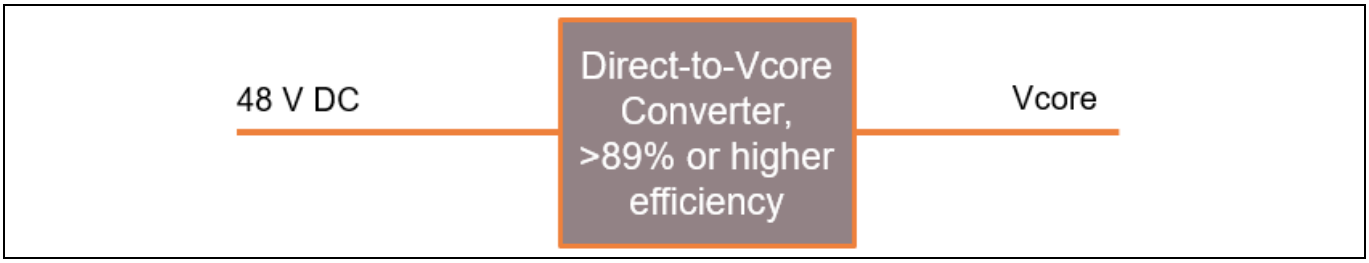


Figure 4 Conventional single-stage 48 V-to-core voltage conversion

The I^2R distribution losses can also be reduced with a single-stage conversion scheme. By distributing 48 V DC for direct conversion at the PoL, the bus supplying the converter carries approximately 25 percent of the current that would be required to deliver the same power at 12 V. Hence I^2R distribution losses from the 48 V source can be reduced by a factor of 16. Reducing I^2R distribution losses becomes increasingly important as total server power continues to increase.

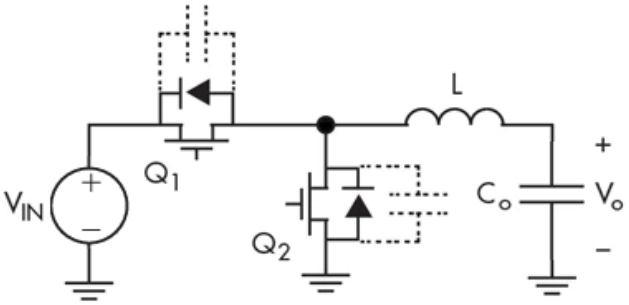
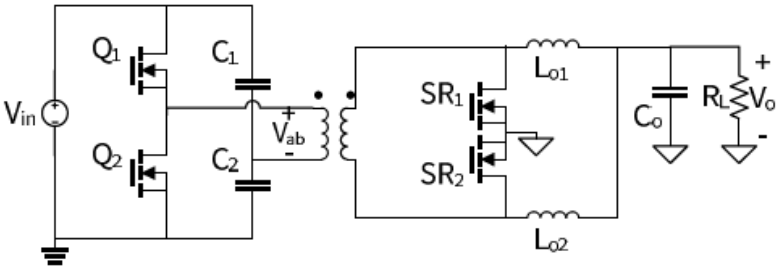
In addition, direct conversion helps to save board real-estate and reduce the cost of materials, electronics assembly and manufacturing. A direct 48 V PoL converter solution can be made smaller in size, compared to the conventional IBC architecture with two-stage conversion, by reducing the number of modules.

Background

The converters should be capable of supporting the low duty cycles required to convert from 48 V to 1 V, while operating at a high switching frequency to ensure fast transient response and minimize reliance on decoupling capacitance and magnetic components.

Generally PoL has many different topologies or configurations, and as yet there appears to be no fixed conversion strategy for stepping down from 48 V to V_{OUT} values that could be as low as 0.9 V. Depending on system requirements, a telecom PoL solution might contain several output channels for different power ratings. In **Table 1**, two topologies used are presented as a core base of the REF_XDP_48V_to_PoL: buck and half-bridge.

Table 1 Applied topologies in MVPoL

Topology	Circuit	Efficiency	Output power
Buck		High	Up to 130 W
HB-CD		Medium	Up to 70 W

The HB converter with CD rectifier is one of the most promising topologies for high input voltage, low output voltage, and high output current applications. The CD rectifier offers the potential benefit of better distributed power dissipation, which would become a vital benefit in densely packed power supplies. Because of its added circuit complexity, this solution could probably be justified in medium- to higher-power and/or high-output current applications.

As a complement, the buck stage might be used for power conversion as a regulated 12 V bus, which is widely in use in telecom applications to distribute electrical power closer to the PoL.

3 System description

The REF_XDP_48V_TO_PoL is a system solution from Infineon for data centers and telecom DC-DC power modules, which operates across a wide range of input voltages (36 V to 75 V). The reference design introduces a single-step digital-controlled hybrid PoL solution with a synchronous buck and a HB-CD delivering 12 V/130 W and 1 V/70 W output power accordingly. The design is implemented using Infineon's single digital power controller XDPP1100, OptiMOS™ MOSFETs and EiceDRIVER™ gate driver ICs, as shown in the block diagram in **Figure 5**.

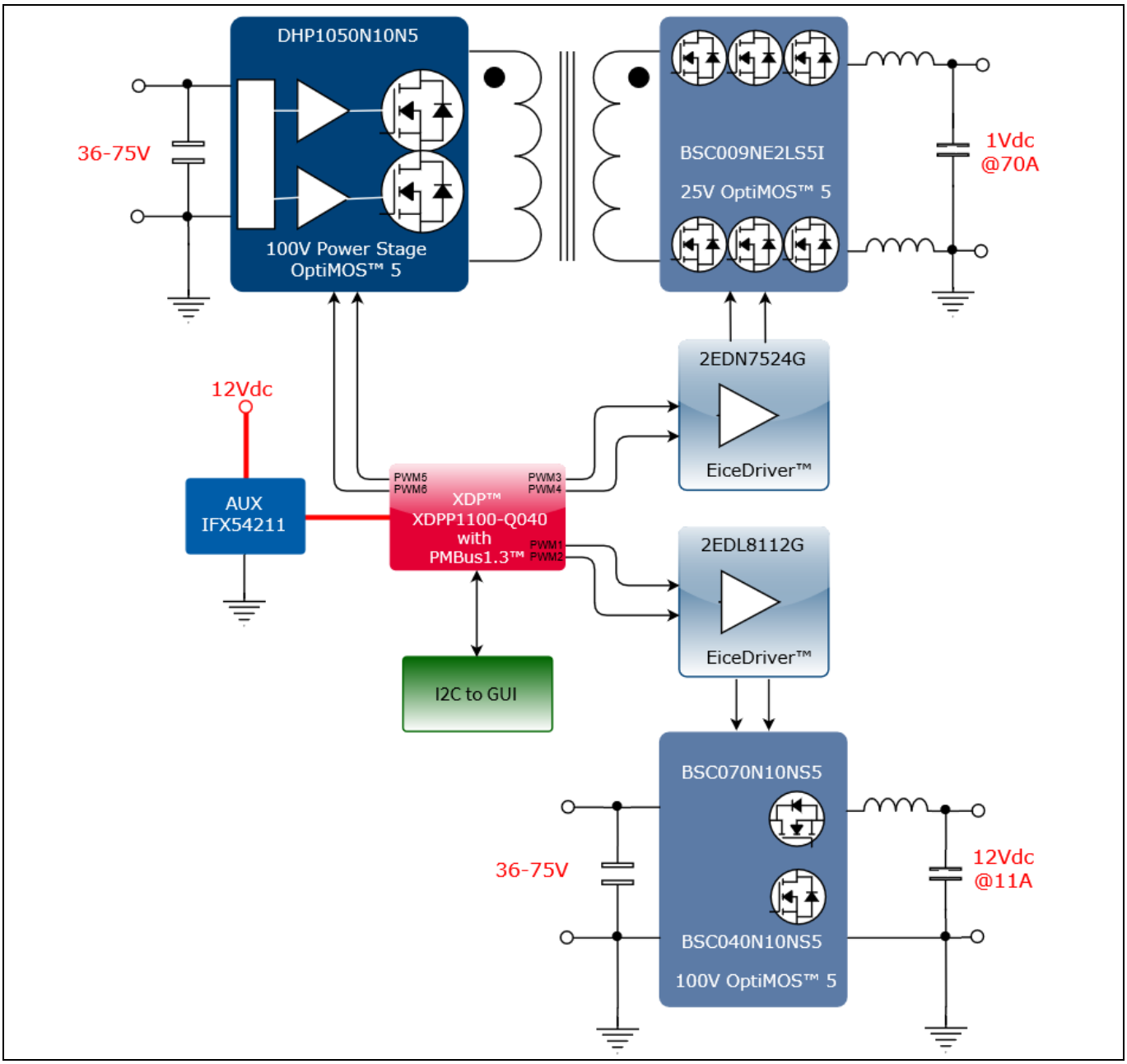


Figure 5 REF_200_HBCD_BUCK_XDPP1100 block diagram

3.1 Buck stage

The buck stage was designed by using EiceDRIVER™ gate driver **2EDL8112G** with a differential input for superb robustness with inherent shoot-through protection to minimize the chance of control signals overlapping, and high-side OptiMOS™ 5 100 V 7 mΩ **BSC070N10NS5** along with low-side OptiMOS™ 5 100 V 4 mΩ **BSC040N10NS5**. A low-side FET transmits three times more current than a high-side FET, so a low-side resistance was picked up lower.

3.2 Half-bridge current-doubler

In its turn, the HB-CD was designed by using a DHP1050N10N5 symmetrical half-bridge with integrated 100 V OptiMOS™ 5 **BSC050N10NS5**, differentiated inputs and level-shift driver on the primary side, along with a dual-channel **2EDN7524G** functional isolated gate driver IC, which controls six OptiMOS™ 5 25 V 0.95 mΩ **BSC009NE2LS5I**s on the secondary side. A planar transformer splits primary and secondary sides and does a voltage step-down with a ratio 6:1. These transformers were implemented to improve power density and reduce board height (low profile). Other benefits are greater surface area to improve heat dissipation capability and greater magnetic cross-section area, which enable fewer turns and a smaller winding area.

3.3 Controller

This design is implemented with Infineon's digital power controller XDPP1100 device. The XDPP1100 device includes an optimized analog front end, multiple pre-programmed peripherals, a fast state-machine-based control loop, and PMBus/I^2C communication peripherals. This unique architecture enhances the performance of isolated and non-isolated DC-DC applications. Moreover, XDPP1100-Q040 supports both VMC and PCMC, which can be configured to operate in this design. **Figure 6** shows the implementation of the REF_XDP_48V_to_PoL.

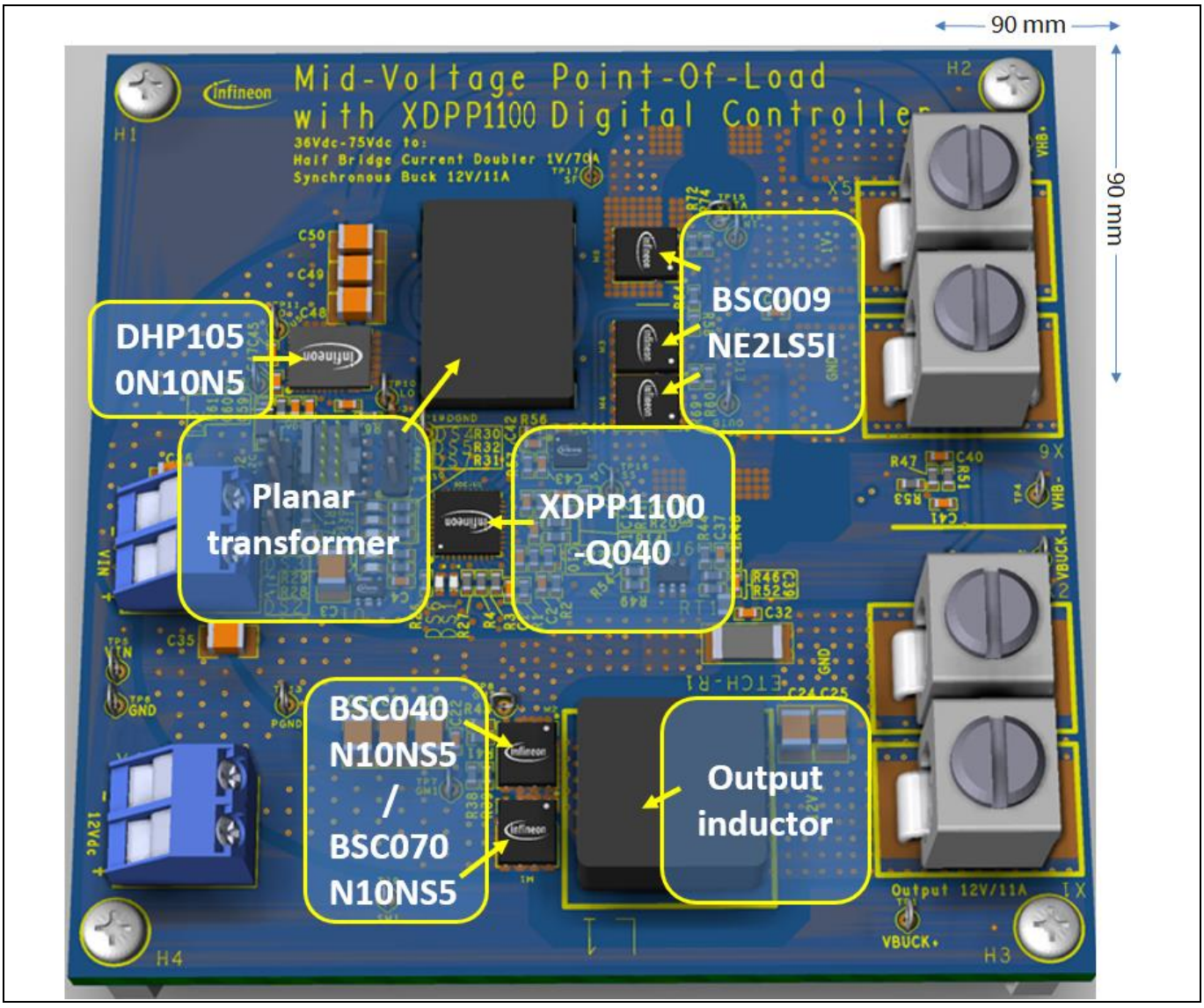


Figure 6 REF_XDP_48V_to_PoL board picture

3.4 Power system specifications

Specifications of the buck power stage:

Table 2 Electrical specifications of synchronous buck side[1]

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V DC	DC input voltage	36	48	75	V	
I_{DC}	Input current	0.037	–	3.7	A	V_{IN} = 36 V to 75 V, no load to full load
V_{OUT}	Output voltage	11.85	12	12.15	V	V_{IN} = 36 V to 75 V, no load to full load
I_{OUT}	Output current	–	–	11	A	V_{IN} = 36 V to 75 V
P_{OUT}	Output power[1]	–	–	132	W	V_{IN} = 36 V to 75 V
	Step-load transient	–	–	230 (pk-pk)	mV	V_{IN} = 36 V to 75 V, I_{out} step-change from 0 A to 11 A, 0.1 A/µs
	Output ripple voltage	–	–	100		V_{IN} = 36 V to 75 V
η	Efficiency[2]		96.5%			V_{IN} = 36 V, I_{OUT} = 50 percent and P_{OUT} = 66 W
			95%			V_{IN} = 36 V, I_{OUT} = 20 percent and P_{OUT} = 26 W
			96%			V_{IN} = 36, I_{OUT} = 100 percent and P_{OUT} = 132 W
F_{SW}	Switching frequency		332		kHz	

Specification of the HB-CD power stage:

Table 3 Electrical specifications of HB-CD side[1]

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V DC	DC input voltage	36	48	75	V	
I_{DC}	Input current	0.02	–	2	A	V_{IN} = 36 V to 75 V, no load to full load
V_{OUT}	Output voltage	0.97	1	1.02	V	V_{IN} = 36 V to 75 V, no load to full load
I_{OUT}	Output current	–	–	70	A	V_{IN} = 36 V to 75 V
P_{OUT}	Output power[1]	–	–	70	W	V_{IN} = 36 V to 75 V
	Step-load transient	–	–	45 (pk-pk)	mV	V_{IN} = 36 V to 75 V, I_{out} step-change from 25 A to 75 A, 0.1 A/µs
	Output ripple voltage	–	–	10		V_{IN} = 36 V to 75 V
η	Efficiency[2]		92.5%			V_{IN} = 36 V, I_{OUT} = 40 percent and P_{OUT} = 28 W
			91.6%			V_{IN} = 36, I_{OUT} = 20 percent and P_{OUT} = 14 W
			87.7%			V_{IN} = 48, I_{OUT} = 100 percent and P_{OUT} = 70 W
F_{SW}	Switching frequency		250		kHz	

[1] Operation at ambient temperature 24°C with forced air cooling (400 LFM)

4 Configuration

XDPP1100-Q040 devices can be configured with Infineon's easy-to-use, complementary GUI tool in two ways: PMBus setting configuration and direct register configuration. These configurations can be stored in a configuration file uploaded to the XDPP1100 non-volatile memory. For additional information, refer to application note "**The XDPP1100 digital power supply controller**". The main configuration settings are highlighted in this section.

4.1 PMBus configuration

The key PMBus commands are listed in **Table 4** (buck loop) and **Table 5** (HB-CD loop).

Table 4 Basic PMBus configuration (loop 0, buck side)

Command	Name	Data	Description
00	PAGE	00	Control loop 0
02	ON_OFF_CONFIG	1F	Responds to operation and EN pin, EN polarity active high
20	VOUT_MODE	14	-12 mode: 0.244 mV output voltage resolution
21	VOUT_COMMAND	0C00	Target output voltage: 12 V
24	VOUT_MAX	0D00	13 V
27	VOUT_TRANSITION_RATE	E850	10,000 mV/µs
29	VOUT_SCALE_LOOP		0.0989532471
32	MAX_DUTY	F180	40 percent
33	FREQUENCY_SWITCH	087D	332 kHz
34	POWER_MODE	03	0x03
61	TON_RISE	F050	Start-up time: 20.000 ms
CD	MFR_VRECT_SCALE		Input voltage resistor-divider factor 0.024902
CE	MFR_TRANSFORMER_SCALE		1
EA (loop 0)	MFR_IOUT_APC (defines ISEN gain for buck I_{OUT})		0.041016 A

Table 5 Basic PMBus configuration (loop 1, HB-CD side)

Command	Name	Data	Meaning
00	PAGE	01	Control loop 1
02	ON_OFF_CONFIG	1F	Responds to operation and EN pin, EN polarity active high
20	VOUT_MODE	14	-12 mode: 0.244 mV output voltage resolution
21	VOUT_COMMAND	0C00	Target output voltage: 1 V
24	VOUT_MAX	0D00	1.1 V
27	VOUT_TRANSITION_RATE	E850	10,000 mV/µs
29	VOUT_SCALE_LOOP		1
32	MAX_DUTY	F180	60 percent
33	FREQUENCY_SWITCH	087D	250 kHz
34	POWER_MODE	03	0 x 03
61	TON_RISE	F050	Start-up time: 20.000 ms
CD	MFR_VRECT_SCALE		0.999023 (VRECT_SCALE is taken from loop 0)
CE	MFR_TRANSFORMER_SCALE		Transformer turns ratio 0.167
EA (loop1)	MFR_IOUT_APC (defines BISEN gain for HB-CD I_{OUT})		0.636 A

4.1.1 Dead-time configuration

Dead-time can be set by PMBus command 0xCF PWM_DEADTIME. The maximum dead-time can be set to 318.75 ns with a resolution of 1.25 ns. **Table 6** shows the dead-time of REF_XDP_48V_to_PoL.

Table 6 Dead-time configuration

PWM output	Edge	Value	Labels: refer to Fig. 7 and Fig. 8	Description
PWM5	Rising	30 ns	Fig. 7. Q1: DT1	Rising time of PWM for the buck primary-side FET
	Falling	0 ns	Fig. 7. Q1: DT2	Falling time of PWM for the buck primary-side FET
PWM6	Rising	30 ns	Fig. 7. Q2: DT4	Rising time of PWM for the buck secondary-side FET
	Falling	0 ns	Fig. 7. Q2: DT3	Falling time of PWM for the buck secondary-side FET
PWM3/4	Rising	7.5 ns	Fig. 8. Q1/2: DT1/3	Rising time of PWM for the HB-CD primary-side FET
	Falling	0 ns	Fig. 8. Q1/2: DT2/4	Falling time of PWM for the HB-CD primary-side FET
PWM1/2	Rising	48.5 ns	Fig. 8. SR1/2: DT9/11	Rising time of PWM for the HB-CD secondary-side FETs
	Falling	0 ns	Fig. 8. SR1/2: DT10/12	Falling time of PWM for the HB-CD secondary-side FETs

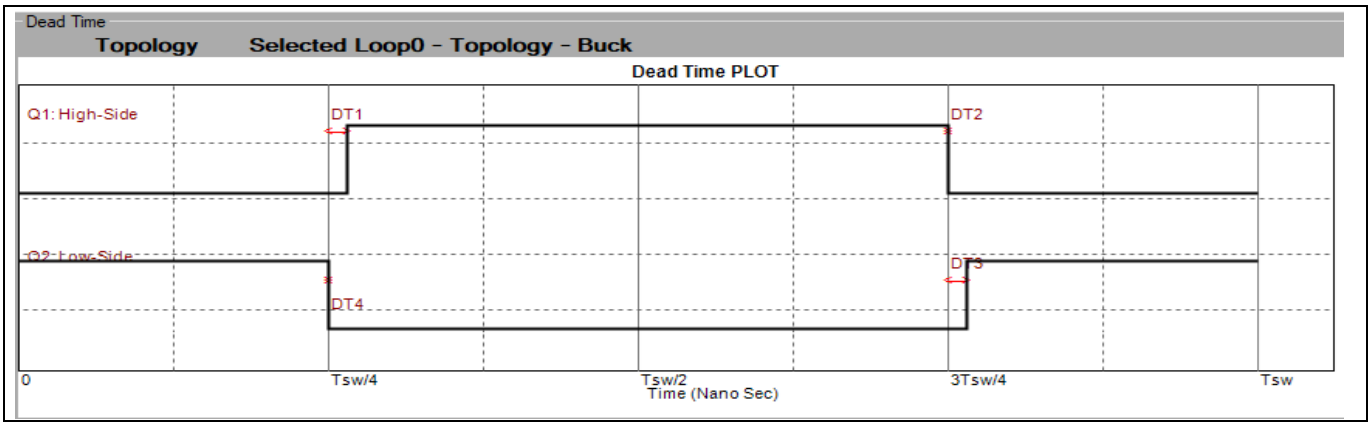


Figure 7 Buck dead-time configuration

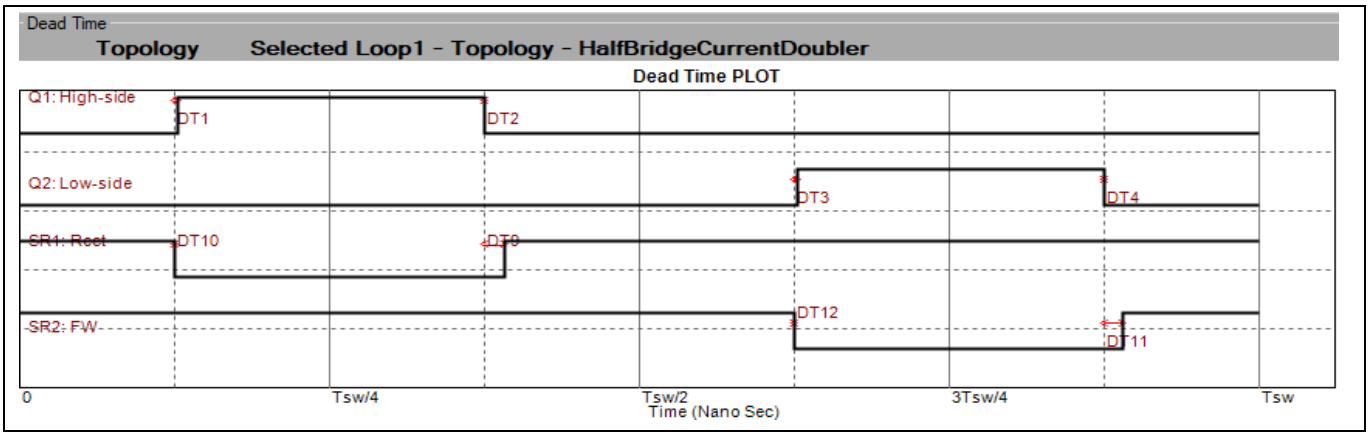


Figure 8 HB-CD dead-time configuration

4.1.2 Regulation configuration

In 0xC5 FW_CONFIG_REGULATION might be set such regulation features as a diode emulation start-up and shutdown or interleaved feature.

Table 7 Buck regulation configuration

Name	Value	Description
V_{OUT} target window	120 mV	Output voltage window frame lets XDPP1100 know the voltage target is being reached. Defines the SR enabling threshold during DE start-up. (Exponent is -8.)
Topology	7	Topology selection – “7” means buck.
EN_IOUT_APC_TEMP_COMP	1	Enable temperature compensation on current sense gain.
EN_DEADTIME_ADJ	1	Enable PWM dead-time adjustment from max. dead-time to set-point at target voltage.

Table 8 HB-CD regulation configuration

Name	Value	Description
V_{OUT} target window	20 mV	Output voltage window frame lets XDPP1100 know the voltage target is being reached. Defines the SR enabling threshold during DE start-up. (Exponent is -8.)
Topology	2	Topology selection – “2” means half-bridge.
EN_IOUT_APC_TEMP_COMP	1	Enable temperature compensation on current sense gain.
EN_DEADTIME_ADJ	1	Enable PWM dead-time adjustment from max. dead-time to set-point at target voltage.
CURRENT_DOUBLER_ENABLE	1	Enable current doubling for two inductors in the circuit.

4.1.3 Temperature configuration

REF_XDP_48V_to_PoL has two temperature sense channels, which are performed with a 47 kΩ NTC thermistor, in parallel with a 12 kΩ resistor connected between ATSEN or BTSEN and ground. This design uses two NTC resistors: the first is connected to BTSEN (tempb) to sense the PCB temperature near the HB-CD current sense copper; the second is placed near the buck current sense resistor and is connected to the ATSEN pin (tempa). The temperature is used to compensate for the current sense resistor value and for overtemperature protection.

MFR_SELECT_TEMPERATURE_SENSOR is used to configure the temperature sensor.

Table 9 Temperature settings: MFR_SELECT_TEMPERATURE_SENSOR

Parameter	HB-CD/value	Buck/value	Description
Fault source select	0: tempb	1: tempa	Input current estimate alpha coefficient Registers: fault_temp_src_sel and fault_temp_fault_hyst. Refer to chapter 5.7
Read_Temperature_1_ Read_Temperature_2	3: tempb tempi	1: tempa tempi	Input current telemetry source select

4.1.4 Protection configuration

XDPP1100 has multiple protection features, which ensure reliable operation under any conditions. The default fault thresholds and fault response of the REF_XDP_48V_to_PoL are listed in **Table 10**.

Table 10 Default fault protection configuration

Protection type		PMBus command	HB-CD/default value (PMBus configurable)	Buck/default value (PMBus configurable)
Output overvoltage	Fault limit threshold	0x40 VOUT_OV_FAULTS_LINIT	1.3 V	14 V
	Warn limit threshold	0x42 VOUT_OV_WARN_LIMIT	1.05 V	13.5 V
	Fault response	0x41 VOUT_OV_FAULT_RESPONSE	Disable and retry, no retry	Disable and retry, no retry
Output undervoltage	Fault limit threshold	0x43 VOUT_UV_FAULTS_LINIT	0.7 V	8 V
	Warn limit threshold	0x44 VOUT_UV_WARN_LIMIT	0.8 V	9 V
	Fault response	0x41 VOUT_UV_FAULT_RESPONSE	Ignore fault	Ignore fault
Output overcurrent	Fault limit threshold	0x46 IOUT_OV_FAULTS_LINIT	78 A	14 A
	Warn limit threshold	0x4A IOUT_OV_WARN_LIMIT	74 A	13 A
	Fault response	0x47 IOUT_OV_FAULT_RESPONSE	Operate for delay time 2 ms, retry once with 2 ms delay	Operate for delay time 2 ms, retry once with 2 ms delay
Output undercurrent	Fault limit threshold	0x4B IOUT_UV_FAULTS_LINIT	-128 A	-128 A
	Fault response	0x4C IOUT_UV_FAULT_RESPONSE	Disable and retry, no retry	Disable and retry, no retry
Overtemperature	Fault limit threshold	0x4F OT_FAULT_LIMIT	125°C	125°C
	Warn limit threshold	0X51 OT_WARN_LIMIT	90°C	90°C
	Fault response	0X50 OT_FAULT_RESPONSE	Disable and resume when OK, fault clears when onboard NTC temperature falls below the warn limit	Disable and resume when OK, fault clears when onboard NTC temperature falls below the warn limit

Protection type		PMBus command	HB-CD/default value (PMBus configurable)	Buck/default value (PMBus configurable)
Undertemperature	Fault limit threshold	0x53 UT_FAULT_LIMIT	-40°C	-40°C
	Warn limit threshold	0x52 UT_WARN_LIMIT	-35°C	-35°C
	Fault response	0x54 UT_FAULT_RESPONSE	Ignore fault	Ignore fault
Input overvoltage	Fault limit threshold	0x55 VIN_OV_FAULT_LIMIT	80 V	80 V
	Warn limit threshold	0x57 VIN_OV_WARN_LIMIT	78 V	78 V
	Fault response	0x56 VIN_OV_FAULT_RESPONSE	Disable and retry, no retry	Disable and retry, no retry
Input undervoltage	Fault limit threshold	0x59 VIN_UV_FAULT_LIMIT	31 V	31 V
	Warn limit threshold	0x58 VIN_UV_WARN_LIMIT	33 V	33 V
	Fault response	0x5A VIN_UV_FAULT_RESPONSE	Ignore fault	Ignore fault
Input overcurrent	Fault limit threshold	0x5B IIN_OC_FAULT_LIMIT	7.5 A	7.5 A
	Warn limit threshold	0x5D IIN_OC_WARN_LIMIT	6.5 A	6.5 A
	Fault response	0x5C IIN_OC_FAULT_RESPONSE	Disable and retry, no retry	Disable and retry, no retry

4.2 Register configuration

The XDPP1100 GUI provides the necessary design tools for the user to configure the registers.

4.2.1 PID filter register configuration

Table 11 PID configuration

Register name	HB-CD/value	Buck/value	Description
pid0/1_kfp1_index_1ph	43	31	PID pre-filter coefficient index
pid0/1_kfp2_index_1ph	43	31	PID post-filter coefficient index
pid0/1_kp_index_1ph	56	57	PID proportional coefficient index
pid0/1_ki_index_1ph	17	20	PID integral coefficient index
pid0/1_kd_index_1ph	61	89	PID derivative coefficient index

4.2.2 Feed-forward register configuration

The FF computation is implemented in hardware and thus offers the fastest response. The XDPP1100-Q040 computes FF duty cycle based on input voltage and output voltage, and the result is added to the feedback loop PID filter output to resolve PWM duty cycle.

$$computed\_feed\_forward = \frac{Vout\_target}{Vin \times trans\_scale\_loop}$$

Basically, the FF filter reads and inverses the input voltage to produce the following relationship:

- when V_{IN} decreases, FF filter output increases and therefore duty cycle will be increased
- when V_{IN} increases, FF filter output decreases and therefore duty cycle will be decreased

In REF_XDP_48V_to_PoL, VRSEN is used for the FF computation. **Table 12** shows the FF settings for both channels.

Table 12 FF settings

Register name	HB-CD/value	Buck/value	Description
pid0/1_ff_dt_adj	11	18	FF adjustment for dead-time
pid0/1_kp_ff_lpf	7	17	FF low-pass filter coefficient
pid0/1_ff_gain_scale	10	16	FF gain scale
pid0/1_ff_vrect_sel	VS1	VS1	FF V_{rect} (V_{IN}) source select
vrs_same_cycle_en	Enabled	Enabled	To enable faster FF response after entering tracking mode. Otherwise, V_{rect} will only be updated on the falling PWM edge.

4.2.3 Telemetry register configuration

The main telemetry settings are presented in this section.

4.2.3.1 Output current register configuration

Exceptional noise immunity is achieved by the use of the internal current estimator. Its settings are presented in **Table 13**.

Table 13 Output current register configuration

Register name	HB-CD/ value	Buck/ value	Description
ce0/1_ktrack_hiz	2	1	Current sense tracking gain in the HiZ state
ce0/1_ktrack_off	8	6	Current sense tracking gain in the off state
ce0/1_ktrack_on	8	6	Current sense tracking gain in the on state
ce0/1_kslope_didv	1	1	Inductor negative current limit (NCL) fault threshold
ce0/1_pwmwin_dly	4	8	Defines delay used to align internal PWM signals to incoming current sense waveform
ce0/1_ladj_en	Enable	Enable	Inductor slope correction function enable
ce0/1_ps_current_emu	0	0	Primary side (1), secondary side (0), current sense select
ce0/1_dt_l_slope	156	2	Defines the slope of the output inductance depending on current
ce0/1_Itrace	6	30	Defines parasitic trace inductance as seen by current sense input
isen1/2_gain_mode	1.45 mV GND	1.45 mV GND	ISEN1/2 (ISEN(1)/BISEN(2)) gain mode select

4.2.3.2 Input current register configuration

When the converter is configured in VMC, the input current telemetry can only be selected as “estimated input current” based on the output current.

The input current is estimated for both loops (see **Table 14**).

Table 14 Input current settings

Register name	Value	Description
tlm_iin_est_alpha	48	Input current estimate alpha coefficient. See the formula: $Iin\_est = Iout \cdot \left[\frac{Vout}{Vin} + alpha \cdot \left(\frac{Duty}{Nx} - \frac{Vout}{Vin}\right)\right]$, where Nx = 2 * N_{turn} if half-bridge = N_{turn} otherwise
tlm_iin_src_sel	2	Input current telemetry source select
tlm_kfp_iin	24	Input current telemetry low-pass filter coefficient index

5 System performance

5.1 Efficiency

REF_XDP_48V_to_PoL efficiency curves at different input voltages are shown below:

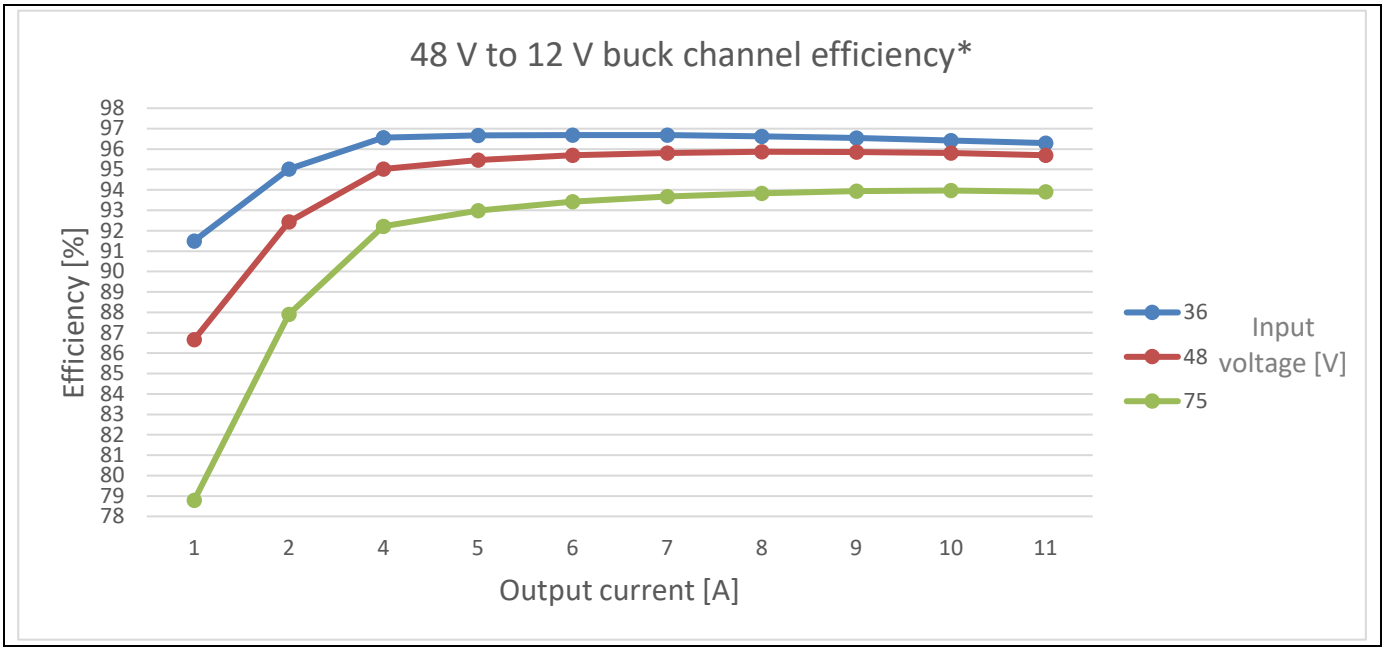


Figure 9 Efficiency of the buck channel for various input voltages

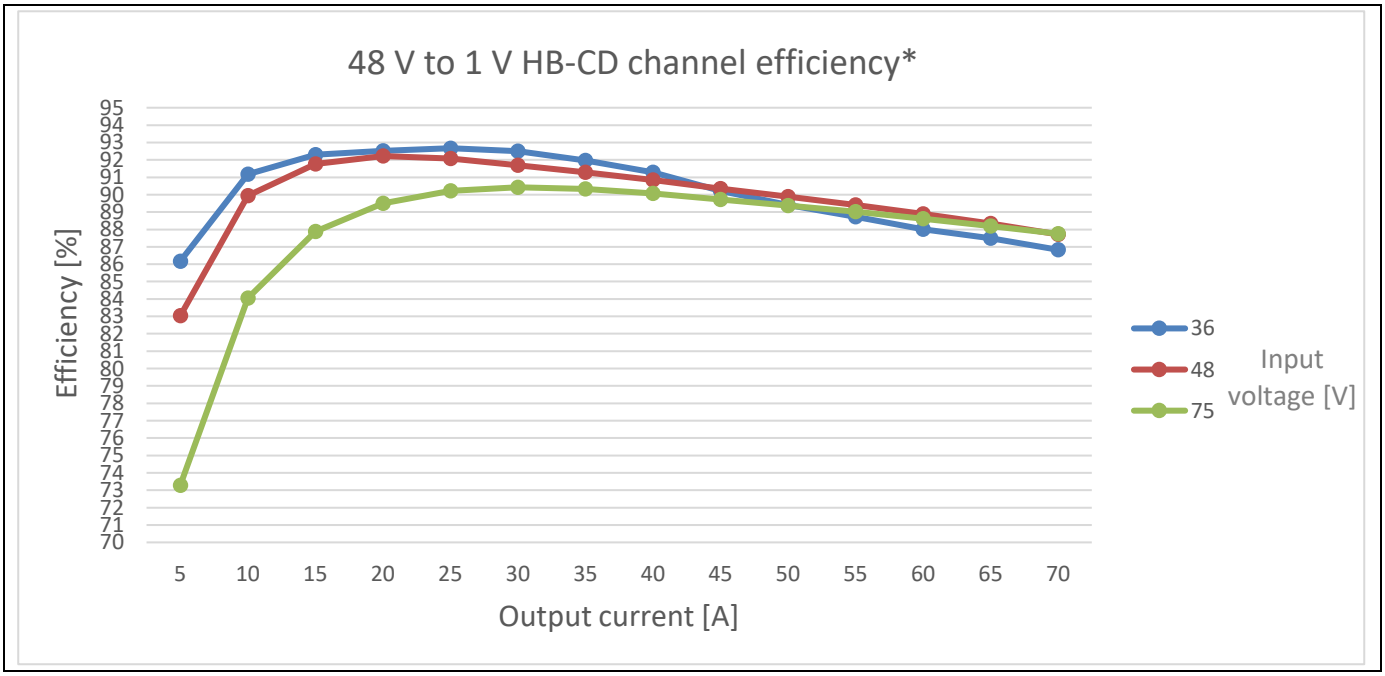


Figure 10 Efficiency of the HB-CD channel for various input voltages

*Efficiency was measured with the following conditions:

- Cooling: from the fan with ~500 LFM
- Room temperature: 25°C
- External V_{DD} 12 V supply = 10.8 V

5.2 Steady-state switching diagrams

The buck and HB-CD converters are operating at fixed frequencies of 330 kHz and 250 kHz respectively. Steady-state waveforms are shown below with applied PID and dead-time settings from the configuration section.

5.2.1 Buck switching diagrams

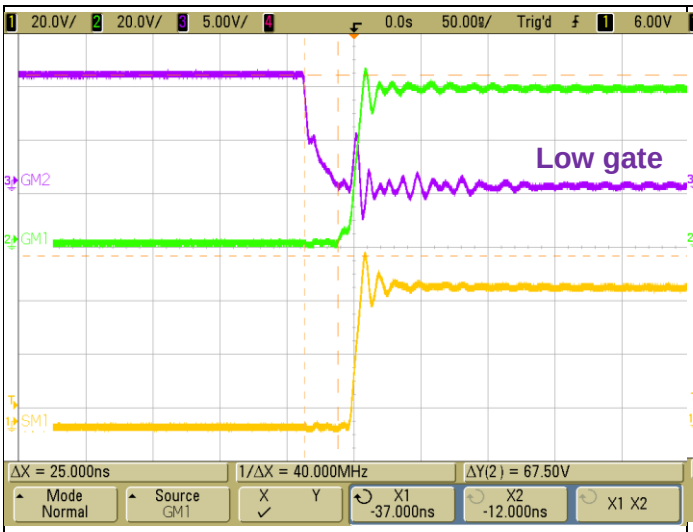


Figure 11a: Buck switching waveforms with 1 A output current

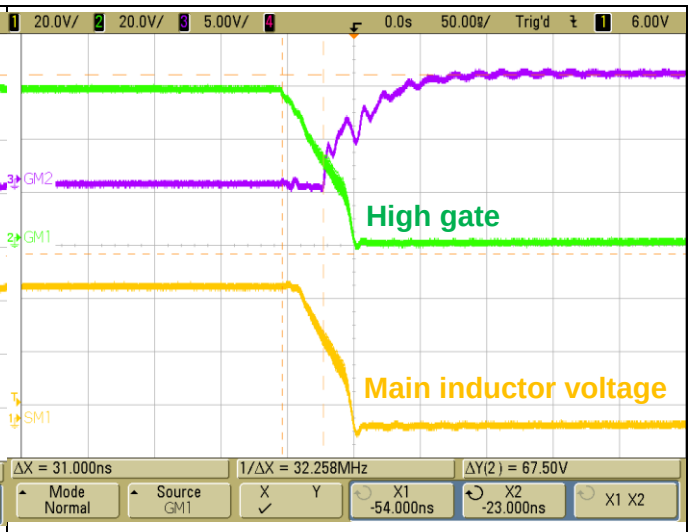


Figure 11a: Buck switching waveforms with 1 A output current

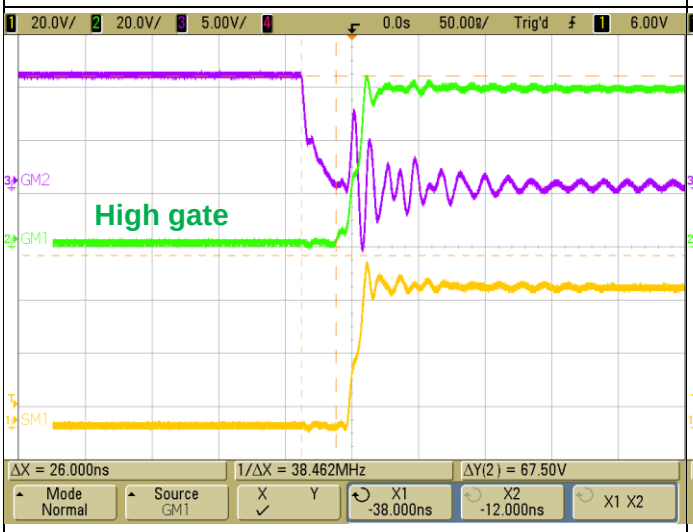


Figure 11b: Buck switching waveforms with 11 A output current

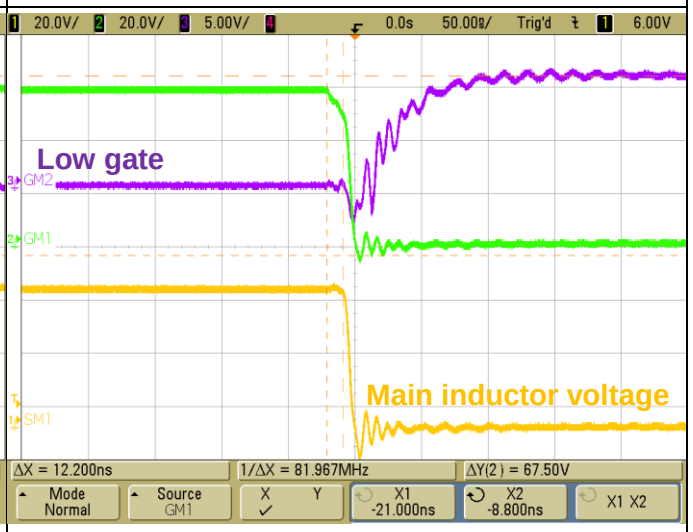


Figure 11b: Buck switching waveforms with 11 A output current

Figure 11 Buck switches with 48 V input voltage

5.2.2 HB-CD switching diagrams

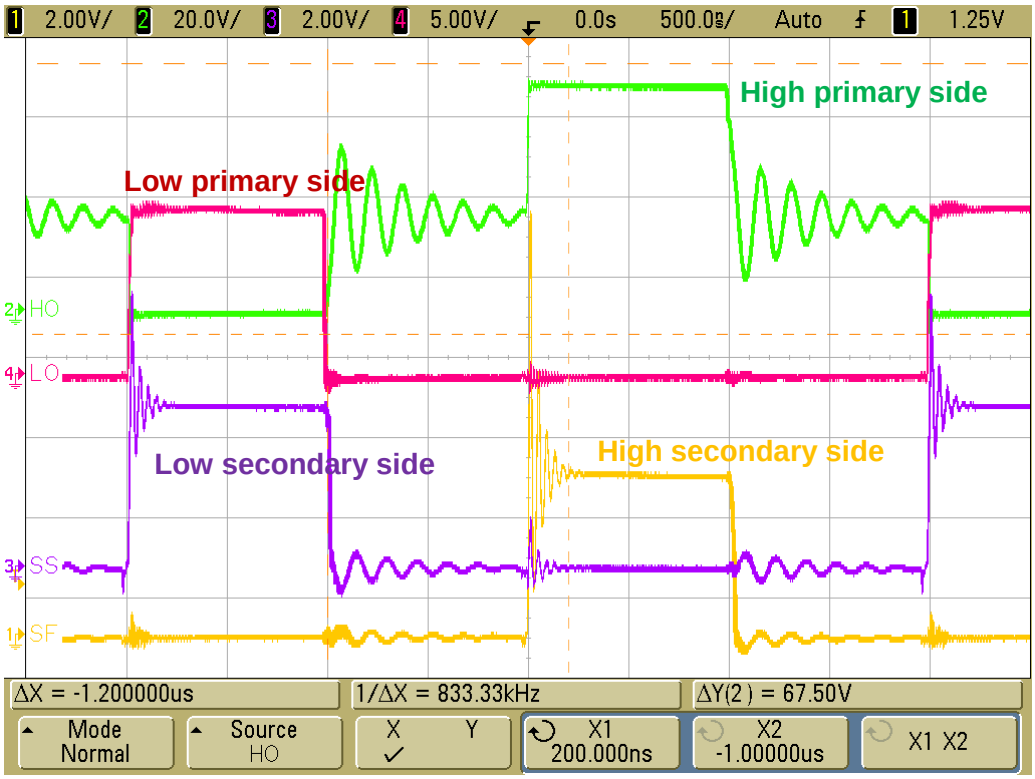


Figure 12a: HB-CD switching waveforms with 5 A output current

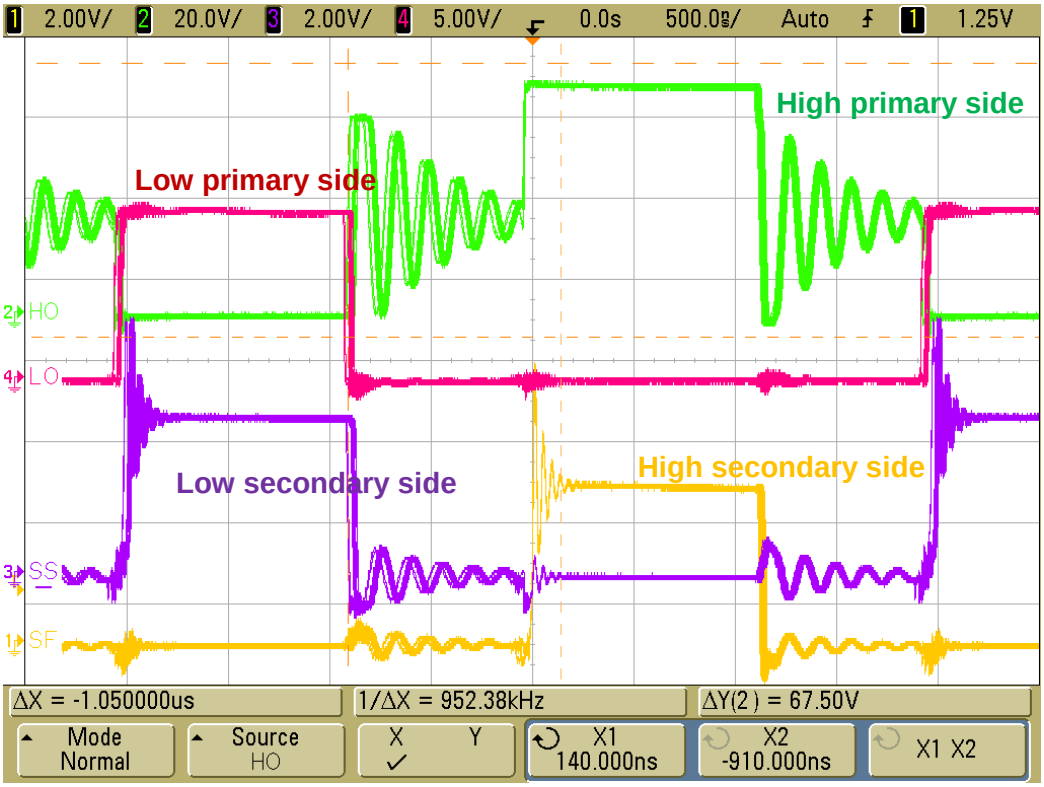


Figure 12b: HB-CD switching waveforms with 70 A output current

Figure 12 HB-CD switching waveforms with 48 V input voltage

5.3 Start-up regulation

A soft-start function minimizes a large input current at start-up by gradually increasing the switch-current limit at start-up, slowing the rate of rise of the output voltage and reducing the peak current required when starting up. The system's start-up was tested for various output load and input voltage conditions. V_{OUT} has monotonic ramp without glitch.

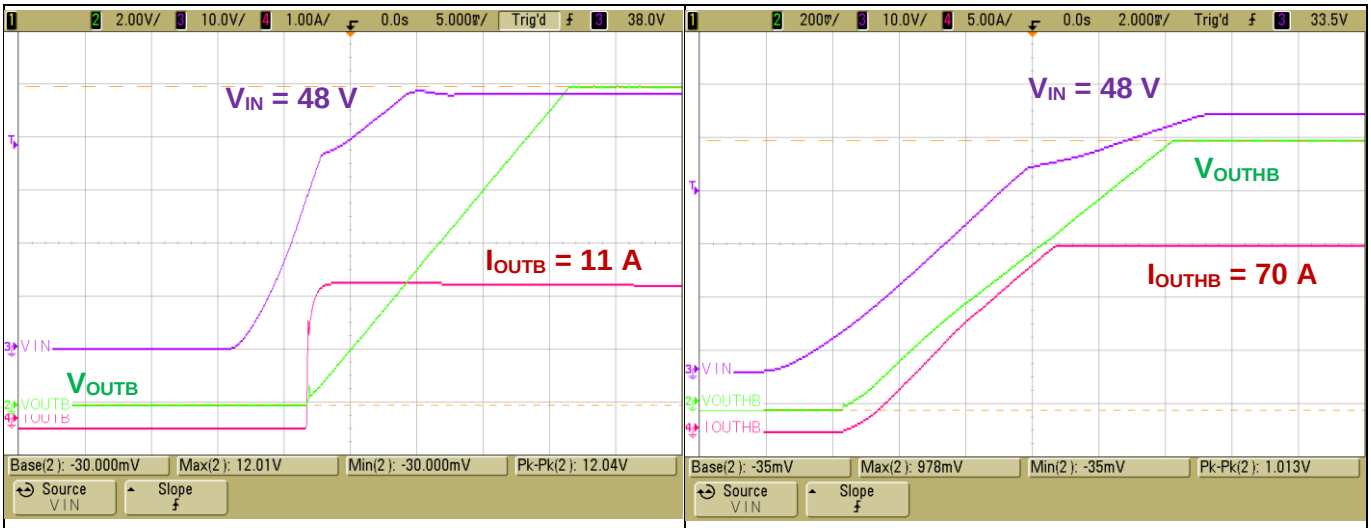


Figure 13a: Buck start-up with 11 A output load and 20 ms TON_RISE

Figure 13b: HB-CD start-up with 70 A output load and 10 ms TON_RISE

Figure 13 REF_XDP_48V_TO_PoL start-up behavior with full output load

5.4 Telemetry accuracy

5.4.1 Output voltage telemetry

The voltage sense ADC is an 11-bit ADC with 50 MHz sampling rate. The ADC resolution is 1.25 mV and enhanced with 3-bit digital modulation for output voltage regulation, which gives 156 µV resolution at the sense pin in total. Assuming an upper boundary of the voltage sense in 2.1 V and to optimize its accuracy, the buck 12 V target output voltage has a voltage divider with a scale 0.099 to reach 1.2 V on the sensing pins VSEN/VREF. In turn, the HB-CD 1 V target output voltage is perfectly suited to the ADC range, so it is connected directly to BVSEN/BVREF.

Figure 14 shows an accuracy of buck V_{OUTB} telemetry for conditions 36 V, 48 V and 75 V input voltages and from 1 A to 11 A output load. The accuracy is within the target range of ±0.5 percent or ±60 mV.

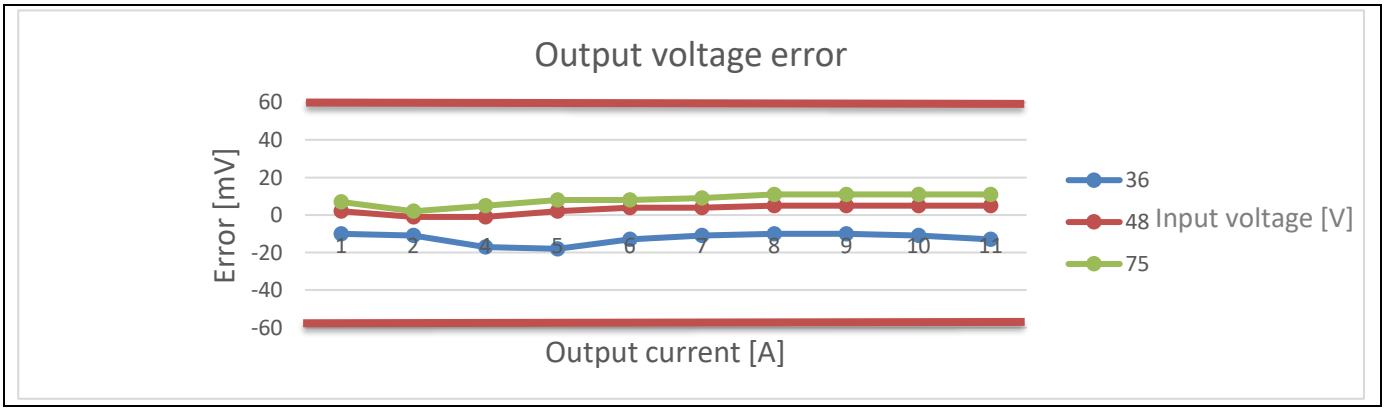


Figure 14 Buck output voltage accuracy

Figure 15 represents HB-CD V_{OUTHB} accuracy in conditions 36 V, 48 V and 75 V input voltages and from 5 A to 70 A output load. The accuracy is within the target range of ±0.5 percent or ±5 mV.

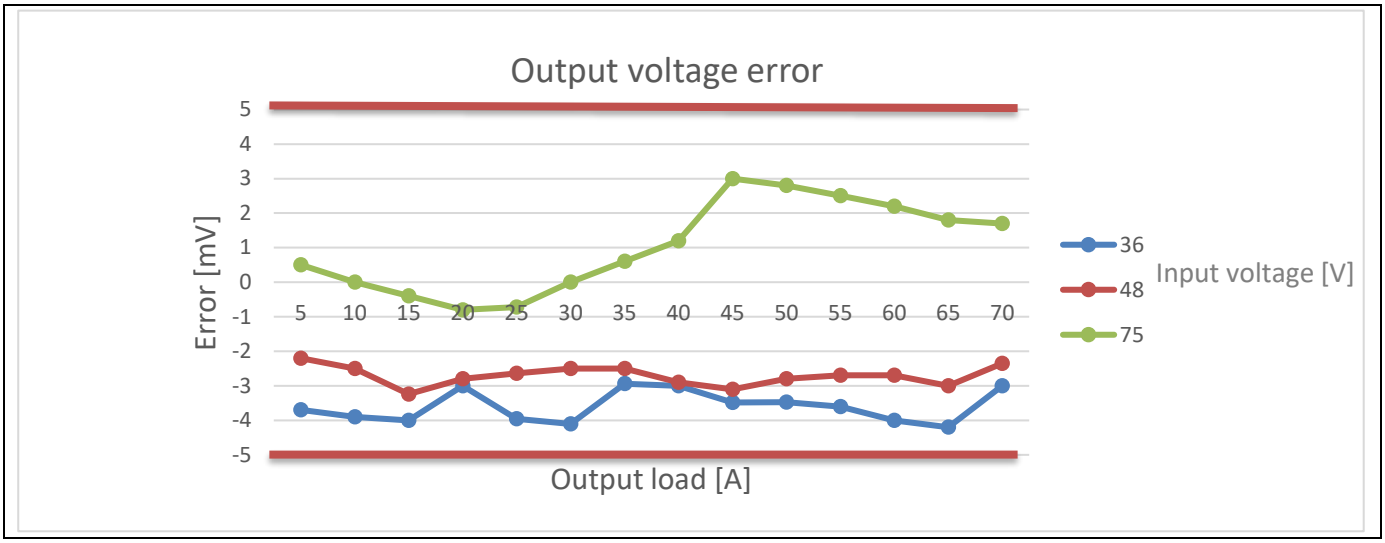


Figure 15 HB-CD output voltage accuracy

5.4.2 Input voltage telemetry

In this design, the input voltage information is taken from the pair of XDPP1100-Q040 pins VRSEN/VRREF, directly connected to the input voltage source through voltage divider.

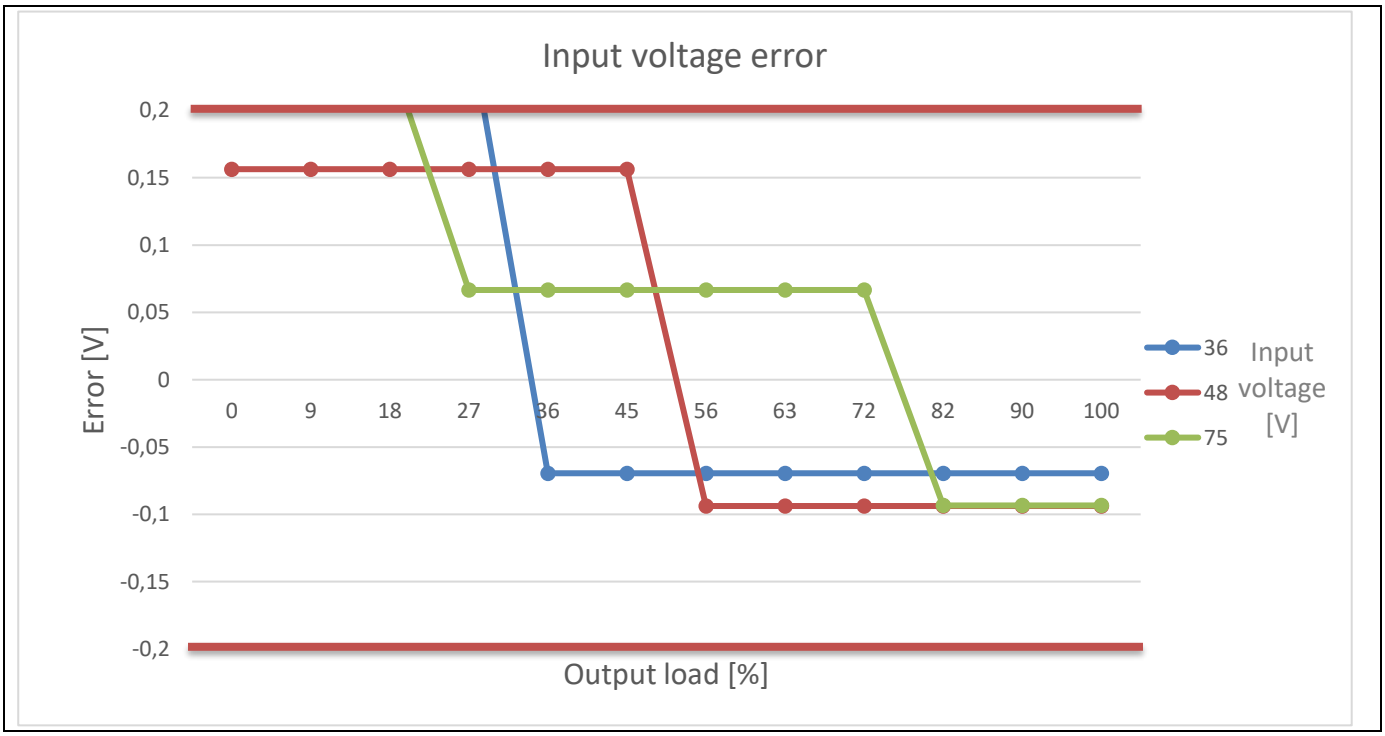


Figure 16 Accuracy of the input voltage telemetry

5.4.3 Output current telemetry

The current sense ADC is a 9-bit ADC with 25 MHz sampling rate. Exceptional noise immunity is achieved by the use of the internal current estimator. This design uses PCB copper trace (0.15 mΩ) to sense HB-CD output current via the BISEN/BIREF pins; however, a SMD current sense resistor (0.5 mΩ) is in use by ISEN/IREF for buck I_{OUTB} accordingly. **Figure 17** and **Figure 18** show the output current telemetry accuracy of the design.

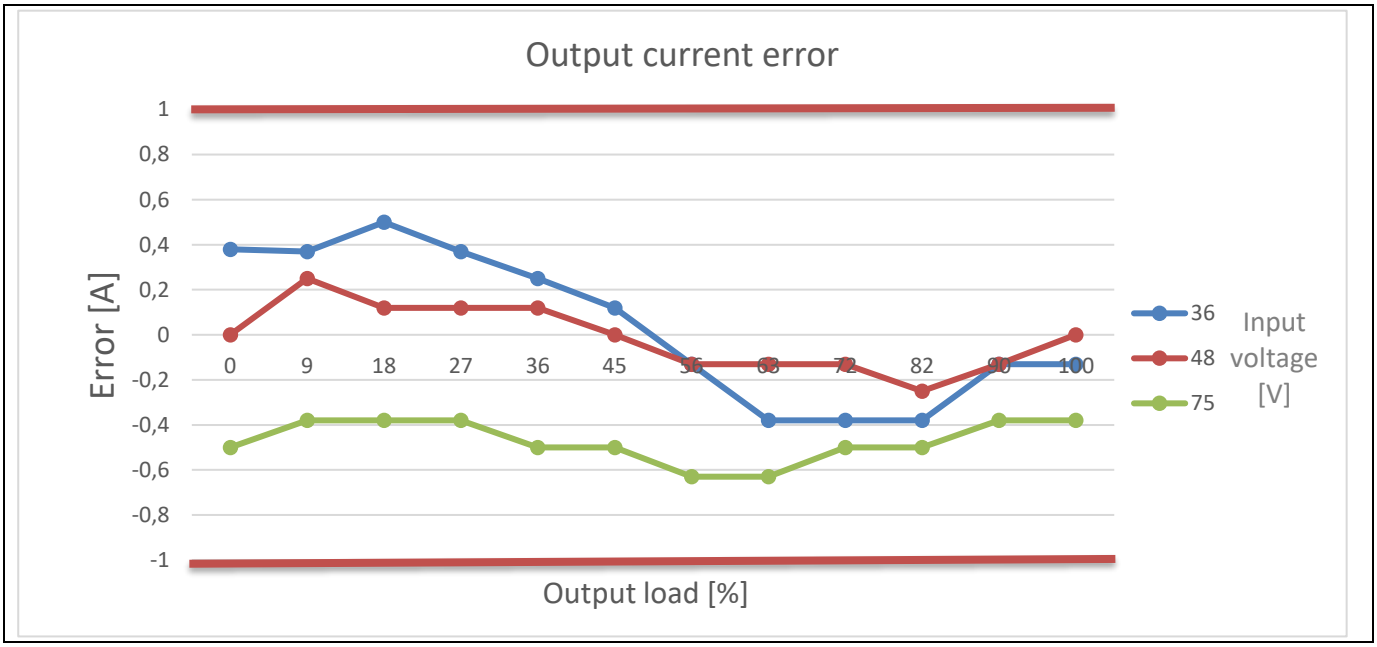


Figure 17 Buck output current error for 36 V to 75 V input voltage

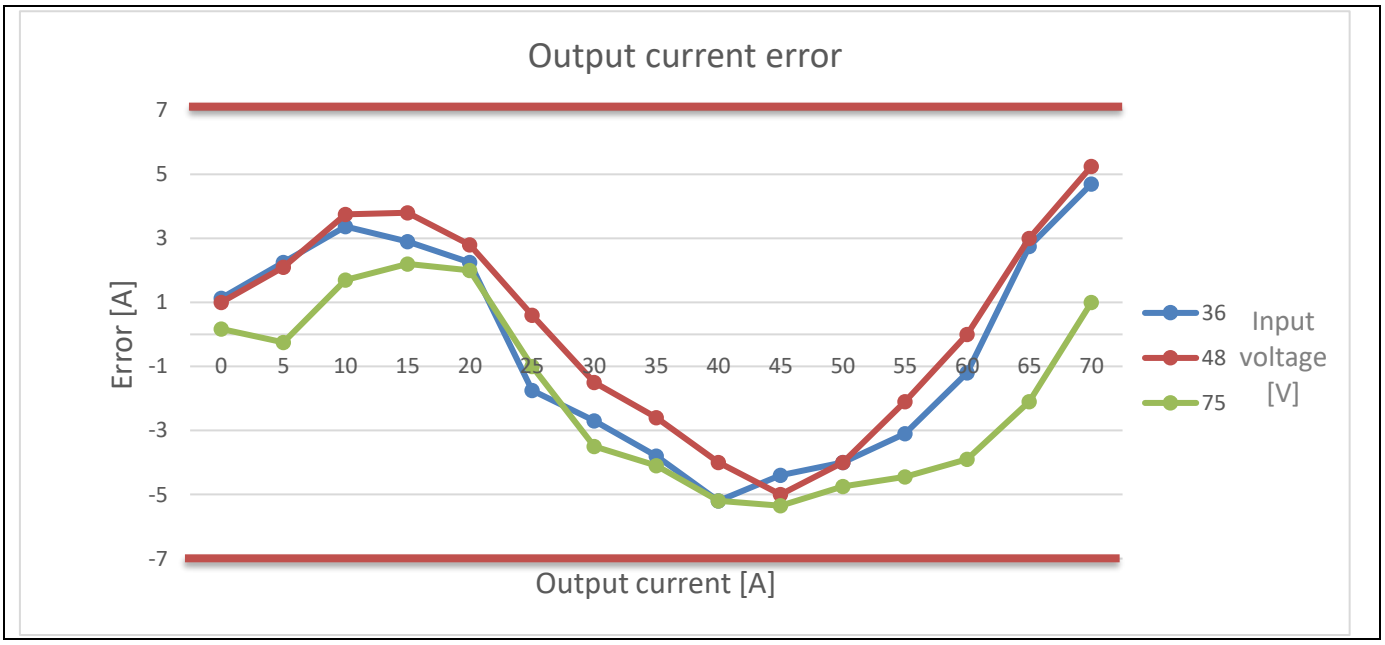


Figure 18 HB-CD output current error for 36 V to 75 V input voltage

The current read with temperature compensation is enabled. The temperature is compensated with a fixed coefficient 0.0039.

5.4.4 Input current telemetry

Input current estimation is based on the output power and the input voltage (tlm0_iin_src_sel = 2). The power read with temperature compensation is enabled. A targeted error range of the input current ±5 percent (±0.15 A) was achieved in this design.

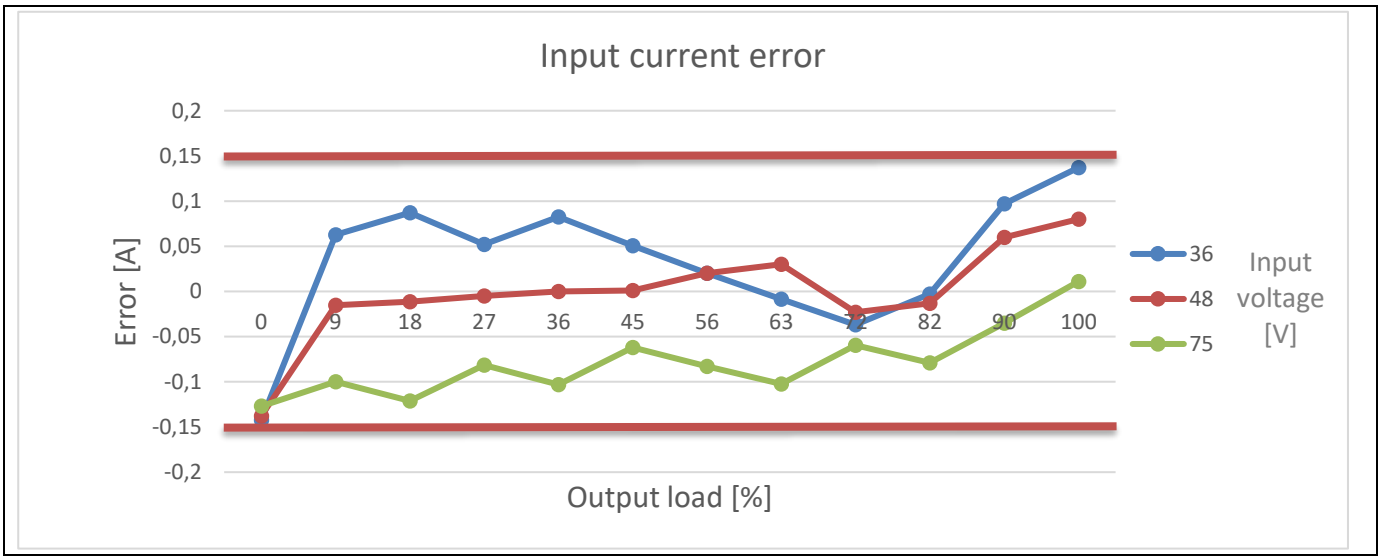


Figure 19 Input current telemetry accuracy

5.4.5 Temperature telemetry

To test temperature telemetry, the unit was heated up by itself during high output power while reading the board temperature through the XDPP1100-Q040 controller without fans to check its own maximum heating temperature and performance. The board was tested at high input voltage of 75 V DC and 11 A and 70 A output load for buck and HB-CD respectively.

5.5 Output voltage ripple

The REF_XDP_48V_to_PoL achieved ±1 percent ripple from targeted output voltage. Output voltage ripple was measured at the tip-and-barrel test point at 20 MHz BW. The ripple shown below (**Figure 20**) is 10 mV for the HB-CD output and (**Figure 21**) 95 mV for the buck output (within ±1 percent).

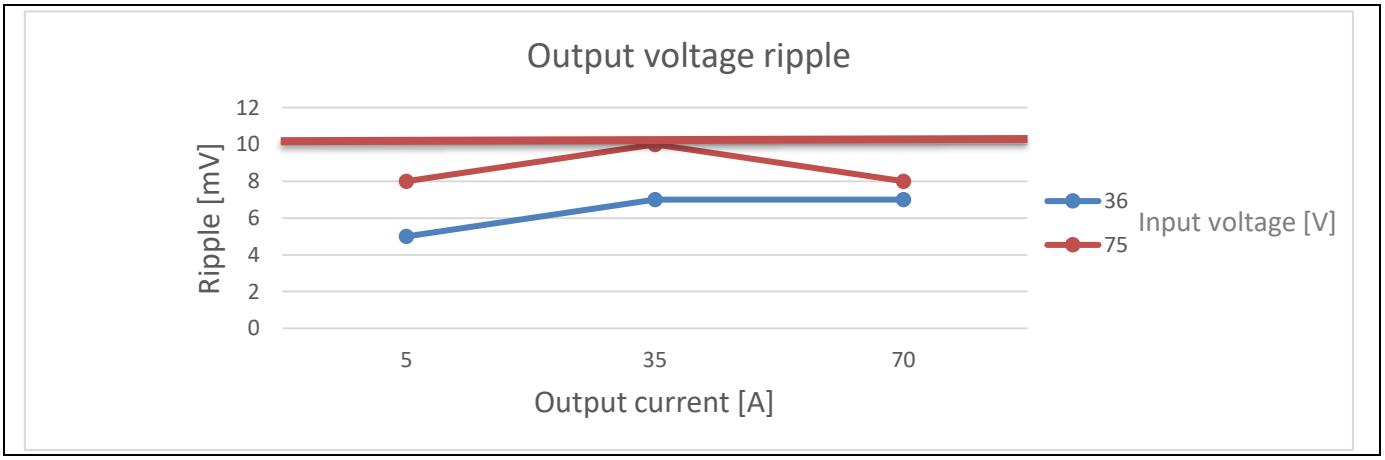


Figure 20 HB-CD output voltage ripple

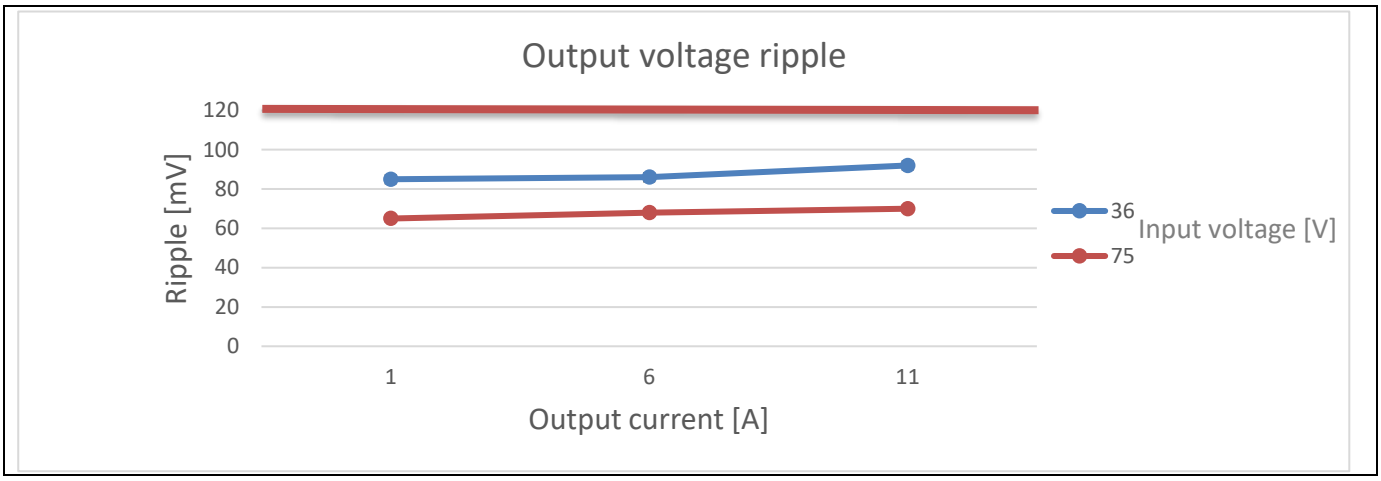


Figure 21 Buck output voltage ripple

5.6 Load regulation

The charts in **Figure 22** and **Figure 24** show the maximum peak-to-peak (P2P) response during output voltage transient for different changes in output load. Explanation of pictures below: “10 percent to 50 percent step” means the output load step from 1 A (10 percent load) to 6 A (50 percent load) with a 0.1 A/µs slope. There is an overshoot, if P2P is positive; and undershoot, if P2P is negative.

Maximum P2P values: 230 mV (**Figure 23**) and 40 mV (**Figure 25**) are within 5 percent of targeted output voltage for both the buck and the HB-CD. In turn, transient time is up to 300 µs and 1 ms accordingly.

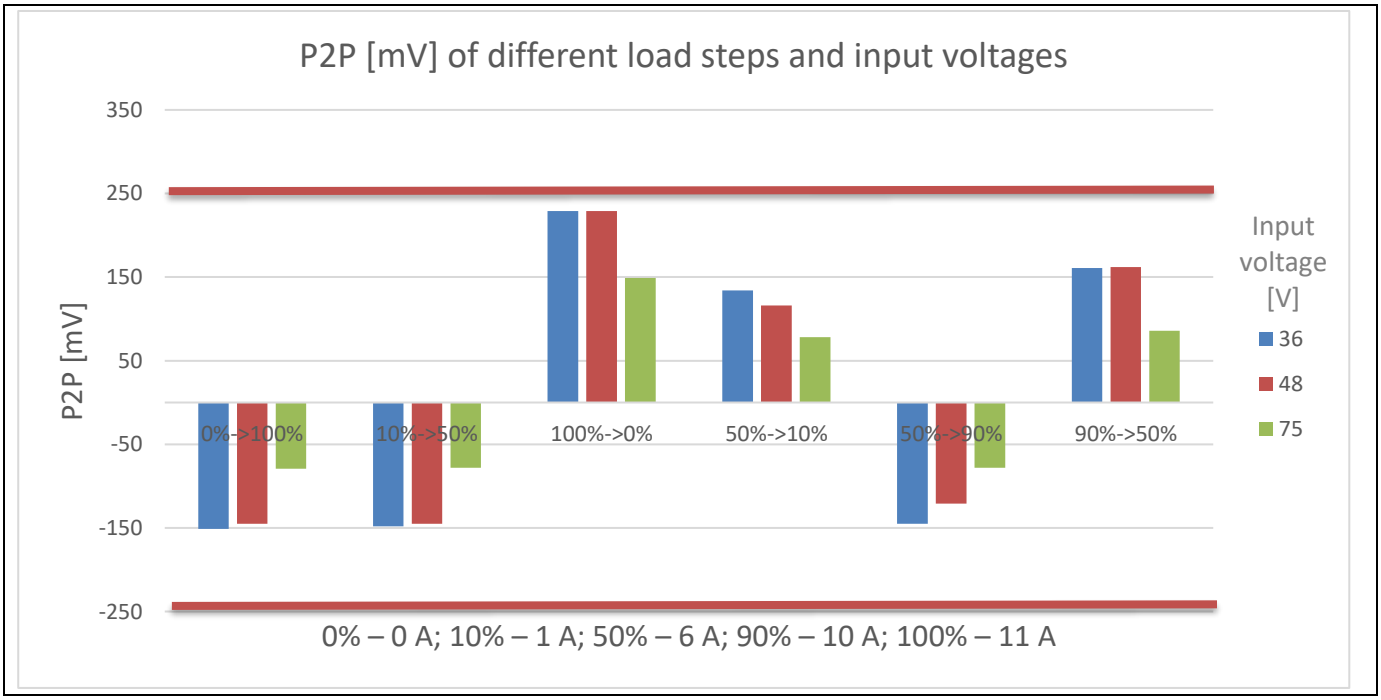


Figure 22 Buck P2P of different load steps and input voltages (36 V to 75 V)

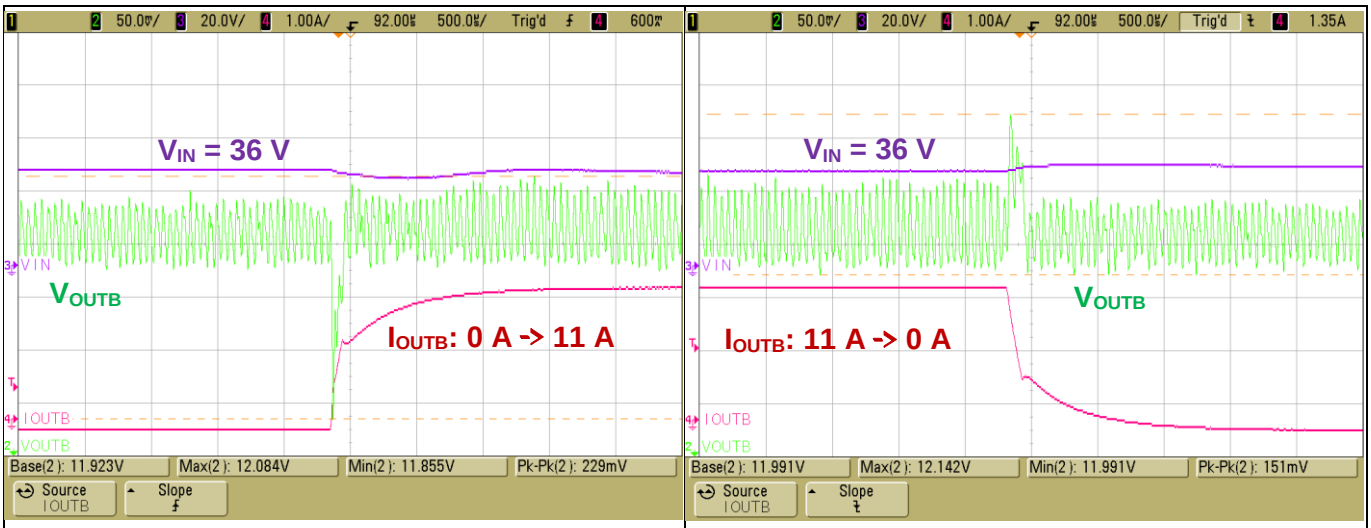


Figure 23a: Output load transient from 0 A to 11 A

Figure 23b: Output load transient from 11 A to 0 A

Figure 23 Extreme buck load transient during 36 V input voltage

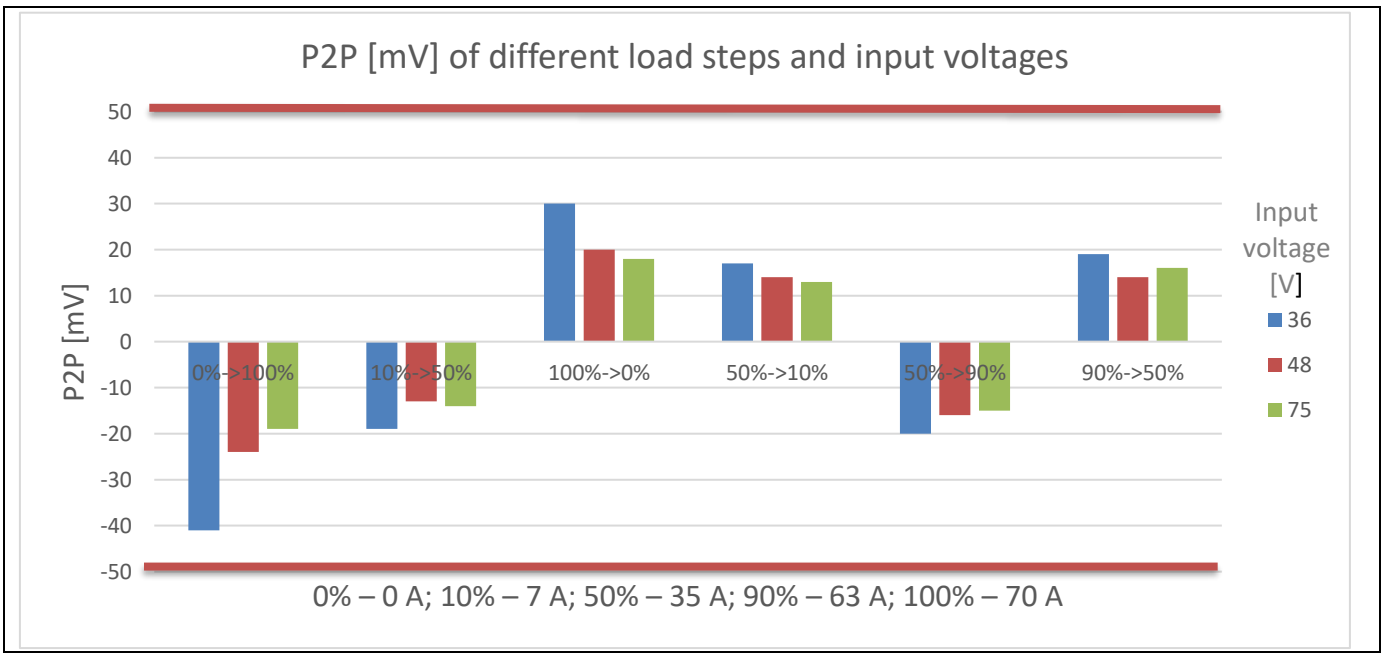


Figure 24 HB-CD P2P of different load steps and input voltages (36 V to 75 V)

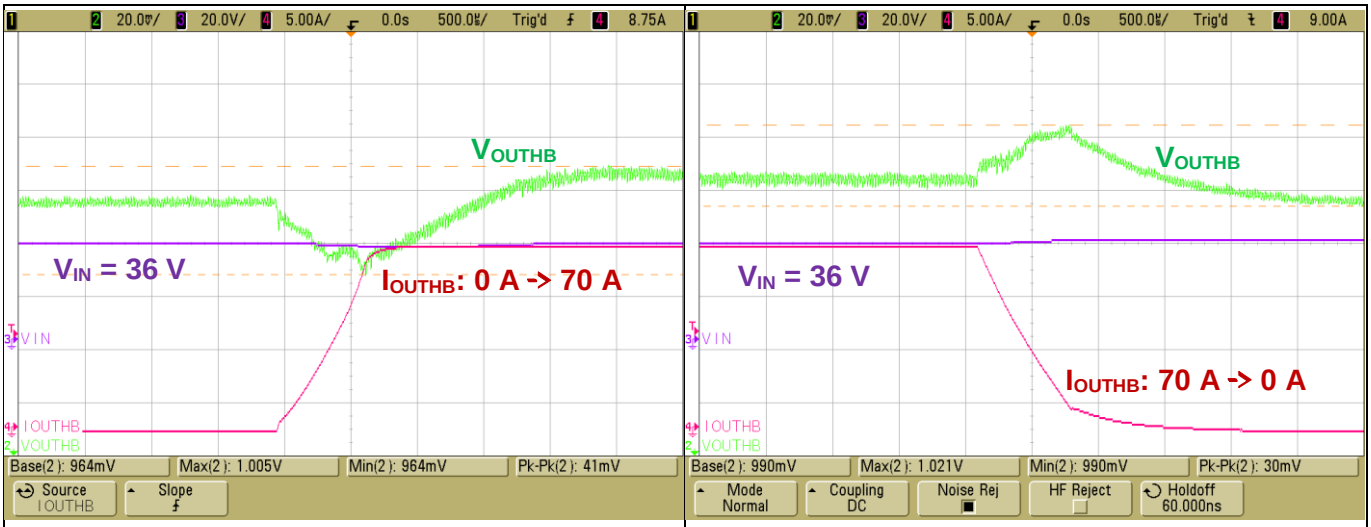


Figure 24a: Output load transient from 0 A to 70 A

Figure 24b: Output load transient from 0 A to 70 A

Figure 25 Extreme HB-CD load transient during 36 V input voltage

5.7 Protection

Fault performance is shown in the figures below. For instance, OCP and OVP/UVP are presented as major protection faults.

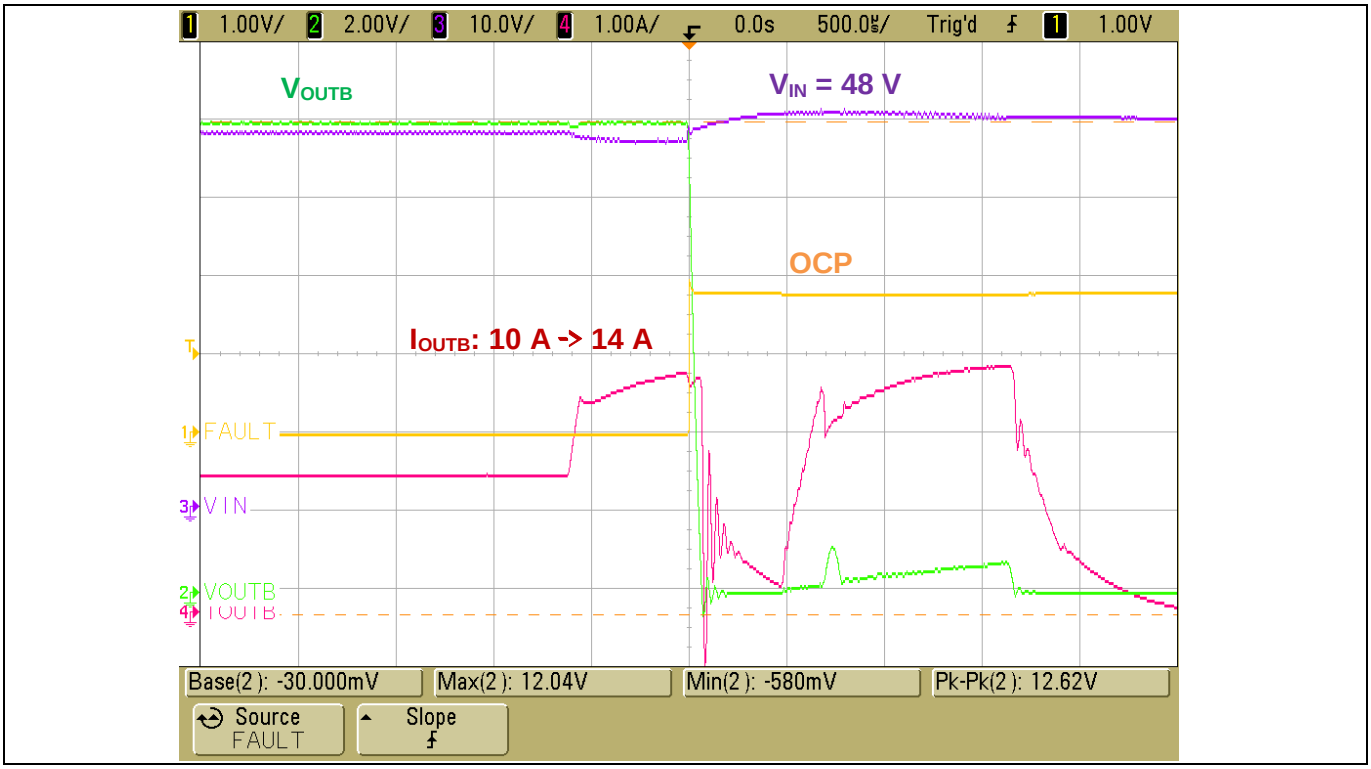


Figure 26 Output current protection (OCP threshold = 12 A) waveform, where OCP – fault pin triggering

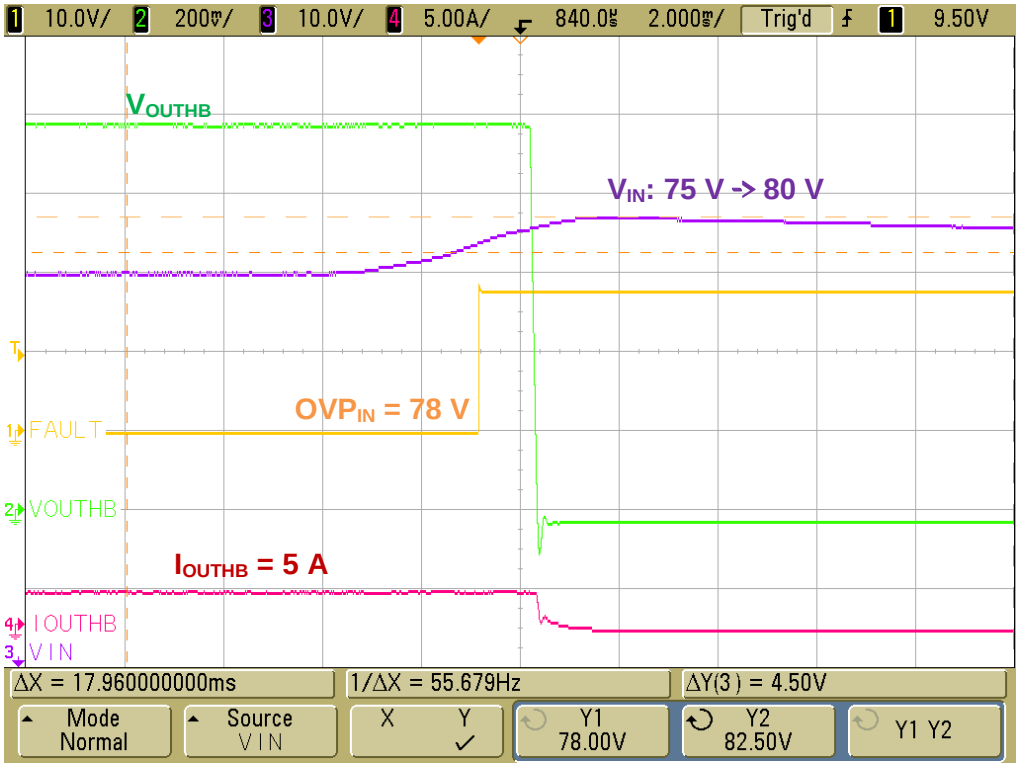


Figure 27a: Input voltage was forced from 75 V to 80 V. OVP input threshold = 78 V.

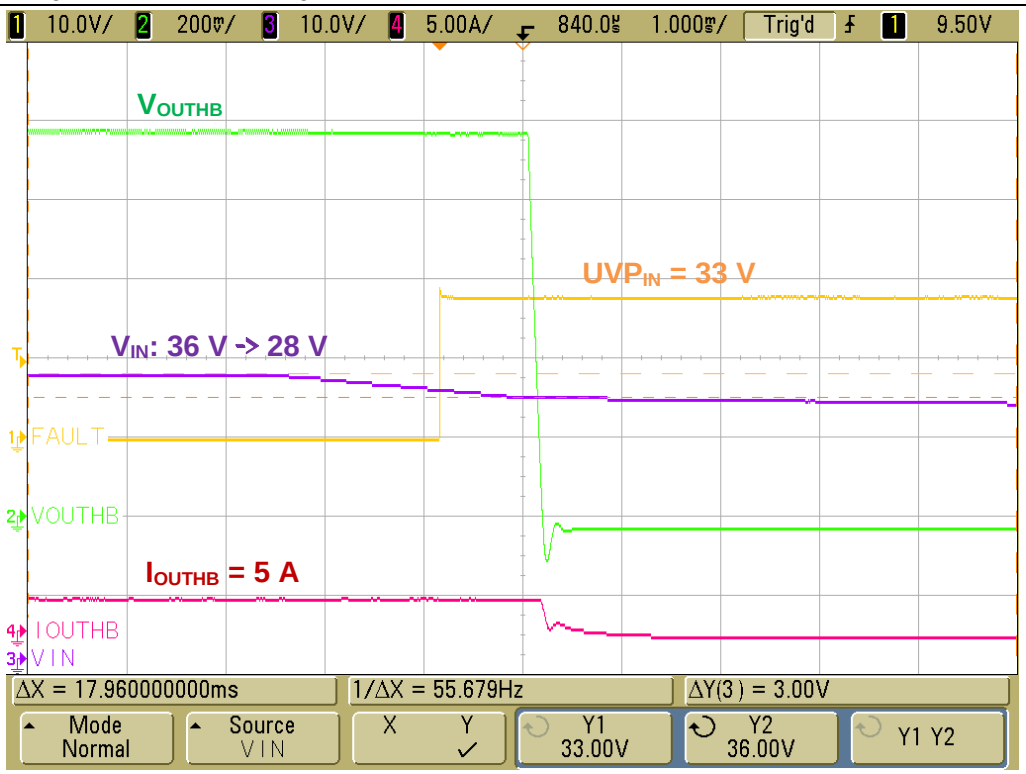


Figure 27b: Input voltage was forced from 36 V to 28 V. UVP input threshold = 33 V.

Figure 27 Input voltage protection waveforms: OVP_{IN}/UVP_{IN} – fault pin triggering

6 Summary

Nowadays, there is a huge demand for new, more efficient, compact and innovative power supply solutions, especially in core PoL supply, due to upcoming 5G, AI and other high-power technologies. Those innovations require high-current CPUs and GPUs to process billions and billions of operations within just a few seconds within IC voltages as low as 1 V. As shown in this document, the medium-voltage PoL REF_XDP_48V_to_PoL reference design is presented as a system solution for telecom and data centers as a unique setup, which combines the benefits of non-isolated SMPS, and eliminates the switching losses of a conventional two-stage solution, while providing a cost-effective single-stage 48 V-to-PoL. It has a unique architecture that includes many optimized power-processing digital blocks to enhance the performance of isolated and non-isolated DC-DC converters, reduce external components and minimize FW development effort.

The flexibility of this design is made possible by the XDPP1100 device, a fully programmable digital power controller, which enables hybrid architectures of intermediate bus and direct conversion with two digital loops to ensure dual-output channels with different power and voltage rates. The XDPP1100 device architecture incorporates advanced power processing algorithms to enhance system efficiency for high-frequency designs. Integrated voltage and current sense ADCs provide best FF and same-cycle response for optimal line-/load-transient performance.

In order to achieve the highest levels of efficiency, XDPP1100 is combined with the latest, best-in-class Infineon devices with their benchmark low $R_{DS(on)}$ and low parasitics. OptiMOS™ 5 power transistors are the latest and best-performing low parasitic devices from Infineon, with an optimized layout and driving circuitry, to achieve incomparable performance with minimum stress on the devices. OptiMOS™ FETs are driven by Infineon's EiceDRIVER™ gate drivers, which have protection features such as fast short-circuit protection (DESAT), active Miller clamp, shoot-through protection, fault, shutdown, and overcurrent protection. In turn, the DHP1050N10N5 power stage acts as a complete symmetrical half-bridge power solution, which brings all its OptiMOS™ 5 benefits.

Specific power management peripherals have been added to enable high efficiency across the entire operating range, high integration for increased power density, reliability, and lowest overall system cost. Such peripherals include: synchronous rectification, input voltage FF, copper trace current sense with temperature compensation, ideal diode emulation, soft-start, feedback loop open- or short-circuit protection, and fast load-transient response.

With all of the described properties and results shown above, REF_XDP_48V_to_PoL has proved its suitability as an appropriate power solution, and its usefulness for engineers who would like to achieve the best results and make this world greener.

References

[1] See the code examples at **www.infineon.com**

[2] **XDPP1100 datasheet**

[3] **XDPP1100 product brief**

Revision history

Document version	Date of release	Description of changes
V 1.0	08-10-2020	First release

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