

DB359 Demo Board Performance Data and Infrastructure for Xilinx Versal Power Delivery

www.infineon.com/power-versal

V1.0

May 13, 2019



Portfolio: Infineon Power Solutions for Xilinx Versal™



Part Number	Feature Description	Proven Solutions & Application Benefits
IR35215MTRPBF Controlled document upon request	Dual-loop digital multi-phase buck controller	Vcore at high current and current transient designs; 8+0, 4+4 loop design options; PMBus/I2C
TDA21472 Controlled document upon request	OptiMOS 5 high current (70A) and high efficiency power stage in 5x6x0.9mm ³ PQFN	Output current capability > 70A; Integrated current and temperature sense, reporting and protection; Boot refresh; HS short protection; Excellent efficiency; up to 1.5MHz
IRPS5401	5-output PMIC, 4 DC-DC (2A, 4A, 8A, PWM for external powerstage) + 1 LDO (0.5A, tracking option), 5W to 50W	Compact design for multiple rails; Integrated sequencer; Integrated FETs; Use with ext. power stage optional; Digital compensation; PMBus/I2C
TDA21240 TDA21242	OptiMOS 5 Power-Stages 25A and 40A in 4mm x 4mm package; high efficiency	FPGA/SoC; best solution for size and efficiency in the market
IR38060, IR38062, IR38063, IR38064	Integrated FET regulators for 6A to 35A	Vcore and SERDES for Xilinx; Excellent thermal performance; PMBus/I2C with integrated sequencer, Fault mgmt., Telemetry
IR3897, IR3898	Integrated FET regulators for 4A and 6A	DDR3/DDR4 tracking +/-4A and +/-6A VTT
IR3883	Integrated FET regulator for 3A	Xilinx VCCIO voltages; low cost
IR3887, IR3889	New 30A High efficiency integrated FET regulators – releasing June 2019	Excellent performance; Efficiency > 90% at load and over temperature
IFX1763	Low Noise LDO	2.5V for Xilinx ZYNQ Ultrascale+ RFSoc
IFX54441	Low Noise LDO	1.8V SERDES for Xilinx ZYNQ Ultrascale+ MPSoC
IR3823	Low Noise analog DC/DC regulator	1.2V SERDES for Xilinx ZYNQ Ultrascale+ FPGAs

-
- Capacitors used for test:
- 10x 560uF
 - 50x 47uF
- Phase inductors for test:
- 5x 100nH/120nH
- 35x 47uF
- 130x 10uF
- 26x 47uF
- 3x 120nH
- 16x 470uF
- 4x 470uF + 14x 47uF
- Infineon DB359 REV 0 8 PLUS 2 DEMO BOARD

Demo Board: DB359 Test Setup: 2 Loops (5-Phases + 2 Phases)

Intel Voltage
Regulator
Transient Test
Tool

Test Conditions:

VID=0.7V

Loop 1:

I_{out}: 120A...165A

Transient steps:

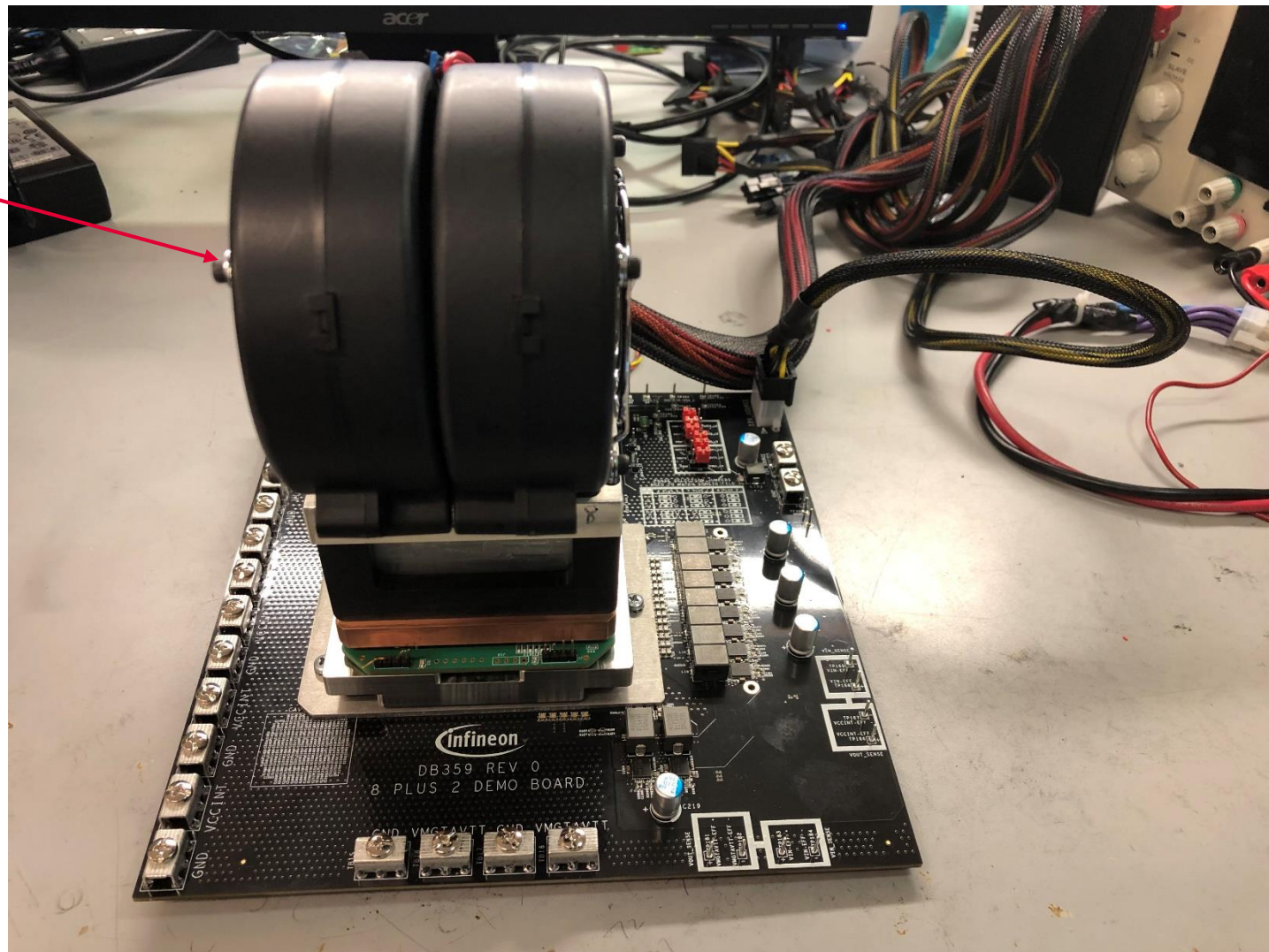
30A...90A at 200A/us

Loop 2:

I_{out}: 25A

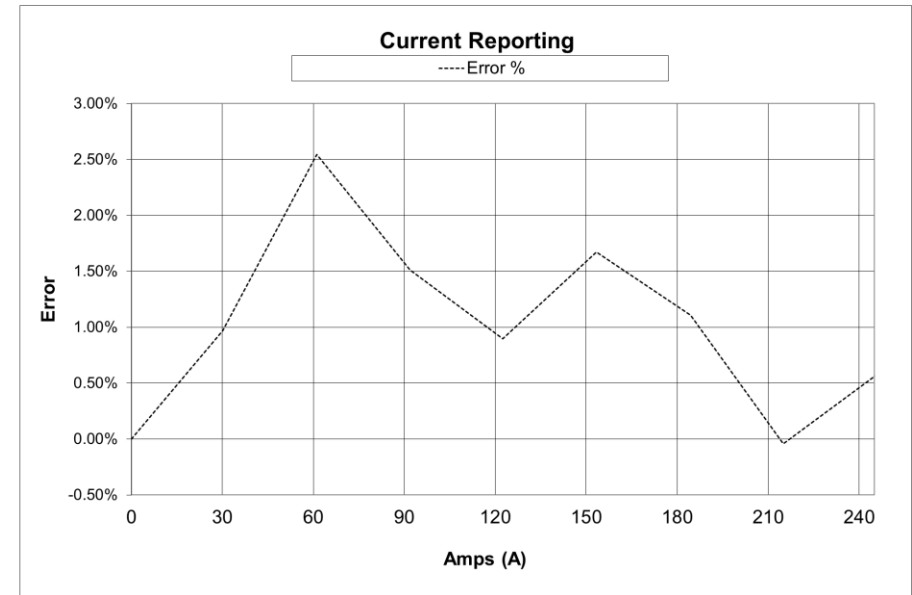
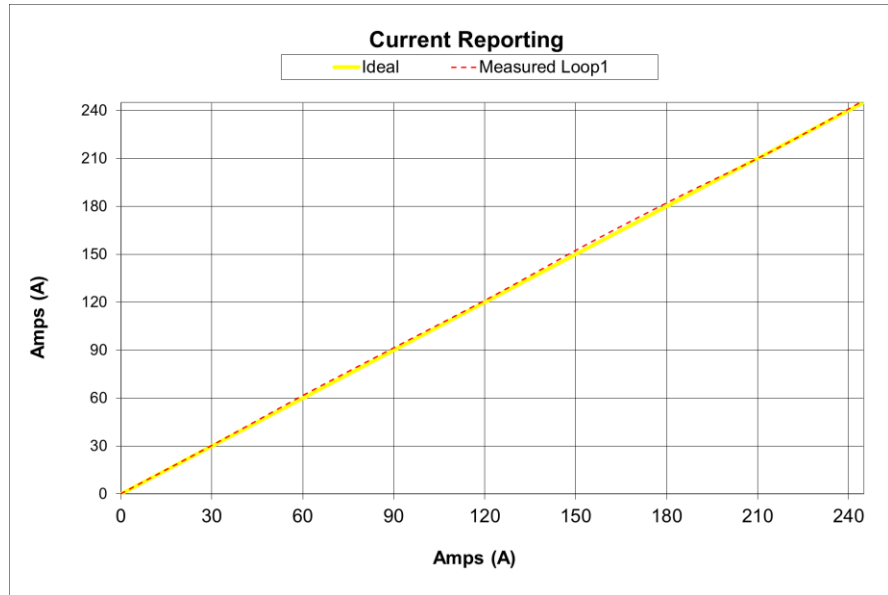
Transient step: 35A

at 200A/us

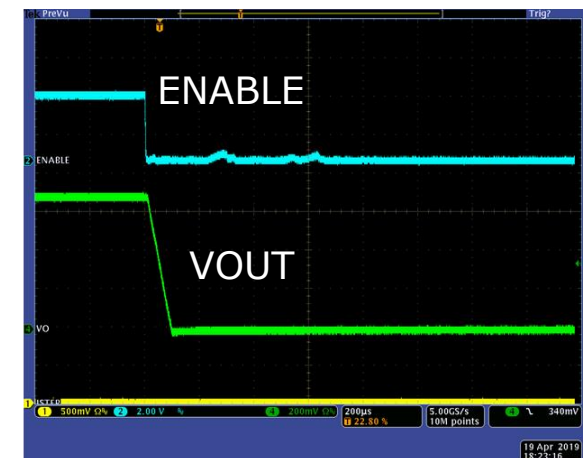
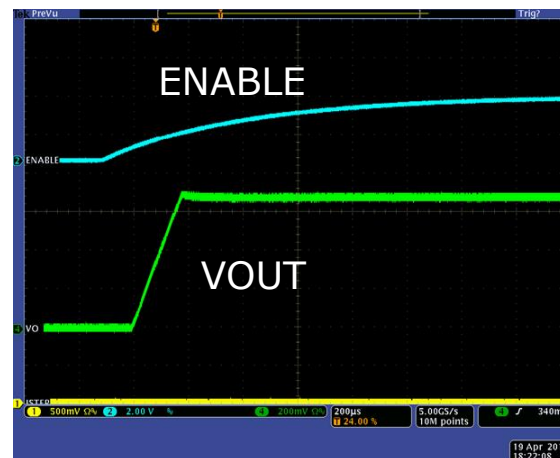


Demo Board: DB359 Loop 1, 5-Phase Performance Results

Current reporting accuracy:



Startup/Shutdown:



Demo Board: DB359 Loop 1, 5-Phase Performance Results

Transient step 90A-150A at 200A/us:



Transient step 60A-150A at 200A/us:

Decoupling:

10x 560uF/3mΩ POSCAP

50x 47uF/0805

260x 10uF/0402 (cavity)

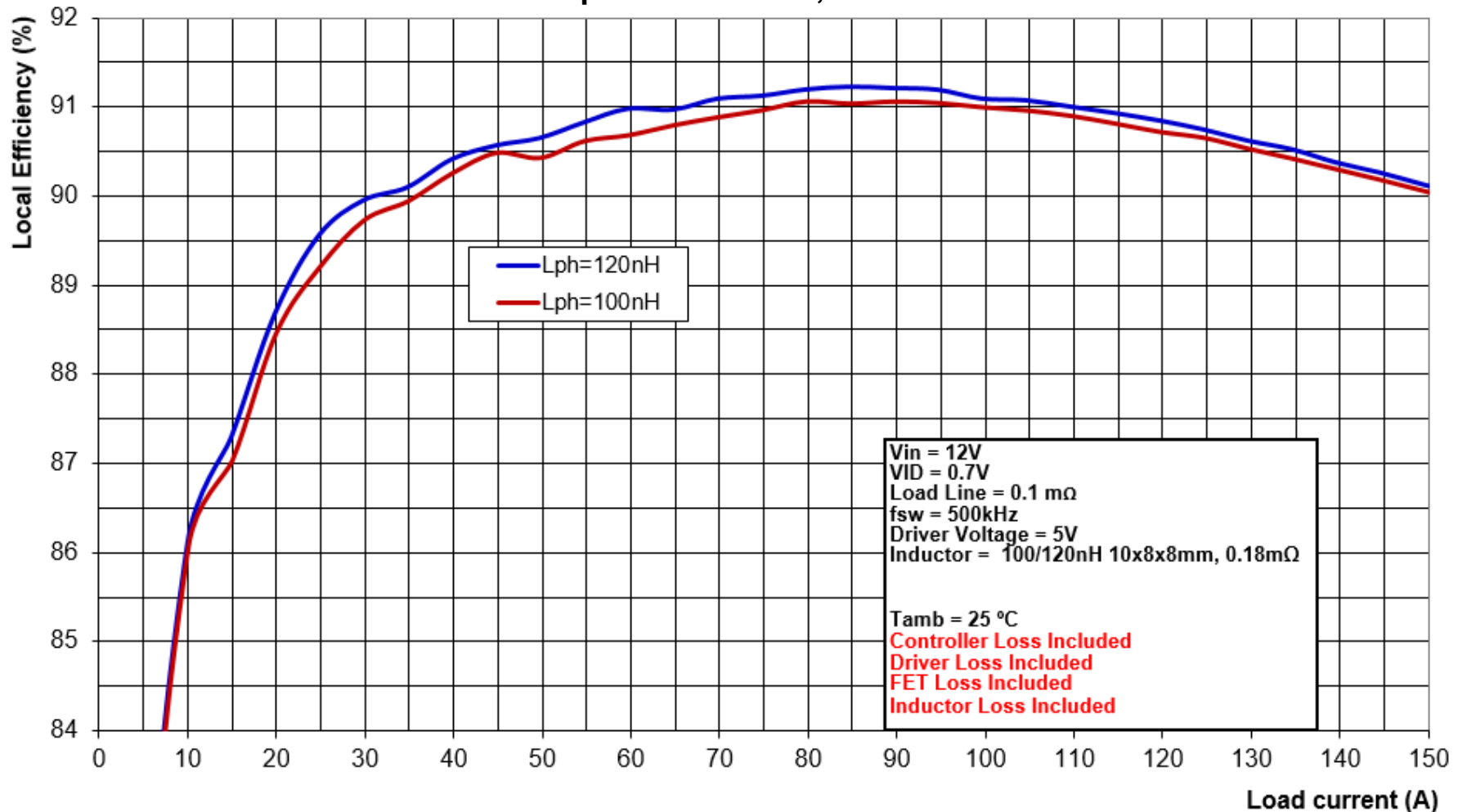


Demo Board: DB359 Loop 1, 5-Phase Performance Results



> Efficiency

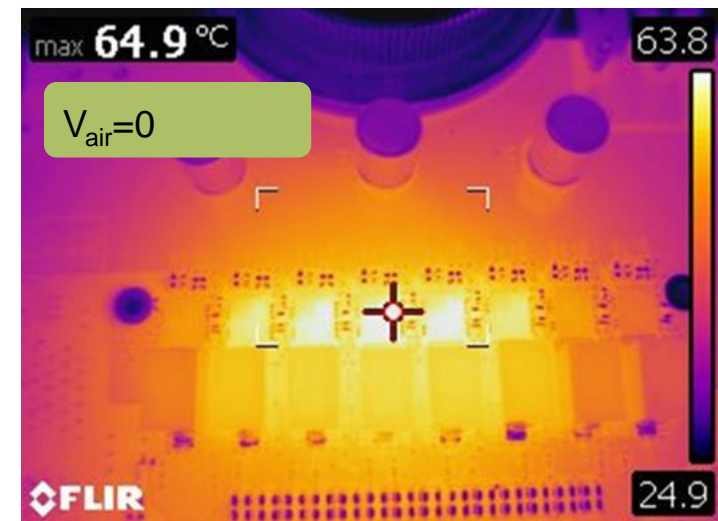
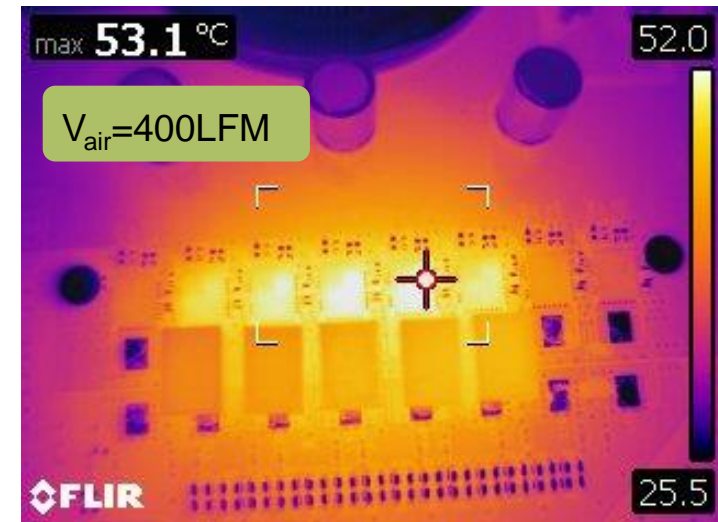
DB359 Rev 0, 5 Phases, TDA21472, 0.1 m Ω LL, Output voltage 0.7V,
100nH/120nH phase inductors, TDC=150A



The board has been tested up to 240A output current with only 5 phases enabled.
The power loss at 240A is 26W.

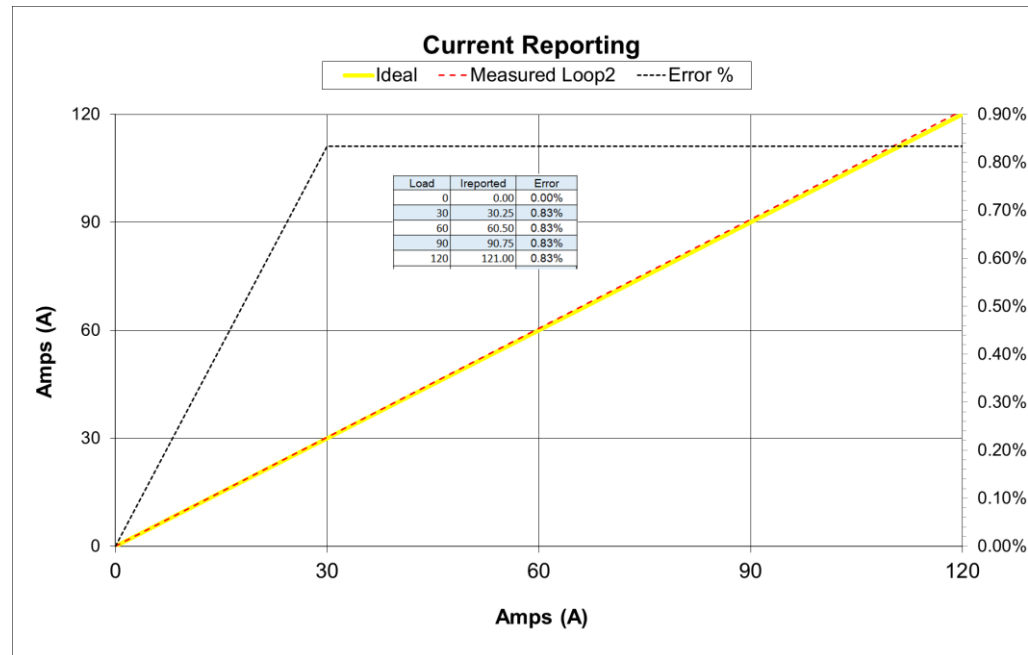
Demo Board: DB359 Loop 1, 5-Phase Performance Results

- › Operating conditions:
 - 5 Phases, TDA21472
 - $LL=0.1m\Omega$
 - $V_{out}=0.7V$
 - $f_{sw}=500kHz$
 - $I_{out}=150A$
 - $L_{ph}=100nH$
 - $T_a=25^\circ C$
 - No heatsink
- › Thermal data taken after 10 min soaking at 150A load current

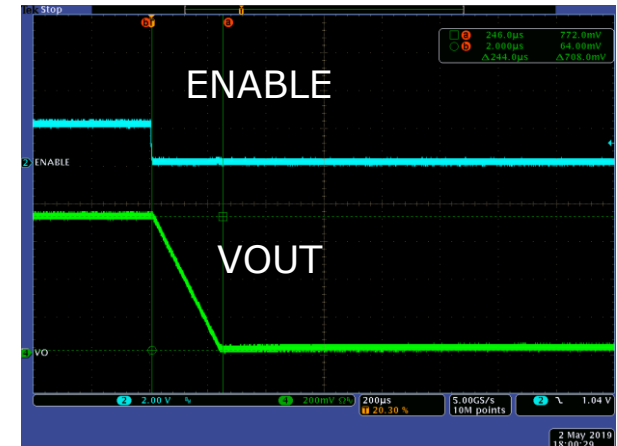
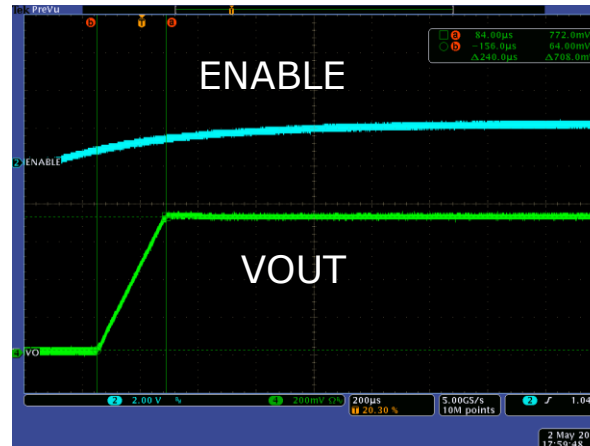


Demo Board: DB359 Loop 2, 2-Phase Performance Results

Current reporting accuracy:



Startup/Shutdown:

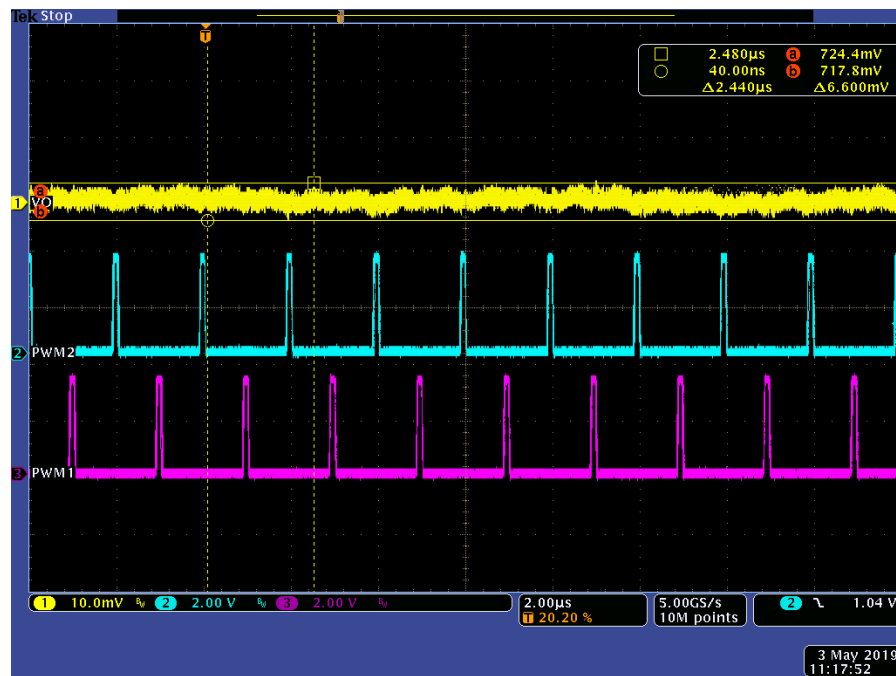


Demo Board: DB359 Loop 2, 2-Phase Performance Results

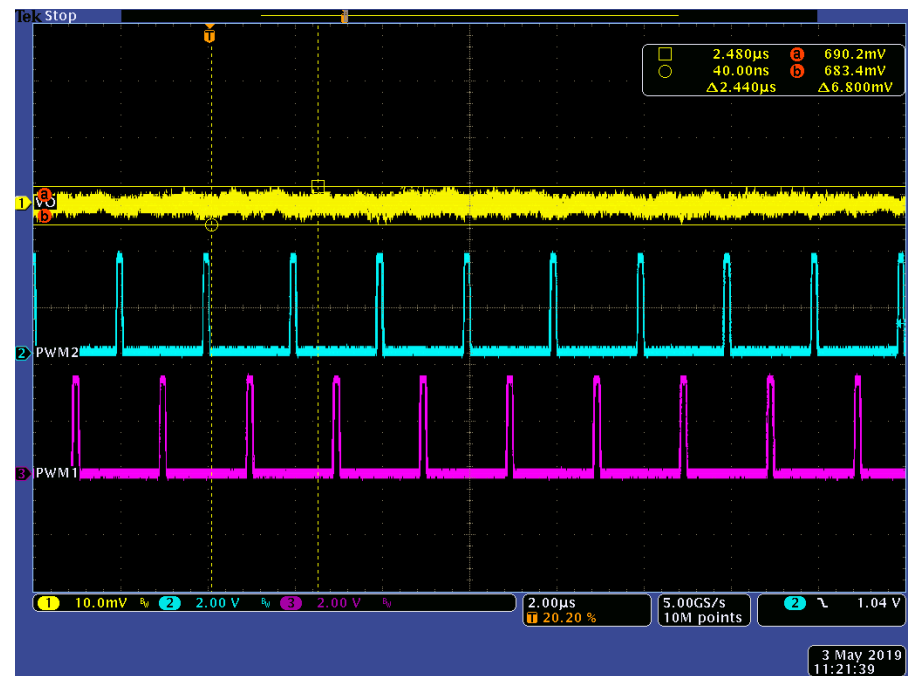


› Steady State Ripple

No Load



60A Load Current

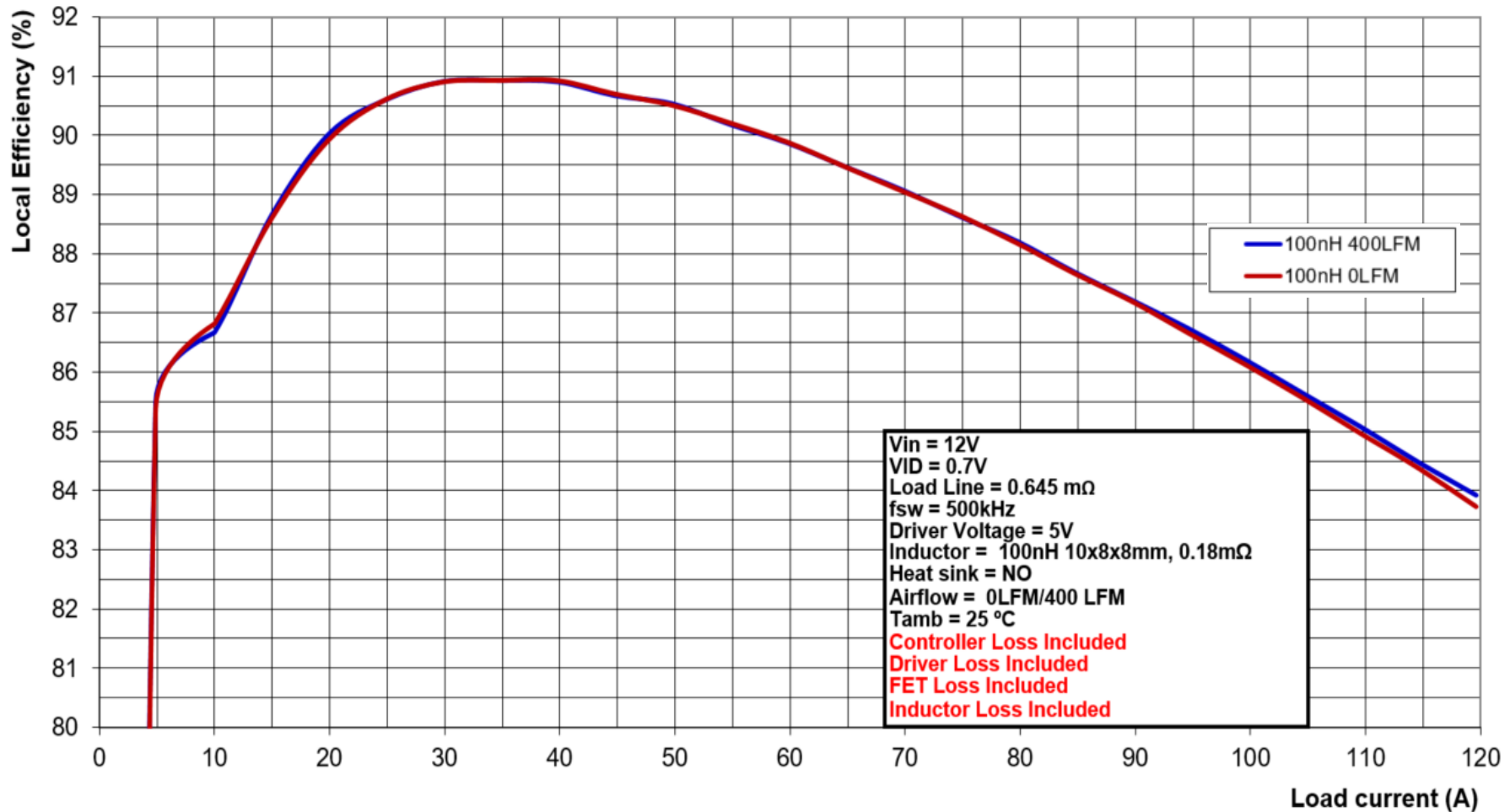


Demo Board: DB359 Loop 2, 2-Phase Performance Results



> Efficiency

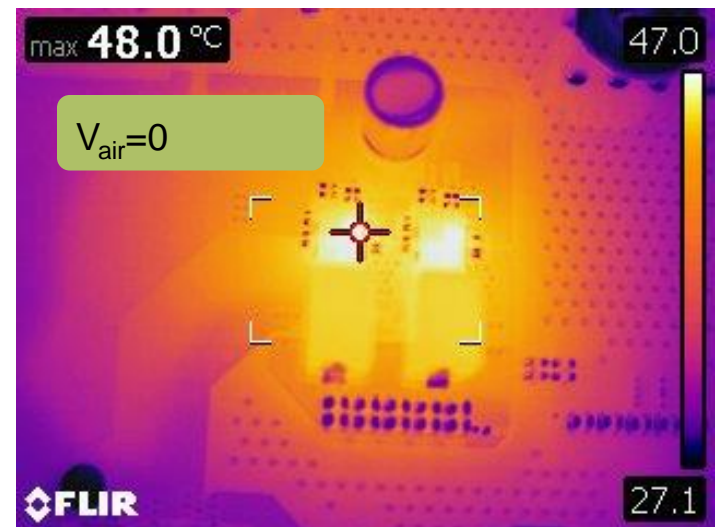
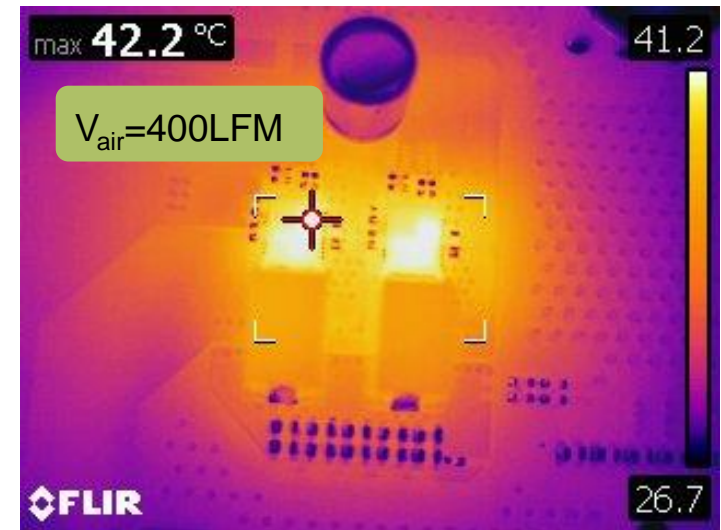
DB359 Rev 0, 2 Phases, TDA21472, 0.645 mΩ LL Output voltage 0.7V,
100nH phase inductor, TDC=60A



The board has been tested up to 120A output current with 2 phases enabled. The power loss at 120A is 15.3W.

Demo Board: DB359 Loop 2, 2-Phase Performance Results

- › Operating conditions:
 - 2 Phases, TDA21472
 - $LL=0.645m\Omega$
 - $V_{out}=0.7V$
 - $f_{sw}=500kHz$
 - $I_{out}=60A$
 - $L_{ph}=100nH$
 - $T_a=25^\circ C$
 - No heatsink
- › Thermal data taken after 10 min soaking at 60A load current



Multiphase: Multiphase Controllers & Power Stages



Reasons to use MultiPhase solutions:

- › Output current exceeds range for a single phase solution
- › High efficiency over wide load range
- › Better transient response
- › Smaller decoupling solution (L, C)
- › Less EMI due to smaller switched current

PowerStages on
Infineon Website:

Key features

- Small 5x6x0.9mm³ overmolded PQFN package, 0.45mm pitch
- Highly accurate current reporting
- Programmable constant current limit OCSET
- Fast switching technology for improved performance at higher frequency, better peak efficiency
- Input voltage range 4.25V to 16V
- Output voltage range from 0.25V up to 5.5V
- Output current capability up to 70A
- Operation up to 1.5MHz
- Optimized for 5V drive

Key benefits

- Peak efficiency >95%
- 2.5mA I_{CC} , with low I_Q (<200µA) disable PS4 (deep sleep mode) capability

Target applications

- [Server](#) and storage
- [Telecom](#)
- Datacom

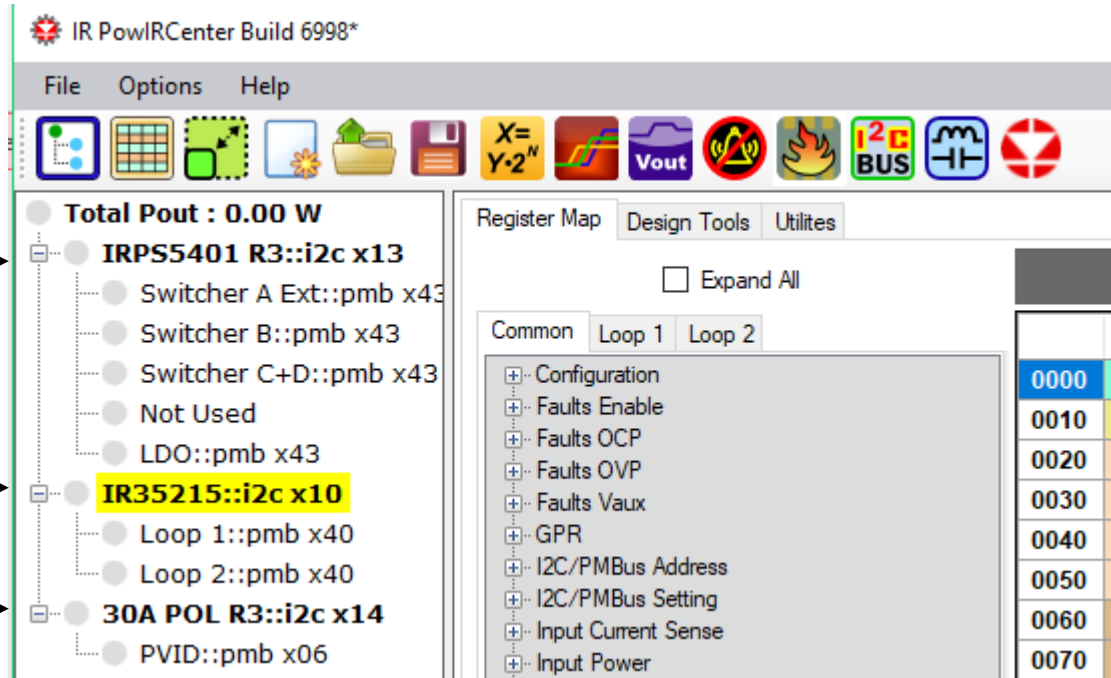
Multiphase: Multiphase Controller IR35215

- › Seamless integration with POL and PMIC devices into the same GUI

- › 5-output PMIC configured for 2 single phase switcher rails, a dual phase rail and an LDO rail

- › 2-output multiphase controller

- › 1-phase 30A POL

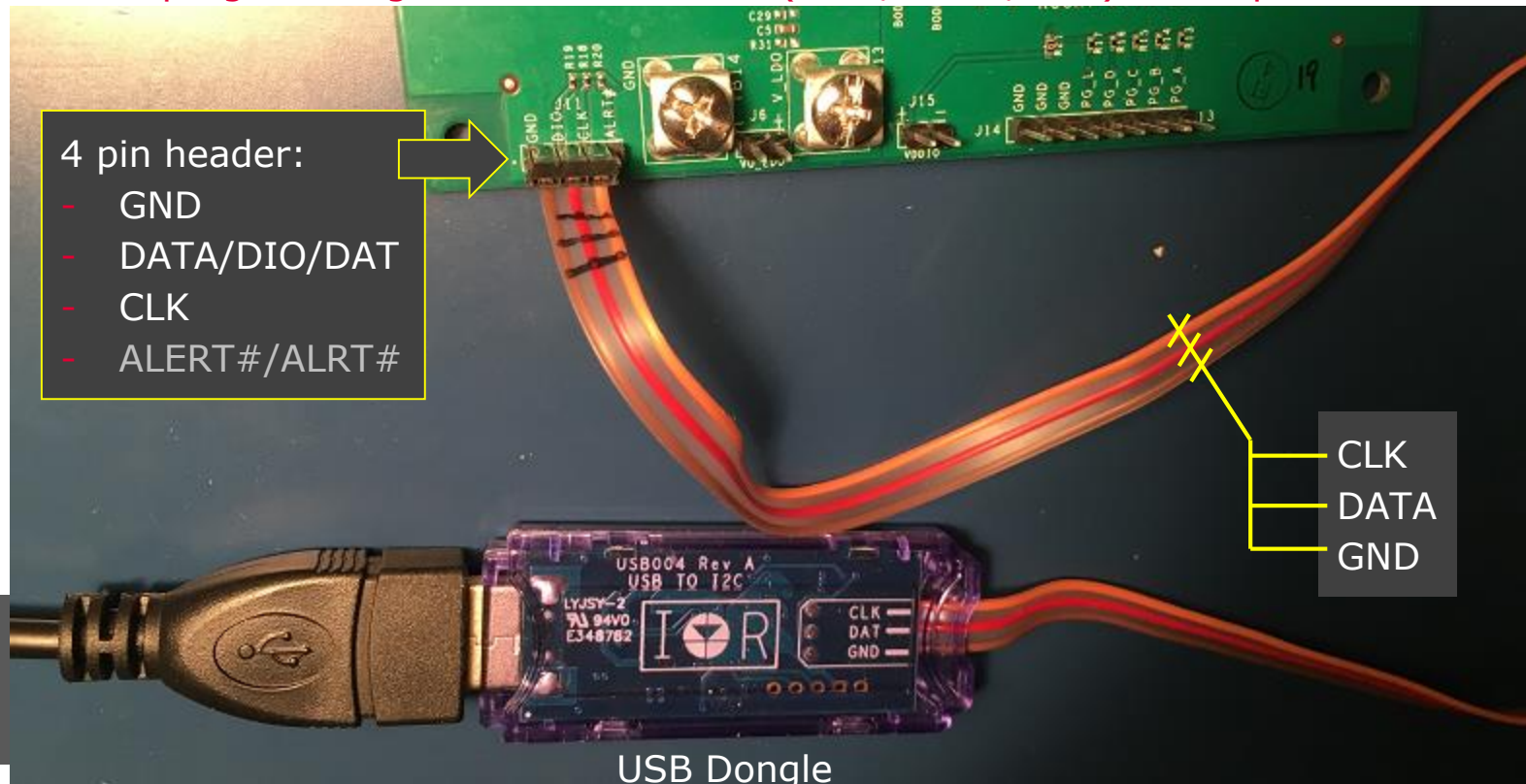


Multiphase: I2C and PMBUS Communication

USB Dongle005 connects
PC and application board



For communication and programming via I2C three wires (GND, DATA, CLK) are required.



Install header on pcb: 4 positions, breakaway connector 2.54mm (0.1") pitch

e.g. Digikey S1011E-04-ND or S1011E-36-ND (36 pins, break off 4 pins)



Multiphase: IR35215 Features



- › Established controller solution for Intel CPU regulation
- › 8/4 phase dual loop controller (2 loops configurable from 1..4+0..4, 5+0..3, 6+0..2, 7+0/1, 8+0)
 - › Active voltage positioning (load-line)
 - › 5mV VID resolution
 - › Voltage mode with active current balancing (active current sharing)
 - › Nonlinear transient support (adaptive transient algorithm)
 - › Digital compensation (no external compensation components)
 - › SVID and I2C/PMBUS
 - › Autophasing (phase shedding)
 - › Telemetry on voltage, current, power, temperature, fault protection and reporting
- › 5mm x 5mm 40-pin QFN-package
- › Digital pin-strapping to select an entire configuration from many
- › Programmable I/O pins to support additional reporting and enable functions

Multiphase: PowIRCenter, IR35215 Device Addresses

(1% tolerance)

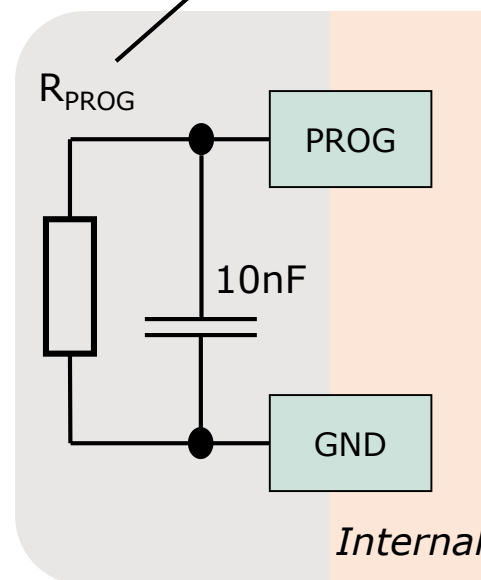
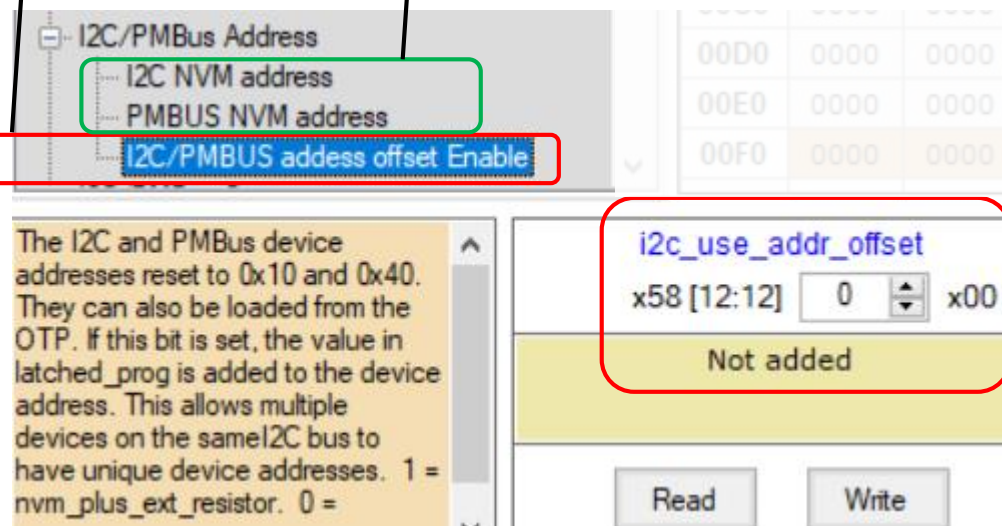
Addr. Offset	R _{PROG} [kΩ]
+0	0.845
+1	1.30
+2	1.78
+3	2.32
+4	2.87
+5	3.48
+6	4.12
+7	4.75
+8	5.49
+9	6.19
+10	6.98
+11	7.87
+12	8.87
+13	10.00
+14	11.00
+15	12.10

If $i2c_use_addr_offset=0$ then Address Offset = 0 else Address Offset = f(R_{PROG})

I2C Address = I2C NVM address + Address Offset

PMBUS Address = PMBUS NVM address + Address Offset

GUI:



Note: The offset for PMBUS and I2C bus is always identical.

Multiphase: IR35215 Multiple Image Files and Segment Selection by PROG Pin Resistor

Example 1:

A .MIC file with 11 configuration sections was written into NVM.

PROG_MAX has been set to the value of 11. The PROG resistor of 5.49 kΩ selects configuration section 9 to be loaded and used.

No further .MIC file can be programmed.

A subsequent programming of a new configuration writes into section 12 which is then being used. Another 15 sections remain free for possible single configuration writes.

(1% tolerance)

Config Offset	.MIC file	R _{PROG} value [kΩ]	Single MTP write
+0	1	0.845	1
+1	2	1.3	2
+2	3	1.78	3
+3	4	2.32	4
+4	5	2.87	5
+5	6	3.48	6
+6	7	4.12	7
+7	8	4.75	8
+8	9	5.49	9
+9	10	6.19	10
+10	11	6.98	11
+11	12	7.87	12
+12	13	8.87	13
+13	14	10	14
+14	15	11	15
+15			16
+16			17
+17			18
+...			...
+26			27

15 sections

Example 2:

The first write into NVM was a single configuration

No .MIC file can be programmed anymore.

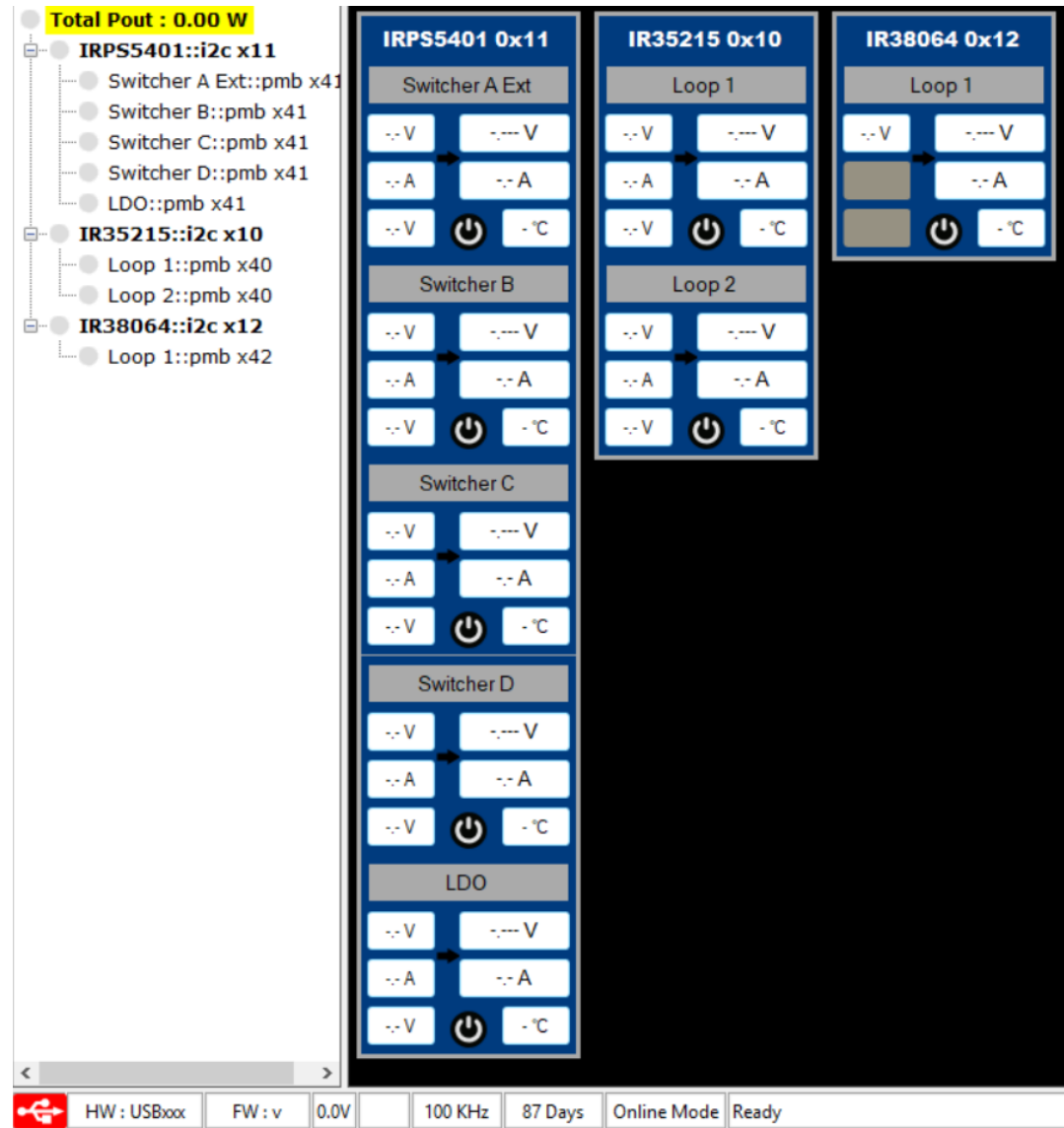
26 more single configuration writes remain available.

In general:

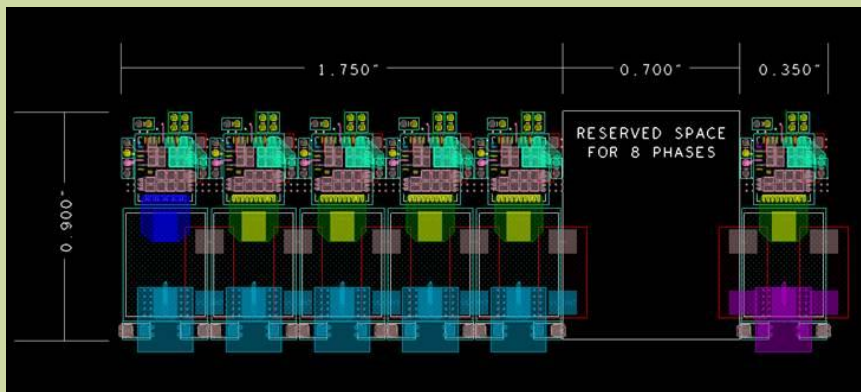
- If *prog_max* is smaller than the number of programmed segments, the last segment will be used.
- If *prog_max* is bigger than the number of programmed segments and
 - R_{PROG} points to a valid segment, this segment will be used.
 - R_{PROG} points to an unprogrammed segment, the part does not start.

Summary: One Software Interface

- › PowIRCenter GUI for all PMBUS devices
- › Reporting status of
 - Interface to board
 - PMBUS/I2C addresses
 - Vin
 - Vout
 - Iin
 - Iout
 - Temperature
 - Status of each rail

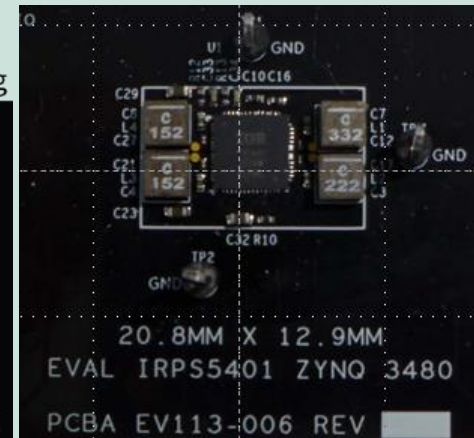
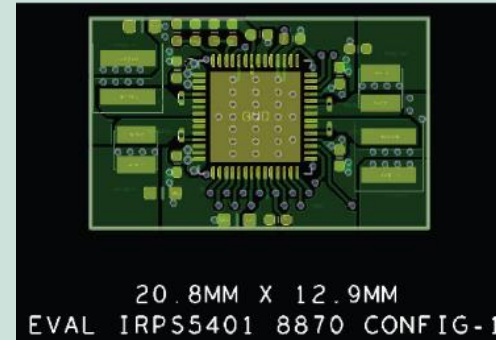


Summary: Enormous Flexibility to Support Any Power Requirement on XILINX VERSAL™



- ❑ Scalability for the Vcore rails from 2-phase to 8-phase to cover from **40A to 300+A** @ >90% Efficiency at Load and Temperature
- ❑ Additional output for DDR3/DDR4 voltages
- ❑ Preset Vcore voltages for Versal
- ❑ Integrated power sequencing
- ❑ PMBus telemetry and margining
- ❑ Ready to go PID designs for load transients and power macros for various Versal power use cases
- ❑ Proven design using Infineon's Power Validation Board – DB359

IRPS5401 - 20.8mm x 12.9mm
5 outputs with L's, Cout's
with integrated power sequencing



Summary:

More Information www.infineon.com/power-versal



<http://www.infineon.com/xilinx>



Please choose a subcategory

+ Expand all subcategories

- + Xilinx Zynq UltraScale+ RFSoc - New!
- + Xilinx Zynq UltraScale+, Embedded Vision, Zu07EV - New!
- + Xilinx Zynq UltraScale+ MPSoc, UltraZED-EG, Zu03
- + All of Infineon's Zynq UltraScale+ MPSoc Power Macros
- + Xilinx Zynq7
- + Xilinx Ultra Scale Kintex 10W Power Design - New!
- + Xilinx Ultra Scale Kintex 45W Power Design
- + Xilinx Artix 7
- + Xilinx Spartan6
- + Xilinx Kintex UltraScale+ (coming soon)
- + Xilinx Virtex UltraScale+ (coming soon)
- + Xilinx Spartan 7 (coming soon)

> Application examples

Infineon - Xilinx Solution Selector

Family: ☐ Virtex ☐ Kintex ☐ Zynq Plus

Power Range: 1 - 99 Watts

FPGA Power: ☐ Core ☐ Platform ☐ Serdes

Voltage Range: 0.1 - 5.0 Volt

Part Number	Xilinx Family	FPGA Power	Volt Rail	Power (W)	Voltage (V)	Features
Total Matched: 238						
IR36021 + IR3553	Virtex	CORE	VCCINT0V95	45	0.95	Digital Multi-phase Controller anc
IR36021 + IR3553	Virtex	CORE	VCCINT_I00V95	45	0.95	Digital Multi-phase Controller anc
IR36021 + IR3553	Virtex	CORE	VCCBRAM0V95	45	0.95	Digital Multi-phase Controller anc
IR3899	Virtex	PLATFORM	VCCAUX1V8	45	1.80	9A Analog SupIRBuck Regulator

Complete power supply reference design for Xilinx Kintex, Virtex FPGAs & Zynq SoCs/MPSoCs highly optimized and flexible design

Power supply reference design for Xilinx Kintex, Virtex FPGAs & Zynq SoCs/MPSoCs highly optimized and flexible design

Hot & New Designs

Hot & New Designs

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Videos

- > How to power up a state-of-the-art SoC
- > Infineon power for Xilinx ZCU-111 Zynq UltraScale+ RFSoc
- > Infineon power for Avnet UltraZED-EV Zu07EV evaluation platform
- > Infineon power for Xilinx ZCU-104 Zu07EV evaluation platform
- > Infineon power macros and reference designs for Xilinx Zynq UltraScale+ MPSoc and RFSoc

e.g.:

<https://www.youtube.com/watch?v=ovRTIxLXDFk>



Search

Group Sequencing

	Device	Loop	TUN_DELAY (ms)	TUN_RISE (ms)	TUN_FALL (ms)	TUN_DELAY (ms)	TUN_RISE (ms)	TUN_FALL (ms)
<input checked="" type="checkbox"/>	RPSS401R2	VCC0 1.8V	10	6	0	1	0	1
<input checked="" type="checkbox"/>	RPSS401R2	Sw_Voltage 3.3V	10	6	0	1	0	1
<input checked="" type="checkbox"/>	RPSS401R2	Sw_Voltage 3.3V	10	6	0	1	0	1
<input checked="" type="checkbox"/>	RPSS401R2	WPS_MOTIRACC	10	6	0	1	0	1
<input checked="" type="checkbox"/>	RPSS401R2	LDO	20	0	0	0	0	0
<input checked="" type="checkbox"/>	RPSS401R2	VCC0_PSD0R_504	48	6	0	12	6	6
<input checked="" type="checkbox"/>	RPSS401R2	WCONT_0300BRA	6	6	0	24	6	6
<input checked="" type="checkbox"/>	RPSS401R2	Sw_Voltage 3.3V	24	6	0	24	6	6
<input checked="" type="checkbox"/>	RPSS401R2	VCC0T	30	6	0	18	6	6
<input checked="" type="checkbox"/>	RPSS401R2	VCC_PSD0R_PLL	0	0	0	0	0	0
<input checked="" type="checkbox"/>	RPSS401R2	VCC0_PSD0	12	6	0	48	6	6
<input checked="" type="checkbox"/>	RPSS401R2	VCC0X_VCC0AC	6	6	0	6	6	6
<input checked="" type="checkbox"/>	RPSS401R2	VCC_PSD0TIP	6	6	0	54	6	6
<input checked="" type="checkbox"/>	RPSS401R2	VCC_PSD0TIP	48	6	0	36	1	6
<input checked="" type="checkbox"/>	RPSS401R2	VCC_PSD0L	0	0	0	0	0	0



Part of your life. Part of tomorrow.