DB359 Demo Board Performance Data and Infrastructure for Xilinx Versal Power Delivery

www.infineon.com/power-versal

V1.0
# Portfolio: Infineon Power Solutions for Xilinx Versal™

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Feature Description</th>
<th>Proven Solutions &amp; Application Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>IR35215MTRPBTF</td>
<td>Dual-loop digital multi-phase buck controller</td>
<td>Vcore at high current and current transient designs; 8+0, 4+4 loop design options; PMBus/I2C</td>
</tr>
<tr>
<td>TDA21472</td>
<td>OptiMOS 5 high current (70A) and high efficiency power stage in 5x6x0.9mm³ PQFN</td>
<td>Output current capability &gt; 70A; Integrated current and temperature sense, reporting and protection; Boot refresh; HS short protection; Excellent efficiency; up to 1.5MHz</td>
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<tr>
<td>IRPS5401</td>
<td>5-output PMIC, 4 DC-DC (2A, 4A, 8A, PWM for external powerstage) + 1 LDO (0.5A, tracking option), 5W to 50W</td>
<td>Compact design for multiple rails; Integrated sequencer; Integrated FETs; Use with ext. power stage optional; Digital compensation; PMBus/I2C</td>
</tr>
<tr>
<td>TDA21240</td>
<td>OptiMOS 5 Power-Stages 25A and 40A in 4mm x 4mm package; high efficiency</td>
<td>FPGA/SoC; best solution for size and efficiency in the market</td>
</tr>
<tr>
<td>TDA21242</td>
<td></td>
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<tr>
<td>IR38060, IR38062, IR38063, IR38064</td>
<td>Integrated FET regulators for 6A to 35A</td>
<td>Vcore and SERDES for Xilinx; Excellent thermal performance; PMBus/I2C with integrated sequencer, Fault mgmt., Telemetry</td>
</tr>
<tr>
<td>IR3897, IR3898</td>
<td>Integrated FET regulators for 4A and 6A</td>
<td>DDR3/DDR4 tracking +/-4A and +/-6A VTT</td>
</tr>
<tr>
<td>IR3883</td>
<td>Integrated FET regulator for 3A</td>
<td>Xilinx VCCIO voltages; low cost</td>
</tr>
<tr>
<td>IR3887, IR3889</td>
<td>New 30A High efficiency integrated FET regulators – releasing June 2019</td>
<td>Excellent performance; Efficiency &gt; 90% at load and over temperature</td>
</tr>
<tr>
<td>IFX1763</td>
<td>Low Noise LDO</td>
<td>2.5V for Xilinx ZYNQ Ultrascale+ RFSoC</td>
</tr>
<tr>
<td>IFX54441</td>
<td>Low Noise LDO</td>
<td>1.8V SERDES for Xilinx ZYNQ Ultrascale+ MPSoC</td>
</tr>
<tr>
<td>IR3823</td>
<td>Low Noise analog DC/DC regulator</td>
<td>1.2V SERDES for Xilinx ZYNQ Ultrascale+ FPGAs</td>
</tr>
</tbody>
</table>
Demo Board: DB359 Board (Load Socket and Decoupling)

- 2-phase to 8-phase Vcore high transient board for Xilinx Versal™ (10 layers)
- Supports Power Macros for Xilinx Versal VC1902 Power Macro Solutions (others in progress)

Capacitors used for test:
- 10x 560uF
- 50x 47uF

Phase inductors for test:
- 5x 100nH/120nH
- 4x 470uF + 14x 47uF

Infineon Proprietary
Demo Board: DB359 Test Setup: 2 Loops (5-Phases + 2 Phases)

Intel Voltage Regulator
Transient Test Tool

Test Conditions:
VID=0.7V
Loop 1:
Iout: 120A…165A
Transient steps:
30A…90A at 200A/us

Loop 2:
Iout: 25A
Transient step: 35A at 200A/us
Demo Board: DB359 Loop 1, 5-Phase Performance Results

Current reporting accuracy:

Startup/Shutdown:
Demo Board: DB359 Loop 1, 5-Phase Performance Results

Transient step 90A-150A at 200A/us:

- 1kHz repetition rate

Transient step 60A-150A at 200A/us:

- 10kHz repetition rate

- 8.7kHz repetition rate

Decoupling:

10x 560uF/3mΩ POSCAP
50x 47uF/0805
260x 10uF/0402 (cavity)
Demo Board: DB359 Loop 1, 5-Phase Performance Results

Efficiency

DB359 Rev 0, 5 Phases, TDA21472, 0.1 mΩ LL, Output voltage 0.7V, 100nH/120nH phase inductors, TDC=150A

The board has been tested up to 240A output current with only 5 phases enabled. The power loss at 240A is 26W.
Operating conditions:

- 5 Phases, TDA21472
- $LL = 0.1\, \text{m}\Omega$
- $V_{out} = 0.7\, \text{V}$
- $f_{sw} = 500\, \text{kHz}$
- $I_{out} = 150\, \text{A}$
- $L_{ph} = 100\, \text{nH}$
- $T_a = 25\, ^\circ\text{C}$
- No heatsink

Thermal data taken after 10 min soaking at 150A load current
Demo Board: DB359 Loop 2, 2-Phase Performance Results

Current reporting accuracy:

![Current Reporting Graph]

Startup/Shutdown:

![Startup/Shutdown Graphs]
Demo Board: DB359 Loop 2, 2-Phase Performance Results

› Steady State Ripple

No Load

60A Load Current
Demo Board:
DB359 Loop 2, 2-Phase Performance Results

Efficiency

DB359 Rev 0, 2 Phases, TDA21472, 0.645 mΩ LL Output voltage 0.7V, 100nH phase inductor, TDC=60A

The board has been tested up to 120A output current with 2 phases enabled. The power loss at 120A is 15.3W.
Operating conditions:

- 2 Phases, TDA21472
- $LL=0.645 \, \Omega$
- $V_{\text{out}}=0.7 \, \text{V}$
- $f_{\text{sw}}=500 \, \text{kHz}$
- $I_{\text{out}}=60 \, \text{A}$
- $L_{\text{ph}}=100 \, \text{nH}$
- $T_a=25 \, ^\circ \text{C}$
- No heatsink

Thermal data taken after 10 min soaking at 60A load current
Multiphase: Multiphase Controllers & Power Stages

Reasons to use MultiPhase solutions:

› Output current exceeds range for a single phase solution
› High efficiency over wide load range
› Better transient response
› Smaller decoupling solution (L, C)
› Less EMI due to smaller switched current

PowerStages on Infineon Website:

Key features
- Small 5x6x0.9mm³ molded PQFN package, 0.45mm pitch
- Highly accurate current reporting
- Programmable constant current limit OCSET
- Fast switching technology for improved performance at higher frequency, better peak efficiency
- Input voltage range 4.25V to 16V
- Output voltage range from 0.25V up to 5.5V
- Output current capability up to 70A
- Operation up to 1.5MHz
- Optimized for 5V drive

Key benefits
- Peak efficiency >95%
- 2.5mA I_{cc}, with low I_o (<200μA) disable PS4 (deep sleep mode) capability

Target applications
- Server and storage
- Telecom
- Datacom
Multiphase: Multiphase Controller IR35215

- Seamless integration with POL and PMIC devices into the same GUI
- 5-output PMIC configured for 2 single phase switcher rails, a dual phase rail and an LDO rail
- 2-output multiphase controller
- 1-phase 30A POL
Multiphase: I2C and PMBUS Communication

USB Dongle005 connects PC and application board

For communication and programming via I2C three wires (GND, DATA, CLK) are required.

4 pin header:
- GND
- DATA/DIO/DAT
- CLK
- ALERT#/ALRT#

Connected to programming USB port

Install header on pcb: 4 positions, breakaway connector 2.54mm (0.1“) pitch

e.g. Digikey S1011E-04-ND or S1011E-36-ND (36 pins, break off 4 pins)
Established controller solution for Intel CPU regulation

8/4 phase dual loop controller (2 loops configurable from 1..4+0..4, 5+0..3, 6+0..2, 7+0/1, 8+0)
  - Active voltage positioning (load-line)
  - 5mV VID resolution
  - Voltage mode with active current balancing (active current sharing)
  - Nonlinear transient support (adaptive transient algorithm)
  - Digital compensation (no external compensation components)
  - SVID and I2C/PMBUS
  - Autophasing (phase shedding)
  - Telemetry on voltage, current, power, temperature, fault protection and reporting
  - 5mm x 5mm 40-pin QFN-package
  - Digital pin-strapping to select an entire configuration from many
  - Programmable I/O pins to support additional reporting and enable functions
Multiphase: PowIRCenter, IR35215 Device Addresses

If `i2c_use_addr_offset` = 0 then Address Offset = 0 else Address Offset = $f(R_{PROG})$

I2C Address = I2C NVM address + Address Offset

PMBUS Address = PMBUS NVM address + Address Offset

- **I2C Address**
  - Address Offset

- **PMBUS Address**
  - Address Offset

Note: The offset for PMBUS and I2C bus is always identical.

### Table of $R_{PROG}$ Values

<table>
<thead>
<tr>
<th>Addr. Offset</th>
<th>$R_{PROG}$ [kΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>+0</td>
<td>0.845</td>
</tr>
<tr>
<td>+1</td>
<td>1.30</td>
</tr>
<tr>
<td>+2</td>
<td>1.78</td>
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<tr>
<td>+3</td>
<td>2.32</td>
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<tr>
<td>+4</td>
<td>2.87</td>
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<tr>
<td>+5</td>
<td>3.48</td>
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<tr>
<td>+6</td>
<td>4.12</td>
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<td>+7</td>
<td>4.75</td>
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<td>+8</td>
<td>5.49</td>
</tr>
<tr>
<td>+9</td>
<td>6.19</td>
</tr>
<tr>
<td>+10</td>
<td>6.98</td>
</tr>
<tr>
<td>+11</td>
<td>7.87</td>
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<tr>
<td>+12</td>
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<tr>
<td>+13</td>
<td>10.00</td>
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<tr>
<td>+14</td>
<td>11.00</td>
</tr>
<tr>
<td>+15</td>
<td>12.10</td>
</tr>
</tbody>
</table>

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**Example 1:**
A .MIC file with 11 configuration sections was written into NVM. `PROG_MAX` has been set to the value of 11. The `PROG` resistor of 5.49 kΩ selects configuration section 9 to be loaded and used.

No further .MIC file can be programmed.

A subsequent programming of a new configuration writes into section 12 which is then being used. Another 15 sections remain free for possible single configuration writes.

<table>
<thead>
<tr>
<th>Config Offset</th>
<th>MIC file</th>
<th>( R_{PROG} ) value [kΩ]</th>
<th>Single MTP write</th>
</tr>
</thead>
<tbody>
<tr>
<td>+0</td>
<td>1</td>
<td>0.845</td>
<td>1</td>
</tr>
<tr>
<td>+1</td>
<td>2</td>
<td>1.3</td>
<td>2</td>
</tr>
<tr>
<td>+2</td>
<td>3</td>
<td>1.78</td>
<td>3</td>
</tr>
<tr>
<td>+3</td>
<td>4</td>
<td>2.32</td>
<td>4</td>
</tr>
<tr>
<td>+4</td>
<td>5</td>
<td>2.87</td>
<td>5</td>
</tr>
<tr>
<td>+5</td>
<td>6</td>
<td>3.48</td>
<td>6</td>
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<tr>
<td>+6</td>
<td>7</td>
<td>4.12</td>
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</tr>
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<td>8</td>
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<td>9</td>
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<td>+...</td>
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<td></td>
</tr>
<tr>
<td>+26</td>
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</tr>
</tbody>
</table>

**Example 2:**
The first write into NVM was a single configuration. No .MIC file can be programmed anymore. 26 more single configuration writes remain available.

**In general:**
- If `prog_max` is smaller than the number of programmed segments, the last segment will be used.
- If `prog_max` is bigger than the number of programmed segments and `R_{PROG}` points to a valid segment, this segment will be used.
- `R_{PROG}` points to an unprogrammed segment, the part does not start.
Summary: One Software Interface

- PowIRCenter GUI for all PMBUS devices
- Reporting status of
  - Interface to board
  - PMBUS/I2C addresses
  - Vin
  - Vout
  - Iin
  - Iout
  - Temperature
  - Status of each rail
Summary: Enormous Flexibility to Support Any Power Requirement on XILINX VERSAL™

- Scalability for the Vcore rails from 2-phase to 8-phase to cover from **40A to 300+A @ >90% Efficiency at Load and Temperature**
- Additional output for DDR3/DDR4 voltages
- Preset Vcore voltages for Versal
- Integrated power sequencing
- PMBus telemetry and margining
- Ready to go PID designs for load transients and power macros for various Versal power use cases
- Proven design using Infineon’s Power Validation Board – DB359

- High integration PMICs for compact design for Versal smaller current rails – 5 outputs
- Each PMIC stores up to 15 simultaneous designs
- Integrated power sequencing (also to external VR)
- Hardware sequencing with external regulators possible
- Capable for **5W to 50W voltage rail combinations**
- PMBus telemetry, margining, tracking LDO
- Proven on many Xilinx reference designs
- Ready to go Versal designs and power macros
Summary:

More Information  [www.infineon.com/power-versal](http://www.infineon.com/power-versal)

http://www.infineon.com/xilinx

Please choose a subcategory

- Xilinx Zyng UltraScale+ RFSoC – New!
- Xilinx Zyng UltraScale+ RFSocC – New!
- Xilinx Zyng UltraScale+ MPSoc 45W Power Design
- Xilinx Zyng UltraScale+ MPSoc, UltraZED-EG, Zu03
- Xilinx Spartan6
- All of Infineon’s Zyng UltraScale+ MPSoc Power Macros
- Xilinx Virtex UltraScale+ (coming soon)
- Xilinx Spartan 7 (coming soon)

Application examples

- How to power up a state-of-the-art SoC
- Infineon power for Xilinx ZCU-111 Zynq UltraScale+ RFSoC
- Infineon power for Avnet UltraZED-EV Zu07EV evaluation platform
- Infineon power for Xilinx ZCU-104 Zu07EV evaluation platform
- Infineon power macros and reference designs for Xilinx Zyng UltraScale+ MPSocC and RFSoC

Videos

- [How to power up a state-of-the-art SoC](https://www.infineon.com/xilinx)
- [Infineon power for Xilinx ZCU-111 Zynq UltraScale+ RFSoC](https://www.youtube.com/watch?v=ovRTIxLXDFk)
- [Infineon power for Avnet UltraZED-EV Zu07EV evaluation platform](https://www.youtube.com/watch?v=ovRTIxLXDFk)
- [Infineon power for Xilinx ZCU-104 Zu07EV evaluation platform](https://www.youtube.com/watch?v=ovRTIxLXDFk)
- [Infineon power macros and reference designs for Xilinx Zyng UltraScale+ MPSocC and RFSoC](https://www.youtube.com/watch?v=ovRTIxLXDFk)
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