Multiphase Buck Converter with TLVR Output Filter

About this document

Scope and purpose

This paper is intended to assist with the design for a trans-inductor voltage regulator (TLVR).[1] Today, applications are evolving that have very high current demands, also requiring the support of very steep load current transient steps. Historically, transient support was largely reliant on the output capacitor bank because the output filter inductors prevented fast current rise coming from the regulator. With the introduction of TLVR filter configurations, this has changed. TLVR topology is used in conjunction with multiphase buck converters to support very steep load transients with a minimum of output capacitance.

Intended audience

The goal of this application note is to explain the theoretical foundation of the topology and to provide basic design equations, enabling technical staff to design with TLVR output filters.

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Introduction

1 Introduction

TLVR was introduced at the APEC conference by Google. Its merit lies in the implementation of phase coupling to optimize coupling performance without infringing on existing patents of coupled inductors or transformer-coupled solutions with additional output inductor.

The TLVR topology applied to the power stage outputs of a multiphase buck regulator enables the regulator to achieve very fast transient response without sacrificing other critical performance parameters. By increasing the transient response, large output capacitors can be removed. These are mostly polymeric capacitors that usually suffer from performance degradation over their lifetime.

Therefore, TLVR improves the circuit reliability and, because of the relatively high cost of polymeric capacitors, it also helps improve the system cost.

2 TLVR circuit

In this document the current from phase node to output of the voltage regulator is referred to as the “primary current”, following the notion of the source of energy. The current in the coupling loop is then the current in the secondary windings of the TLVR transformers.

The duty cycle is defined as: $$D = \frac{V_{out}}{V_{in}} \quad (1)$$

The TLVR circuit compared to a standard multiphase buck regulator can be described as replacing the phase inductors with transformers, and connecting their respective secondary windings in series with an additional inductor. Therefore, the adaptation of a conventional design can be done rather quickly, as it is not a complicated change. However, it is important to select the most suitable components for the task and to avoid some pitfalls when tuning the circuit.

2.1 Operation theory

The following figure shows a simulation of an eight-phase TLVR circuit in steady-state.

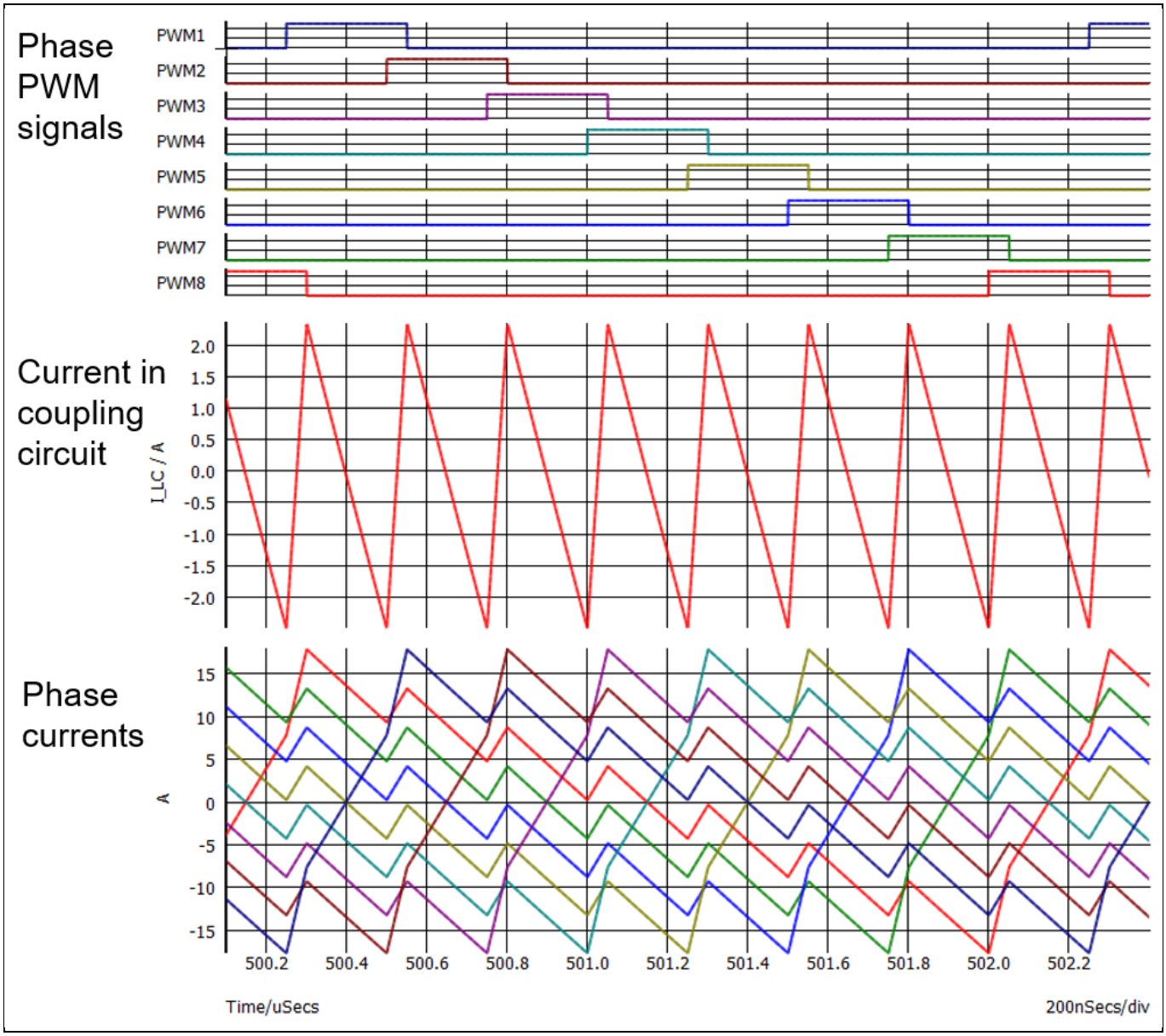

Figure 1 TLVR waveforms

TLVR circuit

By looking at the phase current slopes in steady-state, one can distinguish the following:

- One rising slope and one falling slope: circuit is not coupled, or the duty cycle times phase count is an integer
- One rising slope during the phase on-time and two different slopes during the off-time: coupled and a non-overlapping PWM signal
- Two distinct slopes during the on-time and two different slopes during the off-time: coupled and overlapping PWM signals.

The current in the coupling loop in steady-state is always of a triangular shape or zero.

For analysis of the circuit properties in fixed-frequency interleaved-phase continuous conduction mode (CCM) the different current ramping conditions are being investigated. There are at most four different slopes of phase current for a given set of operation parameters:

1. Turn-on with maximum count of phases in on-state
2. Turn-on with minimum count of phases in on-state
3. Turn-off with maximum count of phases in off-state
4. Turn-off with minimum count of phases in off-state

Furthermore, if the phases have no overlap, case 2 does not exist, as no other phase can be in the on-state.

In the general case of steady-state, the maximum phase count is one higher than the minimum phase count. The exception is when the duty cycle times the phase count is an integer. In that case, no output ripple current exists, and maximum and minimum counts of phases in the on-state are equal, i.e. there are only two slopes present.

The phase current always is the sum of the magnetizing current and the coupled current of the TLVR transformer. The magnetizing current change during the on-time of the high-side switch (HS) over one switching period can be expressed as:

$$\Delta I_{mag\_ph\_up} = \frac{V_{in}-V_{out}}{L_m} \cdot \frac{D}{f_{sw}} = \frac{V_{in}}{L_m \cdot f_{sw}} \cdot (1-D) \cdot D \quad (2)$$

The magnetizing current change during the off-time of the HS switch over one switching period can be written as:

$$\Delta I_{mag\_ph\_down} = \frac{-V_{out}}{L_m} \cdot \frac{1-D}{f_{sw}} = \frac{-V_{in}}{L_m \cdot f_{sw}} \cdot (1-D) \cdot D \quad (3)$$

The magnetizing current ripple calculation in steady-state yields:

$$\Delta I_{mag\_ph} = \Delta I_{mag\_ph\_up} = \left|\Delta I_{mag\_ph\_down}\right| = \frac{V_{in}}{L_m \cdot f_{sw}} \cdot (1-D) \cdot D \quad (4)$$

The ripple current in the secondary winding is exhibiting a ripple frequency of:

$$f_{HF} = N \cdot f_{sw} \quad (5)$$

and a period of:

$$T_{HF} = \frac{1}{f_{HF}} \quad (6)$$

For the calculation of slopes at the resulting ripple frequency one must know the overlapping phase count and duty cycle for the higher frequency (f_{HF}).

TLVR circuit

The maximum number of phases being simultaneously in the on-state is:

$$N_{SimOnMax} = Roundup(N \cdot D, 0) \tag{7}$$

Then the minimum number of phases that are on at any given time are shown as:

$$N_{SimOnMin} = IF(N_{SimOnMax} = N \cdot D, N_{SimOnMax}, N_{SimOnMax} - 1) \tag{8}$$

That also accounts for the special case in which the phase count times the duty cycle is an integer.

The on-time calculation for the total ripple current is the overlap time of the maximum phase count.

$$D_{HF} = \frac{t_{overlap}}{T_{HF}} = N \cdot D - INT(N \cdot D) \tag{9}$$

For the resulting ripple frequency, the time during which the output current ramps up is then defined as overlap and calculated as:

$$t_{overlap} = T_{sw} \cdot [D - INT(N \cdot D)/N] \tag{10}$$

Now, the coupling ripple current can be expressed as:

$$\Delta I_{Lc\_pkpk} = k \cdot (N_{SimOnMax} \cdot V_{in} - N \cdot V_{out}) \cdot \frac{D_{HF}}{L_c \cdot f_{HF}} \tag{11}$$

The phase ripple current is composed of the magnetizing current and the coupled current from the secondary winding. During the rising edge of the magitizing current there is always one more rising instance from the secondary winding than a falling edge coupled back. That leaves as a net result:

$$\Delta I_{ph\_pkpk} = \Delta I_{mag\_ph} + k \cdot \Delta I_{Lc\_pkpk} \tag{12}$$

$$\Delta I_{ph_{pkpk}} = \frac{V_{in}}{L_m \cdot f_{sw}} \cdot (1 - D) \cdot D + k \left(k \cdot (N_{SimOnMax} \cdot V_{in} - N \cdot V_{out}) \cdot \frac{D_{HF}}{L_c \cdot f_{HF}} \right) \tag{13}$$

$$= \frac{V_{in} - V_{out}}{L_m} \cdot t_{on} + k^2 \cdot \frac{N_{SimOnMax} \cdot V_{in} - N \cdot V_{out}}{L_c} \cdot t_{overlap} \tag{14}$$

$$\Delta I_{ph_{pkpk}} = \frac{V_{in}}{f_{sw}} \left[\frac{1}{L_m} \cdot (1 - D) \cdot D + \frac{k^2}{L_c} \left(\frac{N_{SimOnMax}}{N} - D \right) \cdot D_{HF} \right] \tag{15}$$

For the calculation of the resulting output ripple current of the regulator the sum of all phase currents must be considered. It is composed of the sum of all magnetizing phase currents and the coupled currents in each phase. The rise time of the ripple current is the overlap time. With that the ripple current is:

$$\Delta I_{out\_pkpk} = k \cdot N \cdot \Delta I_{Lc_{pkpk}} + N_{SimOnMax} \cdot \Delta I_{mag_{ph}} \cdot \frac{t_{overlap}}{D \cdot T_{sw}} - (N - N_{SimOnMax}) \cdot \Delta I_{mag_{ph}} \cdot \frac{t_{overlap}}{(1 - D) \cdot T_{sw}} \tag{16}$$

$$\Delta I_{out\_pkpk} = k \cdot N \cdot \Delta I_{Lc_{pkpk}} + \frac{\Delta I_{mag_{ph}} \cdot t_{overlap}}{T_{sw}} \cdot \left(\frac{N_{SimOnMax}}{D} - \frac{N - N_{SimOnMax}}{(1 - D)} \right) \tag{17}$$

TLVR circuit

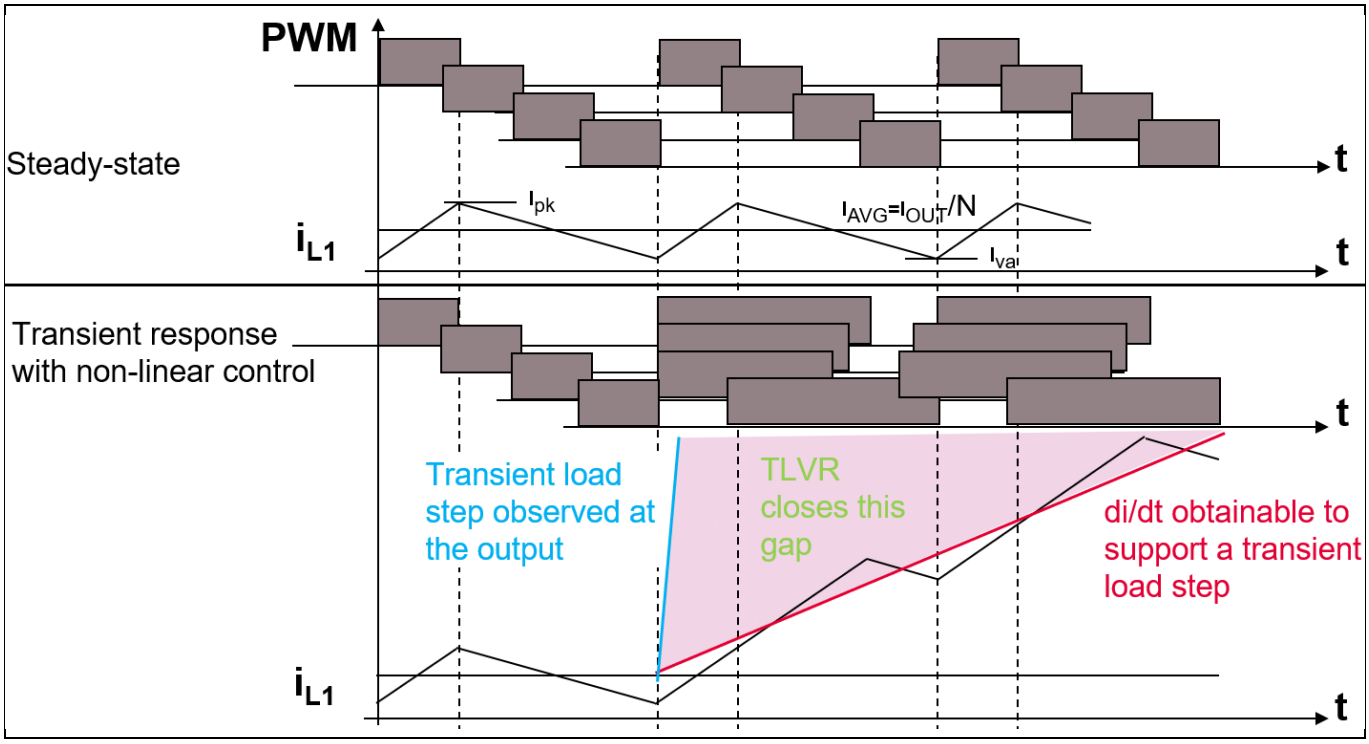

Figure 2 Transient comparison (example)

The TLVR transformer components are high-current transformers with a 1:1 turns ratio. The primary winding is normally designed with more copper so as to minimize the steady-state conduction loss. The core material is mostly ferrite based to obtain low core loss.

Therefore, it is important to study the saturation characteristics carefully to prevent core saturation at high current and temperature. Saturation will have negative effect on controllability and cause excessive stress on the power stages. For the selection of a TLVR transformer, the saturation current should follow this rule:

$$I_{TLVR\_sat} \geq \frac{I_{out\_max}}{N} + \frac{\Delta I_{ph\_pkpk}}{2} \tag{18}$$

Output voltage ripple calculation:

$$\triangle V_{out\_pkpk} = \triangle I_{out\_pkpk} \cdot \left[\frac{1}{8 \cdot C_{out} \cdot N \cdot f_{sw}} + ESR + 2 \cdot N \cdot f_{sw} \cdot ESL\right] \tag{19}$$

with ESR and ESL being the resistive and inductive impedance of the total output capacitance array.

That leaves a first requirement for the minimum output capacitance when an output ripple voltage maximum is given:

$$C_{out} \geq \frac{1}{8 \cdot N \cdot f_{sw}\left[\frac{\triangle V_{out\_pkpk}}{\triangle I_{out\_pkpk}} - (ESR + 2 \cdot N \cdot f_{sw} \cdot ESL)\right]} \tag{20}$$

With ESL being a few pH while *N* x *fsw* may approach a value of 40 MHz, the inductive impedance is likely below 2 µΩ. Therefore, the effect compared to the resistive contribution might be neglected for the sake of simplicity, leading to this requirement:

$$C_{out\_\min\_ripple} \geq \frac{1}{8 \cdot N \cdot f_{sw}} \cdot 1 \Big/ \left(\frac{dV_{out}}{dI_{out\_pkpk}} - ESR_{Cout}\right) \tag{21}$$

For this calculation it is important to consider the minimum phase count and whether or not the phase angles will be dynamically rebalanced.

TLVR circuit

This requirement is usually very weak, as the transient support will likely impose a much higher capacitance value.

It is important to consider some noise effect on the control loop, especially because the bandwidth (BW) is now much higher compared to any traditional approach.

For the selection of the magnetics, multiple aspects are of interest.

1. Estimation of voltage overshoot during load release

   The energy stored in the magnetic components must be released into the output capacitors and will result in a voltage overshoot.

   $$L_m \leq sfac \cdot 2 \cdot \frac{N \cdot C_{out}}{I_{LoadStep}{}^2} \cdot V_{out} \cdot \left[\Delta V_{out\_max} - I_{LoadStep} \cdot \left(ESR + \frac{ESL}{t_{LoadStep}}\right)\right] \quad (22)$$

   (*sfac* is a safety factor)

   The equation is approximate and the factor sfac accounts for margin in the calculation of a maximum value for L_m. Having 10 percent margin for inaccuracies of the effective output capacitance, step current and time as well as parasitic impedances one would set sfac to 0.9, for example. It is also assumed that at the time of the transient step no DC excursion is present in the coupling loop, i.e. the circuit had been in steady-state before.

2. Coupling strength to meet transient target

   The value of the coupling inductance L_c determines the strength of coupling, i.e. the factor of current amplification in the output. For a given transient load the goal is to allow the TLVR current to rise at the same rate when the controller commands. Having more gain in the output filter as needed will require the compensation loop to be detuned to keep the system stable at high load repetition rates, possibly sacrificing DC gain, making the system prone to voltage offsets stemming from the load duty cycle. Too little gain in the output filter will prevent the current slope from reaching the required transient slope, so will require additional output capacitors to decouple the output.

   If the controller is triggered with its non-linear features, a maximum effective duty cycle can be deployed for each PWM. Based on that assumption, the current ramp has to be fast enough to meet the target.

   The magnetizing current per phase ramps on average in a switching cycle by:

   $$\frac{\Delta I_{mag\_ph\_ramp}}{T_{sw}} = \frac{D_{ramp} \cdot V_{in} - V_{out}}{L_m} \quad (23)$$

   The current in the coupling winding ramps on average in a switching cycle by:

   $$\frac{\Delta I_{Lc\_ramp}}{T_{sw}} = k \cdot N \cdot \frac{D_{ramp} \cdot V_{in} - V_{out}}{L_c} \quad (24)$$

   Therefore, the output current change per switching cycle can be calculated as:

   $$\frac{\Delta I_{outramp}}{T_{sw}} = k \cdot N \cdot \frac{\Delta I_{Lcramp}}{T_{sw}} + N \cdot \frac{\Delta I_{magphramp}}{T_{sw}} \quad (25)$$

   $$= k^2 \cdot N^2 \cdot \frac{D_{ramp} \cdot V_{in} - V_{out}}{L_c} + N \cdot \frac{D_{ramp} \cdot V_{in} - V_{out}}{L_m} \quad (26)$$

   $$= \left(D_{ramp} \cdot V_{in} - V_{out}\right) \cdot \left(\frac{k^2 \cdot N^2}{L_c} + \frac{N}{L_m}\right) \quad (27)$$

   This equation also allows for the derivation of the effective transient inductance of the entire regulator:

TLVR circuit

$$\frac{1}{L_{trans}} = \frac{k^2 \cdot N^2}{L_c} + \frac{N}{L_m} \quad (28)$$

$$L_{trans} = \frac{L_m \cdot L_c}{k^2 \cdot N^2 \cdot L_m + N \cdot L_c} \quad (29)$$

In order to reduce all bulk capacitance, the target current ramping slope has to be at least as fast as the transient load step itself:

$$\frac{\Delta I_{Loadstep}}{T_{Loadstep}} \leq \left(D_{ramp} \cdot V_{in} - V_{out}\right) \cdot \left(\frac{k^2 \cdot N^2}{L_c} + \frac{N}{L_m}\right) \quad (30)$$

With a maximum ramp duty cycle and a selected L_m value to meet the overshoot and saturation requirements, L_c can be calculated as:

$$L_c \leq \frac{k^2 \cdot N^2}{\frac{\Delta I_{Loadstep}}{T_{Loadstep} \cdot (D_{ramp} \cdot V_{in} - V_{out})} - \frac{N}{L_m}} \quad (31)$$

Note: The output capacitance must be high enough to absorb the charge stemming from the delay of the regulator reaching the duty cycle D_{ramp}. As an approximation to account for that, the output capacitance should be at least:

$$C_{out\_min\_trans} \geq \frac{t_{Delay} \cdot \Delta I_{Loadstep}}{dV_{out}} \quad (32)$$

This is usually covered by the multi-layer ceramic capacitors (MLCCs) placed at the load, and in most cases a much more stringent criterion than the required output capacitance for the sake of the ripple voltage requirement.

3. Form factor and placement options

As a general rule for layout, the coupling loop should be considered as noisy (comparable to the switching node). Therefore, the best practice for coupling is the routing of the connection only on the top layer without any vias. The connection to close the loop is then the second-layer ground. Vias only need to connect at both ends of the phase and L_c arrangement to ground.

High-current TLVR transformers exist in narrow designs, allowing for very dense phase-to-phase placements. But these TLVR transformers stand tall, up to 12 mm on the PCB. If that is a problem, other form factors might need to be used.

In some cases, the placement of the L_c inductor might be preferred at the opposite site of the PCB when there is no space available to place it on the same side as the TLVRs. In this case, it is highly recommended to connect the inductor on both pins directly with via arrays. If routed on the opposite side, it is very important that the L_c inductor does not saturate. It is recommended to use a soft saturating part if a small form factor is necessary.

In some cases, multiple L_c can be used in series to obtain the target inductance value. This is important for high phase count when there are EMI propagation concerns through the PCB and/or PCB prepreg voltage breakdown voltage violations. More detail is given in the section on layout.

2.2 Regulator bandwidth improvement

2.2.1 L-C double-pole frequency comparison

The L-C double-pole frequency is located at:

$$\omega_{LC} = \frac{1}{\sqrt{L_{AC} \cdot C_{out}}} \tag{33}$$

with L_{AC} being the effective small signal output inductance of the regulator and C_{out} the total output capacitance.

For the TLVR:

$$L_{AC} = L_{trans} = \frac{L_m \cdot L_c}{k^2 \cdot N^2 \cdot L_m + N \cdot L_c} \tag{34}$$

$$\omega_{TLVR}^2 = \frac{k^2 \cdot N^2 \cdot L_m + N \cdot L_c}{L_m \cdot L_c \cdot C_{out}} = \frac{k^2 \cdot \mathrm{N} \cdot L_m + L_c}{L_c} \cdot \frac{N}{L_m \cdot C_{out}} \tag{35}$$

In a conventional multiphase buck regulator, the equation reads:

$$\omega_{MPB}^2 = \frac{N}{L_{ph} \cdot C_{out}} = (2\pi f_{MPB})^2 \tag{36}$$

By comparison, one can determine that the L-C double-pole frequency of a TLVR with the same values in L_m and C_{out} is shifted to higher frequencies:

$$f_{TLVR} = \sqrt{\frac{k^2 \cdot \mathrm{N} \cdot L_m}{L_c} + 1} \cdot f_{MPB} \tag{37}$$

Because one objective of TLVR is to reduce output capacitance the shift toward higher frequency is augmented.

2.2.2 Bandwidth comparison

Taking the L-C double-pole frequency location as a reference for the compensation and assuming that the crossover frequency moves at the same ratio, then a BW comparison can be made for a given phase count, coupling factor and L_c/L_m ratio.

If taking the reduction in C_{out} into account, another factor emerges:

$$f_{TLVR} = \sqrt{\frac{k^2 \cdot \mathrm{N} \cdot L_m}{L_c} + 1} \cdot \frac{1}{\sqrt{C_{out}}} \cdot \sqrt{\frac{N}{2\pi \cdot L_{ph}}} \tag{38}$$

The following graph is a sample plot of the BW improvement of the TLVR versus the standard multiphase buck configuration, taking the aforementioned factors into account.

The assumptions here are:

- Eight phases
- k = 0.98
- 50 percent reduction in total output capacitance

TLVR circuit

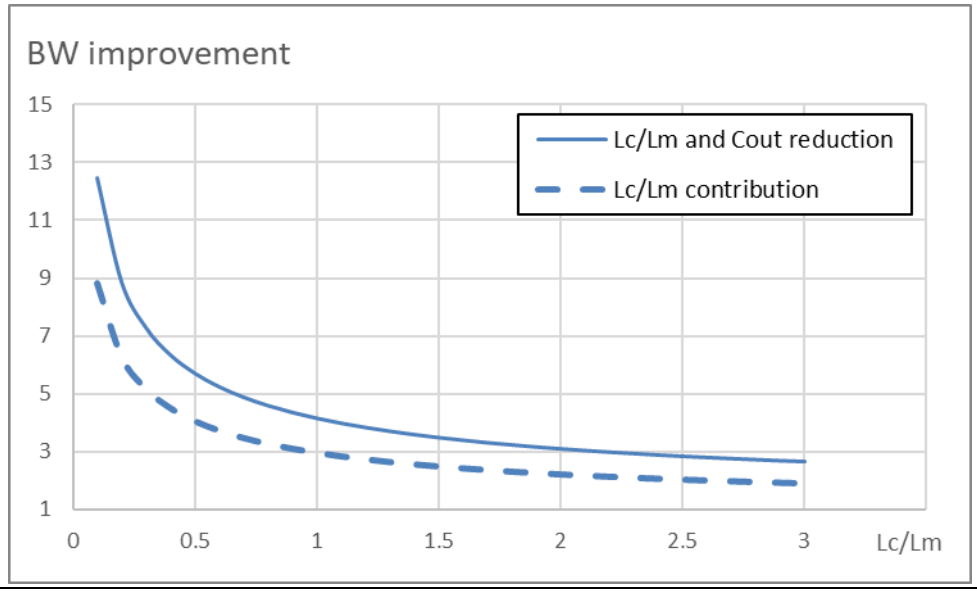

Figure 3 Projected BW improvement with TLVR

Note: The theoretical BW limit is now half of N x f_{sw}. This applies for very strong coupling, i.e. for very high coupling current. Therefore, a reasonable maximum BW should be at a derated effective ripple frequency accounting for the practical coupling strength and applying the rule of thumb to have a crossover frequency of about 10 percent of this frequency.

Current ramp in a conventional system:

$$\frac{\Delta I_{out}}{T_{sw}} = N \cdot \frac{D \cdot V_{in} - V_{out}}{L_{ph}} \tag{39}$$

Current ramp in TLVR:

$$\frac{\Delta I_{out}}{T_{sw}} = N \cdot \left[\frac{D \cdot V_{in} - V_{out}}{L_m} + \frac{k^2}{L_c} \left[\begin{matrix} D_{HF} \cdot (N_{SimOnMax} \cdot V_{in} - N \cdot V_{out}) \\ +(1 - D_{HF}) \cdot \left((N_{SimOnMax} - 1) \cdot V_{in} - N \cdot V_{out} \right) \end{matrix} \right] \right] \tag{40}$$

$$\frac{\Delta I_{out}}{T_{sw}} = N \cdot \left[\frac{D \cdot V_{in} - V_{out}}{L_m} + \frac{k^2}{L_c} \left[(N_{SimOnMax} - 1 + D_{HF}) \cdot V_{in} - N \cdot V_{out} \right] \right] \tag{41}$$

Now the ratio of current increase between TLVR and a conventional system can be expressed as:

$$\frac{\Delta I_{out\_TLVR}}{\Delta I_{out\_MPB}} = \frac{N}{N \cdot \frac{D \cdot V_{in} - V_{out}}{L_{ph}}} \cdot \left[\frac{D \cdot V_{in} - V_{out}}{L_m} + \frac{k^2}{L_c} \left[(N_{SimOnMax} - 1 + D_{HF}) \cdot V_{in} - N \cdot V_{out} \right] \right] \tag{42}$$

When $L_m = L_{ph}$ then:

$$\frac{\Delta I_{out\_TLVR}}{\Delta I_{out\_MPB}} = 1 + \frac{k^2 \cdot L_m}{L_c} \frac{\left[(N_{SimOnMax} - 1 + D_{HF}) \cdot V_{in} - N \cdot V_{out} \right]}{D \cdot V_{in} - V_{out}} \tag{43}$$

$$\frac{\Delta I_{out\_TLVR}}{\Delta I_{out\_MPB}} = 1 + \frac{k^2 \cdot L_m}{L_c} \cdot \frac{\left(Roundup(N \cdot D, 0) - 1 + N \cdot D - INT(N \cdot D) \right) \cdot V_{in} - N \cdot V_{out}}{D \cdot V_{in} - V_{out}}$$

(44)

$$\frac{\Delta I_{out\_TLVR}}{\Delta I_{out\_MPB}} \approx 1 + k^2 \cdot \frac{L_m}{L_c} \cdot N \tag{45}$$

TLVR circuit

For high phase count and k→1:

$$\frac{\Delta I_{out_{TLVR}}}{\Delta I_{out_{MPB}}} \approx \frac{L_m}{L_c} \cdot N \tag{46}$$

In general, a relationship for the crossover frequency of the TLVR can be established:

$$\sqrt{\frac{f_{C\_TLVR}}{f_{C\_MPB}}} = 1 + k^2 \cdot \frac{L_m}{L_c} \cdot N \tag{47}$$

One can see that the current slope can be very large and hence uncontrollable. Therefore, the Nyquist limit must still be considered as an upper value because the loop current adjustment is a time-discrete event.

In addition, controller and powerstages have a response delay, which also poses a limit for the possible BW.

For practical purposes the maximum crossover frequency should be considered as:

$$f_{C\_TLVR} \leq \frac{1}{t_{delay} + \frac{1}{0.10 \cdot MIN\left(\left(1+k^2 \cdot \frac{L_m}{L_c} \cdot N\right)^2, 8.5\right) \cdot f_{SW}}} \tag{48}$$

This equation considers a crossover frequency range from 10% of the switching frequency to a maximum of 85% of it.

Simplified for k→1 and high phase count is will be:

$$f_{C\_TLVR} \leq \frac{1}{t_{delay} + \frac{1}{0.10 \cdot f_{SW} \cdot MIN\left(\left(N \cdot \frac{L_m}{L_c}\right)^2, 8.5\right)}} \tag{49}$$

For example, if switching at 500 kHz with eight phases and having $L_m = L_C$ would lead to a maximum suitable crossover frequency of 402 kHz.

Under most circumstances L_C is small enough that the limit of “1” takes over, and the approximation for the achievable BW simply scales up with the number of phases, up to the point where the speed of the control loop becomes a factor.

However, in order to obtain low jitter and high efficiency, the loop BW should not be made larger than necessary to support the required current transient. One must always bear in mind that the system is prone to noise injection into its rather long feedback lines (voltage and current).

2.3 Schematic

The TLVR schematic is very similar to a conventional multiphase buck. The following picture shows an excerpt of a schematic with TDA21590 power stages driving TLVR transformers. These transformers are all coupled as shown here, and the outer two phases (depicted here) have terminations to GND, on one side directly and on the other side via the L_C inductor.

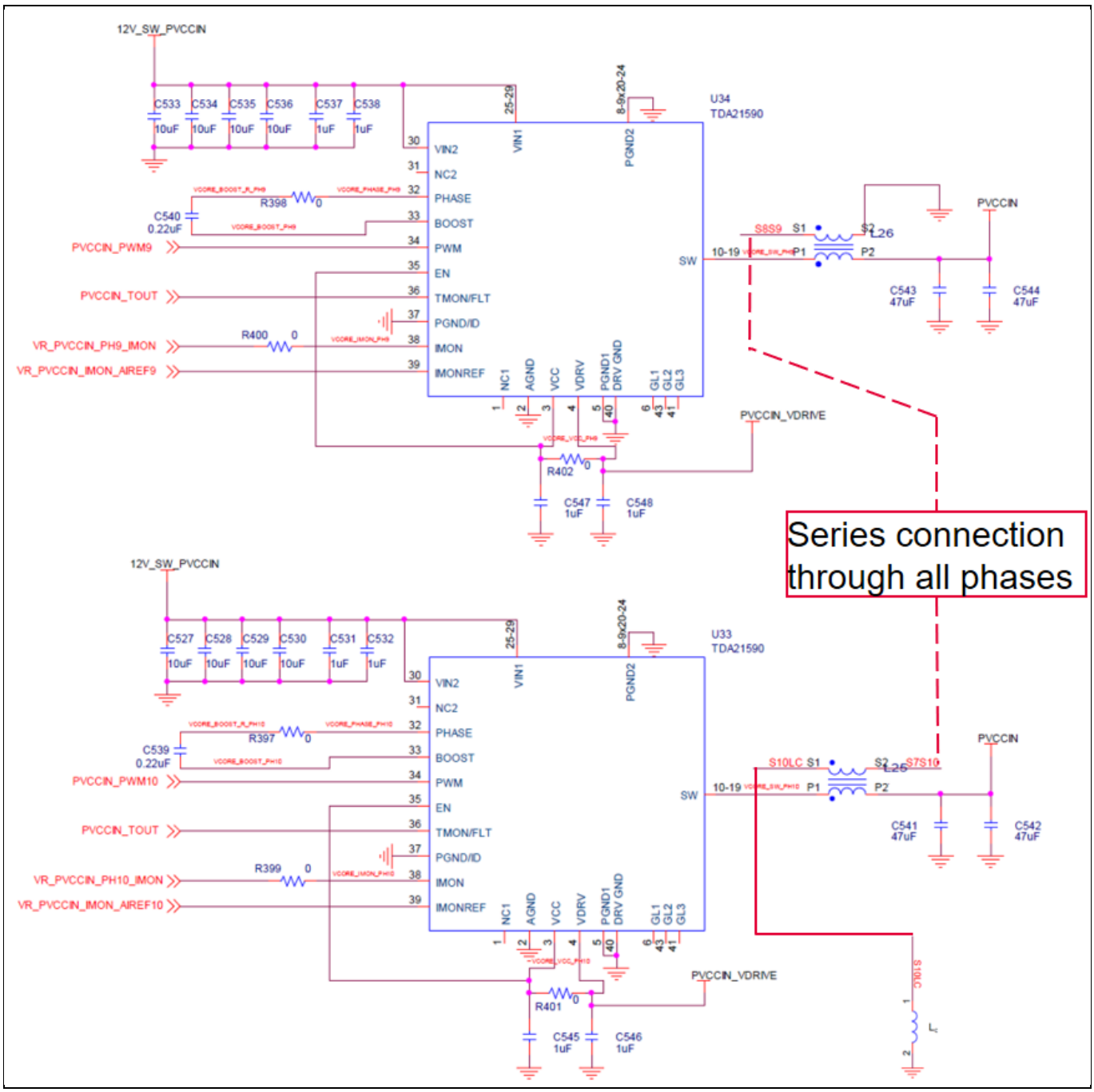

Figure 4 TLVR output filter connections

2.4 TLVR transformer components

The TLVR transformer components are high-current transformers with a 1:1 turns ratio. The primary winding is normally designed with more copper to minimize the steady-state conduction loss. The core material is mostly ferrite based to obtain low core loss. Therefore, it is important to study the saturation characteristic carefully to prevent core saturation at high current and temperature. Saturation will have a negative effect on controllability and causes excessive stress on the power stages.

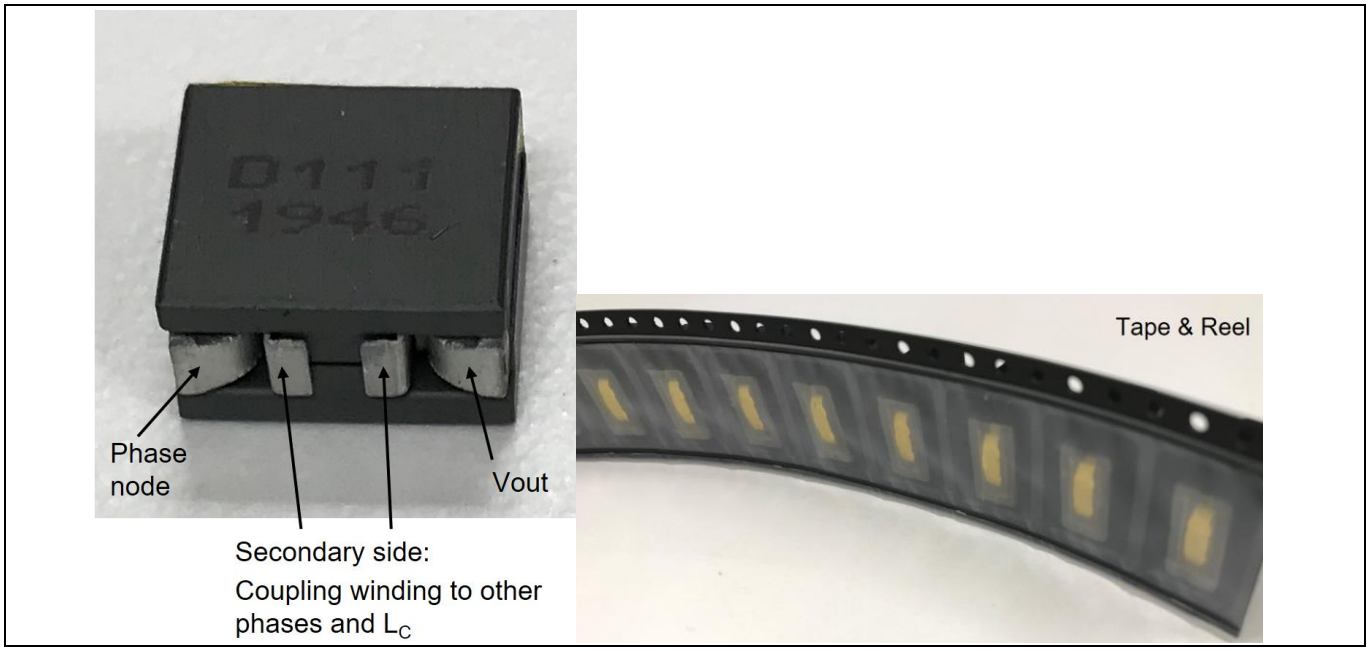

Figure 5 TLVR transformer devices (example)

2.5 TLVR coupling inductance L_C

For the selection of the coupling inductance L_C its power loss and transient behavior must be considered.

The power loss in steady-state is typically not a problem, as the coupling current is very small. The worst case is a high-frequency load-transient event, which causes repetitive high-coupling current excursions.

Worst-case current excursions in the coupling winding can be calculated when taking the load-transient event duration t_{trans_on} into account:

$$\triangle_{I\_TLVR\_Lc\_trans\_on} = k \cdot t_{trans\_on} \cdot \frac{(D_{trans} \cdot N \cdot V_{in} - N \cdot V_{out})}{L_c} \quad (50)$$

D_{trans} is the effective duty cycle considering all phases during the transient event.

The current change during load release is facing the same AC inductance as in the load increase event. That means the current response is as fast.

From the equation above one can see how the choice for L_C is affecting the duty cycle during the transient. The current rise is tied to the change in duty cycle during the step load-transient event. Using the AC inductance of the entire TLVR output filter, a calculation for the required transient duty cycle of the regulator can be derived.

In order to meet a specific transient target, the effective filter inductance has to be not more than:

TLVR circuit

$$L_{AC} \leq \frac{D_{trans} \cdot V_{in} - V_{out}}{\Delta I_{out\_transient}} \cdot \Delta t_{transient} \quad (51)$$

$$D_{trans} \geq \frac{1}{V_{in}} \cdot \left(\frac{L_{AC} \cdot \Delta I_{out\_transient}}{\Delta t_{transient}} + V_{out} \right) \quad (52)$$

Therefore, the maximum value for L_C can be calculated as:

$$L_{AC} = \frac{L_m \cdot L_c}{k^2 \cdot N^2 \cdot L_m + N \cdot L_c} \leq \frac{\Delta t_{transient}}{\Delta I_{out\_transient}} \cdot (D_{trans} \cdot V_{in} - V_{out}) \quad (53)$$

$$\frac{1}{\frac{k^2 \cdot N^2}{L_c} + \frac{N}{L_m}} \leq \frac{\Delta t_{transient}}{\Delta I_{out\_transient}} \cdot (D_{trans} \cdot V_{in} - V_{out}) \quad (54)$$

$$L_c \leq 1 \Big/ \left[\frac{1}{k^2 \cdot N^2} \cdot \left(\frac{\Delta I_{out\_transient}}{\Delta t_{transient} \cdot (D_{trans} \cdot V_{in} - V_{out})} - \frac{N}{L_m} \right) \right] \quad (55)$$

Knowing D_{trans} also allows for the calculation of the current excursion in the coupling winding.

During a load-release transient all phases may have turned on the LS MOSFET, and the transition is supported by the current ramp in the coupling loop. That means the energy in the magnetizing inductances is now driving the current into the L_C inductor. Consequently, this energy couples back through the transformer and charges the output capacitor bank.

The current in the coupling loop is ramping negative and limited to a magnitude of:

$$\Delta I_{c\_trans\_off} = t_{trans\_off} \cdot k \cdot \frac{N \cdot V_{out}}{L_c} \quad (56)$$

The built-up current is dissipating at the rate of:

$$\tau_{Lc} = \frac{L_c}{N \cdot DCR_{TLVR} + DCR_{Lc} + R_{pcb\_Lc}} \quad (57)$$

This time is normally much too long to prevent voltage overshoot from occurring. If a non-linear control method such as tri-stating all phases is deployed to prevent voltage overshoot, then the stored energy keeps recirculating in the coupling loop and decays at the time constant calculated. However, if the controller releases the tri-state condition before the current has decayed sufficiently, it will provide the stored energy to the output again, which at some load frequencies can coincide with the step-up engaging non-linear support for rising current. Together with the very small AC inductance, this can result in instability, causing higher and higher current excursions that can potentially destroy the power stages. Looking from a small-signal analysis point of view, the control loop is determined by the non-linear controls that have a much higher gain than the PID control, which causes instability of the system when there is no time to settle in between the non-linear function activity periods.

Therefore, it is not recommended to deploy non-linear control for load release.

In any case, it is critical to remain in control of the coupling current. That means the L_C must never be allowed to saturate.

If L_C saturates and the current ramps too steeply, then it is translated to all phases and will cause the TLVR transformers to go into saturation too. At this point the controller loses control of the system and the power stage observes practically a short, which can lead to the destruction of the power stage (see also comments in section 2.6).

2.6 Power stages

The power stages in a TLVR circuit are not different from a conventional circuit. The fact that the current ramp at the output is faster yields to a faster and steeper current ramp in the power stage. The peak current in a TLVR circuit is expected to be at about the same magnitude compared to the conventional circuit. When the current ramp of the output can be met, then there is little to no current needed to replenish the output capacitance in a TLVR.

Because the current rise is much faster in a TLVR power stage, the induced parasitic feedback voltages are also larger. Therefore, it is more important to use rugged power stages (such as the Infineon TDAxxxxx power stages) with proper Kelvin drive connections and dv/dt immune technologies.

With the faster current transitions, the current reporting is another important aspect. For voltage feedback one must have differential routing back to the controller to prevent noise injection. A power stage with current reporting, such as the TDA21590, is the part of choice as it is more immune to noise.

Regardless of the power stages used, it is very important in a TLVR circuit to prevent inductor and transformer saturation (as mentioned earlier), as the currents can rise much more quickly and in this case the potential for a power stage destruction is much higher.

2.7 Layout

The layout of a TLVR circuit is rather straightforward. It is very similar to a conventional design with an additional coupling loop. Since the coupling loop can have an arbitrary reference, it is most sensible to use the GND plane on the second layer as a return for the current, and route the coupling from phase to phase without any vias right on the top layer from transformer to transformer, and finally to the coupling inductor. The coupling trace width should be maximized. It is advisable to place accessible probing points on the interconnects of the coupling windings of the TLVR transformers. This is important for troubleshooting, as in some TLVR transformer designs the secondary winding terminals are not accessible.

As calculated, the voltage at the L_C inductor can reach a rather high level, which must be considered with respect to routing and choice of PCB material.

The maximum voltage at the L_C inductor can be as high as:

$$V_{Lc\_\max\_neg} = k \cdot N \cdot (-V_{out}) \tag{58}$$

$$V_{Lc\_\max\_pos} = k \cdot N \cdot (V_{in} - V_{out}) \tag{59}$$

$$V_{Lc\_\max\_abs} = k \cdot N \cdot max(V_{in} - V_{out}, V_{out}) \tag{60}$$

In reality, when the worst-case phase overlap is considered, the maximum voltage can be calculated as:

$$V_{Lc\_\max} = k \cdot max(N_{SimOnMax} \cdot V_{in} - N \cdot V_{out}, N \cdot V_{out}) \tag{61}$$

A reduction in EMI can be achieved by splitting the coupling inductance into two parts in series and referencing their common node to GND. This will reduce the absolute voltage excursion to half of the previous value. It also reduces stress on the PCB, which might be helpful at very high phase counts.

2.8 Circuit derivations

2.8.1 Dual-phase mode

When two power stage PWM inputs are driven from a common PWM output of a controller, a dual-phase operation has been set up. This mode allows for scaling up the current per phase without adding complexity to the controller and system, and simplifies routing.

TLVR circuit

One drawback is that the output ripple current becomes larger. However, at high phase counts this is not a limiting factor.

For calculating the TLVR in that mode the dual phases can be treated as one phase with twice the current.

Since two phases are running in parallel, the resulting magnetizing inductance for one PWM output is half of that of one TLVR transformer component. In the coupling loop one PWM output is now driving twice the voltage, i.e. the current ramps twice as fast per PWM. This will be represented in the calculation by dividing the coupling inductance L_C by two.

2.8.2 Multiple coupling loops

For high phase count one can consider splitting the coupling loop into multiple smaller loops.

If this method is applied in conjunction with the dual-phase mode, then one must make sure that phases connected to fire simultaneously will be in the same coupling loop. This preserves the phase balance.

Dividing the coupling loop has consequences for the coupling strength. For example, if dividing a 16-phase TLVR into two eight-phase coupled loops then the current ramp would not scale up by 16^2 but by only 2×8^2.

The calculation for steady-state currents can then be done for an eight-phase coupled system at half of the total current, assuming that the phase-to-phase angles are all the same. However, this assumption cannot be made in general, especially not when considering transient support. Therefore, it is possible that the coupling current is substantially bigger in such an arrangement compared to a system with all phases coupled in one loop.

2.9 Input capacitance

The purpose of the total input capacitance is to stabilize the input voltage for transient excursions so that the delivering power supply will observe only the average current.

In steady-state, the minimum required capacitance to deliver an average current from a source is for a single phase, given as:

$$C_{in\_1ph\_min} = \frac{I_{out} \cdot D \cdot (1-D)}{\Delta V_{in} \cdot f_{sw}} \tag{62}$$

This can also be applied to the multiphase converter considering the phase overlap:

$$C_{in\_MPB\_min} = \frac{I_{out} \cdot D_{HF} \cdot (1-D_{HF})}{\Delta V_{in} \cdot N^2 \cdot f_{sw}} \tag{63}$$

The transient load energy must be supplied from the input decoupling capacitors initially. Therefore, one can set a voltage deviation target for the transient and calculate the necessary capacitance value:

$$C_{in\_min} = \frac{\Delta I_{transient}}{\Delta V_{in\_transient}} \cdot \Delta t_{transient} \tag{64}$$

From those, the maximum value should be chosen.

By comparison to a conventional multiphase design one can estimate that with the BW improvement the transient time for the input current to rise is reduced proportionally.

From $$\frac{\Delta I_{out_{TLVR}}}{\Delta I_{out_{MPB}}} \approx \frac{L_m}{L_c} \cdot N \tag{46}$$

the minimum required input capacitance for the same conditions (assuming that was designed specifically to meet a lower input voltage limit) as in a standard multiphase buck regulator should have a total of:

TLVR circuit

$$C_{in\_\min\_TLVR} = C_{in\_\min\_MPB} \cdot \frac{L_m}{L_c} \cdot N \tag{65}$$

That implies that either a lot more input capacitance must be deployed, or that the permitted voltage excursion must be bigger. This consideration will likely be a compromise between both requirements. As today, the input capacitance is largely an arbitrary selection of bulk and MLCC capacitors, it is important to increase the value of the MLCC capacitors at each power stage in order to prevent high-frequency input currents from flowing between the phases.

For example, in an eight-phase design with $L_m = L_C$ a good trade-off would be to double the MLCC values at each power stage and also the bulk capacitors, while accepting a larger voltage dip during the transient event.

It is important to consider the total input current ripple. The ripple current calculation must consider the on-situation for the minimum simultaneous phase count and the maximum simultaneous phase count and also the absolute phase current.

The lowest input current value is at the beginning of the ramping with minimum phase count. In circuits with non-overlapping phases this is at zero, and the ramp is also zero. With overlap the minimum simultaneously on phase count is greater than zero, and hence there is initial current I_{in_init} in the system.

The current starts ramping with the minimum phase count by the following value:

$$\Delta I_{In\_NsimOnMin} = t_{nonoverlap} \cdot \left[N_{SimOnMin} \cdot \frac{V_{IN}-V_{OUT}}{L_m} + k^2 \cdot \left(\frac{N_{SimOnMin} \cdot V_{IN} - N \cdot V_{OUT}}{L_C}\right)\right] \tag{66}$$

with

$$t_{nonoverlap} = T_{HF} \cdot (1 - D_{HF}) \tag{67}$$

When the maximum phase count becomes active, the input current jumps to the value of the starting point for the steeper slope with maximum phase count. Since the valley current can be negative, this jump can go up or down. At no load current, the waveform will center around zero. Hence the DC portion to take from the first calculation is half of its value. Of course, this also applies to the second slope term. Therefore, we first calculate the second slope term before deriving the jump magnitude.

The second slope term with maximum phase count in the on-state is:

$$\Delta I_{In\_NsimOnMax} = t_{overlap} \cdot \left[N_{SimOnMax} \cdot \frac{V_{IN}-V_{OUT}}{L_m} + k^2 \cdot \left(\frac{N_{SimOnMax} \cdot V_{IN} - N \cdot V_{OUT}}{L_C}\right)\right] \tag{68}$$

The current jump magnitude is now:

$$\Delta I_{In_{PhaseStep}} = \frac{Iout}{N} - \frac{1}{2}\left(\Delta I_{In\_NsimOnMin} + \Delta I_{In\_NsimOnMax}\right) \tag{69}$$

At the end, when one phase turns off, the current falls back to the initial valley point of I_{in_init}.

This cycle repeats at f_{HF} and the resulting input ripple current is the sum of these components at a current high enough to separate the minimum and maximum phase ripples entirely:

$$\Delta I_{In\_Ripple} = \Delta I_{In\_NsimOnMin} + \Delta I_{In\_PhaseStep} + \Delta I_{In_{NsimOnMax}} \tag{70}$$

$$\Delta I_{In\_Ripple} = \frac{Iout}{N} + \frac{1}{2} \cdot \left(\Delta I_{In\_NsimOnMin} + \Delta I_{In_{NsimOnMax}}\right) \tag{71}$$

TLVR circuit

$$\Delta I_{In_{Ripple}} = \frac{Iout}{N} + \frac{1}{2}\left[\begin{array}{l} T_{HF}\cdot(1-D_{HF})\cdot\left[N_{SimOnMin}\cdot\frac{V_{IN}-V_{OUT}}{L_m} + k^2\cdot\left(\frac{N_{SimOnMin}\cdot V_{IN}-N\cdot V_{OUT}}{L_C}\right)\right] \\ +T_{HF}\cdot D_{HF}\cdot\left[N_{SimOnMax}\cdot\frac{V_{IN}-V_{OUT}}{L_m} + k^2\cdot\left(\frac{N_{SimOnMax}\cdot V_{IN}-N\cdot V_{OUT}}{L_C}\right)\right] \end{array}\right] \quad (72)$$

$$\Delta I_{In_{Ripple}} = \frac{Iout}{N} + \frac{1}{2\cdot f_{HF}}\left[\begin{array}{l} \frac{V_{IN}-V_{OUT}}{L_m}\cdot(N_{SimOnMax}-1+D_{HF}) \\ +\frac{k^2}{L_C}\cdot\left((N_{SimOnMax}-1+D_{HF})\cdot V_{IN}-N\cdot V_{OUT}\right) \end{array}\right] \quad (73)$$

The following is the simulation result of the input current waveform for a TLVR circuit with these parameters:

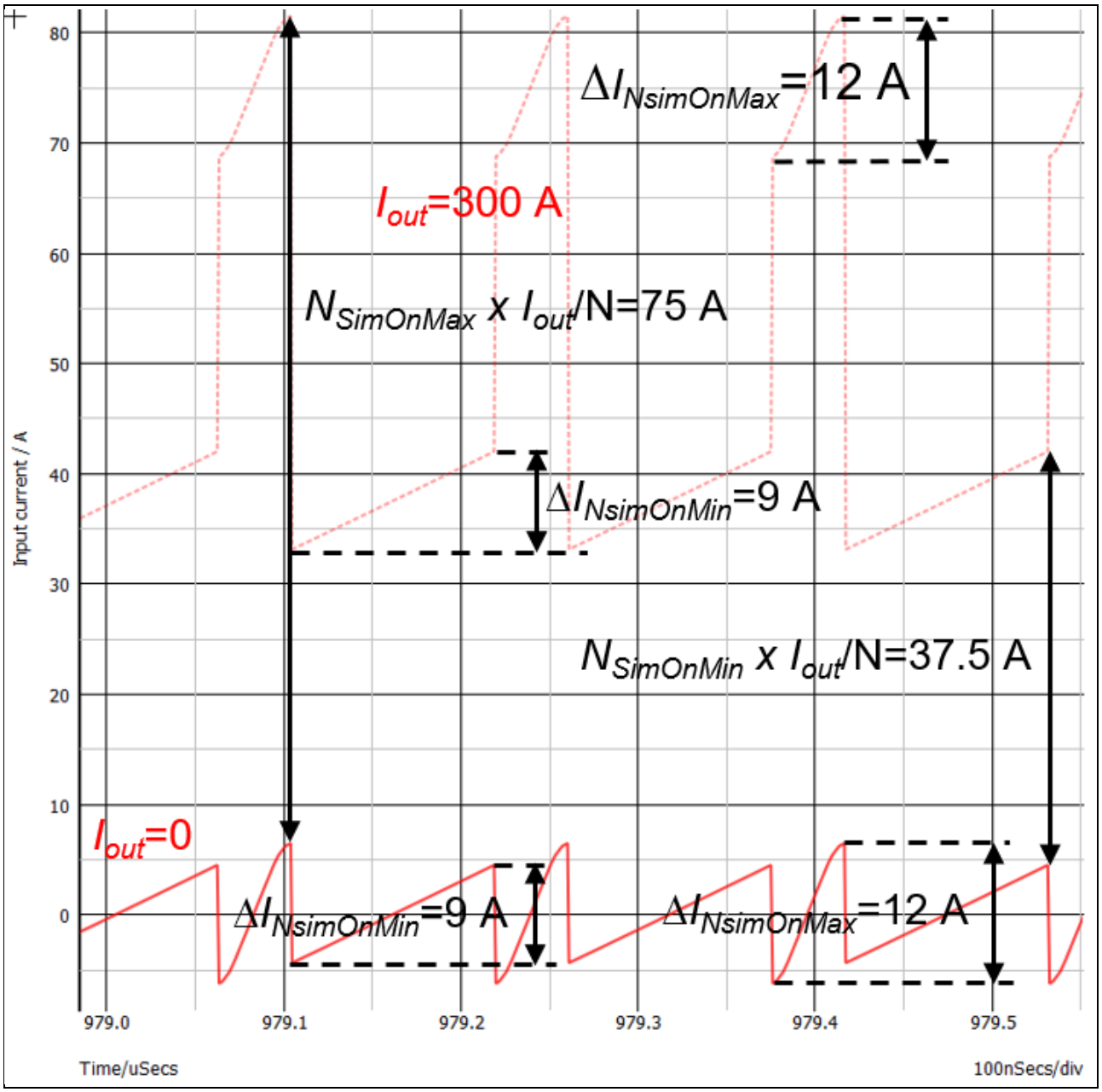

Figure 6 TLVR input current steady-state ripple simulation (800 kHz, V_{in} = 12 V, V_{out} =1.72 V, 8 phases, L_m = 100 nH, L_C = 100 nH, I_{out} = 300 A (red dashed), I_{out} = 0 (red solid)), some loss

TLVR circuit

From the simulation result, it becomes clear that the input ripple current calculation must have a conditional term looking for the ripple DC overlap. A generic approach would be to look at the absolute peak and valley of the waveform:

$$\Delta I_{In_{Ripple}} = Max\left[N_{SimOnMax}\cdot\frac{Iout}{N}+\frac{\Delta I_{In_{NsimOnMax}}}{2}, N_{SimOnMin}\cdot\frac{Iout}{N}+\frac{\Delta I_{In_{NsimOnMin}}}{2}\right] - Min\left[N_{SimOnMax}\cdot\frac{Iout}{N}-\frac{\Delta I_{In_{NsimOnMax}}}{2}, N_{SimOnMin}\cdot\frac{Iout}{N}-\frac{\Delta I_{In\_NsimOnMin}}{2}\right] \quad (74)$$

It is evident that the output current dependency is large, i.e. the worst-case ripple must be calculated at the maximum output current.

2.10 Output capacitance

The total output capacitance value must meet the ripple voltage requirement as well as the transient undershoot requirement.

$$C_{out\_\min\_ripple} \geq \frac{1}{8\cdot N\cdot f_{sw}}\cdot 1/\left(\frac{dV_{out}}{dI_{out\_pkpk}}-ESR_{Cout}\right) \quad (21)$$

$$C_{out\_\min\_trans} \geq \frac{t_{Delay}\cdot\Delta I_{Loadstep}}{dV_{out}} \quad (32)$$

$$C_{out\_\min} = Max\left(C_{out\_\min\_trans}, C_{out\_\min\_ripple}\right) \quad (75)$$

2.11 Phase shedding

Phase shedding can be deployed in a TLVR circuit as well.

When working in phase-shed mode the effective coupling inductance increases by the sum of the magnetizing inductances of the TLVR transformers of the shed phases.

This is not a problem, because the various non-linear control features acting on a steep transient will engage the shed phases, and then the magnetizing energy is coming directly from the primary side, driving up the current in the magnetizing inductance.

3 Design process

3.1 Component selection

1. Determine the required phase count to support the output current.
2. Find a controller supporting the phase count and acknowledge the control scheme (e.g. dual phase).
3. Calculate the maximum current for one phase.
4. Determine the TLVR transformer type.
5. Select the part with the highest magnetizing inductance without saturating (leave margin)
6. Calculate the required coupling inductance for your control scheme to meet the transient requirements:

$$L_c \leq 1/\left[\frac{1}{k^2 \cdot N^2} \cdot \left(\frac{\Delta I_{out\_transient}}{\Delta t_{transient} \cdot (D_{trans} \cdot \mathrm{V}_{in} - \mathrm{V}_{out})} - \frac{N}{L_m}\right)\right] \quad (55)$$

   In case transient requirements cannot be met, either additional capacitance must be accounted for, or a lower value for the TLVR transformer magnetizing inductance must be selected.

7. Calculate the phase ripple current to ensure that the transformer does not saturate:

$$\Delta I_{ph_{pkpk}} = \frac{V_{in}}{f_{sw}} \left[\frac{1}{L_m} \cdot (1 - D) \cdot D + \frac{k^2}{L_c}\left(\frac{N_{SimOnMax}}{N} - D\right) \cdot D_{HF}\right] \quad (15)$$

8. Calculate the transient current excursion in the coupling winding and make sure that the chosen coupling inductance does not saturate:

$$\Delta I_{Lc\_pkpk} = k \cdot (N_{SimOnMax} \cdot V_{in} - N \cdot V_{out}) \cdot \frac{D_{HF}}{L_c \cdot f_{HF}} \quad (11)$$

9. Determine the required minimum output capacitance for meeting the output voltage ripple requirements:

$$C_{out\_\min} = Max\left(C_{out\_\min\_trans}, C_{out\_\min\_ripple}\right) \quad (75)$$

10. Check that the total output capacitance is the maximum of the capacitances calculated in points 6 and 9.
11. Calculate the required input decoupling capacitance:

$$C_{in\_min} = \frac{\Delta I_{transient}}{\Delta V_{in\_transient}} \cdot \Delta t_{transient} \quad (64)$$

12. Calculate the input current ripple and select appropriate input decoupling capacitors based on that computation:

$$\Delta I_{In_{Ripple}} = Max\left[N_{SimOnMax} \cdot \frac{Iout}{N} + \frac{\Delta I_{In_{NsimOnMax}}}{2}, N_{SimOnMin} \cdot \frac{Iout}{N} + \frac{\Delta I_{In_{NsimOnMin}}}{2}\right]$$
$$- Min\left[N_{SimOnMax} \cdot \frac{Iout}{N} - \frac{\Delta I_{In_{NsimOnMax}}}{2}, N_{SimOnMin} \cdot \frac{Iout}{N} - \frac{\Delta I_{In\_NsimOnMin}}{2}\right] \quad (74)$$

3.2 Controller tuning

Follow these steps to tune a TLVR circuit:

1. Disable all non-linear support features.
2. Set the compensation parameters (PI or PID coefficients, depending on the controller) to a stable parameter set.
3. Calculate the maximum required duty cycle and set this with some margin as a limit in the controller.
4. Look for overshoot situations within the desired load-transient range.
5. Use the AVP BW settings and PID values to meet the targets; **do not apply non-linear load-release transient support**, as it will cause a very strong reaction that might result in non-linear undershoot support. (Toggling between non-linear functions causes instability at high current levels, with possible destruction of power stages!)
6. Find worst-case undershoot conditions and apply non-linear undershoot support only as needed. (Non-linear support always acts in a very aggressive manner compared to the standard multiphase solution!)
7. Sweep across the entire frequency range to ensure there are no conditions that violate the output specifications.

4 Support

For calculating the TLVR circuit parameters, one can use a spreadsheet calculation or simply simulate the circuit with a simulation tool such as Simetrix.

For a general understanding, it is best to run an open-loop setup on multiple phases, for example:

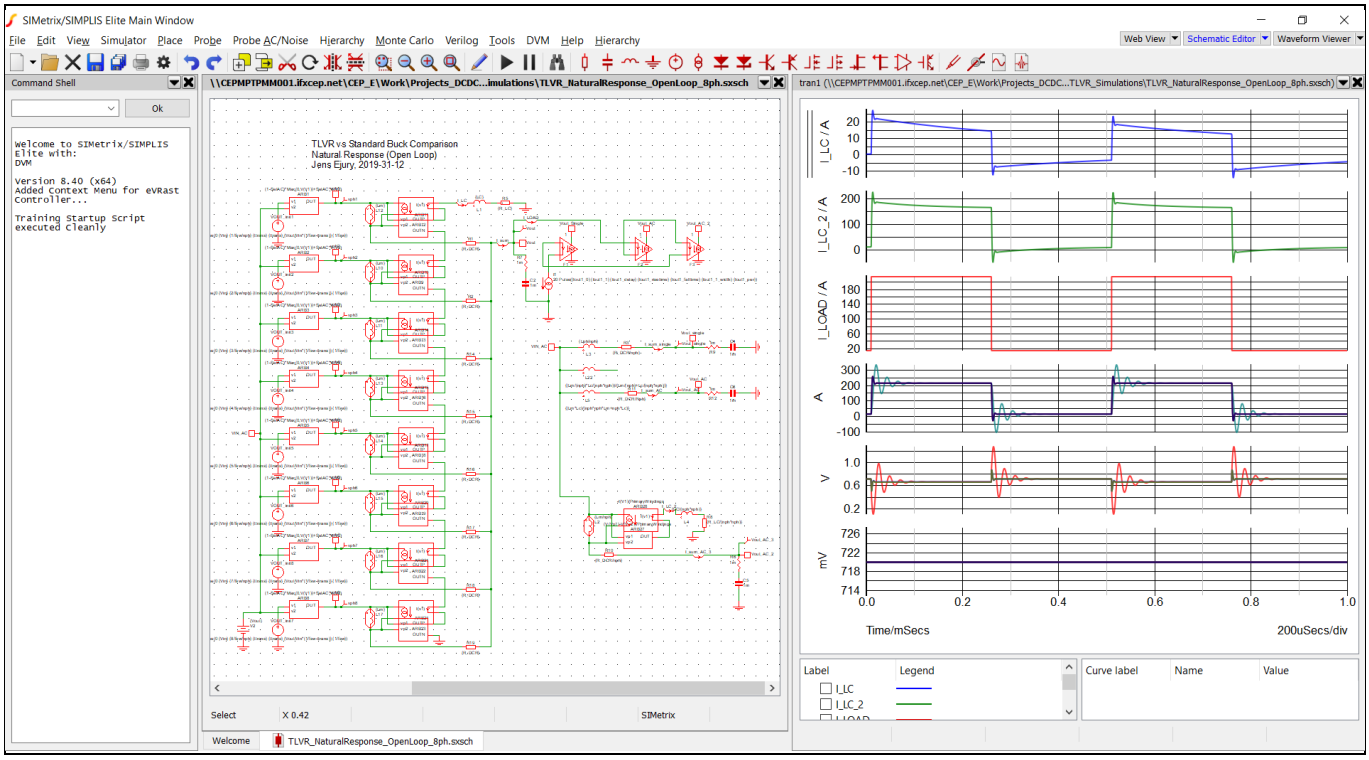

Figure 7 Simetrix open-loop simulation

The figure above shows a comparison between a standard multiphase buck regulator and a TLVR circuit with the same phase count and parameters.

Support

Most of the calculations given in this document have been compiled in a spreadsheet tool to obtain results very quickly. This provides immediate output of relevant current waveforms in steady-state and allows for transient control assumptions that will lead to transient current waveforms and data.

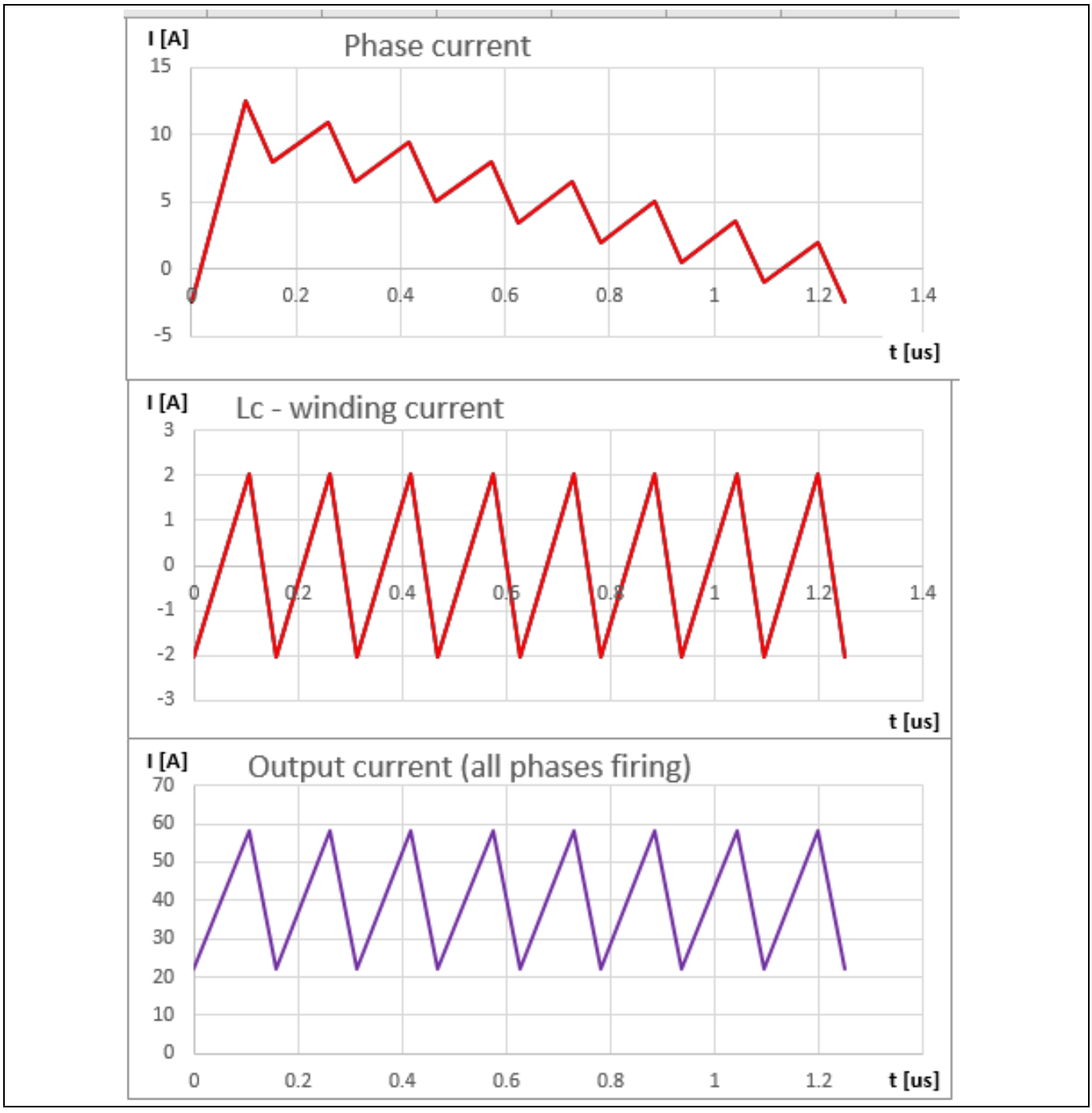

Figure 8 TLVR steady-state current waveforms from spreadsheet

5 FAQ

Q: Can I design a TLVR but have a fallback solution on the same board?

A: Yes, but the fallback solution must account for the required output capacitors of the standard solution. It also requires a very different controller configuration.

Q: Can I deploy non-linear load-release support features?

A: No, this is not recommended as it is too strong, leading to potential instability in some load conditions (see page 14, section 2.5).

Q: I noticed that my input capacitors are getting hot, why is that?

A: The steady-state ripple is comparable to the standard multiphase solution. At high dynamic transient repetition rates the output current is much more directly supported by the power train, and so also causes a high input current ripple. It is important to deploy more MLCC per phase (e.g. double the value) and have a few more bulk capacitors to absorb the current ripple (see page 17, section 2.9).

Q: Why am I seeing power stage failures during controller tuning?

A: Follow the tuning process outlined here. Before starting to tune, disable all non-linear control features and work with the PID only. Make sure that the magnetic components do not saturate at any load condition (see page 22, section 3.2).

Q: Will there be a higher voltage stress on components with TLVR?

A: The highest voltage in a TLVR circuit occurs in dynamic load situations on the L_C in the coupling winding (see page 17, section 2.8.2). If a concern arises, it is recommended to split the coupling inductance into two separate inductors located at opposite ends of the phase array.

Q: What is the required trace width of the coupling loop?

A: The coupling loop trace width should be as wide as possible to provide a good connection and minimize impedance. It should not have vias to parallel layers (see page 16, section 2.7).

Q: What needs to be considered for the saturation current of the TLVR transformer?

A: The maximum phase current at any point in time is the determining current to look for (see paragraph 2.1, equation (18)).

6 References

[1] “Fast multi-phase trans-inductor voltage regulator”, Technical Disclosure Commons (May 9, 2019), https://www.tdcommons.org/dpubs_series/2194

Revision history

Document version	Date of release	Description of changes
V 1.0	12-01-2020	First release
V 1.1	08-31-2021	Section 2.1 description of operation updated, fig 1 updated waveform
V 1.2	12-02-2021	Page 12, wording and equations 48 and 49 updated

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