IRPS5401 Register Map (Rev 02 and R3 Silicon[1])

CONTENTS:

Note 1: Silicon Revision can be read in register 0x00FC[15:8].

16-bit Register Convention

The convention used throughout this document is:

- 'h' or '0x' indicates that the number is expressed in hexadecimal
- 'b' indicates that the number is expressed in binary
- 'd' indicates that the number is expressed in decimal
- Bit 15 is the Most Significant Bit (MSB) in the register
- Bit 0 is the Least Significant Bit (LSB) in the register

Quite often, a 16-bit register is broken into several small pieces and each piece is used for a different function. The convention used in the document uses the following format:

Address	Bits	Function Name
0x0020	15	i2c_use_addr_offset
	[14:8]	i2c_device_addr
	7	i2c__add_data_delay
	[6:0]	pmb_device_addr

The example above indicates that

- Register 0x0020 is broken into 4 functions:
    - i2c_use_addr_offset uses bit 15
    - i2c_device_addr uses bits 8-14
    - i2c_add_data_delay uses bit 7
    - pmb_device_addr uses bits 0-6

While each register is considered to be 16-bits, they are addressed in an 8-bit format. For example, when we refer to register address 0x0020, we are actually refering to addresses 0x0020 AND 0x0021 since each individual register is 8-bits wide.

From a user's perspective, the Rocky Reg Map is byte-addressable. The interface supports both 8 and 16-bit accesses, and registers can be written to or read from in either format.

Also note the endianness of each data word. The format is using what is called the "Little-endian" convention, where the higher byte is to the left and the lower byte is to the right . Therefore when reading register 0x0000 which contains data 0xAA55, it should be interepted as register 0x0001 contains 0xAA and 0x0000 contains 0x55.

Register Map Sections

The register map is organized into three sections. Common, where functions are shared for all loops, and Loop A, B, C, D and LDO, where functions are specific to each loop. Each section contain Trim, User, Read Only, and Read/Write registers. They also contain registers that support PMBus.

Section	Registers	Base Address
Common *(Apply to all outputs)*	Config, Trim and User	0x0000
	Reserved	0x0200
Loop A *PMBus Page 0*	Trim and User	0x0400
	PMBus Registers	0x0600
Loop B *PMBus Page 1*	Trim and User	0x0800
	PMBus Registers	0x0A00
Loop C *PMBus Page 2*	Trim and User	0x0C00
	PMBus Registers	0x0E00
Loop D *PMBus Page 3*	Trim and User	0x1000
	PMBus Registers	0x1200
Loop LDO *PMBus Page 4*	Trim and User	0x1400
	PMBus Registers	0x1600

Common Reg Map Section

OTP Config Registers

otp_config_registers		
ADDR OFFSET	**CONTENTS**	**RST**
0	**[15:12] reserved**	0
	[11:8] cnfg_nvm_prog_max: Defines the maximum number of USER images that can be selected by the MTP pin. If the value specified on the MTP pin exceeds this value, the value in this register will be used. Set this register to 0 to disable this feature.	0
	[7:0] reserved	00
2	**[15:0]** reserved	0000

OTP Trim Registers

otp_trim_registers		
ADDR OFFSET	**CONTENTS**	**RST**
8	**[15] vcc_uv_th:** Sets the undervoltage thresholds for both Vcc and Vdrv. 0=[4.2, 3.9] V, 1=[4.0, 3.7] V.	0
	For Infineon Production Use Only	04
	[7:0] product_id_otp[7:0]: Product ID code. IRPS5401 = 0x52	52
a	*For Infineon Production Use Only*	8000
c		8020
e		A828
10		0000
12		0000

OTP USR Registers

otp_usr_registers		
ADDR OFFSET	**CONTENTS**	**RST**
20	**[15] Reserved** **[14:8] i2c_device_addr[6:0]:** Sets the I2C device address. If set to 0, the I2C interface is effectively disabled. In test mode, the chip also accepts a default value of 0x0A (7-bit address). Locked by register *i2c_pmb_addr_lock*. Reserved I2C/SMBus addresses: (0x00 to 0x07), 0x08, 0x0c, 0x28, 0x37, 0x61, (0x78 to 0x7F). rst:0010000 **[7] Reserved** **[6:0] pmb_device_addr[6:0]:** Sets the PMBus device address. If set to 0, the PMBus interface is effectively disabled. rst:1000000	1040
22	**[15] pad_input_thresh_sel_for_enable_pins:** Sets the input threshold level (0= TTL, 1= VTT) for the 5 ENABLE pins and the SLEEP_N pin. {'ttl levels'=>0, 'vtt levels'=>1} rst:1 **[14] pad_input_thresh_sel:** Sets the input threshold level (0= TTL, 1= VTT) for the SYNC_CLK input pin. { choose_ttl_levels=>0, choose_vtt_levels=>1, } rst:1 **[13] SW_A_use_internal_driver:** Choose internal/external driver. {external_driver=>0, internal_driver=>1,} rst:0 **[12] combine_outputs_c_d:** Set this bit to combine switchers C and D as a single output. rst:0 **[11] por_arming_clk_en:** Enable the POR arming clock (24 MHz). rst:0 **[10] Reserved** **[9] por_sleep_mode_en:** This bit prepares the Power-On Reset circuit to act on the SLEEP input pin. rst:0 **[8:6] telemetry_bw[2:0]:** Telemetry bandwidth for input and output currents, input and output voltages, and temperatures. {'0.97hz'=>0, '1.94hz'=>1, '3.88hz'=>2, '7.78hz'=>3, '15.57hz'=>4, '31.2hz'=>5, '62.66hz'=>6, '126.34hz'=>7} rst:111 **[5:3] int_dr_min_pw[2:0]:** The minimum pulse width for internal driver pwm signal = (int_dr_min_pw+1)*10 ns. rst:011 **[2:0] ext_dr_min_pw[2:0]:** The minimum pulse width for external driver pwm signal = (ext_dr_min_pw+1)*10 ns. rst:011	C1DB
24	**[15:13] reserved[2:0]:**must be 0 **[12] d2a_irs_disable_internal_regulator:** Disable the internal 5V regulator. Set this to a 1 if using an EXTERNAL 5V supply for VCC power rst:0	8500

[11] Reserved:

[10] vcpu_high_release_en: Enable the release of the low-side FETs if the output voltage is below 250 mV after a VCPU high fault. {'dont release'=>0, 'release'=>1} rst:1

[9] vdrv_uv_en: Enable Vdrive undervoltage fault protection. The threshold is set by register *vcc_uv_th*. rst:0

[8] vcc_uv_en: Enable VCC undervoltage fault protection. The threshold is set by register *vcc_uv_th*. rst:1

[7:6] write_protect_mode[1:0]: Select the REGMAP write protection mode. See the table below for details. rst:00

[5:4] read_protect_mode[1:0]: Select the REGMAP read protection mode. See the table below. rst:00

[3:2] write_protect_section[1:0]: Select the REGMAP section to be write protected. Writes to protected registers will be ignored. rst:00

[1:0] read_protect_section[1:0]: Select the REGMAP section to be read protected. Reads from protected registers will return 0xFFFF.

		read_protect_mode / write_protect_mode
value	**mode**	**description**
3	ALWAYS	access protection is enabled and the pin and password are ignored
2	PIN + PASSWORD	access protection is enabled when the PROT pin is asserted OR the password is set
1	PIN	access protection is enabled when the PROT pin is asserted
0	PASSWORD	access protection is enabled when the password is set
		write_protect_section
value	**section**	**protected registers**
3	ALL	all USER registers
2	*rsv*	*reserved*
1	CONFIG	all USER registers backed by NVM *(otp_trim, otp_usr and PMBus registers)*
0	NONE	write protection is disabled
		read_protect_section
value	**section**	**protected registers**
3	ALL	all USER registers
2	Telemetry	all except Telemetry registers: fail codes, *vaux_supply, vcc_value, temperature_value_[0,1], total_input_power*, PMBus: VOUT_MODE, STATUS and telemetry
1	CONFIG	all USER registers backed by NVM *(otp_trim, otp_usr and PMBus registers)*
0	NONE	read protection is disabled

26	**[15:8] ecs_offset_ref_code[7:0]:** 8-bit reference code that overrides the offset code that is	5200

	captured at startup when *rst_is_null* is low. rst:01010010 **[7:0] ecs_scale[7:0]:** Scale factor trim to convert ADC output code to output current in Amps (external current sense). Q = 2^-10. rst:00000000	
28	**[15] ecs_override_offset:** Use the 8-bit trim *ecs_offset_ref_code* instead of the reference code captured at startup time. rst:0 **[14] low_speed_pbal_en:** Enable low speed phase current balance when loops C & D are coupled. rst:1 **[13:8] ldo_iin_bias_current[5:0]:** Input bias current for the LDO. rst:000000 **[7] global_fault_en:** When set, any fault that causes one output to shut down will cause all outputs to shut down. rst:0 **[6] sst_off_at_0v:** Determines the state of the PMBus STATUS_WORD[OFF] bit when regulating at 0V. rst:0 **[5] Reserved:**. rst:0 **[4] i2c_scl_deglitch_en:** Enable the digital SCL deglitcher, for use in sampling data bits. rst:0 **[3] i2c_sda_deglitch_en:** Enable the digital SDA deglitcher, for use in Start and Stop symbol detection (not used for data bits). rst:0 **[2] i2c_take_addr_from_ext:** 0= the I2C device address is taken directly from the NVM. 1= the address is set by the NVM value plus an offset determined by an external resistor. {nvm_plus_ext_resistor=>1, nvm_only=>0, } rst:1 **[1] i2c_add_dout_hold:** Debug only. Provide additional output data hold time (300ns/30ns minimum) on the I2C bus. rst:0 **[0] i2c_high_speed_mode:** By default, we provide additional input data hold time (Thd_dat) on the I2C bus. To run the bus in High Speed mode, set this bit to disable the additional hold delay. {normal_and_fast=>0, high_speed=>1, } rst:0	4004
2a	**[15:0] gpr_customer[15:0]:** General purpose register for customer use. rst:0000000000000000	0000
2c	**pmb_mfr_id[15:0]:** The 16-bit ASCII code for the manufacturers ID. ASCII='IR', hex=0x4952, decimal=18770. rst:0100100101010010	4952
2e	**[15:8] Reserved[7:0]:** reserved rst:00000000 **[7:0] pmb_mfr_id_1[7:0]:** The 8 MSBs of the 24-bit ASCII code for the manufacturers ID. rst:00000000	0000
30	**[15:0] pmb_mfr_model_0[15:0]:** Manufacturer model (16 LSBs). rst:0000000001010010	0052
32	**[15:0] pmb_mfr_model_1[15:0]:** Manufacturer model (16 MSBs). rst:0000000000000000	0000

34	**[15:0] pmb_mfr_revision_0[15:0]:** Manufacturer revision (16 LSBs) rst:0000000000000010	0002
36	**[15:0] pmb_mfr_revision_1[15:0]:** Manufacturer revision (16 MSBs) rst:0000000000000000	
38	**[15:14] Reserved** **[13:12] pmb_pec_mode[1:0]:** PMBus PEC mode. In mode 0 (automatic mode), the logic sinks/sources a PEC byte if the bus master strobes an extra byte following a normal transfer. In mode 1 (PEC Off), inclusion of a PEC byte will cause a CML error (Invalid/Unsupported Data) . In mode 2 (PEC On), omission of a PEC byte will cause a CML error (Other Communication Fault). {automatic_pec=>0, pec_off=>1, pec_always_on=>2,} rst:00 **[11] Reserved:** rst:0 **[10] pmb_nak_while_nvm_busy:** Tell Rocky to NAK all PMBus traffic while the NVM is busy. rst:0 **[9] pmb_no_cml_on_bus_scan:** Set this to prevent CML faults for too-short commands produced by unenlightened I2C/PMBus bus scans. The CML will be latched on the most recently accessed page. rst:0 **[8] pmb_page_plus_latch_new_page:** When set, the Page received in a PAGE_PLUS PMBus command will be retained. Otherwise the Page number will revert to the previous value after the current command completes. rst:0 **[7:6] Reserved:** rst:0 **[5] auto_low_power_en:** Set this bit to allow Rocky to enter low-power mode when the output is disabled. This bit is shared by all outputs. With this bit = 1; all outputs will have a 500usec start-up delay and OVP with ENABLE LOW will be inactive. rst:0 **[4:0] disable_output[4:0]:** Bitfield to disable the Switchers and the LDO ([4]=LDO, [3]=Switcher D, [2]=Switcher C, [1]=Switcher B, [0]=Switcher A.). These bits should only be asserted when their respective outputs are off. They should not be used to enable/disable the outputs. rst:00000	0000
3a	**[15:0] user_password[15:0]:** A 16 bit password that provides read/write protection for the USER section in all REGMAPs. Use of this password is enabled by the Protect Section and Protect Mode registers. This register resets to zero, which is the default password. Once the password is set, access protection is enabled until *user_try_password* is set to the same value. rst:0000000000000000	0000

Read Only Registers

read_only_registers	
ADDR OFFSET	**CONTENTS**
50	**[15] Reserved** **[14] vcc_uv_fault:** Indicates Vcc undervoltage fault. **[13] low_speed_pbal_saturation:** Indicates that currents in phases C and D are highly imbalanced. **[12:8] chip_enables[4:0]:** Displays the state of the synchronized and debounced ENABLE pin for each output. [4]=LDO, [3]=Switcher D, [2]=Switcher C, [1]=Switcher B, [0]=Switcher A. **[7] osc_trim_pass:** Oscillator trim result. **[6] vdrv_uv:** Indicates an undervoltage fault on Vdrv. **[5:4] misc_adc_rflag[1:0]:** Underflow/Overflow flags from the miscellaneous ADC. **[3:0] madc_addr_filt[3:0]:** ADC reading of the VR address (filtered and decoded).
52	**[15:13] Reserved** **[12] nvm_read_no_image:** This flag is set when the user attempts to read an invalid or unavailable image from NVM, in any Section. If an image is read correctly, the *nvm_xxx_loaded* flag for the corresponding Section is set. If multiple images are being read, this flag reflects the last Section read (CNFG is read first, then TRIM, then USER). This flag remains set until the next NVM operation. Note that when a device with a blank NVM powers up, this flag will be asserted. **[11:8] nvm_user_image_sel[3:0]:** Shows the User image that was restored following a power-on reset. This value depends on the voltage sensed at the ADDR pin, plus the value in register *cnfg_nvm_prog_max*. **[7] Reserved** **[6:4] nvm_crc_err[2:0]:** One-hot bitfield shows when a CRC error was detected when reading a CNFG (bit 0), TRIM (bit 1) and/or USER (bit 2) image from NVM. **[3] Reserved** **[2] nvm_user_loaded:** Indicates that the USER registers have been restored from the NVM. **[1] nvm_trim_loaded:** Indicates that the TRIM registers have been restored from the NVM. **[0] nvm_cnfg_loaded:** Indicates that the CNFG registers have been restored from the NVM.
54	**[15:12] nvm_prog_soak_cnt[3:0]:** Indicates the number of NVM Program operations that did not succeed. The NVM word size is 32 bits, and the bits are programmed one at a time. After all bits in a word are programmed, the word is read back and verified. This register is incremented if the verify operation fails. Any bit that was not programmed successfully is subjected to multiple *soak* operations. This register indicates the total number of times that at least one bit within a word was not programmed successfully. The *soak* may be executed multiple times per word. After 10 failed attempts, Rocky will declare defeat and wave the *nvm_prog_fail_flag*. **[11] nvm_prog_fail:** If a bit in the NVM fails to program successfully, the hardware automatically retries that same bit up to 10 times. If the bit cannot be programmed, the program operation aborts and this bit is set. The flag remains asserted until the next NVM operation.

	[10] nvm_prog_invalid_image: This flag indicates an attempt to program an image that has already been programmed, or an image that does not exist. The flag remains asserted until the next NVM operation. **[9] nvm_array_clean_fail:** This flag indicates that the Array Clean operation failed. The flag remains asserted until the next NVM operation. **[8] nvm_test_op_err:** Set when an NVM Test operation is attempted while the TRIM password is engaged. **[7:0] nvm_calc_crc[7:0]:** The value of the CRC byte calculated over the register values during the most recent NVM operation. For reads, this value will be zero if the images are restored without errors. For writes, the register will contain the value of the calculated CRC byte.
56	**[15:14] Reserved** **[13:8] nvm_num_user_images[5:0]:** Shows the total number of USER images that can be stored in the NVM. This is independent of *prog_max* and the MTP pin. **[7:5] nvm_ptr_trim[2:0]:** 3-bit bitfield indicating which TRIM images have been programmed. This register will be 0 for a new, unprogrammed part. It will be 7 ('b111) when all 3 Trim images are programmed. **[4:0] nvm_ptr_cnfg[4:0]:** 5-bit bitfield indicating which CNFG images have been programmed. This register will be 0 for a new, unprogrammed part. It will be 0x1F ('b11111) when all 5 CNFG images are programmed.
58	**[15:0] nvm_ptr_user_msb[15:0]:** The 16 MSBs of the USER pointer.
5a	**[15:0] nvm_ptr_user_lsb[15:0]:** The 16 LSBs of the USER pointer, which is a 32-bit bitfield indicating which USER images have been programmed.
5c	**[15:12] madc_mtp_filt[3:0]:** Filtered ADC output for MTP that is decoded into a 4 bit value. **[11:0] filtered_mtp_code[11:0]:** This is the filtered ADC code corresponding to MTP (during init_measure) or VoutE (other times). Used for low-speed ADC calibration.
5e	**[15:14] Reserved** **[13:9] ro_salert[4:0]:** Reflects the state of the active-high ALERT signal for each output. [4]=LDO, [3]=Switcher D, [2]=Switcher C, [1]=Switcher B, [0]=Switcher A. **[8:0] temperature_value_0[8:0]:** Filtered temperature value for sensor 0. Q=1C. Signed 2s complement. This sensor is used by SW A and B.
60	**[15:9] Reserved** **[8:0] temperature_value_1[8:0]:** Filtered temperature value for sensor 1. Q=1C. Signed 2s complement. This sensor is used by SW C, D and the LDO.
62	**[15:8] vdrv_value[7:0]:** The filtered value of Vdrv. Q=1/32 V. **[7:0] vcc_value[7:0]:** The filtered value of Vcc. Q=1/32 V.
64	**[15] sync_in_range:** 1=Sync clock is within range of the programmed local period (within 6.25% to lock, out of 12.5% to unlock). 0 = Sync clock out of range. **[14:13] sync_state[1:0]:** 0 = use local clock, 1 = locking to sync clock, 2 = use sync clock, 3 = locking to

	local clock. **[12:0] total_input_power[12:0]:** The sum of the input power of all 5 outputs. [u10.3] (1/8 W).
66	**[15:12] a2d_vindiv_lv_sel[3:0]:** the state of the Vin divider ratio based on the output from the VIN_DIV_SEL_CKT **[11:10] Reserved** **[9:0] a2d_lsadc_output_dly[9:0]:** This is the 10-bit output of the low-speed ADC, flopped once with clk_6m.
68	**[15:8] Reserved** **[7:0] pmb_capability[7:0]:** PMBus Capability command value.
6a	**[15:8] Reserved** **[7:0] pmb_revision[7:0]:** PMBus Revision command value (0x22).
6c	**[15:2] Reserved** **[1] trim_password_correct:** Indicates that *trim_password* matches *trim_try_password* **[0] user_password_correct:** Indicates that *user_password* matches *user_try_password*

Read Write Registers

read_write_registers		
ADDR OFFSET	**CONTENTS**	**RST**
70	*For Infineon Production Use Only*	0000
72		0000
74		0000
76		0000
78		0000
7a		03c0
7c		0000
7e		0000
80		0000
82		0000
84		1F00
86	**[15:4]** *For Infineon Production Use Only* **[3]** **write_protect_forever_override:** This bit overrides the LOCK_FOREVER setting in the *write_protect_mode* register. It must be set before setting the protection mode, lest the user be unable to access it. This bit is useful when preparing to program an NVM image with LOCK_FOREVER mode. It allows the user to set the mode but maintain register access. When this bit is cleared and the image is restored from NVM, the protection will be in force. rst:0 **[2]** **i2c_pmb_addr_lock:** This bit prevents write access to the I2C and PMBus device address registers in *regmap_common*. rst:1 **[1]** **ir_debug_lock:** A logic 1 locks the debug registers in the read/write section. rst:1 **[0]** **ir_trim_lock:** This bit prevents write access to the TRIM section of all regmaps (*regmap_common, regmap_loop_N* and *regmap_ldo*). rst:1	0007
88	**[15:0]** **nvm_command[15:0]:** NVM Manager Command register. See Rocky Programming	0000

Guide, AN0034, for additional information.

The NVM_COMMAND register

field	bits	encoding	description
Done	15	1	Command has completed
		0	Ready (or command is in progress). Set this bit to zero when issuing a new command.
Error	14	1	An error occurred during a previous NVM operation. See the other NVM status registers for additional information
		0	The previous operation completed successfully
Image	13:8		image number to be accessed (0x3F = use the most recent image)
Section	7	rsv	This bitfield specifies the NVM section(s) to be accessed. Examples: to read just the TRIM section, set this field to 'b0010. To read the CNFG, TRIM and USER sections, set this field to 'b0111.
	6	USER	
	5	TRIM	
	4	CNFG	
Opcode	3:0	15 - 3	*reserved*
		2	PROGRAM: write the values from the REGMAPs into the NVM
		1	READ: restore the values from NVM to the REGMAPs.
		0	IDLE: nop

8a	**[15:0] trim_try_password[15:0]:** The value in this register must match the value in *trim_password*, lest the read and write protection mechanisms will be enabled. The TRIM password will be locked after 4 failed attempts to set the correct password. rst:0000000000000000	0000

8c	**[15:0] user_try_password[15:0]:** The value in this register must match the value in *user_password*, lest the read and write protection mechanisms will be enabled. The USER password will be locked after 4 failed attempts to set the correct password. rst:0000000000000000	0000
8e	*For Infineon Production Use Only*	0000
90		0000
92		0000
94		0000
96		0000
98		0000

USR Read Only

usr_read_only	
ADDR OFFSET	**CONTENTS**
fa	**[15:0] gpr_ro_usr_0[15:0]:** read only customer register, reflects the contents of the gpr_customer register.
fc	**[15:8] silicon_ver[7:0]:** The silicon version. **[7:0] product_id[7:0]:** The product ID. IRPS5401 = 0x52

Loop A, B, C, and D Reg Map Section

Loop A base address: 0x0400
Loop B base address: 0x0800
Loop C base address: 0x0C00
Loop D base address: 0x1000

NOTE:

- ✓ The registers presented in pages 15 through 19 apply to switching outputs loop A to Loop D.
- ✓ The "ADDR OFFSET" in the table below (shown in hex code) represents the offset that needs to be added to the base address of the particular loop to access the registers associated with that loop.

OTP Trim Registers

otp_trim_registers		
ADDR OFFSET	**CONTENTS**	**RST**
0	*For Infineon Production Use Only*	A040
2		8077
4		601F
6		0079

OTP USR Registers

otp_usr_registers		
ADDR OFFSET	**CONTENTS**	**RST**
20	[15:8] **iin_offset[7:0]:** A fixed offset to adjust the estimated input current. This is a fixed component of the adjustment. 2s complement Q = 1/64 A (external driver) or 1/512 (internal driver). rst:0000 rst:00000000 [7:4] **Reserved[3:0]:** rst:0000 [3:0] **kpole1[3:0]:** Single-phase pole1 coefficient. Bandwidth ~ (kpole1+1)*120.5 KHz. All 1s bypasses the pole. rst:0000	0000
22	[15:14] **gpr_loop_usr_0[1:0]:** general purpose register. rst:00 [13:8] **kp[5:0]:** Single-phase proportional coefficient. Value = (4+loop_1_kp[1:0]) * 2^(loop_1_kp[5:2]-9). rst:100100 [7:6] **gpr_loop_usr_1[1:0]:** general purpose register. rst:00 [5:0] **ki[5:0]:** Single-phase integration coefficient. Value = (4+loop_1_ki[1:0]) * 2^(loop_1_ki[5:2]-21). rst:101010	242A
24	[15:14] **Reserved[1:0]:** reserved rst:00 [13:8] **kd[5:0]:** Single-phase differentiation coefficient. Value = (4+loop_1_kd[1:0]) * 2^(loop_1_kd[5:2]-6). rst:000000 [7:4] **Ie_th[3:0]:** error threshold to go from discontinuous to continuous mode. Threshold = (3+val)*4 mV over diode_emu_thresh. rst:0001 [3:0] **kpwm[3:0]:** coefficient for pulse width modulation. Value = (kpwm+1)/16 rst:0101	0015
26	[15] **vin_uvp_en:** Enable Vin undervoltage fault protection. rst:1 [14:12] **diode_emu_thresh[2:0]:** Error threshold to start a pulse during diode emulation. The resolution is 3mv. rst:000 [11] **fixed_ovp_thresh:** Sets the fixed Over-Voltage protection (Fixed-OVP) threshold. 0= 1.375V, 1= 2.75V. rst:1 [10:8] **diode_emu_pw[2:0]:** Fixed pulse width 'on' time during diode emulation. The pulse width = CCM pulse width * (1 + val/16), rounded to the nearest multiple of 20.8 ns. rst:100 [7:6] **post_de_pw[1:0]:** The width of the first pulse after exiting DCM as a ratio of the DCM pulse width. 0=>4/8, 1=>5/8, 2=>6/8, 3=>1 rst:10 [5:0] **inductor_ni_thresh[5:0]:** Total current threshold below which it is assumed that the inductor current has a negative component. Resolution=1/4 A for external driver, 1/32 A for internal driver. rst:000000	8C80

<table>
<tr>
<td>28</td>
<td>
[15] d2a_pws_drv_sel: Power stage driver select. 1= 3x the drive impedance for both directions on HS-Driver and pullup on LS Driver, 0= normal drive inpedance (~0.25-Ohms).
[14:12] d2a_ecs_gain[2:0]: Controls the External Current Sense gain for loop A only
<table>
<tr><th>d2a_ecs_gain</th><th>gain</th></tr>
<tr><td>0</td><td>10</td></tr>
<tr><td>1</td><td>20</td></tr>
<tr><td>2</td><td>30</td></tr>
<tr><td>3</td><td>40</td></tr>
<tr><td>4</td><td>50</td></tr>
<tr><td>5 - 7</td><td>reserved</td></tr>
</table>
[11] phase_pulldn_en: 1=enable pulldown of a phase in tristate if output voltage is < 1 V.
[10] min_off_time: Minimum off time for the PWM signal. 0=60ns, 1=100ns. rst:1
[9] d2a_lv_en: 1=enable accurate digital measurement of Vin below 3.5V (divider ratio set to 3:14). 0 = default divider ratio of 1:14 (use this setting for Vin > 3.5V). rst:0
[8] ecs_null_below_200mv: Nulls isense input when VID is below 200mV. rst:0
[7:4] dutyc_adj[3:0]: This register is used to adjust the measured dutycycle to compensate for a non ideal driver. 2s complement, Unit 1/256 (or ~0.4%). Only changes input current calculation. rst:0000
[3:0] de_off_time_adj[3:0]: Reduction in the diode emulation off time, to adjust for some drivers. Q=62.5 ns rst:0000
</td>
<td>0C00</td>
</tr>
<tr>
<td>2a</td>
<td>
[15:14] Reserved[1:0]: reserved rst:00
[13] dac_resolution: Set the VDAC resolution to either 5mV (0) or 6.25mV (1). rst:0
[12:8] fine_cst_adj[4:0]: Adjust for the current sense timing signal. Q ~ 2.6ns rst:00000
[7:4] Reserved[3:0]: Always set to 0
[3] bcc_freq: Boot capacitance charging frequency during tristate. 0 = 11.7 KHz, 1 = 23.4 KHz rst:0
[2:0] bcc_width[2:0]: Duration of Sync FET conduction time during boot capacitance charging. Q = 20.8 ns rst:000
</td>
<td>0000</td>
</tr>
</table>

Read Only Registers

read_only_registers	
ADDR OFFSET	**CONTENTS**
50	**[15:8] fail_code_sticky[7:0]:** OT fault, IOUT_OC fault, VOUT_OV fault, VOUT_UV fault, VIN_UV fault, VCC_UV fault, *reserved*, VDRV_UV fault. These fault indications are cleared only by applicaton of the *clear_sticky_codes* register. **[7:0] fail_code_nonstick[7:0]:** OT fault, IOUT_OC fault, VOUT_OV fault, VOUT_UV fault, VIN_UV fault, VCC_UV fault, *reserved*, VDRV_UV fault. These fault indications can be cleared by: • writing a 1 to the *clear_sticky_codes* register • re-enabling the VR output using the OPERATION command and/or the EN pin • non-sticky faults are also cleared when the output restarts after a fault (e.g. OC in hiccup mode) • restarting the VR output, via either the EN pin and/or the OPERATION command, or when the VR auto-restarts following a fault (e.g. OC in hiccup mode)
52	**[15:8] pulse_delay[7:0]:** delay in 96 MHz clock cycles from sync clock. **[7:0] iout_startup_ref_code[7:0]:** The misc_adc code that corresponds to 0A output current.
54	**[15:9] Reserved** **[8:0] vid_decode[8:0]:** The 9-bit target VID DAC code. It is either calculated or taken from the *vid_direct_value* register.
56	**[15] Reserved** **[14] vin_low:** this bit will be high when VIN is below the VIN_OFF threshold. **[13] vin_high:** this bit will be high when a VIN_OV_FAULT condition exists. **[12] c_comp_out:** The ouptut of the common OV/UV analog comparator. **[11:8] sst_curr_state[3:0]:** Soft start FSM state. {Lached off due to fault=>0, ready to start=>1, Reserved=>2, Reserved=>3, Ramp=>4, Regulating=>5, Reserved=>6, OV FAULT OFF=>7, OC HICCUP=>8,} **[7] Reserved** **[6:4] vout_uv_fault_thresh[2:0]:** VOUT under-voltage fault threshold. Range [50 - 400mV], resolution 50mV. **[3] Reserved** **[2:0] vout_ov_fault_thresh[2:0]:** VOUT over-voltage fault threshold. Range [50 - 400mV], resolution 50mV.

Read Write Registers

read_write_registers		
ADDR OFFSET	**CONTENTS**	**RST**
70	**[15:1] Reserved** **[0] clear_sticky_codes:** Writing a 1 to this register clears the *fail_code_sticky* and *fail_code_nonstick* registers. This bit is self-clearing. rst:0	0000
72	**[15:12] Reserved** **[11] vout_uv_by_adc:** 1=Vout undervoltage caused by ADC saturation, 0=Vout undervoltage through comparator. rst:0 **[10] cs_aaf_en_loop1:** Anti-alias filter enable for total current on Loop x. rst:1 **[9] vid_direct_en:** Use register *vid_direct_value* as the target VID DAC code. rst:0 **[8:0] vid_direct_value[8:0]:** This register specifies the target VID DAC code when *vid_direct_en* is asserted. rst:010101101	04AD

Loop LDO Reg Map Section

Loop LDO base address: 0x1400
NOTE:

- ✓ The registers presented in pages 20 through 21 apply to the LDO output only.
- ✓ The "ADDR OFFSET" in the table below (shown in hex code) represents the offset that needs to be added to the base address of the particular loop to access the registers associated with that loop.

OTP Trim Registers

otp_trim_registers		
ADDR OFFSET	**CONTENTS**	**RST**
0	*For Infineon Production Use Only*	40C0
2		8080
4		0000

OTP USR Registers

otp_usr_registers		
ADDR OFFSET	**CONTENTS**	**RST**
20	**[15] ldo_aaf_en:** enable or bypass anti-aliasing filter rst:0 **[14:13] ldo_polezero_config[1:0]:** Configuration bits for advanced user optimization of transient response. rst:00 **[12] ldo_ireport_disable:** Bit to disable current reporting function (power savings for applications that do not utilize LDO current reporting) rst:0 **[11] ldo_foldback_option:** Bit to enable overcurrent foldback functionality rst:0 **[10] ldo_boost_disable:** Disable the boost. rst:0 **[9] ldo_disable:** Bit to disable the LDO and its associated control logic if it is not utilized. It should not be used to turn the LDO output on and off. rst:0 **[8] ldo_track_config:** Configuration bit for tracking (1) or non-tracking (0) applications. rst:0 **[7:0] ldo_target_vout[7:0]:** Specifies the output target voltage in source-only mode. The actual voltage is set by external components. This register is not used in tracking mode. [u2.6] rst:00000000	0000

Read Only Registers

read_only_registers	
ADDR OFFSET	**CONTENTS**
50	**[15:8] ldo_fail_code_sticky[7:0]:** {OT fault, 1'b0, VOUT_OV fault, VOUT_UV fault, VIN_UV fault, VCC_UV fault, 1'b0, 1'b0}. These fault indications are cleared only by applicaton of the *ldo_clear_sticky_codes* register. **[7:0] ldo_fail_code_nonstick[7:0]:** {OT fault, 1'b0, VOUT_OV fault, VOUT_UV fault, VIN_UV fault, VCC_UV fault, 1'b0, 1'b0}. These fault indications can be cleared by: • re-enabling the VR output using the OPERATION command and/or the EN pin • asserting the *ldo_clear_sticky_codes* register
52	**[15:10] Reserved[5:0]:** Reserved space, not to be used, because it's reserved. **[9:0] vout_ov_fault_thr[9:0]:** the calculated VOUT over-voltage fault threshold.

Read Write Registers

read_write_registers		
ADDR OFFSET	**CONTENTS**	**RST**
70	**Reserved[15:0]:** rst:0000000000000000	0000
72	**Reserved[14:0]:** rst:000000000000000 **ldo_clear_sticky_codes:** Writing a 1 to this register clears the *ldo_fail_code_sticky* and *ldo_fail_code_nonstick* registers. This bit is self-clearing. rst:0	0000

PMBUS Reg Map Section

Page 0 (loop A) base address - 0x0600
Page 1 (loop B) base address - 0x0A00
Page 2 (loop C) base address - 0x0E00
Page 3 (loop D) base address - 0x1200
Page 4 (loop LDO) base address - 0x1600

NOTE:

- The registers presented in pages 22 through 38 apply to all outputs.
- The “ADDR OFFSET” in the table below (shown in 3-bit hex code) represents the offset that needs to be added to the base address of the particular loop to access the registers associated with that loop.

Legend	
normal	The command is supported and its value is stored in a register at the specified offset. To address a register, add the "ADDR Offset" (first column) to the base address for the loop (See above)
rsv/unsup	The command is either not supported, or is a reserved PMBus command
no_reg	The command is supported, but has no register storage. If you read the value at the corresponding address (via the I2C bus, or the MFR_REG_ACCESS command), the data is undefined.

CMD	Addr Offset	Bits	Contents	Reset Value
00	0x000		**page:** there is no REGMAP storage for this command.	
01	0x002	15:8	reserved	
		7:0	**operation:** Used to control the Rocky's operational state. The following values are supported: SW: 0x00, 0x40, 0x80, 0x94, 0x98, 0xA4, 0xA8 LDO: 0x00, 0x80 *Note: some bits in this command are don't-care. The corresponding values are accepted but not enumerated here.*	0x0
02	0x004	15:8	reserved	
		7:0	**on_off_config:** Determines how the output is enabled and disabled (pin, command, both, neither). The following values are supported: SW: all values LDO: 0x17, 0x1B, 0x1F	0x17
03	0x006		**clear_faults:** The CLEAR_FAULTS command is write-only. It clears	

			SALERT and all STATUS registers in the current PAGE. There is no register storage for this command.	
04	0x008		phase: command not supported.	
05	0x00a		Reserved PMBus command.	
06	0x00c		**page_plus_read:** Read a command on the specified PMBus Page. The Page will revert to its previous value unless the *regmap_common.pmb_page_plus_latch_new_page* is asserted.	
07	0x00e		Reserved PMBus command.	
08	0x010		Reserved PMBus command.	
09	0x012		Reserved PMBus command.	
0a	0x014		Reserved PMBus command.	
0b	0x016		Reserved PMBus command.	
0c	0x018		Reserved PMBus command.	
0d	0x01a		Reserved PMBus command.	
0e	0x01c		Reserved PMBus command.	
0f	0x01e		Reserved PMBus command.	
10	0x020	15:8	reserved	
		7:0	**write_protect:** Set the PMBus Write Protection mode. Each PAGE has its own protection mode. The following values are supported: 0x00, 0x20, 0x40, 0x80. Note that this PMBus command is not related to the protection mechanism defined in *regmap_common*.	0x0
11	0x022		**store_default_all:** command not supported.	
12	0x024		**restore_default_all:** Write-only command that entices Rocky to restore the contents of the most recent USER image from NVM into the registers. The data for this command is ignored. All USER registers (common, four switchers and the LDO) are restored, regardless of the current PMBus PAGE. Note that the function of this command is identical to RESTORE_USER_ALL. The restore operation takes approximately 40 usec.	
13	0x026		**store_default_code:** command not supported.	
14	0x028		**restore_default_code:** command not supported.	
15	0x02a		**store_user_all:** Write-only command that incites Rocky to program the contents of the NVM-backed USER registers into the NVM array. The data for this command is ignored. All USER registers (common, four switchers and the LDO) are stored, irrespective of the current PMBus PAGE.	

			The duration of the program operation varies based on the number of 1 bits in the registsers (approx. 51 usec per 1 bit). When the programming is complete, *nvm_command[15]* will be set to 1 by the hardware.	
16	0x02c		**restore_user_all:** Write-only command that compels Rocky to restore the contents of the most recent USER image from NVM into the registers. The data for this command is ignored. Note that the function of this command is identical to RESTORE_DEFAULT_ALL. The restore operation takes approximately 50 usec.	
17	0x02e		**store_user_code:** command not supported.	
18	0x030		**restore_user_code:** command not supported.	
19	0x032		**capability:** There is no register storage for this read-only command. The value is provided by the PMBus interface logic.	
1a	0x034		**query:** command not supported.	
1b	0x036		**smbalert_mask:** Provides indirect access to the STATUS_MASK registers. There is no register storage for this command. The status masks are stored in the MSB of the status registers.	
1c	0x038		Reserved PMBus command.	
1d	0x03a		Reserved PMBus command.	
1e	0x03c		Reserved PMBus command.	
1f	0x03e		Reserved PMBus command.	
20	0x040	15:8	reserved	
		7:0	**vout_mode:** The exponent of the VOUT-related commands (e.g. VOUT_COMMAND, VOUT_OV_FAULT_LIMIT, etc.). The following exponents are supported: -8, -9 and -12.	0x18
21	0x042	15:0	**vout_command:** Sets the output voltage in volts (not VID codes). To induce VBOOT-like behavior, the user must configure several PMBus registers properly. Example: 1. Set ON_OFF_CONFIG to 0x17 (or 0x16) so that the output will turn on when the ENABLE pin is asserted 2. Set VOUT_MODE to your desired resolution (e.g. 0x18 for 1/256V resolution) 3. Set VOUT_MAX > VOUT_COMMAND 4. Set VOUT_COMMAND to your desired output voltage Resolution is specified by VOUT_MODE.	0x0
22	0x044	15:0	**vout_trim:** A 2s complement number that is applied to VOUT_COMMAND, VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW. Resolution is specified by VOUT_MODE.	0x0
23	0x046		**vout_cal_offset:** command not supported.	

24	0x048	15:0	**vout_max:** Sets an upper limit on the commanded output voltage. Setting the output voltage to a value higher than the value in this command will cause a VOUT_MAX Warning. Resolution is specified by VOUT_MODE.	0x8000
25	0x04a	15:0	**vout_margin_high:** Specifies the target output voltage when the OPERATION command is set to *margin_high*. Resolution is specified by VOUT_MODE.	0x0
26	0x04c	15:0	**vout_margin_low:** Specifies the target output voltage when the OPERATION command is set to *margin_low*. Resolution is specified by VOUT_MODE.	0x0
27	0x04e	15:0	**vout_transition_rate:** Specifies the output slew rate during regulation. It does not apply to the initial voltage ramp from 0V (turning on, controlled by *TON_RISE*) or the ramp to 0V (turning off, controlled by *TOFF_FALL*). Switcher; 0.125mV/usec to 127mV/usec; 0.125mV/uS resolution	0xE808
28	0x050		**vout_droop:** command not supported.	
29	0x052	15:0	**vout_scale_loop:** Rocky supports 1:1 (0xE808) and 1:2 (0xE804) external resistor-divider ratios.	0xE808
2a	0x054		**vout_scale_monitor:** command not supported.	
2b	0x056		Reserved PMBus command.	
2c	0x058		Reserved PMBus command.	
2d	0x05a		Reserved PMBus command.	
2e	0x05c		Reserved PMBus command.	
2f	0x05e		Reserved PMBus command.	
30	0x060		**coefficients:** command not supported.	
31	0x062		**pout_max:** command not supported.	
32	0x064		**max_duty:** command not supported.	
33	0x066	15:0	**frequency_switch:** Sets the PWM's switching frequency. For synchronization, the values of *frequency_switch* for each loop are restricted as such: the FREQUENCY_SWITCH setting for SW_C (hereafter *SW_C_fs*) dominates. SW_C_fs has a range of 200 to 2000 KHz, 1K and 2K resolution. • SW_B_fs and SW_D_fs = SW_C_fs • SW_A_fs = SW_C_fs if FREQUENCY_SWITCH command to A is ≥ FREQUENCY_SWITCH for C • SW_A_fs = ½*SW_C_fs if FREQUENCY_SWITCH command to A is < FREQUENCY_SWITCH for C • SW_A_fs = SW_C_fs if FREQUENCY_SWITCH < 400KHz	0x0320
34	0x068		Reserved PMBus command.	

<table>
<tr><td>35</td><td>0x06a</td><td>15:0</td><td>vin_on: Sets the VIN voltage above which the output will be allowed to operate.
Switcher: 0-16V, 0.25V resolution
LDO: 0-7.96V, 31.25mV resolution</td><td>0xF001</td></tr>
<tr><td>36</td><td>0x06c</td><td>15:0</td><td>vin_off: Sets the VIN voltage below which the output will refuse to operate. STATUS_INPUT[3] will be set if VIN falls below this value.
Switcher: 0-16V, 0.25V resolution
LDO: 0-7.96V, 31.25mV resolution</td><td>0xF000</td></tr>
<tr><td>37</td><td>0x06e</td><td></td><td>interleave: command not supported.</td><td></td></tr>
<tr><td>38</td><td>0x070</td><td></td><td>iout_cal_gain: command not supported.</td><td></td></tr>
<tr><td>39</td><td>0x072</td><td>15:0</td><td>iout_cal_offset: Set the current sense offset.
Internal driver: -16A to 15.98A; 0.0156A resolution.
External driver: -128A to 127.8A; 0.125A resolution
LDO: -1A to 0.999A; 0.976mA resolution</td><td>0xD000</td></tr>
<tr><td>3a</td><td>0x074</td><td></td><td>fan_config_1_2: command not supported.</td><td></td></tr>
<tr><td>3b</td><td>0x076</td><td></td><td>fan_command_1: command not supported.</td><td></td></tr>
<tr><td>3c</td><td>0x078</td><td></td><td>fan_command_2: command not supported.</td><td></td></tr>
<tr><td>3d</td><td>0x07a</td><td></td><td>fan_config_3_4: command not supported.</td><td></td></tr>
<tr><td>3e</td><td>0x07c</td><td></td><td>fan_command_3: command not supported.</td><td></td></tr>
<tr><td>3f</td><td>0x07e</td><td></td><td>fan_command_4: command not supported.</td><td></td></tr>
<tr><td>40</td><td>0x080</td><td>15:0</td><td>vout_ov_fault_limit: For the switchers, VOUT over-voltage detection in the AFE is relative to VOUT. The AFE uses a 3-bit threshold with a range of 50mV to 400mV with 50mV resolution. The threshold is calculated by taking the difference between the target VOUT and the value specified in this command (note that the target VOUT is set by the combination of VOUT_MODE, VOUT_COMMAND, VOUT_TRIM, et al.).
<table>
<tr><th>(ov_fault_limit - target_vout)</th><th>threshold</th><th>AFE setting</th></tr>
<tr><td><= 50 mV</td><td>50 mV</td><td>0x0</td></tr>
<tr><td>50 mV <= 100 mV</td><td>100 mV</td><td>0x1</td></tr>
<tr><td>100 mV <= 150 mV</td><td>150 mV</td><td>0x2</td></tr>
<tr><td>150 mV <= 200 mV</td><td>200 mV</td><td>0x3</td></tr>
<tr><td>200 mV <= 250 mV</td><td>250 mV</td><td>0x4</td></tr>
<tr><td>250 mV <= 300 mV</td><td>300 mV</td><td>0x5</td></tr>
<tr><td>300 mV <= 350 mV</td><td>350 mV</td><td>0x6</td></tr>
<tr><td>> 350 mV</td><td>400 mV</td><td>0x7</td></tr>
</table>
The AFE setting is available in the read-only register regmap_loop.vout_ov_fault_thresh[2:0].
LDO; read only, 125% of ldo_target_vout
Resolution is specified by VOUT_MODE.</td><td>0x8000</td></tr>
<tr><td>41</td><td>0x082</td><td>15:8</td><td>reserved</td><td></td></tr>
</table>

<table>
<tr><td></td><td></td><td>7:0</td><td>vout_ov_fault_response: SW and LDO both support 0x00 (ignore) and 0x80 (shutdown) responses.</td><td>0x00</td></tr>
<tr><td>42</td><td>0x084</td><td>15:0</td><td>vout_ov_warn_limit: SWs, Resolution is specified by VOUT_MODE.
For the LDO, the VOUT_OV Warning threshold is RO, set to 12.5% over the target VOUT. Resolution is specified by VOUT_MODE.</td><td>0x8000</td></tr>
<tr><td>43</td><td>0x086</td><td>15:0</td><td>vout_uv_warn_limit: SWs, Resolution is specified by VOUT_MODE.
For the LDO, the VOUT_OV Warning threshold is RO, set to 12.5% under the target VOUT. Resolution is specified by VOUT_MODE.</td><td>0x0</td></tr>
<tr><td>44</td><td>0x088</td><td>15:0</td><td>vout_uv_fault_limit: Similar to VOUT_OV_FAULT_LIMIT.
Switchers; the 3-bit threshold value is available as a read-only register in regmap_loop.vout_uv_fault_thresh[2:0].
LDO; read only, 75% of ldo_target_vout
Resolution is specified by VOUT_MODE.</td><td>0x0</td></tr>
<tr><td rowspan="2">45</td><td rowspan="2">0x08a</td><td>15:8</td><td>reserved</td><td></td></tr>
<tr><td>7:0</td><td>vout_uv_fault_response: Specify Rocky's behavior in response to a VOUT_UV fault.
The following responses are supported: 0x00 (ignore) and 0x80 (shutdown).</td><td>0x00</td></tr>
<tr><td>46</td><td>0x08c</td><td>15:0</td><td>iout_oc_fault_limit: This field sets the threshold for the Analog OCP comparator as shown below. The values are shown for both 2A and 4A power stages. This command is read-only for the LDO.
A and B Internal driver: 0A to 4A; 31.25mA resolution.
C and D Internal driver: 0A to 8A; 31.25mA resolution.
C PLUS D Internal driver: 0A to 16A; 31.25mA resolution.
External driver: 0A to 255.75A; 0.25A resolution
LDO: read only 0.72A
<table>
<tr><th colspan="4">OC current limit conversion for internal drivers</th></tr>
<tr><th colspan="2">2A drivers</th><th colspan="2">4A drivers</th></tr>
<tr><th>current limit</th><th>code</th><th>current limit</th><th>code</th></tr>
<tr><td>0.00 - 0.25A</td><td>0x0</td><td>0.00 - 0.5A</td><td>0x0</td></tr>
<tr><td>0.28 - 0.50A</td><td>0x1</td><td>0.53 - 1.0A</td><td>0x1</td></tr>
<tr><td>0.53 - 0.75A</td><td>0x2</td><td>1.03 - 1.5A</td><td>0x2</td></tr>
<tr><td>0.78 - 1.00A</td><td>0x3</td><td>1.53 - 2.0A</td><td>0x3</td></tr>
<tr><td>1.03 - 1.25A</td><td>0x4</td><td>2.03 - 2.5A</td><td>0x4</td></tr>
<tr><td>1.28 - 1.50A</td><td>0x5</td><td>2.53 - 3.0A</td><td>0x5</td></tr>
<tr><td>1.53 - 1.75A</td><td>0x6</td><td>3.03 - 3.5A</td><td>0x6</td></tr>
<tr><td>1.78 - 2.00A</td><td>0x7</td><td>3.53 - 4.0A</td><td>0x7</td></tr>
<tr><td>2.03 - 2.25A</td><td>0x8</td><td>4.03 - 4.5A</td><td>0x8</td></tr>
<tr><td>2.28 - 2.50A</td><td>0x9</td><td>4.53 - 5.0A</td><td>0x9</td></tr>
<tr><td>2.53 - 2.75A</td><td>0xA</td><td>5.03 - 5.5A</td><td>0xA</td></tr>
<tr><td>2.78 - 3.00A</td><td>0xB</td><td>5.53 - 6.0A</td><td>0xB</td></tr>
<tr><td>3.03 - 3.25A</td><td>0xC</td><td>6.03 - 6.5A</td><td>0xC</td></tr>
<tr><td>3.28 - 3.50A</td><td>0xD</td><td>6.53 - 7.0A</td><td>0xD</td></tr>
<tr><td>3.53 - 3.75A</td><td>0xE</td><td>7.03 - 7.5A</td><td>0xE</td></tr>
</table></td><td>0xD900</td></tr>
</table>

			3.78 - 4.00A | 0xF | 7.53 - 8.0A | 0xF
47	0x08e	15:8	reserved
		7:0	**iout_oc_fault_response:** Specifies Rocky's behavior in response to a IOUT over-current fault. The following responses are supported: 0xC0 (shutdown, no retry), 0xF0 (retry 6 times then latch off), and 0xF8 (retry indefinitely).
48	0x090		**iout_oc_lv_fault_limit:** command not supported.
49	0x092		**iout_oc_lv_fault_response:** command not supported.
4a	0x094	15:0	**iout_oc_warn_limit:** Sets the threshold for the detection of over current warnings. *A and B Internal driver: 0A to 4A; 31.25mA resolution.* *C and D Internal driver: 0A to 8A; 31.25mA resolution.* *C PLUS D Internal driver: 0A to 16A; 31.25mA resolution.* *External driver: 0A to 255.75A; 0.25A resolution* *LDO: read only 0.72A*
4b	0x096		**iout_uc_fault_limit:** command not supported.
4c	0x098		**iout_uc_fault_response:** command not supported.
4d	0x09a		Reserved PMBus command.
4e	0x09c		Reserved PMBus command.
4f	0x09e	15:0	**ot_fault_limit:** Sets the over-temperature fault threshold *0C to 255C, 1C Resolution*
50	0x0a0	15:8	reserved
		7:0	**ot_fault_response:** Specifies Rocky's behavior in response to an over-temperature fault. The following responses are supported: 0x00 (ignore), 0x80 (shutdown) and 0xC0 (shutdown, restart when fault condition is removed).
51	0x0a2	15:0	**ot_warn_limit:** Sets the over-temperature warning threshold, *0C to 255C, 1C Resolution*
52	0x0a4		**ut_warn_limit:** command not supported.
53	0x0a6		**ut_fault_limit:** command not supported.
54	0x0a8		**ut_fault_response:** command not supported.
55	0x0aa	15:0	**vin_ov_fault_limit:** Sets the VIN over-voltage fault threshold. *Switcher: 0-63.9V, 6.25mV resolution* *LDO: 0-7.99V, 7.8125mV resolution*
56	0x0ac	15:8	reserved

		7:0	**vin_ov_fault_response:** Specifies Rocky's behavior in response to a VIN over-voltage fault. The following responses are supported: 0x00 (ignore) and 0x80 (shutdown).	0x00
57	0x0ae		**vin_ov_warn_limit:** command not supported.	
58	0x0b0	15:0	**vin_uv_warn_limit:** Sets the VIN under-voltage warning threshold. *Switcher: 0-63.9V, 6.25mV resolution* *LDO: 0-7.99V, 7.8125mV resolution*	0xE000
59	0x0b2		**vin_uv_fault_limit:** command not supported.	
5a	0x0b4		**vin_uv_fault_response:** command not supported.	
5b	0x0b6		**iin_oc_fault_limit:** command not supported.	
5c	0x0b8		**iin_oc_fault_response:** command not supported.	
5d	0x0ba		**iin_oc_warn_limit:** command not supported.	
5e	0x0bc	15:0	**power_good_on:** Sets the output voltage above which the PowerGood indication is asserted. Resolution is specified by VOUT_MODE.	0x0
5f	0x0be	15:0	**power_good_off:** Sets the output voltage below which the PowerGood indication is deasserted. Resolution is specified by VOUT_MODE.	0x0
60	0x0c0	15:0	**ton_delay:** Specifies the time (in milliseconds) from when the output is enabled until the voltage starts to ramp. *0-63.5msec, 0.5msec resolution*	0xF800
61	0x0c2	15:0	**ton_rise:** Specifies the time (in milliseconds) from when the output is enabled until it reaches the target voltage. This value is only used for the initial ramp. *VOUT_TRANSITION_RATE* controls the slew rate during regulation. *0.25msec to 31.75msec, 0.25msec resolution*	0xF004
62	0x0c4	15:0	**ton_max_fault_limit:** The TON_MAX_FAULT_LIMIT command sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. If a UV fault is detected at the end of this time, a TON_MAX_FAULT will be flagged. UV faults after this time will be flagged as a VOUT_UV_FAULT. The time interval specified here starts after TON_DELAY expires. *0msec to 31.75msec, 0.25msec resolution*	0xF004
63	0x0c6	15:8	reserved	
		7:0	**ton_max_fault_response:** Set the response type in the event of a TON_MAX Fault. The following responses are supported: 0x00 (ignore) and 0x80 (shutdown).	0x00

64	0x0c8	15:0	**toff_delay:** Specifies the time (in milliseconds) from when the output is disabled until the voltage begins to ramp to 0V. *0-63.5msec, 0.5msec resolution*	0xF800
65	0x0ca	15:0	**toff_fall:** Specifies the time (in milliseconds) from when the output is disabled to when the voltage completes the ramp to 0V. This value is only used when turning the output off. *VOUT_TRANSITION_RATE* controls the slew rate during regulation. *0.25msec to 31.75msec, 0.25msec resolution*	0xF004
66	0x0cc		**toff_max_warn_limit:** command not supported.	
67	0x0ce		Reserved PMBus command.	
68	0x0d0		**pout_op_fault_limit:** command not supported.	
69	0x0d2		**pout_op_fault_response:** command not supported.	
6a	0x0d4		**pout_op_warn_limit:** command not supported.	
6b	0x0d6		**pin_op_warn_limit:** command not supported.	
6c	0x0d8		Reserved PMBus command.	
6d	0x0da		Reserved PMBus command.	
6e	0x0dc		Reserved PMBus command.	
6f	0x0de		Reserved PMBus command.	
70	0x0e0		Reserved PMBus command.	
71	0x0e2		Reserved PMBus command.	
72	0x0e4		Reserved PMBus command.	
73	0x0e6		Reserved PMBus command.	
74	0x0e8		Reserved PMBus command.	
75	0x0ea		Reserved PMBus command.	
76	0x0ec		Reserved PMBus command.	
77	0x0ee		Reserved PMBus command.	
78	0x0f0		**status_byte:** The 8 LSBs of STATUS_WORD. There is no REGMAP storage for this command.	
79	0x0f2	15:0	**status_word:** 16-bit STATUS summary. **bit** / **STATUS_WORD** 7 VOUT 6 IOUT 5 INPUT 4 MFR_SPECIFIC 3 POWER_GOOD#	0x0

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>2</td><td>unused</td></tr>
<tr><td>1</td><td>unused</td></tr>
<tr><td>0</td><td>unused</td></tr>
<tr><th>bit</th><th>STATUS_BYTE</th></tr>
<tr><td>7</td><td>unused</td></tr>
<tr><td>6</td><td>OFF</td></tr>
<tr><td>5</td><td>VOUT_OV_FAULT</td></tr>
<tr><td>4</td><td>IOUT_OC_FAULT</td></tr>
<tr><td>3</td><td>VIN_UV_FAULT</td></tr>
<tr><td>2</td><td>TEMPERATURE</td></tr>
<tr><td>1</td><td>CML</td></tr>
<tr><td>0</td><td>NONE_OF_THE_ABOVE</td></tr>
</table>
</td><td></td></tr>
<tr><td rowspan="2">7a</td><td rowspan="2">0x0f4</td><td>15:8</td><td>status_vout_mask: Status MASK bits. Typically accessed indirectly via the SMBALERT_MASK command.</td><td>0x0</td></tr>
<tr><td>7:0</td><td>status_vout: Fault and warning information related to VOUT.
<table>
<tr><th>bit</th><th>Status</th></tr>
<tr><td>7</td><td>VOUT_OV_FAULT</td></tr>
<tr><td>6</td><td>VOUT_OV_WARNING</td></tr>
<tr><td>5</td><td>VOUT_UV_WARNING</td></tr>
<tr><td>4</td><td>VOUT_UV_FAULT</td></tr>
<tr><td>3</td><td>VOUT_MAX_Warning</td></tr>
<tr><td>2</td><td>TON_MAX_FAULT</td></tr>
<tr><td>1</td><td>unused</td></tr>
<tr><td>0</td><td>unused</td></tr>
</table>
</td><td>0x0</td></tr>
<tr><td rowspan="2">7b</td><td rowspan="2">0x0f6</td><td>15:8</td><td>status_iout_mask: Status MASK bits. Typically accessed indirectly via the SMBALERT_MASK command.</td><td>0x0</td></tr>
<tr><td>7:0</td><td>status_iout: Fault and warning information related to IOUT.
<table>
<tr><th>bit</th><th>Status</th></tr>
<tr><td>7</td><td>IOUT_OC_FAULT</td></tr>
<tr><td>6</td><td>unused</td></tr>
<tr><td>5</td><td>IOUT_OC_WARNING</td></tr>
<tr><td>4</td><td>unused</td></tr>
<tr><td>3</td><td>unused</td></tr>
<tr><td>2</td><td>unused</td></tr>
<tr><td>1</td><td>unused</td></tr>
<tr><td>0</td><td>unused</td></tr>
</table>
</td><td>0x0</td></tr>
<tr><td rowspan="2">7c</td><td rowspan="2">0x0f8</td><td>15:8</td><td>status_input_mask: Status MASK bits. Typically accessed indirectly via the SMBALERT_MASK command.</td><td>0x0</td></tr>
<tr><td>7:0</td><td>status_input: Fault and warning information related to VIN.
<table>
<tr><th>bit</th><th>Status</th></tr>
</table>
</td><td>0x0</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td><table>
<tr><td>7</td><td>VIN_OV_FAULT</td></tr>
<tr><td>6</td><td>unused</td></tr>
<tr><td>5</td><td>VIN_UV_WARNING</td></tr>
<tr><td>4</td><td>unused</td></tr>
<tr><td>3</td><td>Off due to VIN_UV</td></tr>
<tr><td>2</td><td>unused</td></tr>
<tr><td>1</td><td>IIN_OC_WARNING</td></tr>
<tr><td>0</td><td>unused</td></tr>
</table></td><td></td></tr>
<tr><td rowspan="2">7d</td><td rowspan="2">0x0fa</td><td>15:8</td><td>status_temperature_mask: Status MASK bits. Typically accessed indirectly via the SMBALERT_MASK command.</td><td>0x0</td></tr>
<tr><td>7:0</td><td>status_temperature: Fault and warning information related to Temperature.<table>
<tr><th>bit</th><th>Status</th></tr>
<tr><td>7</td><td>OT_FAULT</td></tr>
<tr><td>6</td><td>OT_WARNING</td></tr>
<tr><td>5:0</td><td>unused</td></tr>
</table></td><td>0x0</td></tr>
<tr><td rowspan="2">7e</td><td rowspan="2">0x0fc</td><td>15:8</td><td>status_cml_mask: Status MASK bits. Typically accessed indirectly via the SMBALERT_MASK command.</td><td>0x0</td></tr>
<tr><td>7:0</td><td>status_cml: Fault and warning information related to PMBus communications.<table>
<tr><th>bit</th><th>Status</th></tr>
<tr><td>7</td><td>Invalid/Unsupported command</td></tr>
<tr><td>6</td><td>Invalid/Unsupported data, or
send_too_many_bytes</td></tr>
<tr><td>5</td><td>PEC check failed</td></tr>
<tr><td>4</td><td>unused: processor fault</td></tr>
<tr><td>3</td><td>unused: memory fault</td></tr>
<tr><td>2</td><td>unused: reserved</td></tr>
<tr><td>1</td><td>send_too_few_bits OR
read_bit_set_in_addr OR
read_too_few_bits OR
read_too_many_bytes OR
command_too_short</td></tr>
<tr><td>0</td><td>unused: other memory/logic fault</td></tr>
</table></td><td>0x0</td></tr>
<tr><td>7f</td><td>0x0fe</td><td></td><td>status_other: command not supported.</td><td></td></tr>
<tr><td>80</td><td>0x100</td><td></td><td>status_mfr_specific: command not supported.</td><td></td></tr>
<tr><td>81</td><td>0x102</td><td></td><td>status_fans_1_2: command not supported.</td><td></td></tr>
<tr><td>82</td><td>0x104</td><td></td><td>status_fans_3_4: command not supported.</td><td></td></tr>
<tr><td>83</td><td>0x106</td><td></td><td>Reserved PMBus command.</td><td></td></tr>
</table>

84	0x108		Reserved PMBus command.	
85	0x10a		Reserved PMBus command.	
86	0x10c		**read_ein:** command not supported.	
87	0x10e		**read_eout:** command not supported.	
88	0x110	15:0	**read_vin:** Telemetry: input voltage. SW: 31.25mV resolution LDO: 7.8125mV resolution	0x0
89	0x112	15:0	**read_iin:** Telemetry: input current. *SW internal drivers: 7.8125mA resolution* *SW external drivers: 62.5mA resolution*	0x0
8a	0x114		**read_vcap:** command not supported.	
8b	0x116	15:0	**read_vout:** Telemetry: output voltage. Resolution is set by VOUT_MODE.	0x0
8c	0x118	15:0	**read_iout:** Telemetry: output current. The LDO will NAK this command if *regmap_ldo.ldo_ireport_disable* is set. *SW internal drivers: 15.6mA resolution* *SW external drivers: 125mA resolution* *LDO: 0.976mA resolution*	0x0
8d	0x11a	15:0	**read_temperature_1:** Telemetry: temperature. There are two temperature sensors on Rocky. Temp_0 is connected to SW A and SW B (PMBus pages 0 and 1). Temp_1 is connected to SW C, SW D and the LDO (PMBus pages 2, 3 and 4) *1degC resolution*	0x0
8e	0x11c		**read_temperature_2:** command not supported.	
8f	0x11e		**read_temperature_3:** command not supported.	
90	0x120		**read_fan_speed_1:** command not supported.	
91	0x122		**read_fan_speed_2:** command not supported.	
92	0x124		**read_fan_speed_3:** command not supported.	
93	0x126		**read_fan_speed_4:** command not supported.	
94	0x128		**read_duty_cycle:** command not supported.	
95	0x12a		**read_frequency:** command not supported.	
96	0x12c	15:0	**read_pout:** Telemetry: output power. *SW internal drivers: 31.25mW resolution* *SW external drivers: 250mW resolution* *LDO: 15.625mW resolution*	0x0
97	0x12e	15:0	**read_pin:** Telemetry: input power. *SW internal drivers: 31.25mW resolution*	0x0

			SW external drivers: 250mW resolution *LDO: 15.625mW resolution*	
98	0x130		**pmbus_revision:** there is no REGMAP storage for this command.	
99	0x132		**mfr_id:** there is no REGMAP storage for this command.	
9a	0x134		**mfr_model:** there is no REGMAP storage for this command.	
9b	0x136		**mfr_revision:** there is no REGMAP storage for this command.	
9c	0x138		**mfr_location:** command not supported.	
9d	0x13a		**mfr_date:** command not supported.	
9e	0x13c		**mfr_serial:** command not supported.	
9f	0x13e		**app_profile_support:** command not supported.	
a0	0x140		**mfr_vin_min:** command not supported.	
a1	0x142		**mfr_vin_max:** command not supported.	
a2	0x144		**mfr_iin_max:** command not supported.	
a3	0x146		**mfr_pin_max:** command not supported.	
a4	0x148		**mfr_vout_min:** command not supported.	
a5	0x14a		**mfr_vout_max:** command not supported.	
a6	0x14c		**mfr_iout_max:** command not supported.	
a7	0x14e		**mfr_pout_max:** command not supported.	
a8	0x150		**mfr_tambient_max:** command not supported.	
a9	0x152		**mfr_tambient_min:** command not supported.	
aa	0x154		**mfr_efficiency_ll:** command not supported.	
ab	0x156		**mfr_efficiency_hl:** command not supported.	
ac	0x158		**mfr_pin_accuracy:** command not supported.	
ad	0x15a		**ic_device_id:** there is no REGMAP storage for this command.	
ae	0x15c		**ic_device_rev:** there is no REGMAP storage for this command.	
af	0x15e		Reserved PMBus command.	
b0	0x160		**user_data_00:** command not supported.	
b1	0x162		**user_data_01:** command not supported.	
b2	0x164		**user_data_02:** command not supported.	
b3	0x166		**user_data_03:** command not supported.	

b4	0x168		**user_data_04:** command not supported.	
b5	0x16a		**user_data_05:** command not supported.	
b6	0x16c		**user_data_06:** command not supported.	
b7	0x16e		**user_data_07:** command not supported.	
b8	0x170	15:9	reserved	
		8:0	reserved	0
b9	0x172	15:9	reserved	
		8:0	reserved	0
ba	0x174	15:9	reserved	
		8:0	reserved	0
bb	0x176	15:9	reserved	
		8:0	reserved	0
bc	0x178	15:9	reserved	
		8:0	reserved	0
be	0x17c		**user_data_14:** command not supported.	
bf	0x17e		**user_data_15:** command not supported.	
c0	0x180		**mfr_max_temp_1:** command not supported.	
c1	0x182		**mfr_max_temp_2:** command not supported.	
c2	0x184		**mfr_max_temp_3:** command not supported.	
c3	0x186		Reserved PMBus command.	
c4	0x188		Reserved PMBus command.	
c5	0x18a		Reserved PMBus command.	
c6	0x18c		Reserved PMBus command.	
c7	0x18e		Reserved PMBus command.	
c8	0x190		Reserved PMBus command.	

c9	0x192		Reserved PMBus command.	
ca	0x194		Reserved PMBus command.	
cb	0x196		Reserved PMBus command.	
cc	0x198		Reserved PMBus command.	
cd	0x19a		Reserved PMBus command.	
ce	0x19c		Reserved PMBus command.	
cf	0x19e		Reserved PMBus command.	
d0	0x1a0		**mfr_reg_access:** This command provides read/write access to non-PMBus registers. This command uses the SMBus Process Call protocol for reads, and the Block Write protocol for writes, shown below. The first address byte contains the address offset for the target register. The second address byte contains the base address of the target REGMAP.	
d1	0x1a2		**mfr_specific_d1:** command not supported.	
d2	0x1a4		**mfr_specific_02:** command not supported.	
d3	0x1a6		**mfr_specific_03:** command not supported.	
d4	0x1a8		**mfr_specific_04:** command not supported.	
d5	0x1aa		**mfr_specific_05:** command not supported.	
d6	0x1ac		**mfr_i2c_address:** This command returns the value in *regmap_common.i2c_device_addr*.	
d7	0x1ae		**mfr_specific_07:** command not supported.	
d8	0x1b0	15:0	**mfr_tpgdly:** Specifies the delay from VOUT exceeding the Power Good threshold to the assertion of the Power Good signal. *0 to 15msec, 1msec resolution*	0x0
d9	0x1b2	15:8	reserved	
		7:0	**mfr_fccm:** 0x0 sets Adaptive On-Time; 0x1 sets Forced Continuous Conducton Mode.	0x1
da	0x1b4		**mfr_specific_10:** command not supported.	
db	0x1b6	15:0	**mfr_vout_peak:** The value in this register represents the maximum VOUT voltage since the previous read (or reset). Reading this register clears the value. Resolution is set by VOUT_MODE.	0x0
dc	0x1b8	15:0	**mfr_iout_peak:** The value read from this register represents the maximum IOUT current since the previous read (or reset). Reading this register clears the value. *SW internal drivers: 15.6mA resolution*	0xE800

			SW external drivers: 125mA resolution *LDO: 0.976mA resolution*	
dd	0x1ba	15:0	**mfr_temperature_peak:** The value in this register represents the maximum Temperature since the previous read (or reset). Reading this register clears the value. *1degC resolution*	0x0
de	0x1bc		**mfr_ldo_margin:** command not supported.	
df	0x1be		**mfr_specific_15:** command not supported.	
e0	0x1c0		**mfr_specific_16:** command not supported.	
e1	0x1c2		**mfr_specific_17:** command not supported.	
e2	0x1c4		**mfr_specific_18:** command not supported.	
e3	0x1c6		**mfr_specific_19:** command not supported.	
e4	0x1c8		**mfr_specific_20:** command not supported.	
e5	0x1ca		**mfr_specific_21:** command not supported.	
e6	0x1cc		**mfr_specific_22:** command not supported.	
e7	0x1ce		**mfr_specific_23:** command not supported.	
e8	0x1d0		**mfr_specific_24:** command not supported.	
e9	0x1d2		**mfr_specific_25:** command not supported.	
ea	0x1d4		**mfr_specific_26:** command not supported.	
eb	0x1d6		**mfr_specific_27:** command not supported.	
ec	0x1d8		**mfr_specific_28:** command not supported.	
ed	0x1da		**mfr_specific_29:** command not supported.	
ee	0x1dc		**mfr_specific_30:** command not supported.	
ef	0x1de		**mfr_specific_31:** command not supported.	
f0	0x1e0		**mfr_specific_32:** command not supported.	
f1	0x1e2		**mfr_specific_33:** command not supported.	
f2	0x1e4		**mfr_specific_34:** command not supported.	
f3	0x1e6		**mfr_specific_35:** command not supported.	
f4	0x1e8		**mfr_specific_36:** command not supported.	
f5	0x1ea		**mfr_specific_37:** command not supported.	
f6	0x1ec		**mfr_specific_38:** command not supported.	

f7	0x1ee		**mfr_specific_39:** command not supported.	
f8	0x1f0		**mfr_specific_40:** command not supported.	
f9	0x1f2		**mfr_specific_41:** command not supported.	
fa	0x1f4		**mfr_specific_42:** command not supported.	
fb	0x1f6		**mfr_specific_43:** command not supported.	
fc	0x1f8		**mfr_specific_44:** command not supported.	
fd	0x1fa		**mfr_specific_45:** command not supported.	
fe	0x1fc		**mfr_specific_command_ext:** command not supported.	
ff	0x1fe		**pmbus_command_ext:** command not supported.	

Formats for Reading/Writing

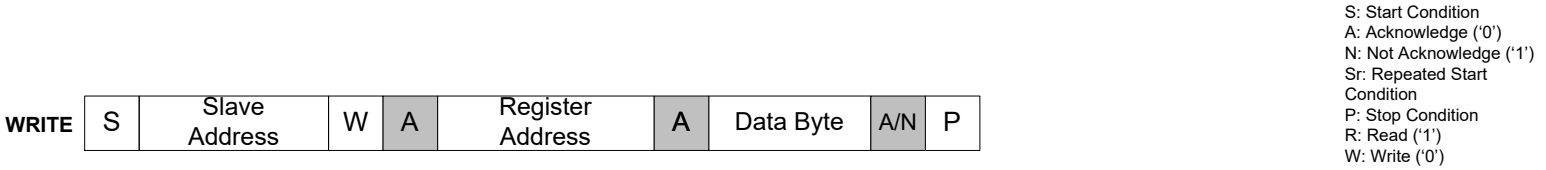

Figure 1: I2C Write

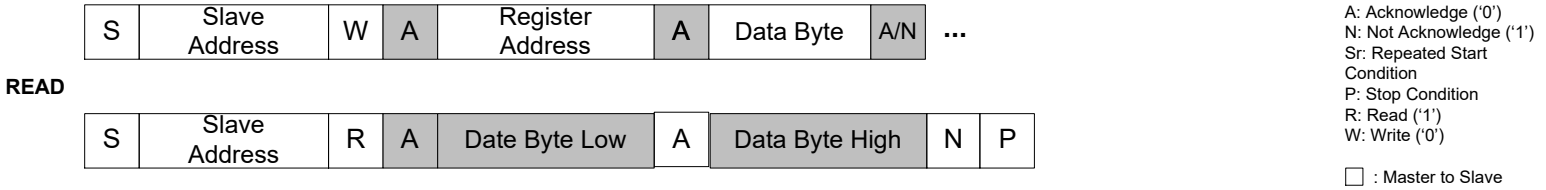

Figure 2: I2C Read

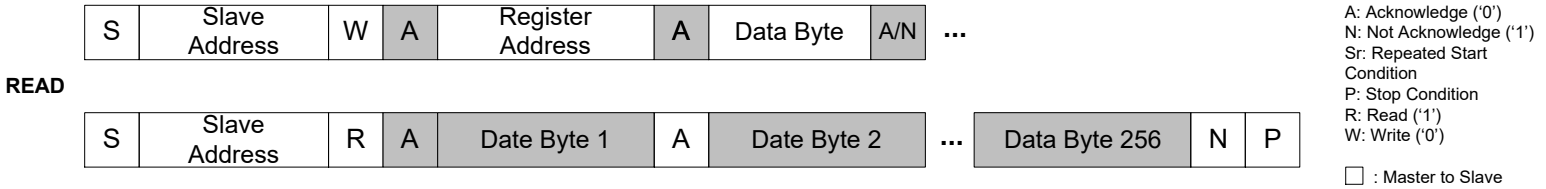

Figure 3: I2C 256 Byte Read

Note: Data1, data2, etc. are the data bytes read from the device, with data1 corresponding to the data returned from address 0x0000, data2 corresponding to the data returned from address 0x0001, etc.

Data and specifications subject to change without notice.

International
IOR Rectifier

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Revision History

Version	ECN#	Reason for Change	Date	Modified by:	Approved by:
1.0	N/A	Initial Release	30MAY2017	D. Caron	
1.1		Changed pin reference in description for register **cnfg_nvm_prog_max** from "ADDR" pin to "MTP" pin.	25OCT2018	J. Lee	
1.2		Update VOUT_OV_WARN, VOUT_UV_WARN	31JAN2019	D. Caron	
1.3		Remove LDO support from READ_IIN command (89h)	13SEPT2019	D. Caron	