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OptiMOS™ Source-Down

a new era in MOSFET performance

Introducing a new industry benchmark MOSFET footprint

The OptiMOS™ Source-Down Power MOSFET

By Bastian Lang, Product Marketing Manager at Infineon Technologies

When it comes to power management, the market is striving for higher energy efficiency, power density, ruggedness and improved lifetime for end applications. While advancements in silicon technologies are pushing the envelope of key performance parameters, new package concepts offering groundbreaking benefits are seldom. With the introduction of the new Source-Down technology and the release of a whole new product family, Infineon is leading the way towards defining a new industry standard footprint.

Drain-Down versus Source-Down

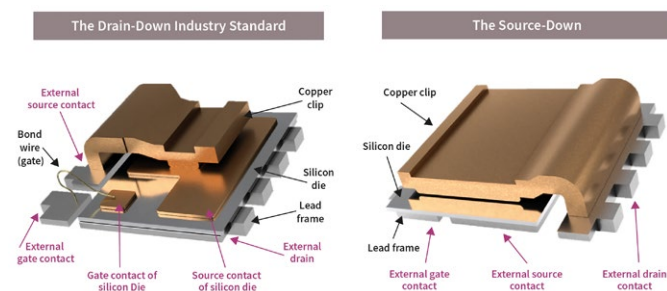


Figure 1: the internal construction of a PQFN 3.3x3.3 mm Drain-Down power MOSFET (left) and the internal construction of a PQFN 3.3x3.3 mm Source-Down power MOSFET (right)

Figure 1 (on the left) shows the structure of a modern vertical trench power MOSFET, giving an idea of the cross-section of a power MOSFET underneath a PQFN 3.3x3.3 mm package. The base of this architecture is a lead frame. This is serving as the carrier of the thin silicon die and the drain connection of the silicon on the bottom side. In a vertical trench MOSFET, the current is flowing vertically through the device, the top- and the bottom side of the device therefore serve as electrical connections. The active trenches of an n-channel power MOSFET are on the source side of the die which is typically located at the top. The source connection of the silicon die is established with a copper clip that is connecting the top area of the silicon die with a part of the lead frame. The gate connection is also located on the side of the active trenches and typically connected with the lead frame via a bond wire. With this construction, all three electrical connections can be brought onto the lead frame so that the MOSFET can be mounted on a PCB.

The Source-Down concept

This new approach is simple yet groundbreaking. We take the silicon die inside of the MOSFET package and flip it upside down. This way now the source potential is connected to the lead frame instead of the drain potential. Figure 1 (on the right) shows the structure of the new Source-Down technology. The

gate and source connection of the silicon die is directly established on the lead frame. The electrical connection of the drain (from the top of the die) can be achieved with a very large copper clip.

Figure 2 shows the difference in the footprints of the PQFN 3.3x3.3 mm OptiMOS™ MOSFET family. The electrical connection of drain, source and gate are still at the same location making a drop-in replacement very easy.

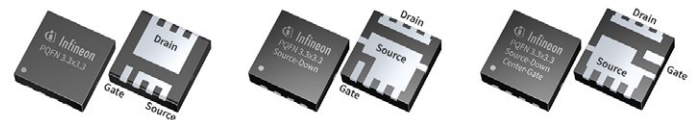


Figure 2: (a) A standard PQFN 3.3x3.3 mm, (b) the new Source-Down PQFN 3.3x3.3 mm and (c) the new Source-Down Center-Gate PQFN 3.3x3.3 mm package footprints

With the introduction of the new Source-Down concept, two new footprints are established. The Source-Down Standard-Gate (Figure 2b) and the Source-Down Center-Gate (Figure 2c).

Utilizing the Source-Down benefits

These new footprints come with several benefits such as:

- 1) Improved $R_{DS(on)}$
- 2) Reduced thermal resistance
- 3) New thermal management capabilities

$R_{DS(on)}$: Flipping the die upside down removes some construction limitations that apply to the standard drain-down devices. With the Source-Down approach, some of these constraints are loosened enabling the use of much bigger dies and hence reduction of $R_{DS(on)}$ by 30%. Lower $R_{DS(on)}$ is directly linked to the reduction of I^2R losses in the application and leads to greater power densities.

Thermal management: It is one of the strongest disciplines in power electronics design. Keeping your thermals under control directly translates to longer end-device lifetimes or the ability to increase power density. The Source-Down concept offers multiple benefits enabling cooler designs. A significant reduction in $R_{DS(on)}$ has an impact on thermals too: as it lowers losses in the device, consequently the device-temperature is decreased. The active trenches of a vertical power MOSFET are located on the source side of the silicon die. This is where most of the losses are generated during the operation and ultimately where the losses are converted to excess heat. In a traditional Drain-Down device, this heat needs to be transported through the silicon to the drain side which is connected to the lead frame and then to the PCB.

Flipping the die upside down puts these active trenches of the silicon die directly onto the copper lead frame. The heat that is generated in those trenches can, therefore, be conducted

directly into the PCB over the lead frame. This new construction setup leads to a reduction in R_{thJC} of 22 percent from 1,8 K/W down to 1,4 K/W.

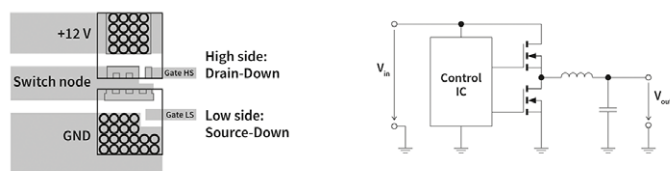


Figure 3: (a) the schematic of a synchronous buck converter implemented with a half-bridge MOSFET configuration and (b) example layout of a Drain-Down (in the high side) and a Source-Down (in the low side) in a half-bridge MOSFET configuration

The Source-Down concept has a number of advantages in a half- or full-bridge configuration designs. The copper area of the PCB that is connected to the thermal pad of the MOSFET is generally very helpful in distributing the losses generated in the MOSFET. Figure 3a shows the schematic of a widely used synchronous buck converter as an example. The drain potential of the high-side FET is connected to the input voltage. The source contact of the low-side FET is connected to the GND potential. The source potential of the high-side device is connected to the drain of the low-side MOSFET forming the switch node. By using the Drain-Down in the low-side of a half-bridge, the thermal pad would be connected to the switch node area. The switch node potential is a modulated waveform and therefore jumping between V_{in} and the GND potential. This area should be minimized to reduce the noise emitted into the system but this minimization would limit the thermal management capabilities of the low-side MOSFET. The Source-Down concept overcomes this challenge as the thermal pad of the low-side MOSFET is now on the ground potential. Since the ground area is generally kept large, it serves as a heatsink that can be utilized with the big thermal pad of the Source-Down device. Additionally, thermal vias can easily be used on the GND potential right under the device. Figure 3b depicts an example of a possible PCB layout. As can be seen, the two potentials that can be considered silent (or not jumping) are +12V and GND.

Based on the above, the three major benefits that make the new Source-Down concept a thermal management champion are:

- Significant reduction of $R_{DS(on)}$
- Decrease of R_{thJC} by 22%
- Optimal layout possibilities

Parallel operation

In applications like OR-ing and battery protection, large currents must be handled statically. For this, very low on-state-resistance is key to limit the losses in the system and keep the temperature at acceptable levels. To accomplish the lowest $R_{DS(on)}$, multiple MOSFETs are connected in parallel. The Center-Gate option offers a wider creepage distance between the drain and source contacts, which allows that the gates of multiple devices can be connected on one single PCB layer instead of being routed through vias and connected to other layers of the board.

Application benefits, real-life examples

Discussing a real-life example helps to explore where the new Source-Down concept really plays out its benefits. In the follow-

ing case, a buck converter was designed with the best-in-class devices currently available in the market. Figure 4 shows the configurations (a) with a PQFN 5x6 mm solution (b) using the currently available best-in-class PQFN 3.3x3.3 mm and finally (c) when applying the Source-Down solution.

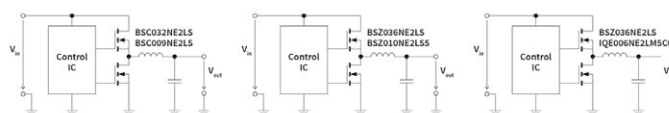


Figure 4 Configurations (a) with a PQFN 5x6 mm solution, (b) the currently available best-in-class PQFN 3.3x3.3 mm and (c) the Source-Down solution

Looking at the efficiency in the application in Figure 5, the Source-Down solution clearly outperforms the other two options. For instance, for the full load scenario, 1.5 percent improvement is achieved. This point is critical because of the thermal limitations. Enhancements in full load are directly tied to achieving higher power densities in the end application. In addition to the efficiency, the thermal performance of the device as a static switch was also analyzed. Thanks to the innovative Source-Down concept, much larger silicon dies can be housed in the PQFN 3.3x3.3 mm footprint enabling a significant improvement in $R_{DS(on)}$. This combined with a better R_{thJC} makes the Source-Down device stays significantly cooler than common-footprint components. A 10°C cooler design compared to the current available PQFN 3.3x3.3 mm solution could be achieved at 20 A constant current.

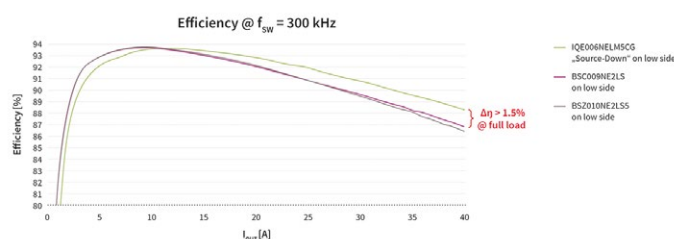


Figure 5 System efficiency for different MOSFET configurations (demonstrated in Figure 4)

The new industry benchmark

The Source-Down concept in Power MOSFETs is opening up some layout related constraints in power management. With the improvements of the electrical and thermal performance parameters of the device paired with the newly gained flexibility in system design, there are no more limitations for engineers to explore new concepts and bring their applications performance to unprecedented levels.

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