Power Semis - Selection Options Are Endless

By: Kevin Parmenter, FAE Director, Taiwan Semiconductor NA

When I first started in the power electronics industry in the seventies, device selection was limited. We were moving from silicon bipolar transistors and rudimentary rectifiers to MOSFETS and better rectifiers. Surface-mount technology and co-packaged ICs with power devices and/or drivers were unheard of and using WBG (wide bandgap) devices was a theoretical dream. I remember finding sample parts by flipping through databooks and calling distributors to see what they might have in stock locally and driving to pick them up or waiting for weeks for delivery. Today designers have a choice of more power devices than ever thought possible 20 or 30 years ago.

Now we have silicon MOSFETS. We have IGBTs, both silicon and small-signal semiconductors. They are still used for new designs daily and will be with us long after the old designs are no longer used. The co-packaging of devices was introduced, nobody imagined they could be improved upon. But here we are with thin SMA packages mainstreaming to lower the height/thickness of products. We also have packages, such as SOD128 and other alternatives, increasing power density. These newer devices not only produce less heat and have higher efficiency in applications, they also are able to remove that heat into the PCB much faster by using thermal heat spreaders incorporated into the packages, thus enabling end-applications to increase power density without increasing cost.

The co-packaging of devices was simply unheard of not too long ago. Now, not only do we have better power semiconductors and better discrete packaging (or no packaging, just die), we also have device combinations with functionally integrated blocks with either the controller included or driver power device partitioned to using an external controller. We also have complete power stages: just add the missing blocks and you are ready to process power. In other words, designers can add a handful of external parts, use the online tools to do the design, and they have a fully working power converter with relative ease compared to yesteryear.

In the DC-DC area, integrated point-of-load (POL) devices, complete with integrated magnetics, are available and cost effective. And even though we have access to parts for our designs that would have seemed to be out of science fiction not long ago, some things were predicted incorrectly. For instance, the demise of through-hole devices and small-signal semiconductors. They are still used for new designs daily and will be with us a long time.

What is next when it comes to device and package options? If past is prologue, I would say the possibilities are endless.

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Solar Inverter Design
The Race to Design High-Efficiency, High-Power-Density Inverters
By: Mostafa Khazraei, Senior Staff Application Engineer and Damijan Zupanic, Application Engineer, Infineon Technologies

Due to the ever-increasing demand for a clean and renewable source of energy, installing solar systems has accelerated significantly in the last decade. Contemporary solar applications require very highly efficient, power-dense and lightweight grid-tied inverters.

Traditionally, IGBT has been the device of choice in both three-phase and single-phase (≤10 kW) solar inverter designs while superjunction (SJ) MOSFETS (600/650 V) also have been used in some single-phase designs. But both IGBTs and SJ MOSFETS have their drawbacks that limit the efficiency and power density of inverters.

Recently engineers have focused on two different approaches to improve efficiency and power density of single-phase inverters to even higher levels. One is replacing IGBT and SJ MOSFETS with wide bandgap devices like SiC MOSFETS. Another approach is replacing the traditional topologies (H4, H5, H6, etc.) with multilevel topologies using lower voltage silicon MOSFETS. As we discuss in this article, using these two approaches efficiency up to 99% and very high power density inverters can be designed.

Replacing IGBTs and SJ MOSFETS with SiC MOSFETS
IGBTs suffer from high switching losses that limit their use to only frequencies less than 20 kHz. On the other hand, high Qrr, slow body diode and relatively high RDS(on) limit SJ MOSFETS usage in inverter applications. These constraints limit the efficiency and power density of conventional single-phase solar inverters to around 98% and below.

On the contrary, SiC MOSFETS offer very fast parallel diode, very low Qrr and switching losses much lower than IGBTs. Recently, Infineon has introduced its 650 V silicon carbide CoolSiC™ MOSFET that can directly replace IGBTs and SJ MOSFETS with no need for change in the inverter topology. SiC MOSFETS enable switching at a higher frequency which means a significant reduction in magnetic size, capacitor filter, and enclosure size. As the power level goes up, reduction in size and weight will save costs. Figure 1 clearly indicates how by replacing a SJ with a SiC MOSFET, switching loss decreases significantly.

As shown in figure 1, considered in terms of drain-source charge (QDS), recovery charge (Qrr) and gate charge (Qg), SiC MOSFETS (i.e., the CoolSiC™ MOSFET 650 V) have superior figures-of-merit than the best alternative SJ MOSFETS (i.e., 600 V CoolMOS™ CFD).
Compared to the conventional design, the inductor and capacitor filter size is multiple times smaller in a multilevel inverter. This, along with the need for a smaller cooling system, allows for a much lighter design with a smaller enclosure. On the other hand, due to the lower voltage rating of MV MOSFETs, more MOSFETs are used in a multilevel design compared to conventional topologies. This also means that the generated heat due to the power loss in the multilevel inverter (which is less than in a conventional design) is distributed among more devices. As a result, the thermal management of the multilevel inverter is more efficient which paves the way for heatsink-free and fanless designs.

Replacing traditional topologies with multilevel topologies

Traditionally topologies like H4, H5, H6, and so on using IGBTs and SJ MOSFETs have been widely used in single-phase solar inverter applications. One novel approach that has gained more attention recently to improve efficiency and power density is to replace these conventional topologies with multilevel topology (for an example see Figure 3), based on medium-voltage MOSFETs (60 V to 300 V). Infineon’s OptiMOS™ 5 product family of medium-voltage MOSFETs have excellent figures-of-merit (extremely low $R_{DS(on)} \times Q_g$, $R_{DS(on)} \times Q_{rr}$, and $R_{DS(on)} \times Q_{oss}$) and enable very high-efficiency (up to 99 percent) and power-density designs, when used in multilevel inverters.

In a typical single-phase string inverter (power ≥ 3 kW), semiconductors commonly account for less than 10 percent of the overall costs. However, cooling systems and magnetics are usually more expensive. While semiconductor device prices are continuously dropping, the cost of other components such as magnetic and heatsinks remain unchanged. That means for single-phase solar inverters with a full power capability of more than 3 kW, where the cost of mechanical components is a significant portion of the design, using multilevel inverter contributes to production cost saving.

One other big advantage of multilevel inverter is that lower loss per MOSFET allows using SMD packages. Utilizing SMD packages helps with assembly cost saving by applying automated pick and place process. In addition, the reduced package inductances improve the switching performance at higher frequencies.

Scalability is another big advantage of multilevel inverters. A multilevel inverter can be easily scaled to higher power design with almost the same design and PCB layout.

But to mention, multilevel inverters face one big challenge too. Compared to conventional topologies, there is a need for a greater number of gate drivers and isolated power supplies to power them up. This challenge is tackled by using very
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Figure 3: Increase efficiency and power density by replacing conventional topologies with multilevel topology

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Figure 4 shows the schematic of the multilevel inverter demonstration board while Table 1 lists the specification of this inverter. Given that this is a five-level inverter, 150 V BSC09615N65 (9.3 mΩ, OptiMOS™ 5) MOSFETs were used despite the 400 VDC bus voltage. This device has much better figures-of-merit (orders of magnitude) compared to IGBTs and SJ MOSFETs.

Figure 5 shows the efficiency of the demonstration board in relation to the output power. The maximum efficiency (approximately 99.1 percent) is achieved at around 2 kW. At full load (4 kW), the efficiency is still very high, at around 98.7 percent.

Beyond question, replacing silicon-based devices with SiC MOSFETs requires less effort compared to altering the topology. But although this change to SiC will increase efficiency and power density, still not as much as the multilevel solution. A heatsink is still needed and for a higher power range (>5 kW), forced cooling probably should be also considered.

Table 1: Multilevel inverter specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input DC voltage (Vdc), load</td>
<td>400 V, passive RL load</td>
</tr>
<tr>
<td>Switch type</td>
<td>2BSC09615N65 (150 V, 6.5 mΩ), overall 48 MOSFETs, gate driver: 12-2EDF7275F</td>
</tr>
<tr>
<td>Effective output switching frequency</td>
<td>40 kHz</td>
</tr>
<tr>
<td>Max. continuous power</td>
<td>4000 VA</td>
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</tbody>
</table>

Infinion Technologies AG www.infineon.com

Figure 5: Efficiency of the demonstration board in relation to the output power

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<td>Power density</td>
<td>1 W</td>
</tr>
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</table>

The 4 kW heatsink-free, fanless, medium-voltage MOSFET-based multilevel inverter

In this section, a 4 kW, five-level single-phase flying-capacitor-based active neutral point clamped multilevel inverter demonstration board will be introduced. This fanless, heatsink-free design offers more than 99 percent peak efficiency and full power efficiency as of 98.7 percent.

Figure 4 shows the schematic of the multilevel inverter

Conclusion

Now the question for an inverter designer who is looking for higher efficiency and power density is which one of the above-described solutions to choose. Replacing IGBTs and SJ MOSFETs with SiC MOSFETs or replacing the conventional with the multilevel topology?

Beyond question, replacing silicon-based devices with SiC MOSFETs requires less effort compared to altering the topology. But although this change to SiC will increase efficiency and power density, still not as much as the multilevel solution. A heatsink is still needed and for a higher power range (>5 kW), forced cooling probably should be also considered.

Even though the multilevel topology is more complex than conventional topologies, if a designer has previous experience with this type of topology or willing to learn and invest R&D effort into it, moving to the multilevel inverter is recommended as 99 percent of efficiency and very high power density can be easily achieved.

Transformer loss elements, core-related

Hysteresis loss derives from the energy required to alternately align core magnetic domains as magnetisation continuously reverses with applied high-frequency current. The loss can intuitively be seen as related to frequency, or the number of times per second the domains are reversed and the degree of magnetisation of the material or flux density (teslas). This in turn is proportional to voltage applied to a driven winding at frequency and inversely proportional to core cross-sectional area and number of turns on the winding. The constants of proportionality vary with temperature and frequency for different mixes of core materials, so the best guide to actual losses is the published curves by core material manufacturers, Figure 1 for

Modern power conversion techniques all push towards higher efficiency for good reason; energy saving is clearly important but there are applications where functionality is also enhanced. Examples would be alternative energy systems such as solar and wind, and electric vehicle chargers where fewer losses equate to shorter recharging times or longer range for a given charge time. Better efficiency can also yield smaller, lighter and cooler operating equipment, enhancing usability and reliability. An enabling technology for higher efficiency has been the introduction of wide band-gap semiconductors such as silicon carbide (SiC) and now gallium nitride (GaN), which have reduced switch losses dramatically with their low on-resistance, fast switching and low device capacitances.

With such improvements in semiconductors, focus has increasingly shifted to losses elsewhere in power converters, particularly in magnetics. Previously, losses in high-frequency transformers, for example, were not considered substantial for system efficiency considerations. Now, however, just 1% of output power dissipated in a transformer could be the whole loss budget. Over the years, better materials have lowered core losses, but winding techniques are often still rooted in the 19th century. Now that operating frequencies have increased, the form factors of proportionality vary with different mixtures of core materials, so the best guide to actual losses is the published curves by core material manufacturers, Figure 1 for

Figure 1: Transformer loss elements, core-related