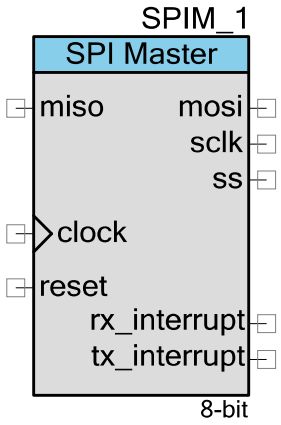
Serial Peripheral Interface (SPI) Master

2.21



Features

- 3- to 16-bit data width
- Four SPI operating modes
- Bit rate up to 18 Mbps*

General Description

The SPI Master component provides an industry-standard, 4-wire master SPI interface. It can also provide a 3-wire (bidirectional) SPI interface. Both interfaces support all four SPI operating modes, allowing communication with any SPI slave device. In addition to the standard 8-bit word length, the SPI Master supports a configurable 3- to 16-bit word length for communicating with nonstandard SPI word lengths.

SPI signals include the standard Serial Clock (SCLK), Master In Slave Out (MISO), Master Out Slave In (MOSI), bidirectional Serial Data (SDAT), and Slave Select (SS).

When to Use the SPI Master

Use the SPI Master component any time the PSoC device must interface with one or more SPI slave devices. In addition to “SPI slave” labeled devices, you can use the SPI Master with many devices implementing a shift-register-type serial interface.

Use the SPI Slave component in instances in which the PSoC device must communicate with an SPI master device. Use the Shift Register component in situations where its low-level flexibility provides hardware capabilities not available in the SPI Master component.

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* This value is valid only for the case when High Speed Mode Enable option is set (see DC and AC Electrical Characteristics for details) . Otherwise, the maximum bit rate value is up to 9 Mbps.

Input/Output Connections

This section describes the various input and output connections for the SPI component. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

miso – Input *

The miso input carries the Master In Slave Out (MISO) signal from a slave device. This input is visible when the **Data Lines** parameter is set to **MOSI + MISO**. If visible, this input must be connected.

sdat – Inout *

The sdat inout carries the Serial Data (SDAT) signal. This input is used when the **Data Lines** parameter is set to **Bidirectional**.

Figure 1. SPI Bidirectional Mode (data transmission from Master to Slave)

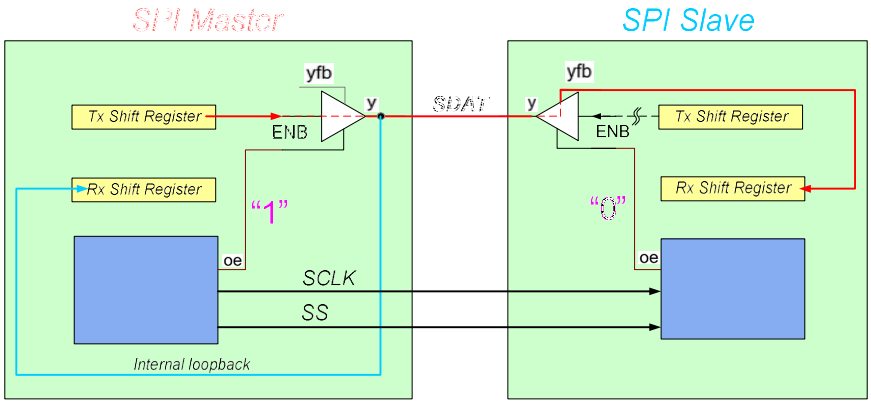
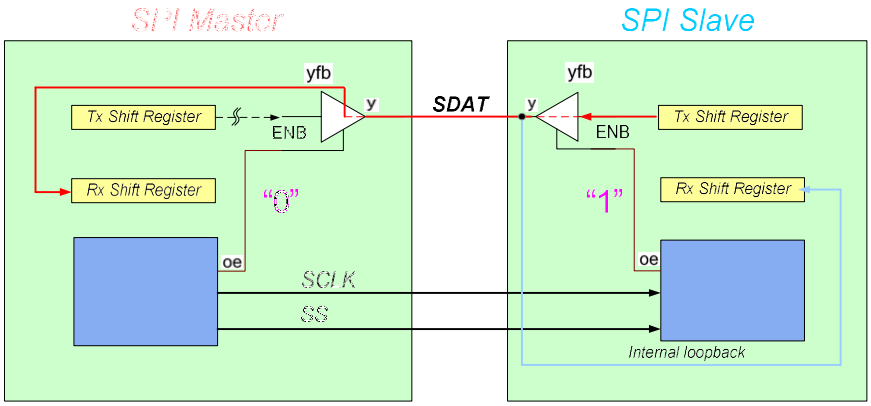


Figure 2. SPI Bidirectional Mode (data transmission from Slave to Master)



The component's initial state in Bidirectional Mode is Rx mode or data transmission from Slave to Master, as shown in Figure 2. Use the SPIM_TxEnable() and SPIM_Tx_Disable() API functions to switch between Rx and Tx mode.

clock – Input *

The clock input defines the bit rate of the serial communication. The bit rate is one-half the input clock frequency.

The clock input is visible when the **Clock Selection** parameter is set to **External Clock**. If visible, this input must be connected. If you select **Internal Clock**, you must define the desired data bit rate; PSoC Creator solves and provides the required clock.

reset – Input

Resets the SPI state machine to the idle state. This throws out any data that was currently being transmitted or received but does not clear data from the FIFO that has already been received or is ready to be transmitted. Note that ES2 silicon does not support routed reset functionality, so leave this input unconnected when the component is used in ES2 silicon projects.

mosi – Output *

The mosi output carries the Master Out Slave In (MOSI) signal from the master device on the bus. This output is visible when the **Data Lines** parameter is set to **MOSI + MISO**.

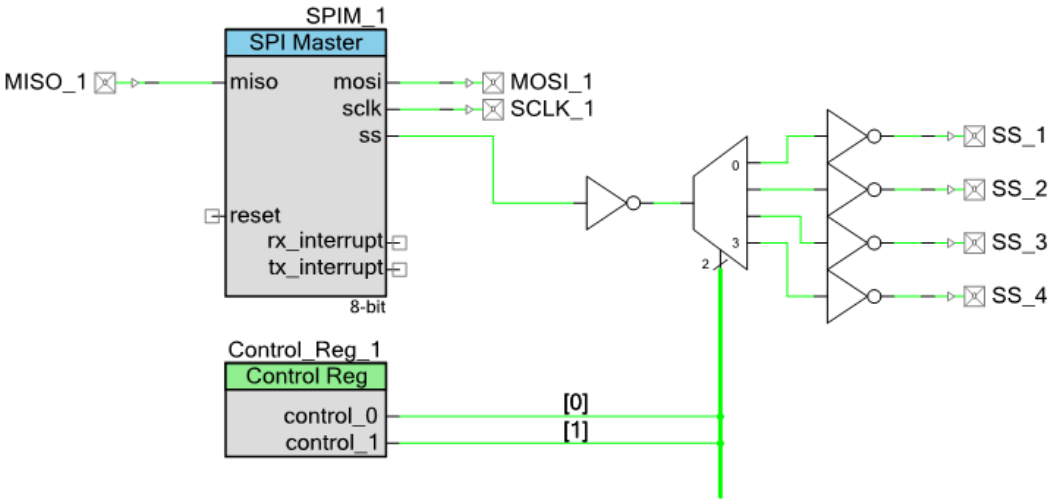
sclk– Output

The sclk output carries the Serial Clock (SCLK) signal. It provides the master synchronization clock output to the slave devices on the bus.

ss – Output

The ss output is hardware controlled. It carries the Slave Select (SS) signal to the slave devices on the bus. You can connect a digital demultiplexer to handle multiple slave devices, or to have a completely firmware-controlled SS. See Figure 3 and Figure 4 for examples.

Figure 3. Slave Select Output to Demultiplexer



Unless you put inverters at the output of the demux, a logic ‘0’ can’t be transferred through it, because the other unselected channels will also have logic ‘0’. To compensate for this, put an inverter at the input of the demux.

Figure 4. Firmware Controlled Slave Selects

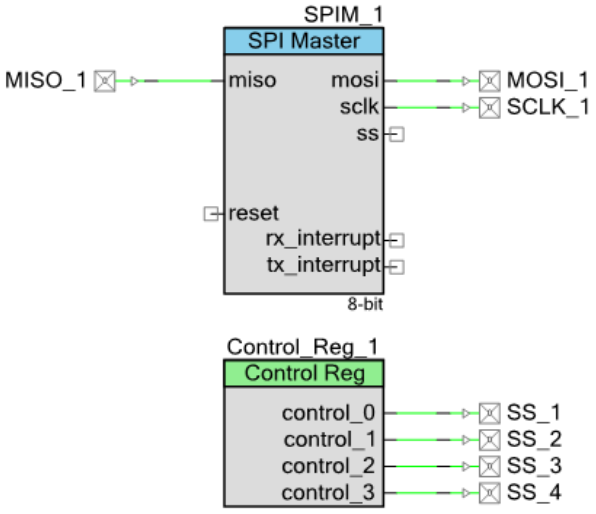
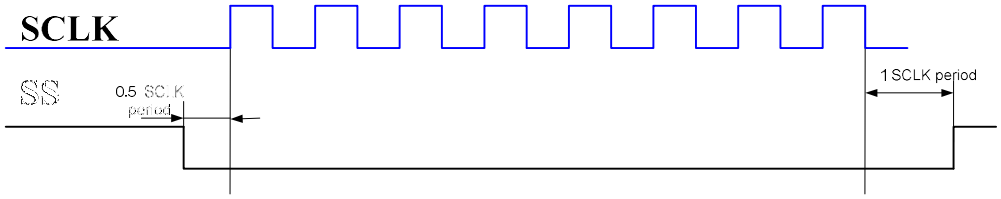


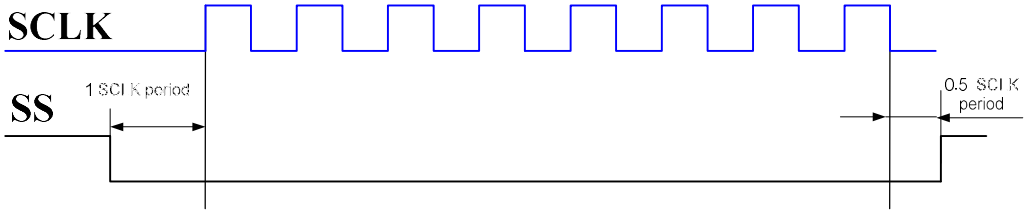
Figure 5 shows the timing correlation between SS and SCLK.

Figure 5. SS and SCLK Timing Correlation

CPHA =0:



CPHA =1:



Note SS is not set to high during a multi-byte/word transmission if the “SPI Done” condition was not generated.

rx_interrupt – Output

The interrupt output is the logical OR of the group of possible Rx interrupt sources. This signal goes high while any of the enabled Rx interrupt sources are true.

tx_interrupt – Output

The interrupt output is the logical OR of the group of possible Tx interrupt sources. This signal goes high while any of the enabled Tx interrupt sources are true.

Schematic Macro Information

By default, the PSoC Creator Component Catalog contains Schematic Macro implementations for the SPI Master component. These macros contain already connected and adjusted input and output pins and clock source. Schematic Macros are available both for 4-wire (Full Duplex) and 3-wire (Bidirectional) SPI interfacing.

Figure 6. 4-Wire (Full Duplex) Interfacing Schematic Macro

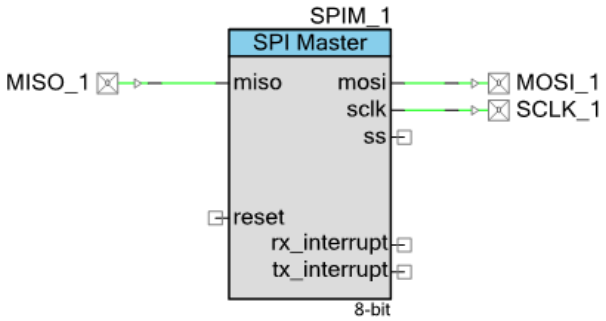
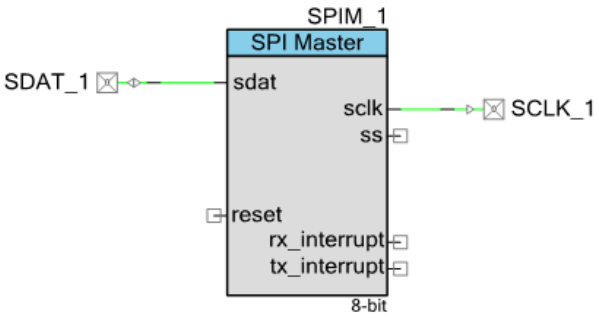


Figure 7. 3-Wire (Bidirectional) Interfacing Schematic Macro



Note If you do not use a Schematic Macro, configure the Pins component to deselect the Input Synchronized parameter for each of the assigned input pins (MISO or SDAT inout). The parameter is located under the Pins > Input tab of the applicable Pins Configure dialog.

Component Parameters

Drag an SPI Master component onto the design. Double-click the component symbol to open the **Configure** dialog.

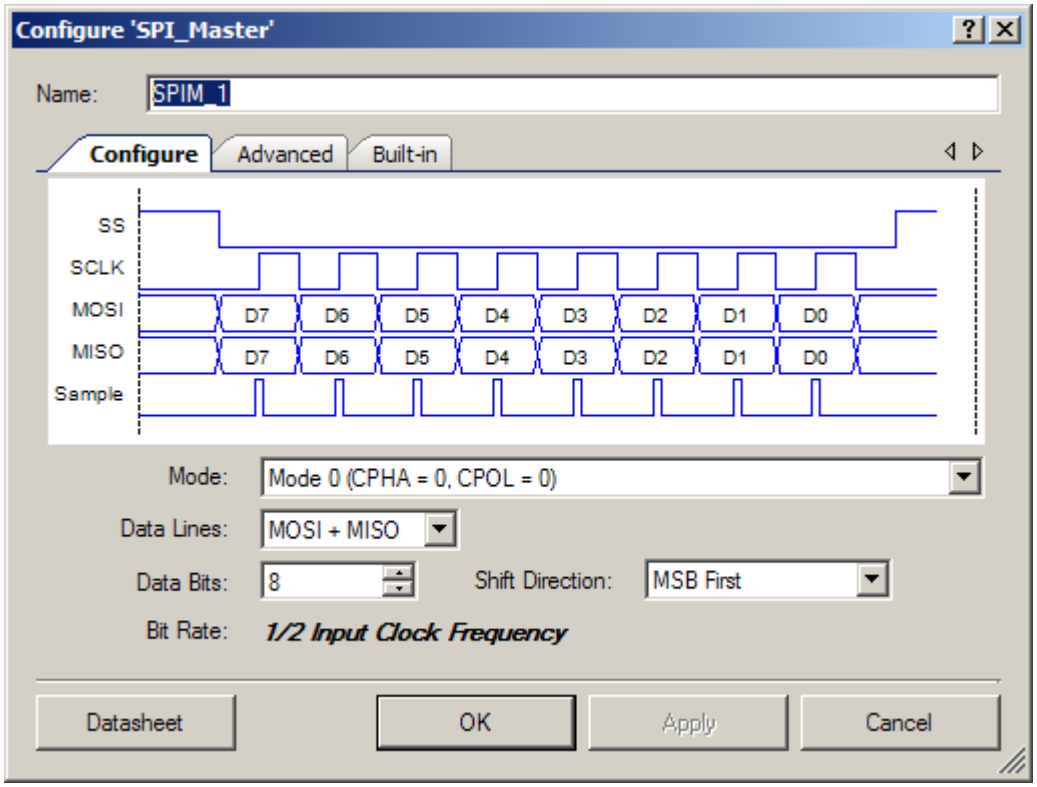
The following sections describe the SPI Master parameters, and how they are configured using the Configure dialog. They also indicate whether the options are implemented in hardware or software.

Hardware versus Software Options

Hardware configuration options change the way the project is synthesized and placed in the hardware. You must rebuild the hardware if you make changes to any of these options. Software configuration options do not affect synthesis or placement. When setting these parameters before build time you are setting their initial value, which can be modified at any time with the provided APIs. Hardware-only parameters are marked with an asterisk (*).

Configure Tab

The **Configure** tab contains basic parameters required for every SPI component. These parameters are the first ones that appear when you open the **Configure** dialog.



Note The sample signal in the waveform is not an input or output of the system; it only indicates when the data is sampled at the master and slave for the mode settings selected.

Mode *

The **Mode** parameter defines the clock phase and clock polarity mode you want to use in the communication. The options are **Mode 0**, **Mode 1**, **Mode 2**, and **Mode 3**. These modes are defined in the following table. See Functional Description for more information.

Mode	CPHA	CPOL
0	0	0
1	0	1
2	1	0
3	1	1

Data Lines

The **Data Lines** parameter defines which interface is used for SPI communication: 4-wire (MOSI + MISO) or 3-wire (Bidirectional).

Data Bits *

The number of **Data Bits** defines the bit width of a single transfer as transferred with the SPIM_ReadRxData() and SPIM_WriteTxData() functions. The default number of bits is a single byte (8 bits). Any integer from 3 to 16 is a valid setting.

Shift Direction *

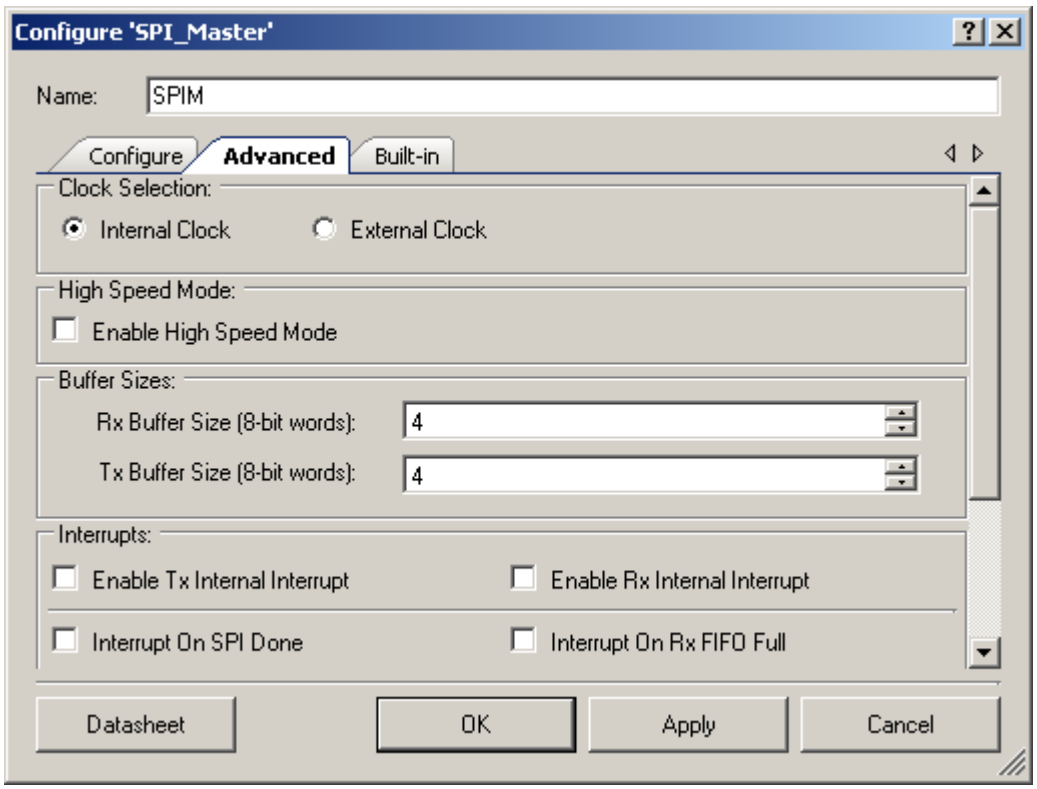
The **Shift Direction** parameter defines the direction in which the serial data is transmitted. When set to **MSB First**, the most-significant bit is transmitted first. This is implemented by shifting the data left. When set to **LSB First**, the least-significant bit is transmitted first. This is implemented by shifting the data right.

Bit Rate *

If the **Clock Selection** parameter (on the **Advanced** tab) is set to **Internal Clock**, the **Bit Rate** parameter defines the SCLK speed in Hertz. The clock frequency of the internal clock is 2x the SCLK rate. This parameter has no effect if the **Clock Selection** parameter is set to **External Clock**.

Advanced Tab

The **Advanced** tab contains parameters that provide additional functionality.



Clock Selection *

The **Clock Selection** parameter allows you to choose between an internally configured clock or an externally configured clock for data rate and SCLK generation. When set to **Internal Clock**, PSoC calculates and configures the required clock frequency based on the **Bit Rate** parameter. When set to **External Clock**, the component does not control the data rate but displays the expected bit rate based on the user-connected clock source. If this parameter is set to **Internal Clock**, the clock input is not visible on the symbol.

Note When setting the bit rate or external clock frequency value, make sure that PSoC Creator can provide this value using the current system clock frequency. Otherwise, a warning about the clock accuracy range is generated while building the project. This warning contains the actual clock value set by PSoC Creator. Choose whether the system clock or component clock should be changed to fit the clocking system requirements and achieve an optimal value.

RX Buffer Size *

The **RX Buffer Size** parameter defines the size (in bytes/words) of memory allocated for a circular data buffer. If this parameter is set to 1 to 4, the fourth byte/word of the FIFO is implemented in the hardware. Values 1 to 3 are available only for compatibility with the previous versions; using them causes an error icon to display that the value is incorrect. All other values up to 255 bytes/words use the 4-byte/word FIFO and a memory array controlled by the supplied API.

TX Buffer Size *

The **TX Buffer Size** parameter defines the size (in bytes/words) of memory allocated for a circular data buffer. If this parameter is set to 1 to 4, the fourth byte/word of the FIFO is implemented in the hardware. Values 1 to 3 are available only for compatibility with the previous versions; using them causes an error icon to display that the value is incorrect. All other values up to 255 use the 4-byte/word FIFO and a memory array controlled by the supplied API.

Using the Software Buffer

Selecting Rx/Tx Buffer Size values greater than 4 allows you to use the Rx/Tx circular software buffers. The internal interrupt handler is used when you select the Tx/Rx software buffer option. Its main purpose is to provide interaction between software and hardware Tx/Rx buffers. In the initial state, the BufferRead and BufferWrite pointers point to the zero element of the software buffer. After writing the first data, the BufferWrite pointer moves to the first element of the software buffer and points to writing data; the BufferRead pointer stays on the zero element. As the buffers work, the pointers move to the next buffer elements. The BufferWrite pointer points to the last written data,. The BufferRead pointer points to the oldest data that has not been read. Software buffer overflow can happen without any overflow indication. You must handle any software buffer overflow situation.

You should also consider that using the software buffer leads to greater timing intervals between transmitted words because of the extra time the interrupt handler needs to execute (depending on the selected bus clock value). When setting timing intervals between transmitted words, use DMA along with a hardware buffer.

Enable High Speed Mode

The **Enable High Speed Mode** parameter allows you to extend maximum bit rate value to 18 Mbps (see DC and AC Electrical Characteristics for details). When this option is not enabled, the SPI Master component samples the MISO signal one-half clock cycle after the SCLK clock edge that initiates a read from the SPI slave. In High Speed mode, the MISO signal is sampled a full clock cycle after the SCLK clock edge that initiates the read. So, you can use High Speed mode with any SPI slave device that maintains the MISO signal for the full clock cycle. This is typical of most SPI slave implementations.

Enable TX / RX Internal Interrupt

The **Enable TX / RX Internal Interrupt** options allow you to use the predefined Tx and Rx ISRs of the SPI Master component, or supply your own custom ISRs. If enabled, you may add your own code to these predefined ISRs if small changes are required. If the internal interrupt is deselected, you may supply an external interrupt component with custom code connected to the interrupt outputs of the SPI Master.

If the Rx or Tx buffer size is greater than 4, the component automatically sets the appropriate parameters. The internal ISR is needed to handle transferring data from the hardware FIFO to the Rx buffer, the Tx buffer, or both. The interrupt output pins of the SPI Master are always visible and usable, outputting the same signal that goes to the internal interrupt. This output can

then be used as a DMA request source or as a digital signal to be used as required in the programmable digital system.

Notes:

- When Rx buffer size is greater than 4 bytes/words, the 'RX FIFO NOT EMPTY' interrupt is always enabled and cannot be disabled, because it causes incorrect buffer functionality.
- When Tx buffer size is greater than 4 bytes/words, the 'TX FIFO NOT FULL' interrupt is always enabled and cannot be disabled, because it causes incorrect buffer functionality.
- For buffer sizes greater than 4 bytes/words, the SPI slave and global interrupt must be enabled for proper buffer handling.

Interrupts

The **Interrupts** selection parameters allow you to configure the internal events that are enabled to cause an interrupt. Interrupt generation is a masked OR of all of the enabled Tx and Rx status register bits. The bits chosen with these parameters define the mask implemented with the initial component configuration.

Clock Selection

When the internal clock configuration is selected, PSoC Creator calculates the needed frequency and clock source, and generates the clocking resource needed for implementation. Otherwise, you must supply the clock component and calculate the required clock frequency. That frequency is 2x the desired bit rate and SCLK frequency.

Note When setting the bit rate or external clock frequency value, make sure that PSoC Creator can provide this value by using the current system clock frequency. Otherwise, a warning about the clock accuracy range is generated while building the project. This warning contains the real clock value set by PSoC Creator. Choose whether the system clock or component clock should be changed to fit the clocking system requirements and achieve an optimal value.

Placement

The SPI Master component is placed into the UDB array and all placement information is provided to the API through the *cyfitter.h* file.

Resources

Resolution	Digital Blocks				API Memory (Bytes)		Pins (per External I/O)
	Datapath Cells	PLDs	Status Cells	Control/ Counter7 Cells	Flash	RAM	
8-bit (MOSI+MISO)	1	5	2	1	849	19	7
8-bit (Bidirectional)	1	5	2	1	849	19	6
16-bit (MOSI+MISO)	2	5	2	1	926	21	7
16-bit (Bidirectional)	2	5	2	1	926	21	6
8-bit High Speed (MOSI+MISO)	1	7	2	1	849	19	7
8-bit High Speed (Bidirectional)	1	7	2	1	849	19	6
16-bit High Speed (MOSI+MISO)	2	7	2	1	926	21	7
16-bit High Speed (Bidirectional)	2	7	2	1	926	21	6

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software at run time. The following table lists and describes the interface to each function. The subsequent sections discuss each function in more detail.

By default, PSoC Creator assigns the instance name “SPIM_1” to the first instance of a component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol for the instance. For readability, the instance name used in the following table is “SPIM.”

Function	Description
SPIM_Start()	Calls both SPIM_Init() and SPIM_Enable(). Should be called the first time the component is started.
SPIM_Stop()	Disables SPI Master operation.

Function	Description
SPIM_EnableTxInt()	Enables the internal Tx interrupt irq.
SPIM_EnableRxInt()	Enables the internal Rx interrupt irq.
SPIM_DisableTxInt()	Disables the internal Tx interrupt irq.
SPIM_DisableRxInt()	Disables the internal Rx interrupt irq.
SPIM_SetTxInterruptMode()	Configures the Tx interrupt sources enabled.
SPIM_SetRxInterruptMode()	Configures the Rx interrupt sources enabled.
SPIM_ReadTxStatus()	Returns the current state of the Tx status register.
SPIM_ReadRxStatus()	Returns the current state of the Rx status register.
SPIM_WriteTxData()	Places a byte/word, which will be sent at the next available bus time, in the transmit buffer.
SPIM_ReadRxData()	Returns the next byte/word of received data available in the receive buffer.
SPIM_GetRxBufferSize()	Returns the size (in bytes/words) of received data in the Rx memory buffer.
SPIM_GetTxBufferSize()	Returns the size (in bytes/words) of data waiting to transmit in the Tx memory buffer.
SPIM_ClearRxBuffer()	Clears the Rx buffer memory array and Rx FIFO of all received data.
SPIM_ClearTxBuffer()	Clears the Tx buffer memory array and Tx FIFO of all transmit data.
SPIM_TxEnable()	If configured for bidirectional mode, sets the SDAT inout to transmit.
SPIM_TxDisable()	If configured for bidirectional mode, sets the SDAT inout to receive.
SPIM_PutArray()	Places an array of data into the transmit buffer.
SPIM_ClearFIFO()	Clears any received data from the Rx hardware FIFO.
SPIM_Sleep()	Prepares the SPI Master component for low-power modes by calling the SPIM_SaveConfig() and SPIM_Stop() functions.
SPIM_Wakeup()	Restores and re-enables the SPI Master component after waking from low-power mode.
SPIM_Init()	Initializes and restores the default SPI Master configuration.
SPIM_Enable()	Enables the SPI Master to start operation.
SPIM_SaveConfig()	Saves the SPI Master hardware configuration.
SPIM_RestoreConfig()	Restores the SPI Master hardware configuration.

Global Variables

Variable	Description
SPIM_initVar	Indicates whether the SPI Master has been initialized. The variable is initialized to 0 and set to 1 the first time SPIM_Start() is called. This allows the component to restart without reinitialization after the first call to the SPIM_Start() routine. If reinitialization of the component is required, then the SPIM_Init() function can be called before the SPIM_Start() or SPIM_Enable() function.
SPIM_txBufferWrite	Transmits the buffer location of the last data written into the buffer by the API.
SPIM_txBufferRead	Transmits the buffer location of the last data read from the buffer and transmitted by the SPI Master hardware.
SPIM_rxBufferWrite	Receives the buffer location of the last data written into the buffer after being received by the SPI Master hardware.
SPIM_rxBufferRead	Receives the buffer location of the last data read from the buffer by the API.
SPIM_rxBufferFull	Indicates the software buffer has overflowed.
SPIM_RXBUFFER[]	Stores received data.
SPIM_TXBUFFER[]	Stores data for sending.

void SPIM_Start(void)

Description: This function calls both SPIM_Init() and SPIM_Enable(). This should be called the first time the component is started.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_Stop(void)

Description: This function disables SPI Master operation by disabling the internal clock and internal interrupts, if the SPI Master is configured that way.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_EnableTxInt(void)

Description: This function enables the internal Tx interrupt irq.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_EnableRxInt(void)

Description: This function enables the internal Rx interrupt irq.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_DisableTxInt(void)

Description: This function disables the internal Tx interrupt irq.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_DisableRxInt(void)

Description: This function disables the internal Rx interrupt irq.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_SetTxInterruptMode(uint8 intSrc)

Description: This function configures which status bits trigger an interrupt event.

Parameters: uint8 intSrc: Bit field containing the interrupts to enable.

Bit	Description
SPIM_INT_ON_SPI_DONE	Enable interrupt caused by SPI done
SPIM_INT_ON_TX_EMPTY	Enable interrupt caused by Tx FIFO empty
SPIM_INT_ON_TX_NOT_FULL	Enable interrupt caused by Tx FIFO not full
SPIM_INT_ON_BYTE_COMP	Enable interrupt caused by byte/word complete
SPIM_INT_ON_SPI_IDLE	Enable interrupt caused SPI IDLE

Based on the bit-field arrangement of the Tx status register. This value must be a combination of Tx status register bit masks defined in the header file.

For more information, see Defines.

Return Value: None

Side Effects: None

void SPIM_SetRxInterruptMode(uint8 intSrc)

Description: This function configures which status bits trigger an interrupt event.

Parameters: uint8 intSrc: Bit field containing the interrupts to enable.

Bit	Description
SPIM_INT_ON_RX_FULL	Enable interrupt caused by Rx FIFO Full
SPIM_INT_ON_RX_NOT_EMPTY	Enable interrupt caused by Rx FIFO Not Empty
SPIM_INT_ON_RX_OVER	Enable interrupt caused by Rx Buf Overrun

Based on the bit-field arrangement of the Rx status register. This value must be a combination of Rx status register bit masks defined in the header file.

For more information, see Defines.

Return Value: None

Side Effects: None

uint8 SPIM_ReadTxStatus(void)

Description: This function returns the current state of the Tx status register. For more information, see Status Register Bits.

Parameters: None

Return Value: uint8: Current Tx status register value

Bit	Description
SPIM_STS_SPI_DONE	SPI done
SPIM_STS_TX_FIFO_EMPTY	Tx FIFO empty
SPIM_STS_TX_FIFO_NOT_FULL	Tx FIFO not full
SPIM_STS_BYTE_COMPLETE	Byte/Word complete
SPIM_STS_SPI_IDLE	SPI IDLE

Side Effects: Tx Status register bits are cleared on read.

uint8 SPIM_ReadRxStatus(void)

Description: This function returns the current state of the Rx status register. For more information, see Status Register Bits.

Parameters: None

Return Value: uint8: Current Rx status register value

Bit	Description
SPIM_STS_RX_FIFO_FULL	Rx FIFO Full
SPIM_STS_RX_FIFO_NOT_EMPTY	Rx FIFO Not Empty
SPIM_STS_RX_FIFO_OVERRUN	Rx Buf Overrun

Side Effects: Rx Status register bits are cleared on read.

void SPIM_WriteTxData(uint8/uint16 txData)

Description: This function places a byte/word in the transmit buffer to be sent at the next available SPI bus time.

Parameters: uint8/uint16 txData: The data value to transmit from the SPI.

Return Value: None

Side Effects: Data may be placed in the memory buffer and will not be transmitted until all other previous data has been transmitted. This function blocks until there is space in the output memory buffer.

Clears the Tx status register of the component.

uint8/uint16 SPIM_ReadRxData(void)

Description: This function returns the next byte/word of received data available in the receive buffer.

Parameters: None

Return Value: uint8/uint16: The next byte/word of data read from the FIFO.

Side Effects: Returns invalid data if the FIFO is empty. Call SPIM_GetRxBufferSize(), and if it returns a nonzero value then it is safe to call the SPIM_ReadRxData() function.

uint8 SPIM_GetRxBufferSize(void)

Description: This function returns the number of bytes/words of received data currently held in the Rx buffer.

- If the Rx software buffer is disabled, this function returns 0 = FIFO empty or 1 = FIFO not empty.
- If the Rx software buffer is enabled, this function returns the size of data in the Rx software buffer. FIFO data is not included in this count.

Parameters: None

Return Value: uint8: Integer count of the number of bytes/words in the Rx buffer

Side Effects: Clears the Rx status register of the component.

uint8 SPIM_GetTxBufferSize(void)

Description: This function returns the number of bytes/words of data ready to transmit currently held in the Tx buffer.

- If the Tx software buffer is disabled, this function returns 0 = FIFO empty, 1 = FIFO not full, or 4 = FIFO full.
- If the Tx software buffer is enabled, this function returns the size of data in the Tx software buffer. FIFO data is not included in this count.

Parameters: None

Return Value: uint8: Integer count of the number of bytes/words in the Tx buffer

Side Effects: Clears the Tx status register of the component.

void SPIM_ClearRxBuffer(void)

Description: This function clears the Rx buffer memory array and Rx hardware FIFO of all received data. Clears the Rx RAM buffer by setting both the read and write pointers to zero. Setting the pointers to zero indicates that there is no data to read. Thus, writing resumes at address 0, overwriting any data that may have remained in the RAM.

Parameters: None

Return Value: None

Side Effects: Any received data not read from the RAM buffer and FIFO is lost when overwritten by new data.

void SPIM_ClearTxBuffer(void)

Description: This function clears the Tx buffer memory array of data waiting to transmit. Clears the Tx RAM buffer by setting both the read and write pointers to zero. Setting the pointers to zero indicates that there is no data to transmit. Thus, writing resumes at address 0, overwriting any data that may have remained in the RAM.

Parameters: None

Return Value: None

Side Effects: Does not clear data already placed in the Tx FIFO. Any data not yet transmitted from the RAM buffer is lost when overwritten by new data.

void SPIM_TxEnable(void)

Description: If the SPI Master is configured to use a single bidirectional pin, this function sets the bidirectional pin to transmit.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_TxDisable(void)

Description: If the SPI master is configured to use a single bidirectional pin, this function sets the bidirectional pin to receive.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_PutArray(uint8/uint16 * buffer, uint8/uint16 byteCount)

Description: This function places an array of data into the transmit buffer

Parameters: uint8 * buffer: Pointer to the location in RAM containing the data to send

uint8/uint16 byteCount: The number of bytes/words to move to the transmit buffer

Return Value: None

Side Effects: The system will stay in this function until all data has been transmitted to the buffer. This function is blocking if there is not enough room in the Tx buffer. It may get locked in this loop if data is not being transmitted by the master and the Tx buffer is full.

void SPIM_ClearFIFO(void)

Description: This function clears any received data from the Tx and Rx FIFOs.

Parameters: None

Return Value: None

Side Effects: Clears status register of the component.

void SPIM_Sleep (void)

Description: This function prepares the SPI Master for low-power modes by calling the SPIM_SaveConfig() and SPIM_Stop() functions.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_Wakeup (void)

Description: This function prepares the SPI Master to wake up from a low-power mode. It calls the SPIM_RestoreConfig() and SPIM_Enable() functions and clears all data from the Rx buffer, Tx buffer, and hardware FIFOs.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_Init(void)

Description: This function initializes or restores the component according to the customizer Configure dialog settings. It is not necessary to call SPIM_Init() because the SPIM _Start() routine calls this function and is the preferred method to begin component operation.

Parameters: None

Return Value: None

Side Effects: When this function is called, it initializes all of the necessary parameters for execution. These include setting the initial interrupt mask, configuring the interrupt service routine, configuring the bit-counter parameters, and clearing the FIFO and Status Register.

void SPIM_Enable(void)

Description: This function enables the SPI Master for operation. It starts the internal clock if the SPI Master is configured that way. If the SPI Master is configured for an external clock, it must be started separately before calling this function. The SPIM_Enable() function should be called before SPI Master interrupts are enabled. This is because this function configures the interrupt sources and clears any pending interrupts from device configuration, and then enables the internal interrupts if there are any. A SPIM_Init() function must have been previously called.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_SaveConfig(void)

Description: This function saves SPI Master hardware configuration before entering a low-power mode.

Parameters: None

Return Value: None

Side Effects: None

void SPIM_RestoreConfig(void)

Description: This function restores the SPI Master hardware configuration saved by the SPIM_SaveConfig() function after waking from a lower-power mode.

Parameters: None

Return Value: None

Side Effects: If this function is called without first calling SPIM_SaveConfig(),the following registers are restored to the default values from the Configure dialog:

```
SPIM_STATUS_MASK_REG
SPIM_COUNTER_PERIOD_REG
```

Defines

- **SPIM_TX_INIT_INTERRUPTS_MASK** – Defines the initial configuration of the interrupt sources chosen in the Configure dialog. This is a mask of the bits in the Tx status register that have been enabled at configuration as sources for the interrupt. See Status Register Bits for bit-field details.
- **SPIM_RX_INIT_INTERRUPTS_MASK** – Defines the initial configuration of the interrupt sources chosen in the Configure dialog. This is a mask of the bits in the Rx status register that have been enabled at configuration as sources for the interrupt. See Status Register Bits for bit-field details.

Status Register Bits

SPIM_TXSTATUS

Bits	7	6	5	4	3	2	1	0
Value	Interrupt	Unused	Unused	SPI IDLE	Byte/Word Complete	Tx FIFO Not Full	Tx FIFO. Empty	SPI Done

SPIM_RXSTATUS

Bits	7	6	5	4	3	2	1	0
Value	Interrupt	Rx Buf. Overrun	Rx FIFO Not Empty	Rx FIFO Full	Unused	Unused	Unused	Unused

- Byte/Word Complete: Set when a byte/word of data has been transmitted.
- Rx FIFO Overrun: Set when Rx Data has overrun the 4-byte/word FIFO without being moved to the Rx buffer memory array (if one exists)
- Rx FIFO Not Empty: Set when the Rx Data FIFO is not empty. That is, at least one byte/word is in the Rx FIFO (does not indicate the Rx buffer RAM array conditions).

- Rx FIFO Full: Set when the Rx Data FIFO is full (does not indicate the Rx buffer RAM array conditions).
- Tx FIFO Not Full: Set when the Tx Data FIFO is not full (does not indicate the Tx buffer RAM array conditions).
- Tx FIFO Empty: Set when the Tx Data FIFO is empty (does not indicate the Tx buffer RAM array conditions).
- SPI Done: Set when all of the data in the transmit FIFO has been sent. This may be used to signal a transfer complete instead of using the byte/word complete status. (Set when Byte/Word Complete has been set and Tx Data FIFO is empty.)
- SPI IDLE: Set when the SPI Master state machine is in the IDLE State. This is the default state after the component starts. It is also the next state after SPI Done. IDLE is still set until Tx FIFO Not Empty status has been detected.

SPIM_TXBUFFERSIZE

Defines the amount of memory to allocate for the Tx memory array buffer. This does not include the four bytes/words included in the FIFO. If this value is greater than 4, interrupts are implemented that automatically move data to the FIFO from the circular memory buffer.

SPIM_RXBUFFERSIZE

Defines the amount of memory to allocate for the Rx memory array buffer. This does not include the four bytes/words included in the FIFO. If this value is greater than 4, interrupts are implemented that automatically move data from the FIFO to the circular memory buffer.

SPIM_DATAWIDTH

Defines the number of bits per data transfer chosen in the Configure dialog.

Sample Firmware Source Code

PSoC Creator provides many example projects that include schematics and example code in the Find Example Project dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or File menu. As needed, use the Filter Options in the dialog to narrow the list of projects available to select.

Refer to the “Find Example Project” topic in the PSoC Creator Help for more information.

Functional Description

Default Configuration

The default configuration for the SPI Master is as an 8-bit SPI master with Mode 0 configuration. By default, the internal clock is selected with a bit rate of 1 Mbps.

Modes

The following four waveforms show the component's status bits and the signal values that they assume during data transmission. They are based on the assumption that five data bytes are transmitted (four bytes are written to the SPI Master's Tx buffer at the beginning of transmission and the fifth is thrown after the first byte has been loaded into the A0 register). The numbers in circles on the waveforms represent the following events:

1 – Tx FIFO Empty is cleared when four bytes are written to the Tx buffer.

2 – Tx FIFO Not Full is cleared because Tx FIFO is full after four bytes are written.

3 – SPI IDLE state bit is cleared because of bytes detected in the Tx buffer.

4 – Tx FIFO Not Full status is set when the first byte has been loaded into the A0 register and cleared after the fifth byte has been written to the empty place in the Tx buffer.

5 – Slave Select line is set low, indicating beginning of the transmission.

6 – Tx FIFO Not Full status is set when the second bit is loaded to the A0. Rx Not Empty status is set when the first received byte is loaded into the Rx buffer. Byte/Word Complete is also set.

7 – Tx FIFO Empty status is set at the moment that the last byte to be sent is loaded into the A0 register (to simplify, this is not shown in detail).

8 – At the moment the fourth byte is received, Rx FIFO Full is set along with Byte/Word Complete.

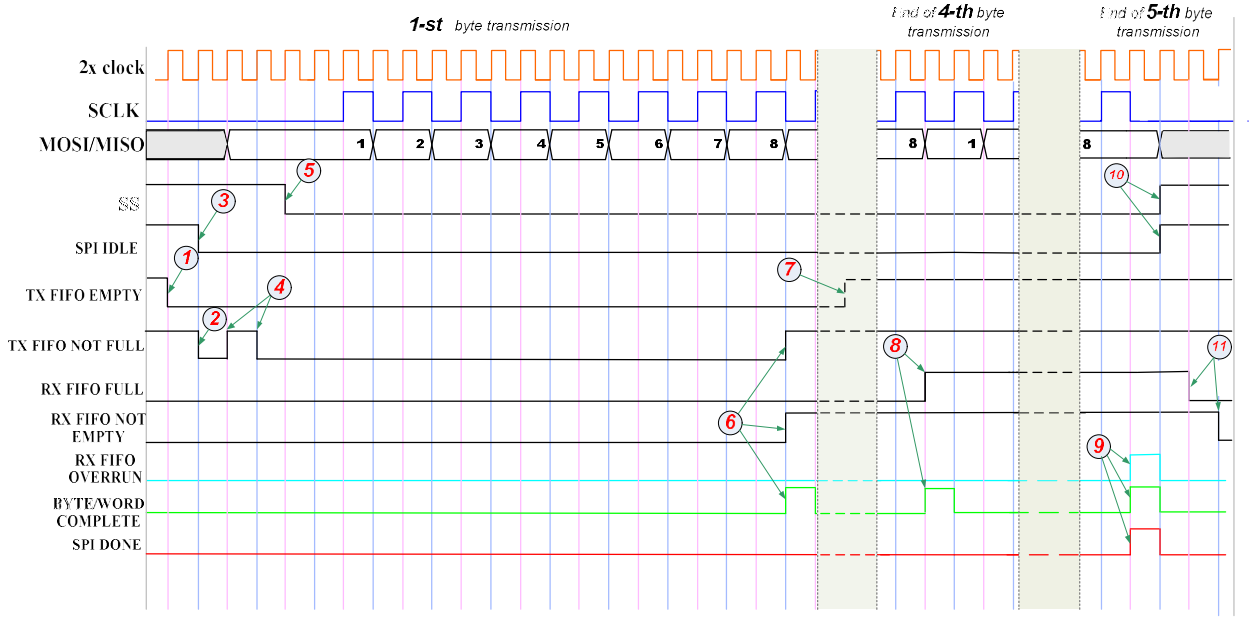
9 – Byte/Word Complete, SPI Done, and Rx Overrun are set because all bytes have been transmitted and an attempt to load data into the full Rx buffer has been detected.

10 – SS line is set high to indicate that transmission is complete. SPI IDLE state is also set.

11 – Rx FIFO Full is cleared when the first byte has been read from the Rx buffer and Rx FIFO Empty is set when all of them have been read.

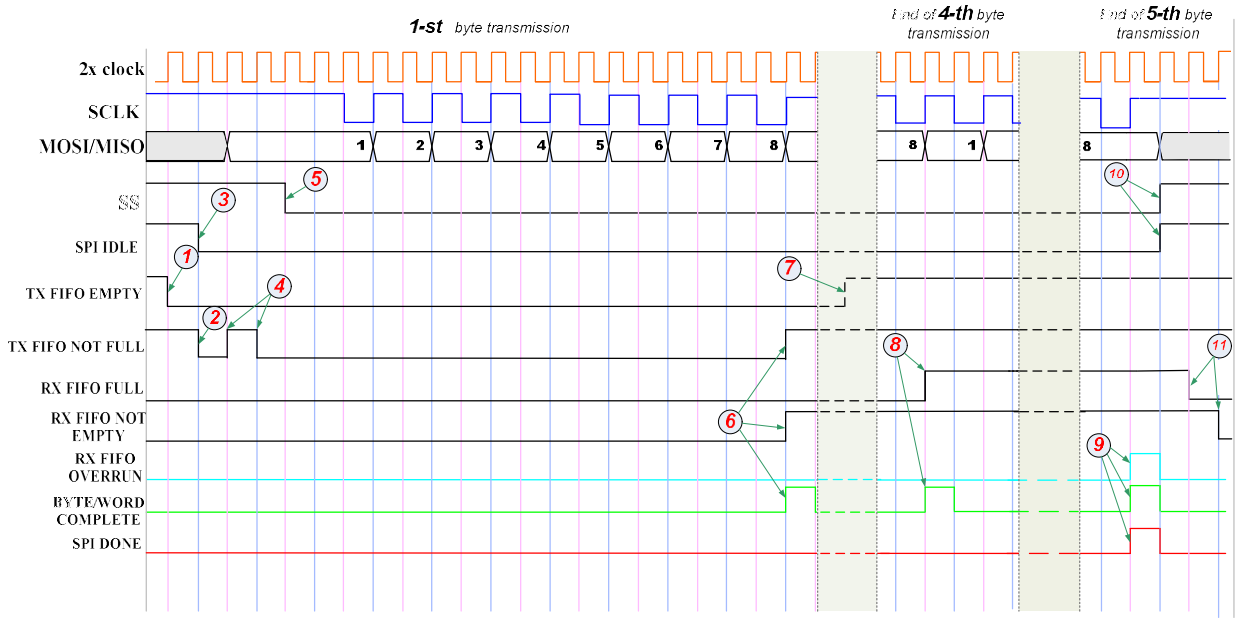
SPI Master Mode: 0 (CPHA == 0, CPOL == 0)

Mode 0 has the following characteristics:



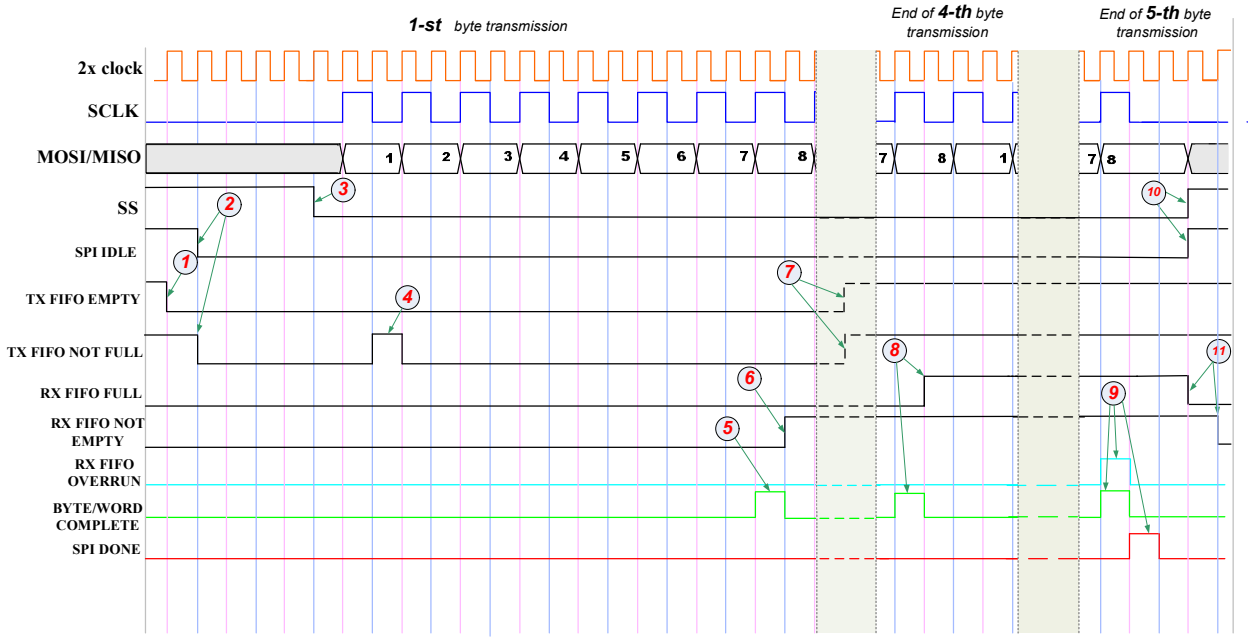
SPI Master Mode: 1 (CPHA == 0, CPOL == 1)

Mode 1 has the following characteristics:



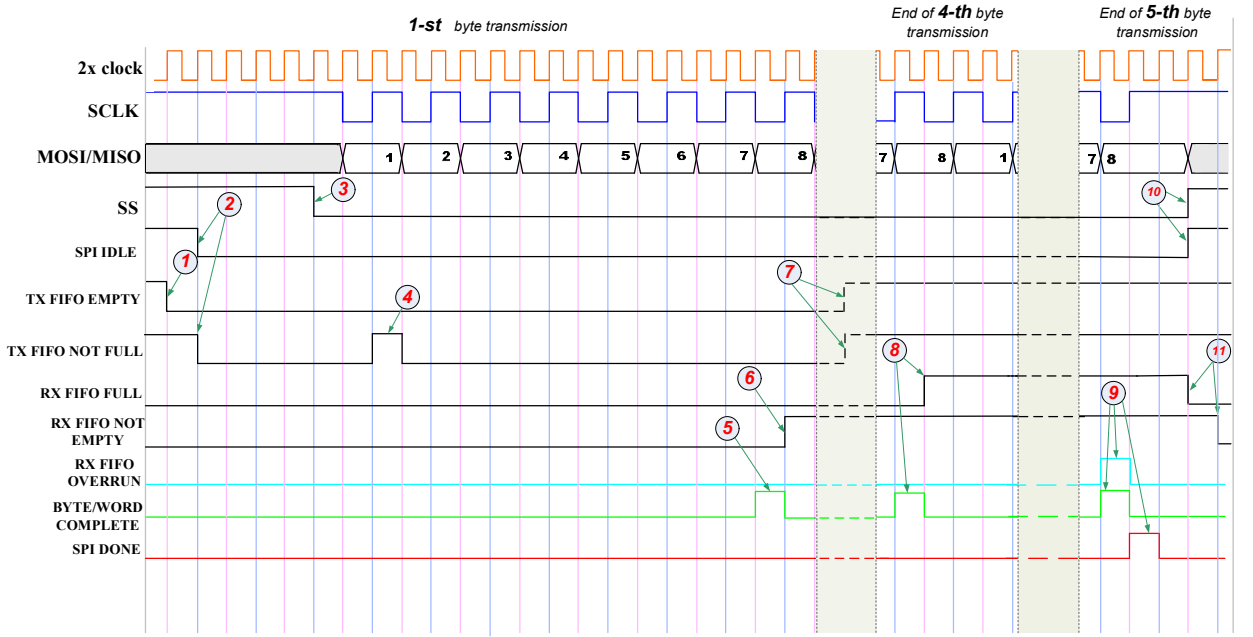
SPI Master Mode: 2 (CPHA == 1, CPOL == 0)

Mode 2 has the following characteristics:



SPI Master Mode: 3 (CPHA == 1, CPOL == 1)

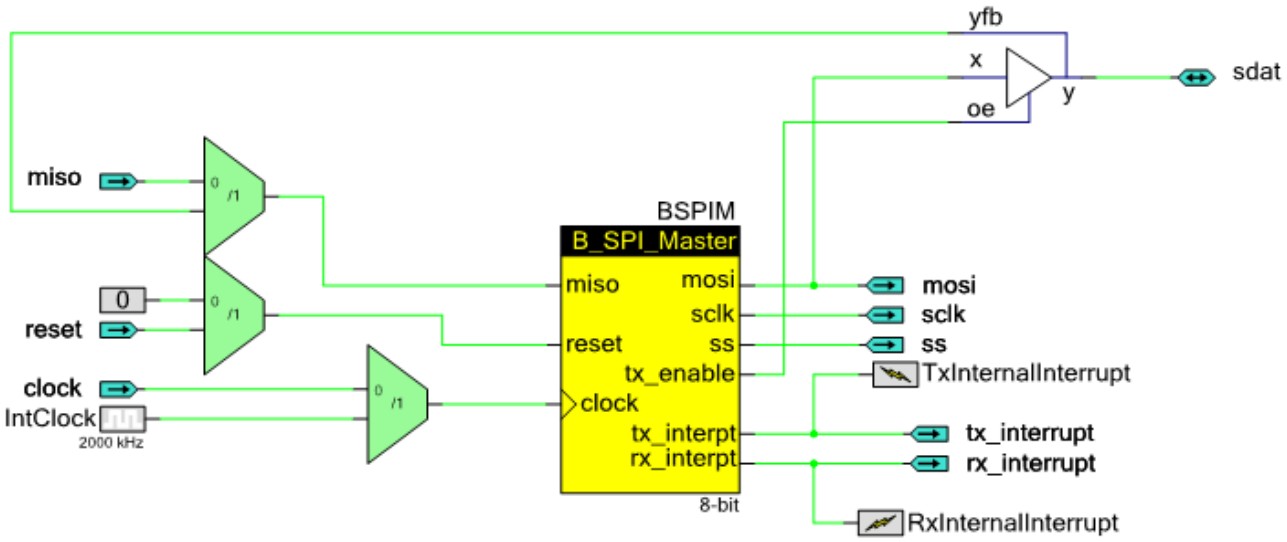
Mode 3 has the following characteristics:



Block Diagram and Configuration

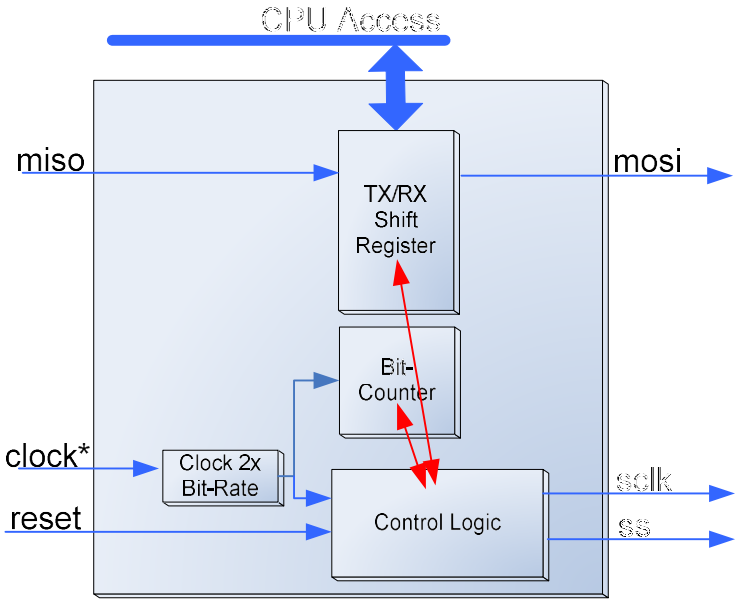
The SPI Master is only available as a UDB configuration. The registers are described here to define the hardware implementation of the SPI Master.

Figure 8. SPI Master Schematic



The implementation is described in Figure 9.

Figure 9. SPI Master Block Diagram



Registers

Tx Status Register

The Tx status register is a read-only register that contains the various transmit status bits defined for a given instance of the SPI Master component. Assuming that an instance of the SPI Master is named “SPIM,” you can get the value of this register using the SPIM_ReadTxStatus() function.

The interrupt output signal is generated by ORing the masked bit fields within the Tx status register. You can set the mask using the SPIM_SetTxInterruptMode() function. Upon receiving an interrupt, you can retrieve the interrupt source by reading the Tx status register with the SPIM_ReadTxStatus () function.

Sticky bits in the Tx status register are cleared on reading, so the interrupt source is held until the SPIM_ReadTxStatus() function is called. All operations on the Tx status register must use the following defines for the bit fields, because these bit fields may be moved within the Tx status register at build time. Sticky bits used to generate an interrupt or DMA transaction must be cleared with either a CPU or DMA read to avoid continuously generating the interrupt or DMA.

There are several bit fields defined for the Tx status registers. Any combination of these bit fields may be included as an interrupt source. The bit fields indicated with an asterisk (*) in the following list are configured as sticky bits in the Tx status register. All other bits are configured as real-time indicators of status. Sticky bits latch a momentary state so that they may be read at a later time and cleared on read. The following #defines are available in the generated header file (for example, *SPIM.h*):

- SPIM_STS_SPI_DONE * – This bit is set high as the data-latching edge of SCLK (edge is mode dependent) is output. This happens after the last bit of the configured number of bits in a single SPI word is output onto the MOSI line and the transmit FIFO is empty. It is cleared when the SPI Master is transmitting data or the transmit FIFO has pending data. It tells you when the SPI Master has completed a multiword transaction.
- SPIM_STS_TX_FIFO_EMPTY – This bit reads high while the transmit FIFO contains no data pending transmission. It reads low if data is waiting for transmission.
- SPIM_STS_TX_FIFO_NOT_FULL – This bit reads high while the transmit FIFO is not full and has room to write more data. It reads low if the FIFO is full of data pending transmit and there is no room for more writes at this time. It tells you when it is safe to pend more data into the transmit FIFO.
- SPIM_STS_BYTE_COMPLETE * – This bit is set high as the last bit of the configured number of bits in a single SPI word is output onto the MOSI line. It is cleared* as the data latching edge of SCLK (edge is mode dependent) is output.
- SPIM_STS_SPI_IDLE * – This bit is set high as long as the component state machine is in the SPI IDLE state (component is waiting for Tx data and is not transmitting any data).

RX Status Register

The Rx status register is a read-only register that contains the various receive status bits defined for the SPI Master. You can get the value of this register using the SPIM_ReadRxStatus() function.

The interrupt output signal is generated by ORing the masked bit fields within the Rx status register. You can set the mask using the SPIM_SetRxInterruptMode() function. Upon receiving an interrupt, you can retrieve the interrupt source by reading the Rx status register with the SPIM_ReadRxStatus () function.

Sticky bits in the Rx status register are cleared on reading, so the interrupt source is held until the SPIM_ReadRxStatus() function is called. All operations on the Rx status register must use the following defines for the bit fields, because these bit fields may be moved within the Rx status register at build time. Sticky bits used to generate an interrupt or DMA transaction must be cleared with either a CPU or DMA read to avoid continuously generating the interrupt or DMA.

There are several bit fields defined for the Rx status register. Any combination of these bit fields can be included as an interrupt source. The bit fields indicated with an asterisk (*) in the following list are configured as sticky bits in the Rx status register. All other bits are configured as real-time indicators of status. Sticky bits latch a momentary state so that they may be read at a later time and cleared when read. The following #defines are available in the generated header file (for example, *SPIM.h*):

- SPIM_STS_RX_FIFO_FULL – This bit reads high when the receive FIFO is full and has no more room to store received data. It reads low if the FIFO is not full and has room for additional received data and tells you if there is room for new received data to be stored.
- SPIM_STS_RX_FIFO_NOT_EMPTY – This bit reads high when the receive FIFO is not empty. It reads low if the FIFO is empty and has room for additional received data.
- SPIM_STS_RX_FIFO_OVERRUN * – This bit reads high when the receive FIFO is already full and additional data was written to it. It tells you if data has been lost from the FIFO because of slow FIFO servicing.

Tx Data Register

The Tx data register contains the transmit data value to send. This is implemented as a FIFO in the SPI Master. There is an optional higher-level software state machine that controls data from the transmit memory buffer. It handles large amounts of data to be sent that exceed the FIFO's capacity. All APIs that involve transmitting data must go through this register to place the data onto the bus. If there is data in this register and the control state machine indicates that data can be sent, then the data is transmitted on the bus. As soon as this register (FIFO) is empty, no more data will be transmitted on the bus until it is added to the FIFO. DMA can be set up to fill this FIFO when empty, using the TXDATA_REG address defined in the header file.

Rx Data Register

The Rx data register contains the received data. This is implemented as a FIFO in the SPI Master. There is an optional higher-level software state machine that controls data movement from this receive FIFO into the memory buffer. Typically, the Rx interrupt indicates that data has been received. At that time, that data has several routes to the firmware. DMA can be set up from this register to the memory array, or the firmware can call the SPIM_ReadRxData() function. DMA must use the RXDATA_REG address defined in the header file.

Conditional Compilation Information

The SPI Master requires only one conditional compile definition to handle the 8- or 16-bit datapath configuration necessary to implement the configured NumberOfDataBits. The API must conditionally compile for the data width defined. APIs should never use these parameters directly but should use the following define:

- SPIM_DATAWIDTH – This defines how many data bits will make up a single “byte” transfer. Valid range is 3 to 16 bits.

DC and AC Electrical Characteristics

The following values indicate expected performance and are based on initial characterization data.

Timing Characteristics "Maximum with Nominal Routing"

Parameter	Description	Config	Min	Typ	Max [1]	Units
f_{SCLK}	SCLK frequency	Config 1 [2]			9	MHz
		Config 2 [3]			9	MHz
		Config 3 [4]			8	MHz
		Config 4 [5]			8	MHz
		Config 5 [6]			18	MHz
		Config 6 [7]			18	MHz

[1] The maximum component clock frequency is derived from t_{SCLK_MISO} in combination with the routing path delays of the SCLK input and the MISO output (described later in this document). These "Nominal" numbers provide a maximum safe operating frequency of the component under nominal routing conditions. It is possible to run the component at higher clock frequencies, at which point you will need to validate the timing requirements with STA results.

[2] Config 1 options:
Data Lines: MOSI+MISO
Data Bits: 8
Standard Mode

[3] Config 2 options:
Data Lines: MOSI+MISO
Data Bits: 16
Standard Mode

[4] Config 3 options:
Data Lines: Bidirectional
Data Bits: 8
Standard Mode

[5] Config 4 options:
Data Lines: Bidirectional
Data Bits: 16
Standard Mode

[6] Config 5 options:
Data Lines: MOSI+MISO
Data Bits: 8
High Speed Mode

[7] Config 6 options:
Data Lines: MOSI+MISO
Data Bits: 16
High Speed Mode

Parameter	Description	Config	Min	Typ	Max [1]	Units
		Config 7 [8]			16	MHz
		Config 8 [9]			16	MHz
f_{CLOCK}	Component clock frequency [10]	Config 1 [2]	2 × f_{SCLK}		18	MHz
		Config 2 [3]	2 × f_{SCLK}		18	MHz
		Config 3 [4]	2 × f_{SCLK}		16	MHz
		Config 4 [5]	2 × f_{SCLK}		16	MHz
		Config 5 [6]	2 × f_{SCLK}		36	MHz
		Config 6 [7]	2 × f_{SCLK}		36	MHz
		Config 7 [8]	2 × f_{SCLK}		32	MHz
		Config 8 [9]	2 × f_{SCLK}		32	MHz
t_{CKH}	SCLK high time			0.5		$1/f_{SCLK}$
t_{CKL}	SCLK low time			0.5		$1/f_{SCLK}$
t_{S_MISO}	MISO input setup time		25			ns
t_{H_MISO}	MISO input hold time			0		ns
t_{SS_SCLK}	SS active to SCLK active		-20		20	ns
t_{SCLK_SS}	SCLK inactive to SS inactive		-20		20	ns

[8] Config 7 options:
Data Lines: Bidirectional
Data Bits: 8
High Speed Mode

[9] Config 8 options:
Data Lines: Bidirectional
Data Bits: 16
High Speed Mode

[10] Component clock is equal to the bit rate × 2. It is also used to clock the status registers. Routing may limit the maximum frequency of this parameter; therefore, the maximum is listed with nominal routing results.

Timing Characteristics "Maximum with All Routing"

Parameter	Description	Config	Min	Typ	Max [12]	Units
f_{SCLK}	SCLK frequency (is always equal to one-half of the f_{CLOCK})	Config 1 [13]			4.5	MHz
		Config 2 [14]			4.5	MHz
		Config 3 [15]			4	MHz
		Config 4 [16]			4	MHz
		Config 5 [17]			9	MHz
		Config 6 [18]			9	MHz
		Config 7 [19]			8	MHz
		Config 8 [20]			8	MHz

[12] The Maximum for All Routing timing numbers are calculated by derating the Nominal Routing timing numbers by a factor of 2. If your component instance operates at or below these speeds, then meeting timing should not be a concern for this component.

[13] Config 1 options:
Data Lines: MOSI+MISO
Data Bits: 8
Standard Mode

[14] Config 2 options:
Data Lines: MOSI+MISO
Data Bits: 16
Standard Mode

[15] Config 3 options:
Data Lines: Bidirectional
Data Bits: 8
Standard Mode

[16] Config 4 options:
Data Lines: Bidirectional
Data Bits: 16
Standard Mode

[17] Config 5 options:
Data Lines: MOSI+MISO
Data Bits: 8
High Speed Mode

[18] Config 6 options:
Data Lines: MOSI+MISO
Data Bits: 16
High Speed Mode

[19] Config 7 options:
Data Lines: Bidirectional
Data Bits: 8
High Speed Mode

[20] Config 8 options:
Data Lines: Bidirectional
Data Bits: 16
High Speed Mode

Parameter	Description	Config	Min	Typ	Max [12]	Units
f_{CLOCK}	Component clock frequency[21]	Config 1 [13]		2 × f_{SCLK}	9	MHz
		Config 2 [14]		2 × f_{SCLK}	9	MHz
		Config 3 [15]		2 × f_{SCLK}	8	MHz
		Config 4 [16]		2 × f_{SCLK}	8	MHz
		Config 5 [17]		2 × f_{SCLK}	18	MHz
		Config 6 [18]		2 × f_{SCLK}	18	MHz
		Config 7 [19]		2 × f_{SCLK}	16	MHz
		Config 8 [20]		2 × f_{SCLK}	16	MHz
t_{CKH}	SCLK high time			0.5		$1/f_{SCLK}$
t_{CKL}	SCLK low time			0.5		$1/f_{SCLK}$
t_{S_MISO}	MISO input setup time		25			ns
t_{H_MISO}	MISO input hold Time			0		ns
t_{SS_SCLK}	SS active to SCLK active		–20		20	ns
t_{SCLK_SS}	SCLK inactive to SS inactive		–20		20	ns

[21] Component clock is equal to the bit rate × 2. It is also used to clock the status registers. Routing may limit the maximum frequency of this parameter; therefore, the maximum is listed with nominal routing results.

Figure 10. Mode CPHA = 0 Timing Diagram

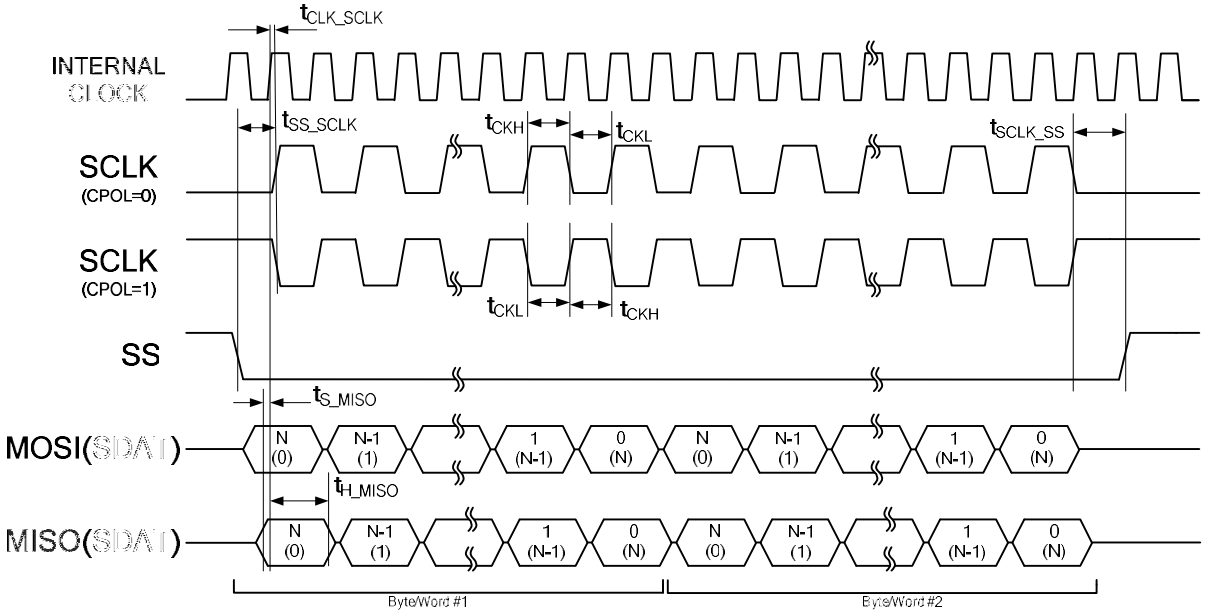
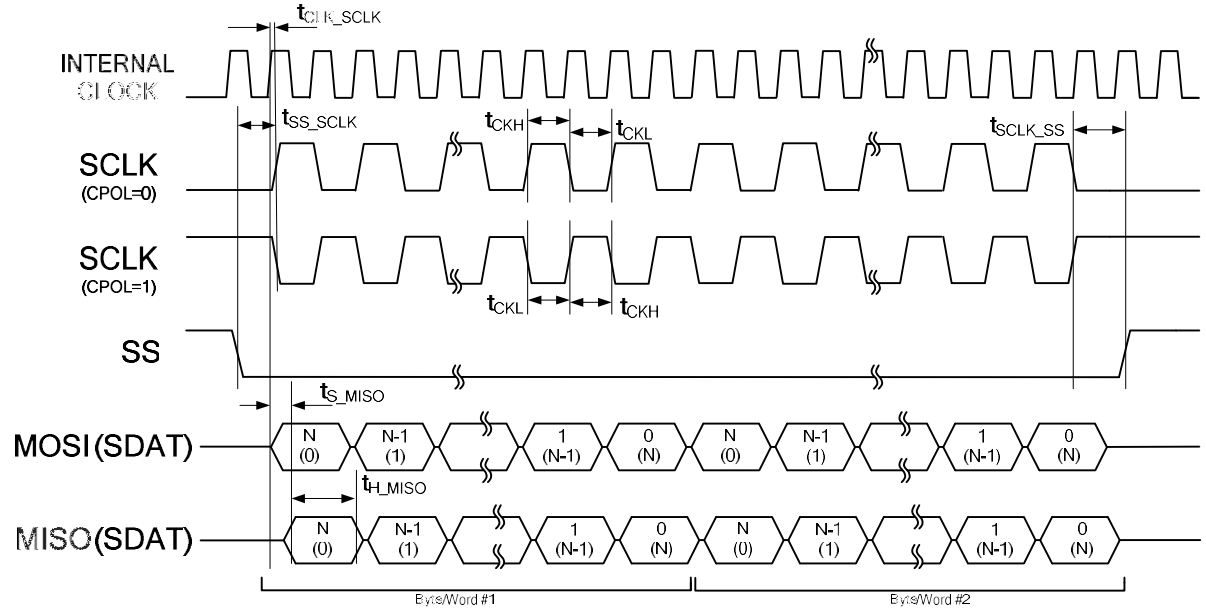


Figure 11. Mode CPHA = 1 Timing Diagram

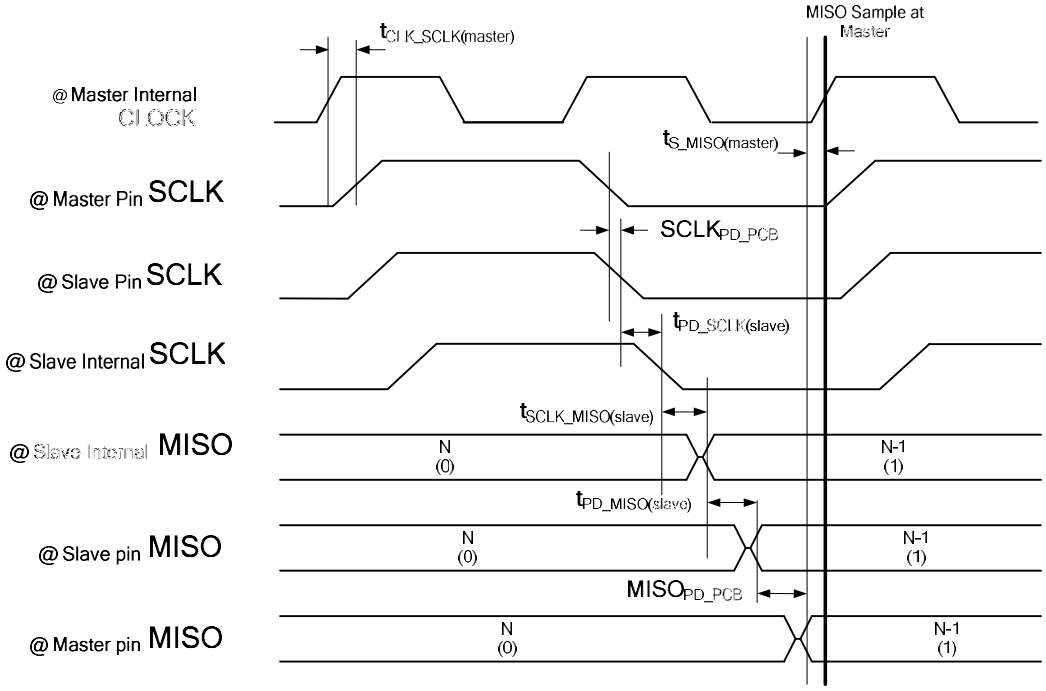


How to Use STA Results for Characteristics Data

Nominal route maximums are gathered through multiple test passes with Static Timing Analysis (STA). You can calculate the maximums for your designs with the STA results using the following mechanisms:

f_{SCLK} The maximum frequency of SCLK (or the maximum bit rate) is not provided directly in the STA. However, the data provided in the STA results indicates some of the internal logic timing constraints. To calculate the maximum bit rate, you must consider several factors. You will need board-layout and slave-communication device specs to fully understand the maximum. The main limiting factor in this parameter is the round-trip path delay from the falling edge of SCLK at the pin of the master, to the slave and the path delay of the MISO output of the slave, back to the master.

Figure 12 Calculating Maximum f_{SCLK} Frequency



In this case, the component must meet the setup time of MISO at the master using the following equation:

$$t_{RT\_PD} < 1 / \{ [½ \times f_{SCLK}] - t_{CLK\_SCLK(master)} - t_{S\_MISO(master)} \}$$

-- OR --

$$f_{SCLK} < 1 / \{2 * [T_{RT\_PD} + t_{CLK\_SCLK(master)} + t_{S\_MISO(master)}] \}$$

Where:

$t_{CLK\_SCLK(master)}$ is the path delay of the input CLK to the SCLK output. This is provided in the STA results clock to output section as shown in the following example:

- **Clock To Output Section**

  - **SPIM_1_IntClock**

Source	Destination	Delay (ns)
Net_25/q	SCLK_1(0)_PAD	24.800

$t_{S\_MISO(Master)}$ is the path delay from MISO input pin to internal logic of the master component. This is provided in the STA results input to clock section as shown in the following example:

- **Input To Clock Section**

  - **SPIM_1_IntClock**

Source	Destination	Delay (ns)
MISO_1(0)_PAD	\SPIM_1:BSPIM:sR8:Dp:u0\/route_si	20.906

For High Speed mode, the setup time equation looks like the following:

$t_{RT\_PD} < 1 / \{ [f_{SCLK}] - t_{CLK\_SCLK(master)} - t_{S\_MISO(master)}\}$

-- OR --

$f_{SCLK} < 1 / \{ [T_{RT\_PD} + t_{CLK\_SCLK(master)} + t_{S\_MISO(master)}] \}$

Note There are two values in the report: setup times to the component clock at register A0 and register A1. Select the larger one for calculation.

t_{RT_PD} is defined as:

$t_{RT\_PD} = [SCLK_{PD\_PCB} + t_{PD\_SCLK(slave)} + t_{SCLK\_MISO(slave)} + t_{PD\_MISO(slave)} + MISO_{PD\_PCB}]$

and:

$SCLK_{PD\_PCB}$ is the PCB path delay of SCLK from the pin of the master component to the pin of the slave component.

$t_{PD\_SCLK(slave)} + t_{SCLK\_MISO(slave)} + t_{PD\_MISO(slave)}$ must come from the slave device datasheet. $MISO_{PD\_PCB}$ is the PCB path delay of MISO from the pin of the slave component to the pin of the master component.

The final equation that provides the maximum frequency of SCLK, and therefore the maximum bit rate, is:

f_{SCLK} (Max.) $= 1 / \{2 \times [t_{CLK\_SCLK(master)} + SCLK_{PD\_PCB} + t_{PD\_SCLK(slave)} + t_{SCLK\_MISO(slave)} + t_{PD\_MISO(slave)} + MISO_{PD\_PCB} + t_{S\_MISO(master)}] \}$

For High Speed mode:

f_{SCLK} (Max.) $= 1 / \{ [t_{CLK\_SCLK(master)} + SCLK_{PD\_PCB} + t_{PD\_SCLK(slave)} + t_{SCLK\_MISO(slave)} + t_{PD\_MISO(slave)} + MISO_{PD\_PCB} + t_{S\_MISO(master)}] \}$

f_{CLOCK} Maximum component clock frequency is provided in Timing results in the clock summary as the IntClock (if internal clock is selected) or the named external clock. An example of the internal clock limitations from the STA report file follows:

- **Clock Summary Section**

Clock	Type	Nominal Frequency (MHz)	Required Frequency (MHz)	Maximum Frequency (MHz)	Violation
BUS_CLK	Sync	60.000	60.000	N/A	
ClockBlock/clk_bus	Async	60.000	60.000	N/A	
ClockBlock/dclk_0	Async	15.000	15.000	N/A	
ILO	Async	0.001	0.001	N/A	
IMO	Async	3.000	3.000	N/A	
MASTER_CLK	Sync	60.000	60.000	N/A	
PLL_OUT	Async	60.000	60.000	N/A	
SPIM_1_IntClock	Sync	15.000	15.000	61.870	

Its value is limited to either 2x of the f_{CLOCK} or by the number from the STA report, but in practice the limitation is 2x of the f_{CLOCK}.

t_{CKH} The SPI Master component generates a 50-percent duty cycle SCLK.

t_{CKL} The SPI Master component generates a 50-percent duty cycle SCLK.

t_{CLK_SCLK} Internal clock to SCLK output time. Time from posedge of Internal Clock to SCLK available on master pin.

t_{S_MISO} To meet the setup time of the internal logic, MISO must be valid at the pin, before Internal clock is valid at the pin, by this amount of time.

t_{H_MISO} To meet the hold time of the internal logic, MISO must be valid at the pin, after Internal clock is valid at the pin, by this amount of time.

t_{SS_SCLK} To meet the internal functionality of the block, Slave Select (SS) must be valid at the pin before SCLK is valid at the pin, by this parameter.

t_{SCLK_SS} Maximum - To meet the internal functionality of the block. Slave Select (SS) must be valid at the pin after the last falling edge of SCLK at the pin, by this parameter.

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
2.21	Added High Speed Mode functionality. Fixed SPI Modes diagrams.	Verilog implementation is updated to allow maximum bit rate up to 18 Mbps. Added details to description of Bidirectional Mode. SPI Modes diagrams changed to hide Rx data as internal implementation details. Description of High Speed Mode is added to “Advanced Tab” section. “Resources”, “AC and DC electrical Characteristics” and “How to use STA results for Characteristics data” sections are updated with data related to High Speed Mode.

Version	Description of Changes	Reason for Changes / Impact
2.20	Updated Internal clock component with cy_clock_v1_60. Fixed verilog defect that caused STA warning.	Clock v1_60 is the latest component version. Verilog defect fixed to remove STA warning founded using the updated STA tool. Screenshots in “AC and DC electrical characteristics” section are updated by report generated by the new STA tool.
2.10.a	Datasheet corrections (Mode 2 and Mode 3 diagram corrected)	Datasheet defects fixed
2.10	Changed Data Bits range is changed from 2 to 16 bits to 3 to 16.	Changes related to status synchronization issues fixed in current version.
	Added the “Interrupt on SPI Idle” checkbox to the component configure dialog.	Component customizer defect fixed
	Changed the “Byte transfer complete” checkbox name to the “Byte/Word transfer complete”	To fit the real meaning
	Added characterization data to datasheet	
	Minor datasheet edits and updates	
2.0.a	Moved component into subfolders of the component catalog.	
2.0	Added SPIM_Sleep()/SPIM_Wakeup() and SPIM_Init()/SPIM_Enable APIs.	To support low-power modes, and to provide common interfaces to separate control of initialization and enabling of most components.
	Changed the number and positions of component I/Os: ▪ The clock input is now visible in default placement (external clock source is the default setting now) ▪ The reset input has a different position ▪ The interrupt output was removed. rx_interrupt, tx_interrupt outputs are added instead.	The clock input was added for consistency with SPI Slave. The reset input place changed because the clock input was added. Two status interrupt registers (Tx and Rx) are now presented instead of one shared. These changes must be taken into account to prevent binding errors when migrating from previous SPI versions
	Removed SPIM_EnableInt(), SPIM_DisableInt(), SPIM_SetInterruptMode(), and SPIM_ReadStatus() APIs. Added SPIM_EnableTxInt(), SPIM_EnableRxInt(), SPIM_DisableTxInt(), SPIM_DisableRxInt(), SPIM_SetTxInterruptMode(), SPIM_SetRxInterruptMode(), SPIM_ReadTxStatus(), SPIM_ReadRxStatus() APIs.	The removed APIs are obsolete because the component now contains Rx and Tx interrupts instead of one shared interrupt. Also updated the interrupt handler implementation for Tx and Rx Buffer.
	Renamed SPIM_ReadByte(), SPIM_WriteByte()APIs to SPIM_ReadRxData(), SPIM_WriteTxData().	Clarifies the APIs and how they should be used.

Version	Description of Changes	Reason for Changes / Impact
The following changes were made to the base SPI Master component B_SPI_Master_v2_0, which is implemented using Verilog:		
	spim_ctrl internal module was replaced by a new state machine.	It uses fewer hardware resources and does not contain any asynchronous logic.

	Two status registers are now presented (status are separate for Tx and Rx) instead of using one common status register for both.
	`/*SPI_Master_v1_20 status bits*/`
	`SPIM_STS_SPI_DONE_BIT = 3'd0;`
	`SPIM_STS_TX_FIFO_EMPTY_BIT = 3'd1;`
	`SPIM_STS_TX_FIFO_NOT_FULL_BIT = 3'd2;`
	`SPIM_STS_RX_FIFO_FULL_BIT = 3'd3;`
	`SPIM_STS_RX_FIFO_NOT_EMPTY_BIT = 3'd4;`
	`SPIM_STS_RX_FIFO_OVERRUN_BIT = 3'd5;`
	`SPIM_STS_BYTE_COMPLETE_BIT = 3'd6;`
	
	`/*SPI_Master_v2_0 status bits*/`
	`localparam SPIM_STS_SPI_DONE_BIT = 3'd0;`
	`localparam SPIM_STS_TX_FIFO_EMPTY_BIT = 3'd1;`
	`localparam SPIM_STS_TX_FIFO_NOT_FULL_BIT = 3'd2;`
	`localparam SPIM_STS_BYTE_COMPLETE_BIT = 3'd3;`
	`localparam SPIM_STS_SPI_IDLE_BIT = 3'd4;`
	`localparam SPIM_STS_RX_FIFO_FULL_BIT = 3'd4;`
	`localparam SPIM_STS_RX_FIFO_NOT_EMPTY_BIT = 3'd5;`
	`localparam SPIM_STS_RX_FIFO_OVERRUN_BIT = 3'd6;`
		Fixed a defect found in previous versions of the component where software buffers were not working as expected.

	Added ‘BidirectMode’ boolean parameter to the base component. Control Register with ‘clock’ input and SYNC mode bit is now selected to drive ‘tx_enable’ output for PSoC 3 Production silicon. Control Register w/o clock input drives ‘tx_enable’ when ES2 silicon is selected. Bufoe component is used on component schematic to support Bidirectional Mode. MOSI output of base component is connected to bufoe ‘x’ input. ‘yfb’ is connected to 'miso' input. Bufoe ‘y’ output is connected to 'sdat' output terminal. Routed reset is connected to datapaths, Counter7 and State Machine.	Added Bidirectional Mode support to the component

Version	Description of Changes	Reason for Changes / Impact
	Added udb_clock_enable component to Verilog implementation with sync = `TRUE` parameter.	New requirements for all clocks used in Verilog to indicate functionality so the tool can support synchronization and Static Timing Analysis.
	'*2' is replaced by '<< 1' in Counter7 period value.	Verilog improvements.
	Maximum Bit Rate value is changed to 10 Mbps	Bit Rate value more than 10 Mbps is not supported (verified during the component characterization)
	Added a description of the Bidirectional Mode	Data sheet defect fixed
	Reset input description now contains the note about ES2 silicon incompatibility	Data sheet defect fixed
	Changed timing correlation diagram between SS and SCLK signals is changed	Data sheet defect fixed
	Removed sample firmware source code	Added reference to the component example project instead
	SPI Modes diagrams are changed (Tx and Rx FIFO status values are added)	Data sheet defect fixed