



PSoC 4 Operational Amplifier (Opamp)

Features

- Follower or Opamp configuration
- Rail-to-rail inputs and output
- Output direct low resistance connection to pin
- 1mA or 10mA output current
- Internal connection for follower

General Description

The Opamp operates as an off-the-shelf operation amplifier. A direct connection is made between the Opamp output to a GPIO pin for a low output resistance. Two output modes (Internal only and Output to pin) are provided to drive internal or external signals respectively. The Output to pin may drive both internal (SAR component) and external signals. The user also has control of different overall power levels that provide a tradeoff between power and bandwidth.

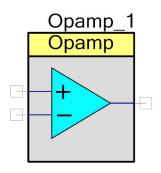
For PSoC 4200 BLE devices the Comparator can operate in the Deep Sleep power mode.

Note External resistors are required to perform amplification.

When to Use the Opamp

The following is a list of common use cases for the Opamp component:

- Gain for SAR ADC
- High impedance buffer for SAR ADC
- General purpose signal amplifier
- Active filter



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Input/Output Connections

This section describes various input and output connections for the Opamp.

Positive Input – Analog Input

When the Opamp is configured in follower Mode, this I/O is the voltage input. If the Opamp is configured in Opamp Mode, this I/O acts as the standard Opamp noninverting input.

Negative Input – Analog Input*

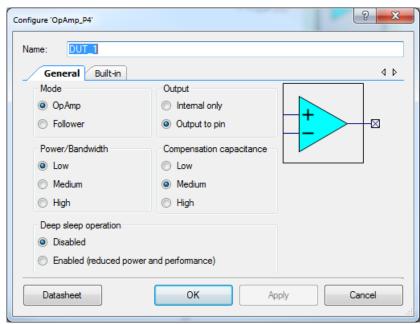
When the Opamp component is configured in Opamp Mode, this I/O is the normal inverting input. When the Opamp is configured in Follower Mode, this I/O is hard-connected to the output and the I/O is unavailable.

Vout – Analog output

The output can be directly connected to a pin and/or routed to an internal load using the Output parameter. The drive strength is selectable as either Output to pin or Internal only. Connections to pins require the Output to pin setting. Internal connections can operate with either the Internal only or Output to pin setting, but should normally be configured for Internal only.

Component Parameters

Drag Opamp onto your design and double-click it to open the Configure dialog.



The Opamp provides the following parameters:



Mode

This parameter allows you to select between two configurations: **Opamp** and **Follower**. **Opamp** is the default configuration. In this mode, all three terminals are available for connection. In the follower mode, the inverting input is internally connected to the output to create a voltage follower.

Power/Bandwidth

The Opamp works over a wide range of operating currents. Higher operating current increases the Opamp bandwidth. The **Power/Bandwidth** parameter allows you to select the power level: High, Medium, and Low.

Output

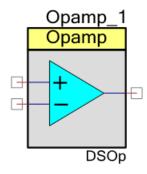
This parameter selects an output mode: Internal only – internal connections or Output to pin – connection to pin (external).

Compensation

The opamp offers three compensation settings: Low, Med and High. This allows reducing the compensation (hence increase the bandwidth) when the Opamp's loop gain is reduced.

Deep sleep operation

This parameter is available for PSoC 4200 BLE devices only. It enables the component operation in Deep Sleep mode. If this option is enabled, a "DSOp" label will be displayed under the symbol.



Note Only dedicated pins may be used for operation in Deep Sleep mode.

Note For correct operation in Deep Sleep mode, the V_{DDA} must be larger than 2.5 V. The boost pump does not operate in Deep Sleep mode.



Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name "Opamp_1" to the first instance of a component in a given design. You can rename it to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "Opamp"

Functions

Function	Description	
Opamp_Start()	Performs all of the required initialization for the component and enables power to the block.	
Opamp_Stop()	Turns off the Opamp block.	
Opamp_Init()	Initializes or restores the component according to the customizer Configure dialog settings.	
Opamp_Enable()	Activates the hardware and begins component operation.	
Opamp_SetPower()	Sets the drive power to one of three settings; LOW_POWER, MED_POWER, HIGH_POWER.	
Opamp_PumpControl()	Turn the boost pump on or off.	
Opamp_Sleep()	This is the preferred API to prepare the component for sleep.	
Opamp_Wakeup()	This is the preferred API to restore the component to the state when Opamp_Sleep() was called.	

void Opamp_Start(void)

Description: Performs all of the required initialization for the component and enables power to the block. The first time the routine is executed, the Power level, Mode, and Output mode is set. When called to restart the Opamp following a Stop() call, the current component parameter settings are retained.

Parameters:	None
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Return Value: None

Side Effects: None



void Opamp_Stop(void)

Description:	Turn off the Opamp block.	
Parameters:	None	
Return Value:	None	
Side Effects:	Does not affect the Opamp mode or power settings	

void Opamp_Init(void)

Description:	Initializes or restores the component according to the customizer Configure dialog settings. It is not necessary to call Init() because the Start() API calls this function and is the preferred method to begin the component operation.
Parameters:	None
Return Value:	None
Side Effects:	All the registers will be set to values according to the customizer Configure dialog.

void Opamp_Enable(void)

Description:	Activates the hardware and begins the component operation. It is not necessary to call		
	Enable() because the Start() API calls this function, which is the preferred method to begin		
	component operation.		

Parameters:NoneReturn Value:None

Side Effects: None

void Opamp_SetPower(uint32 power)

Description: Sets the opamp to one of three power levels..

Parameters: (uint32) power: Power levels. See table below.

Parameter Value	Description
Opamp_LOW_POWER	Lowest active power.
Opamp_MED_POWER	Medium power.
Opamp_HIGH_POWER	Highest active power.

Return Value: None



void Opamp_PumpControl(uint32 onOff)

Description: Allows the user to turn the Opamp's boost pump on or off. By Default the Opamp_Start() function turns on the pump. Use this command to turn it off. The boost must be turned on when the supply is less than 2.7 volts and off if the supply is more than 4 volts.

Parameters: (uint32) onOff: Control the pump. See the table below.

Parameter Value	Description
Opamp_PUMP_OFF	Turn off the pump
Opamp_PUMP_ON	Turn on the pump

Return Value: None

Side Effects: Turning this pump off will reduce the Opamp input range by 1.8 volts or (Vssa to (Vdda – 1.8 volts)).

void Opamp_Sleep(void)

Description:	This is the preferred API to prepare the component for sleep. The Sleep() API saves the current component state. Call the Sleep() function before calling the CySysPmDeepSleep() or the CySysPmHibernate() functions. The "Deep sleep operation" option has an influence on this function implementation.
Parameters:	None
Return Value:	None
Side Effects:	None

void Opamp_Wakeup(void)

Description:	This is the preferred API to restore the component to the state when Sleep() is called. If the
	component has been enabled before the Sleep() function is called, the Wakeup() function
	will also re-enable the component. The "Deep sleep operation" option has an influence on
	this function implementation.

Parameters: None

Return Value: None

Side Effects: Calling the Wakeup() function without first calling the Sleep() function may produce unexpected behavior.



Sample Firmware Source Code

PSoC Creator provides numerous example projects that include schematics and example code in the Find Example Project dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or **File** menu. As needed, use the **Filter Options** in the dialog to narrow the list of projects available to select.

Refer to the "Find Example Project" topic in the PSoC Creator Help for more information.

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined:

- project deviations deviations that are applicable for all PSoC Creator components
- specific deviations deviations that are applicable only for this component

This section provides information on the component-specific deviations. The project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The Opamp component has the following specific deviations:

MISRA-C: 2004 Rule	Rule Class (Required/Advisory)	Rule Description	Description of Deviation(s)
19.7	Δ	A function is used in preference to a function-like macro.	Deviated since function-like macros are used to allow more efficient code.

API Memory Usage

The component memory usage varies significantly, depending on the compiler, device, number of APIs used and component configuration. The following table provides the memory usage for all APIs available in the given component configuration.

The measurements have been done with the associated compiler configured in the Release mode with an optimization set for Size. For a specific design, the map file generated by the compiler can be analyzed to determine the memory usage.

PSoC 4 (GCC)

Configuration		Flash Bytes	SRAM Bytes
Deep sleep operation	Disabled	240	9
	Enabled	188	8



Functional Description

This component is a basic operational amplifier. You may configure power, output strength, and interconnect the Opamp to other components. Low resistive connections are made from the Opamp to three selected pins to provide the optimal performance.

Using of the Compensation option

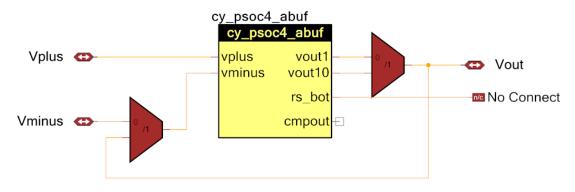
There are recommended settings for the Compensation option:

	Load Capacitance		
Loop Gain	Less than 50 pF	50pF to 125 pF	
1-6	Medium	High	
7 or more	Low	Medium	

These settings are applicable for the Output to pin setting, which is capable to drive a pin. 125 pF is the maximum load capacitance for this output.

Block Diagram and Configuration

The component uses cy_psoc4_abuf primitive.



Placement

Each Opamp is directly connected to specific GPIOs along with being connected to the internal fabric. The Output connection to a GPIO requires the use of the directly connected pin. Refer to the device datasheet for the part being used for the specific physical pin connections.

Registers

See the chip Technical Reference Manual (TRM) for more information about the registers.



Component Debug Window

PSoC Creator allows viewing debug information about the components in the design. Each component window lists the memory and registers for the instance. For detailed hardware registers descriptions, refer to the appropriate device technical reference manual. For detailed UDB registers descriptions used in the component, refer to the Registers section of this datasheet.

To open the Component Debug window:

- 1. Make sure the debugger is running or in break mode.
- 2. Choose **Windows > Components...** from the **Debug** menu.
- 3. In the Component Window Selector dialog, select the component instances to view and click **OK**.

The selected Component Debug window(s) will open within the debugger framework. Refer to the "Component Debug Window" topic in the PSoC Creator Help for more information.

Resources

The Opamp uses one of the opamp (Constant Time Block – mini (CTBm)) blocks in PSoC 4. No other resources are required.

DC and AC Electrical Characteristics

Specifications are valid for $-40 \text{ °C} \le T_A \le 85 \text{ °C}$ and $T_J \le 100 \text{ °C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
I _{DD}	Opamp Block current. No load.		_	_	-	-
I _{DD_HI}	Power = high		_	1000	1300	μA
I _{DD_MED}	Power = medium		-	320	500	μA
I _{DD_LOW}	Power = low		-	250	350	μA
I _{DD}	Opamp Block current. VDD = 1.8 V. No load.	For PSoC 4200 BLE family	-	-	-	-
I _{DD_HI}	Power = high	For PSoC 4200 BLE family	-	1000	1300	μA
I _{DD_MED}	Power = medium	For PSoC 4200 BLE family	-	500	-	μA
IDD_LOW	Power = low	For PSoC 4200 BLE family	_	250	350	μA
I _{DD_HI}	Power = high	For PSoC 4100M/ PSoC 4200M	Ι	1100	1850	μA



Parameter	Description	Conditions	Min	Тур	Мах	Units
I _{DD_MED}	Power = medium	For PSoC 4100M/ PSoC 4200M	-	550	950	μA
	Power = low	For PSoC 4100M/ PSoC 4200M	_	150	350	μA
I _{OUT_MAX}	$V_{DDA} \ge 2.7 \text{ V}, 500 \text{ mV}$ from rail		_	_	-	_
Iout_max_hi	Power = high		10	_	_	mA
I _{OUT_MAX_MID}	Power = medium		10	_	-	mA
I _{OUT_MAX_LO}	Power = low		_	5	_	mA
I _{OUT}	V _{DDA} = 1.71 V, 500 mV from rail		-	_	-	_
I _{OUT_MAX_HI}	Power = high		4	_	_	mA
IOUT_MAX_MID	Power = medium		4	_	_	mA
IOUT_MAX_LO	Power = low		-	2	_	mA
V _{IN}	Charge pump on, $V_{DDA} \ge 2.7 \text{ V}$		-0.05	_	VDDA – 0.2	V
V _{CM}	Charge pump on, $V_{\text{DDA}}\!\geq\!2.7~\text{V}$		-0.05	-	VDDA – 0.2	V
Vout	$V_{DDA} \ge 2.7 V$		_	_	_	
V _{OUT_1}	Power = high, I _{LOAD} =10 mA		0.5	_	VDDA – 0.5	V
V _{OUT_2}	Power = high, I _{LOAD} =1 mA		0.2	_	VDDA – 0.2	V
V _{OUT_3}	Power = medium, I _{LOAD} =1 mA		0.2	-	VDDA – 0.2	V
V _{OUT_4}	Power = low, I _{LOAD} =0.1mA		0.2	_	VDDA – 0.2	V
V _{OS}	Offset voltage	High mode	1	±0.5	1	mV
V _{OS}	Offset voltage	Medium mode	-	±1	_	mV
V _{OS}	Offset voltage	Low mode	_	±2	-	mV
V _{OS_DR}	Offset voltage drift	High mode	-10	±3	10	μV/C
V _{OS_DR}	Offset voltage drift	Medium mode	-	±10	_	μV/C
V _{OS_DR}	Offset voltage drift	Low mode	-	±10	_	μV/C
CMRR	DC	VDDD = 3.6 V	70	80	_	dB
CMRR	DC	For PSoC 4200 BLE family VDDD = 3.6 V, High- Power Mode	65	70	_	dB
CMRR	DC Common mode rejection ratio. High Power mode. Common Model Voltage Range from 0.5V to VDDA - 0.5V.	For PSoC 4100M/ PSoC 4200M VDDD = 3.6 V	60	70	-	dB
PSRR	At 1 kHz, 100 mV ripple	VDDD = 3.6 V	70	85	-	dB



AC Specifications

2.7 V Mathematical Mathematical Mathematical Mathematical SBW_MED Power = medium 4 MHz SBW_LO Power = nedium 4 MHz SBW_LO Power = nedium For PSoC 4200 BLE family, PSoC 4100M/PSoC 4200M 1 MHz SBW_LO Power = nedium For PSoC 4100M/PSoC 4200M 1 MHz SBW_LO Power = nigh For PSoC 4100M/PSoC 4200M 1 MHz SBW_LO Input referred, 1 KHz, power = high 94 µVrm /wa Input referred, 10kHz, power = high 72 nVrtH /wa Input referred, 10kHz, power = high 15 nVrtH /wa Input referred, 10kHz, power = high, Yooo 2 2.7 V 125 pF Slew_rate Cload = 50 pF, Power = High, Yooo 2 2.7 V 125 µSec I_op_wake From disable to enable,	Parameter	Description	Conditions	Min	Тур	Мах	Units
SBW_MED Power = medium 4 - - MHz SBW_LO Power = low 2 - - MHz SBW_LO Power = low For PSoC 4200 BLE family, PSoC 4100M/PSoC 4200M - 1 - MHz SBW_LO Power = low For PSoC 4200 BLE family, PSoC 4100M/PSoC 4200M - 1 - MHz Noise - - - - - - - - MHz Noise - 10 Power = high - 94 - µVrms Input referred, 1 KHz, power = high - 72 - nV/rH Ava Input referred, 10KHz, power = high - 15 - nV/rH Ava Input referred, 10KHz, power = ligh, Voao 2: 07. - 125 pF n nV/rH Cload Stable up to maximum load. Performance specs at 50 pF. - 125 pF - 125 pF Slew_rate Cload = 50 pF, Power = High, Voao 2: 07.	GBW			-	-	_	_
Dem_LOPower = low2MHzDBW_LOPower = lowFor PSoC 4200 BLE family, PSoC 4100M/PSoC 4200M-1-MHzValse N_{N1} Input referred, 1 Hz - 1GHz, power = high-94- μ Vrms I_{N2} Input referred, 1 kHz, power = high-72-nV/rtH I_{N2} Input referred, 10kHz, power = high-28-nV/rtH I_{N3} Input referred, 10kHz, power = high-15-nV/rtH I_{N4} Input referred, 10kHz, power = high15-nV/rtH I_{N4} Nobe 10 enable, no external RC dominating-25-125Ipput referred, Ipput referred, Ipput referred, Ipput referred, Ipput referred, Ipput referred, Ipput r	GBW_HI	Power = high		6	_	-	MHz
Deriv BRW_DPower = lowFor PSoC 4200 BLE family, PSoC 4100M/PSoC 4200M-1-MHzNoise (N_{11}) Input referred, 1 Hz - 1GHz, power = high-94- μ /Vrm (N_{12}) Input referred, 1 kHz, power = high-72-n//rtH (N_{12}) Input referred, 10kHz, power = high-28-n//rtH (N_{13}) Input referred, 10kHz, power = high-15-n//rtH (N_{14}) Noba berofmanance specs at 50 pF125p/ (T_{14}) Cload = 50 pF, Power = High, $N_{50,A} < 2.7 V$ 300- μ Sec (T_{20}) Profmanane berofmanane <td>GBW_MED</td> <td>Power = medium</td> <td></td> <td>4</td> <td>_</td> <td>-</td> <td>MHz</td>	GBW_MED	Power = medium		4	_	-	MHz
PSoC 4100M/PSoC 4200M Image: Control of the state of th	GBW_LO	Power = low		2	-	-	MHz
V_{N1} Input referred, 1 Hz - 1GHz, power = high-94- μ Vrms V_{N2} Input referred, 1 kHz, power = high-72-nV/rtH V_{N3} Input referred, 10kHz, power = high-28-nV/rtH V_{N4} Input referred, 10kHz, power = high-15-nV/rtH V_{N4} Input referred, 10kHz, power = high-15-nV/rtH V_{N4} Input referred, 10kHz, power = Performance specs at 50 pF15-nV/rtH C_{LOAD} Stable up to maximum load. Performance specs at 50 pF125pFSlew_rateCload = 50 pF, Power = High, Vopa ≥ 2.7 V-300- μ SecT_op_wakeFrom disable to enable, no external RC dominatingPSoC 4100M/PSoC 4200M-25- μ SecDep-Sleep Mode(For PSoC 4200 BLE family; only guaranteed for VDDA ≥ 2.5 V)-kHz μ AMos_DSGain bandwidth product-50-kHzDD_DSCurrent-50- μ AVos_DSOffset voltage drift-20- μ V/rCVout_DSOutput voltage0.2-VDD-0.2VVom_DSCommon mode voltage0.2-VDD-1.8VDep-Sleep Mode(For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA ≥ 2.7 VVDD-1.8VDep-Sleep Mode(For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA ≥ 2.7 VVDD-1.8<	GBW_LO	Power = low		-	1	-	MHz
power = highImage: Constraint of the second se	Noise			-	-	-	-
highImageImageImageImage V_{N3} Input referred, 10kHz, power = highImage-28-nV/rtH V_{N4} Input referred, 10kHz, power = high-15-nV/rtH C_{L0AD} Stable up to maximum load. Performance specs at 50 pF15-nV/rtH C_{L0AD} Stable up to maximum load. Performance specs at 50 pF125pFSlew_rateCload = 50 pF, Power = High, Voba > 2.7 V6V/use T_op_wake From disable to enable, no external RC dominatingPSoC 4100M/PSoC 4200M-25- μ SecDeep-Sleep Mode (For PSoC 4200 BLE family; only guaranteed for VDDA > 2.5 V)-50-kHzDD_DSCurrent-50-mV/vC Vos_DS Offset voltage-5-mV/vC Vos_DS Offset voltage drift-0.2- $VDD-0.2$ V Vom_DS Courtont under splate GBW.0.2-VDD-0.2V Vom_DS Common mode voltage0.2-VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA > 2.7 V)VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA > 2.7 V)VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA > 2.7 V)VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA > 2.7 V)VDD-1.8V	V _{N1}			-	94	-	µVrms
highImageImageImageImage V_{N4} Input referred, 100kHz, power = highImageImageImageN/rtH C_{LOAD} Stable up to maximum load. Performance specs at 50 pF.ImageImageImageImageImage C_{LOAD} Stable up to maximum load. Performance specs at 50 pF.ImageI	V _{N2}			-	72	_	nV/rtHz
highh	V _{N3}			-	28	-	nV/rtHz
Performance specs at 50 pF.Image: Constraint of the species of the spe	V _{N4}			-	15	-	nV/rtHz
VDDA \geq 2.7 VImage: Constraint of the sector	C _{LOAD}			-	-	125	pF
Image: constraint of the state of the st	Slew_rate			6	-	_	V/µsec
Image: content and conten	T_op_wake			-	300	_	µSec
GBW_DSGain bandwidth product-50-kHzDD_DSCurrent-15- μA Vos_DSOffset voltage-5-mVVos_dr_DSOffset voltage drift-20- $\mu V/^{\circ} C$ Vout_DSOutput voltage0.2-VDD-0.2VVcm_DSCommon mode voltage0.2-VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA ≥ 2.7 V)Vode 2 is lowest current range. Mode 1 has higher GBW1400uADD_HI_M1Mode 1, High current25 °C-700uADD_LOW_M1Mode 1, Low current25 °C-200uA	T_op_wake		PSoC 4100M/PSoC 4200M	-	25	-	µSec
DD_DSCurrent-15- μA Vos_DSOffset voltage-5-mVVos_dr_DSOffset voltage drift-20- $\mu V/^{\circ}C$ Vout_DSOutput voltage0.2-VDD-0.2VVcm_DSCommon mode voltage0.2-VDD-1.8VDeep-Sleep Mode(For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA ≥ 2.7 V)VVMode 2 is lowest current range. Mode 1 has higher GBW1400uADD_HI_M1Mode 1, High current25 °C-700uADD_LOW_M1Mode 1, Low current25 °C-200uA	Deep-Sleep Mode	e (For PSoC 4200 BLE family; only g	juaranteed for VDDA > 2.5 V)				
Vos_DSOffset voltage-5-mVVos_DSOffset voltage drift-20- $\mu V/^{\circ} C$ Vos_dr_DSOutput voltage0.2-VDD-0.2VVout_DSOutput voltage0.2-VDD-0.2VVcm_DSCommon mode voltage0.2-VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA \geq 2.7 V)Vode 2 is lowest current range. Mode 1 has higher GBW1400uADD_HI_M1Mode 1, High current25 °C-700uA-DD_LOW_M1Mode 1, Low current25 °C-200uA	GBW_DS	Gain bandwidth product		-	50	-	kHz
LLLLLLLLVos_dr_DSOffset voltage drift-20- $\mu V/^{\circ} C$ Vout_DSOutput voltage0.2-VDD-0.2VVcm_DSCommon mode voltage0.2-VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA \geq 2.7 V)VVVMode 2 is lowest current range. Mode 1 has higher GBW1400uADD_HI_M1Mode 1, High current25 °C-700uADD_LOW_M1Mode 1, Low current25 °C-200uA	IDD_DS	Current		-	15	-	μA
Vout_DSOutput voltage0.2- $VDD-0.2$ VVcm_DSCommon mode voltage0.2-VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA \geq 2.7 V)VVVMode 2 is lowest current range. Mode 1 has higher GBW.DD_HI_M1Mode 1, High current25 °C-1400uADD_MED_M1Mode 1, Medium current25 °C-700uAUADD_LOW_M1Mode 1, Low current25 °C-200uA	Vos_DS	Offset voltage		-	5	-	mV
Vcm_DSCommon mode voltage 0.2 $-$ VDD-1.8VDeep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA ≥ 2.7 V)Mode 2 is lowest current range. Mode 1 has higher GBW.DD_HI_M1Mode 1, High current $25 ^{\circ}$ C $-$ 1400uADD_MED_M1Mode 1, Medium current $25 ^{\circ}$ C $-$ 700uADD_LOW_M1Mode 1, Low current $25 ^{\circ}$ C $-$ 200uA	Vos_dr_DS	Offset voltage drift		-	20	-	µV/°C
Deep-Sleep Mode (For PSoC 4100M/PSoC 4200M; only guaranteed for VDDA \geq 2.7 V)Mode 2 is lowest current range. Mode 1 has higher GBW.DD_HI_M1Mode 1, High current25 °C-1400uADD_MED_M1Mode 1, Medium current25 °C-700uADD_LOW_M1Mode 1, Low current25 °C-200uA	Vout_DS	Output voltage		0.2	_	VDD-0.2	V
Mode 2 is lowest current range. Mode 1 has higher GBW. DD_HI_M1 Mode 1, High current 25 °C - 1400 uA DD_MED_M1 Mode 1, Medium current 25 °C - 700 uA DD_LOW_M1 Mode 1, Low current 25 °C - 200 uA	Vcm_DS	Common mode voltage		0.2	_	VDD-1.8	V
DD_MED_M1Mode 1, Medium current25 °C-700uADD_LOW_M1Mode 1, Low current25 °C-200uA	• •						
DD_LOW_M1 Mode 1, Low current 25 °C - 200 uA	IDD_HI_M1	Mode 1, High current	25 °C	-	1400	uA	
	IDD_MED_M1	Mode 1, Medium current	25 °C	-	700	uA	
DD_HI_M2 Mode 2, High current 25 °C - 120 uA	IDD_LOW_M1	Mode 1, Low current	25 °C	-	200	uA	
	IDD_HI_M2	Mode 2, High current	25 °C	-	120	uA	



Parameter	Description	Conditions	Min	Тур	Мах	Units
IDD_MED_M2	Mode 2, Medium current	25 °C	-	60	uA	
IDD_LOW_M2	Mode 2, Low current	25 °C	-	15	uA	
GBW_HI_M1	Mode 1, High current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	4	MHz	
GBW_MED_M1	Mode 1, Medium current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	2	MHz	
GBW_LOW_M1	Mode 1, Low current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.5	MHz	
GBW_HI_M2	Mode 2, High current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.5	MHz	
GBW_MED_M2	Mode 2, Medium current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.2	MHz	
GBW_LOW_M2	Mode 2, Low current	20-pF load, no DC load 0.2 V to VDDA-1.5 V	-	0.1	MHz	
VOS_HI_M1	Mode 1, High current	With trim 25 °C, 0.2 V to VDDA- 1.5 V	-	5	mV	
VOS_MED_M1	Mode 1, Medium current	With trim 25 °C, 0.2 V to VDDA- 1.5 V	-	5	mV	
VOS_LOW_M2	Mode 1, Low current	With trim 25 °C, 0.2 V to VDDA- 1.5 V	-	5	mV	
VOS_HI_M2	Mode 2, High current	With trim 25 °C, 0.2 V to VDDA- 1.5 V	-	5	mV	
VOS_MED_M2	Mode 2, Medium current	With trim 25 °C, 0.2 V to VDDA- 1.5 V	-	5	mV	
VOS_LOW_M2	Mode 2, Low current	With trim 25 °C, 0.2 V to VDDA- 1.5 V	-	5	mV	
IOUT_HI_M!	Mode 1, High current	Output is 0.5 V to VDDA-0.5 V	-	10	mV	
IOUT_MED_M1	Mode 1, Medium current	Output is 0.5 V to VDDA-0.5 V	-	10	mV	
IOUT_LOW_M1	Mode 1, Low current	Output is 0.5 V to VDDA-0.5 V	-	4	mV	
IOUT_HI_M2	Mode 2, High current	Output is 0.5 V to VDDA-0.5 V	-	1	mV	
IOU_MED_M2	Mode 2, Medium current	Output is 0.5 V to VDDA-0.5 V	-	1	mV	
IOU_LOW_M2	Mode 2, Low current	Output is 0.5 V to VDDA-0.5 V	-	0.5	mV	



Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.10.c	Edited the datasheet.	Updated Offset voltage and Offset voltage drift parameter names into DC Specifications table.
1.10.0		Updated DC and AC Electrical Characteristics section with PSoC 4100M/ PSoC 4200M data.
1.10.b	Edited the datasheet.	Added CMRR parameter values for PSoC 4200 BLE devices.
1.10.a	Edited the datasheet.	Added information that for correct operation in deep sleep mode, V_{DDA} must be larger than 2.5 V.
	Added the Deep sleep operation parameter to control component availability in Deep Sleep mode.	Updates to support PSoC 4200 BLE devices.
	Updated API Memory usage and MISRA compliance sections.	opuales to support P SOC 4200 BLE devices.
1.10	Removed references to SaveConfig() and RestoreConfig() APIs because they are empty.	
	Changed output mode parameters from "1mA" and "10mA" to "Internal only" and "Output to pin" respectively.	
1.0.a	Updated datasheet.	Corrected specs to match device datasheet.
1.0	First release	

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