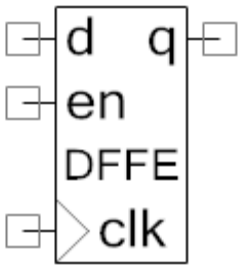
# D Flip Flop w/ Enable

1.0




## Features

- Enable input allows d input to be selectively captured.
- Configurable width for array of D Flip Flops with a single enable.

## General Description

The D Flip Flop w/ Enable selectively captures a digital value.

### When to Use a D Flip Flop w/ Enable

Use the D Flip Flop w/ Enable to implement sequential logic.

## Input/Output Connections

This section describes the various input and output connections for the D Flip Flop w/ Enable.

### d – Input

This input determines the next value of the output. The output does not change until the next rising edge of the clock.

### en – Input

This input determines whether the current value on the d input will be stored and propagated to the output.

### clock – Input

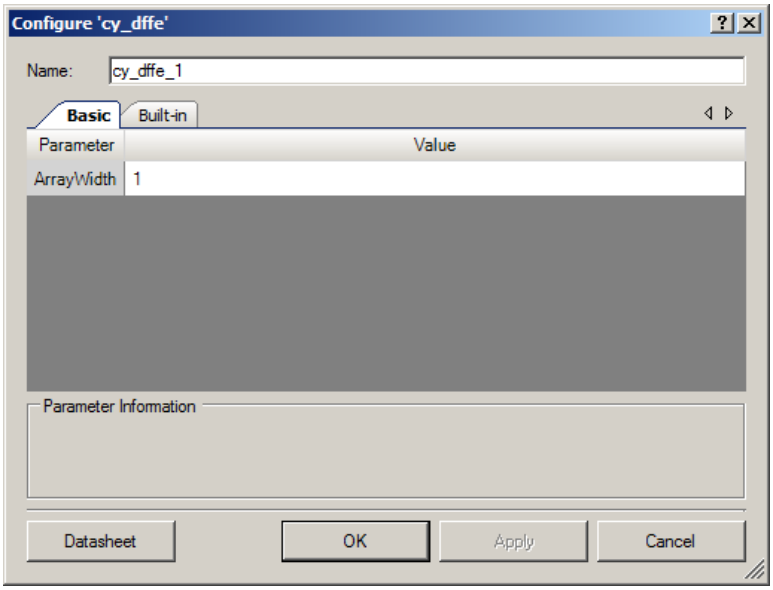
The clock signal determines when the output will change. The output changes when a rising edge of the clock is detected.

### q – Output

The stored value.

# Component Parameters

Drag a D Flip Flop w/ Enable onto your design and double-click it to open the **Configure** dialog.




The D Flip Flop w/ Enable provides the following parameters.

### ArrayWidth

You can create an array of D Flip Flops with a single Enable, which is useful if the input or output is a bus. This parameter defines the bus width of the d and q terminals. The value must be between 1 and 32. The default is **1**.

# Functional Description

The D Flip Flop w/ Enable is implemented in PLD macrocells. All macrocell flip-flops are initialized to a 0 value at power up and after any reset of the device. The enable functionality is implemented in product terms in the PLD using the following logical equation:

$Q = En ? D : Q_{PREV}$

**Table 1. 1-ArrayWidth D Flip Flop w/ Enable Truth Table**

| $Q_{PREV}$ | Enable | D | Q |
|---|---|---|---|
| 0 | 0 | X | 0 |
| 1 | 0 | X | 1 |
| X | 1 | 0 | 0 |
| X | 1 | 1 | 1 |

A letter ‘X’ in the truth table indicates that the input does not affect the output.

# Resources

The D Flip Flop w/ Enable uses one macrocell. If the ArrayWidth parameter is greater than 1, the D Flip Flop w/ Enable uses a number of macrocells equal to ArrayWidth. All D Flip Flop w/ Enable components in the same PLD must have the same clock signal for clocking.

# MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined: project deviations – deviations that are applicable for all PSoC Creator components and specific deviations – deviations that are applicable only for this component. This section provides information on component specific deviations. Non PSoC 6 project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment. For PSoC 6, refer to PSoC Creator Help > Building a PSoC Creator Project > Generated Files (PSoC 6) for information on MISRA compliance and deviations for files generated by PSoC Creator.

The D Flip Flop w/ Enable component does not have any C source code APIs.

# DC and AC Electrical Characteristics

The D Flip Flop w/ Enable component supports the maximum device frequency.

# Component Changes

This section lists the major changes in the component from the previous version.

| Version | Description of Changes | Reason for Changes / Impact |
|---|---|---|
| 1.0.b | Updated MISRA section.<br>Added PSoC 6 support. | |
| 1.0.a | Minor datasheet edits. | |
| 1.0 | First version of this component. | |