

The advantages of Complementary Power MOSFETs in Non-isolated Point of Load

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1 Introduction

In low power Non-isolated Point of Loads there is a trend to reduce the size of the overall converter. This is achieved by increasing the switching frequencies up to 2MHz. However, at these high frequencies there will be a big problem with the parasitic inductor in the circuit. A couple of nano-Henrys of inductance can cause huge voltage spikes that can destroy the MOSFETs. To avoid this destruction an extra protection circuit has to be implemented but this will increase converter design complexity and cost.

The purpose of this application note is to give an overview of Complementary Power MOSFETs for Non-isolated Point of Load applications and how they can simplify the converters design complexity whilst at the same time reducing the size.

2 What is a Complementary Power MOSFET

Complementary Power MOSFETs are devices with both a P-channel and an N-channel MOSFET contained within the same package. This makes them very suitable for low power Non-isolated Point of Loads. Within a complementary device the P-channel and N-channel MOSFETs are not electrically connected. Thermally they have little influence on each other but it depends entirely on the cooling area. This feature makes it suitable for two-transistor non-isolated DC/DC converters such as Buck, Boost and non-inverted Buck-Boost converters.

3 Problems in high frequency Non-isolated Point of Load

In low power high frequency DC/DC converters a common potential cause of failure of the MOSFETs is parasitic inductance in the circuit which can cause huge voltage spikes. This can be illustrated in detail with an example. Consider a 3.3W Non-isolated Point of Load with 12V of input voltage and 5V of output voltage operating at a frequency of 800kHz. Figure 1 is a typical circuit configuration of a Non-isolated Point of Load.

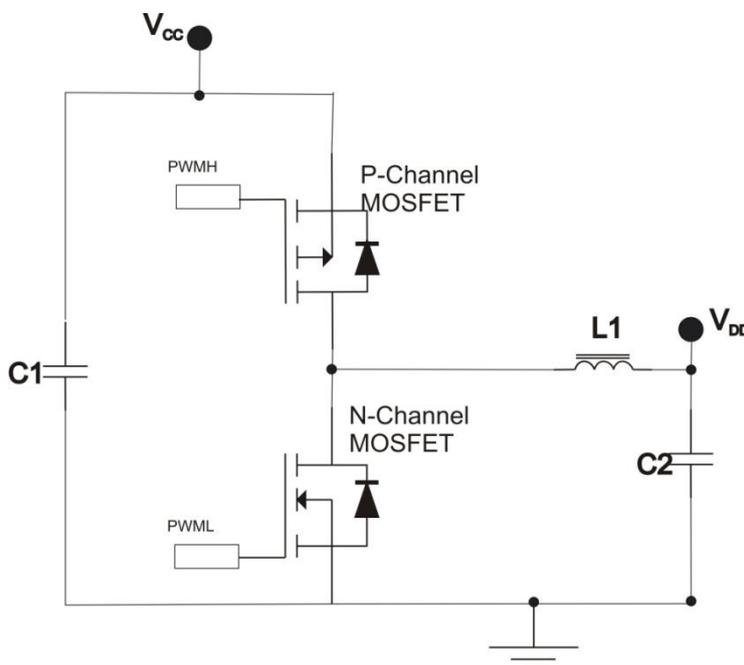


Figure 1: Typical Non-isolated Point of Load

The MOSFETs used in the system have a breakdown voltage of 20V. It is also considered that the entire system is assembled on a 1oz. copper PCB. Figure 2 shows a sample PCB layout of the converter.

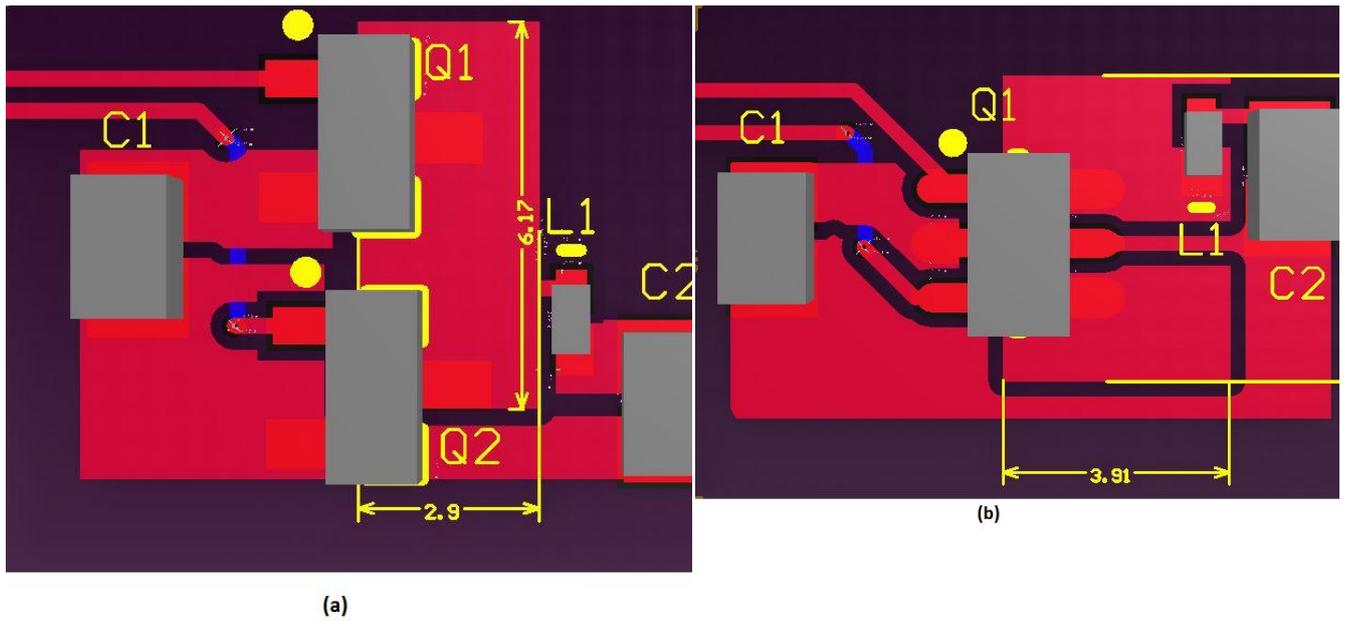


Figure 2: Non-isolated Point of Load sample layout (a) with discrete MOSFETs (b) with a Complementary MOSFET

An approximation for the inductance of the PCB trace is

$$L_{trace} = 0.0002 * l \left[\ln\left(\frac{2l}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5 \right] \mu H$$

l ... length of the trace

W ... width of the trace

H ... height of the trace

The height of the trace is usually 35µm/1oz. copper or 70µm/2oz. copper.

Figure 3 below shows the variation of inductance with trace length and width.

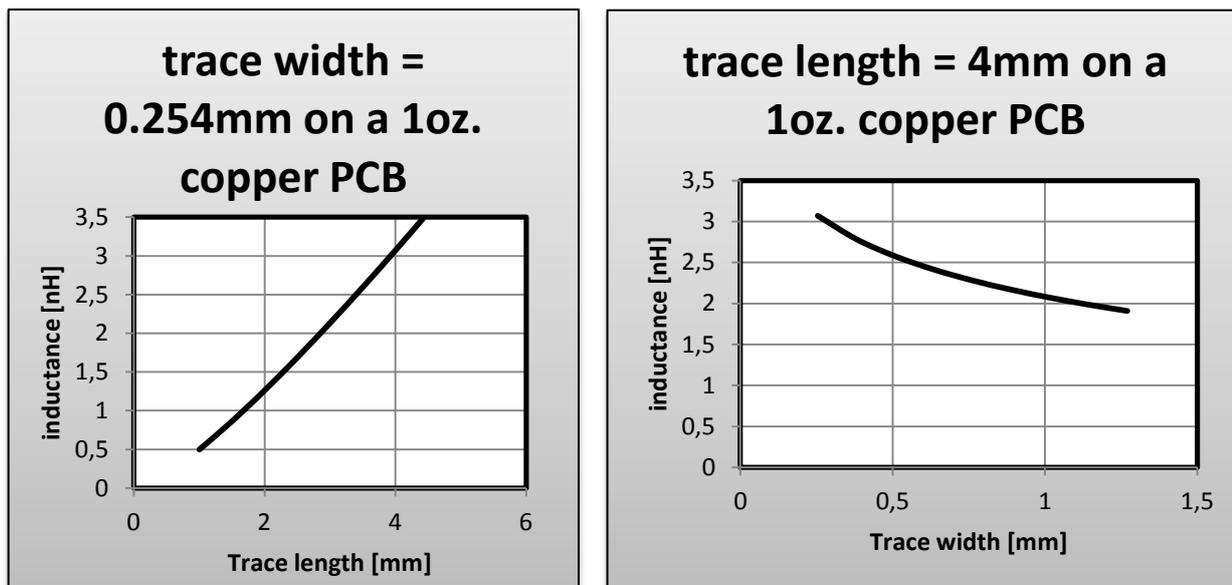


Figure 3: PCB trace inductance

As shown in the layout (Figure 2 (a)), the parasitic inductance in the circuit is ~3nH. At a switching frequency of 800kHz this inductance can cause a voltage spike up to the MOSFET breakdown voltage as shown in Figure 4 below. This voltage spike may destroy or degrade the MOSFET over time.

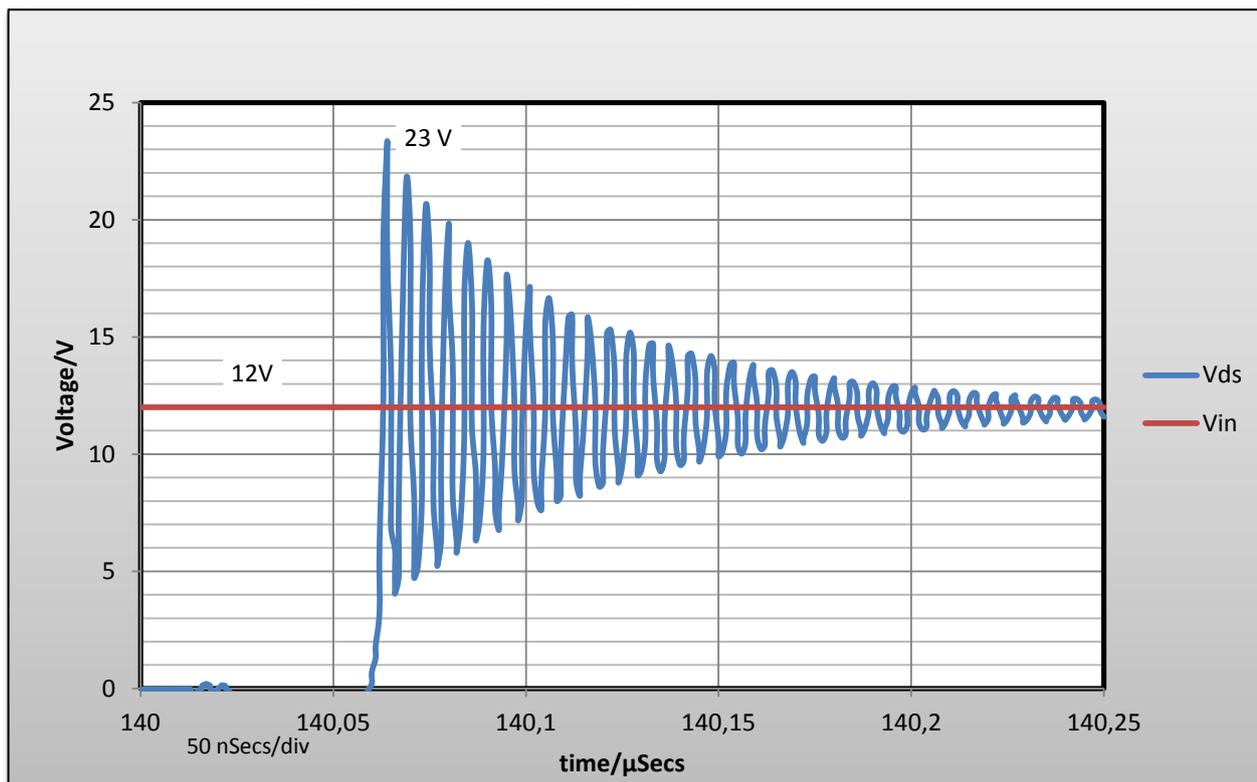


Figure 4: Drain voltage of low side MOSFET

From the above example it is clear that for high frequency DC/DC converters, parasitic inductance is a big problem. A protection circuit can be implemented but this increases the circuit complexity and the total cost of the system. From Figure 3 it is clear that a wider PCB track can be used to reduce this inductance. Doubling the width of the track reduces the inductance by 11%. However, the most effective way is to reduce the length of the track. Halving the length can reduce the inductance by 44%.

4 Complementary Power MOSFETs in Non-isolated Point of Load

Infineon's Complementary Power MOSFETs are available in SOT363, TSOP-6 and in SO-8 packages. Table 1 below shows the Infineon Complementary Power MOSFET portfolio

	Package	$V_{DS,max}$ [V]	$R_{DS(on),max}$ [mΩ]	$I_{D,max}$ [A]	Q_G [nC]	$P_{tot,max}$ [W]
BSD235C	SOT363	-20	2100	-0.53	-0.4	0.5
		20	600	0.95	0.34	
BSL215C	TSOP6	20	250	1.5	0.73	0.5
		-20	280	-1.5	-3	
BSL308C	TSOP6	-30	80	-2	-5	0.5
		30	57	2.3	1.5	
BSL306C	TSOP6	30	160	1.4	0.6	0.5
		-30	150	-1.5	-2.4	
BSO612CV G	SO-8	-60	300	-2	10.5	2.0
		60	120	3	10.3	
BSO615C G	SO-8	-60	300	-2	13.5	2.0
		60	110	3.1	15	

Table 1: Complementary Power MOSFET portfolio

Let's consider an example with the TSOP-6 package. Figure 5 shows the pin configuration.

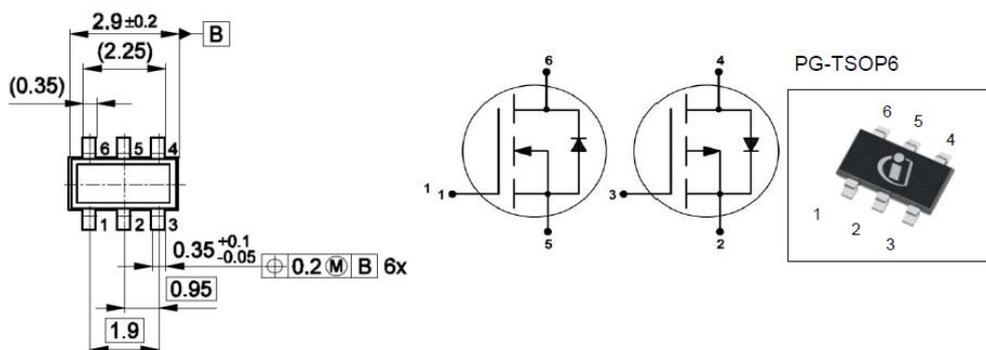


Figure 5: Complementary Power MOSFET configuration in TSOP-6

Since both the transistors are in a single package the parasitic inductance in the circuit will be reduced drastically. So, for the same system shown in figure 1, replacing the two transistors with a Complementary MOSFET as shown in Figure 2(b) will reduce the parasitic inductance by ~44%.

The reduced parasitic inductance will keep the voltage spike on the MOSFET to a minimum. Since the voltage spike is minimal there is no need for a protection circuit in the design thus reducing design complexity.

5 Conclusion

Combining a P-channel and an N-channel MOSFET within a single package reduces the parasitic inductance in the circuit and is the best fit for low power high frequency DC/DC converter applications. The P-channel MOSFET also simplifies the high side gate driver circuitry.

A Complementary Power MOSFET gives an opportunity to reduce the complexity of the design and the number of components without compromising circuit functionality.