REF_IRS2461S_5KW

2.5kW x 2 channel Class D audio amplifier using IRS2461S

About this document

Scope and purpose

The REF_IRS2461S_5KW evaluation board is a two-channel, 2500W/ch (2Ω at ±103.5V) half-bridge Class D audio power amplifier for after market car audio or high-power audio system applications. This evaluation board demonstrates how to use the IRS2461S controller IC, implement protection circuits, and design an optimum PCB layout. This design can be scaled for a 1600W/ch (4Ω at ±120V) and instruction of doing so are included.

Intended audience

- After-market car audio applications
- High power audio systems

Features

- Output power: 2500W x 2 channel (1% THD+N)
- Multiple protection features
  - Over-current protection (OCP), high side and low side FETs
  - Over-voltage protection (OVP)
  - Under-voltage protection (UVP)
  - Over-temperature protection (OTP)
- PWM modulator
  - Self-oscillating half bridge topology with optional clock synchronization

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1 Specifications

Table 1 General test conditions

Conditions		Notes/conditions
Supply voltages	±75V to ±119V	Bipolar power supply
	±103.5V	Nominal bipolar power supply
Rated load impedance	2Ω	Resistive load
Self-oscillating frequency	317kHz	No input signal, adjustable
Voltage gain	30.85 dB	

Table 2 Electrical data

Data	Typical	Notes/conditions
Infineon devices used	IRS2461S Class D IC with IPP220N25NFD x4	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Output power CH1-4: (1% THD+N)	2500W	1kHz, R_L = 2Ω
Output power CH1-4: (10% THD+N)	3150W	1kHz, R_L = 2Ω
Rated load impedance	2Ω	
Idling supply current	±140 mA	No input signal, ±103.5V
THD+N	0.08 %	@1kHz, 100W_{out}, 2Ω
Residual noise	140 µVrms	IHF-A weigthed, AES-17 filter, 20kHz SPCL
	220 µVrms	AES-17 filter, 20kHz SPCL
Signal to noise ratio	113 dB	

Table 3 Other features

Feature	Optional	Adjustable	Setting
Over temperature protection (OTP)	Yes	Yes	110^{0}C
Over current protection (OCP)	No	Yes	177A @T_j = 25^{0}C
Over voltage protection (OVP) & under voltage protection (UVP)	Yes	Yes	119V (OVP) 75V (UVP)
DC protection (DCP)	Yes	Yes	2V

2 Board sections and typical connection setup

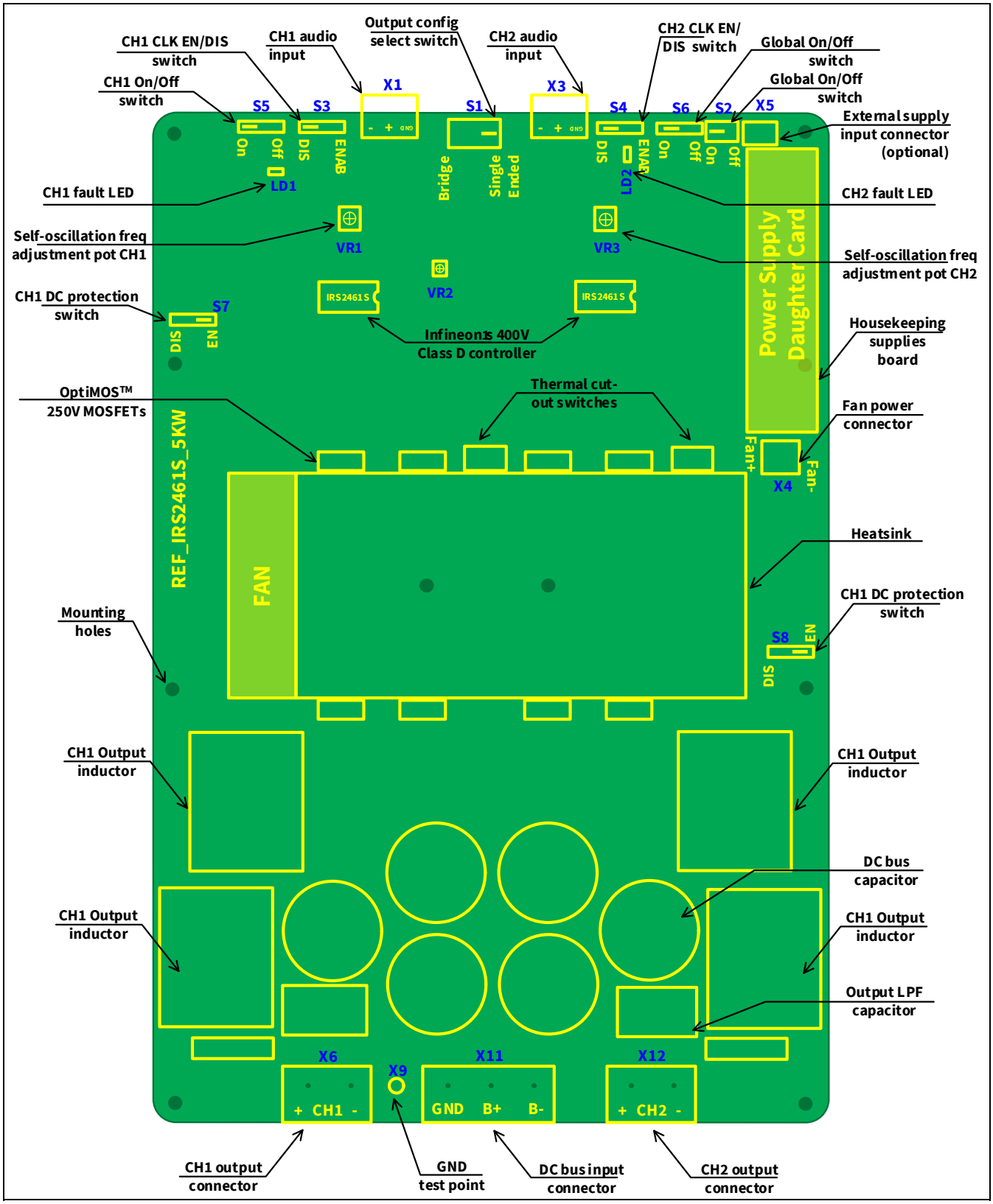


Figure 1 Main components on the main board

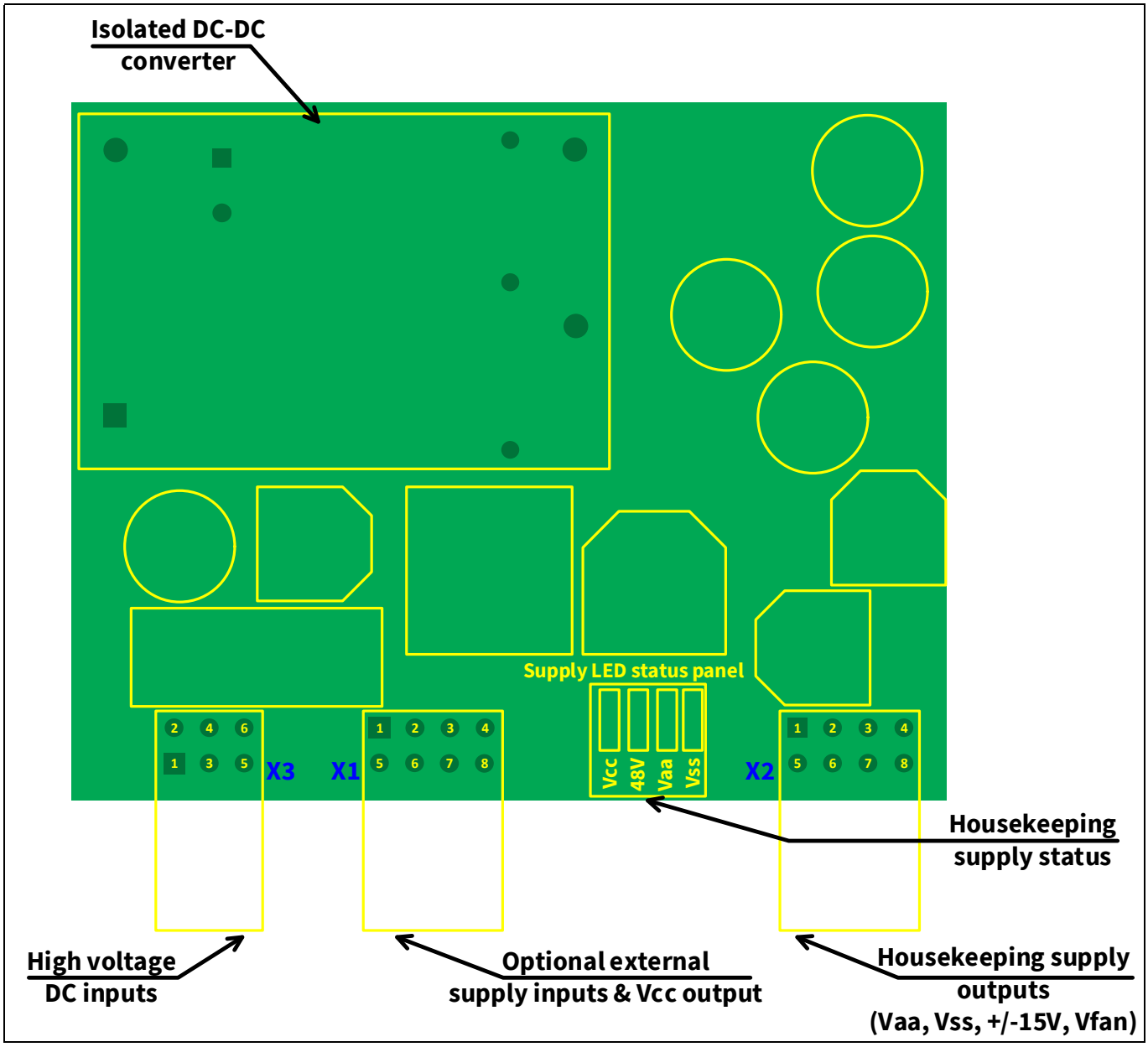


Figure 2 Power Supply Daugther Card (PSDC)

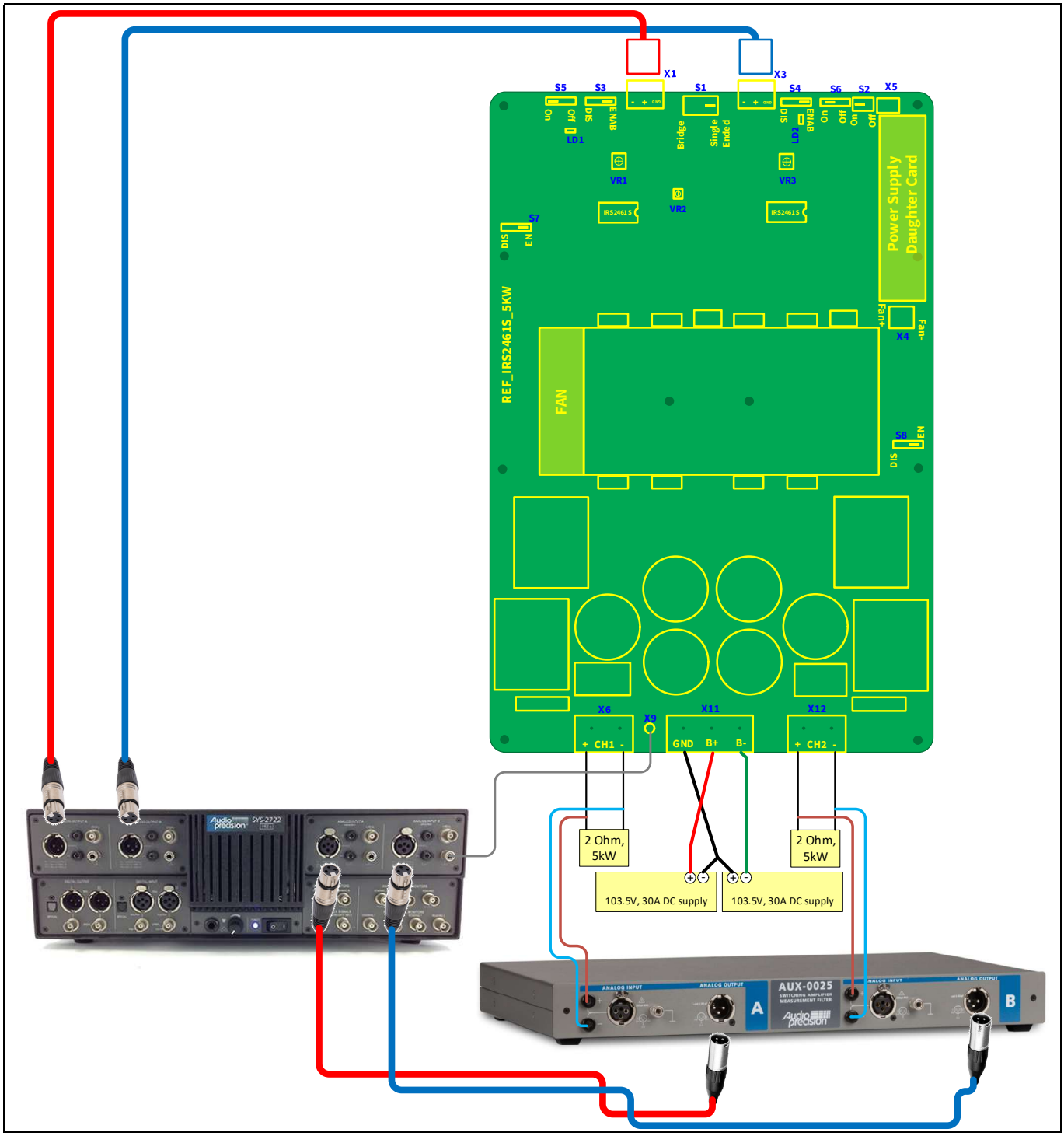


Figure 3 Connection setup for Mother Board (Single ended)

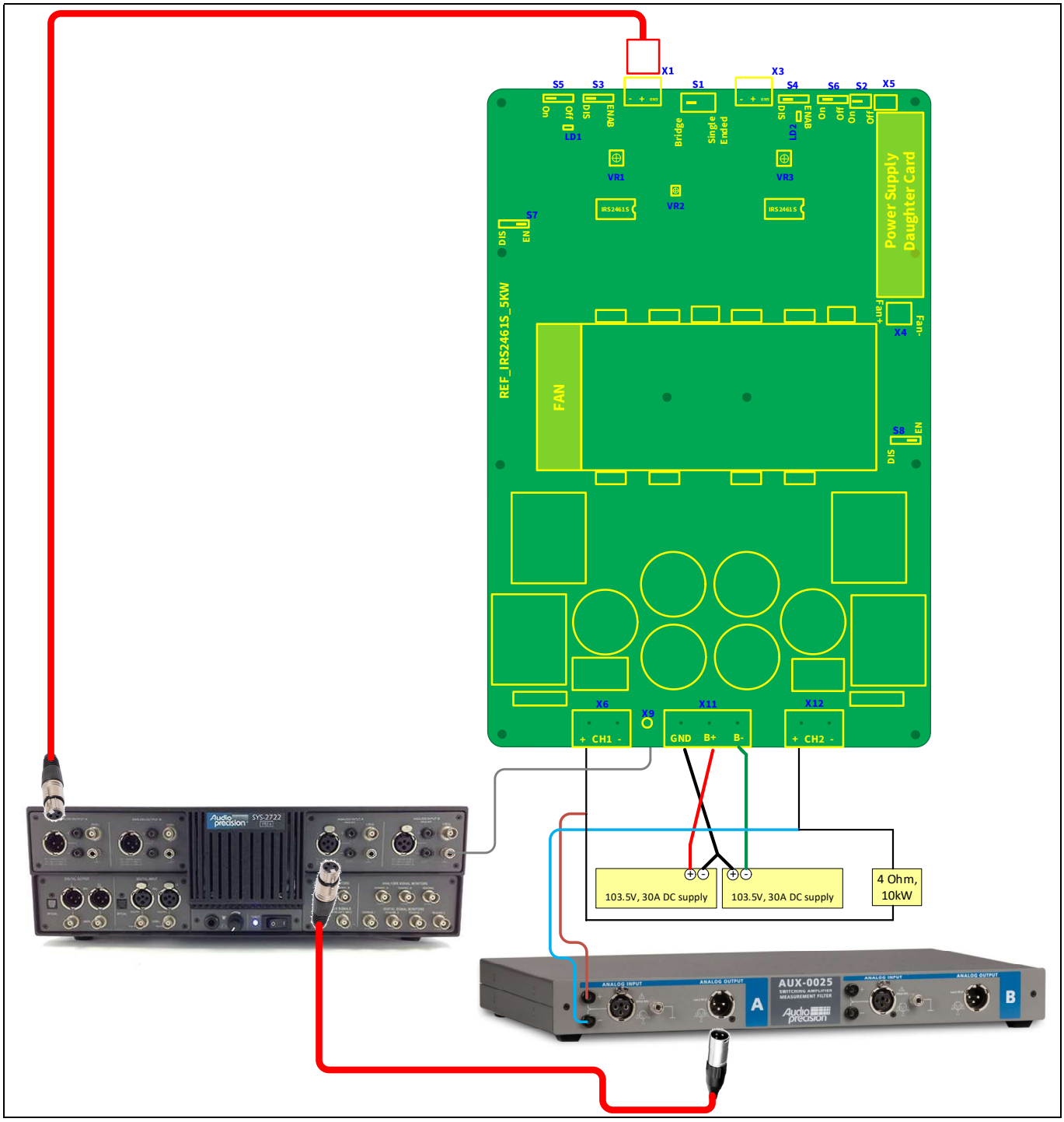


Figure 4 Connection setup for Mother Board (Bridge-tie load (BTL))

3 Connector description

Table 4 Mother Board (MB) connector description

Signal	Connector	Description
CH1 IN	X1	Analog input for CH1
CH2 IN	X3	Analog input for CH2
CH1 CLK enable	S3 switch	Clock injection enable/ disable switch for CH1
CH2 CLK enable	S4 switch	Clock injection enable/ disable switch for CH2
CH1 On/Off	S5 switch	CH1 On/Off switch
Ch2 On/Off	S6 switch	CH2 On/Off switch
CH1/CH2 On/Off	S2 switch	CH1 and CH2 global On/Off switch
CH1 DC protection EN/DIS switch	S7 switch	Enable or disable CH1 DC protection (useful for no-load testing)
CH2 DC protection EN/DIS switch	S8 switch	Enable or disable CH2 DC protection (useful for no-load testing)
Fan supply	X4	Fan power supply connector
POWER	X11	Positive and negative supply (+B/-B)
CH1_OUT	X6	Output for CH1
CH2_OUT	X12	Output for CH2
Single ended/ Bridged output	S1	Single ended or Bridged output selection switch
External Supply	X5	Input for external supply (modifications are needed on the Power Supply daughter card). See the board silkscreen or the schematic/ layout files to see pin description
Power supply connector	X2, X7, X8	Input/output connectors for the Power Supply daughter card

Table 5 Power Supply Daughter Card (PSDC) connector description

Signal	Connector	Description
B+	X3 pin 1, pin 2	Positive DC rail input
GND	X3 pin 3, pin 4 X1 pin 3, pin 7 X2 pin 2, pin 6	Power GND
B-	X3 pin 5, pin 6 X1 pin 5, pin 6	Negative DC rail input
Vcc	X1 pin 1	Vcc supply output
Vcc_ext	X1 pin 2	Vcc supply input (optional)
15V+_ext	X1 pin 4	Positive 15V supply input (optional)
15V-_ext	X1 pin 8	Negative 15V supply input (optional)

Signal	Connector	Description
+5Vaa	X2 pin 1	Vaa supply output
-5Vss	X2 pin 5	Vss supply output
15V+	X2 pin 3	Positive 15V supply output
15V-	X2 pin 7	Negative 15V supply output
24Vfan+	X2 pin 4	Positive terminal 24V fan supply output
24Vfan-	X2 pin 8	Negative terminal 24V fan supply output

3.1 Hardware required

3.1.1 Cabling

It is recommended to use thick wires (10 AWG or lower) for all power connections (B+, B-, GND on X11 connector and channel outputs on X6 and X12 connectors). The board connectors allow easy connection and disconnection of these wires.

For the audio input, it is possible to select either BNC output or the XLR from the AP. A custom cable can be prepared by using

1) BNC to alligator cable such as 501-1131-ND
2) Female XLR connector such as Neutrik NC3FXX

and cabling it to the mating connector (Pheonix Contact p.n. 1900471) for X1 and X3.

3.1.2 Power supplies

It is recommended to use high-voltage and low noise power supplies such as Keysight N8760A (2-phase rated power operation) or N8740A (for testing 1 phase rated power operation).

3.1.3 Dummy load

A high-power resistive load such as TE2500B8R2J is recommended for testing the setup. It is recommended to use forced airflow to maintain stable ohmic value for high power testing. Also note that such loads have significant inductance at frequencies >1kHz. This can affect frequency response measurements. For frequency response tests, it is recommended to use low power non-inductive resistive loads.

3.2 Audio Precision (AP) setup

REF_IRS2461S_5KW and AP shall be connected according to the Figure 5.

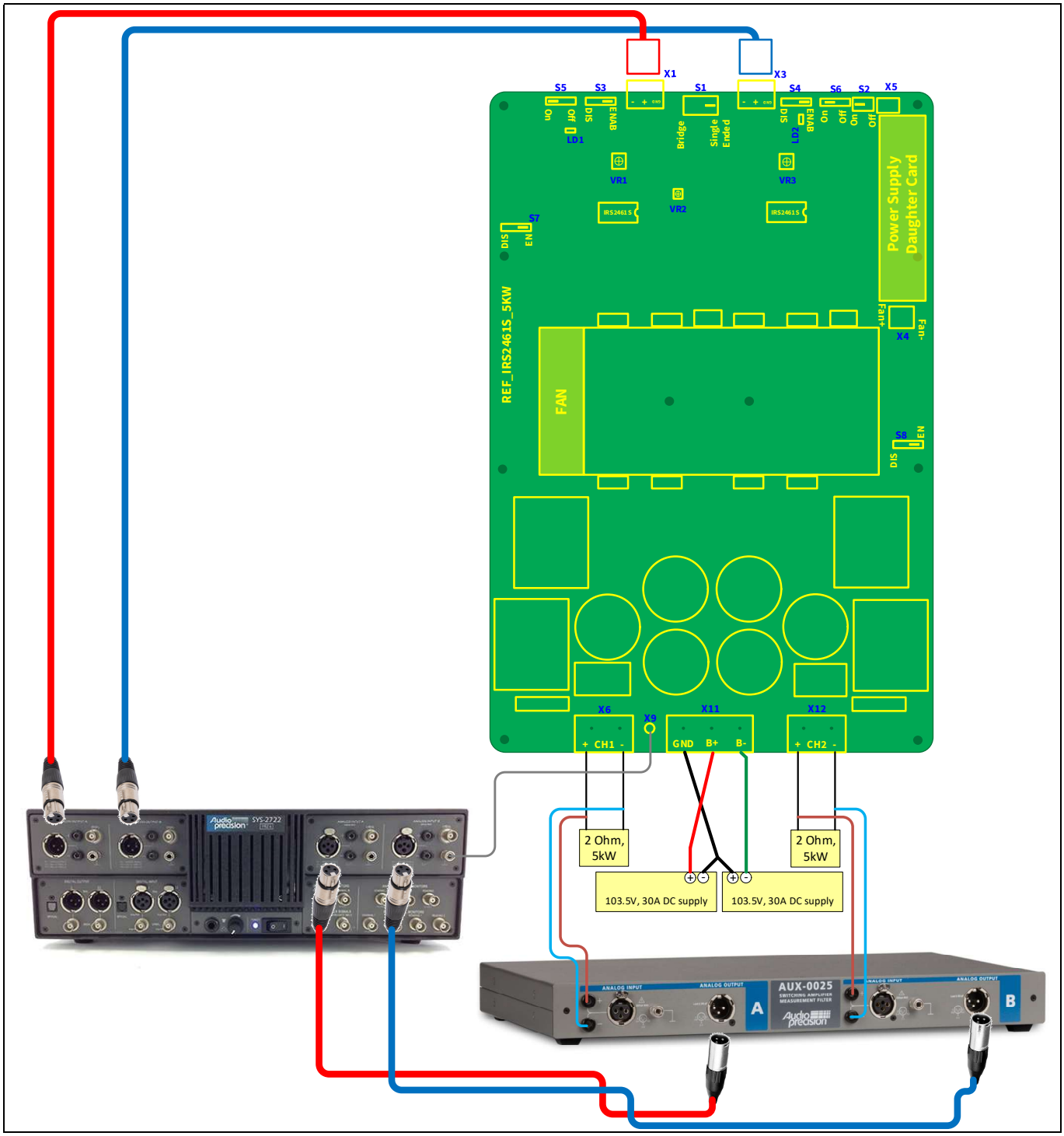


Figure 5 Audio Precision (AP) connection

4 Test procedure

4.1 Test setup

1. Connect 2Ω – 5000W dummy loads to the output connectors (X6, X12 as shown in Figure 5)
2. Connect the Audio Precision (AP) analyzer signal generator output to X1 and X3. Use Balanced connection with Zout ≤ 20Ω.
3. Connect the Power Supply Daughter Card (PSDC) on the mother board.
4. Initially set the voltage of the dual power supplies to ±103.5V with current limit of 0.3A. Make sure the output of the power supply is off.
5. Connect the power to X11 = +B, GND, -B (±103.5V, current limit = 300mA).
6. Make sure switch S2 is in the OFF position.

4.2 Power-up sequence

1. Turn on the ±103.5V power supply at the same time. All the Green LEDs on the PSDC should light up.
2. Flip S2 switch to the ON position. Also flip S5, S6 to the ON position to turn on CH1 and CH2. Red LEDs, LD1 and LD2, should turn off.
3. The power supply should read ±103.5V and 90 mA (±10mA), 140 mA (±10mA)

4.3 Functionality audio tests

1. With AP no filter set in the analyzer (>500kHz setting), monitor the channel's switching frequency on the AP's analog analyzer.
2. Set S3 and S4 to disable Clock injection for CH1 and CH2.
3. Disable CH2 by adjusting S6 to OFF position. Switch S5 to ON position to turn ON CH1. Read the frequency on AP's analog analyzer. If the frequency is not 317kHz ± 5kHz , then adjust VR1 on the board to self-oscillation frequency of 317kHz ± 5kHz.
4. Disable CH1 by adjusting S5 to OFF position. Switch S5 to ON position to turn ON CH2. Read the frequency on AP's analog analyzer. If the frequency is not 317kHz ± 5kHz , then adjust VR3 on the board to self-oscillation frequency of 317kHz ± 5kHz.
5. Set AP's analog analyzer to 20kHz AES17 filter. It is also recommended to introduce the AUX-0025 filter in the setup only at this stage as shown in Figure 5. If the AUX-0025 filter is added before this step, the audio analyzer will not be able to accurately detect the self-oscillation frequency.
6. Connect audio signal from AP to X1 and X3.
7. To measure the audio ouputs of the board, use the balanced inputs at the AP and connect them across output terminals, X6 and X12.
8. Connect AP frame ground to GND at terminal X11.
9. Set up the AP to sweep the audio signal voltage from 15mV$_{RMS}$ to 2.6V$_{RMS}$. (Before running this sweep, please increase the current limits for ±103.5V supplies to 30A. Additionally, if the supply hits current limit, then it is recommended to change the AP generator setting to inverted CH2 output to reduce ripple current on the supply.)
10. Run AP THD+N vs Power test as shown in Figure 5.

4.4 On-board clock function

1. With AP no filter (>500 kHz), monitor the channel's switching frequency on the AP's analog analyzer.
2. Set S3 and S4 to disable Clock injection for CH1 and CH2.
3. Disable CH2 by adjusting S6 to OFF position. Switch S5 to ON position to turn ON CH1. Read the frequency on AP's analog analyzer. If the frequency is not 317kHz ± 5kHz , then adjust VR1 on the board to self-oscillation frequency of 317kHz ± 5kHz.
4. Disable CH1 by adjusting S5 to OFF position. Switch S5 to ON position to turn ON CH2. Read the frequency on AP's analog analyzer. If the frequency is not 317kHz ± 5kHz , then adjust VR3 on the board to self-oscillation frequency of 317kHz ± 5kHz.
5. Set S3 and S4 to ENABLE position in order to enable the on-board clock oscillator injection.
6. Adjust VR2 on the board to change the clock frequency. Monitor the clock frequency by reading the frequency on AP's analog analyzer panel. Adjust the clock frequency to 305kHz± 2kHz.
7. Set AP's analog analyzer to 20 kHz AES17 filter. It is also recommended to introduce the AUX-0025 filter in the setup only at this stage as shown in Figure 5. If the AUX-0025 filter is added before this step, the audio analyzer will not be able to accurately detect the self-oscillation frequency.
8. Connect audio signal from AP to X1 and X3.
9. Set up the AP to sweep the audio signal voltage from 15 mVRMS to 2.6 VRMS. (Before running this sweep, please increase the current limits for ±103.5V supplies to 28A-30A. Additionally, if the supply hits current limit, then it is recommended to change the AP generator setting to output inverted CH2 to reduce ripple current on the supply.)
10. Run AP THD+N vs Power test as shown in Figure 5. The obtained results should look similar to Figure 6.

4.5 Power-down sequence

1. Flip S5, S6 to the OFF position to turn off CH1 and CH2. Red LEDs, LD1 and LD2, should turn on. Flip S1 switch to the off position.
2. Turn off the ±103.5V power supply. Note that when turning off the power supply, please turn them off simultaneously. In case only the positive supply is turned off, a loud sweeping noise can be expected on the speakers. This does not damage the board but it is unpleasant.
3. Green LEDs on the Power Supply Daughter Card turn off after a short delay.

5 Performance and test graphs

5.1 THD+N vs Power

Measurements for 4Ω and 8Ω are taken after modifications suggested in section 11.3.

5.1.1 2Ω

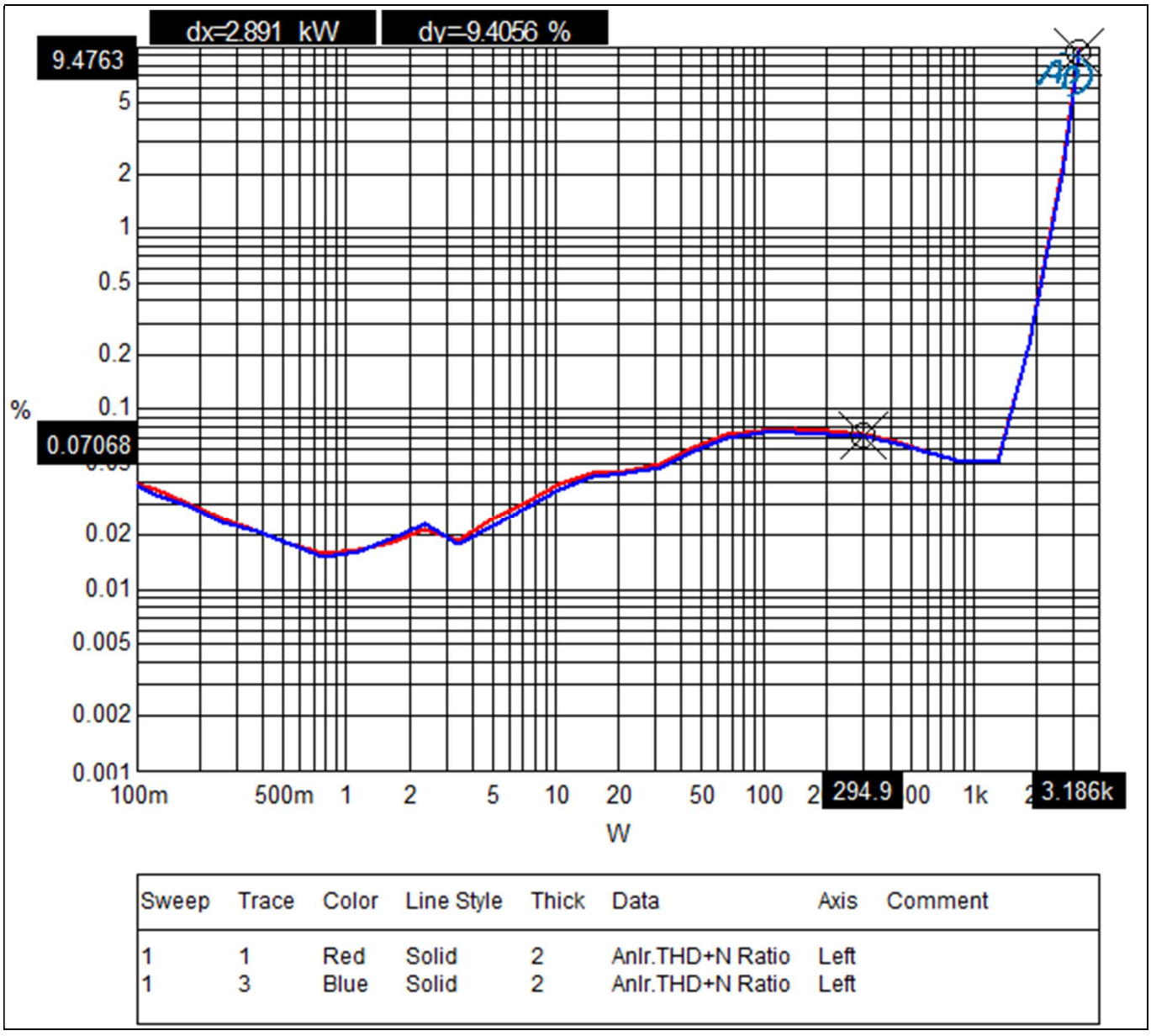
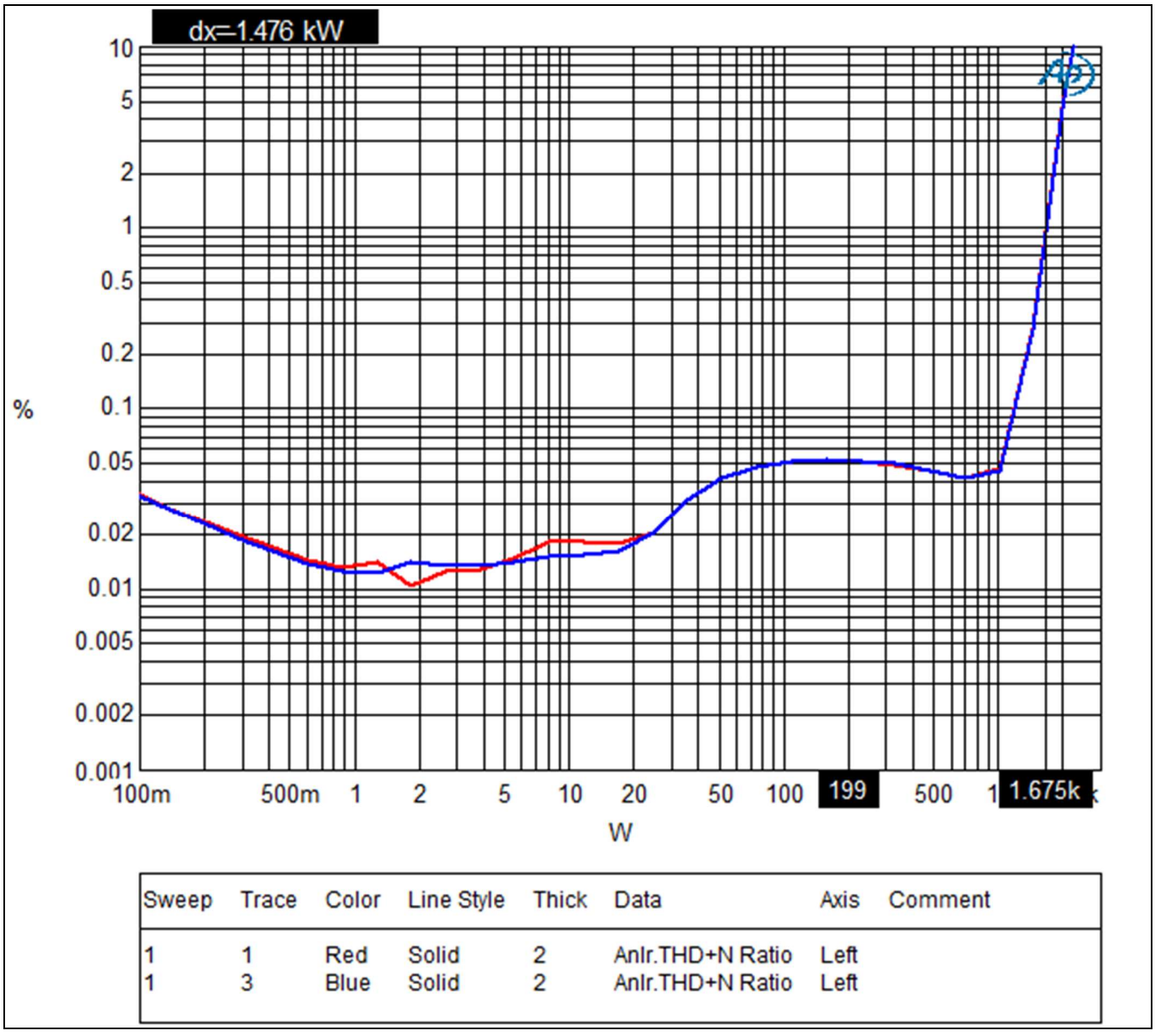


Figure 6 THD+N vs Power sweep for CH1 and CH2 with clock injection

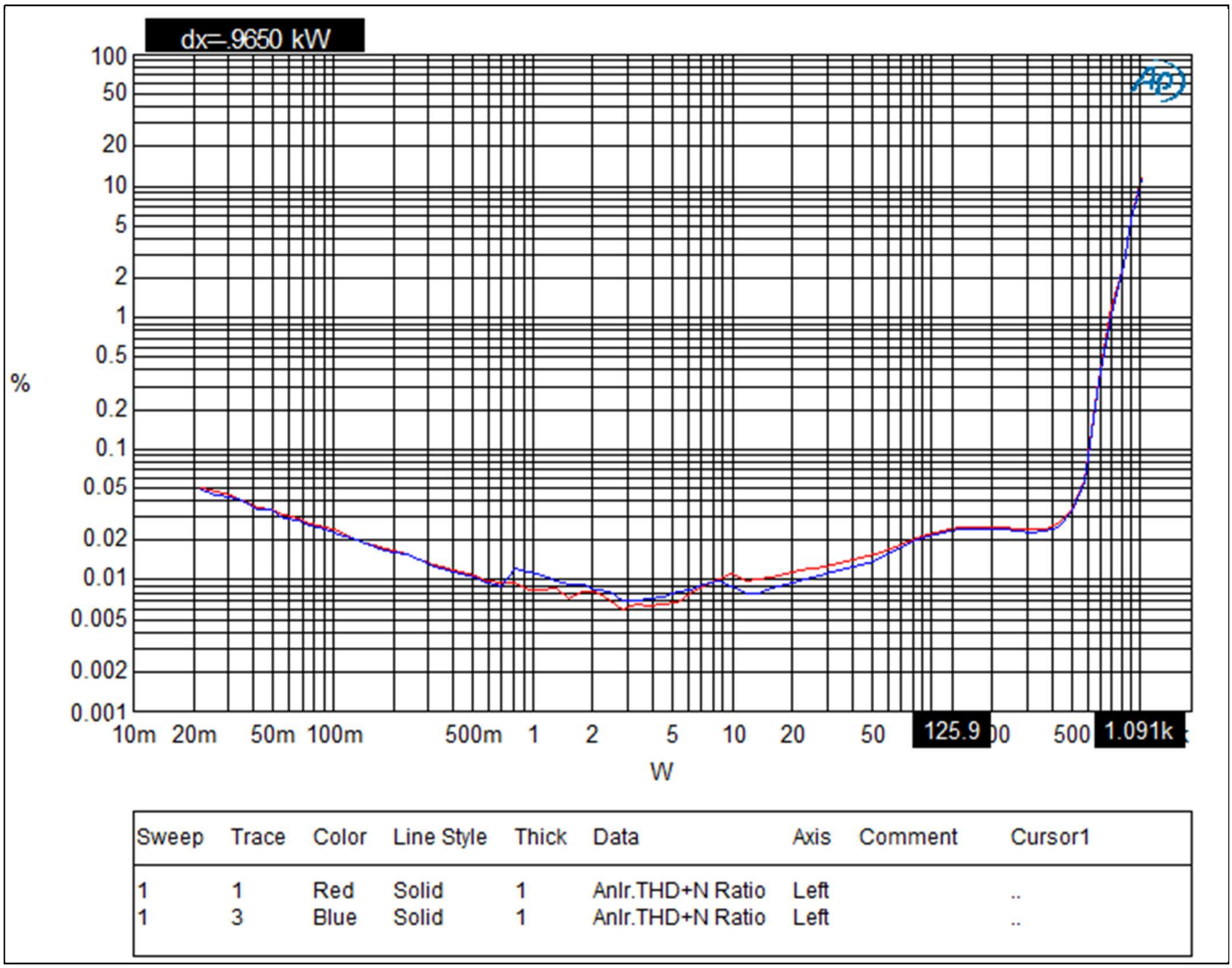
5.1.2 4Ω



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	
1	3	Blue	Solid	2	Anlr.THD+N Ratio	Left	

Figure 7 THD+N vs Power sweep for CH1 and CH2 with clock injection

5.1.3 8Ω

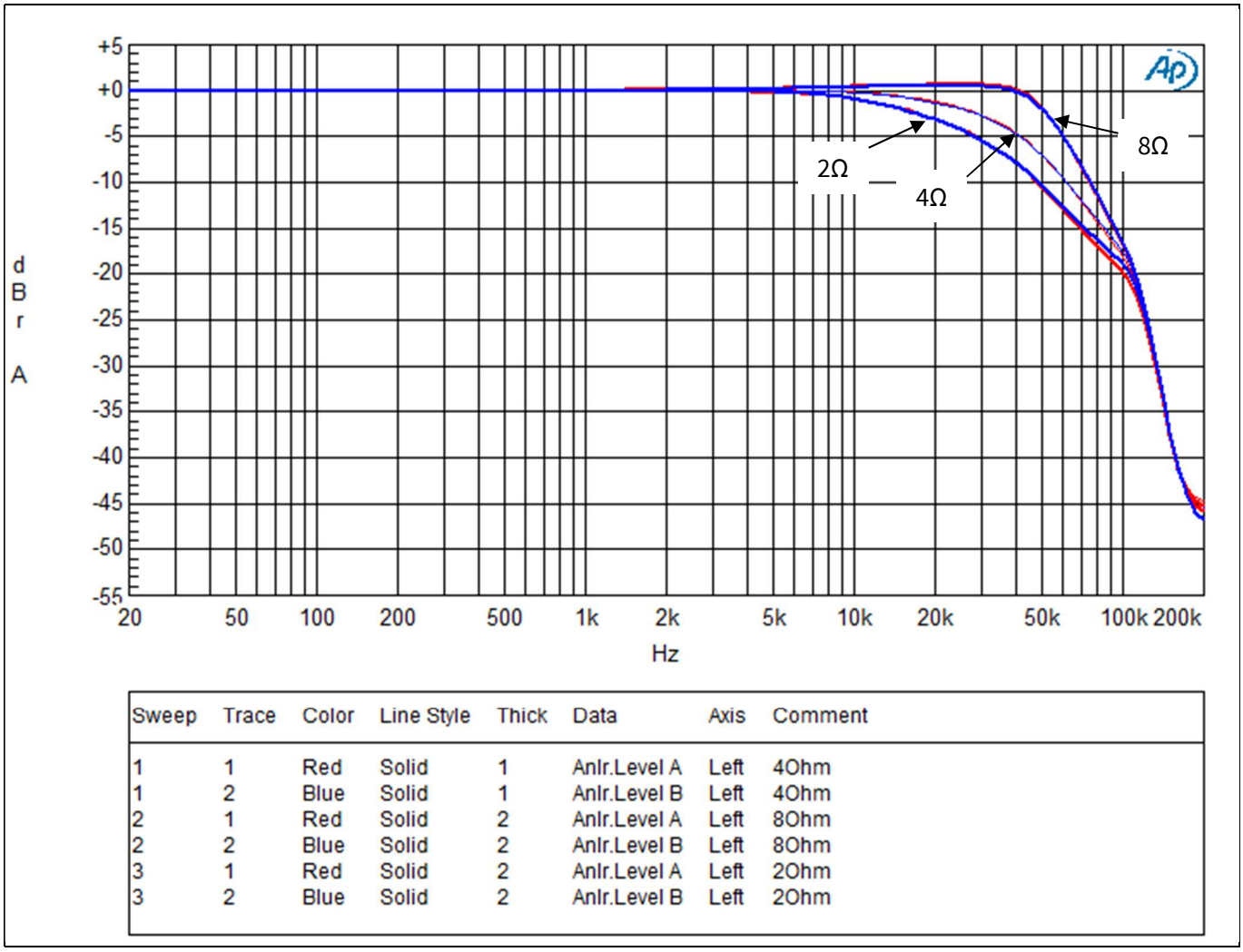


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Red	Solid	1	Anlr.THD+N Ratio	Left		..
1	3	Blue	Solid	1	Anlr.THD+N Ratio	Left		..

Figure 8 THD+N vs Power sweep for CH1 and CH2 with clock injection

5.2 Frequency response

Measurements for 4Ω and 8Ω are taken after modifications suggested in section 11.3.



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	AnIr.Level A	Left	4Ohm
1	2	Blue	Solid	1	AnIr.Level B	Left	4Ohm
2	1	Red	Solid	2	AnIr.Level A	Left	8Ohm
2	2	Blue	Solid	2	AnIr.Level B	Left	8Ohm
3	1	Red	Solid	2	AnIr.Level A	Left	2Ohm
3	2	Blue	Solid	2	AnIr.Level B	Left	2Ohm

Figure 9 Frequency response sweep for 2Ω, 4 Ω and 8 Ω load for CH1 and CH2

5.3 Noise floor

Measurements for 4Ω and 8Ω are taken after modifications suggested in section 11.3.

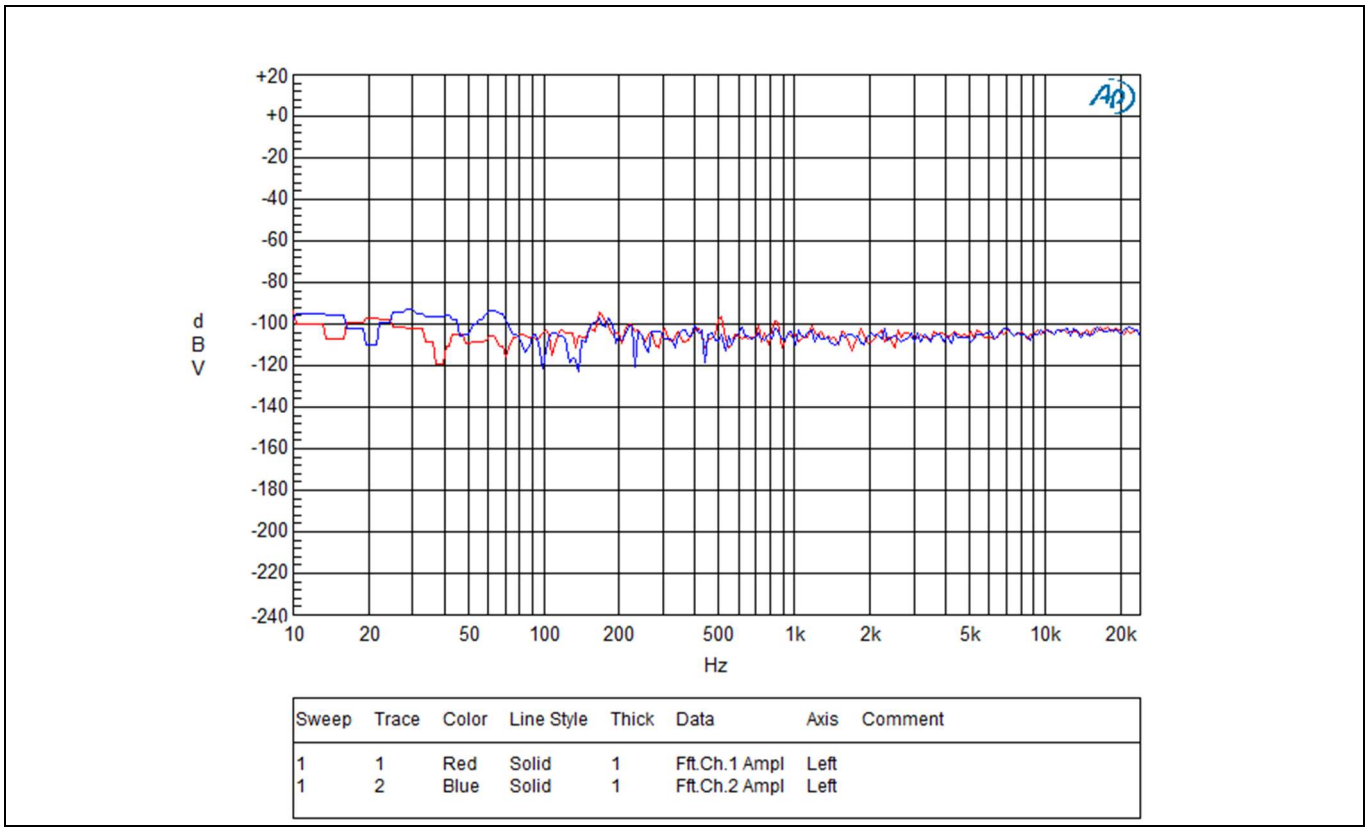


Figure 10 Noise floor with clock injection and both CH1 and CH2 active for 2Ω load

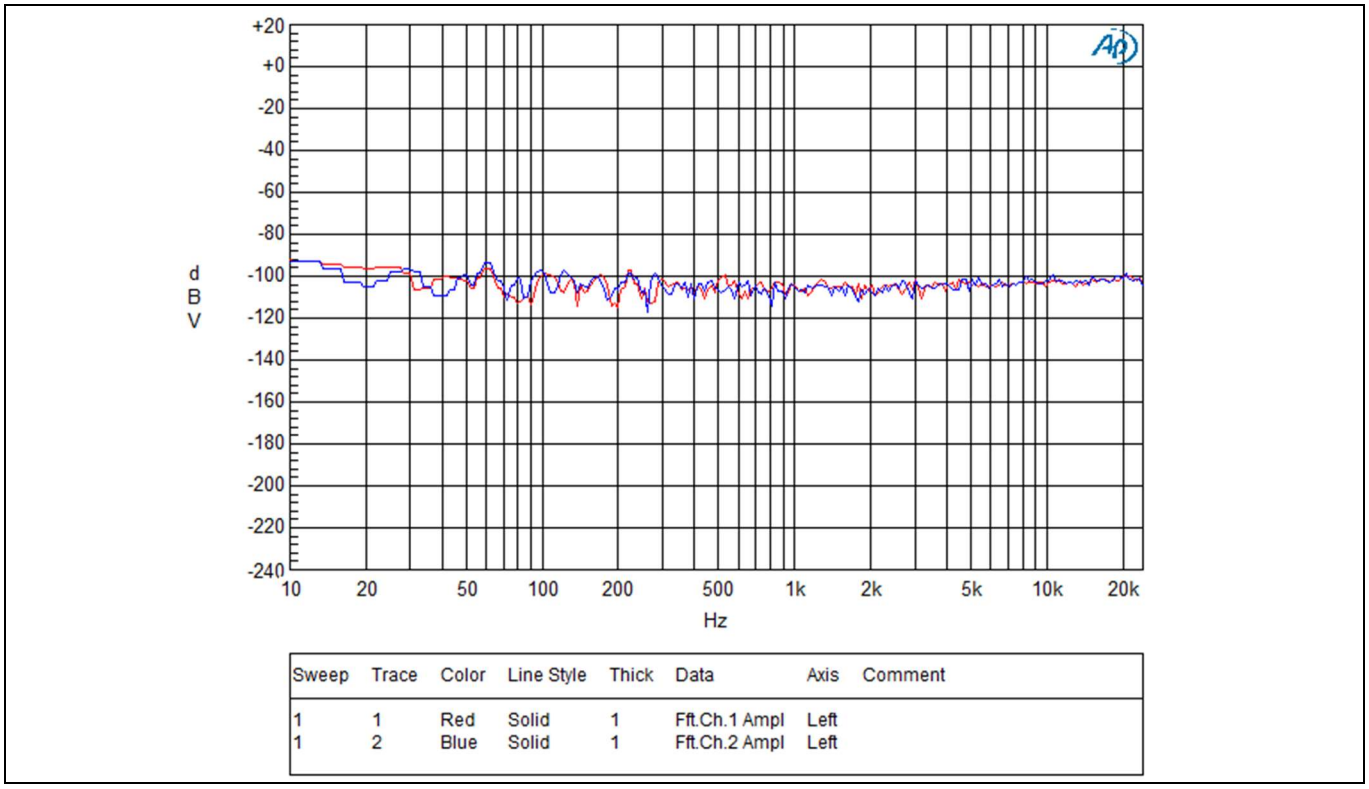


Figure 11 Noise floor with clock injection and both CH1 and CH2 active for 4Ω load

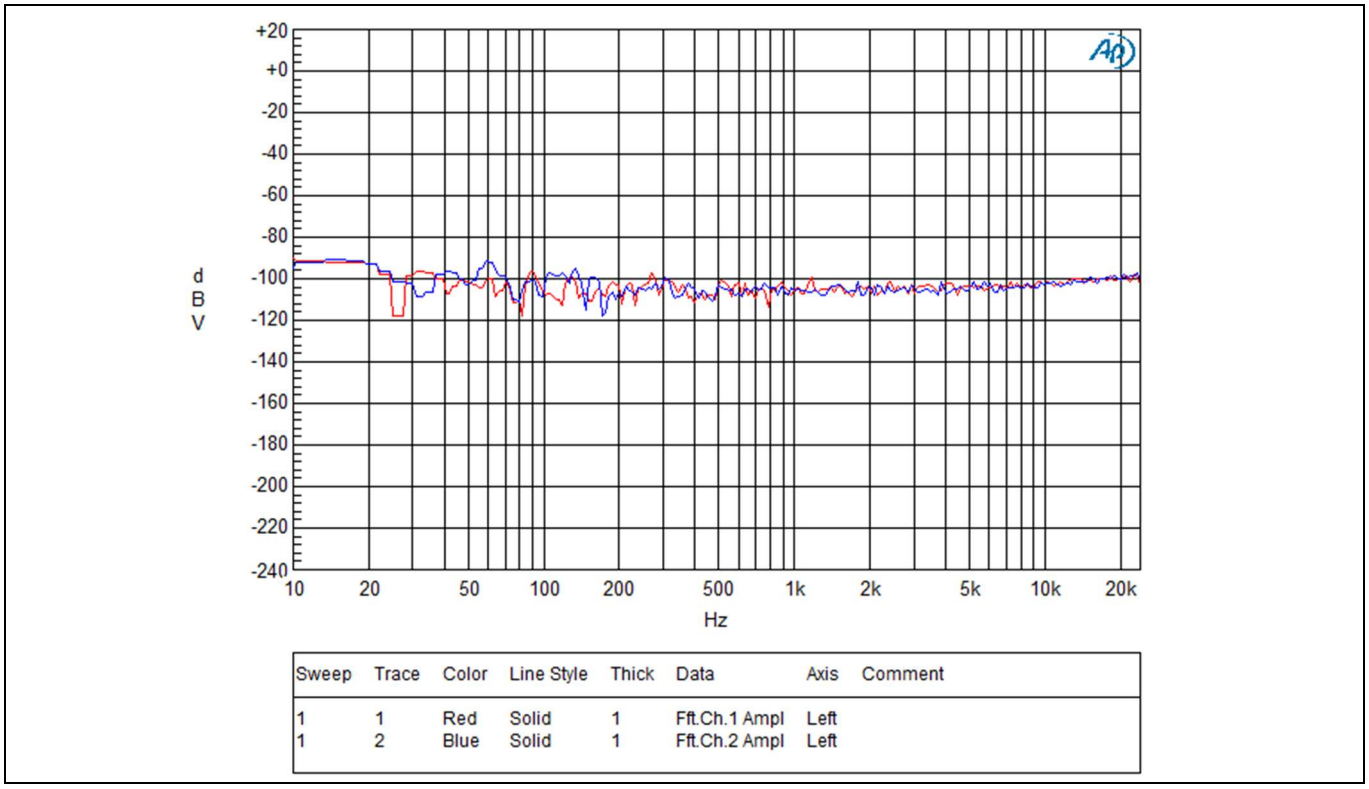


Figure 12 Noise floor with clock injection and both CH1 and CH2 active for 8Ω load

5.4 Noise floor with 1Vrms output

Measurements for 4Ω and 8Ω are taken after modifications suggested in section 11.3.

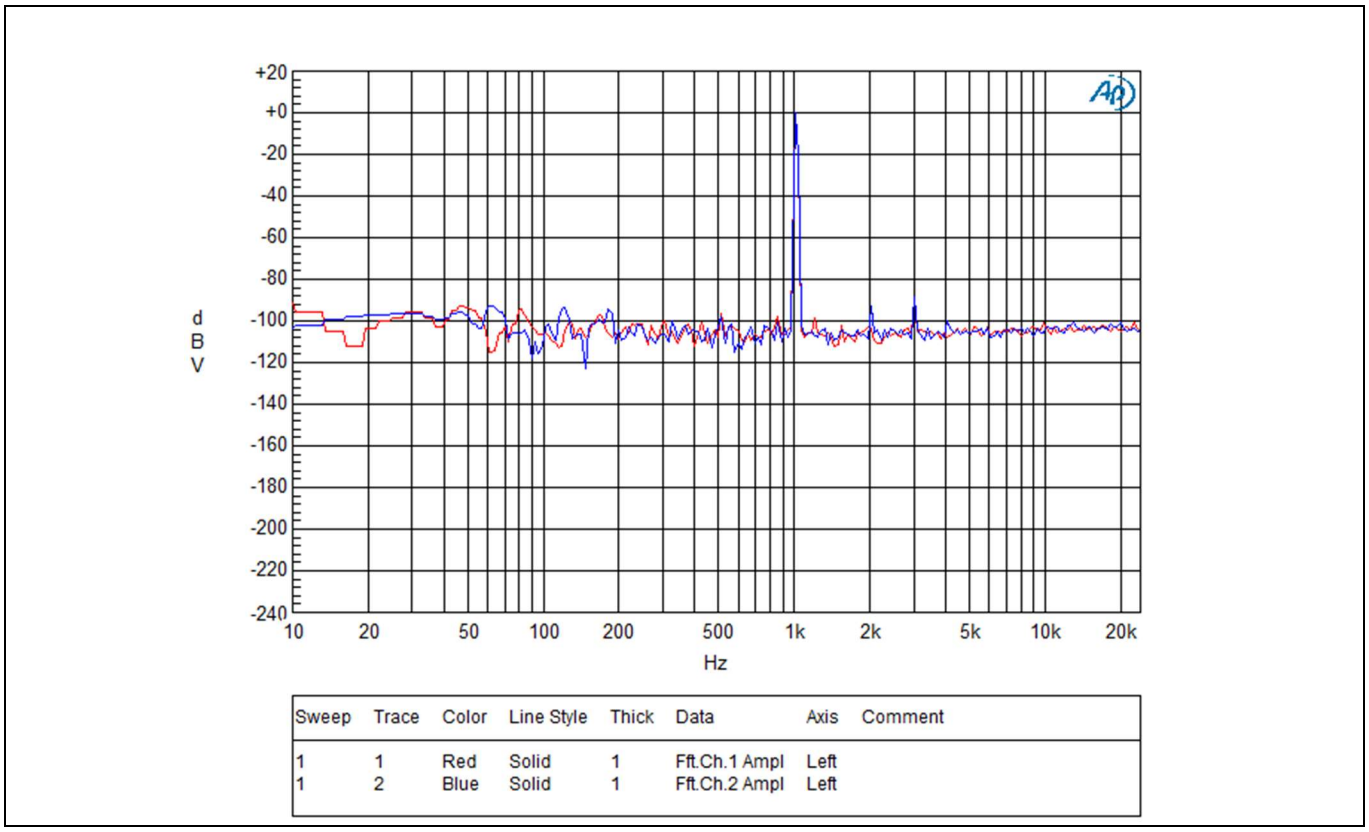


Figure 13 Noise floor with 1Vrms output for 2Ω load with both CH1 and CH2 active

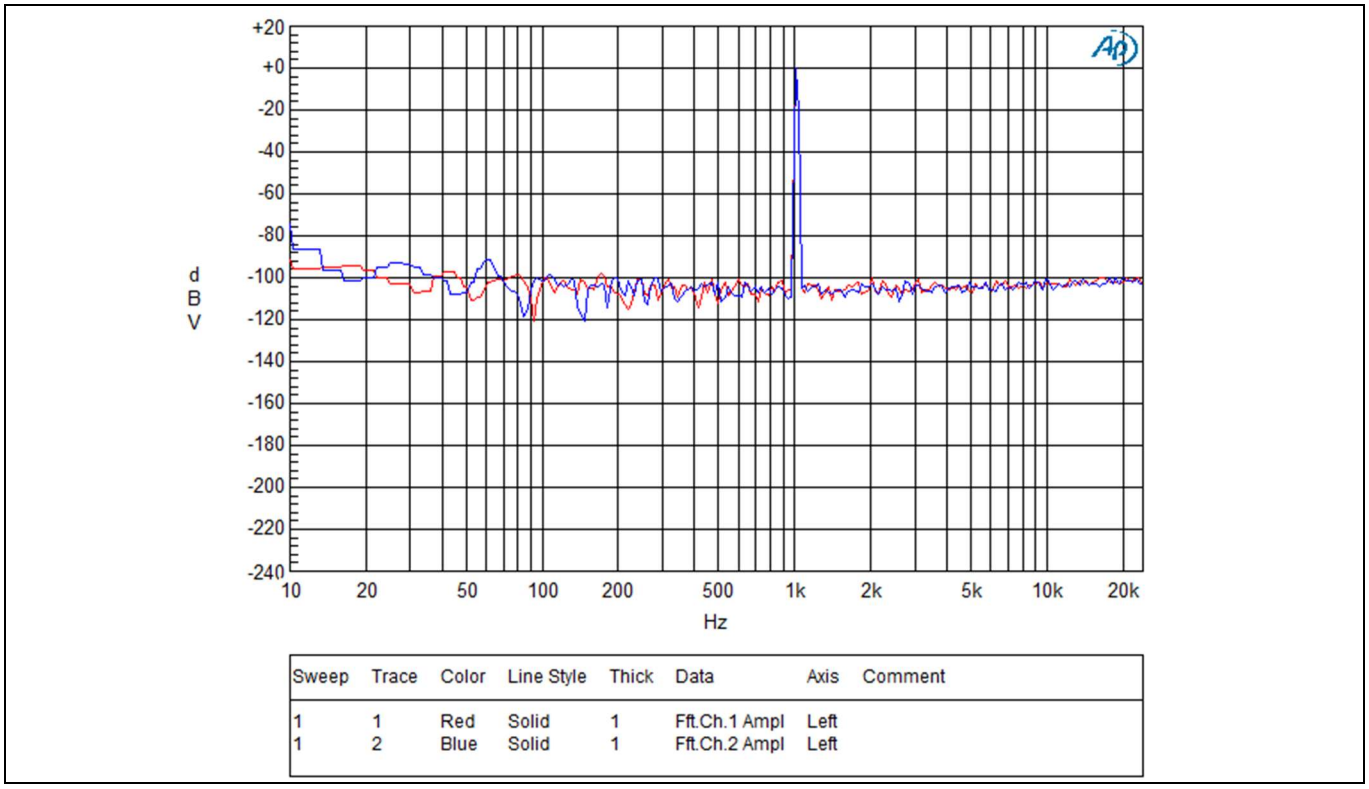


Figure 14 Noise floor with 1Vrms output for 4Ω load with both CH1 and CH2 active

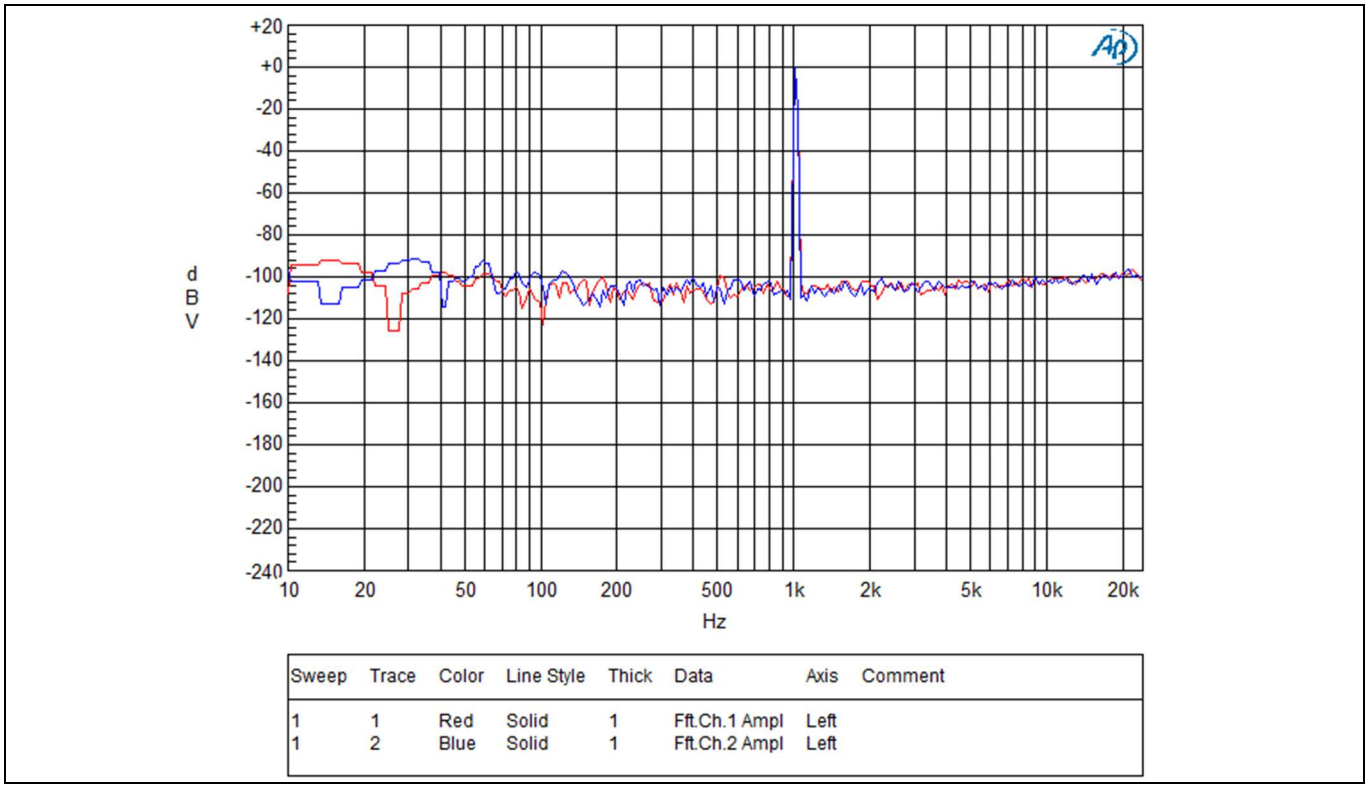


Figure 15 Noise floor with 1Vrms output for 8Ω load with both CH1 and CH2 active

6 Over-current protection (OCP) test

The OCP test results are obtained by shorting the load. It should be noted that below a certain output voltage, depending on the total stray or parasitic resistance, OCP will not be triggered. For such output voltage levels, the output current is limited by the stray resistance and is below OCP limit set by the resistive divider. In such cases, the output short condition cannot be detected by OCP immediately. Once the MOSFET temperature rises and correspondingly OCP limit naturally falls, eventually the output short condition will be detected as an OCP event. This operating condition is left for the reader to consider and design for.

For the test, the output voltage was set to 13Vrms (85W @2Ohm).

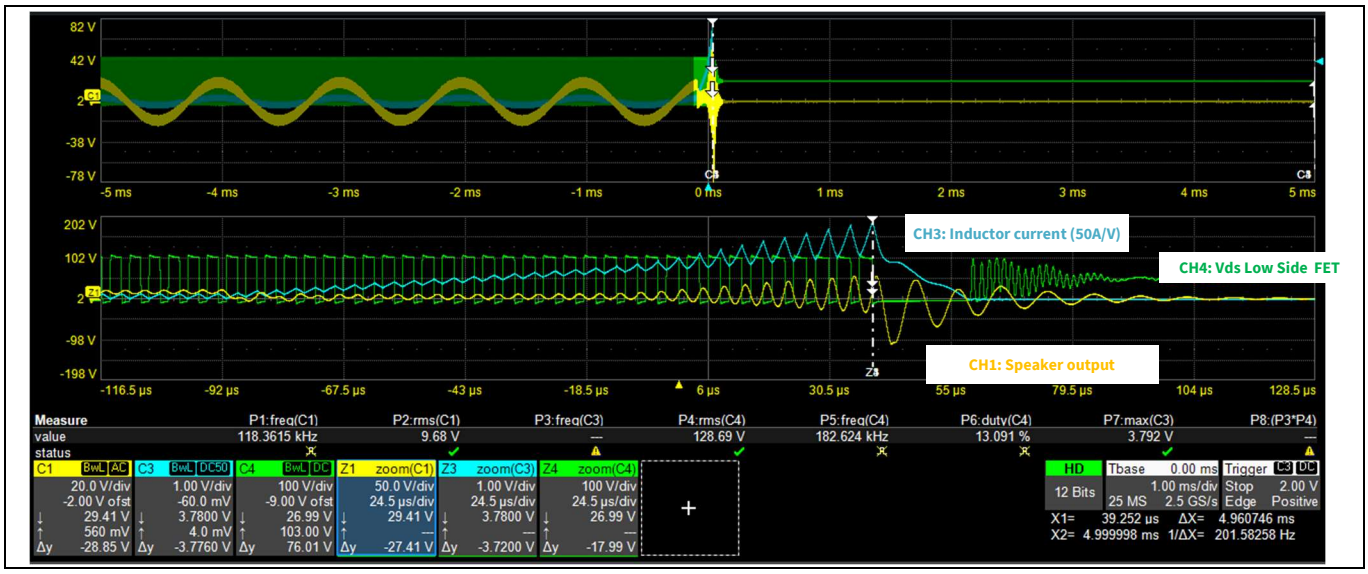


Figure 16 OCP in the positive cycle

As shown in Figure 16 , OCP is trigerred at ~189A in the positive cycle.

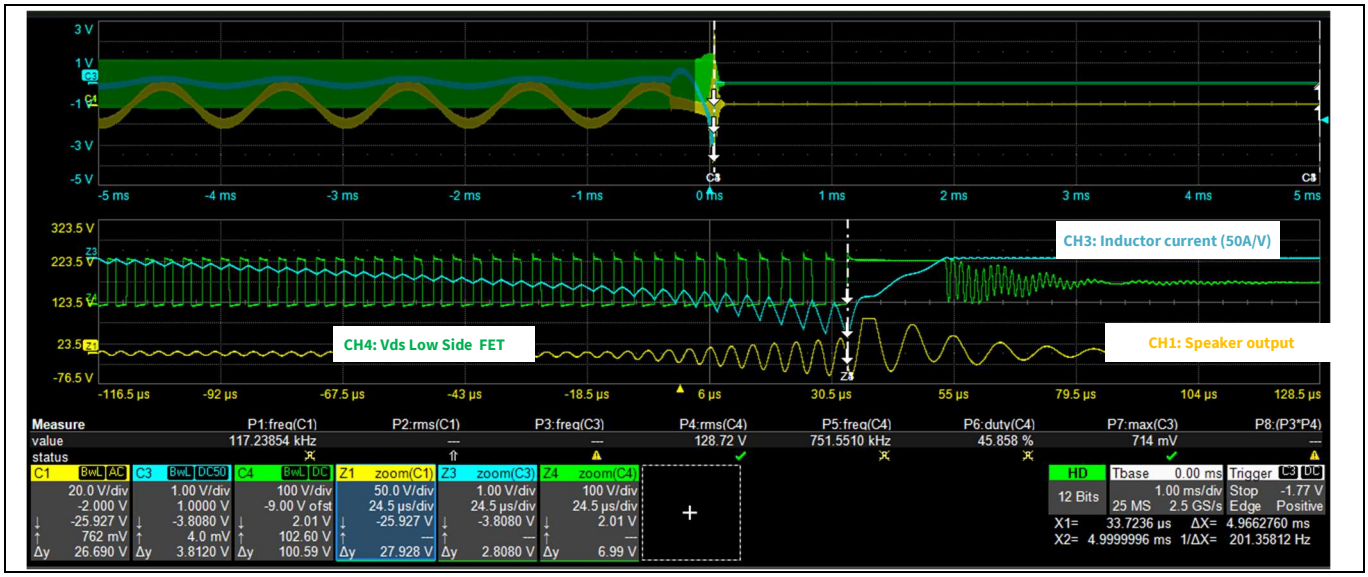


Figure 17 OCP in the negative cycle

As shown in Figure 17, OCP is triggered at 190A in the negative cycle.

7 Thermal information

7.1 Peak power duration thermal information

The thermal performance of the design was tested at rated power and the measured data has been shown below. Please note that in all these tests, both channels were active.

A low thermal resistance thermal interface pad (Laird, p.n. # A15037003) was used for these tests.

Measurements for 4Ω and 8Ω are taken after modifications suggested in section 11.3.

Table 6

Load Z	Pout @1% THD (in W)	Duration
2Ω	2500W	>1 min, no thermal shutdown at $T_{HEATSINK}$ = 51°C
4Ω	1600W	>1 min, no thermal shutdown at $T_{HEATSINK}$ = 47°C
8Ω	900W	>1 min, no thermal shutdown at $T_{HEATSINK}$ = 32°C

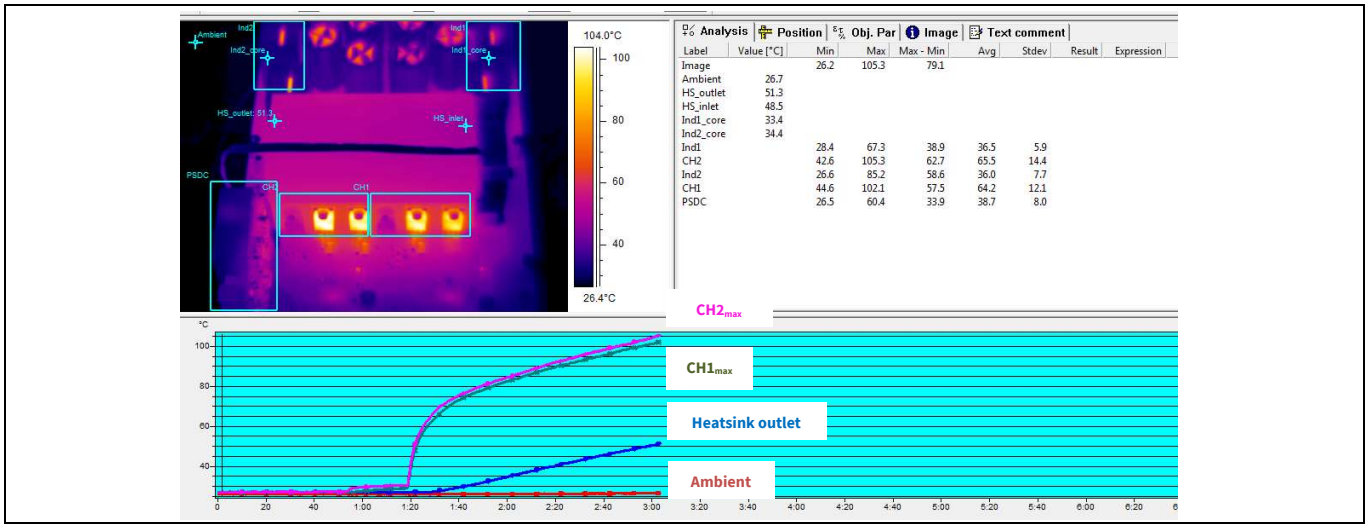


Figure 18 2Ω load - Max MOSFET case temperature 106°C at 100 seconds, Tambient = 27°C

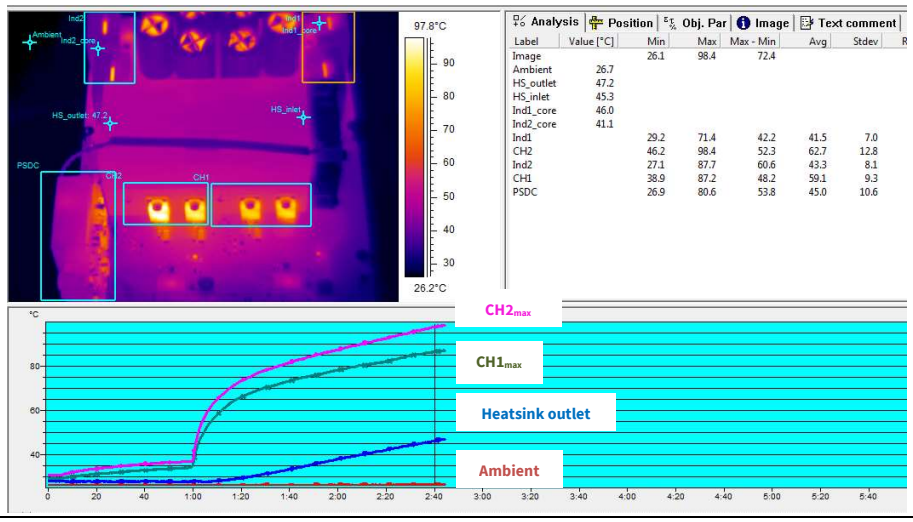


Figure 19 **4Ω load - Max MOSFET case temperature 99^{0}C at 100 seconds, Tambient = 27^{0}C**

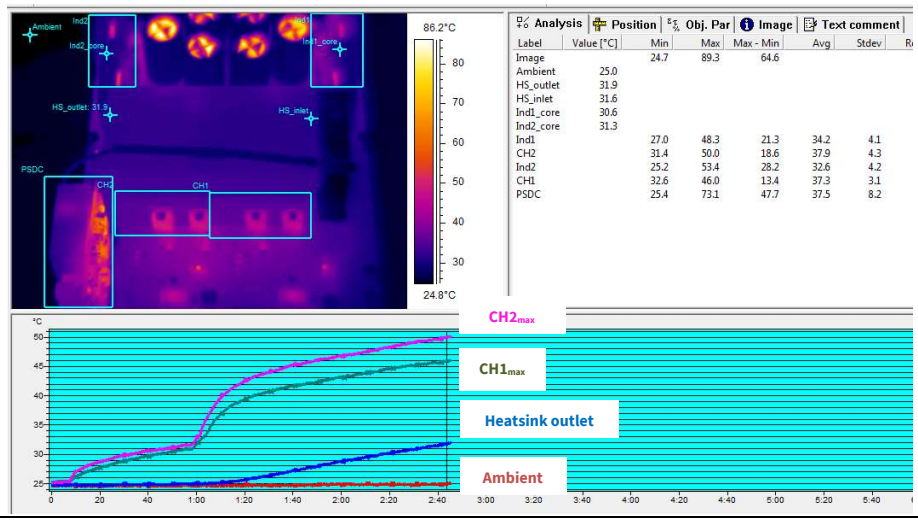


Figure 20 **8Ω load - Max MOSFET case temperature 50^{0}C at 100 seconds, Tambient = 27^{0}C**

7.2 1/8th clipping power duration thermal information

The thermal performance of the design was tested at 1/8th clipping power and the measured data has been shown below. Please note that in all these tests, both channels were active.

A low thermal resistance thermal interface pad (Laird, p.n. # A15037003) was used for these tests.

Measurements for 4Ω and 8Ω are taken after modifications suggested in section 11.3.

Table 7

Load Z	Pout/8 (in W)	Duration
2Ω	313W	>30 min, no thermal shutdown at $T_{HEATSINK}$ = 70^{0}C

Load Z	Pout/8 (in W)	Duration
4Ω	200W	>30 min, no thermal shutdown at $T_{HEATSINK}$ = 64°C
8Ω	113W	>30 min, no thermal shutdown at $T_{HEATSINK}$ = 41°C

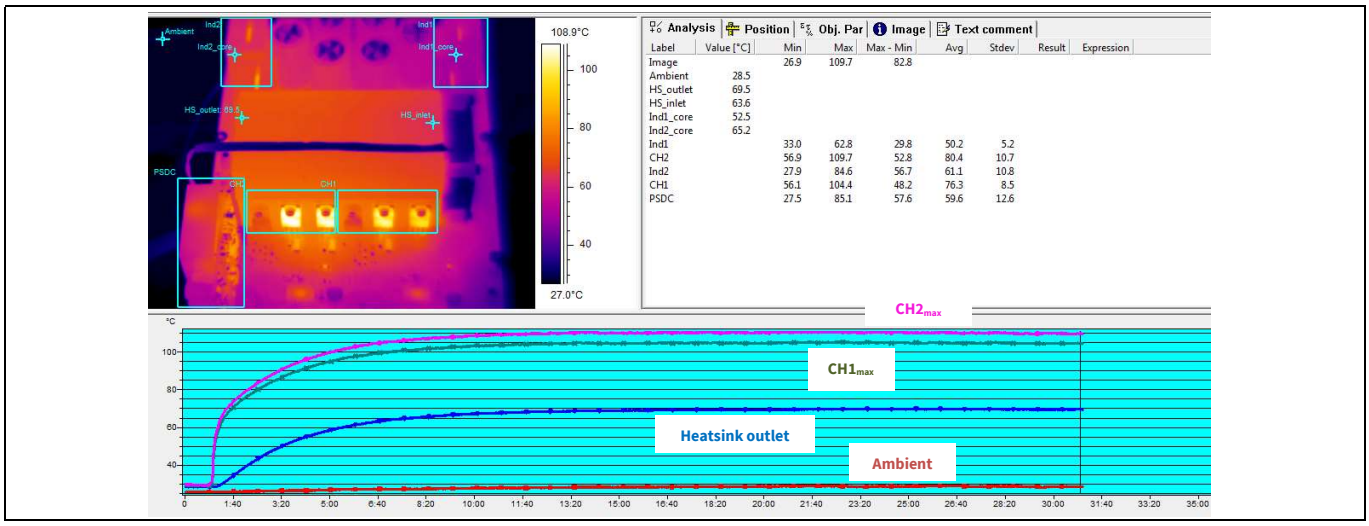


Figure 21 2Ω load - Max MOSFET case temperature 110°C at 30minute, Tambient = 28.5°C

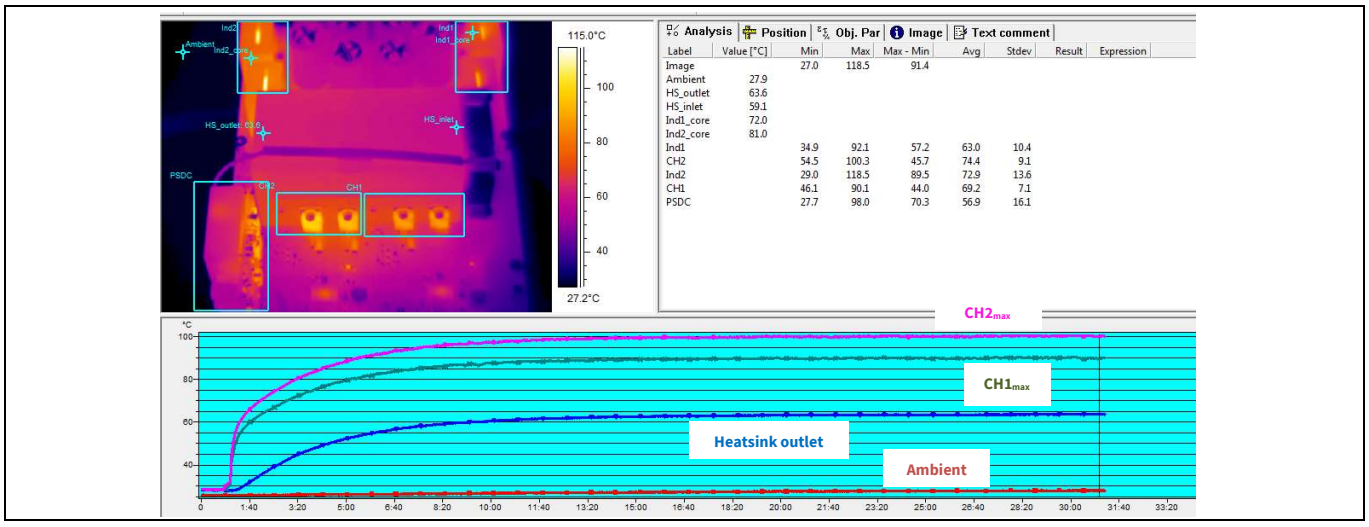


Figure 22 4Ω load - Max MOSFET case temperature 101°C at 30minute, Tambient = 28°C

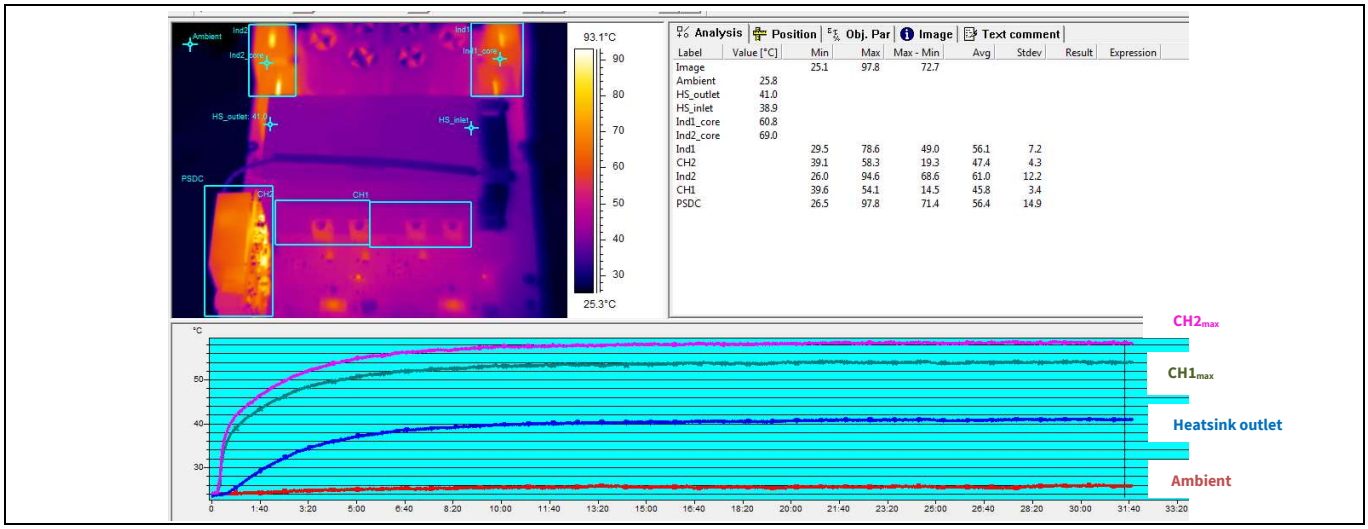


Figure 23 8Ω load - Max temperature 58^{0}C at 30minute, Tambient = 25.8^{0}C

7.3 Heatsink information

An off the shelf heatsink, LAM 5 K 100 24 or LAM 5 100 24, has been chosen for this design. Two mounting options are possible.

1) Heatsink clip: Several heatsink clips are available from Fischer Elektronik such as THFU2. This mounting method can only be used with LAM 5 **K** 100 24.

2) Screw mounting: Fischer Elektronik can drill the heatsink on request. You can use 36-3049-ND washer for spacing between the screw and the MOSFET metal tab and use a M3 screw to mount the TO-220 MOSFET on to the heatsink. Please aim to drill the holes in the heatsink at a height that minimizes lead length. Also take care to avoid damaging a heatsink fin when drilling the hole to prevent loss of heatsink performance.

More information on LAM 5 K 100 24 heatsink is available at this Fischer Elektronik webpage.

8 Schematics

REF_IRS2461S_5KW is a 2-channel design with a pre-amplifier and optional clock injection from an onboard clock. Additionally, the design includes optional circuits to trigger over-voltage protection (OVP) and under-voltage protection (UVP) by monitoring the negative DC rail (B-) and DC protection (DCP) by monitoring the output.

The Power Supply Daughter Card generates all the housekeeping power supplies, including a supply for heatsink fan, with only B+, B- and GND inputs.

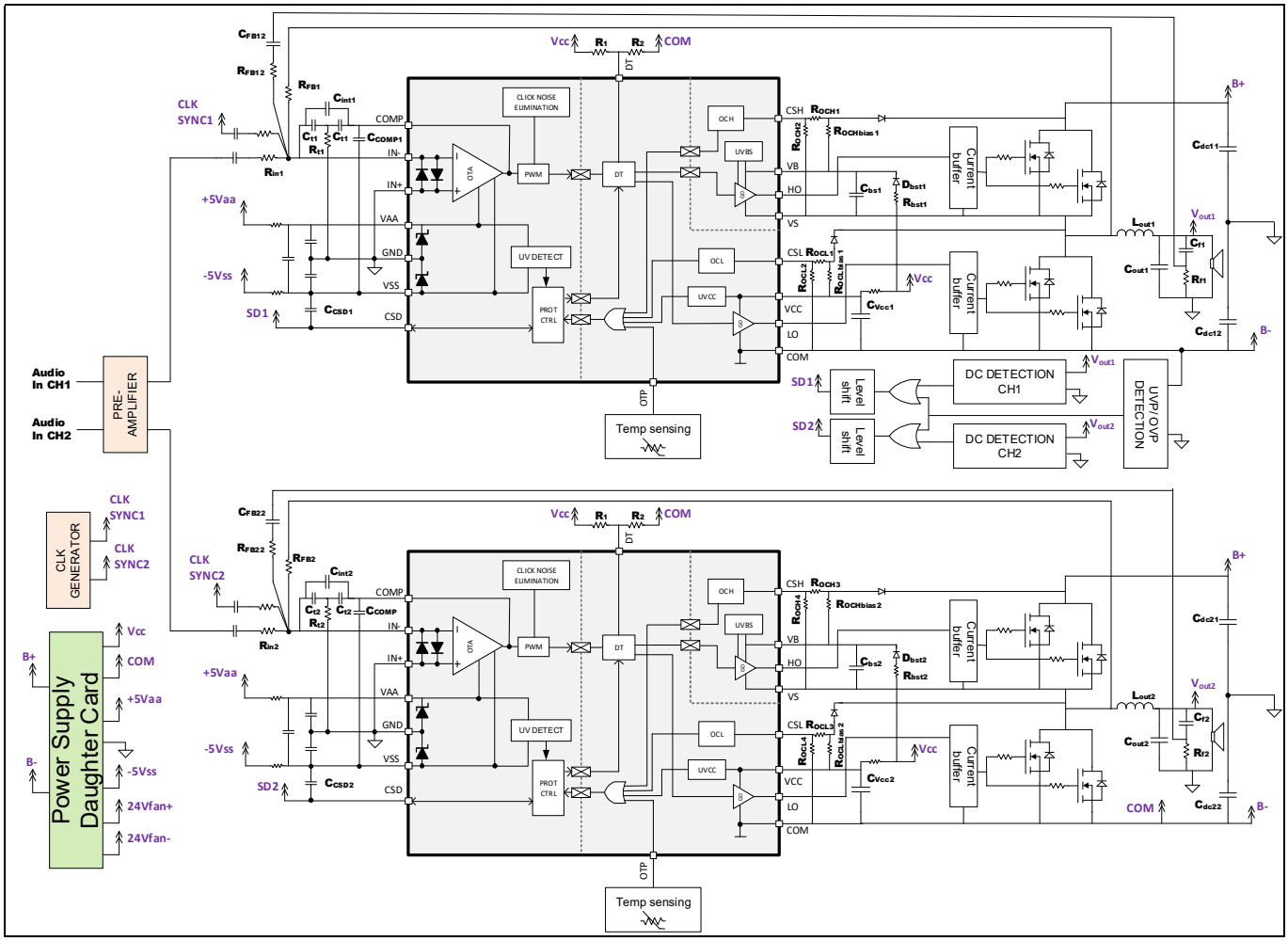


Figure 24 Simplified REF_IRS2461S_5KW schematic

The schematics are developed in Altium Designer and are available on request. The design is hierarchical in nature. The MB schematics for different sheets are shown in Figure 25 to Figure 33. The PSDC schematics is shown in Figure 34.

8.1 Mother Board (MB) schematics

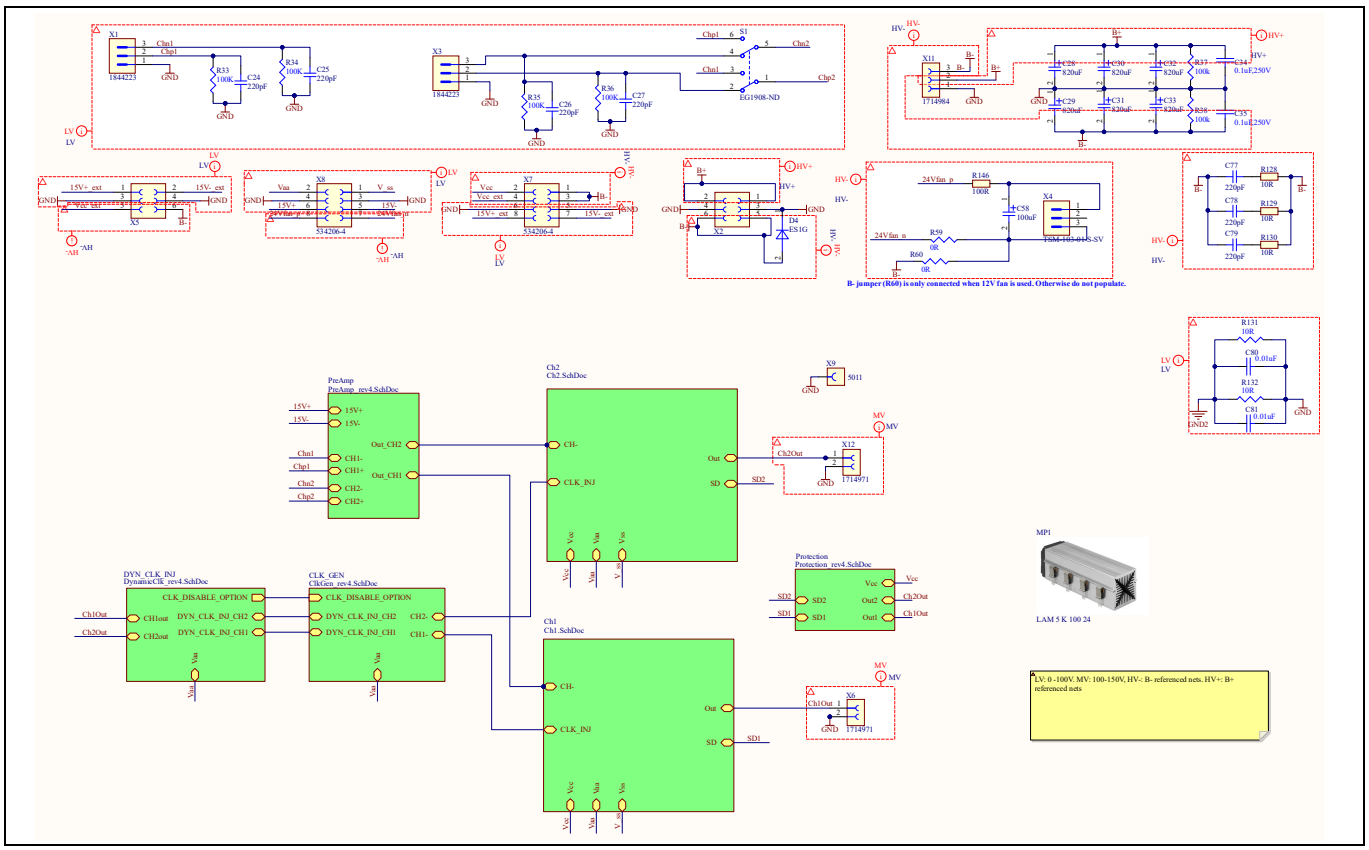


Figure 25 REF_IRS2461S_5KW Mother Board schematics – Overview

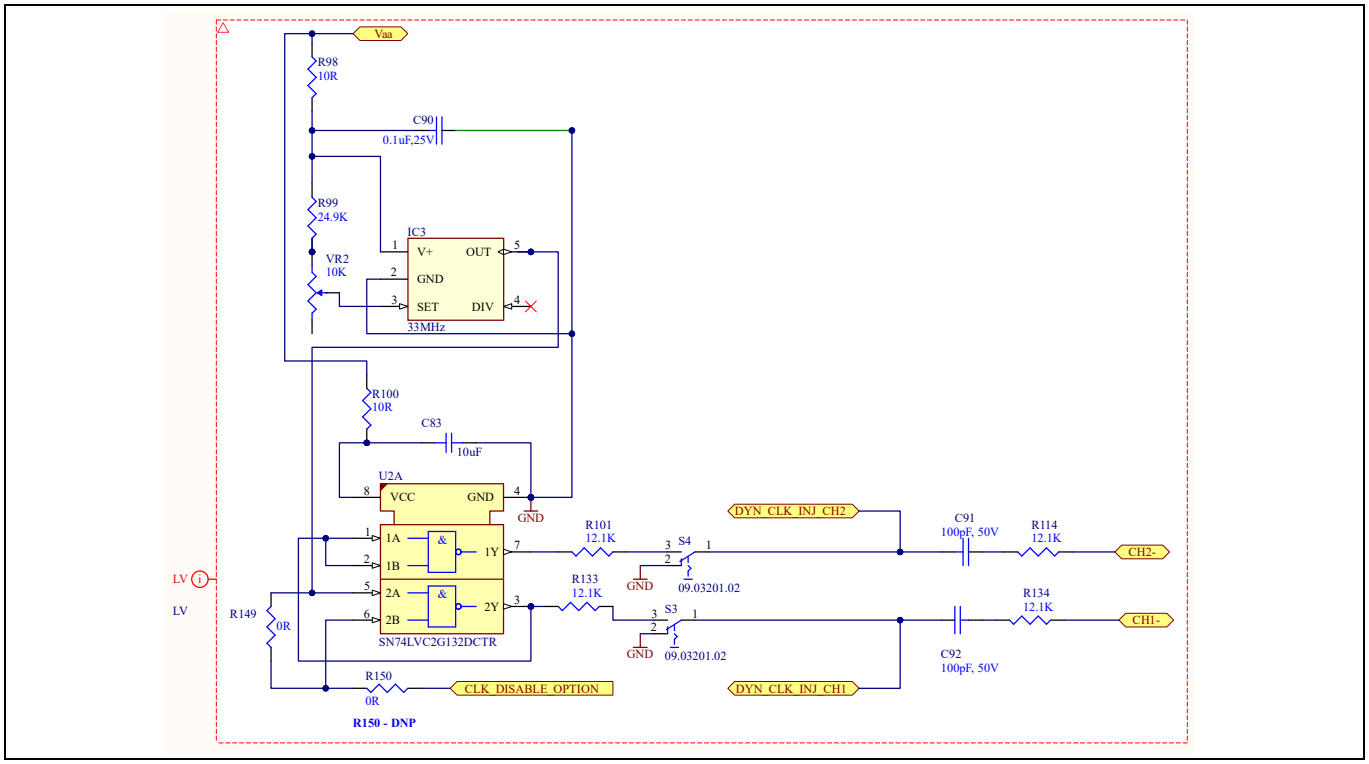


Figure 26 REF_IRS2461S_5KW Mother Board schematics – Clock generation

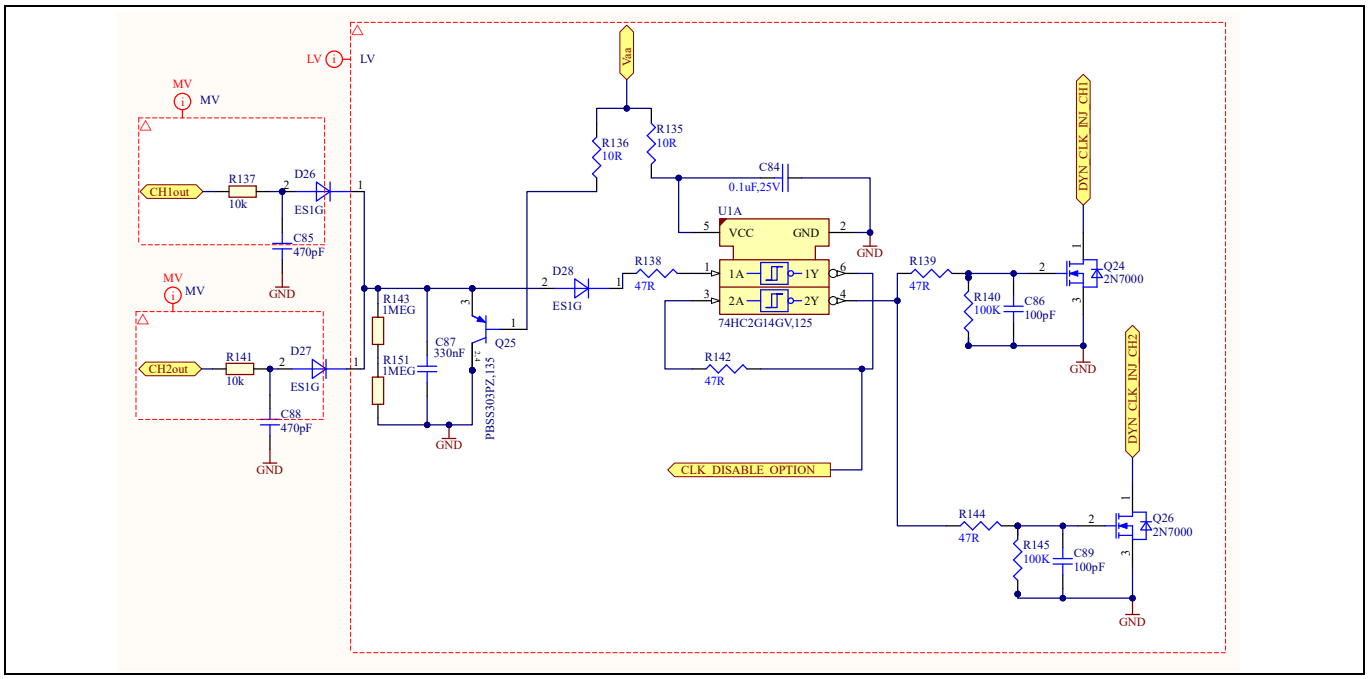


Figure 27 REF_IRS2461S_5KW Mother Board schematics – Dynamic clock injection

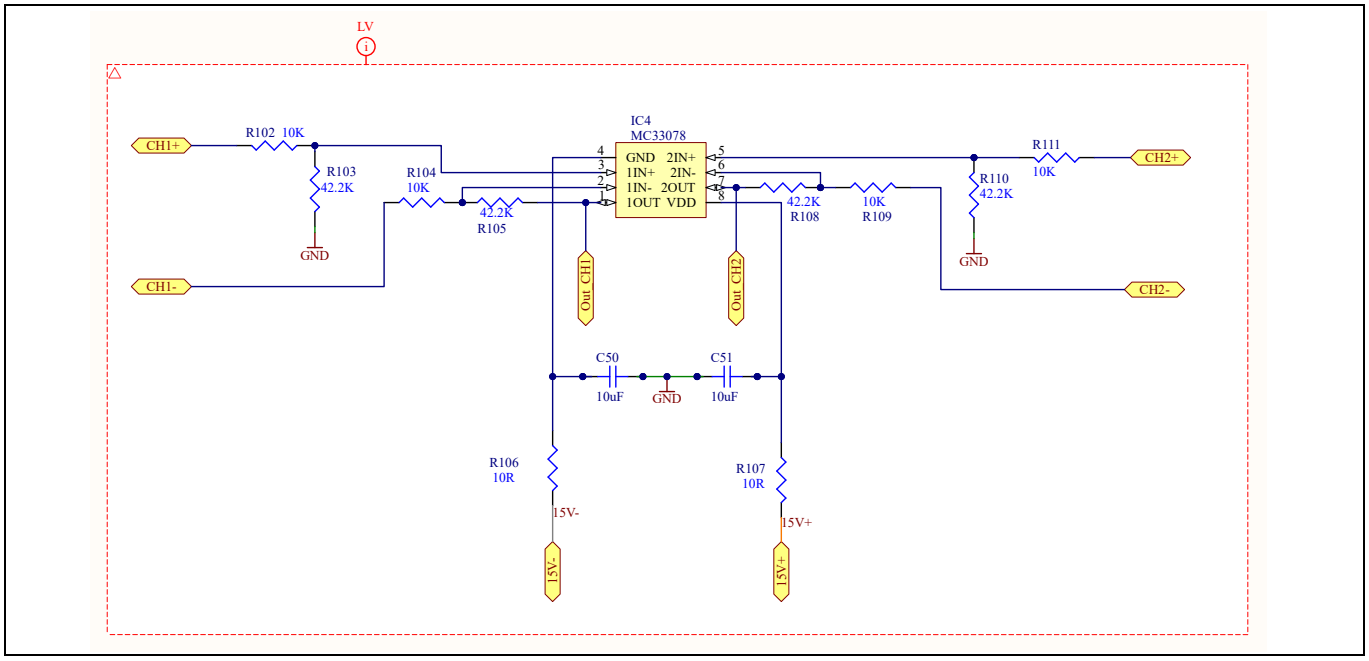


Figure 28 REF_IRS2461S_5KW Mother Board schematics – Pre-amp

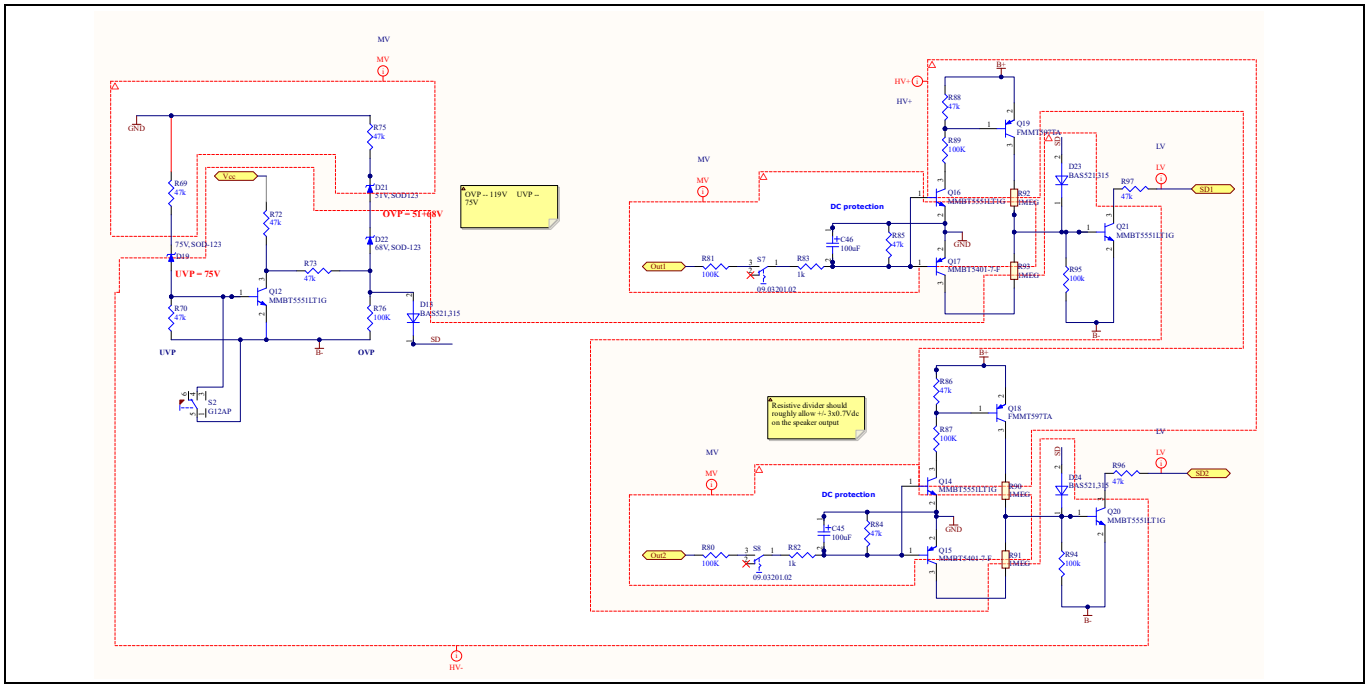


Figure 29 REF_IRS2461S_5KW Mother Board schematics – Optional UVP, OVP and DCP circuits

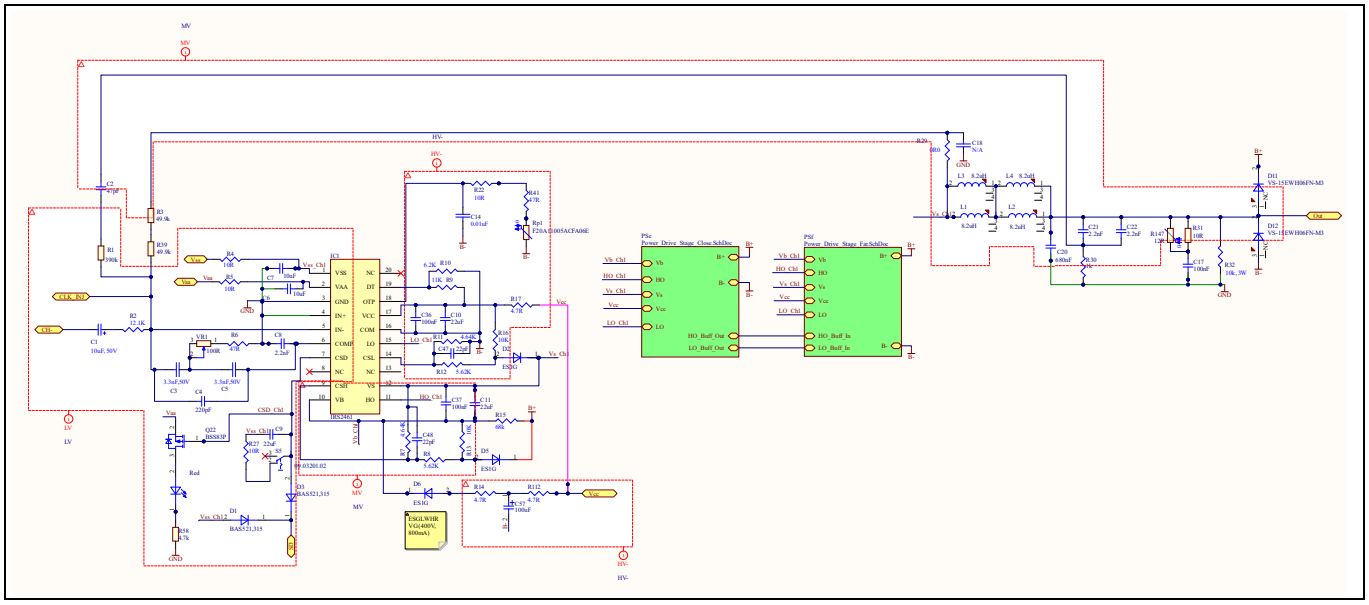


Figure 30 REF_IRS2461S_5KW Mother Board schematics – Channel 1

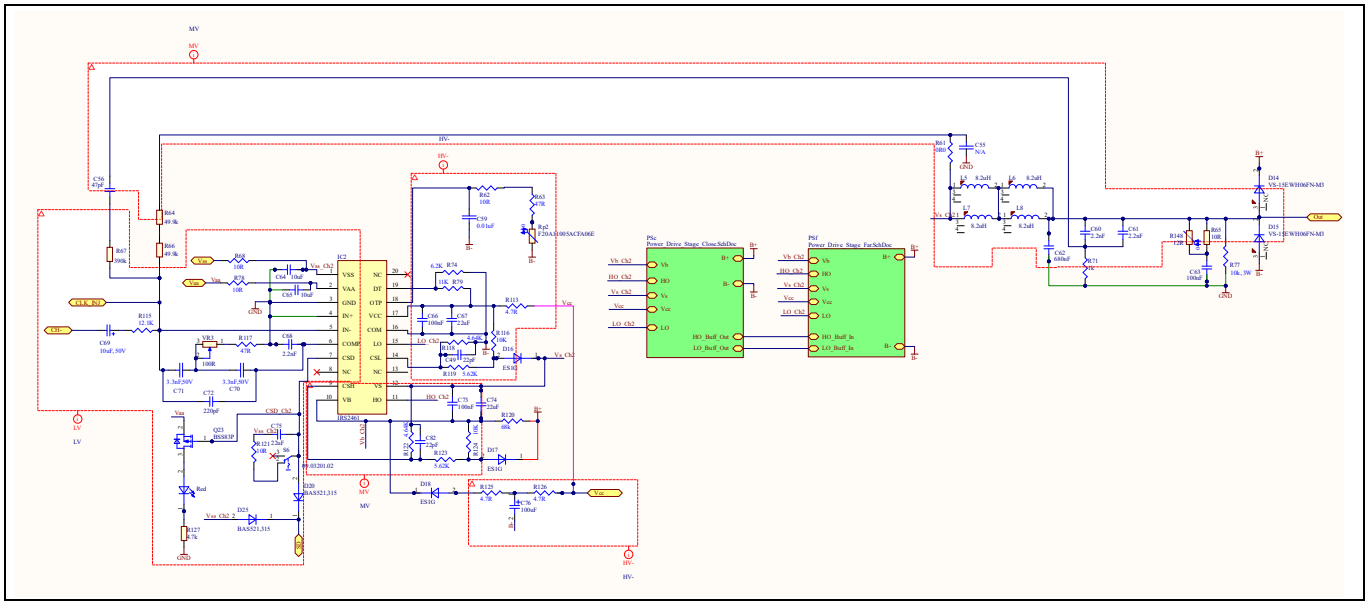


Figure 31 REF_IRS2461S_5KW Mother Board schematics – Channel 2

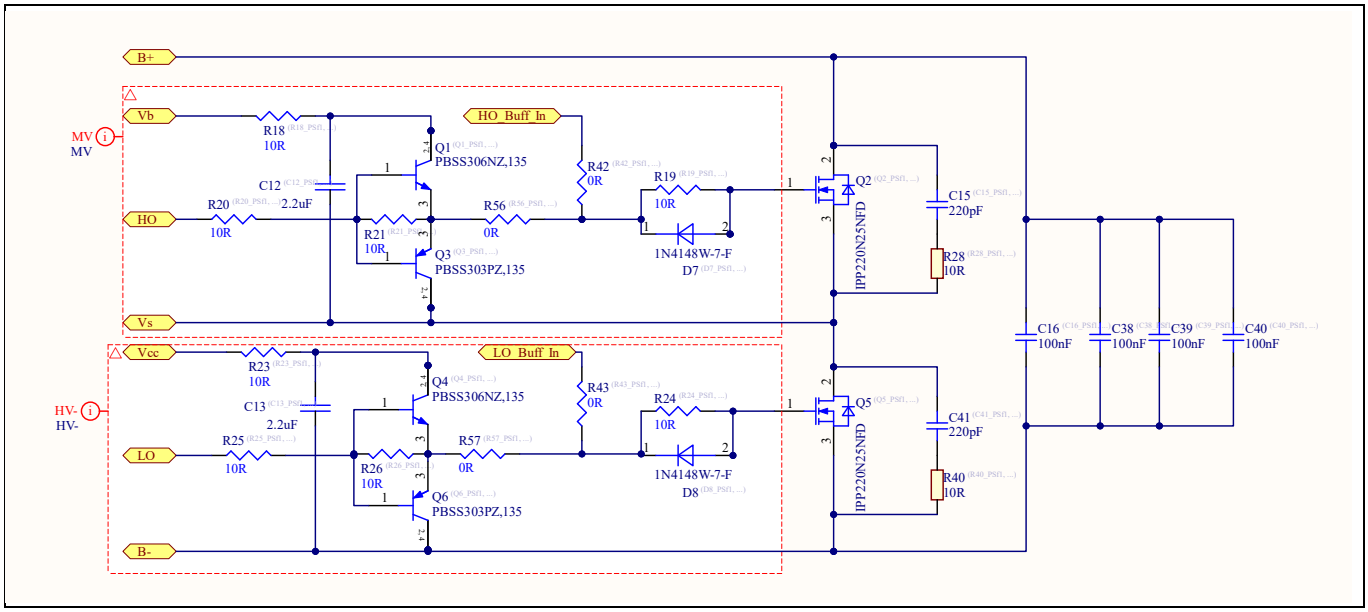


Figure 32 REF_IRS2461S_5KW Mother Board schematics – Power_Drive_Stage_Far schematics

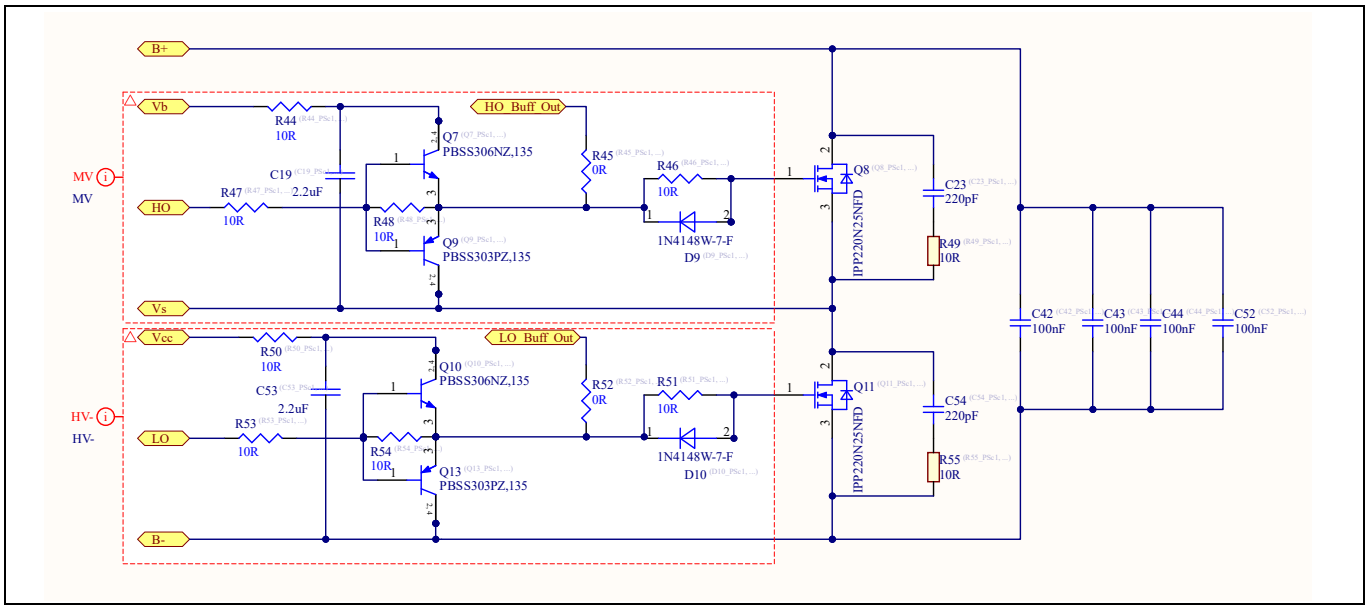


Figure 33 REF_IRS2461S_5KW Mother Board schematics – Power_Drive_Stage_Close schematics

8.2 Power Supply Daughter Card (PSDC) schematics

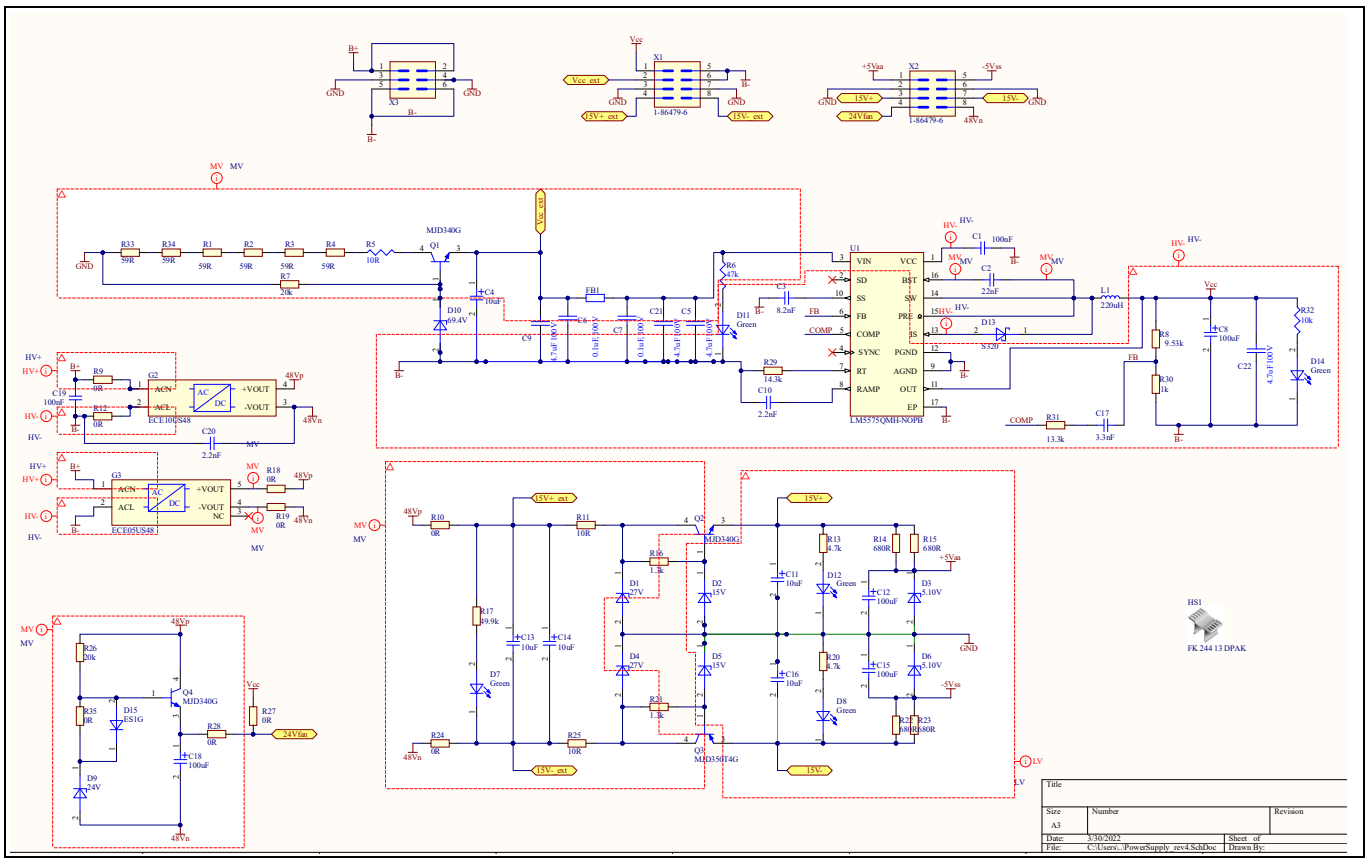


Figure 34 REF_IRS2461S_5KW Power Supply Daughter Card schematics

9 Bill of Materials

Table 8 Main Board bill of materials (BOM)

Sl. No.	Designator	Value	Description	Comment
1	Designator	Value	Description	Final
2	X11	1714984	PCB terminal block, nominal current, number of positions: 3, Number of rows: 1, Number of positions per row: 3	1714984
3	X9	5011	PC Test Point-Multipurpose THT, Black	36-5011-ND
4	X7, X8	534206-4	Receptacle Assembly, Mod II, Double Row, Dual Entry, Vertical Mount	534206-4
5	X6, X12	1714971	PCB terminal block, nominal current, number of positions: 2, Number of rows: 1, Number of positions per row: 2	1714971
6	X4	TSM-103-01-S-SV	SMT .025'' SQ Post Header, 2.54mm pitch, 3 pin, vertical, single row	TSM-103-01-S-SV
7	X2, X5	534206-3	Receptacle Assembly, Mod II, Double Row, Dual Entry, Vertical Mount	534206-3
8	X1, X3	1844223	Header, Nominal current: 8 A, Nom. voltage: 160 V, Pitch: 3.5 mm, Number of positions: 3	1844223
9	VR2		POTENTIOMETER	ST32ETB103CT-ND
10	VR1, VR3	100R	RES / VAR / 100R / 250mW / - / 100ppm/K / -55°C to 125°C / Trimmer, SMD, 3 pin, 5.00 mm L X 4.50 mm W X 2.30 mm H body / - / -	ST4ETB101
11	U2	SN74LVC2G132DCTR	Dual 2-Input NAND Gate With Schmitt-Trigger Inputs	SN74LVC2G132DCTR
12	U1	74HC2G14GV,125	Dual Inverting Schmitt Trigger	74HC2G14GV,125
13	S3, S4, S5, S6, S7, S8	09.03201.02	3 pins 2.54mm pitch Single-pole changeover slide switch, Low profile slider, Straight	09.03201.02
14	S2	G12AP	Process Sealed Ultra Miniature Toggle Switch, Logic Level 0.4VA Max, 80mohm Contact Resistance	G12JPCF
15	S1		Switch	EG1908-ND

Sl. No.	Designator	Value	Description	Comment
16	Rp1, Rp2	F20A11005ACFA06E	Thermostat 230°F (110°C) SPST-NC Potted	F20A11005ACFA06E
17	R147, R148	12R	RES / PTC / 12R / - / - / - / 0°C to 70°C / 5.00mm C X 0.60mm W 10.50mm L X 5.50mm T X 15.50mm H / - / -	PTCCL11H251HBE
18	R146	100R	RES / STD / 100R / 500mW / 1% / 100ppm/K / -55°C to 155°C / 1210(3225) / SMD / -	CRCW1210100RFKTA
19	R137, R141	10k	RES / STD / 10k / 1W / 1% / 100ppm/K / -55°C to 155°C / 2512(6332) / SMD / -	CRGP2512F10K
21	R103, R105, R108, R110			RMCF0603FT42K2
22	R99			RNCP0603FTD24K9
23	R90, R91, R92, R93, R143, R151	1MEG	RES / STD / 1MEG / 500mW / 1% / 100ppm/K / -55°C to 155°C / 1210 / SMD / -	CRCW12101M00FKTA
24	R82, R83, R30, R71		RES SMD 1K OHM 1% 1/2W 0805	ERJ-P06F1001V
25	R69, R70, R72, R73, R75, R84, R85, R86, R88, R96, R97			ERJ-PA3F4702V
27	R58, R127	4.7k	RES / STD / 4.7k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603 / SMD / -	RC0603FR-074K7L
28	R56_PSf1, R56_PSf2, R57_PSf1, R57_PSf2, R59, R149			RMCF0603ZT0R00
29	R60, R42_PSf1, R42_PSf2, R43_PSf1, R43_PSf2, R45_PSc1, R45_PSc2, R52_PSc1, R52_PSc2, R150			DNP
30	R37, R38		RES SMD 100K OHM 5% 1/2W 0805	P100KADCT-ND
31	R33, R34, R35, R36, R76, R80, R81, R87, R89, R94, R95, R140, R145			ESR03EZPJ104
32	R32, R77		352210KJT	A121121CT-ND
33	R31, R65	10R	RES / STD / 10R / 5W / 1% / 100ppm/K / -55°C to 155°C / 11.00mm L X 5.00mm W X 1.20mm H / - / -	355010RFT
34	R29, R61		RES SMD 0 OHM JUMPER 1/8W 0805	RMCF0805ZT0R00
37	R28_PSf1, R28_PSf2, R40_PSf1, R40_PSf2, R49_PSc1, R49_PSc2, R55_PSc1, R55_PSc2,	10R	RES / STD / 10R / 1W / 1% / 100ppm/K / -55°C to 155°C / 2512 / SMD / -	CSRT2512FT10R0-UP

Sl. No.	Designator	Value	Description	Comment
38	R128, R129, R130	10R	RES / STD / 10R / 1W / 1% / 100ppm/K / -55°C to 155°C / 2512 / SMD / -	DNP
40	R20_PSf1, R20_PSf2, R25_PSf1, R25_PSf2, R47_PSc1, R47_PSc2, R53_PSc1, R53_PSc2, R4, R5, R22, R27, R62, R68, R78, R98, R100, R106, R107, R121, R135, R136			13-RC0603FR-1310RLCT-ND
41	R18_PSf1, R18_PSf2, R21_PSf1, R21_PSf2, R23_PSf1, R23_PSf2, R26_PSf1, R26_PSf2, R44_PSc1, R44_PSc2, R48_PSc1, R48_PSc2, R50_PSc1, R50_PSc2, R54_PSc1, R54_PSc2, R19_PSf1, R19_PSf2, R24_PSf1, R24_PSf2, R46_PSc1, R46_PSc2, R51_PSc1, R51_PSc2			ERJ-P06F10R0V
42	R15, R120		RES SMD 68K OHM 1% 3/4W 1206	HRG3216P-6802-D-T1
43	R14, R17, R112, R113, R125, R126			ERJ-PA3J4R7V
45	R13, R16, R102, R104, R109, R111, R116, R124			RNCP0603FTD10K0
46	R131, R132			DNP
47	R10, R74			P6.2KBZCT-ND
48	R9, R79			ERJ-PA3J113V
49	R8, R12, R119, R123			RC0603FR-075K62L
50	R7, R11, R118, R122			RC0603FR-074K64L
51	R6, R41, R63, R117, R138, R139, R142, R144		RES SMD 47 OHM 5% 1/10W 0603	RC0603FR-0747RL
53	R3, R39, R64, R66	49.9k	RES / STD / 49.9k / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805 / SMD / -	AC0805FR-0749K9L
54	R2, R101, R114, R115, R133, R134			RMCF0603FT12K1
55	R1, R67	390k	Standard Thick Film Chip Resistor	CRCW0805390KFKEAHP
56	Q24, Q26	2N7000	N-Channel Enhancement Mode Field-Effect Transistor	2368-2N7000-ND
57	Q22, Q23	BSS83P	SIPMOS Small-Signal-Transistor	3757-PJA3439-AU_R1_000A1CT-ND

Sl. No.	Designator	Value	Description	Comment
58	Q18, Q19	FMMT597TA	PNP High Voltage Transistor, -300 V, 500 mW	NSVMMBT6520LT1G
59	Q15, Q17	MMBT5401-7-F	PNP Small Signal Transistor -150 V 300 mW	MMBT5401-7-F
60	Q12, Q14, Q16, Q20, Q21	MMBT5551LT1G	NPN Bipolar Transistor; 0.06 A; 160 V	SMMBT5551LT1G
61	Q3_PSf1, Q3_PSf2, Q6_PSf1, Q6_PSf2, Q9_PSc1, Q9_PSc2, Q13_PSc1, Q13_PSc2, Q25	PBSS303PZ,135	PNP low VCEsat (BISS) transistor	PBSS303PZ,135
62	Q2_PSf1, Q2_PSf2, Q5_PSf1, Q5_PSf2, Q8_PSc1, Q8_PSc2, Q11_PSc1, Q11_PSc2	IPP220N25NFD	OptiMOS FD Power-Transistor,250 V	IPP220N25NFD
63	Q1_PSf1, Q1_PSf2, Q4_PSf1, Q4_PSf2, Q7_PSc1, Q7_PSc2, Q10_PSc1, Q10_PSc2	PBSS306NZ,135	NPN Low VCEsat Transistor	PBSS306NZ,135
64	MP1	LAM 5 K 100 24	Miniature cooling aggregates	LAM 5 K 100 24
65	LD1, LD2	Red	SmartLED 0603 / Hyper-Bright Low Current LED	LS L29K-G1J2-1-Z
66	L3, L4, L5, L6	8.2uH	IND / STD / 8.2uH / 75A / 20% / -40°C to 125°C / 5.65mR / THT / Inductor, THT, 22.00 mm L X 31.00 mm W X 33.00 mm H Body / THT / -	CPD3122SA-8R2M
67	L1, L2, L7, L8	8.2uH	IND / STD / 8.2uH / 55A / 20% / -40°C to 125°C / 3.1mR / THT / Inductor, THT; 4 pin, 19.00mm L X 31.00 mm W X 33.00 mm H body / THT / -	DNP
68	IC4		MC33078	296-17724-5-ND
69	IC3	33MHz	1kHz to 33MHz Resistor Set SOT-23 Oscillator	LTC1799IS5#TRPBF
70	IC1, IC2		IRS2461S	IRS2461S
71	D22		DIODE ZENER 68V 500MW SOD123	MMSZ5266BT1GOSCT-ND
72	D21		DIODE ZENER 51V 500MW SOD123	MMSZ51T1G
73	D19		DIODE ZENER 75V 500MW SOD123	BZT52B75-E3-08GITR-ND
74	D11, D12, D14, D15	VS-15EWH06FN-M3		VS-15EWH06FN-M3

Sl. No.	Designator	Value	Description	Comment
75	D7_PSf1, D7_PSf2, D8_PSf1, D8_PSf2, D9_PSc1, D9_PSc2, D10_PSc1, D10_PSc2	1N4148 W-7-F	Surface Mount Fast Switching Diode	PMEG3020EGWJ
76	D2, D4, D5, D6, D16, D17, D18, D26, D27, D28	ES1G		ES1G
77	D1, D3, D13, D20, D23, D24, D25	BAS521, 315	Single high-voltage switching diode 300V 0.25A	BAS521,315
78	C91, C92			C0603C101J5GAC7867
79	C87	330nF	CAP / CERA / 330nF / 16V / 10% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	CGA3E3X7R1H334K080AB
80	C86, C89	100pF	CAP / CERA / 100pF / 50V / 1% / C0G (EIA) / NP0 / -55°C to 125°C / 0603(1608) / SMD / -	C0603C101F5GAC
81	C85, C88	470pF	CAP / CERA / 470pF / 250V / 10% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	885342006005
82	C57, C58, C76	100uF	CAP / - / 100uF / 25V / 20% / Aluminiumelectrolytic / -55°C to 105°C / 6.60mm L X 6.60mm W X 7.70mm H / SMD / -	865060445005
83	C47, C48, C49, C82	22pF	CAP / CERA / 22pF / 50V / 2% / C0G (EIA) / NP0 / -55°C to 125°C / 0603(1608) / SMD / -	GRM1885C1H220GA01D
84	C45, C46	100uF	ALUMINUM ELECTROLYTIC CAPACITOR,100 µF ,6.3V	UVR0J101MDD1TD
85	C36, C37, C66, C73, C84, C90	100nF	CAP / CERA / 100nF / 50V / 10% / X7R (EIA) / -55°C to 125°C / 603(1608) / SMD / -	06035C104K4Z2A
86	C34, C35			C3216X7R2E104K160AA
87	C28, C29, C30, C31, C32, C33	820uF	CAP / - / 820uF / 160V / 20% / - / -40°C to 105°C / 10.00mm C X 0.85mm W 23.50mm Dia X 37.00mm H / - / -	LGG2C821MELZ35
88	C21, C22, C60, C61	2.2nF	CAP / - / 2.2nF / 200V / 10% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	GRM21AR72D222KW01D
89	C20, C62	680nF	CAP / FILM / 680nF / 400V / 5% / MKP (Metallized Polypropylene) / -55°C to 110°C / 15.00mm C X 0.80mm W 18.00mm L X 11.00mm T X 18.50mm H / - / -	R46KI368000P0K
90	C18, C55			DNP

Sl. No.	Designator	Value	Description	Comment
91	C17, C63	100nF	CAP / FILM / 100nF / 560V / 10% / MKP (Metallized Polypropylene) / -40°C to 110°C / 15.00mm C X 0.60mm W 17.90mm L X 4.85mm T X 11.10mm H / - / -	R46KI310050M1K
92	C16_PSf1, C16_PSf2, C38_PSf1, C38_PSf2, C39_PSf1, C39_PSf2, C40_PSf1, C40_PSf2, C42_PSc1, C42_PSc2, C43_PSc1, C43_PSc2, C44_PSc1, C44_PSc2, C52_PSc1, C52_PSc2	100nF	SMD Comm X7R HV, Ceramic, 0.1 uF, 10%, 500 VDC, X7R, SMD, MLCC, High Voltage, Temperature Stable, 1210	C1210V104KCRAC7800
93	C15_PSf1, C15_PSf2, C23_PSc1, C23_PSc2, C41_PSf1, C41_PSf2, C54_PSc1, C54_PSc2	220pF	CAP / CERA / 220pF / 500V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 1206(3216) / SMD / -	CC1206KKX7RBBB221
94	C14, C59		CAP CER 10000PF 50V X7R 0603	C0603C103K5RAC7411
95	C80, C81		CAP CER 10000PF 50V X7R 0604	DNP
96	C12_PSf1, C12_PSf2, C13_PSf1, C13_PSf2, C19_PSc1, C19_PSc2, C53_PSc1, C53_PSc2		CAP CER 2.2UF 25V X7R 0805	587-2991-1-ND
97	C9, C75, C10, C11, C67, C74	22uF	Commerical Grade Multilayer Ceramic Chip Capacitor	GRM32ER71E226ME15K
98	C8, C68	2.2nF	Chip Monolithic Ceramic Capacitor	GRM188R72A222KA01
99	C6, C7, C50, C51, C64, C65, C83, C93, C94	10uF	Commerical Grade Multilayer Ceramic Chip Capacitor	CL31B106KAHSFNE
100	C77, C78, C79	220pF	CAP / CERA / 220pF / 50V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 603 / SMD / -	DNP
101	C4, C72, C24, C25, C26, C27	220pF	CAP / CERA / 220pF / 50V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 603 / SMD / -	885012006059
102	C3, C5, C70, C71			399-7901-1-ND
103	C2, C56	47pF	Chip Monolithic Ceramic Capacitor	GRM21A5C2E470JW01D
104	C1, C69		CAP ALUM 10UF 20% 50V RADIAL	565-1106-ND

Table 9 Power Supply Daughter Card bill of materials (BOM)

Sl. No.	Designator	Value	Description	Part number
1	C1	100nF	CAP / CERA / 100nF / 50V / 5% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	C0805C104K5RAC7210
2	C2	22nF	CAP / CERA / 22nF / 50V / 10% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	C0805C223K5RACTU
3	C3	8.2nF	CAP / CERA / 8.2nF / 50V / 5% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	CGA3E2C0G1H822J080AE
4	C4, C11, C13, C14, C16	10uF	Aluminum Electrolytic Capacitor 10 µF,160V	UVR2C100MPD1TD
5	C5, C9, C21, C22		CAP CER 4.7UF 100V X7S 1210	CNA6P1X7R2A475K250AE
6	C6, C7		CAP CER 0.1UF 100V X7R 0603	HMK107B7104KAHT
7	C8, C12, C15	100uF	CAP / ELCO / 100uF / 25V / 20% / - / -40°C to 105°C / 8.30mm L X 8.30mm W X 10.50mm H / - / -	EEE-FC1E101P
8	C10	2.2nF	CAP / CERA / 2.2nF / 50V / 5% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	C0805C222K5RACTU
9	C17	3.3nF	CAP / CERA / 3.3nF / 50V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 0805(2012) / SMD / -	GRM2165C1H332JA01D
10	C18	100uF	CAP / ELCO / 100uF / 50V / 20% / Aluminiumelectrolytic / -40°C to 105°C / 10.30mm L X 10.30mm W X 10.50mm H / - / -	63SGV100M10X10.5
11	C19	100nF	CAP / FILM / 100nF / 630V / 5% / MKP (Metallized Polypropylene) / -55°C to 110°C / 15.00mm C X 0.80mm W 18.00mm L X 7.00mm T X 12.50mm H / - / -	B32672L6104J000
12	C20	2.2nF	CAP / CERA / 2.2nF / 500V / 10% / X7R (EIA) / -55°C to 125°C / 1206(3216) / SMD / -	CL31B222KHFNFNE
13	D1, D4, D9	27V	Zener Voltage Regulator, Vz 27V Nominal, IZT 4.6mA	MMSZ5254BT1G
14	D2, D5	15V	Zener Voltage Regulator, 15V	SZMMSZ15ET1G
15	D3, D6	5.10V	500mW Surface Mount Zener Diode	MMSZ5231BT3G
16	D7, D8, D11, D12, D14	Green	WL-SMCW SMT Mono-color Chip LED Waterclear, Green, 515nm	150060GS84000
17	D10	69.4V	Single Zener diodes in a SOD123 package	BZT52-B68J
18	D13	S320	Schottky Diodes & Rectifiers 3A, 200V	SK3200B-LTP
19	D15	ES1G		ES1G
20	FB1		FERRITE BEAD 2 KOHM 1210 1LN	FBMH3225HM202NTV
21	G2	ECE10US48	AC/DC Power Module	ECE10US48
22	G3	ECE05US48	AC/DC Power Module	Do not populate

Sl. No.	Designator	Value	Description	Part number
23	HS1	FK 244 13 DPAK	Board Level heatsinks, Heatsinks for D PAK and others, direct PCB mounting thru solderable surface	FK 244 13 D PAK
24	L1	220uH	IND / STD / 220uH / 2.8A / 10% / -40°C to 85°C / 225mR / SMT / Inductor, SMD, 9.50 mm pitch, 2 pin, 12.00 mm L X 12.00 mm W X 10.20 mm H body / - / -	MSS1210-224KEB
25	Q1, Q2, Q4	MJD340G	NPN Bipolar Power Transistor 0.5 A, 300 V High Voltage	863-MJD340G
26	Q3	MJD350T4G	High Voltage Bipolar Transistor PNP 0.5 A; 300 V	MJD350T4
27	R1, R2, R3, R4, R33, R34	59R	RES / STD / 59R / 1W / 1% / 100ppm/K / -55°C to 155°C / 2512(6332) / SMD / -	CRM2512-FX-59R0ELF
28	R5			ESR18EZPJ100
29	R6			ESR03EZPJ473
30	R7	20k	RES / STD / 20k / 250mW / 0.1% / 25ppm/K / -55°C to 155°C / 1206(3216) / SMD / -	CRCW120620K0JNEAHP
31	R8	9.53k	RES / STD / 9.53k / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805 / SMD / -	ERJ-6ENF9531V
32	R18, R19	0R	RES / STD / 0R / 100mW / 0R / 0ppm/K / -55°C to 155°C / 0603 / SMD / -	DNP
33	R9, R12	0R	RES / STD / 0R / 100mW / 0R / 0ppm/K / -55°C to 155°C / 0603 / SMD / -	AC0603JR-070RL
34	R27	0R	RES / STD / 0R / 125mW / 0R / 0ppm/K / -55°C to 155°C / 0805 / SMD / -	DNP
35	R10, R24	0R	RES / STD / 0R / 125mW / 0R / 0ppm/K / -55°C to 155°C / 0805 / SMD / -	RC0805JR-070RL
36	R11, R25	10R	RES / STD / 10R / 1W / 1% / 100ppm/K / -55°C to 155°C / 2512 / SMD / -	RMCF2512FT10R0
37	R13, R20	4.7k	RES / STD / 4.7k / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805 / SMD / -	ERJ-P06F4701V
38	R14, R15, R22, R23	680R	RES / STD / 680R / 500mW / 1% / 100ppm/K / -55°C to 155°C / 1210 / SMD / -	CRCW1210680RFKEAHP
39	R16, R21	1.3k	RES / STD / 1.3k / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805 / SMD / -	ERJ-P06F1331V
40	R17	49.9k	RES / STD / 49.9k / 250mW / 1% / 100ppm/K / -55°C to 155°C / 1206 / SMD / -	RC1206FR-0749K9L
41	R26	20k	RES / STD / 20k / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805 / SMD / -	ERJ-P06J203V
42	R28, R35	0R	RES / STD / 0R / 500mW / - / - / -55°C to 155°C / 0805 / SMD / -	RC0805JR-070RL

Sl. No.	Designator	Value	Description	Part number
43	R29	14.3k	RES / STD / 14.3k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603 / SMD / -	RMCF0603FT14K3
44	R30	1k	RES / STD / 1k / 500mW / 1% / 100ppm/K / -55°C to 155°C / 0805 / SMD / -	ERJ-P06F1001V
45	R31	13.3k	RES / STD / 13.3k / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603 / SMD / -	CRCW060313K3FKEB
46	R32			ERJ-PA3J103V
47	U1	LM5575QMH-NOPB	1.5-A Step-down Switching Regulator	LM5575QMH-NOPB
48	X1, X2	1-86479-6	Assembly, MOD II, Double row .100 X .100, Right Angle with Spanked Tails, 8Pins, 2.54mm Pitch	1-86479-6
49	X3	929745-01-03-I	6Pin Strip Header Dual Row, 3 Pins per row, 2.54mm Pitch	929745-02-03-EU

10 PCB specification

- Four layer SMT PCB with through holes
- 2/0 oz. Cu
- FR4 material
- Solder mask to be green enamel EMP110DBG (CARAPACE) or Enthone Endplate DSR-3241 or equivalent
- Silk screen to be white empoxy non conductive per IPC-RB 276 standard
- All exposed copper is finished with tin-lead Sn 60 or 63 for 100u inch thick
- PCB acceptance criteria as defined for class II PCB’s standards

11 Schematic, layout and design considerations

This section discusses key design considerations for REF_IRS2461S_5KW.

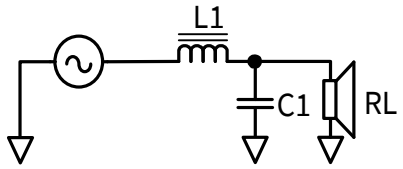
11.1 Low pass filter selection

The output low pass filter (LPF) demodulates the amplified audio signal. It is also necessary for efficient operation of a Class D amplifier; therefore, selecting the right components is critical for both audio performance and system efficiency.

A typical ouput LPF uses a second order Butterworth LC filter designed to acheive maximum flat frequency response up to a corner frequency with nominal load impedance. Figure 35 explains how to calculate the component values for a load impedance. The corner frequency should be set according to the bandwidth requirement. A corner frequency of 40 kHz would be a good tradeoff point between 20 kHz bandwidth, inductor ripple current, and inductance in other words the size of the inductor and the PWM carrier leak amplitude in the output. Note that the higher the corner frequency the higher the switching carrier leakage, and the lower the corner frequency the bigger the inductor size.

The inductance of the inductor changes with load current bias, which causes distortion in audio output. Core saturation increases the inductor ripple significantly which could trigger the over current protection immediately. Use an inductor with a saturation point that is higher than the peak load current. Consider the IRMS rating of an inductor for temperature rise condition with 1/8 rated power and peak current for maximum load current. Considering both ISAT (>52A) and IRMS (>36A) ratings, two series connected CODACA 8µH inductors CPD3122SA-8R2M have been selected for REF_IRS2461S_5KW.

Use a capacitor which meets AC voltage ratings at the highest audio frequency output. Use a film capacitor with lower series inductance structure type. Ceramic capacitors could add audio distortion from the strong bias voltage dependency in capacitance; this is especially demonstrated in high dielectric coefficient ceramic capacitors such as Y5V.



$$L_n = \frac{1.414 \cdot R_L}{2 \cdot \pi \cdot f_C}$$

$$C_n = \frac{0.707}{2 \cdot \pi \cdot f_C \cdot R_L}$$

Figure 35 Output LPF design

11.2 MOSFET selection

MOSFET selection for REF_IRS2461S_5KW has been done based on requirements such as the breakdown voltage, power loss and package size. Simetrix simulation were used to find the optimum number of FETs in parallel for 2Ohm load by mimizing power loss in order to minimize heatsink size. IPP220N25NFD is the recommended MOSFET for REF_IRS2461S_5KW design. This design can be modified to operate for 4Ohm, 1600W (1% THD+N) and 8Ohm, 800W (1% THD+N) operation as well. It is covered in the next section.

11.3 Scalability

A class D amplifier design is determined by the output power and load impedance. From these values, the DC bus voltage can be calculated. The next step is to select the correct UVP and OVP voltage thresholds for the DC bus to setup protection limits. The DC bus voltage determines the breakdown voltage of power MOSFETs. A typical practice is to limit the bus voltage to 80% of the MOSFET breakdown voltage. The MOSFET selection is also determined by the power loss caused by switching and conduction losses in each MOSFET. In high power designs, MOSFETs are often paralleled to reduce the conduction loss per MOFET ($\propto {I_{drain}}^2$). The trade-off in paralleling MOSFETs is increased switching losses. The other crucial design variable is the switching frequency. This frequency is determined by the inductor ripple current which influences idling losses as well as MOFET losses. Finally, based on the losses for each MOSFET and the maximum allowed operating temperature requirement, a suitable thermal interface material (TIM), typically thermally conducting grease or pad, and heatsink with suitable $R_{Th}$and mass can be selected to meet continuous and peak power requirements. OCP trigger point of the design naturally lowers as the junction temperature of the MOSFET increases. One possible method to select the OCP setting for the class D stage can be to set it to 1.6-1.7 times the peak current at maximum allowed operating temperature to allow rated power operation up to this allowed temperature.

The present design can be scaled for 2Ω, 4Ω and 8Ω operation. The appropriate parts selection guidelines are given below.

Load impedance (Power)	DC bus voltage	MOSFET (x #of parallel FETs)	Low pass filter	UVP/OVP settings	OCP setting (R12/(R11+R12))	Gain settings (R2, R115) & (R103, R105, R108, R110) [in kOhms]
2Ω (2500W)	±103.5V	IPP220N25NFD (x 2)	2x8µH (CPD3122SA-8R2M), 680nF	75V (D19), 119V (D22+D21)	0.45	(12.1, 12.1) & (42.2, 42.2, 42.2, 42.2)
4Ω (1600W)	±120V	IPP410N30N (x2)	2x12uH (CPD3119-120M), 470nF	75V (D19), 135V (D22+D21)	0.45	(11, 11) & (47.5, 47.5, 47.5, 47.5)
8Ω (900W)	±120V	IPP410N30N (x2)	2x12uH (CPD3119-120M), 470nF	75V (D19), 135V (D22+D21)	0.45	(11, 11) & (47.5, 47.5, 47.5, 47.5)

The resistors R11 and R12 are selected as an example. Both high side and low side OCP settings should be set to the same level by selecting identical resistor values. Also, to avoid excessive delay and false OCP triggers, it is recommended to choose the OCP setting resistor (R11, R12, R7, R8, R118, R119, R122, R123) values that are lower than 6kΩ.

11.4 Feedback topology

In no load conditions, the high Q of the output low pass filter (L-C filter) can resonate. To dampen this high Q, a secondary feedback network is added to sense the output voltage. The component values of this secondary

feedback network have been determined and tested for stability and optimized for frequency response and THD+N performance of REF_IRS2461S_5KW.

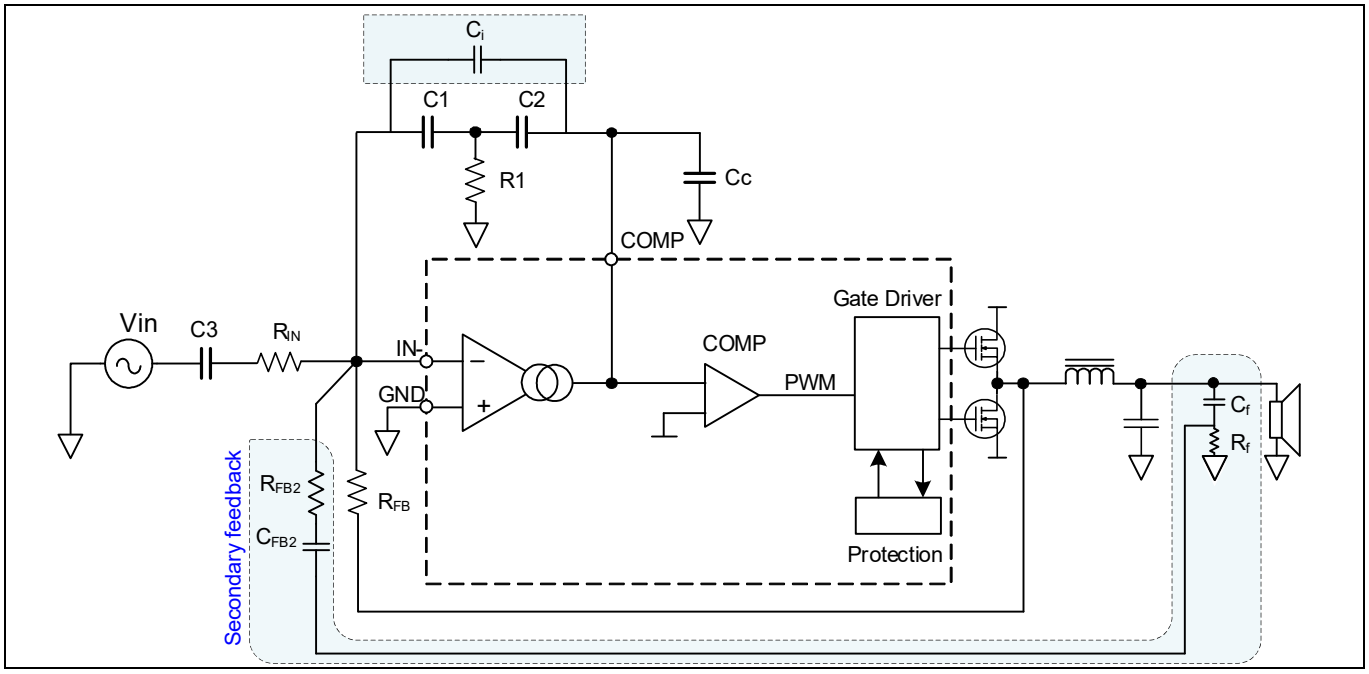


Figure 36 Feedback topology

11.5 Clock synchronization

In the PWM control loop design example, the self-oscillating frequency can be set and synchronized to an external clock as shown in Figure 37. Through the Cclk-Rlck network, an external clock signal (Vclk) can inject pulsating charge into the integrator, forcing oscillations to lock up to the clock frequency. To maximize audio performance, the self-oscillation frequency should be 20-30% higher than the clock frequency. The external clock should be 50% duty cycle.

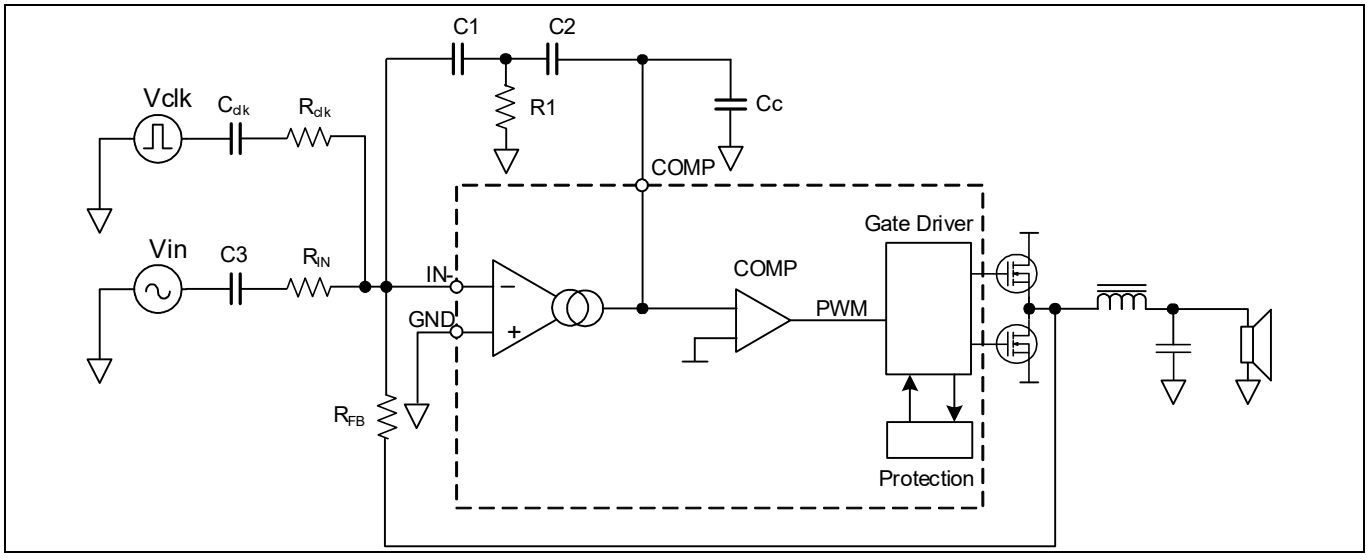
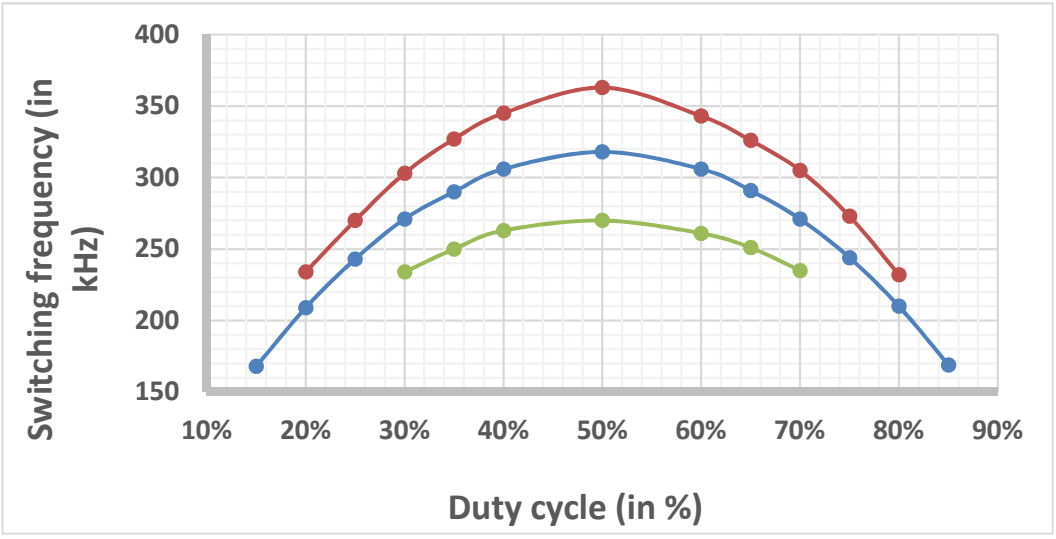


Figure 37 Clock synchronization

Figure 38 shows how a self-oscillating frequency locks up to an external clock frequency. The design is based on a 320 kHz self-oscillating frequency synchronized to clock whose frequency is within the orange and green border lines.



Red: Self-oscillating frequency, Gray: upper lock range, Yello: lower lock range

Figure 38 Typical lock range to external clock for REF_IRS2461S_5KW

11.5.1 Dynamic clock injection

A dynamic clock injection circuit has been added to improve the low power THD+N performance of the design. A balance between strong clock injection to obtain good lock range for manufacturing purposes and THD+N performance is difficult to strike. Typically, this balance means trading-off one kind of performance for the other. The dynamic clock injection circuit shuts down clock injection when the ouput level exceeds ~4W, thereby improving THD+N performance in ~5-50W region. This additional circuit allows the designer flexibility by eliminating the trade-off mentioned above. Therefore, for multi-channel high power designs, it is recommended to use such a scheme to obtain best system performance and maintain good clock lock range.

11.6 Power supply daughter card

The power supply daughter card is designed to simplify user testing experience by providing all the necessary housekeeping power supplies on board. The design specifications are as shown in Table 10. In this design, the continuous bus voltage should be restricted between ±75 to ±135V_{dc}. This is defined by the MOSFET ratings. For the power supply daughter card only, operation up to ±150V_{dc} is possible for short periods of time. This is limited by thermal design and for operation at higher voltages a redesignand additional testing are necessary for both thermal and component selection reasons.

Table 10 Power supply daughter card specifications

Supply name	Input voltage range (in V)	Output voltage (in V)	Iout_max (in A)	Pout (in W)
Vaa, Vss	±75 to ±150 V_{bus}	+5.1, -5.1V	25mA	125mW
Vcc	±75 to ±150 V_{bus}	12V	0.5A	6W
+15V, -15V	±75 to ±150 V_{bus}	+5.1, -5.1V	40mA	600mW
24Vfan	±75 to ±150 V_{bus}	24V	25mA	600mW

11.7 Layout

The layout of REF_IRS2461S_5KW limits the noise coupling in the IN- pin of IRS2461S. Additionally, the layout of CSH and CSL pins of IRS2361S are optimized to minimize noise coupling.

A star connection to the DC bus bulk capacitors is used for B- and B+ planes for each channel. This is done to avoid any noise cross-coupling between the two channels.

Layer by layer layout is given in figures from Figure 39 to Figure 45.

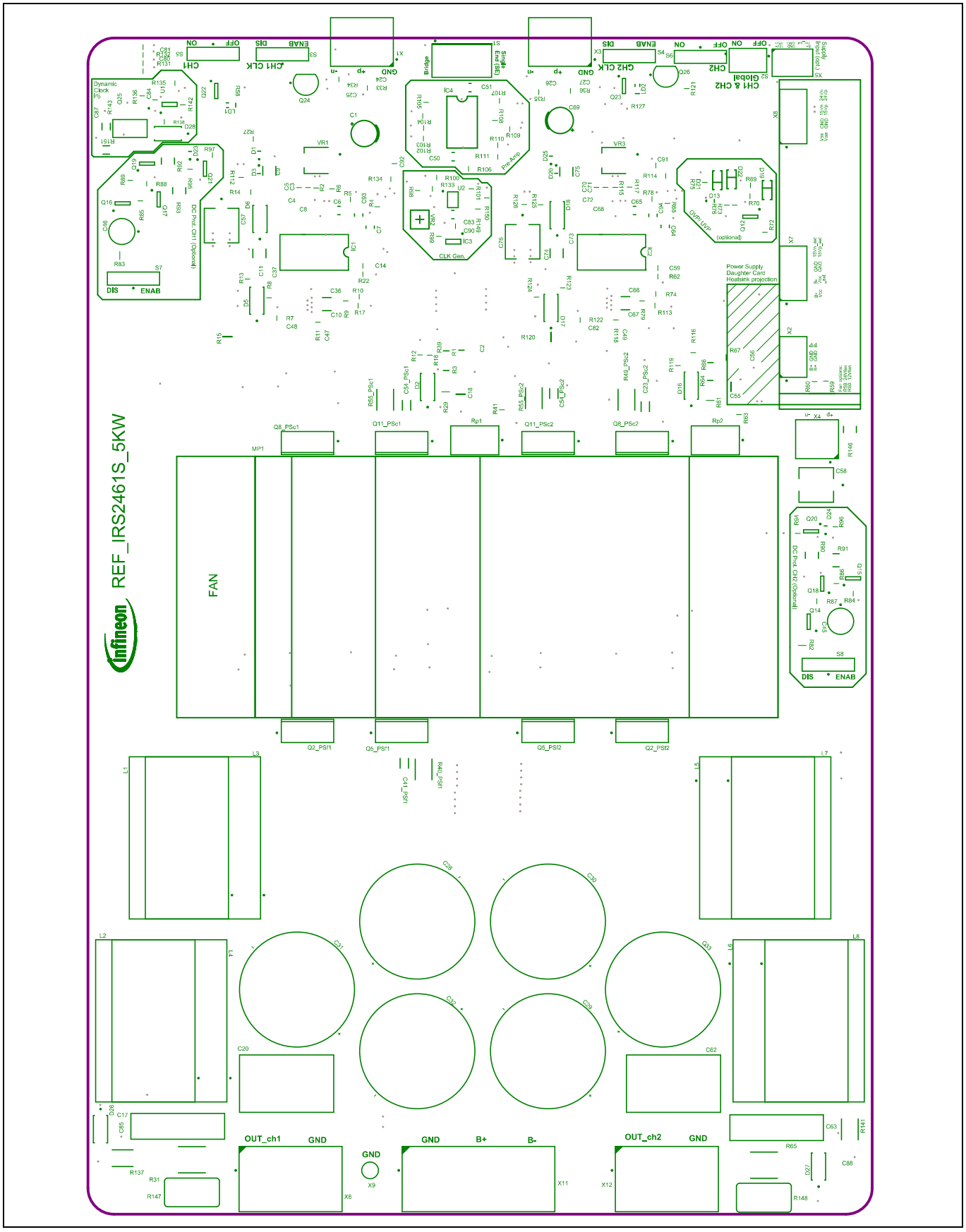


Figure 39 REF_IRS2461S_5KW - Top Overlay

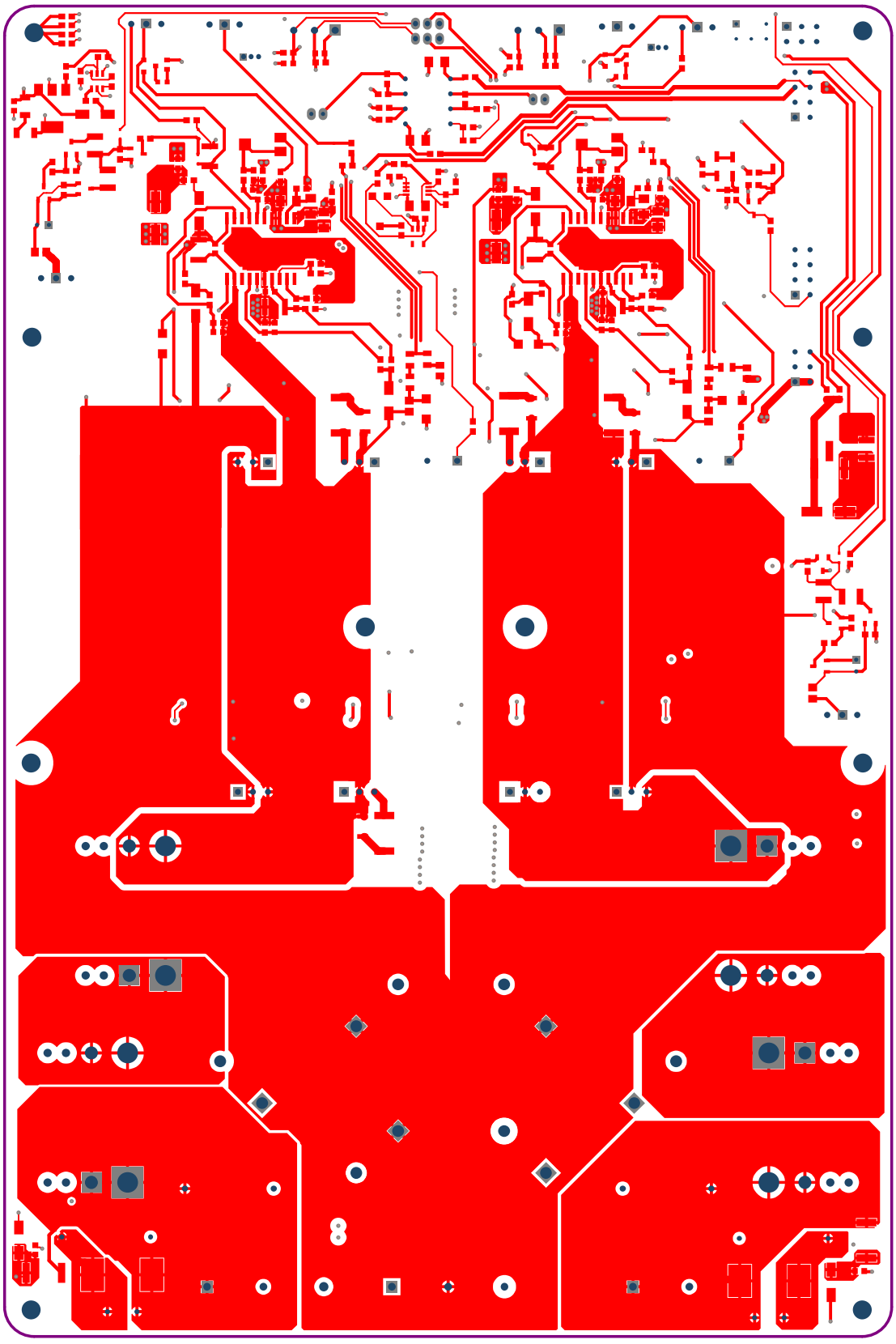


Figure 40 REF_IRS2461S_5KW – Top layer

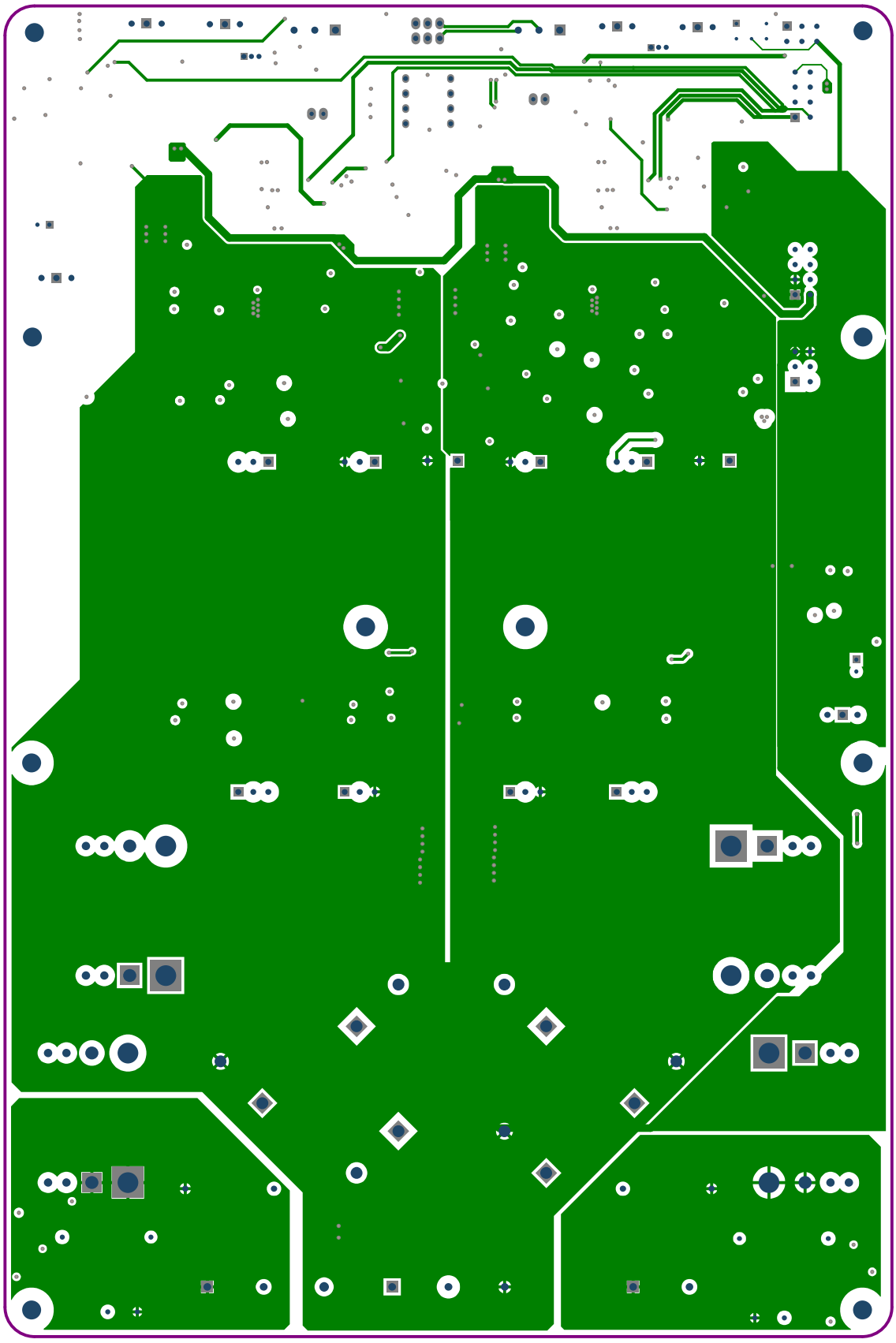


Figure 41 REF_IRS2461S_5KW – Mid layer 1

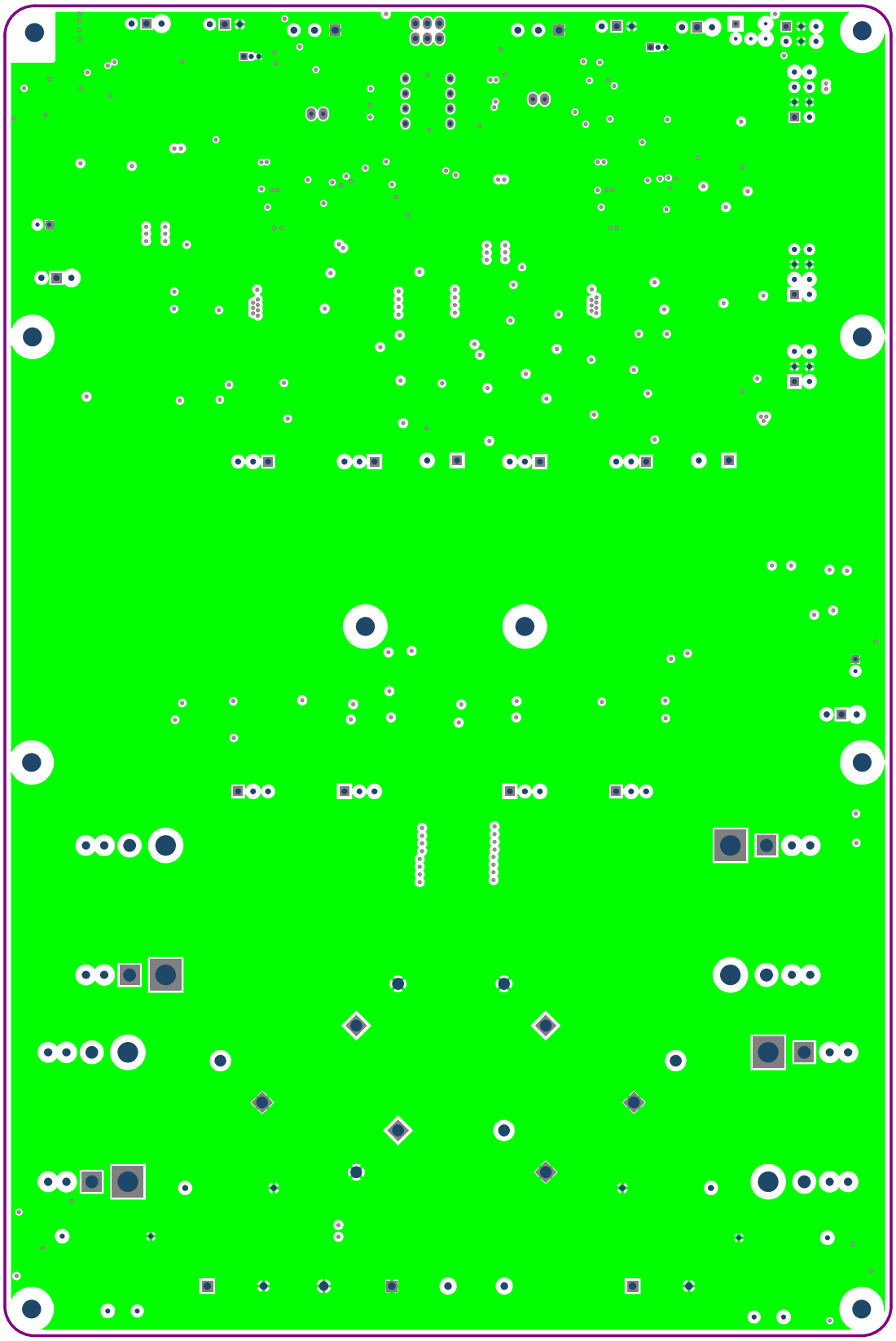


Figure 42 REF_IRS2461S_5KW – Mid layer 2

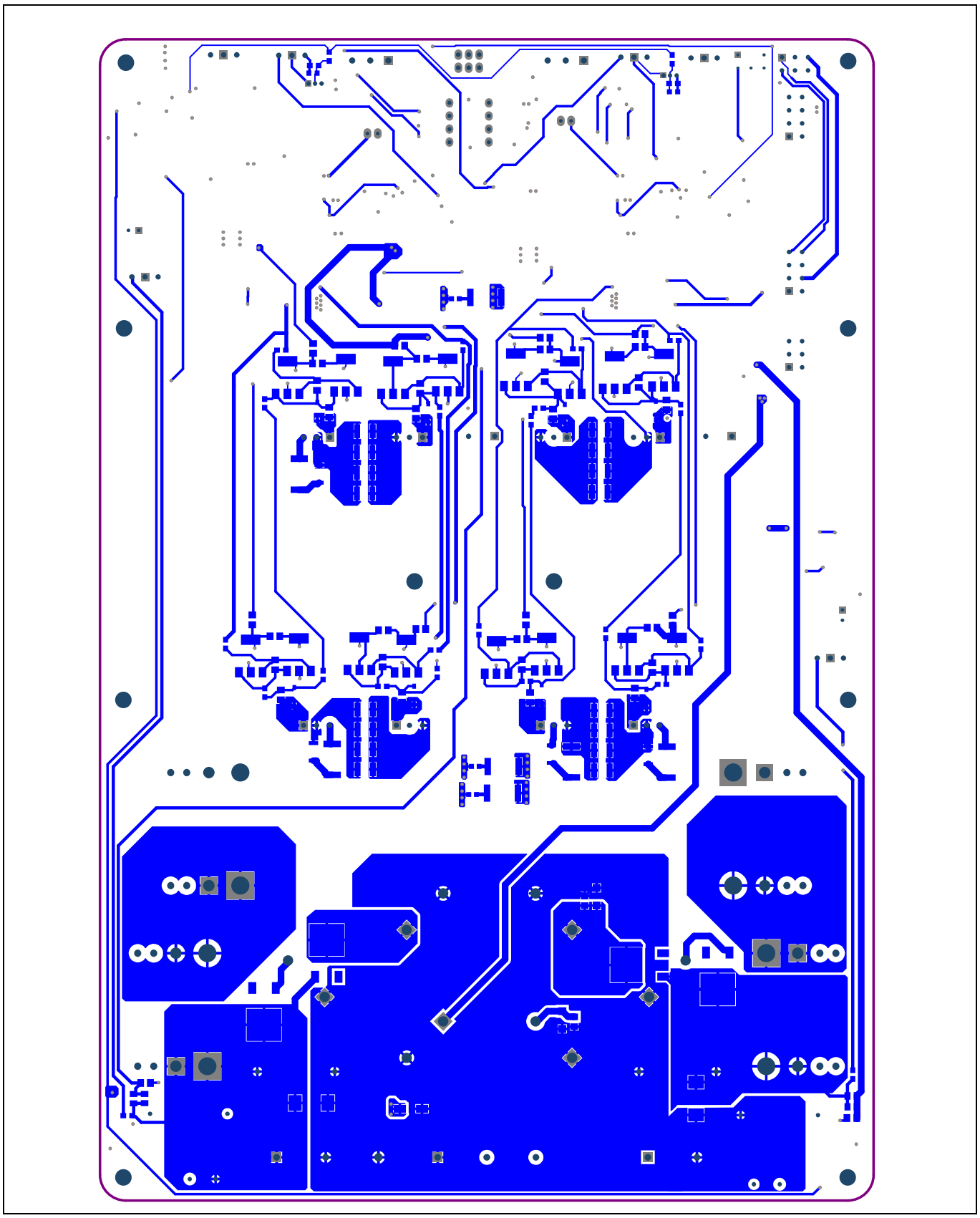


Figure 43 REF_IRS2461S_5KW – Bottom layer

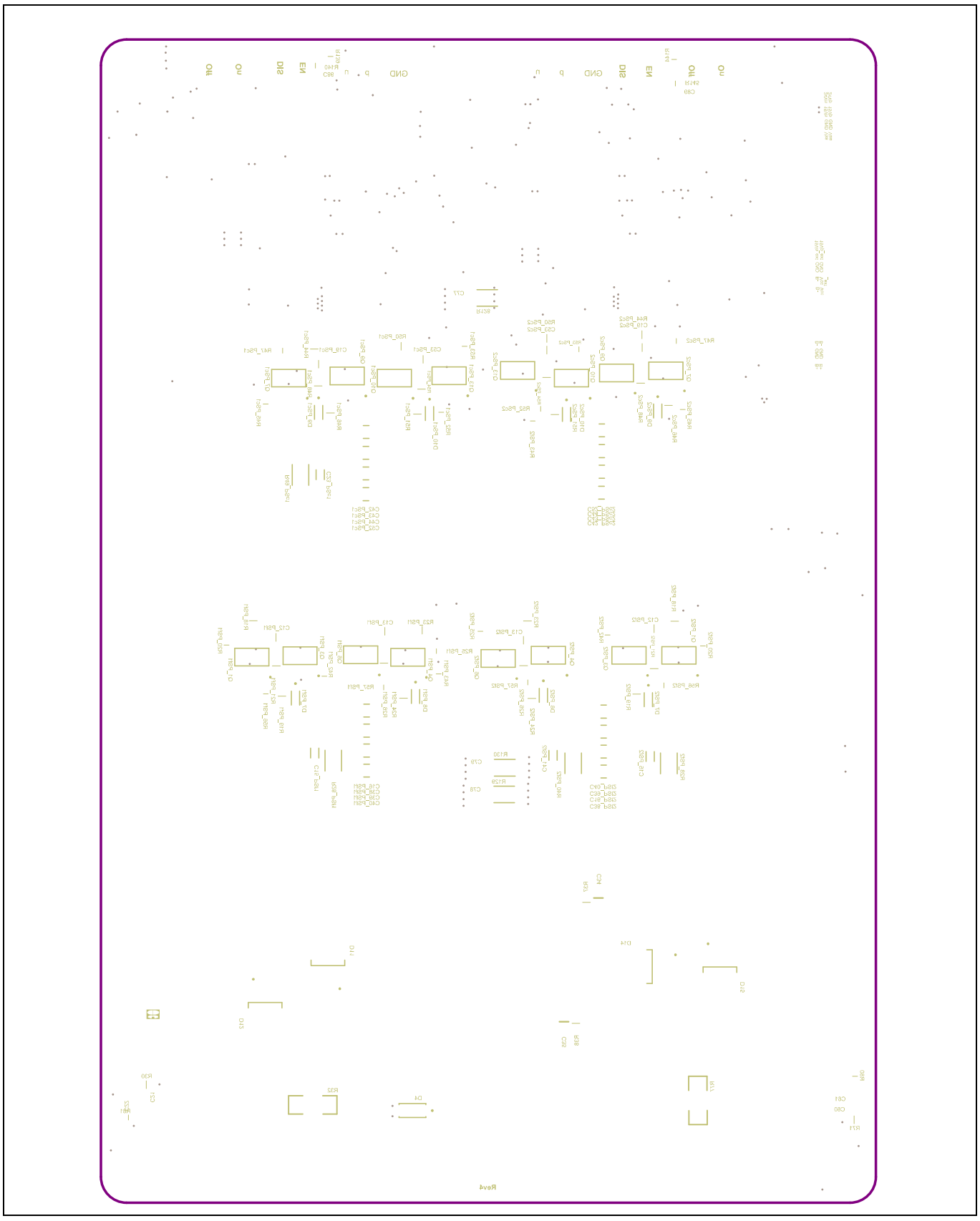


Figure 44 REF_IRS2461S_5KW – Bottom overlay

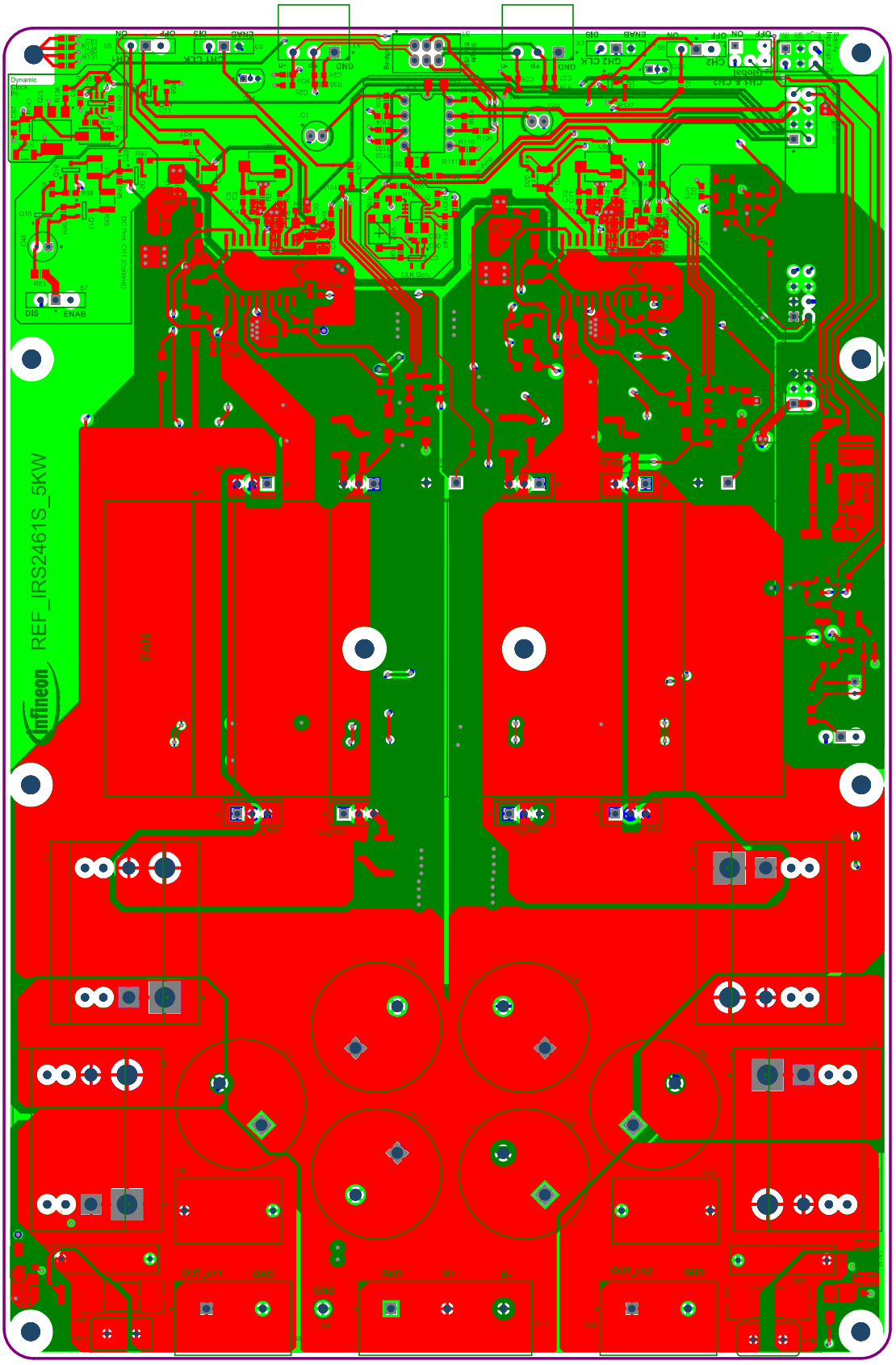


Figure 45 REF_IRS2461S_5KW – Multilayer composite

12 Useful debugging tips

- Check all the connections
- Check power supply LEDs on the Power supply daughter card status LED panel as shown in Figure 2
- Check position of S1 (Single ended/ Bridge), S2 (On/Off), S5 (CH1 On/Off) and S6 (CH2 On/Off).
- LD1 and LD2 should be Off during normal operation
- Check if B+ and B- voltage are within the input range, i.e. greater than UVP setting (75V) and less than OVP setting (119V)
- Measure supply voltage levels with a multimeter. Expected DC voltage levels are as follows: Vcc ~ 12V (w.r.t. B-), VAA ~ 5V (w.r.t. GND), Vss ~ -5V (w.r.t. GND), VB ~ 11V (w.r.t. Vs). These measurements can be made across the following components:
- Measure voltage across CSD pin w.r.t. Vss. Expected voltage ~10V.

Revision history

Document version	Date of release	Description of changes
1.0	June 16, 2022	First release
1.1	November 13, 2023	Editorial edits

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