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**For More Information**

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Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

**June 06, 2012**

## Chip Errata for the MB9AB40N/A40N/340N/140N Series, FM3 Family Microcontroller

This document describes the errata for the MB9AB40N/A40N/340N/140N Series FM3 Family Microcontroller. Details include Flash memory dual operation problems, scope of impact and available workarounds. Compare this document to the device's data sheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

### Part Numbers Affected

| Part Number |
|---|
| MB9AB40N/A40N/340N/140N Series |

# Problem Description

In the FLASH macro mounted on the target products in Item 3, two problems were found.
We would provide the information on the problems and their countermeasures.
Please accept our apology for the inconvenience caused by these failures.
We appreciate if you confirm the failures described in this document and take the appropriate countermeasures.

**Outline of Problem1**
During writing (programming) to FLASH memory of an upper bank, FLASH memory of a lower bank could not be read at a specific timing in some operation combination.

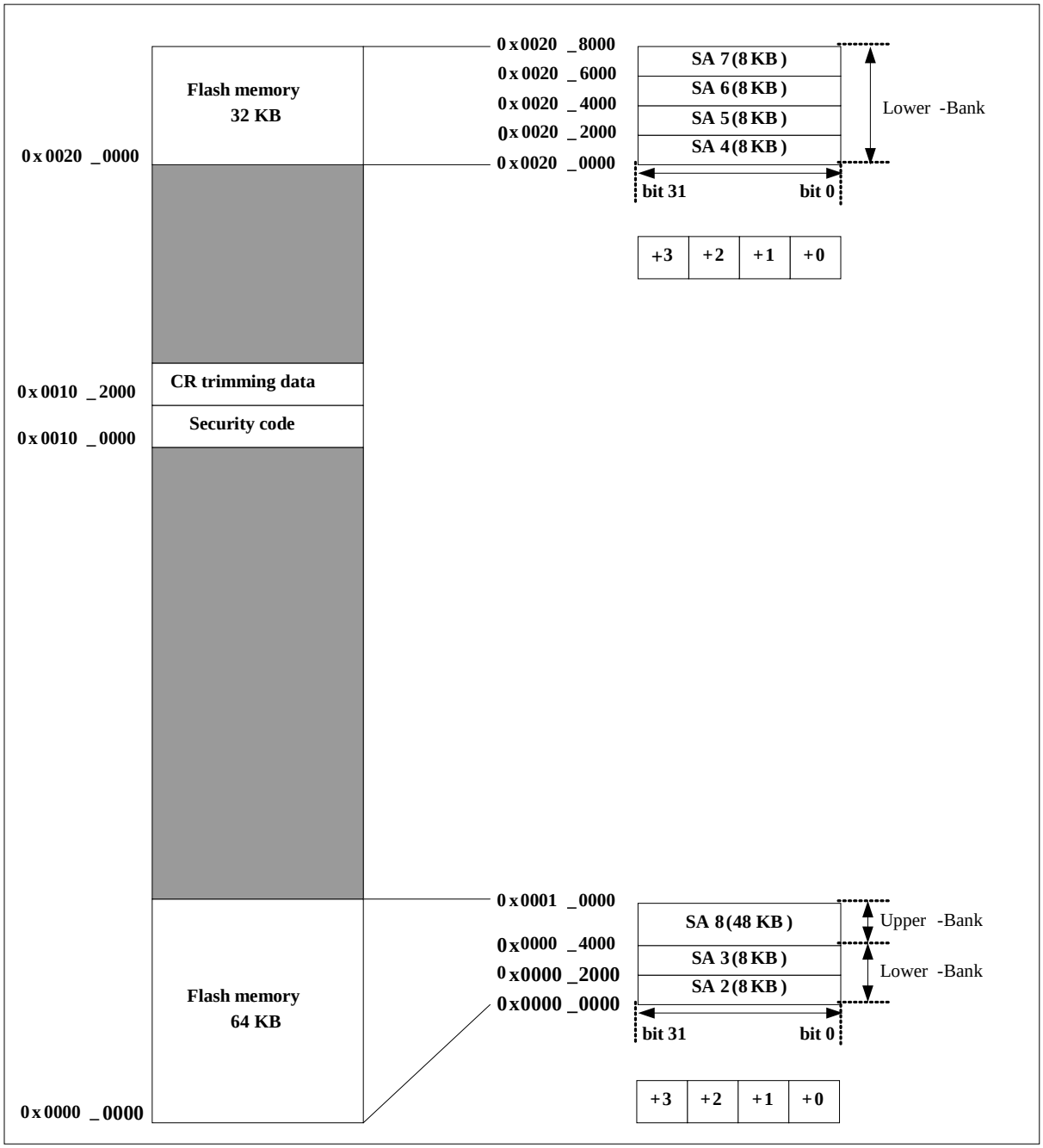
**Outline of Problem 2**
When writing is executed during sector erase suspend, FLASH memory could not be read correctly at a specific timing.

# Problem Conditions

### (1) Occurrence Conditions of Problem 1

At the specific timing, the FLASH memory lower bank (smaller sector) is not correctly read while writing(programming) to the FLASH memory upper bank (larger sector). Therefore, the instruction in the lower bank could not be read correctly and the writing sequence to the upper bank executed by the instruction would lead to a hard fault or run-away. Moreover, when the lower bank is read while writing to the upper bank by the instruction on RAM, an incorrect value might be read.

**Figure 1. FLASH Memory MAP**



The problem occurs at the combination of the following operations.

| Upper bank (Larger sector) | Lower bank (Smaller sector) | Judgment |
|---|---|---|
| Instruction/data reading | | Normal operation |
| Instruction/data reading | Writing | Normal operation |
| Instruction/data reading | Sector erase | Normal operation |
| Writing | **Instruction/data reading** | **At a specific timing, a correct value could not be read.** |
| Sector erase | Instruction/data reading | Normal operation |
| FLASH memory(all sectors) erase | | Normal operation |

**(2) Occurrence Condition of Problem 2**

When writing to the upper bank or the lower bank at a sector erase suspend, reading to the opposite bank might result in reading of an incorrect value at a specific timing. Therefore, FLASH memory could not be correctly read in the following flow, and a hard fault or a run-away might occur.

(a) Erase a sector of the lower bank.

(b) Suspend the sector erase operation.

(c) Write to a different sector of the lower bank.

(d) Execute an instruction in the upper bank.

Different from Problem 1, this problem would occur in the reverse operation combination of used banks.

The problem occurs at some combinations of the following operations.

| Operation during suspend | | Judgement |
|---|---|---|
| **Upper bank (Larger sector)** | **Lower bank (Smaller sector)** | |
| Instruction/data reading | | Normal operation |
| **Instruction/data reading** | Writing | At a specific timing, a correct value cannot be read. |
| Writing | **Instruction/data reading** | |

## Affected Devices

The following devices are affected:

| Series names | Part number of affected products |
|---|---|
| MB9A140N series | MB9AF141L, MB9AF141M, MB9AF141N<br>MB9AF142L, MB9AF142M, MB9AF142N<br>MB9AF144L, MB9AF144M, MB9AF144N |
| MB9A340N series | MB9AF341L, MB9AF341M, MB9AF341N<br>MB9AF342L, MB9AF342M, MB9AF342N<br>MB9AF344L, MB9AF344M, MB9AF344N |
| MB9AA40N series | MB9AFA41L, MB9AFA41M, MB9AFA41N<br>MB9AFA42L, MB9AFA42M, MB9AFA42N<br>MB9AFA44L, MB9AFA44M, MB9AFA44N |
| MB9AB40N series | MB9AFB41L, MB9AFB41M, MB9AFB41N<br>MB9AFB42L, MB9AFB42M, MB9AFB42N<br>MB9AFB44L, MB9AFB44M, MB9AFB44N |

## Affected Modules

This problem is affecting the operation of the FLASH memory

## Root Cause

The failures are caused by design mistake.

## Workaround

To solve these problems we would re-design the circuit of the affected devices.
Before the re-design, the problems could be avoided by taking the following countermeasures:

- Countermeasures against Problem 1
To rewrite the upper bank of FLASH memory, store the write instruction in RAM instead of the lower bank and read the instruction from RAM to execute. Do not access the lower bank until the write operation is completed (RDY=1). Especially to disable the vector fetch to the lower bank of the FLASH memory at an interrupt occurred, the interrupt should be prohibited or the vector address should be set to RAM by the vector table offset register.

- Countermeasures against Problem 2
We could not provide an effective countermeasure against Problem 2.
So, do not execute the write operation to a different sector in the same bank at sector erase suspend.

## Corrective action by Cypress Semiconductor

Cypress Semiconductor will correct these problems by a redesign of the affected devices
New part numbers are made by adding “A” at the end of the previous product types and new device delivery schedule is as follows:

| Series name or product type | ES Delivery Date | Mass-production Start Date |
|---|---|---|
| MB9AF141LA, MB9AF141MA, MB9AF141NA<br>MB9AF142LA, MB9AF142MA, MB9AF142NA<br>MB9AF144LA, MB9AF144MA, MB9AF144NA | The 31st of August, 2012 | The 28th of September ,2012 |
| MB9AF341LA, MB9AF341MA, MB9AF341NA<br>MB9AF342LA, MB9AF342MA, MB9AF342NA<br>MB9AF344LA, MB9AF344MA, MB9AF344NA | The 31st of August, 2012 | The 28th of September, 2012 |
| MB9AFA41LA, MB9AFA41MA, MB9AFA41NA<br>MB9AFA42LA, MB9AFA42MA, MB9AFA42NA<br>MB9AFA44LA, MB9AFA44MA, MB9AFA44NA | The 31st of August, 2012 | The 28th of September ,2012 |
| MB9AFB41LA, MB9AFB41MA, MB9AFB41NA<br>MB9AFB42LA, MB9AFB42MA, MB9AFB42NA<br>MB9AFB44LA, MB9AFB44MA, MB9AFB44NA | The 31st of August, 2012 | The 28th of September, 2012 |

## Document History Page

| Document Title: Chip Errata for the MB9AB40N/A40N/340N/140N Series, FM3 Family Microcontroller<br>Document Number: 002-04518 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Description of Change** |
| ** | _ | YUIS | Initial release |
| *A | 5232550 | YUIS | Migrated to Cypress format |

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