Schematic modified for
CY8CKIT-064S0S2-4343W PSoC 64 Standard Secure - AWS Wi-Fi BT Pioneer Kit

CYW9-BASE-01 Pioneer Baseboard

CONTENTS

Drawing Numbers	
PCBA	121-60579-01
PCB	600-60552-01
FAB DRW	610-60552-01
ASSY DRW	620-60552-01
SCH DRW	630-60552-01

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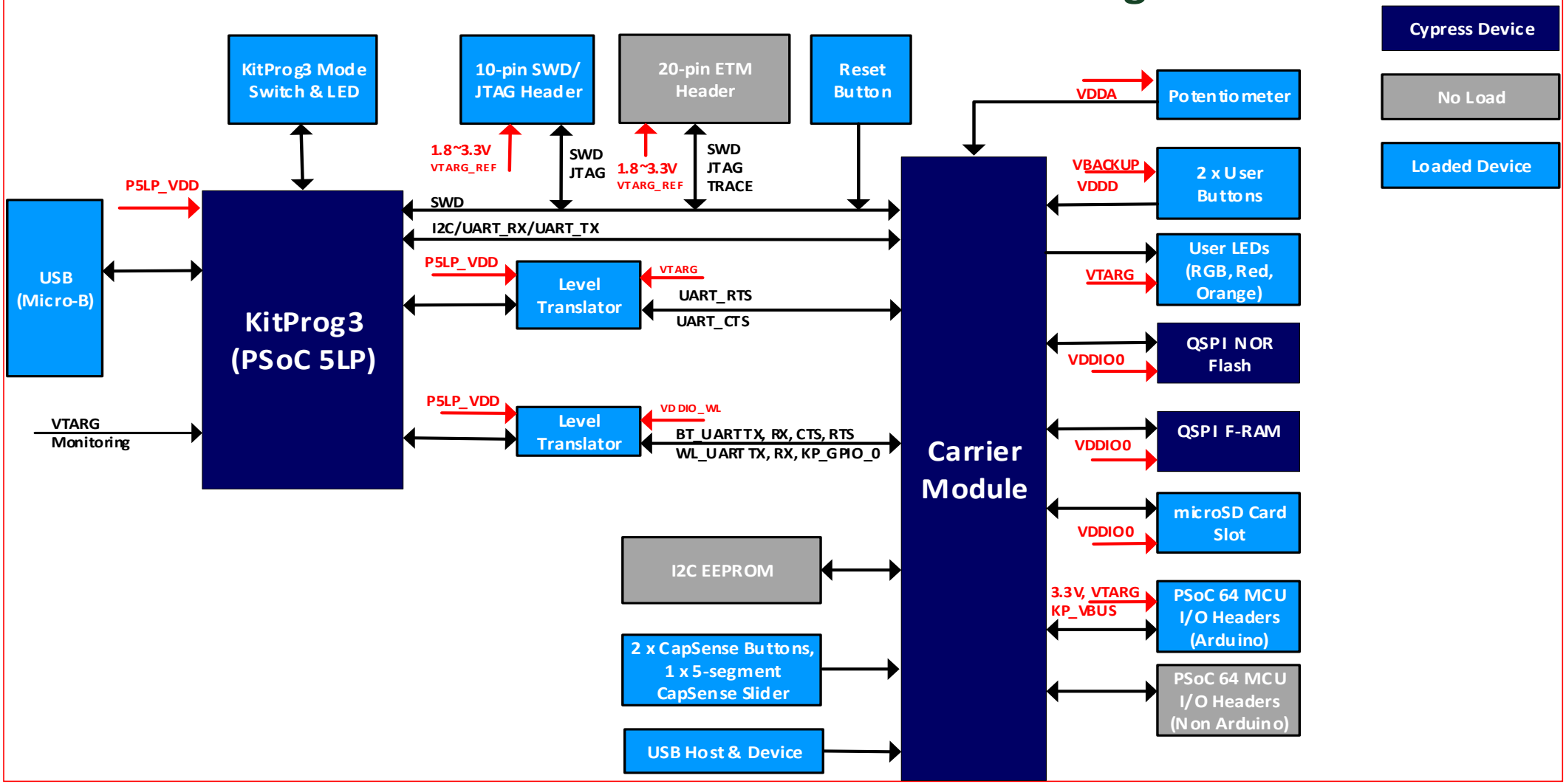
SCH Title : CYW9-BASE-01 Pioneer Baseboard

Page Title : Title Page

Size	Document Number	Drawn By	Approved By	Rev
A4	630-60552-01	TARE	RKAD	08

Date: Tuesday, November 24, 2020 Sheet 1 of 13

CYW9-BASE-01 Functional Block Diagram



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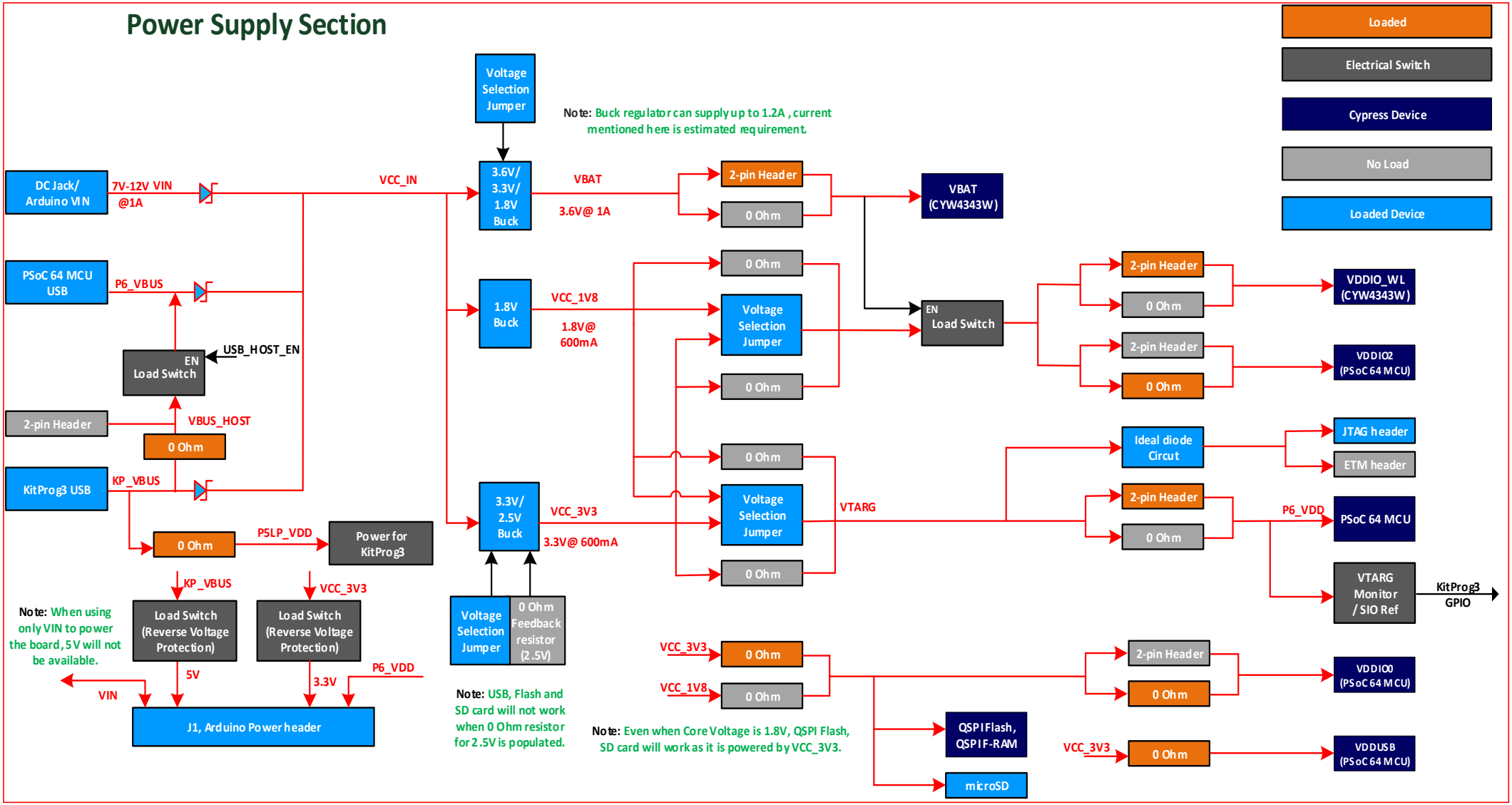
SCH Title : CYW9-BASE-01 Pioneer Baseboard

Page Title : Functional Block Diagram

Size	Document Number	Drawn By	Approved By	Rev
A4	630-60552-01	TARE	RKAD	08

Date: Thursday, August 06, 2020 Sheet 2 of 13

Power Supply Section



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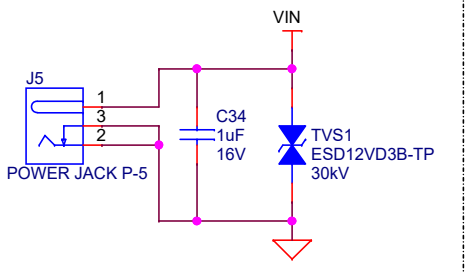
SCH Title : CYW9-BASE-01 Pioneer Baseboard

Page Title : Power Supply Block Diagram

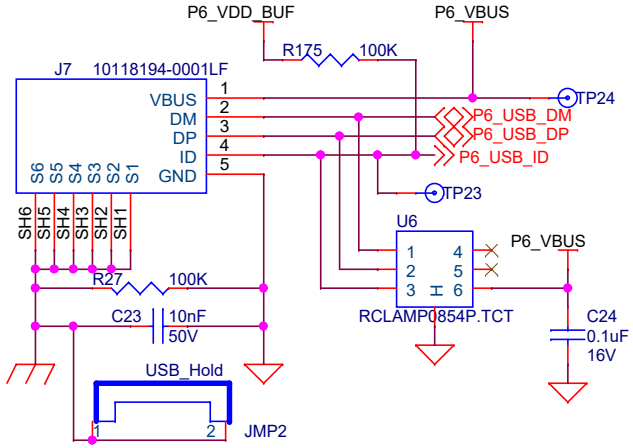
Size	Document Number	Drawn By	Approved By	Rev
A4	630-60552-01	TARE	RKAD	08

Date: Wednesday, September 23, 2020 Sheet 3 of 13

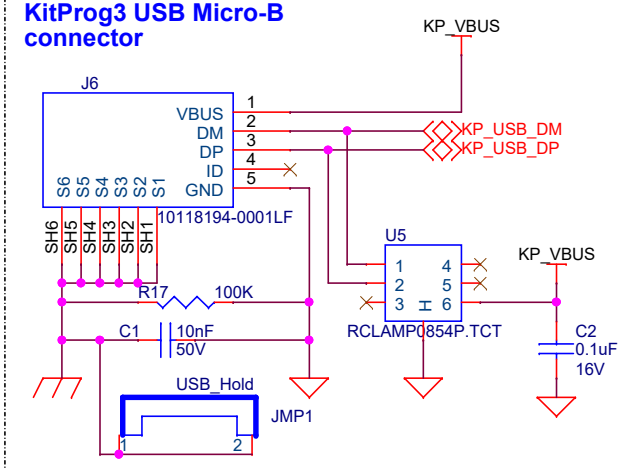
VIN Header

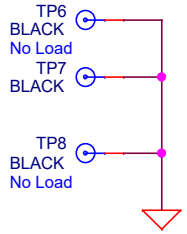


PSoC 64 MCU USB Host/Device Micro-B connector

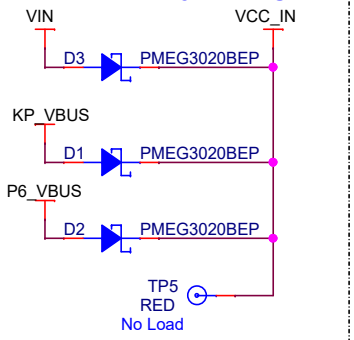


KitProg3 USB Micro-B connector

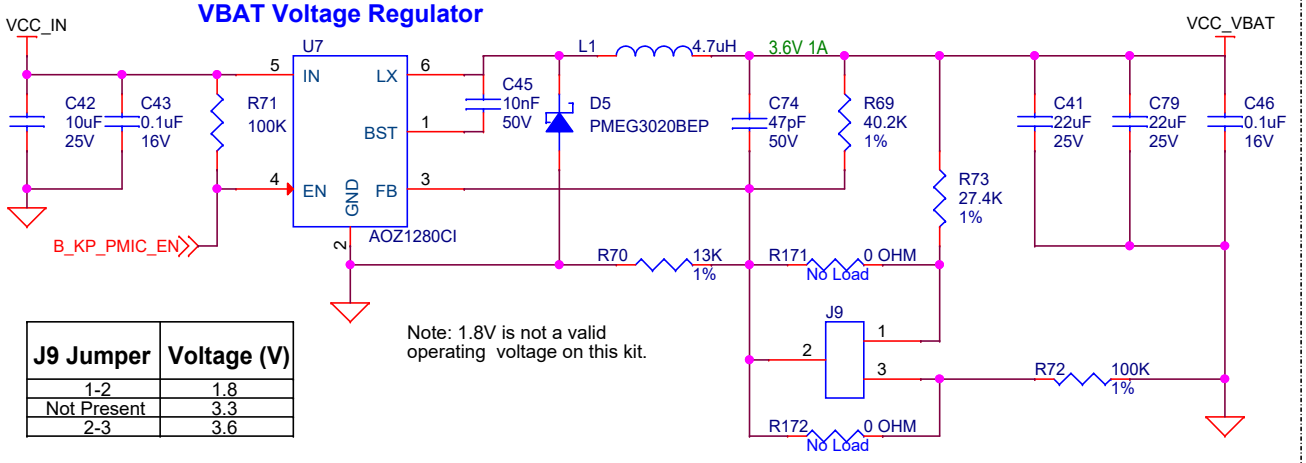




Power Supply 'OR'ing



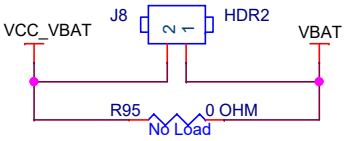
VBAT Voltage Regulator



J9 Jumper	Voltage (V)
1-2	1.8
Not Present	3.3
2-3	3.6

Note: 1.8V is not a valid operating voltage on this kit.

Current Measurement



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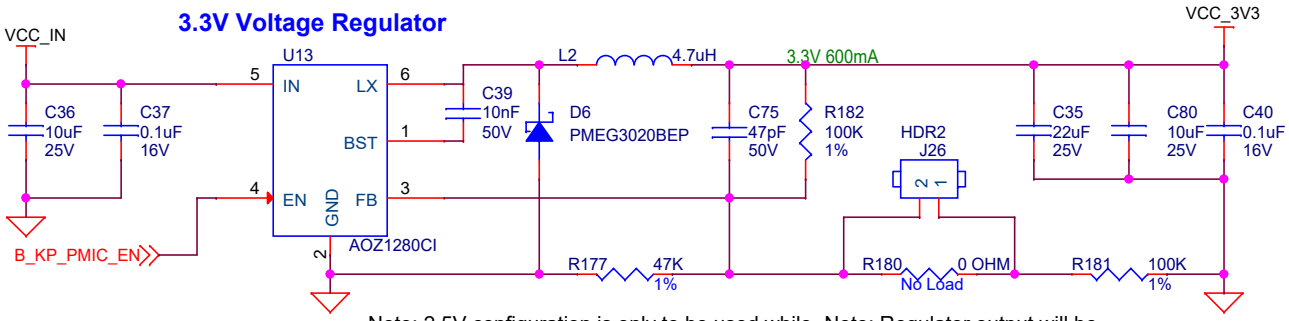
SCH Title : CYW9-BASE-01 Pioneer Baseboard

Page Title : Power Supply (1)

Size	Document Number	Drawn By	Approved By	Rev
A4	630-60552-01	TARE	RKAD	08

Date: Thursday, August 06, 2020 Sheet 4 of 13

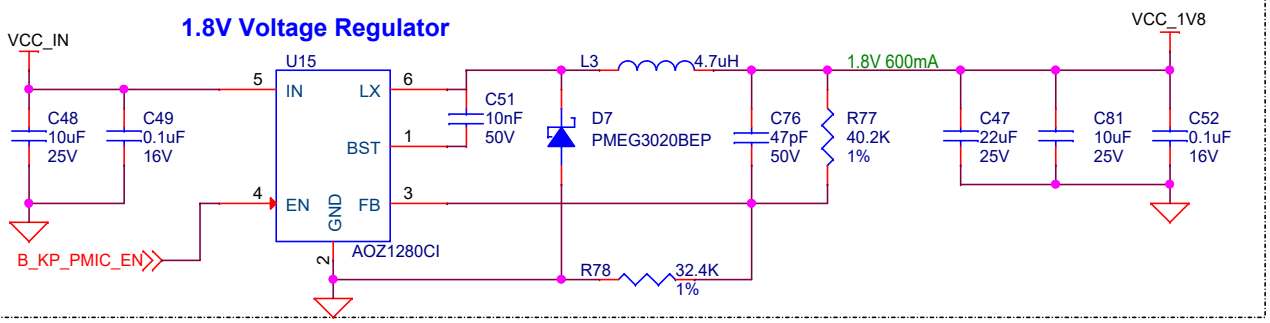
3.3V Voltage Regulator



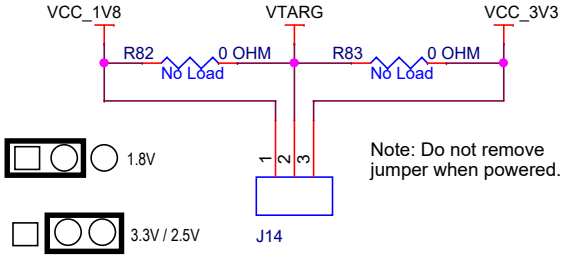
Note: 2.5V configuration is only to be used while eFuse programming. Normal operation is supported only in 3.3V configuration.

Note: Regulator output will be 3.3V when J26 jumper is loaded and 2.5V when removed.

1.8V Voltage Regulator

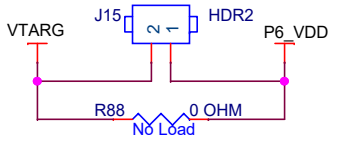


VTARG Voltage Selection Header

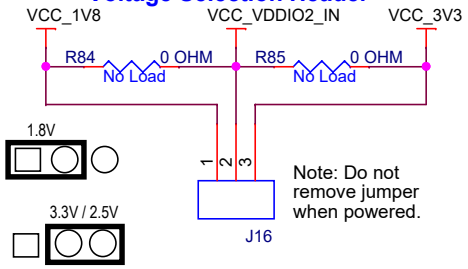


Note: Do not remove jumper when powered.

P6_VDD Current Measurement

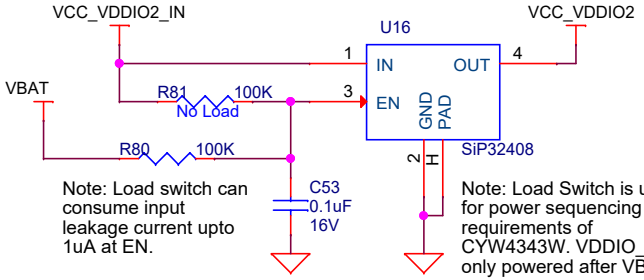


VCC_VDDIO2_IN Voltage Selection Header



Note: Do not remove jumper when powered.

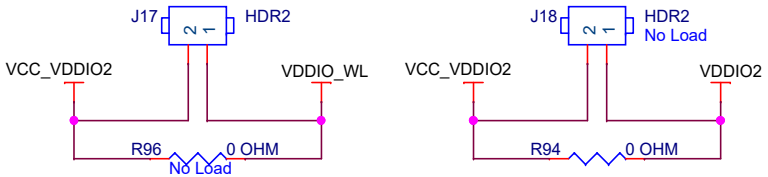
VCC_VDDIO2 Load Switch



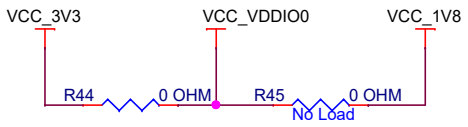
Note: Load switch can consume input leakage current upto 1uA at EN.

Note: Load Switch is used for power sequencing requirements of CYW4343W. VDDIO_WL only powered after VBAT.

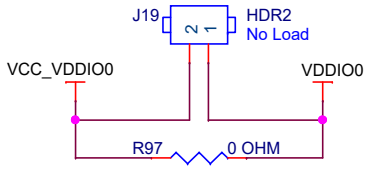
VDDIO_WL & VDDIO2 Current Measurement



VDDIO0 Voltage Selection



VDDIO0 Current Measurement



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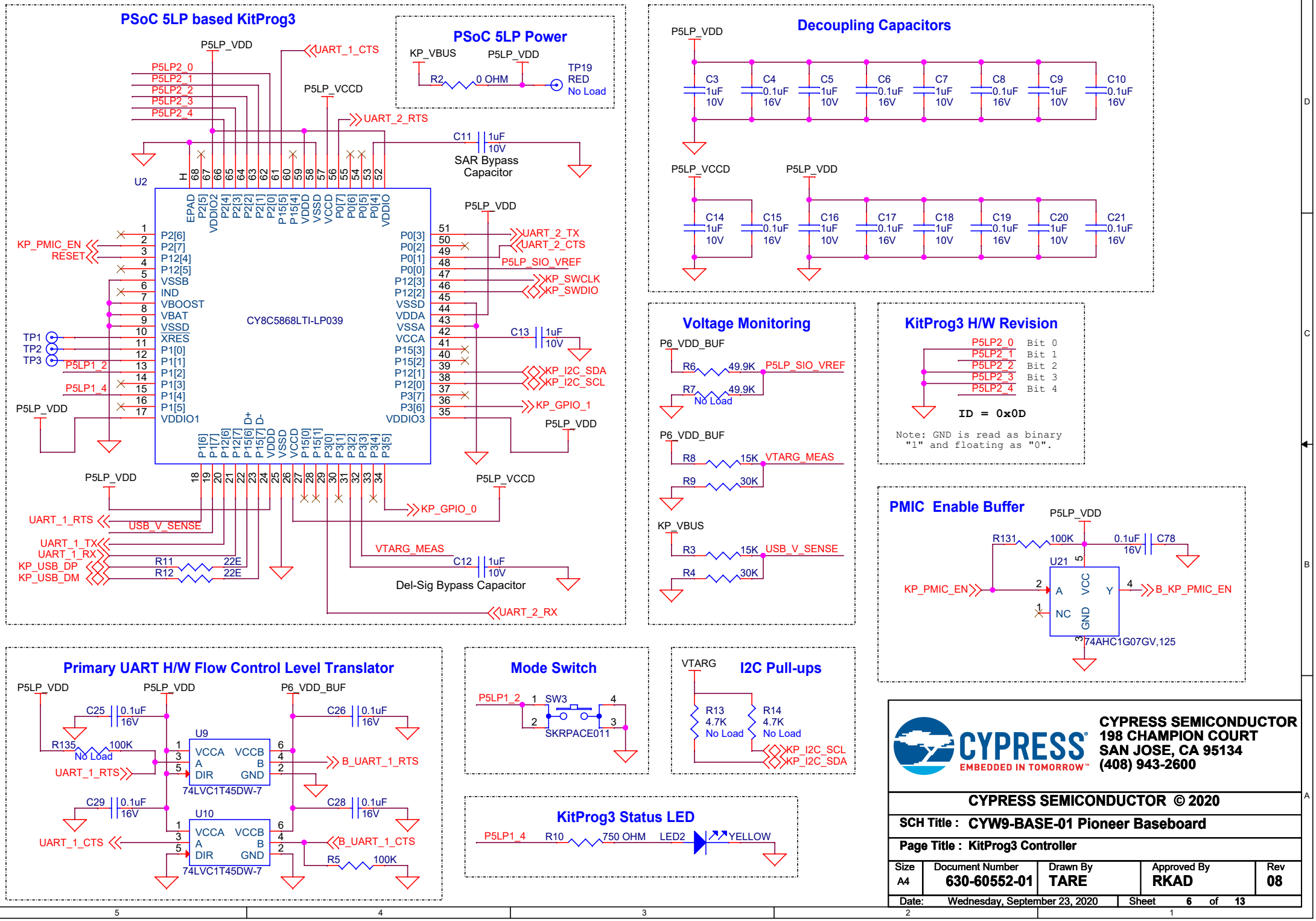
SCH Title : CYW9-BASE-01 Pioneer Baseboard				
Page Title : Power Supply (2)				
Size: A4	Document Number: 630-60552-01	Drawn By: TARE	Approved By: RKAD	Rev: 08
Date: Wednesday, September 23, 2020		Sheet 5 of 13		


PSoC 5LP based KitProg3
CY8C5868LTI-LP039
U2
P5LP_VDD
P5LP_VCCD
UART_1_CTS
UART_2_RTS
C11 1uF 10V
SAR Bypass Capacitor
P5LP2_0
P5LP2_1
P5LP2_2
P5LP2_3
P5LP2_4
KP_PMIC_EN
RESET
TP1
TP2
TP3
P5LP1_2
P5LP1_4
UART_2_TX
UART_2_CTS
P5LP_SIO_VREF
KP_SWCLK
KP_SWDIO
C13 1uF 10V
KP_I2C_SDA
KP_I2C_SCL
KP_GPIO_1
KP_GPIO_0
UART_1_RTS
USB_V_SENSE
UART_1_TX
UART_1_RX
KP_USB_DP
KP_USB_DM
R11 22E
R12 22E
VTARG_MEASS
C12 1uF 10V
Del-Sig Bypass Capacitor
UART_2_RX
PSoC 5LP Power
KP_VBUS
R2 0 OHM
TP19 RED No Load
Decoupling Capacitors
C3 1uF 10V
C4 0.1uF 16V
C5 1uF 10V
C6 0.1uF 16V
C7 1uF 10V
C8 0.1uF 16V
C9 1uF 10V
C10 0.1uF 16V
C14 1uF 10V
C15 0.1uF 16V
C16 1uF 10V
C17 0.1uF 16V
C18 1uF 10V
C19 0.1uF 16V
C20 1uF 10V
C21 0.1uF 16V
Voltage Monitoring
P6_VDD_BUF
R6 49.9K
R7 49.9K No Load
R8 15K
R9 30K
VTARG_MEAS
R3 15K
R4 30K
USB_V_SENSE
KitProg3 H/W Revision
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
ID = 0x0D
Note: GND is read as binary "1" and floating as "0".
PMIC Enable Buffer
R131 100K
0.1uF 16V C78
U21
74AHC1G07GV,125
B_KP_PMIC_EN
Primary UART H/W Flow Control Level Translator
U9
U10
74LVC1T45DW-7
C25 0.1uF 16V
C26 0.1uF 16V
C28 0.1uF 16V
C29 0.1uF 16V
R135 100K No Load
B_UART_1_RTS
B_UART_1_CTS
R5 100K
Mode Switch
SW3
SKRPACE011
I2C Pull-ups
R13 4.7K No Load
R14 4.7K No Load
KitProg3 Status LED
R10 750 OHM
LED2
YELLOW
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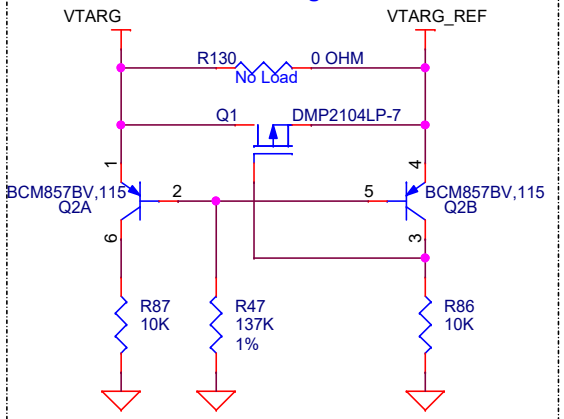
SCH Title : CYW9-BASE-01 Pioneer Baseboard
Page Title : KitProg3 Controller
Size A4
Document Number 630-60552-01
Drawn By TARE
Approved By RKAD
Rev 08
Date: Wednesday, September 23, 2020
Sheet 6 of 13

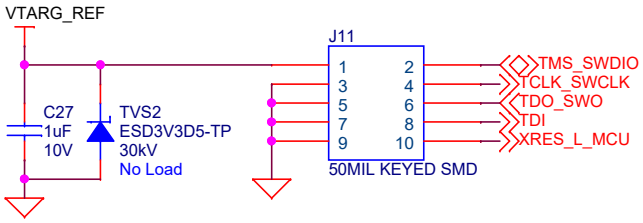
VTARG Reverse Voltage Protection



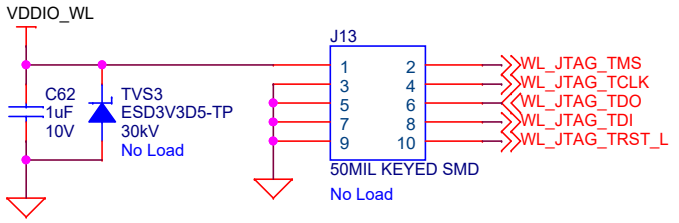
Note: VTARG_REF is only output voltage sense line for external debuggers. PSoC 64 MCU can't be powered using external debugging headers J11 and J12.

Note: If R130 is loaded and external power is used, make sure to remove jumper shunt from J14 to prevent reverse voltage to on-board regulator.

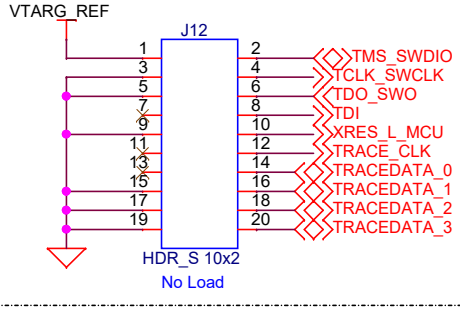
MCU 10-pin SWD/JTAG Header



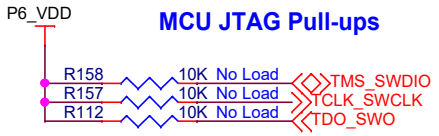
CYW4343W 10-pin SWD/JTAG Header



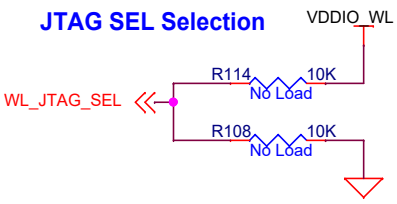
MCU 20-pin ETM Header



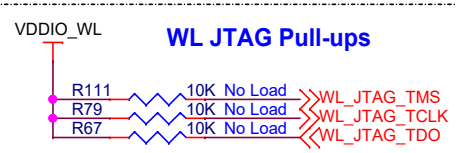
MCU JTAG Pull-ups



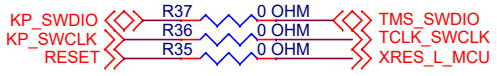
JTAG SEL Selection



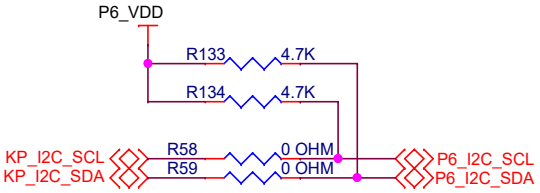
WL JTAG Pull-ups



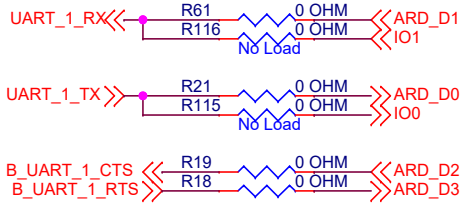
MCU SWD KitProg3 Interface



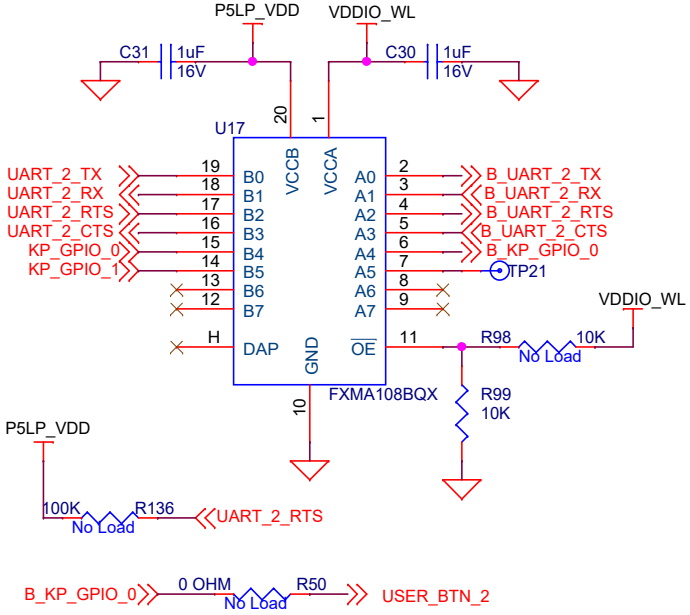
KitProg3 I2C Interface



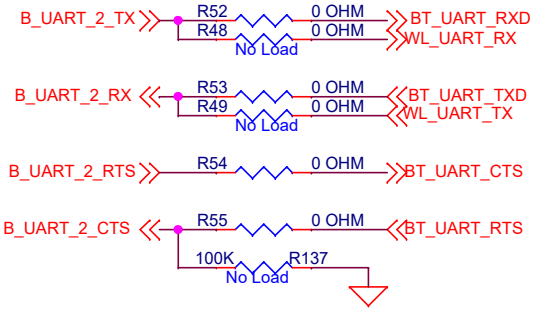
KitProg3 UART Interface



KitProg3 Level Translator for Secondary UART and GPIO



KitProg3 Secondary UART Multiplexing



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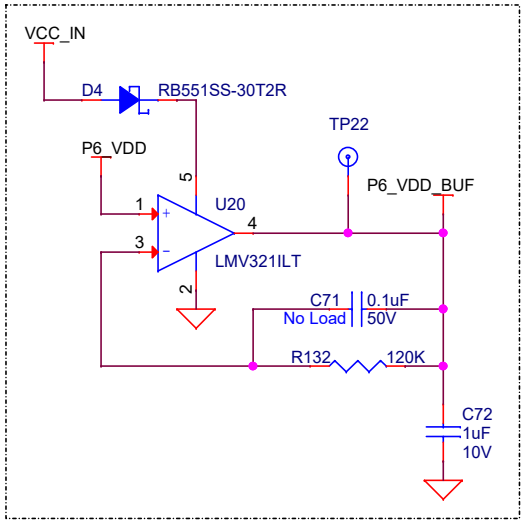
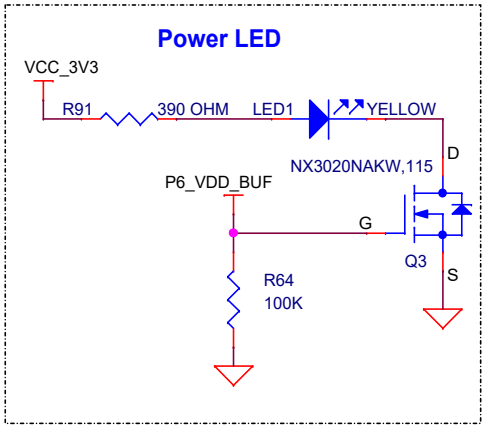
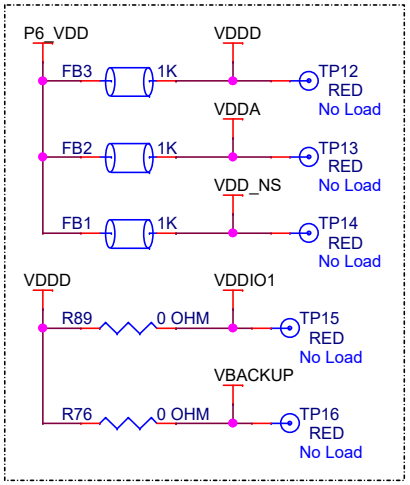
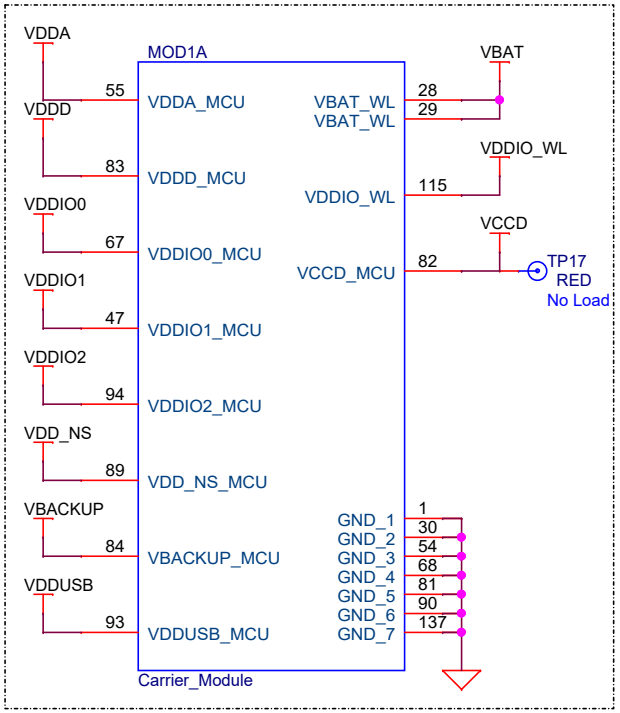
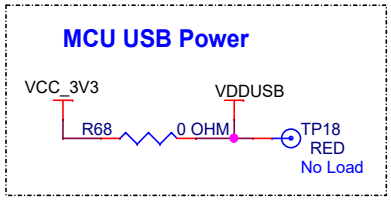
SCH Title : CYW9-BASE-01 Pioneer Baseboard				
Page Title : KitProg3 Power and Headers				
Size: A4	Document Number: 630-60552-01	Drawn By: TARE	Approved By: RKAD	Rev: 08
Date: Wednesday, September 23, 2020		Sheet 7 of 13		

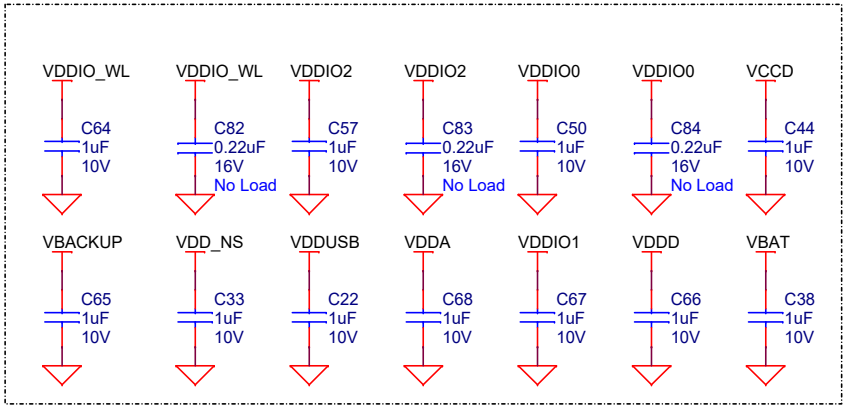












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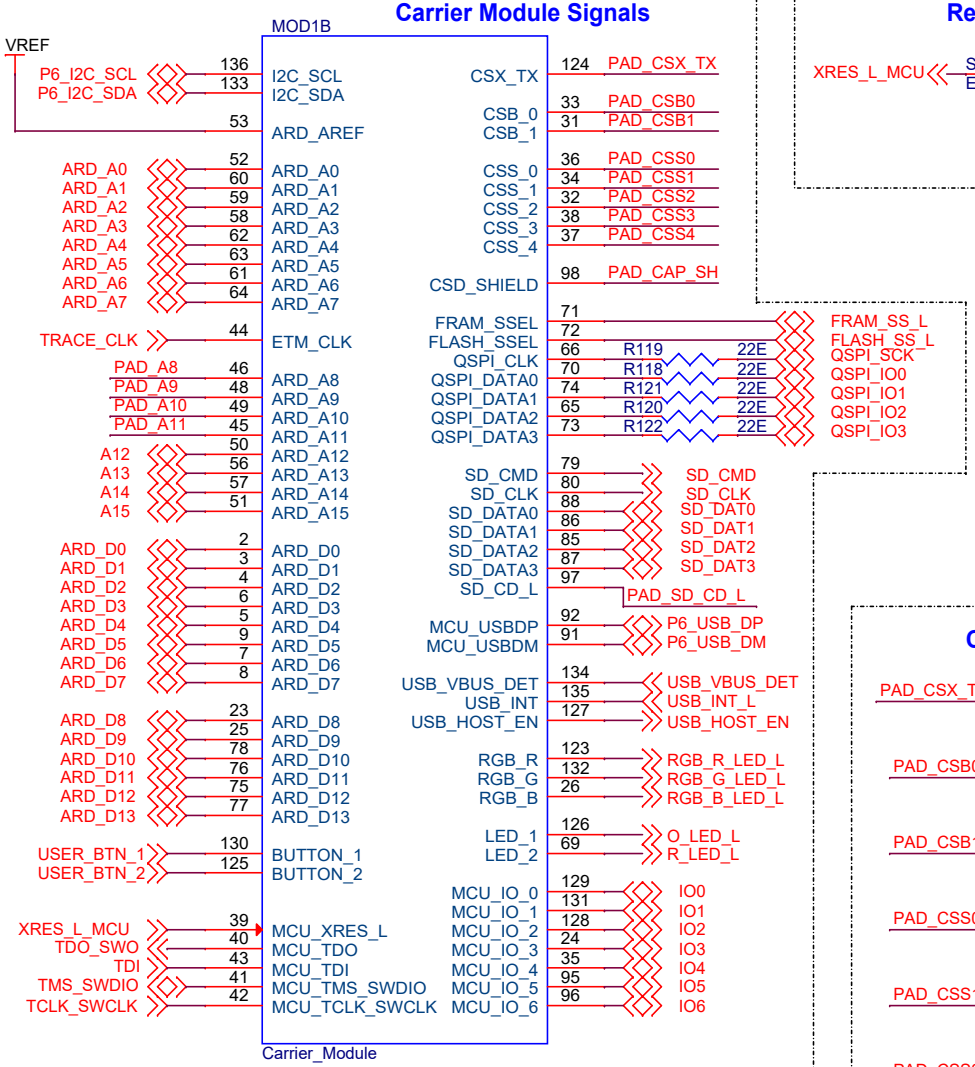
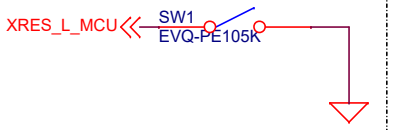
SCH Title : CYW9-BASE-01 Pioneer Baseboard				
Page Title : Carrier Module Power				
Size: A4	Document Number: 630-60552-01	Drawn By: TARE	Approved By: RKAD	Rev: 08
Date: Wednesday, September 23, 2020		Sheet 8 of 13		

Carrier Module Signals

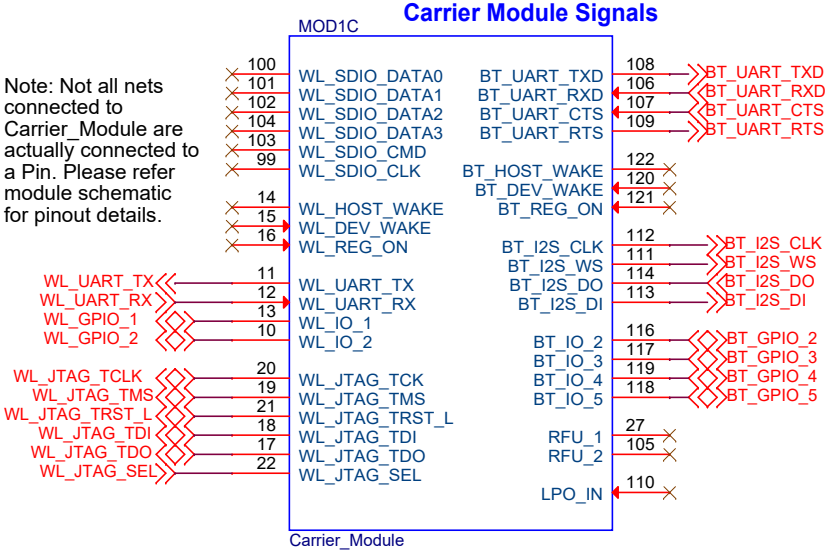


Reset Button

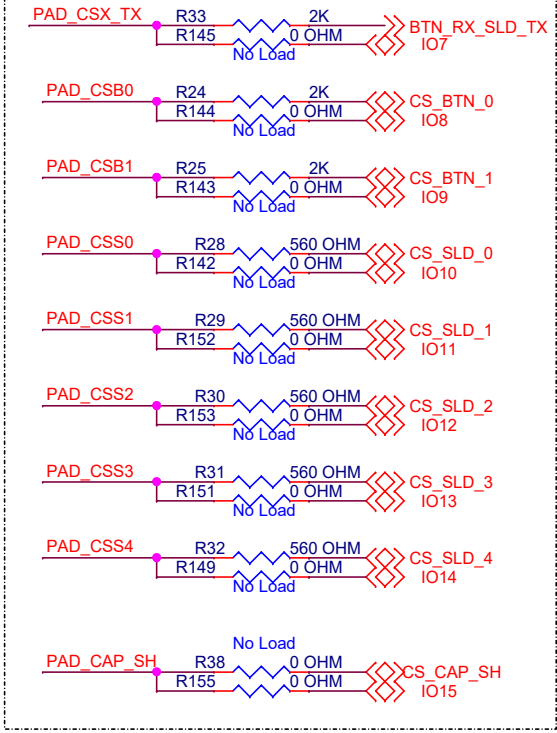


Carrier Module Signals

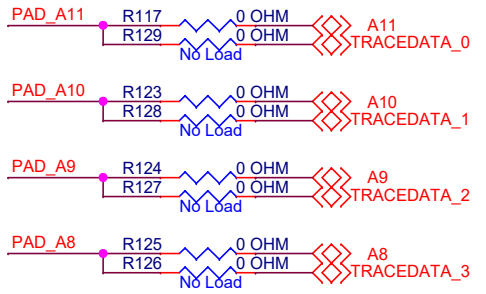
Note: Not all nets connected to Carrier_Module are actually connected to a Pin. Please refer module schematic for pinout details.



CapSense Multiplexed Pins



TRACE Multiplexed Pins



P6_USB_ID

Card Detect Multiplexing

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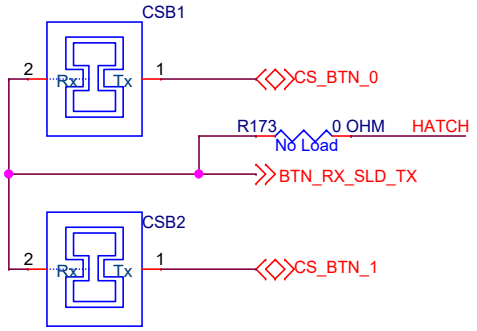
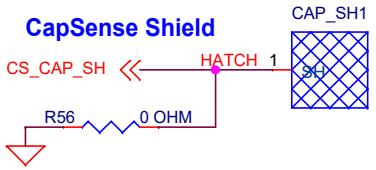
Page Title : Carrier Module Signals				
Size: A4	Document Number: 630-60552-01	Drawn By: TARE	Approved By: RKAD	Rev: 08
Date: Wednesday, September 23, 2020		Sheet 9 of 13		

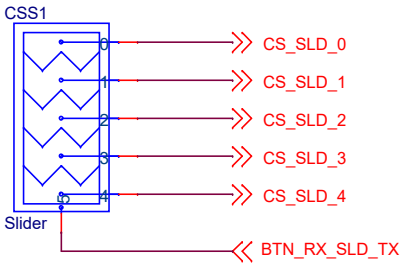
CapSense Buttons



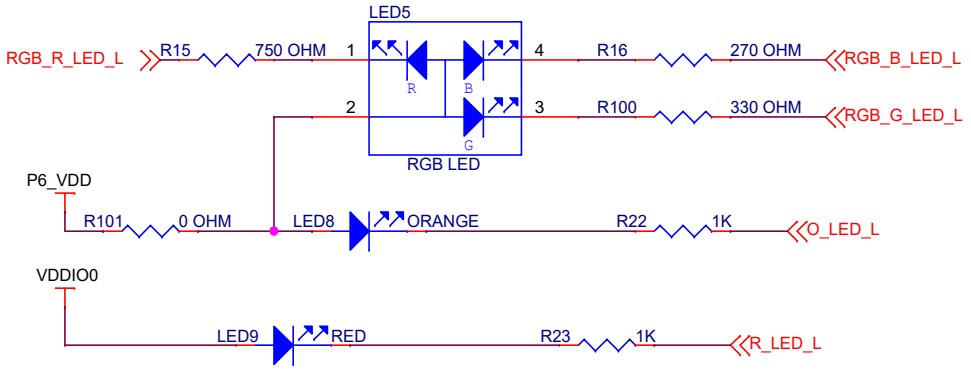
CapSense Shield



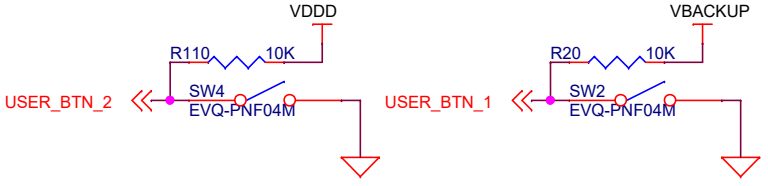
CapSense Slider



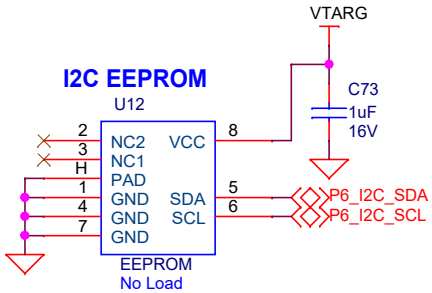
User LEDs



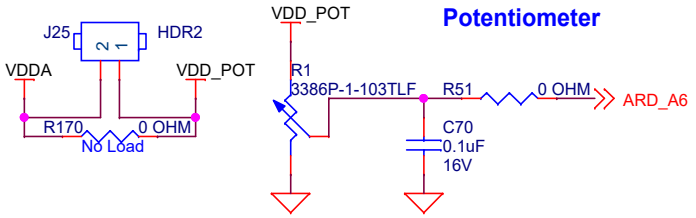
User Buttons / Hibernate Wakeup



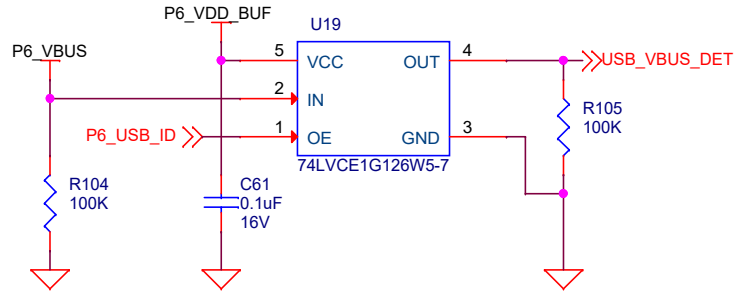
I2C EEPROM



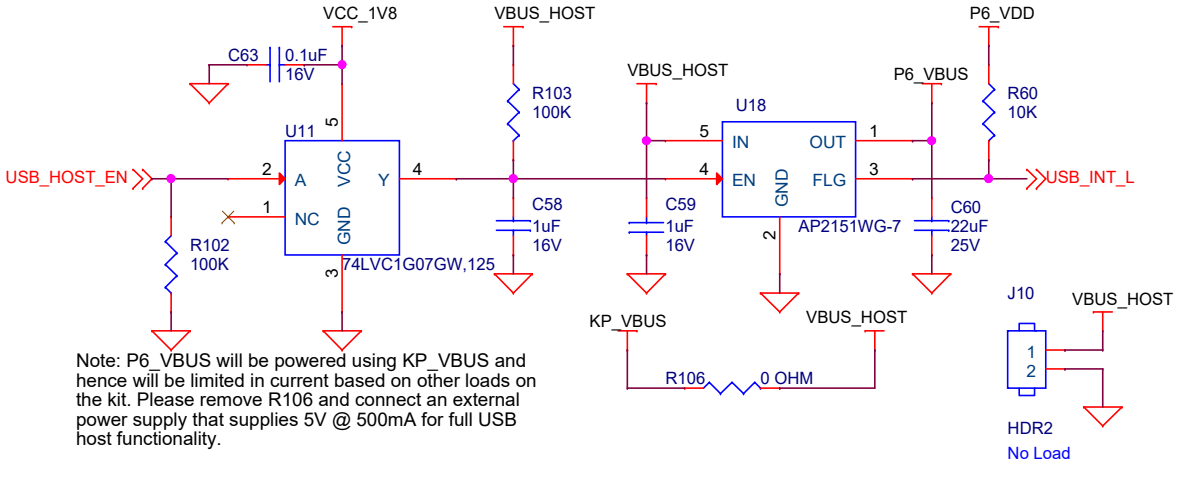
Potentiometer



USB Device Port VBUS Detect



USB Host VBUS Enable



Note: P6_VBUS will be powered using KP_VBUS and hence will be limited in current based on other loads on the kit. Please remove R106 and connect an external power supply that supplies 5V @ 500mA for full USB host functionality.

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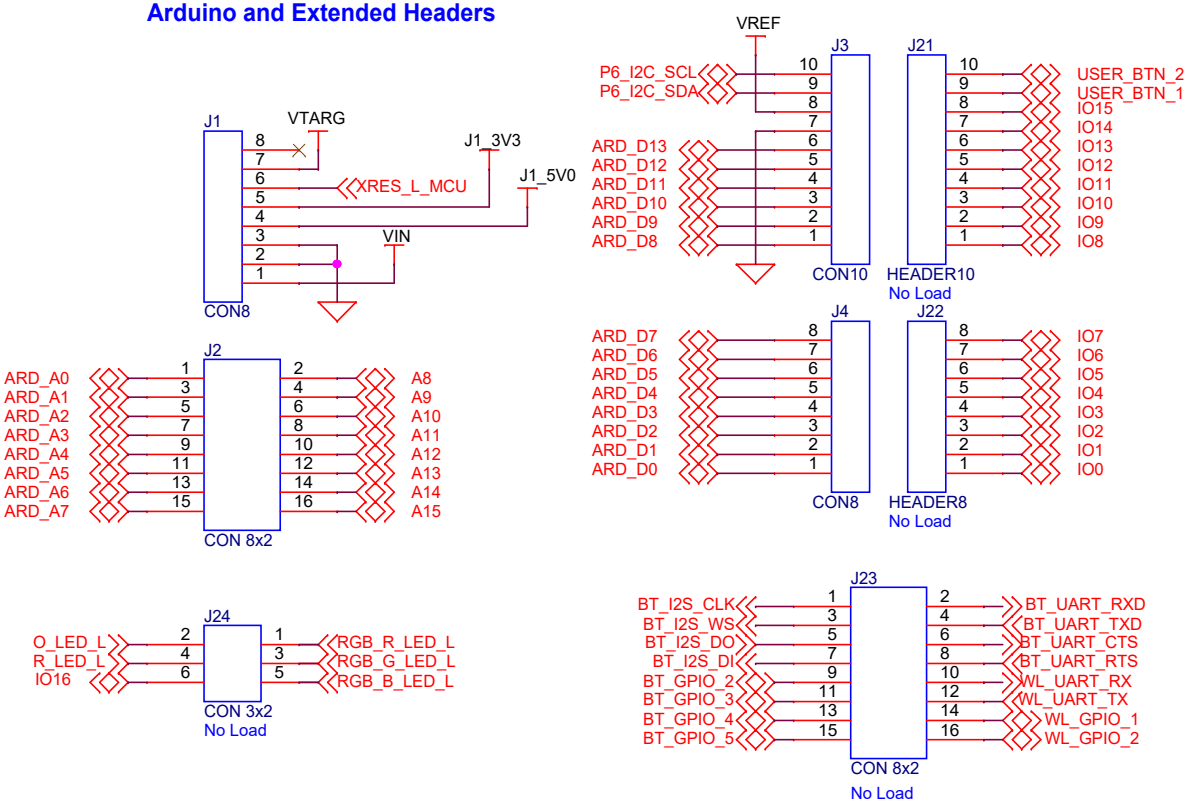
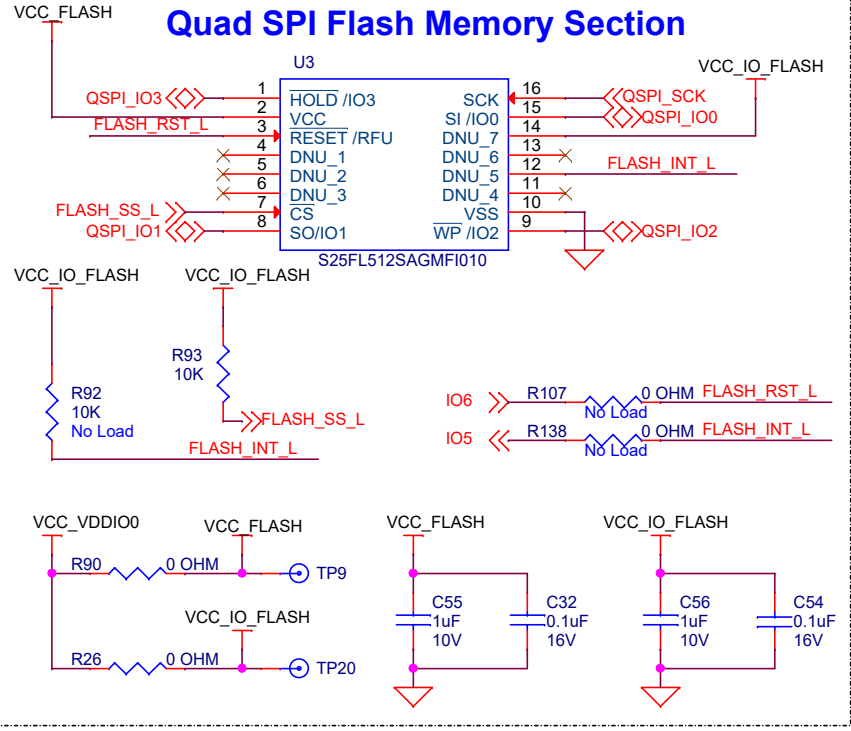
SCH Title : CYW9-BASE-01 Pioneer Baseboard				
Page Title : Peripherals				
Size: A4	Document Number: 630-60552-01	Drawn By: TARE	Approved By: RKAD	Rev: 08
Date: Wednesday, September 23, 2020		Sheet 10 of 13		

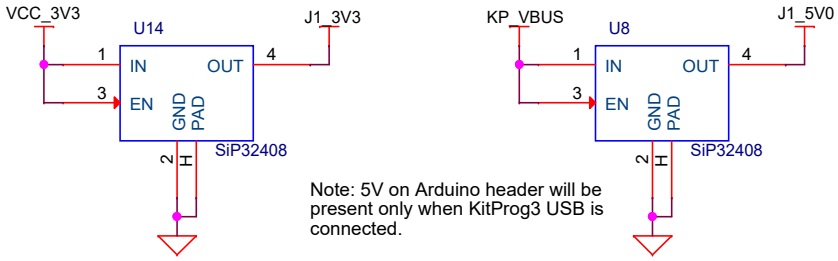
Arduino and Extended Headers



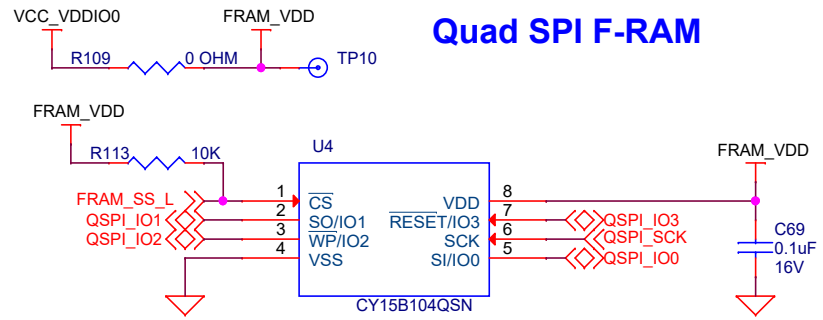
Quad SPI Flash Memory Section



Arduino Header O/P



Quad SPI F-RAM



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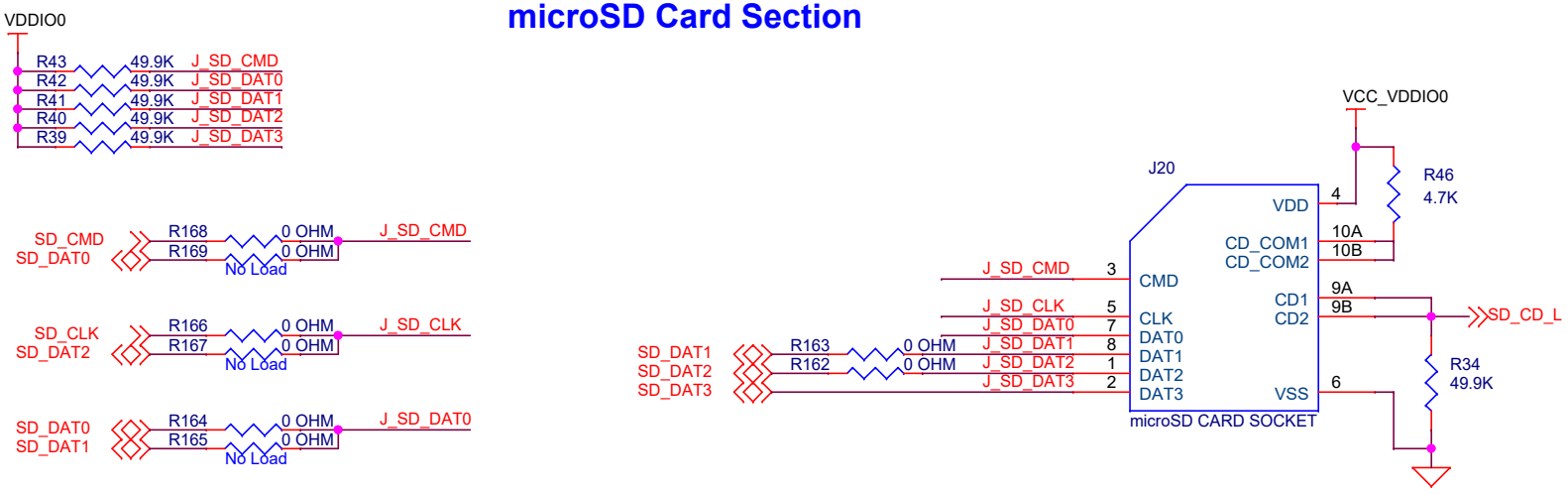
SCH Title : CYW9-BASE-01 Pioneer Baseboard				
Page Title : Expansion Headers & Memory				
Size: A4	Document Number: 630-60552-01	Drawn By: TARE	Approved By: RKAD	Rev: 08
Date: Wednesday, September 23, 2020		Sheet 11 of 13		

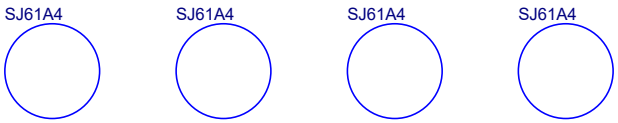
microSD Card Section

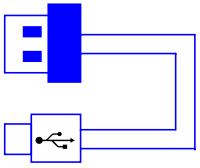


Note: Load R165, R167 and R169 and remove R162, R163, R164, R166 and R168 to change from SDHC to SPI interface for microSD card.

Accessories

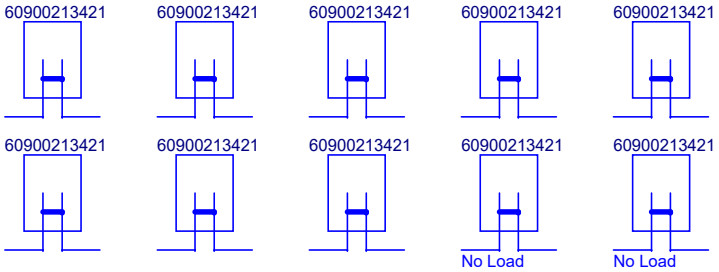
Cylindrical Bump-ons





PCBA label

Jumper Shunts



Acrylic Overlay

Overlay

Color: Clear, Transparent
Finish: Matt

Dimensions:
45.21mm - length
36.93mm - height
1mm - thickness

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Page Title : microSD card & Accessories				
Size: A4	Document Number: 630-60552-01	Drawn By: TARE	Approved By: RKAD	Rev: 08
Date: Wednesday, September 23, 2020		Sheet 12 of 13		

REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Internal Release	2019/05/13
02	Internal Release	2019/05/21
03	Internal Release	2019/07/23
04	Internal Release	2019/08/08
05	Initial Release	2019/09/18
06	Internal Release	2019/12/09
07	1. Added optional jumper header J26 at VCC_3V3 output voltage selection between 3.3V and 2.5V 2. VCC of USB Device VBUS Detect is changed from VTARG to P6_VDD_BUF	2020/01/28
08	Loaded R133, R134 instead of R13, R14 Kit MPN is modified as CY8CKIT-064S0S2-4343W PSoC 64 Standard Secure - AWS Wi-Fi BT Pioneer Kit	2020/08/06

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Size	Document Number	Drawn By	Approved By	Rev
A4	630-60552-01	TARE	RKAD	08

Date: Thursday, August 06, 2020 Sheet 13 of 13