


**Schematic modified for
CY8CKIT-064B0S2-4343W PSoC 64 Secure Boot Wi-Fi BT Pioneer Kit**

CYW9-BASE-01 Pioneer Baseboard

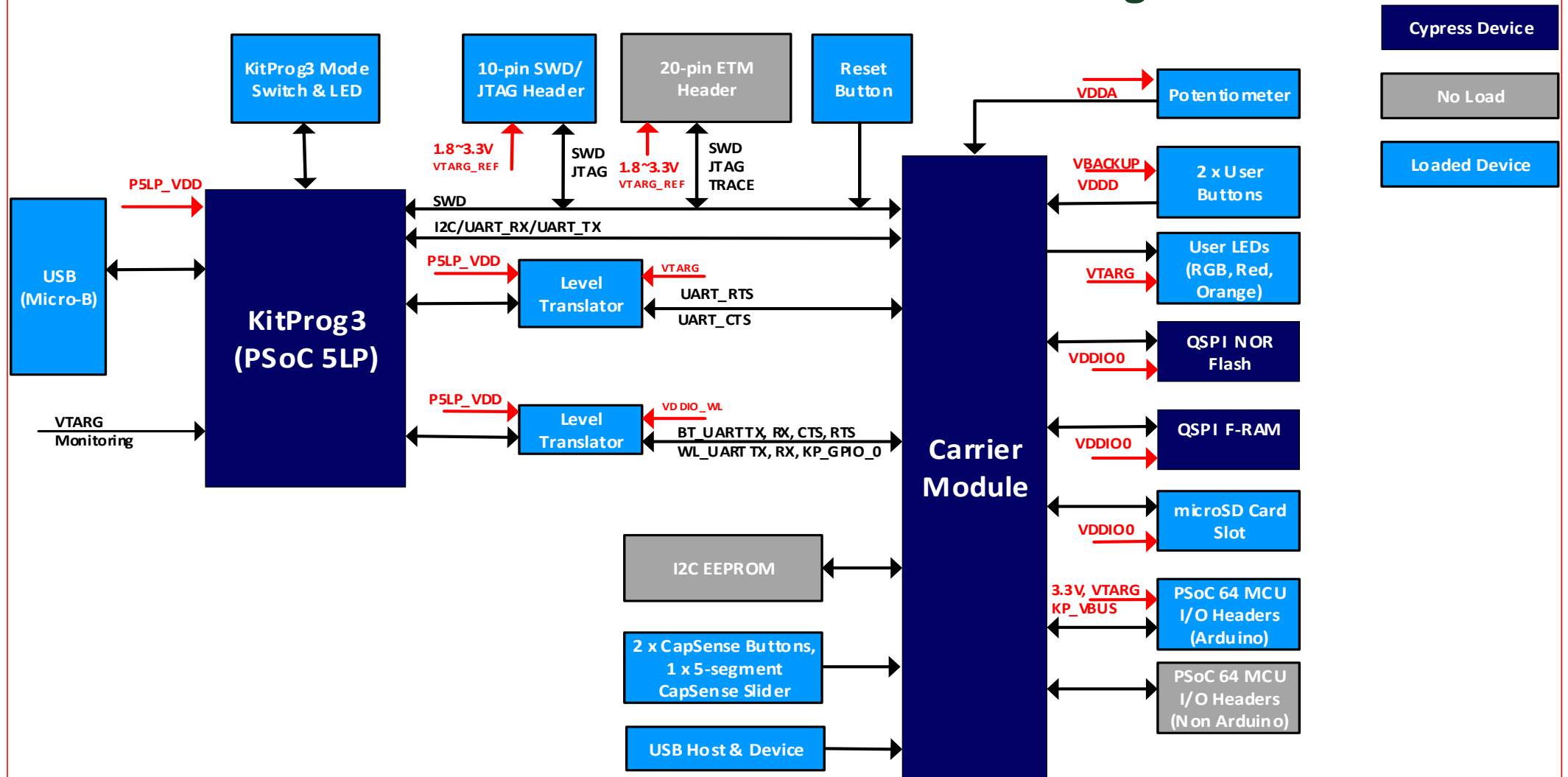
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04	Power Supply (1)
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06	KitProg3 Controller
07	KitProg3 Power and Headers
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Drawing Numbers

PCBA	121-60578-01
PCB	600-60552-01
FAB DRW	610-60552-01
ASSY DRW	620-60552-01
SCH DRW	630-60552-01

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SCH Title : CYW9-BASE-01 Pioneer Baseboard							
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CYW9-BASE-01 Functional Block Diagram



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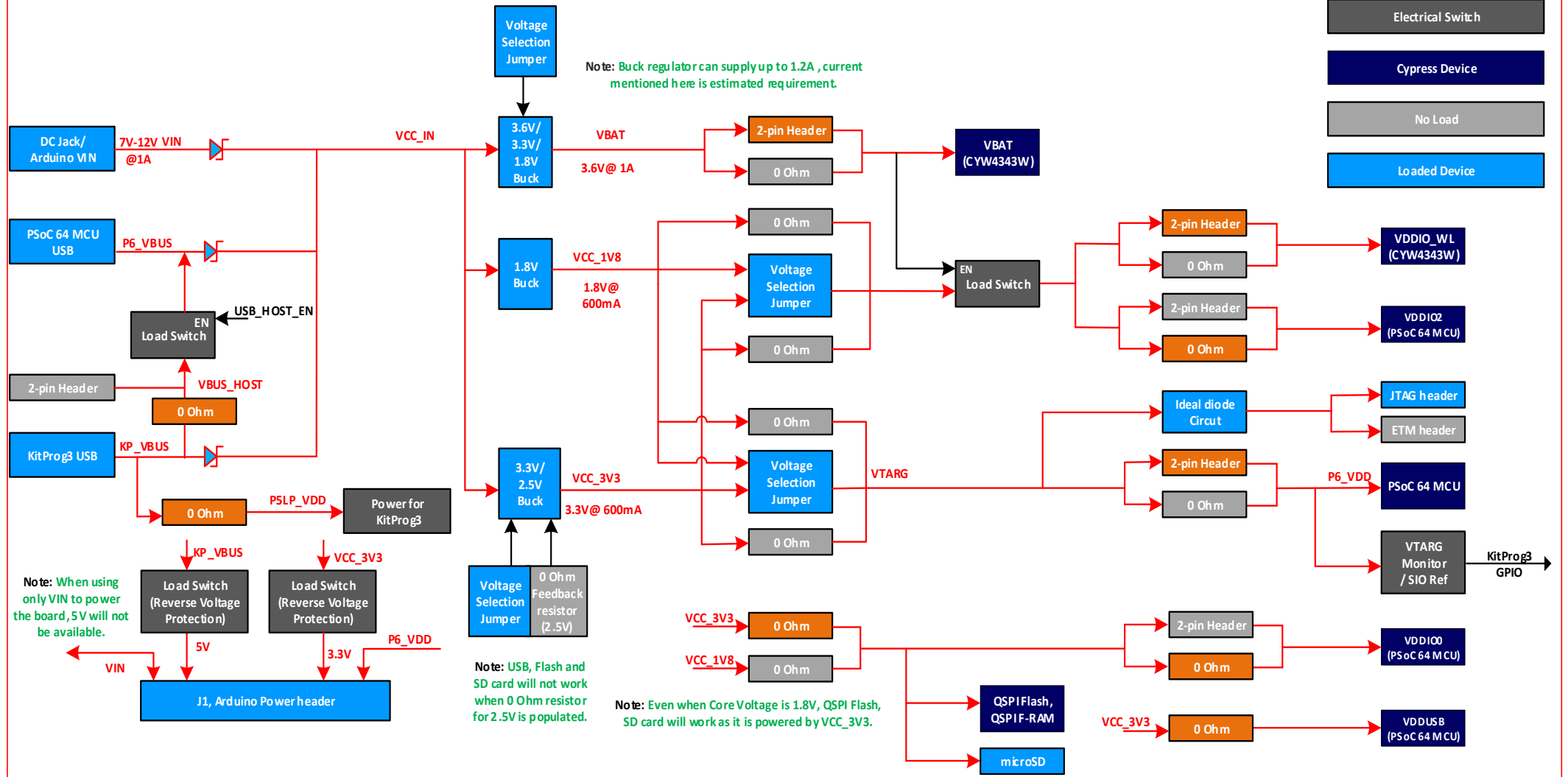
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SCH Title : CYW9-BASE-01 Pioneer Baseboard

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Power Supply Section



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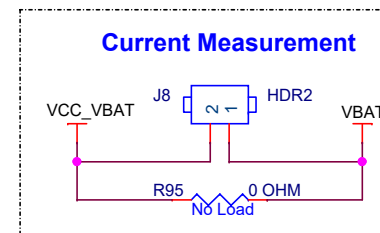
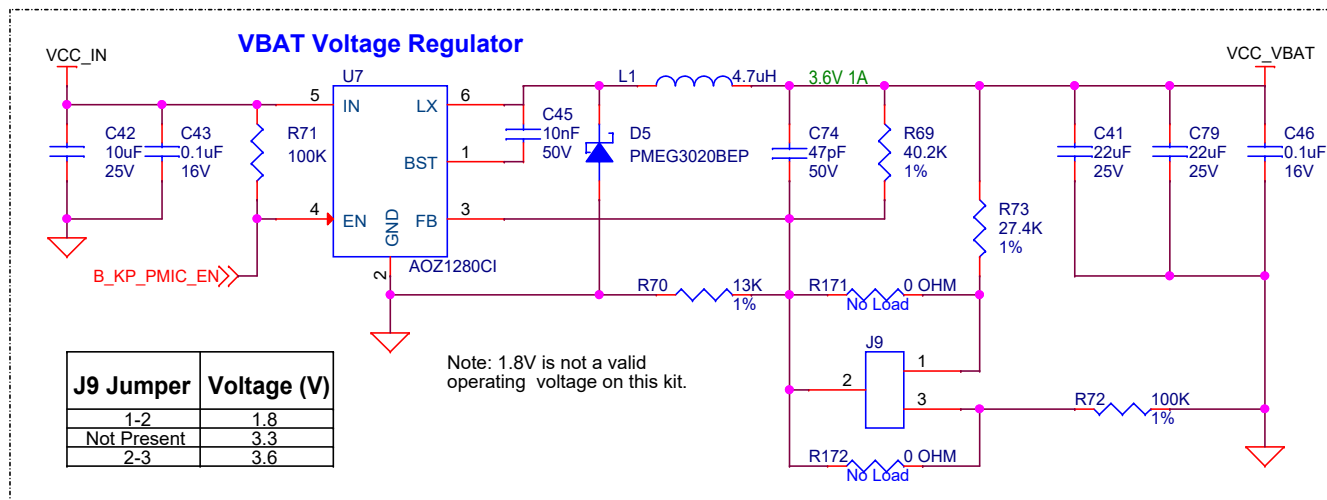
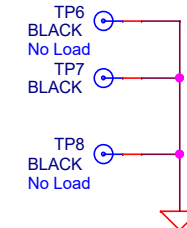
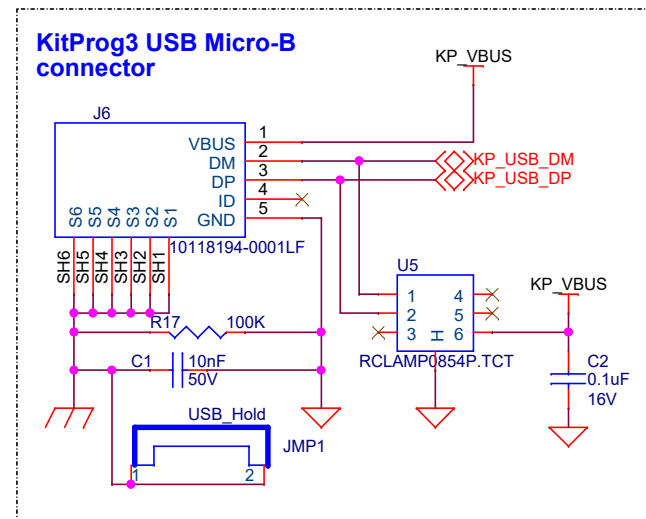
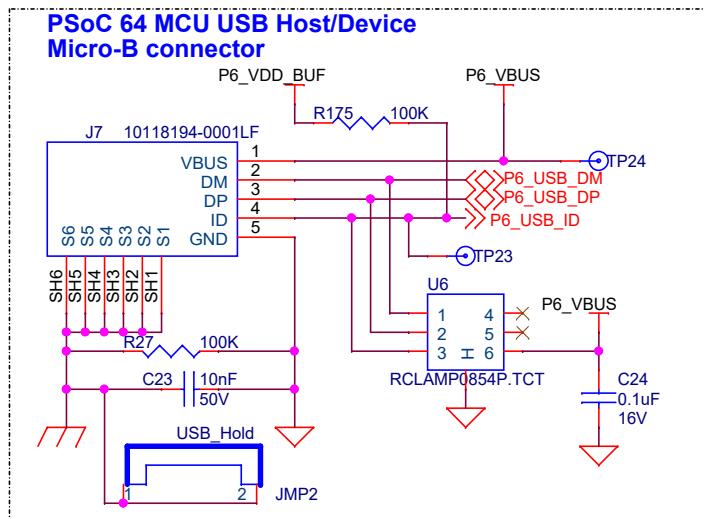
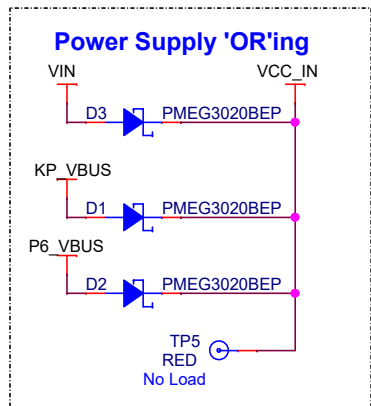
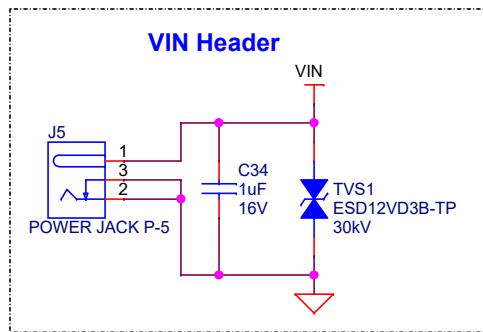
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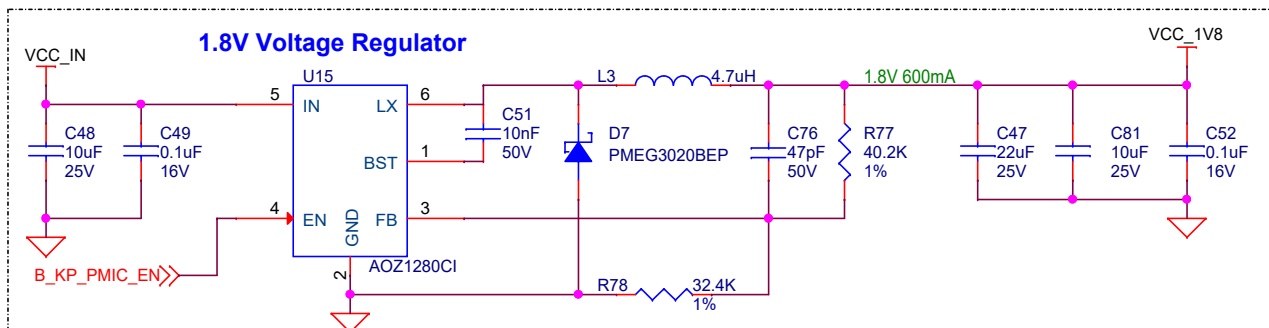
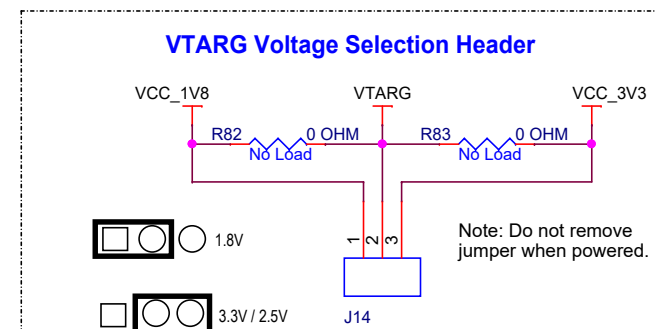
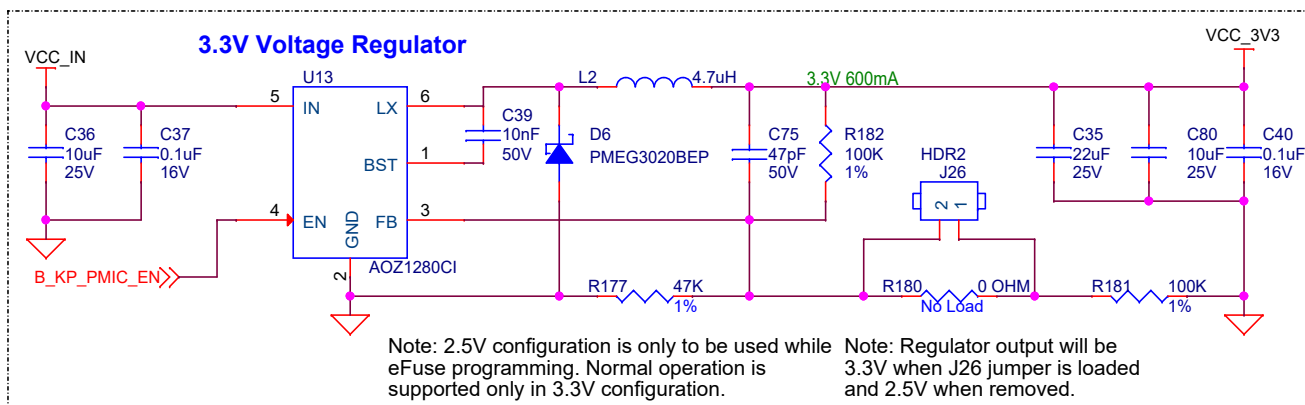
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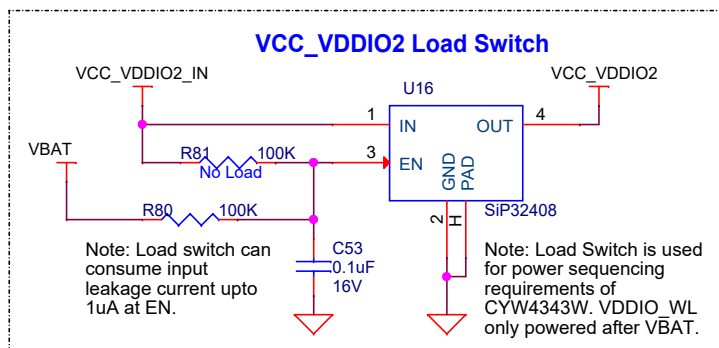
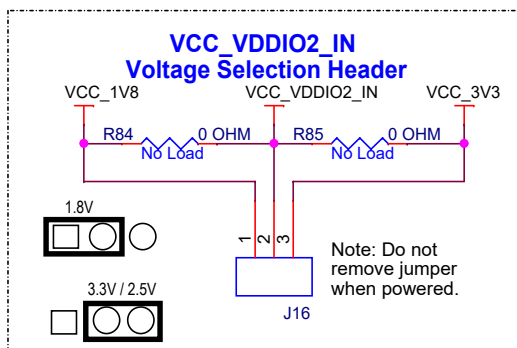
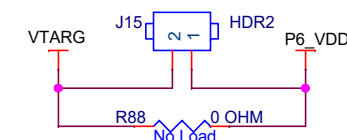


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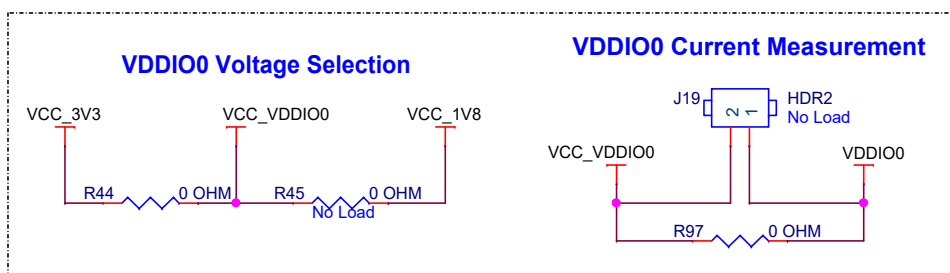
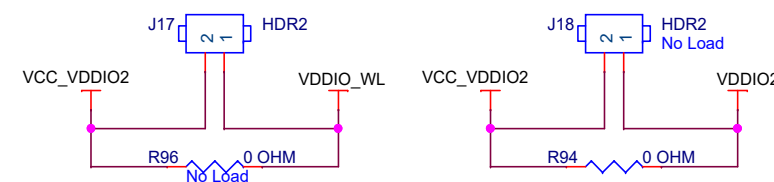
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SCH Title : CYW9-BASE-01 Pioneer Baseboard				
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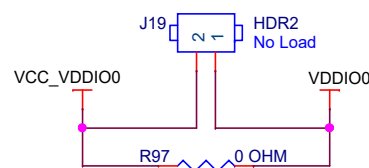
P6_VDD Current Measurement



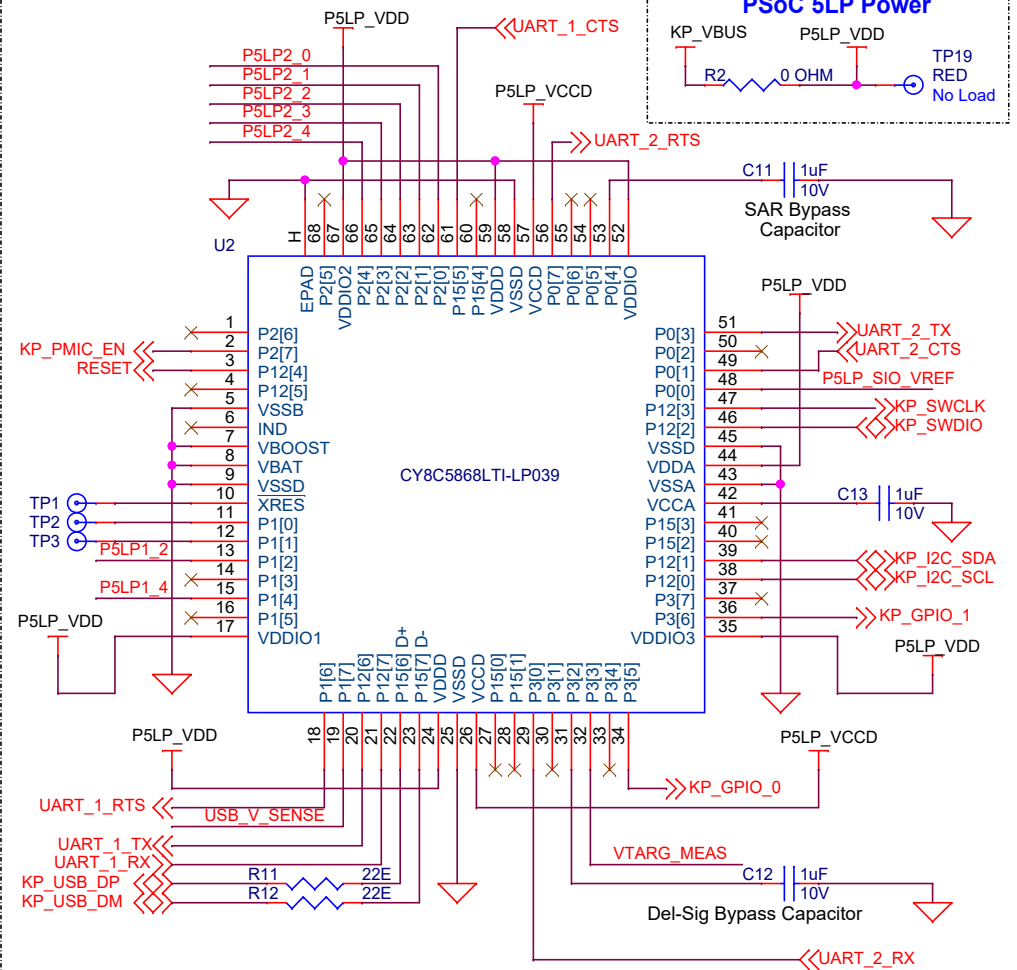
VDDIO_WL & VDDIO2 Current Measurement



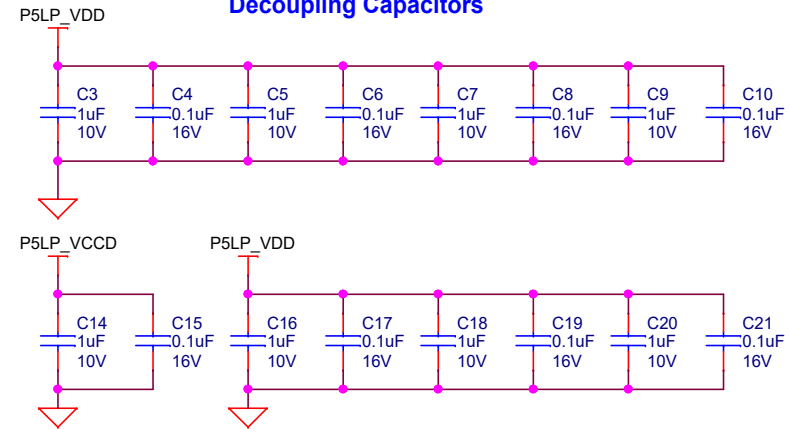
VDDIO0 Current Measurement



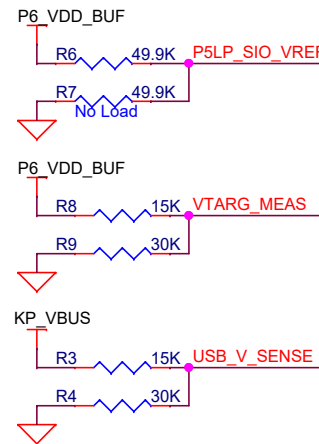
PSoC 5LP based KitProg3



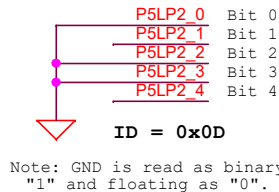
Decoupling Capacitors



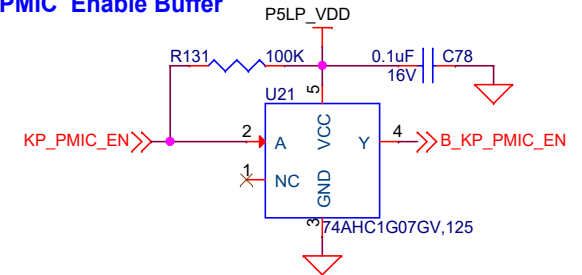
Voltage Monitoring



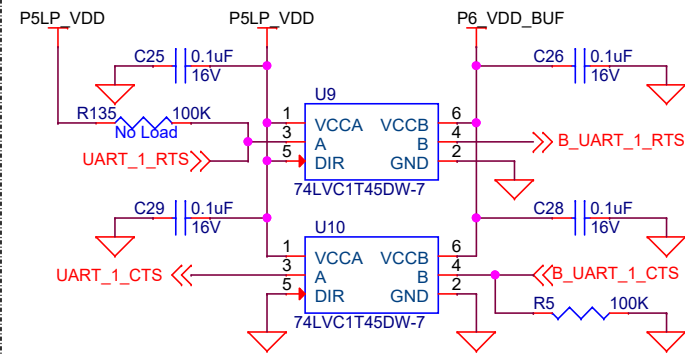
KitProg3 H/W Revision



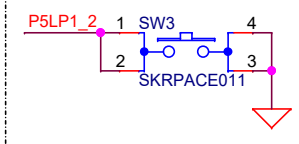
PMIC Enable Buffer



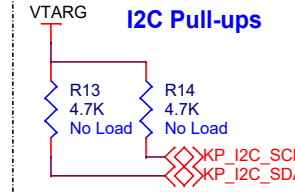
Primary UART H/W Flow Control Level Translator



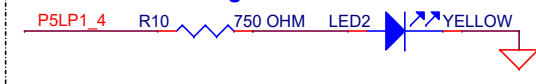
Mode Switch



I2C Pull-ups



KitProg3 Status LED



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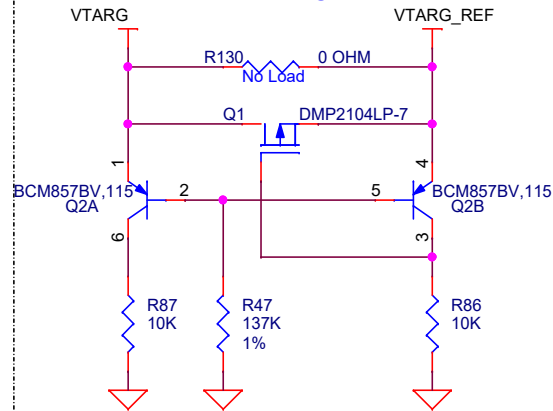
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Page Title : KitProg3 Controller

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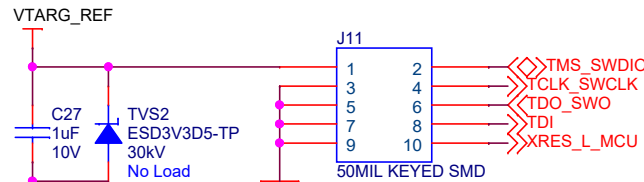
VTARG Reverse Voltage Protection



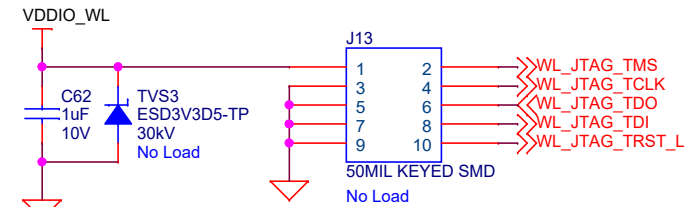
Note: VTARG_REF is only output voltage sense line for external debuggers. PSoC 64 MCU can't be powered using external debugging headers J11 and J12.

Note: If R130 is loaded and external power is used, make sure to remove jumper shunt from J14 to prevent reverse voltage to on-board regulator.

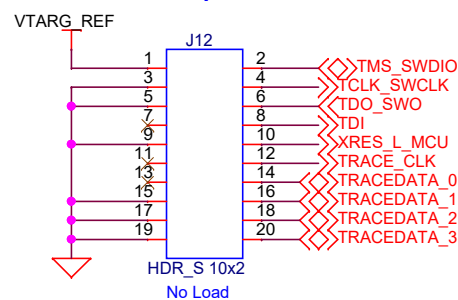
MCU 10-pin SWD/JTAG Header



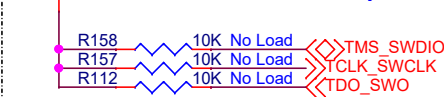
CYW4343W 10-pin SWD/JTAG Header



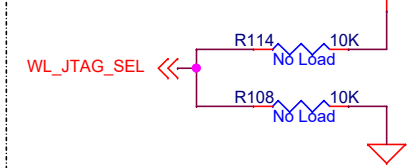
MCU 20-pin ETM Header



MCU JTAG Pull-ups



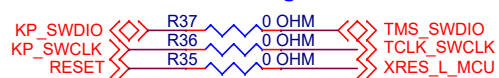
JTAG SEL Selection



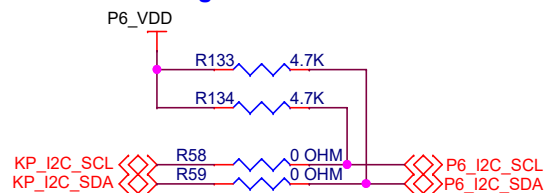
WL JTAG Pull-ups



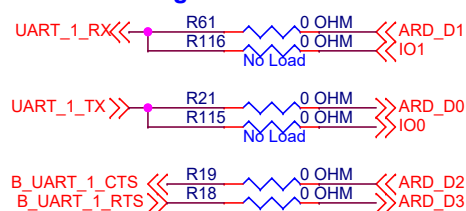
MCU SWD KitProg3 Interface



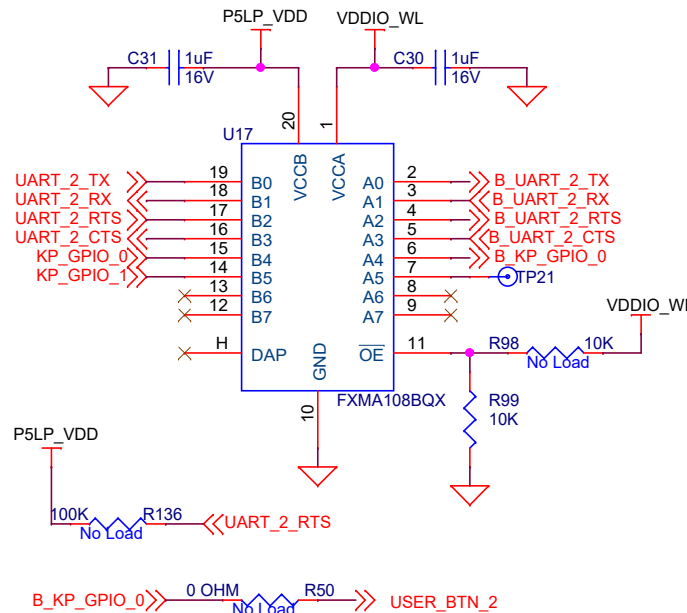
KitProg3 I2C Interface



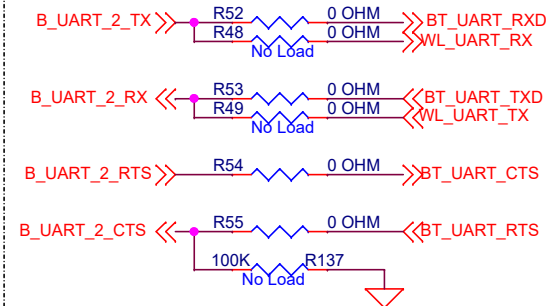
KitProg3 UART Interface



KitProg3 Level Translator for Secondary UART and GPIO



KitProg3 Secondary UART Multiplexing



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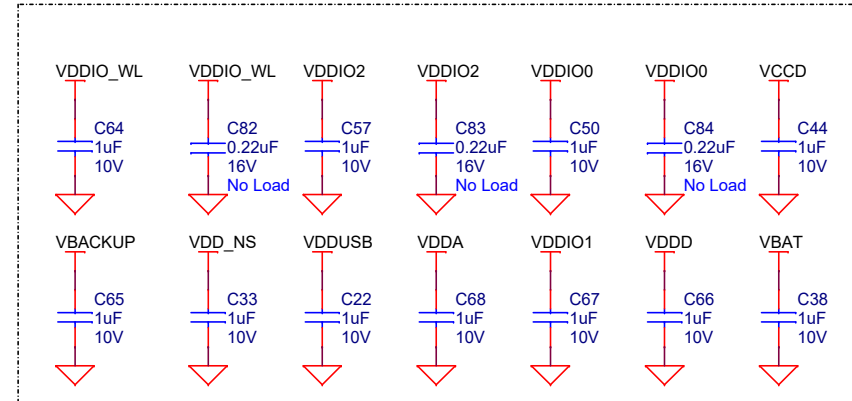
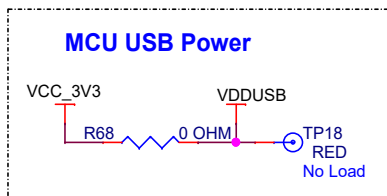
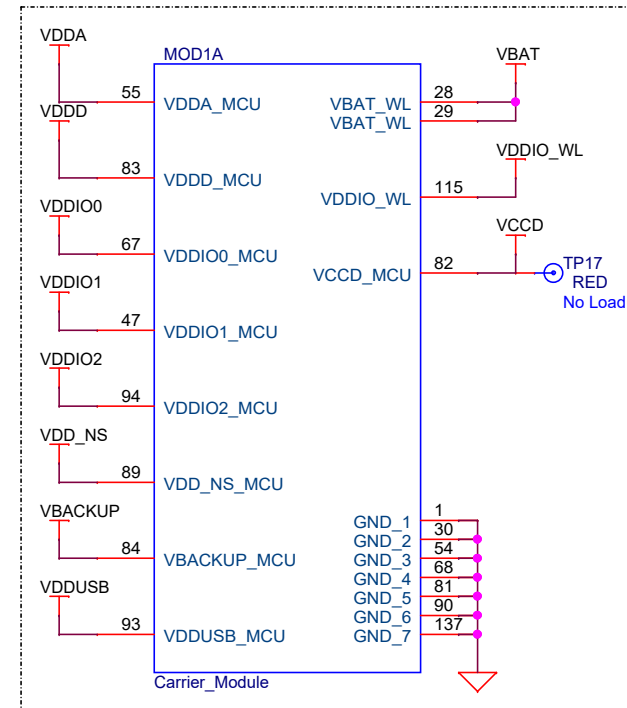
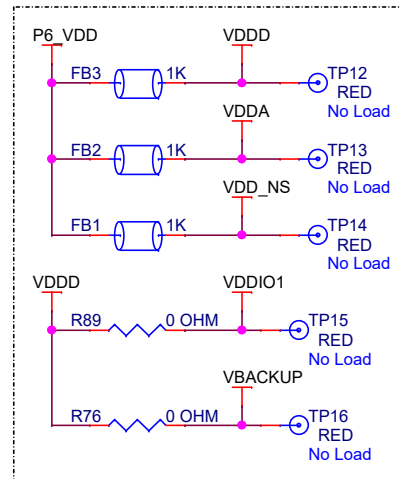
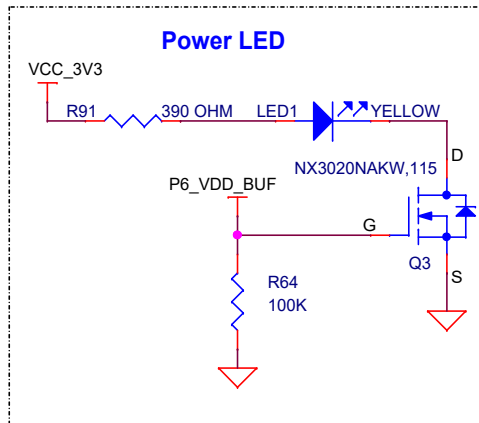
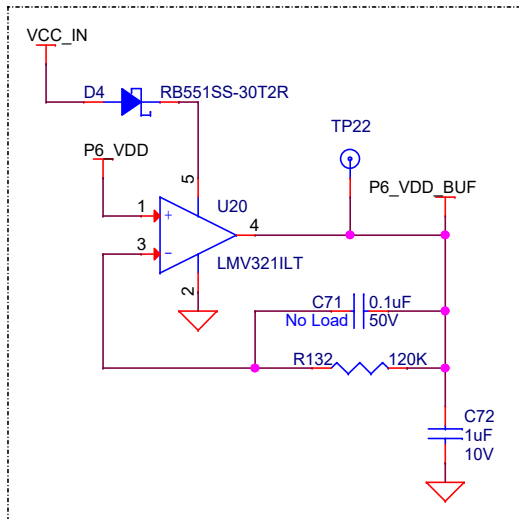
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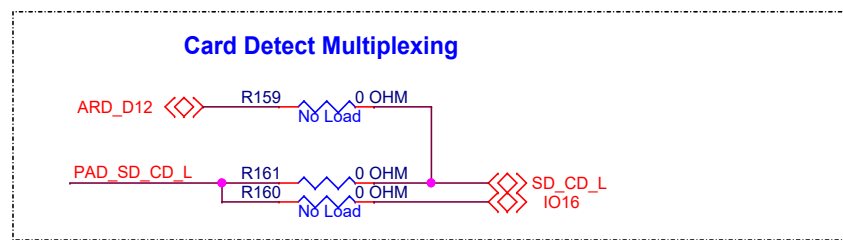
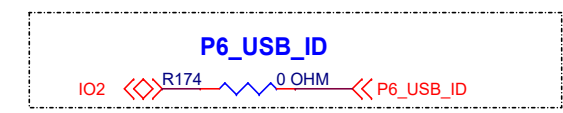
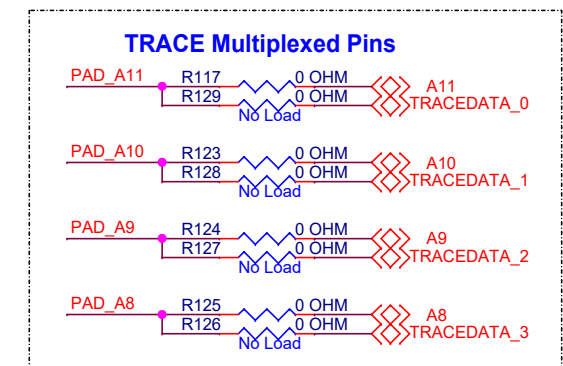
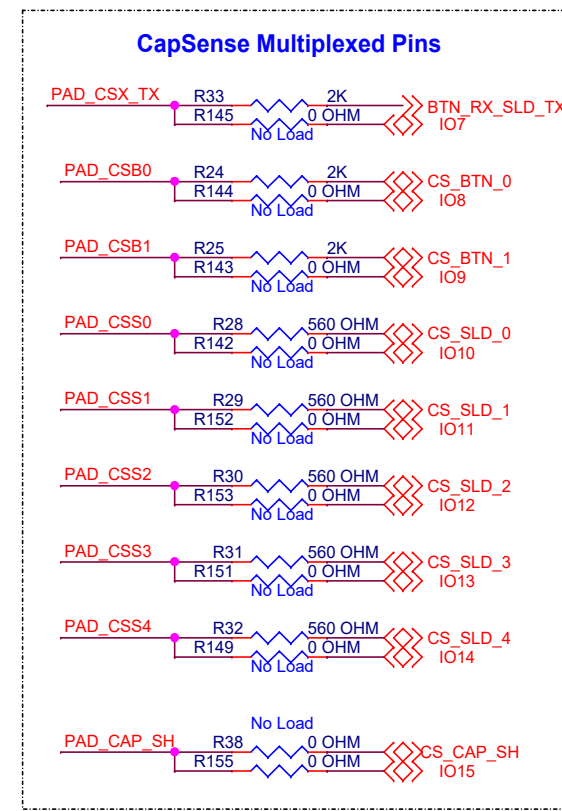
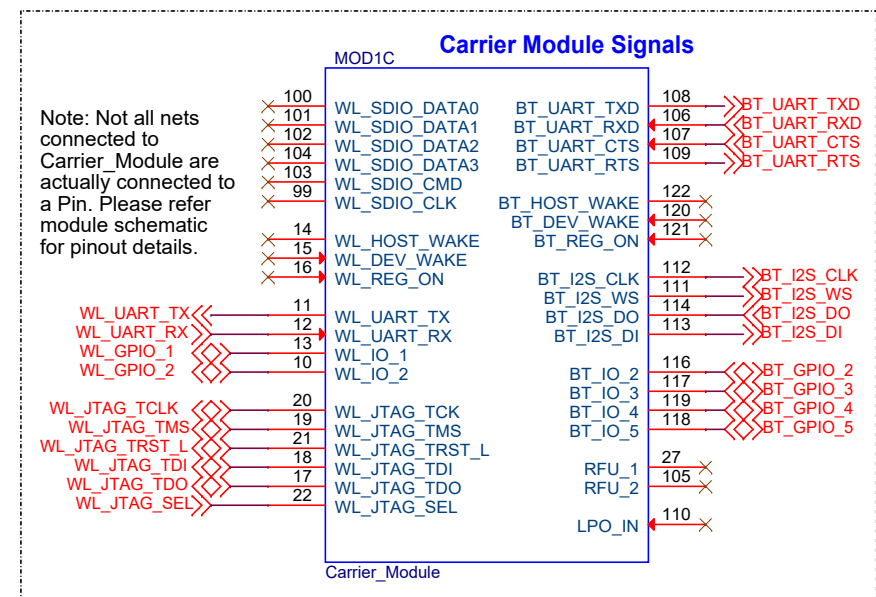
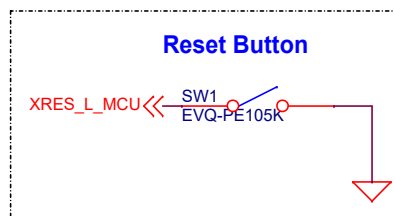
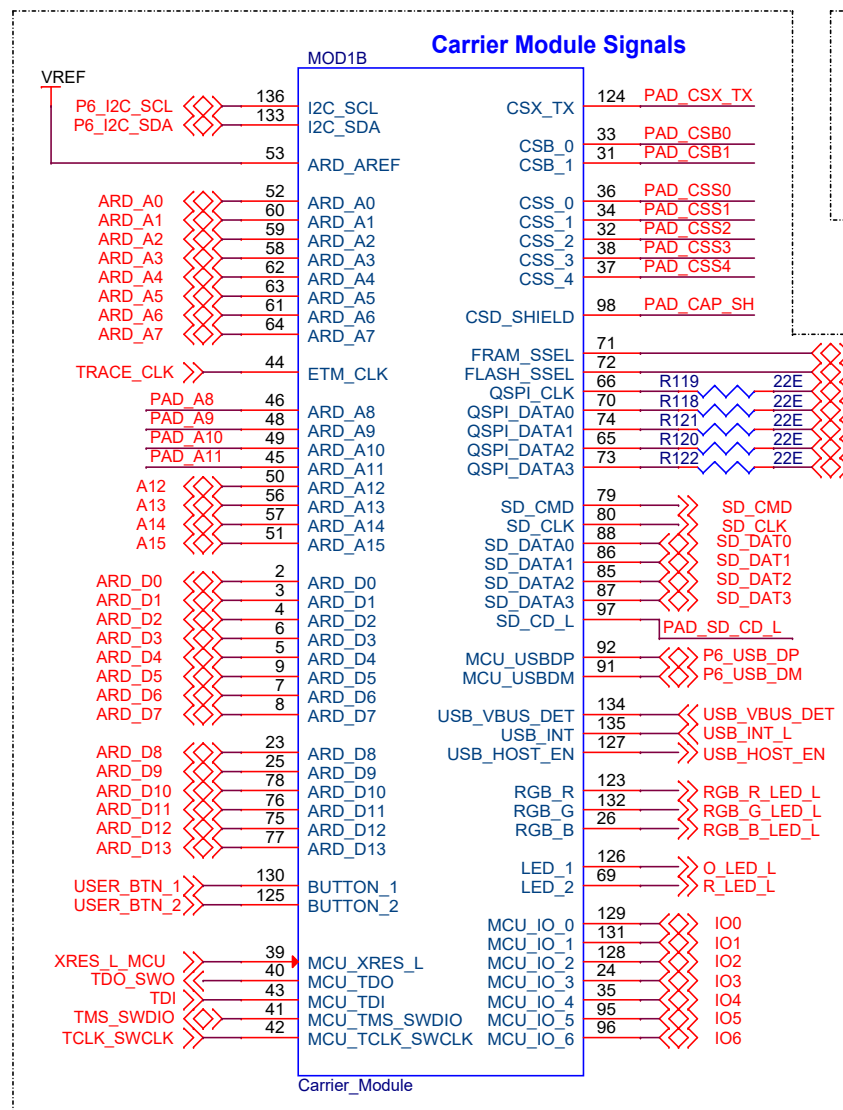
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Page Title : KitProg3 Power and Headers

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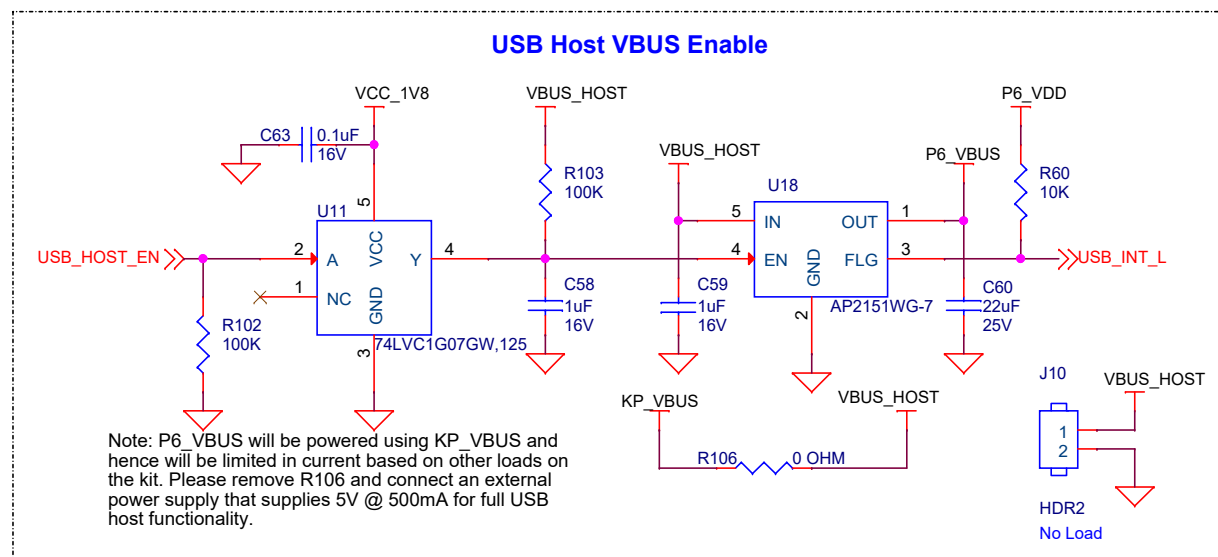
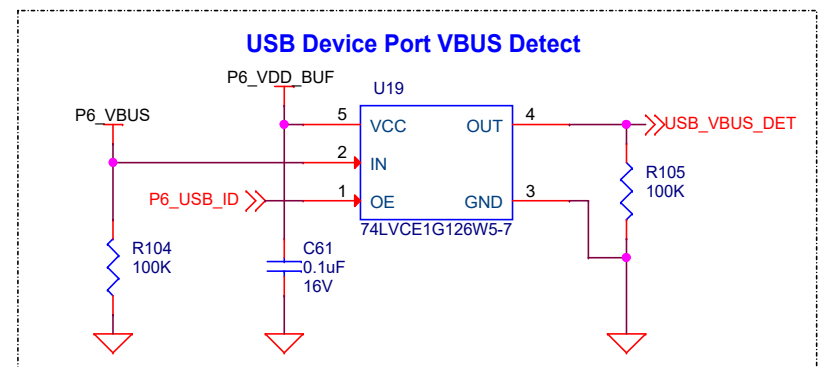
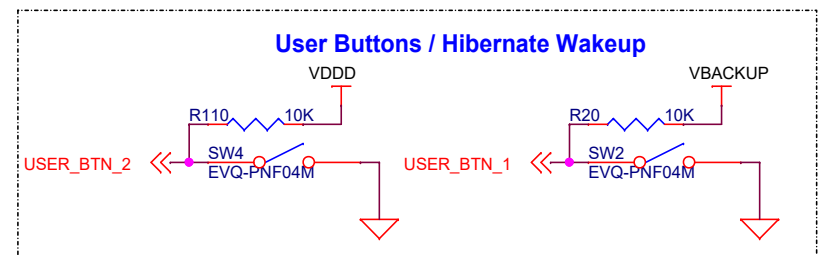
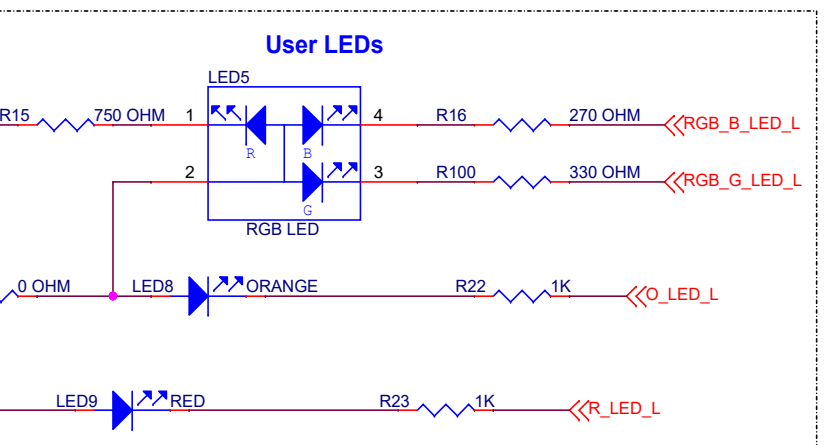
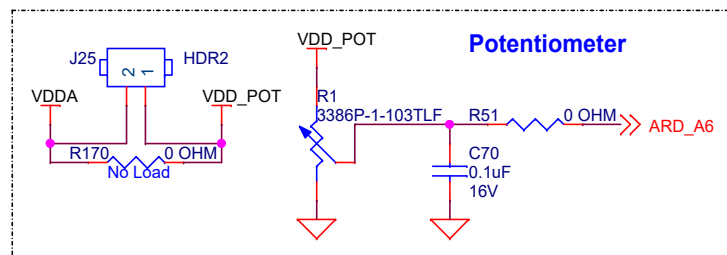
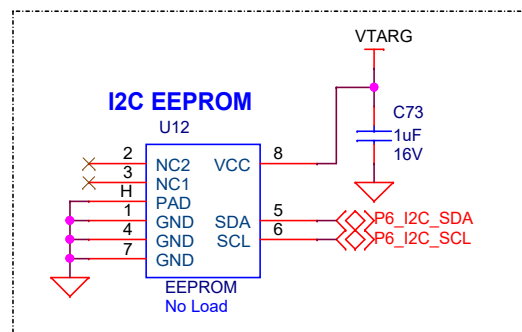
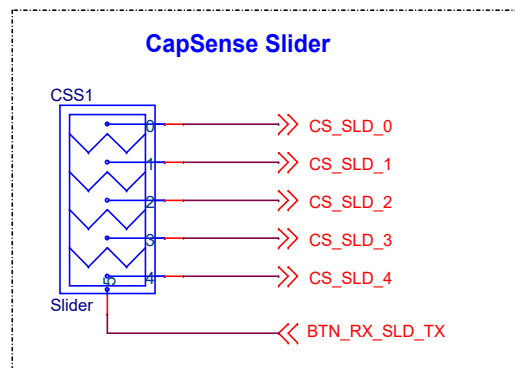
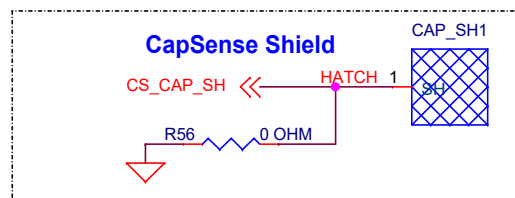
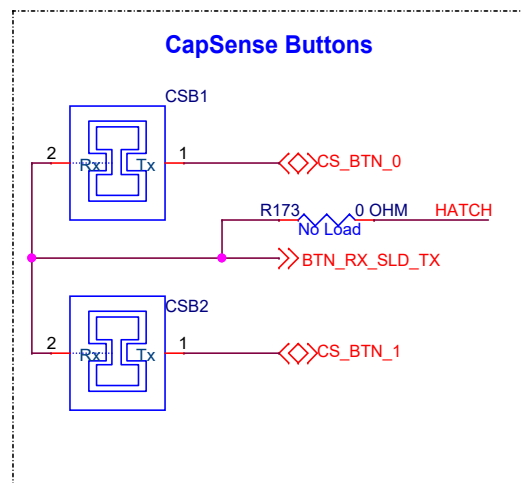
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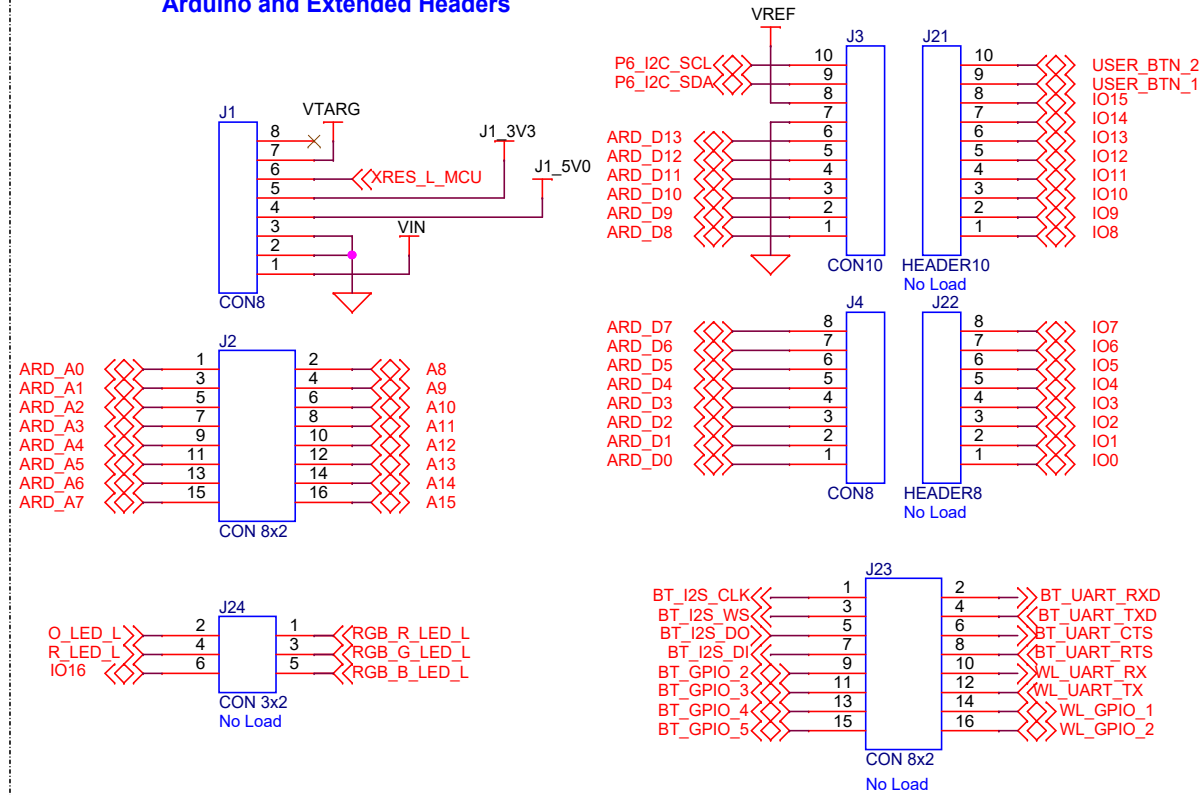
Page Title : Carrier Module Signals

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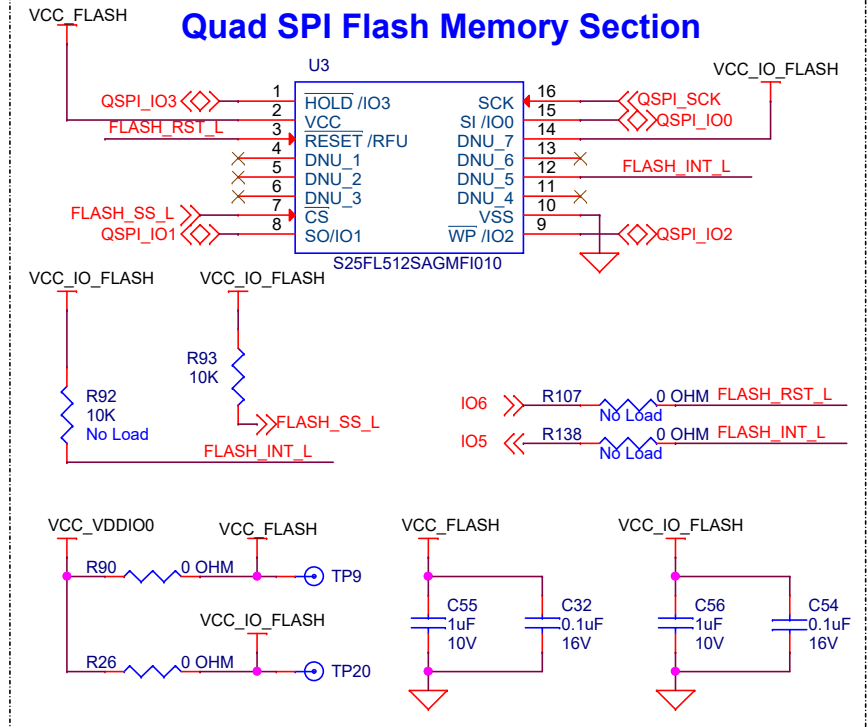


Note: P6_VBUS will be powered using KP_VBUS and hence will be limited in current based on other loads on the kit. Please remove R106 and connect an external power supply that supplies 5V @ 500mA for full USB host functionality.

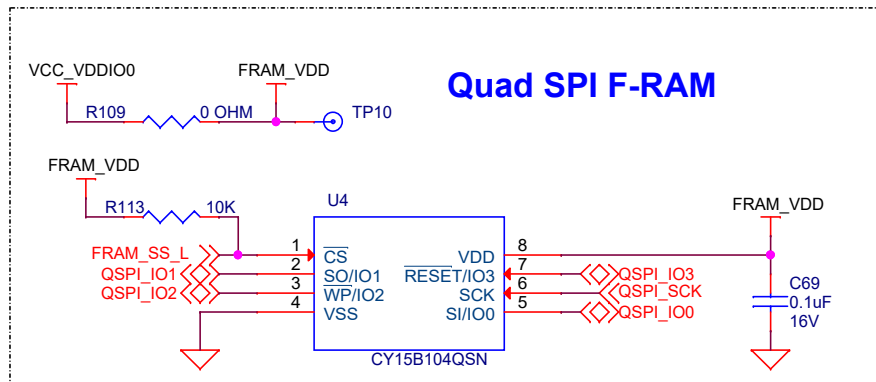
Arduino and Extended Headers



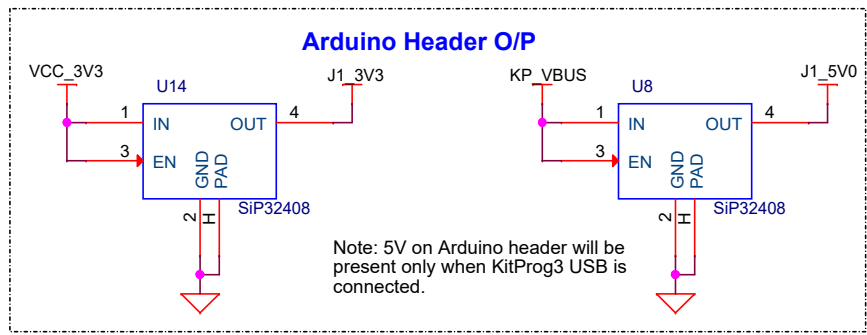
Quad SPI Flash Memory Section



Quad SPI F-RAM



Arduino Header O/P



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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Internal Release	2019/05/13
02	Internal Release	2019/05/21
03	Internal Release	2019/07/23
04	Internal Release	2019/08/08
05	Initial Release	2019/09/18
06	Internal Release	2019/12/09
07	1. Added optional jumper header J26 at VCC_3V3 output voltage selection between 3.3V and 2.5V 2. VCC of USB Device VBUS Detect is changed from VTARG to P6_VDD_BUF	2020/01/28
08	Loaded R133, R134 instead of R13, R14	2020/08/06



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