CYW43439 PCB Layout Guidelines

About this document

Scope and purpose

This document provides PCB layout guidelines for a board design based on the Cypress CYW43439 WLBGA device. The Cypress reference schematic and layout files (see References *[3]* on page **25**) form the basis of the guidelines provided.

Intended audience

This guide is intended for board designers.

Table of contents

1 CYW43439 Chip Information

This section contains a subset of the CYW43439 chip information. For more information, see the CYW43439 datasheet (References *[1]* on page **25**).

1.1 Introduction

The document contains a list of recommended components for the Power Management Unit (PMU) circuitry.

The document is divided into the following four sections:

- **CYW43439 Chip Information** on page **3** contains the chip information. For detailed chip information, see the CYW43439 datasheet (References *[1]* on page **25**).
- **CYW43439 WLBGA Reference Board** on page **8** contains Cypress reference board layout excerpts.
- **Component Selection** on page **14** contains the component selection information for various capacitors and inductors.
- **Routing Guidelines** on page **16** provides the core PCB layout guidelines.

1.2 Purpose and Audience

This reference guide contains examples, guidelines, and requirements to help board designers do the following:

- Facilitate optimal board routing and chip performance.
- Address noise coupling/electromagnetic interference (EMI) current-flow capability and PMU performance.
- Understand the comparative differences of various components (footprint and rating tradeoff) and the impact on overall PMU functionality and performance.

1.3 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms used in Cypress documents, go to **www.cypress.com/glossary**.

1.4 IoT Resources

Cypress provides a wealth of data at **www.cypress.com/internet-things-iot** to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (**community.cypress.com**).

1.5 Device Description

CYW43439 integrates the following on a single die:

- 2.4-GHz WLAN IEEE802.11 b/g/n MAC/baseband/radio
- Bluetooth 4.2 support

The platform-agnostic design and integration of the MAC, PHY, and RF allow CYW43439 to be added to any mobile device regardless of the application processor used. CYW43439 is based on the 40-nm CMOS process technology, making it smaller and more power-efficient than chips with process technologies are above 40 nm. For more package and assembly information, see the WLBGA overview and assembly guidelines (References *[2]* on page 25).

CYW43439 comes with Cypress' latest wireless coexistence technology. Handset makers can use this technology on 4G LTE cellular platforms to minimize the possibility of radio interference between Wi-Fi, Bluetooth, and LTE. Cypress' Global Coexistence Interface supports the Bluetooth Special Interest Group's (SIG) LTE coexistence scheme and can be applied to future Cypress LTE platforms as well as 4G cellular platforms from other vendors.

1.6 CYW43439 Ball Map

Figure 1 shows the ball map of the CYW43439 WLBGA package.

	A	B	C	D	E	F	G	H	J	K	L	M	
1	BT_UART_RXD	BT_DEV_WAKE	BT_HOST_WAKE		FM_RF_IN	BT_VCO_VDD	BT_IF_VDD	BT_PAVDD	WLRF_2G_eLG	WLRF_2G_RF		WLRF_PA_VDD	1
2	BT_UART_TXD	BT_UART_CTS_N	FM_OUT1	FM_OUT2	FM_RF_VDD	BTFM_PLL_VDD	BTFM_PLL_VSS	BT_IF_VSS	WLRF_LNA_GND	WLRF_GENERAL_GND	WLRF_PA_GND	WLRF_VDD_1P35	2
3			BT_UART_RTS_N	VDDC	FM_RF_VSS			BT_VCO_VSS	WLRF_GPIO		WLRF_VCO_GND	WLRF_XTAL_VDD1P2	3
4		BT_PCM_OUT	BT_PCM_IN	VSSC			VDDC	WLRF_AFE_GND			WLRF_XTAL_GND	WLRF_XTAL_XOP	4
5	BT_PCM_CLK	BT_PCM_SYNC				LPO_IN			VSSC		GPIO_2	WLRF_XTAL_XON	5
6	SR_VLX	PMU_AVSS	VOUT_CLDO	VOUT_LNLDO	BT_REG_ON	WCC_VDDIO	WL_REG_ON	GPIO_1	GPIO_0	SDIO_DATA_0	SDIO_CMD	CLK_REQ	6
7	SR_PVSS	SR_VDDBAT5V	LDO_VDD1P5		VOUT_3P3	LDO_VDDBAT5V		SDIO_DATA_1	SDIO_DATA_3		SDIO_DATA_2	SDIO_CLK	7
	A	B	C	D	E	F	G	H	J	K	L	M	

Figure 1 CYW43439 WLBGA Ball Map

1.7 CYW43439 WLBGA Package Keep-Out Areas

Figure 2 shows the keep-out areas on the CYW43439 device. Do not route traces below the highlighted keep-out areas.

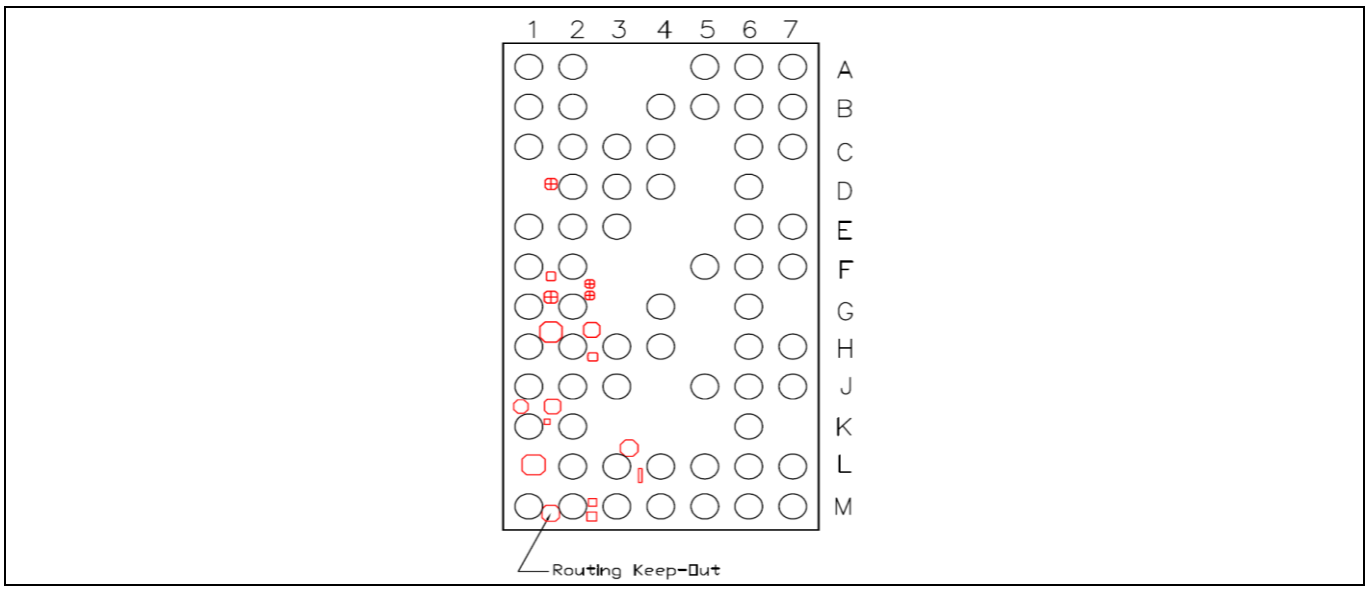

Figure 2 CYW43439 WLBGA Package Keep-out Areas

1.8 Power Topology

Figure 3 and Figure 4 show a typical power topology for CYW43439. The shaded area is external to CYW43439.

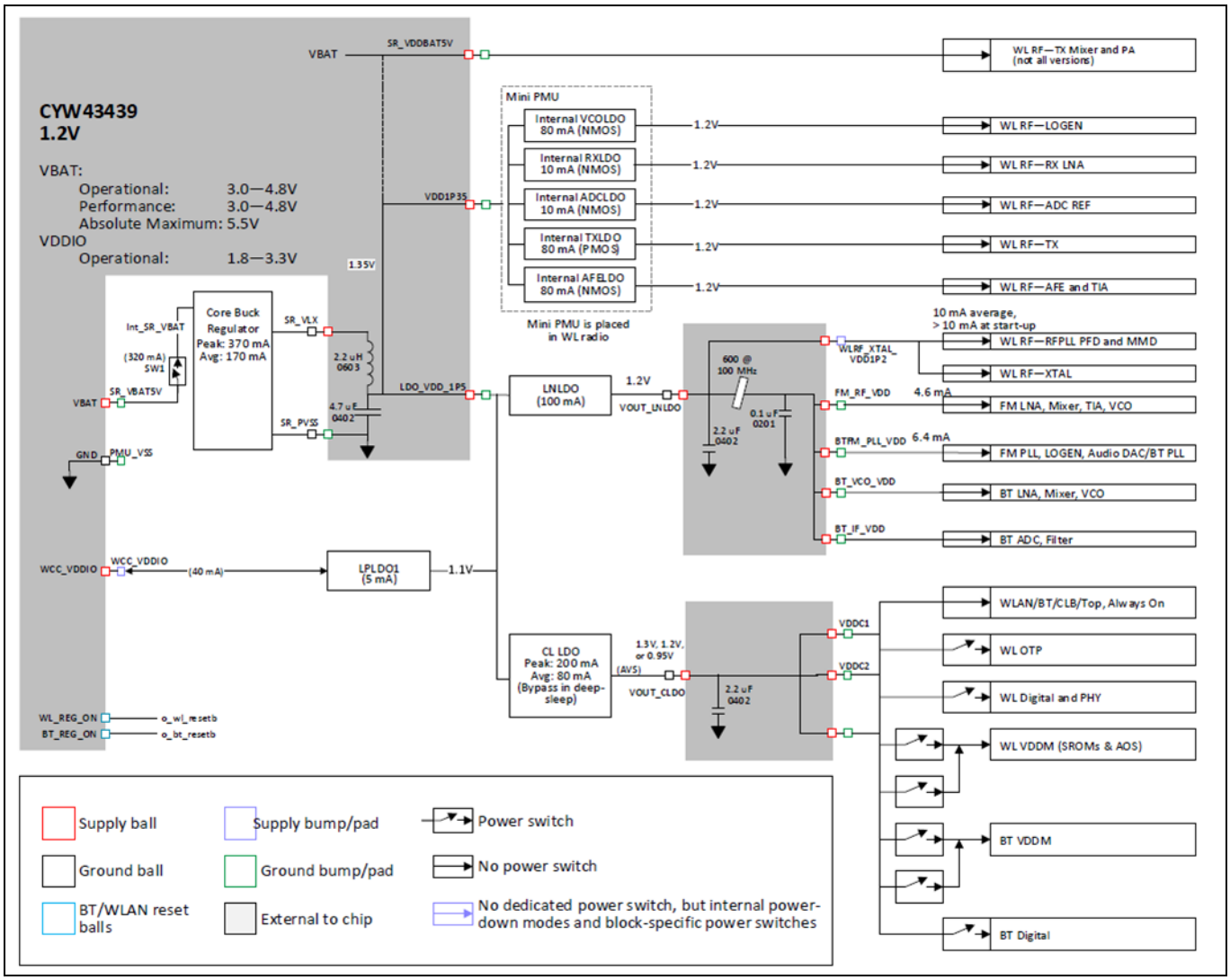

Figure 3 Typical Power Topology (1 of 27)

CYW43439 Chip Information

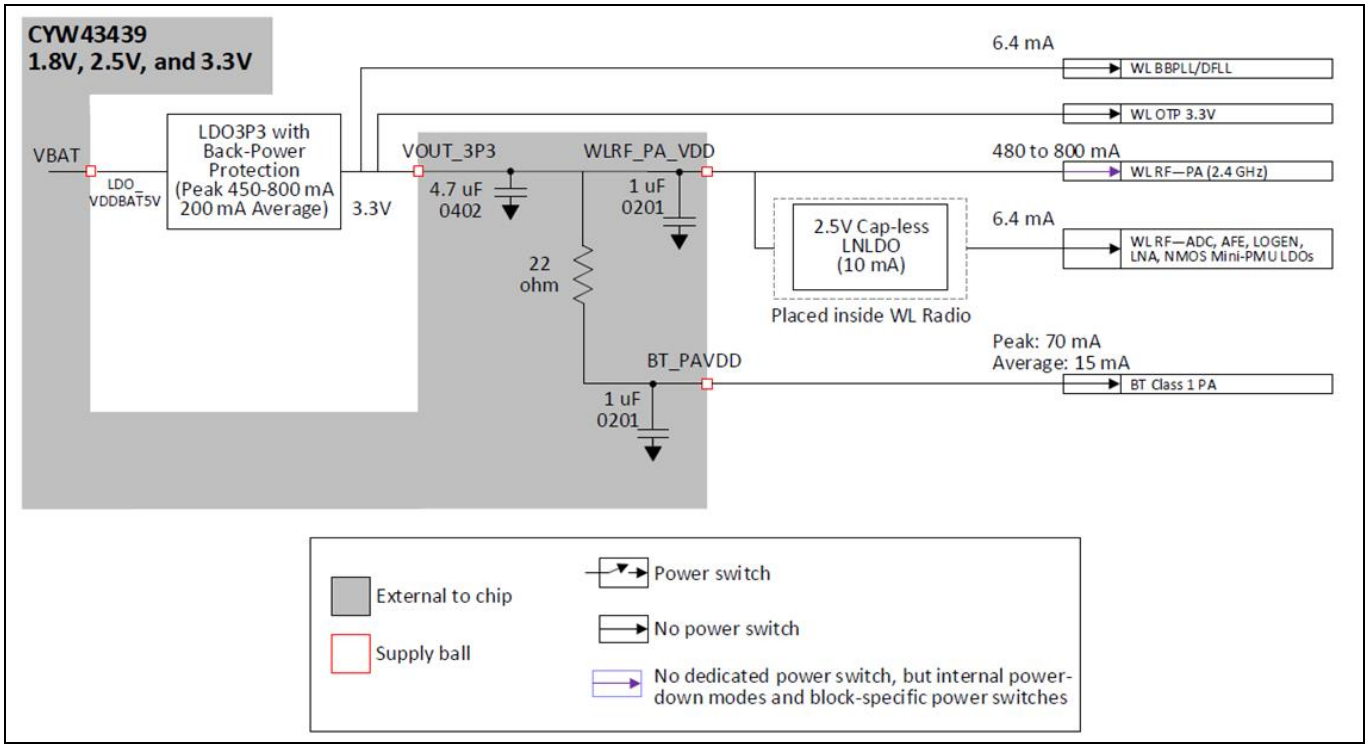

Figure 4 Typical Power Topology (2 of 2)

2 CYW43439 WLBGA Reference Board

2.1 Reference Board Block Diagram

Figure 5 shows the CYW43439 reference board block diagram (CYW943439WLPTH).

Note: The schematic and the Allegro layout file (.brd) are available through the Cypress Customer Support Portal (see References **[3]** on page **25**). Throughout this document, excerpts from the layout file are provided to show various areas of importance.*

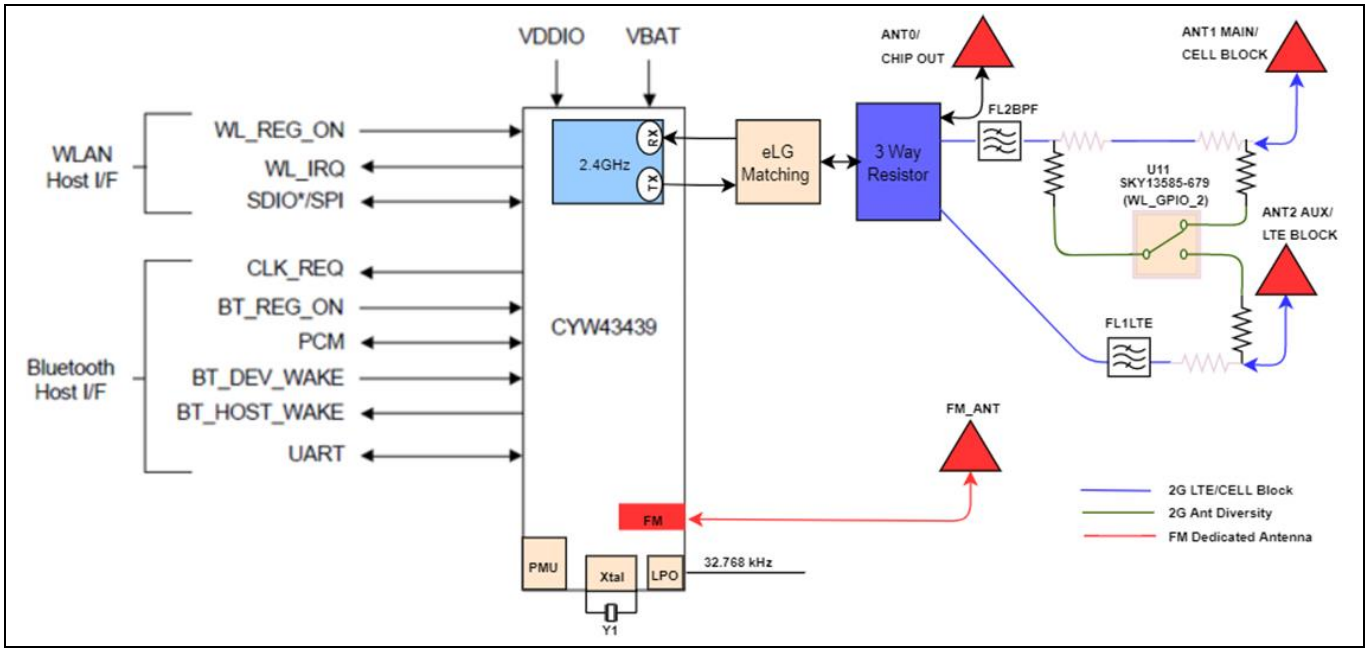

Figure 5 CYW43439 Reference Board Block Diagram

2.2 Major Components in the Reference Design

Table 1 shows some of the major reference design components that are mentioned throughout the document.

The power topology diagram in Figure 3 shows where each component is placed. See the reference board schematic for additional component information.

Table 1 Major Reference Design Components

Reference Design Component Designation	Description	Value
C52	VBAT capacitor	4.7 µF
L11	CBUCK inductor	2.2 µH
C9	CBUCK capacitor	4.7 µF
C27	VOUT3P3 capacitor	4.7 µF
C96	VOUT_LNLDO (Low-noise LDO) capacitor	2.2 µF
C74	VOUT_CLDO (Core LDO) capacitor	2.2 µF
C45	WLRF_PA_VDD capacitor	1 µF
C4	BT_PAVDD capacitor	1 µF
R1	BT_PAVDD resistor	22 Ω
C1	WLRF_VDD_1P35 capacitor	1 µF
C23	XTAL_VDD_1P2 capacitor	0.1 µF
C3	BTFM_PLL_VDD/BT_IF_VDD/ BT_VCO_VDD capacitor	1 µF
C24	FM_RF_VDD capacitor	0.1 µF
C76	VDDC (VOUT_CORE) capacitor	0.1 µF

2.3 Reference Board Layers

This section shows all four layers of the Cypress reference board. Layer 1 shows how components are placed around the CYW43439 device. The crystal area, PMU section, and some ground isolation areas are identified.

2.3.1 PCB Layer Description

Table 2 lists the four layers of the reference platform's PCB. The remainder of this section provides images of each PCB layer.

Table 2 CYW43439 WLBGA Board Layer Description

Layer	Description
1	See **Layer 1 (Component Placement)** on page **10**. Includes RF signals, PMU sections, SDIO and BT UART/PCM traces.
2	Ground Plane. See **Layer 2 (Ground Plane)** on page **11**.
3	Ground plane See **Layer 3 (Ground Plane)** on page **12**.
4	Power plane. See **Layer 4 (Power Plane)** on page **13**.

2.3.2 Layer 1 (Component Placement)

Figure 6 shows Layer 1, the component layer, of the reference board.

Regulators are sensitive to routing parasitics that can cause instability, power efficiency losses, and in extreme cases, loss of voltage regulation. Extreme parasitics due to long and thin traces can create large switching voltage spikes that can lead to long-term chip reliability problems.

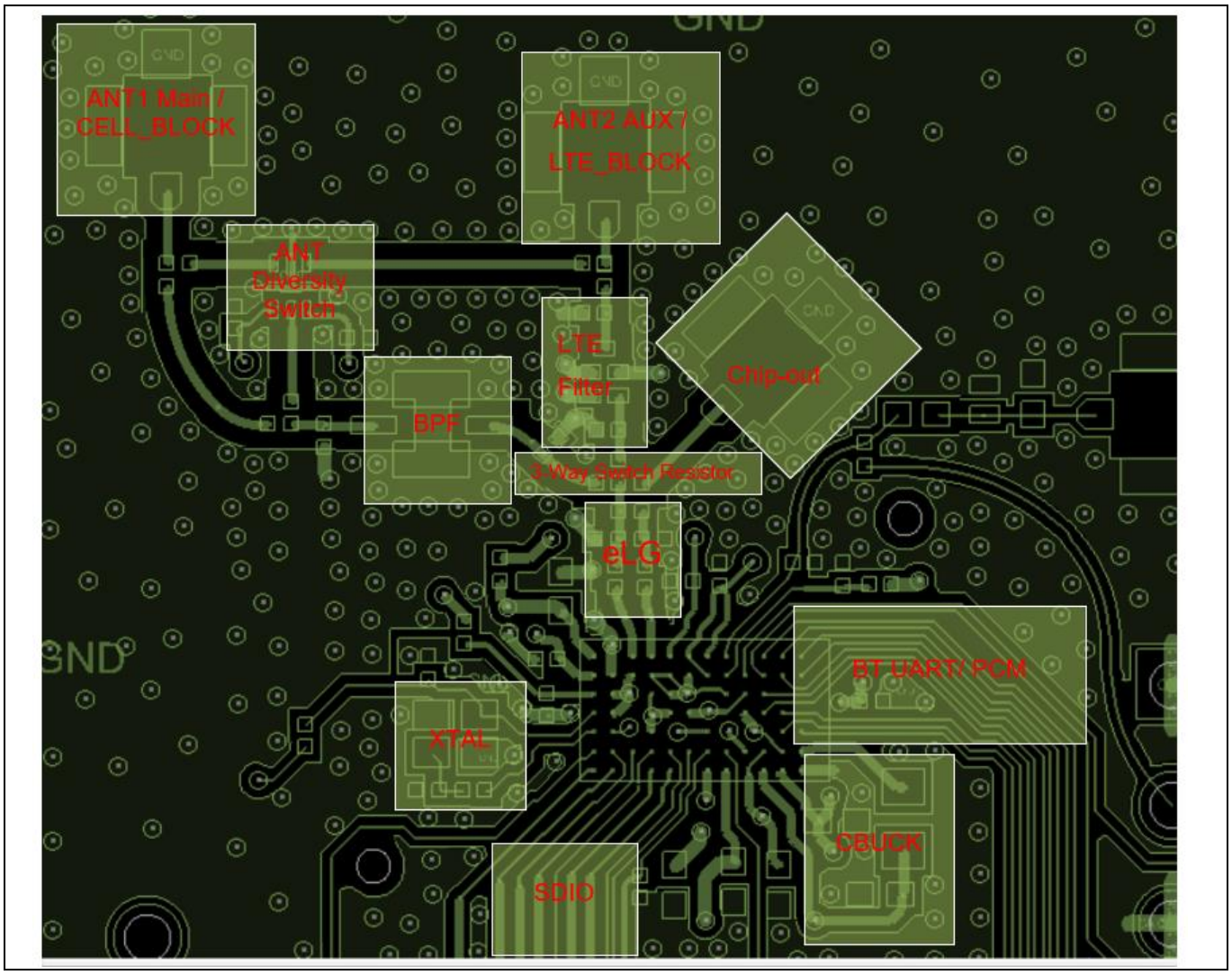

Figure 6 CYW43439 Reference Board Layer 1

2.3.3 Layer 2 (Ground Plane)

Figure 7 shows Layer 2, which is predominantly a ground plane. The ground cuts under the XTAL is also shown. If the FM section is not in use, the FM ground cut can be ignored.

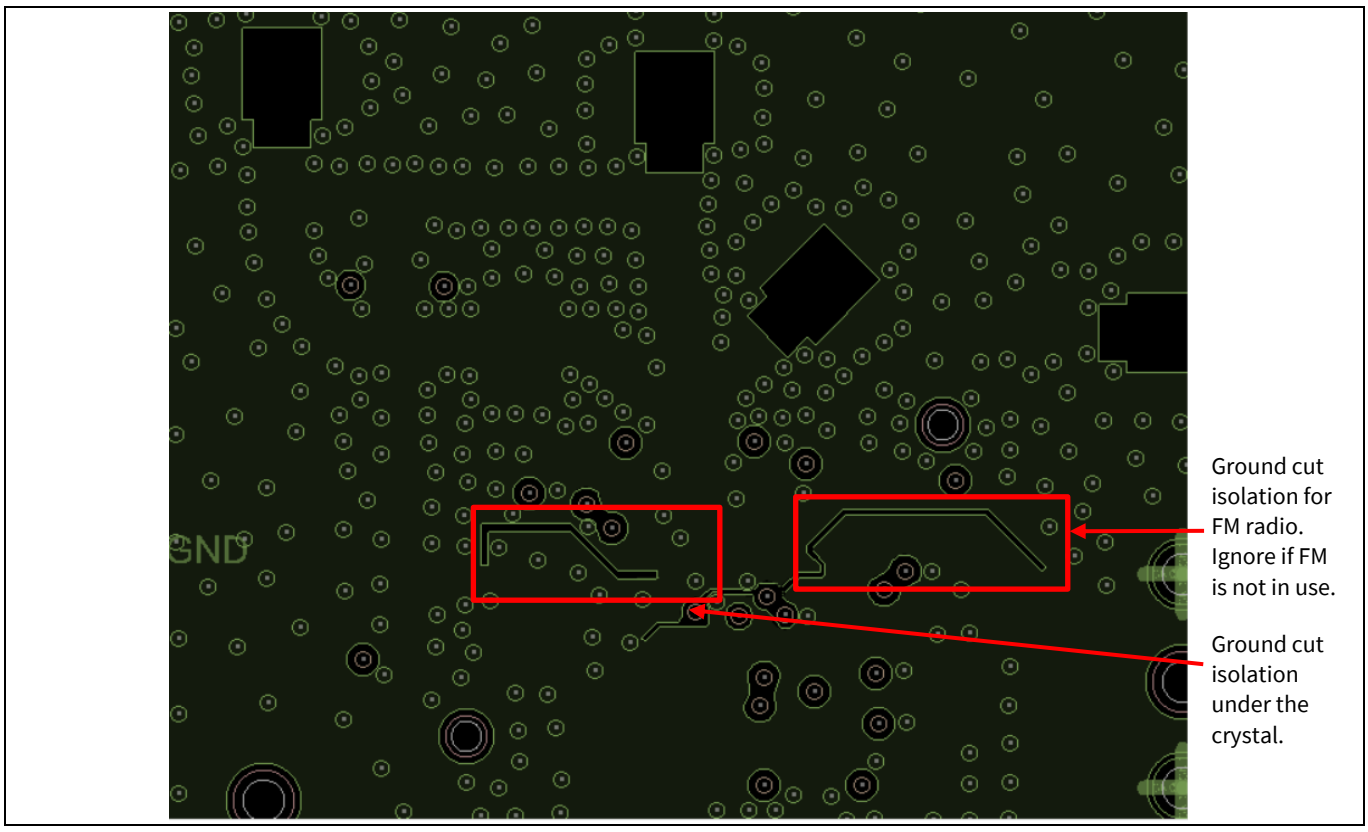

Figure 7 CYW43439 Reference Board Layer 2 (Ground Plane)

2.3.4 Layer 3 (Ground Plane)

Figure 8 shows Layer 3, which is also predominantly a ground plane. If the FM section is not in use, the FM ground cut can be ignored.

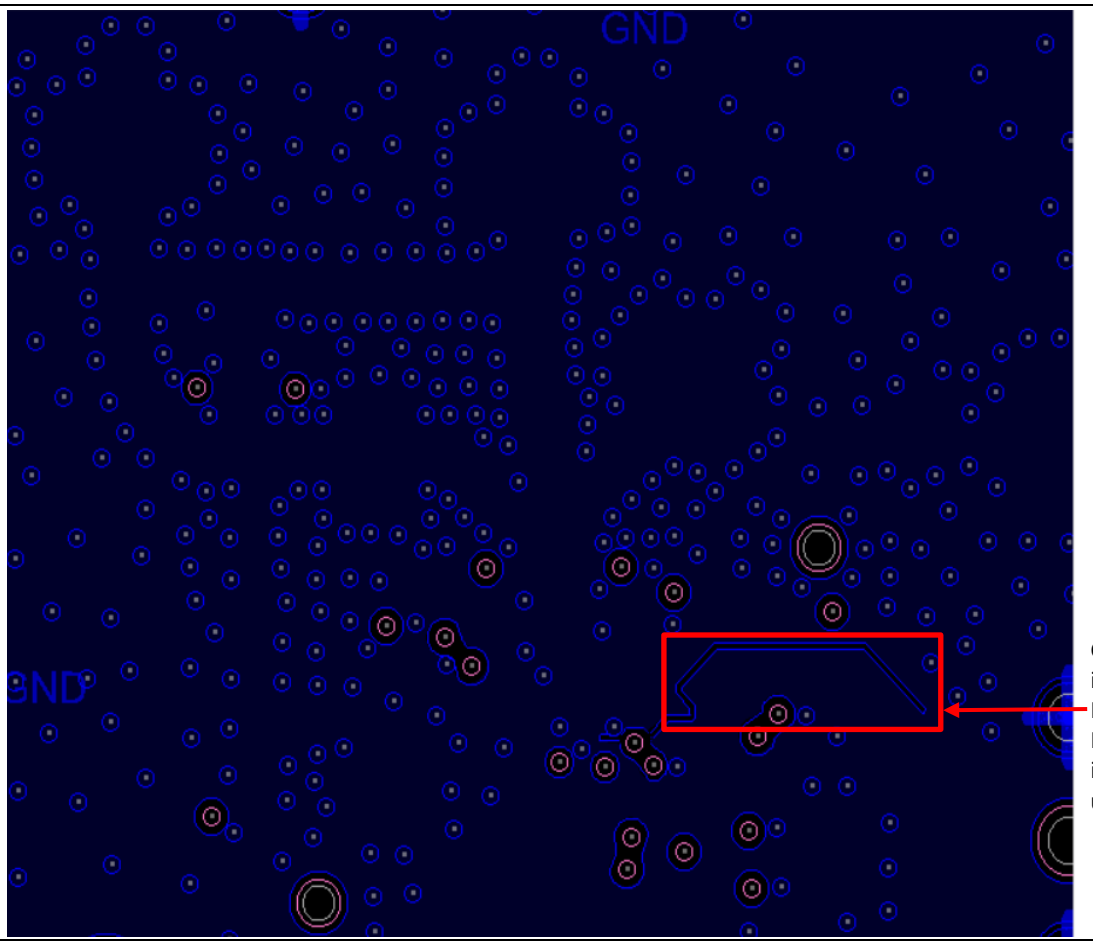

Figure 8 CYW43439 Reference Board Layer 3 (Ground Plane)

2.3.5 Layer 4 (Power Plane)

Figure 9 shows the Layer 4, which includes power supply traces.

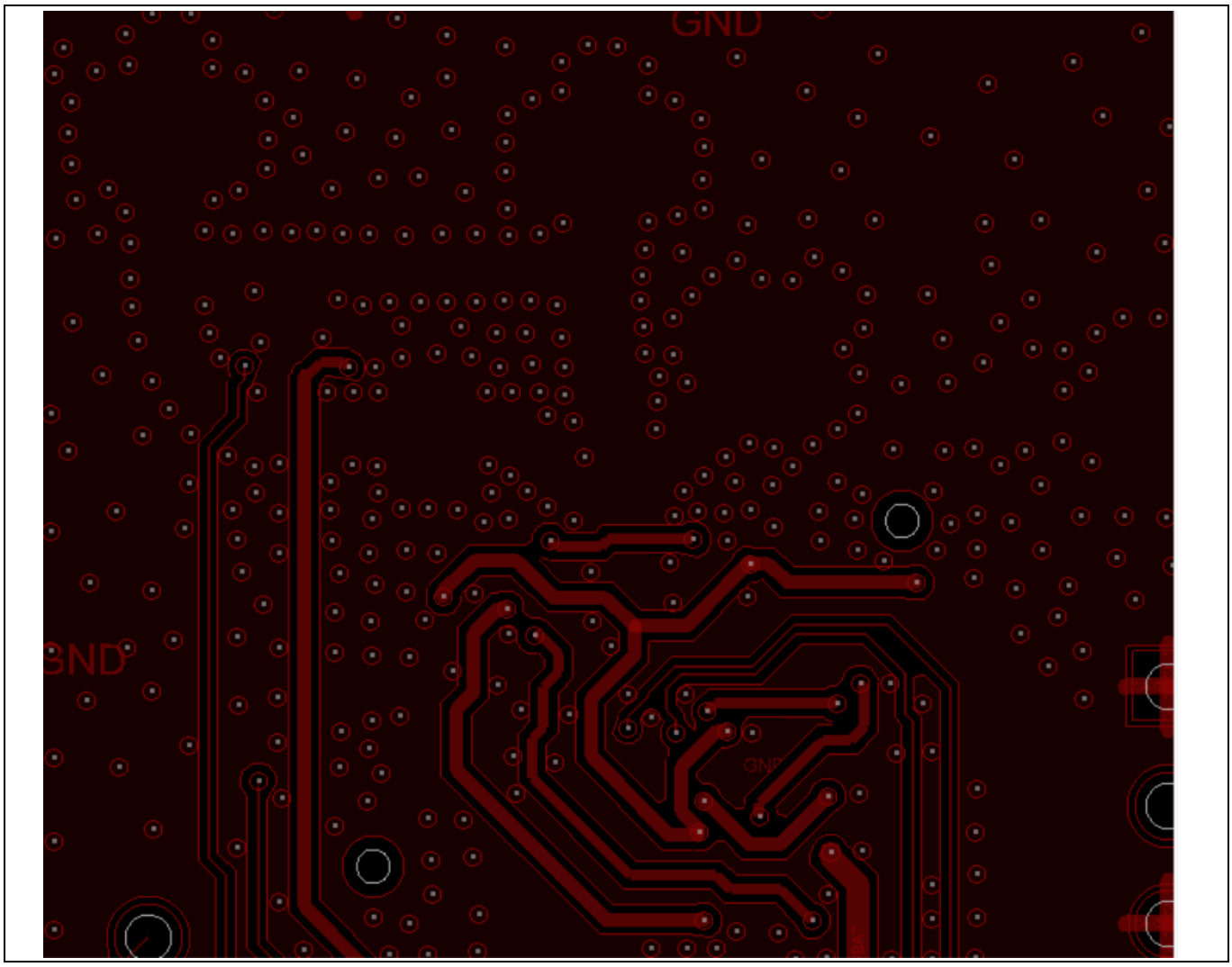

Figure 9 CYW43439 Reference Board Layer 4 (Power Plane)

3 Component Selection

This section provides component selection guidance for optimizing the performance of the following power rails:

- VBAT capacitance
- CBUCK
- VOUT_3P3 output capacitance
- CLDO/LNLDO output capacitance

3.1 VBAT Capacitance

The nominal SR_VDDBAT5V and LDO_VDDBAT5V shared capacitance value is 4.7 µF (0402 package, 10 V, 20%, X5R, ceramic surface-mount). The following criteria apply:

- Effective capacitance should NOT drop below 1.645 µF at 4.8 V.
- Effective capacitance should NOT drop below 1.88 µF at 4.2 V.
- Effective capacitance should NOT drop below 2.2 µF at 3.6 V.
- Recommended part for VBAT capacitor is Murata GRM155R61A475MEAA or any cap matching or better than the DC bias profile.

Table 3 Capacitor Recommendations

Part Number	Description	Manufacturer
GRM155R61A475MEAA	0402 X5R 4.7 µF 20% 10 V	Murata
GRM188R60J475ME84D	0603 X5R 4.7 µF 20% 6.3 V	Murata
GRM188R60J475ME19D	0603 X5R 4.7 µF 20% 6.3 V	Murata
GRM155R60J475ME87D	0402 X5R 4.7 µF 20% 6.3 V	Murata

3.2 CBUCK

3.2.1 CBUCK Output Capacitance

The nominal CBUCK output capacitance value is 4.7 µF (0402 package, 6.3 V, 20%, X5R, ceramic surface-mount). The following criteria apply:

- The effective capacitance should NOT drop below 3.622 µF at 1.35 V
- Recommended part for CBUCK capacitor is Murata GRM155R60J475ME87D or any cap matching or better than the DC bias profile.

Table 4 CBUCK Capacitor Recommendations

Part Number	Description	Package Size	Manufacturer
GRM155R60J475ME87D	X5R 4.7 µF 20% 6.3 V	0402	Murata
GRM188R60J475ME19D	X5R 4.7 µF 20% 6.3 V	0603	Murata
GRM188R61A475KE15	X5R 4.7 µF 20% 10 V	0603	Murata

3.2.2 CBUCK Inductance

The nominal CBUCK inductor value is 2.2 µH. The choice of inductor depends on operating temp range, DCR, ACR, saturation currents based on (L-30%) and +40 °C self-heating temperature rise criteria and footprint/height.

Table 5 CBUCK Inductor Recommendations

Manufacturer	Part No.	Width (mm)	Length (mm)	Max. Height (mm)	Typ. L (µH)	L Tol. (%)	Typ. DCR (mΩ)	Typ. Idc (A) [a]
Murata	LQM18PN2R2MGHD	0.8	1.6	1	2.2	20	200	1.15

a. Based on temperature rise. When applied Rated Current, temperature rise caused by self-generated heat shall be limited to 40 °C max.

The recommended part is Murata LQM18PN2R2MGHD. This is the most critical part in the BOM; Cypress strongly recommends that you use this part for CYW43439 design as the CBUCK inductor.

3.3 VOUT_3P3 Output Capacitance

The nominal VOUT_3P3 output capacitance value is 4.7 µF (0402 package, 6.3 V, 20%, X5R, ceramic surface-mount). The following criteria apply:

- Effective capacitance should NOT drop below 1.773 µF at 3.3 V.
- Recommended part for VOUT_3P3 capacitor is Murata GRM155R60J475ME87D or any cap matching or better than the DC bias profile.

Table 6 VOUT_3P3 Output Capacitor Recommendations

Part Number	Description	Package Size	Manufacturer
GRM155R60J475ME87D	X5R 4.7 µF 20% 6.3 V	0402	Murata
GRM188R60J475ME84D	X5R 4.7 µF 10% 6.3 V	0603	Murata

3.4 CLDO/LNLDO Output Capacitance

The nominal CLDO/LNLDO output capacitance value is 2.2 µF (0402 package, 6.3 V, 20%, X5R, ceramic surface-mount). The following criteria apply:

- Effective capacitance should NOT drop below 1.87 µF at 1.2 V
- Recommended part for CLDO/LNLDO output capacitor is Murata GRM155R60J225ME15D or any capacitor matching or better than the DC bias profile.

Table 7 CLDO/LNLDO Output Capacitor Recommendations

Part Number	Description	Package Size	Manufacturer
GRM155R60J225ME15D	X5R 2.2 µF 20% 6.3 V	0402	Murata
C1005X5R225MCTS	X5R 2.2 µF 20% 6.3 V	0402	DARFON

4 Routing Guidelines

4.1 General PCB Design Guidelines

Follow these general PCB design guidelines:

- Keep noisy lines away from RF traces, and place ground vias along RF traces.
- Do not use ground cuts under RF traces.
- Properly ground RF switches using vias.
- Do not place noisy supply lines (VBAT, VOUT_3P3, and VIO) or digital lines (UART and PCM) over sensitive power supply traces like VOUT_LN, VIN_LDO, and VOUT_CORE.
- Directly connect each pin to the reference ground.
- Minimize the coupling of noisy signals to crystal traces.
- Avoid placing crystal-trace vias close to noisy signals on other layers.
- Use a solid ground layer under the crystal.
- Use a solid ground layer under the CBUCK regulator.
- Use power supply traces wide enough to support required currents. For example, a 10-mil, half-ounce copper trace can handle 500 mA (at 10 °C). The width must be increased to 25 mils for 900 mA. Current-carrying capacity goes up to 700 mA for 10 mils and 1.5 A for 25 mils at 30 °C for the same half-ounce copper weight.
- Microvias handle less current than through-vias. Therefore, multiple microvias may be required in some cases. This 4-layer reference design (CYW943439WLPTH) uses through-hole vias, which can support large current.
- In several figures throughout this section, a star symbol is used to indicate a star connection. A star connection is formed at a decoupling capacitor that attaches to more than one circuit element.

Use the **Table 8** as a general guideline for typical trace width in mils.

Table 8 Trace Width Instructions

Net name	Width (mils)	Net Name	Width (mils)
VBAT	12-15	RF signals	5 – 8
VDDIO	3-6	XTAL/LPO signals	3 – 4
		XTAL_VDD1P2	7 – 8
SR_VLX	10-12		
VIN_LDO	10-12	SDIO signals	4 – 5
VOUT_3P3	8-10	GPIO/JTAG signals	3 – 4
VOUT_LN	8-10	BT PCM/UART/I2S	3 – 4
BT_PAVDD	8-10	WL/BT_HOST/DEV_WAKE	3 – 4
VOUT_CORE	8-10	WL/BT_REG_ON	3 – 4

Figure 10 and **Figure 11** show the overall layout block diagram for the CYW43439 device, component placement, and trace routing instructions.

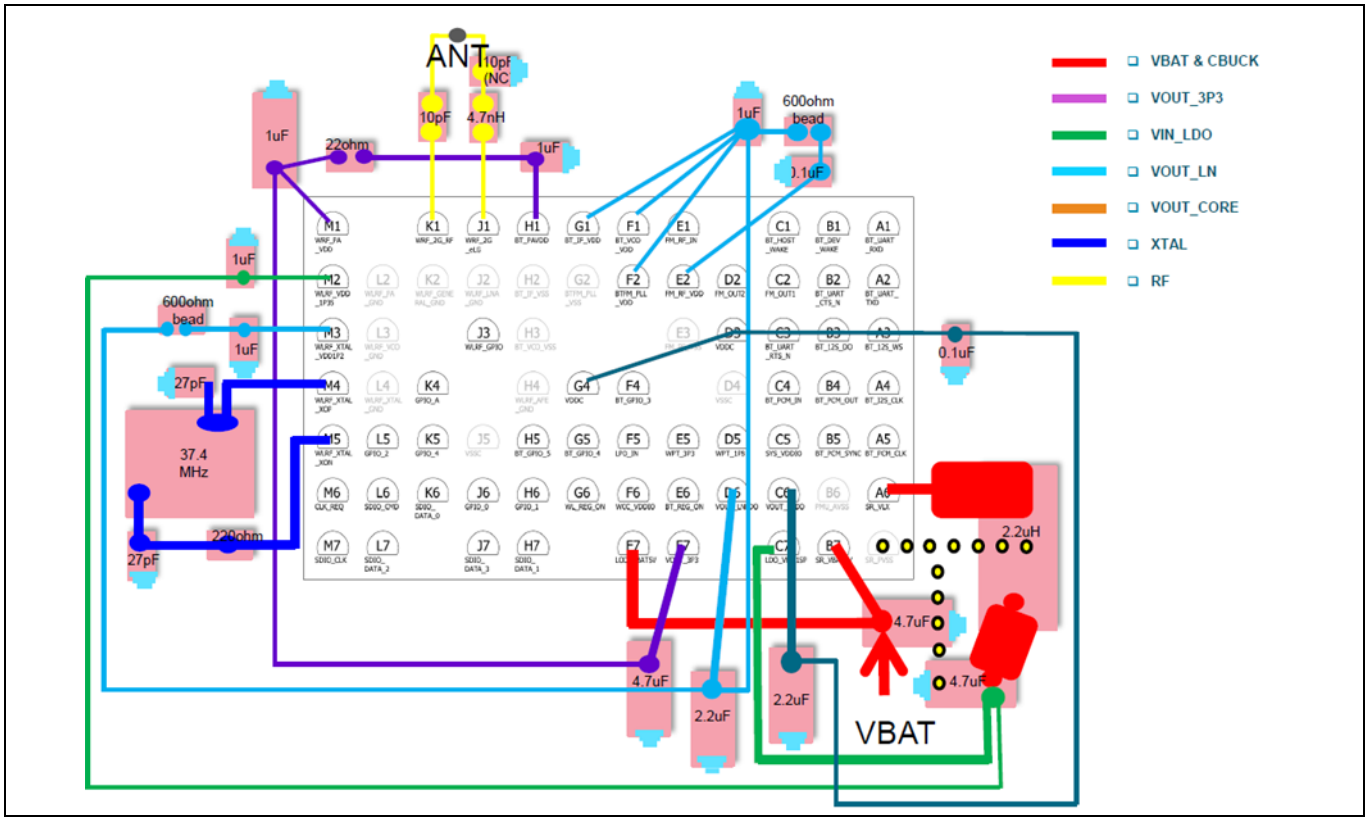

Figure 10 Overall Layout Block Diagram with CYW43439

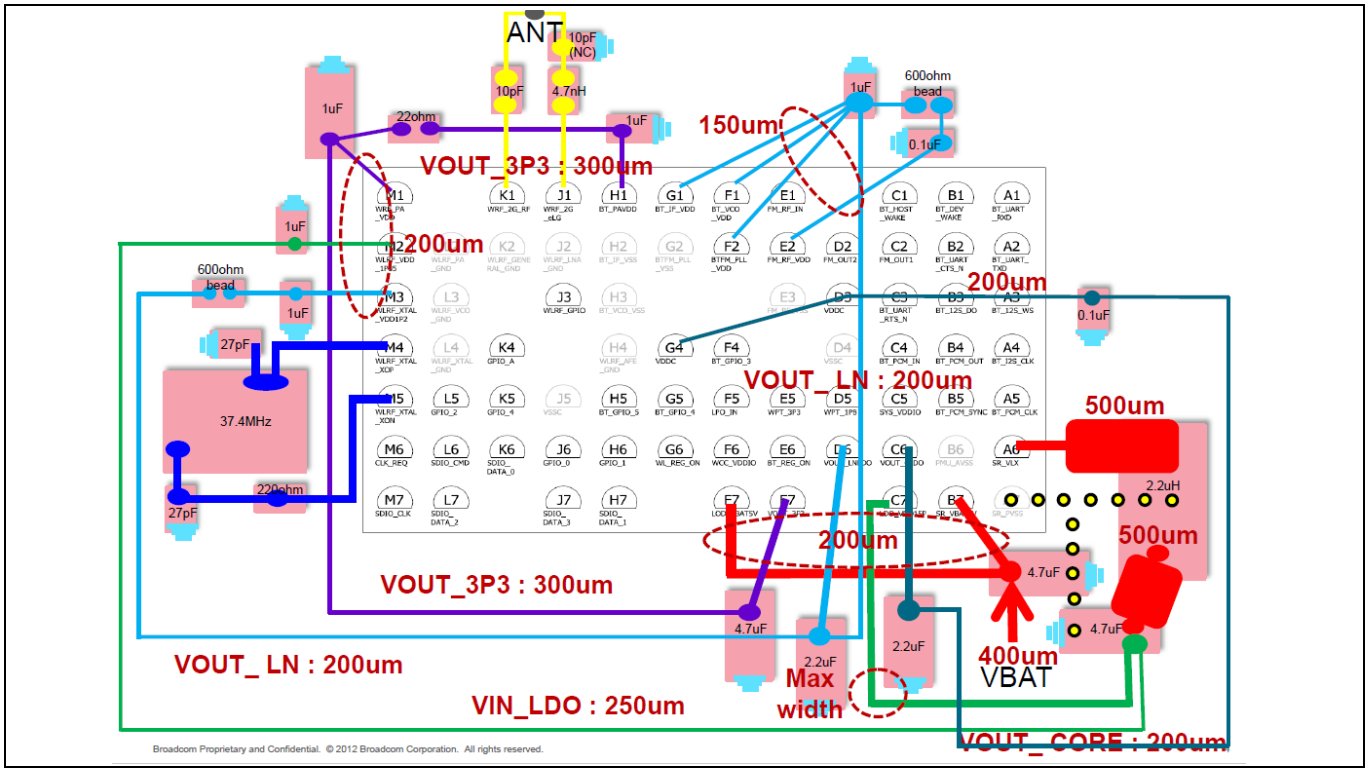

Figure 11 Overall Layout Block Diagram with CYW43439 with Trace Width

4.2 Routing and Placement for VBAT and CBUCK Networks

Connect SR_PVSS, VBAT Cap, and CBUCK Cap together as shown in one complete GND pad. Keep the AC return current loop small and provide a local island among the three GND pads. Do a star connection between pins B7/F7 to the VBAT Cap.

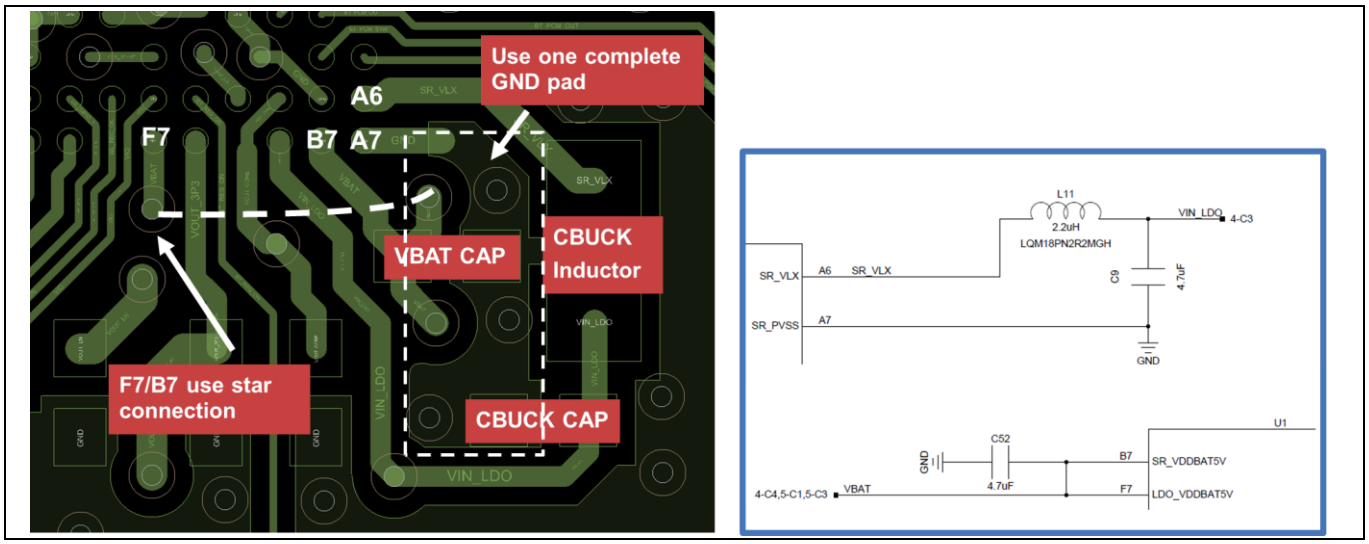

Figure 12 VBAT and CBUCK Power Networks

4.3 LDO's Output Capacitor Placements

Place all LDO output caps close to the CYW43439 device to reduce the current return path.

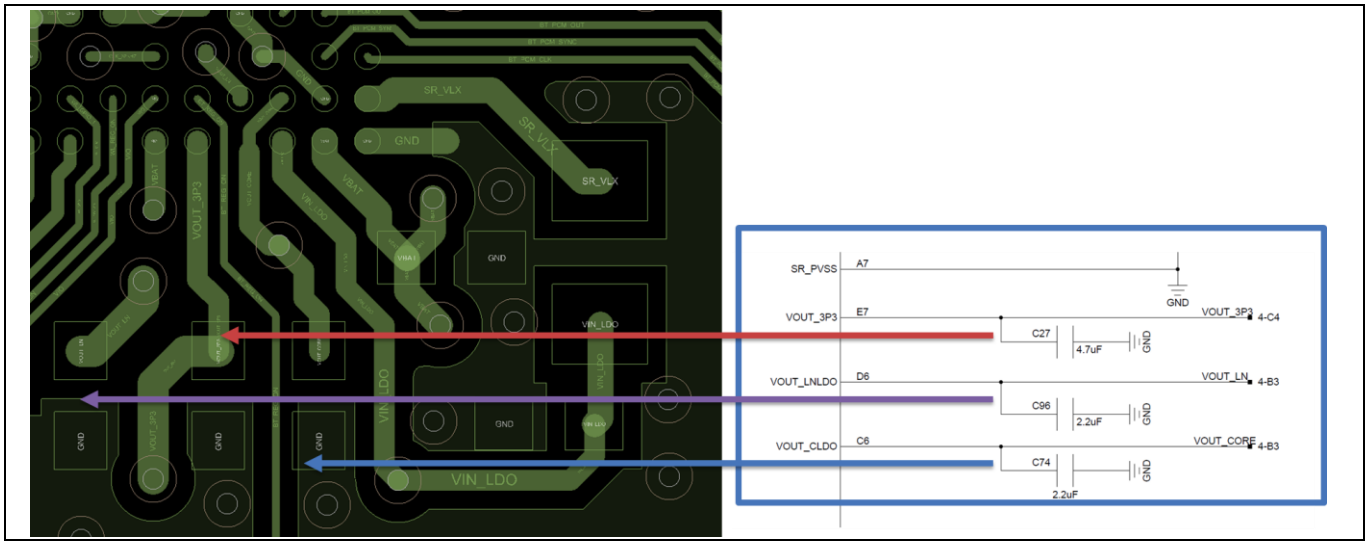

Figure 13 LDO Output Capacitors

4.4 Routing the LDO: VOUT3P3

Implement the star topology for M1 and H1. Use thick traces and through-hole vias to support large current.

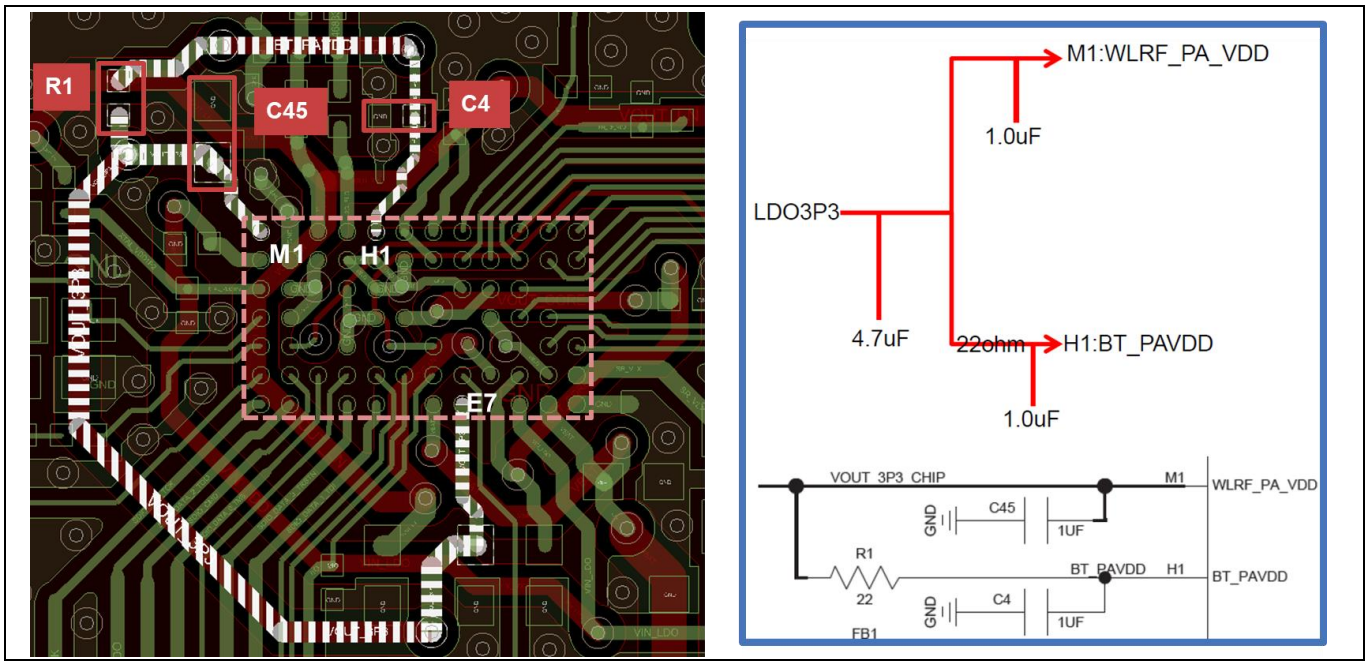

Figure 14 VOUT_3P3 Network

4.5 Routing the VIN_LDO Network

Implement the star topology for M2 and C7.

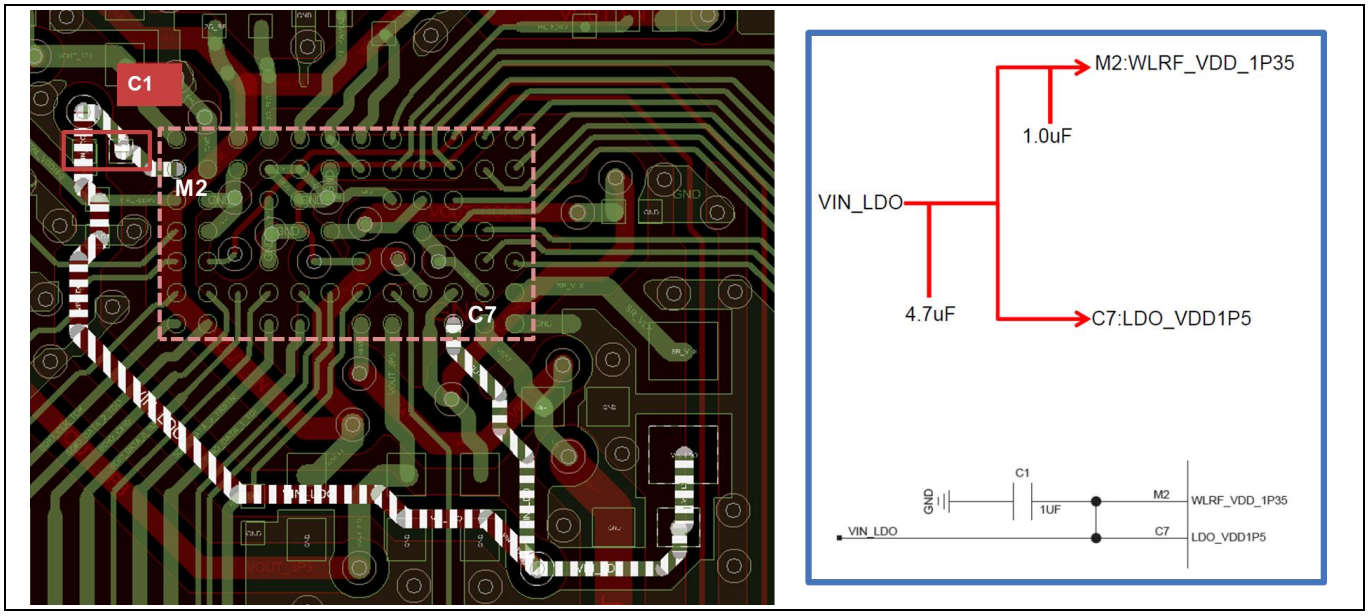

Figure 15 VIN_LDO Network

4.6 Routing the VOUT_LN (LNLDO) Network

Implement the star topology. If the FM section is not used, E2 can be directly connected to the VOUT_LN network (FB3 and C24 can be ignored).

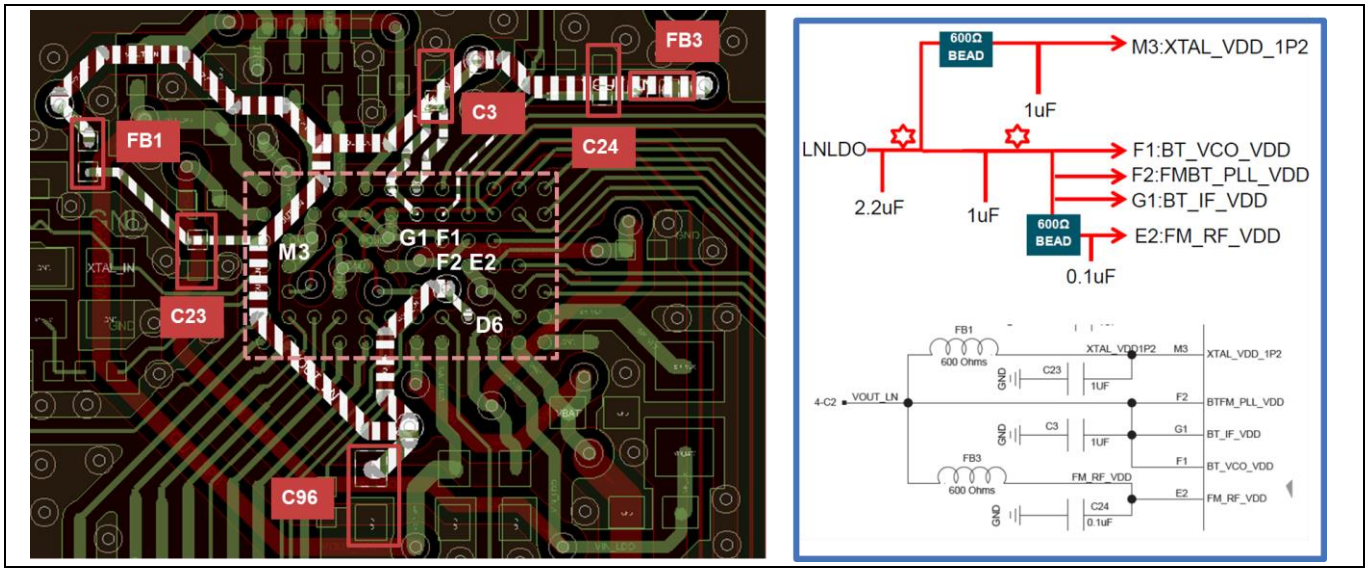

Figure 16 VOUT_LN Network

4.7 Routing CLDO Network

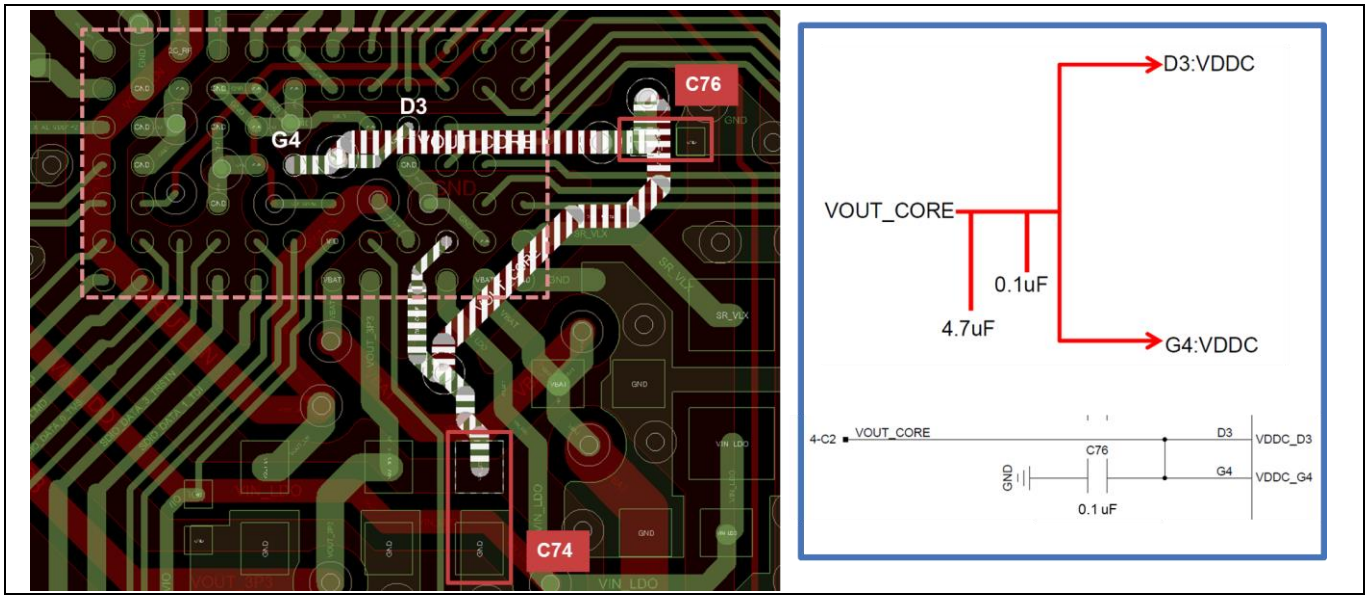

Figure 17 CLDO Network

4.8 Routing XTAL Network

Do not switch layers for XTAL_IN and XTAL_OUT networks. Ensure that XTAL_IN and XTAL_OUT do not cross or overlap each other. Use complete GND planes with through-hole vias to ensure good ground condition. Use solid GND plane under the XTAL area.

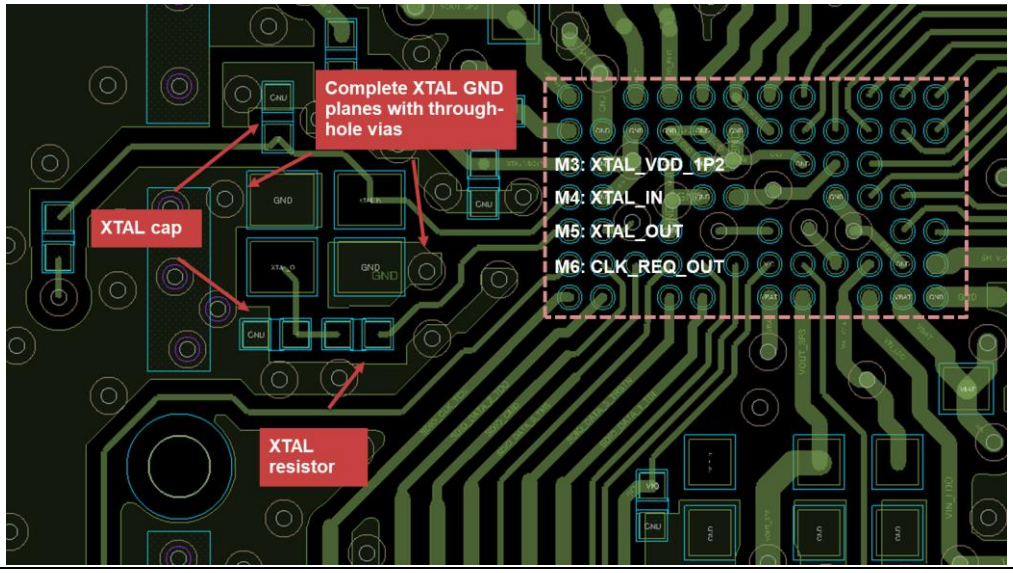

Figure 18 XTAL Network

4.9 Routing Host Interface SDIO 2.0

The following criteria apply:

- SDIO 2.0 trace should be maintained to within 50 ohms of the line impedance.
- Trace should not have any stubs; the DATA trace length should not be greater than CLK trace.
- Length match SDIO lines to equal or within +/- 100 mils.
- Keep SDIO_CLK away from SDIO CMD and DATA lines (use the 2:1 rule of thumb). Insert GND barriers for SDIO_CLK.
- Routing SDIO_CLK closely parallel to command and data lines can cause glitches on the bus, affecting SDIO operation.

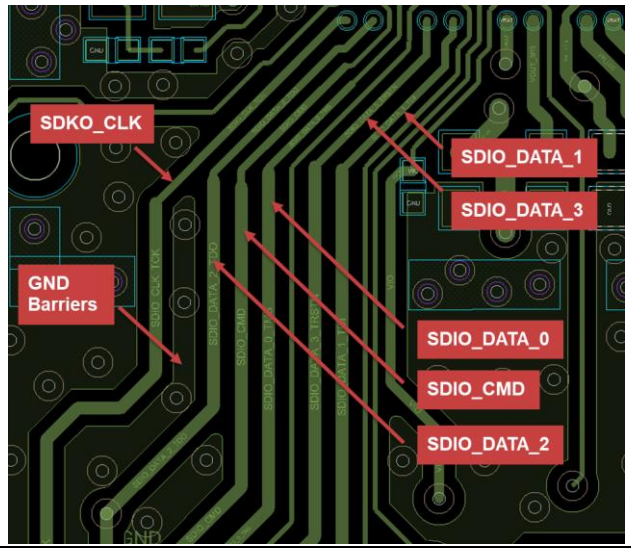

Figure 19 Host Interface SDIO 2.0

4.10 Routing BT Control Signals and BT Digital Signals

Route BT control signals (BT_HOST_WAEK, BT_DEV_WAKE) and BT digital signals traces (UART and PCM) on Layer 1.

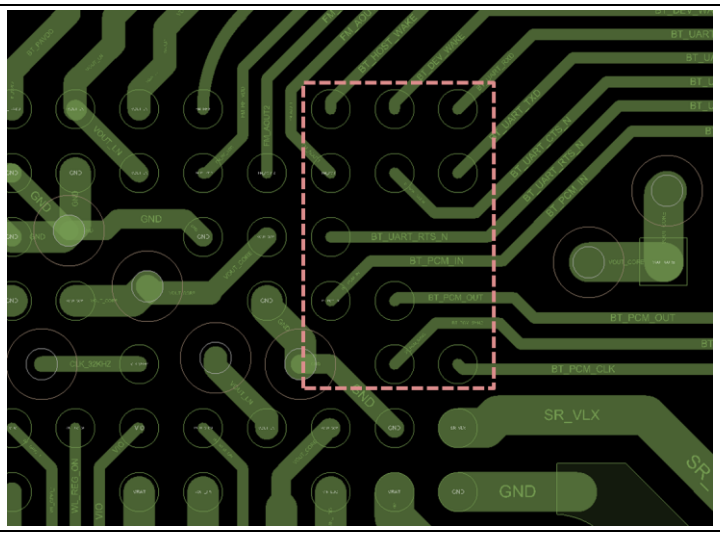

Figure 20 BT Control Signals and BT Digital Signals

4.11 Routing RF Front End Signals

The following criteria apply:

- Space out RF lines to minimize RF coupling and add GND stitches along it. Insert GND stiches to reduce harmonics radiation.
- Avoid changing layers for the RF front-end network.
- If the FM section is not used, FM_RF_IN can be left open.
- Use the 'CHIP_OUT' path to evaluate the chip-out performance. Use the 'LTE BLOCK' to evaluate the performance with the LTE filter. Use the 'CELL_BLOCK' path to evaluate the performance with a band pass filter. Use a 3-way switching resistor for path selection.

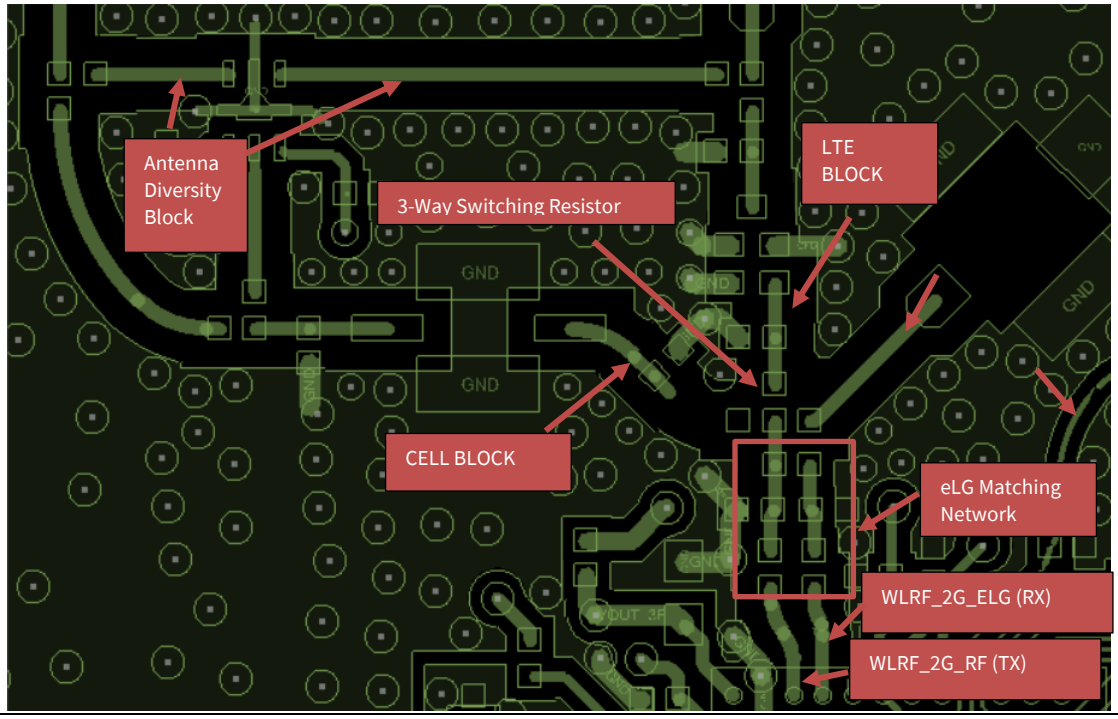

Figure 21 RF Front End

5 References

Use the references in this section in conjunction with this document.

Note: *Cypress provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads and Support site (see **IoT Resources**).*

[1] 002-30348: Single-Chip IEEE 802.11 b/g/n MAC/Baseband/Radio with Integrated Bluetooth 4.2

[2] Wafer-Level Ball Grid Array Overview and Assembly Guidelines

[3] CYW943439WLPTH reference design Rev 1.0[b]

b. Contact your local Cypress FAE or sales representative for access to the design package including latest 43439 datasheet.

Revision history

Date	Version	Description
2020-05-29	**	Initial release.
2020-10-14	*A	Updated to Infineon format.

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