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ADVANCE

CYW43143

Single Chip IEEE 802.11 b/g/n MAC/PHY/Radio with USB/SDIO Host Interface

The CYW43143 is a single-band, single-stream, IEEE 802.11n compliant, MAC/PHY/Radio system-on-a-chip with internal 2.4 GHz Power Amplifier (PA) and integrated T/R switch. The CYW43143 supports internal RX diversity by providing two antenna ports. The device enables development of USB or SDIO 802.11n WLAN clients that can take advantage of the high throughput and extended range of Cypress second-generation solution. The CYW43143 maintains compatibility with legacy IEEE 802.11b/g devices.

State-of-the-art security is provided by industry standard support for WPA, WPA2 (802.11i), and hardware-accelerated AES encryption/decryption, coupled with TKIP, IEEE 802.1X support, and a WLAN Authentication and Privacy Infrastructure (WAPI) hardware engine.

Embedded hardware acceleration enables increased system performance and reduced host-CPU utilization in both client and access point configurations. The CYW43143 also supports Cypress widely accepted and deployed WPS to easily secure WLAN networks.

- SDIO and USB wireless client modules for digital TVs, Blu-ray Disc® players, set-top boxes, game consoles, and printers.
- Supports the I²S digital audio interface.
- Stand-alone wireless USB dongles and multimedia streaming boxes.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

| Broadcom Part Number | Cypress Part Number |
|----------------------|---------------------|
| BCM43143 | CYW43143 |
| BCM43143KMLG | CYW43143KMLG |

Features

Supports 3.3V ±10% power supply input with high efficiency Power Management Unit (PMU).

- Programmable dynamic power management.
- Eight GPIOs with multiplexed JTAG interface.
- Complies with USB 2.0 specification and link power management.
- Supports standard SDIO v2.0 (50 MHz, 4-bit and 1-bit) and USB host interfaces.
- 20 MHz reference clock.

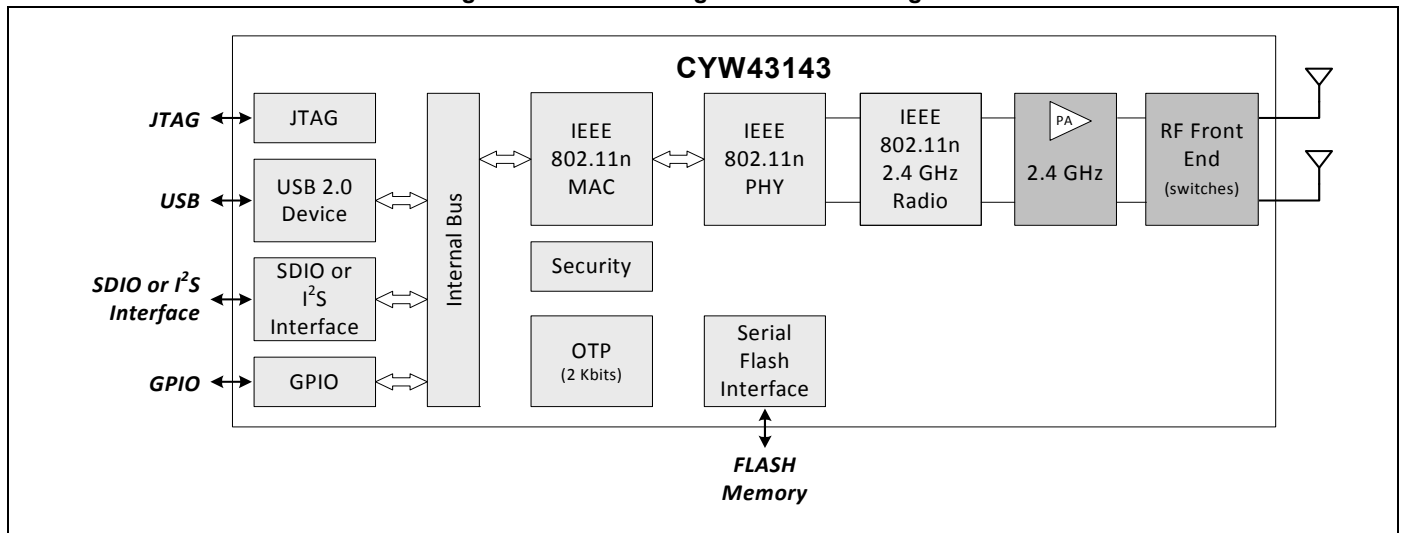
IEEE 802.11x Key Features:

- IEEE 802.11n compliant.
- 2.4 GHz internal PA.
- Internal T/R and RX diversity switches.
- Supports MCS 0–7 coding rates.
- Support for Short Guard Interval (SGI).
- Supports USB 2.0, standard SDIO v2.0 (50 MHz, 4-bit and 1-bit) host interfaces.
- Supports the I²S audio interface.
- Greenfield, mixed mode, and legacy mode support.
- 802.11n MPDU/MSDU aggregation support for high throughput.

- Full IEEE 802.11b/g legacy compatibility with enhanced performance.
- Supports Cypress OneDriver™ software.
- Supports drivers for Windows®, Linux®, and Android™ operating systems.
- Comprehensive wireless network security support that includes WPA, WPA2, and AES encryption/decryption, coupled with TKIP, IEEE 802.1X support, and a WAPI encryption/decryption engine.
- Single stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 150 Mbps for typical upper-layer throughput in excess of 90 Mbps.
- Supports the IEEE 802.11n RX space-time block coding (STBC) and low-density parity check (LDPC) options for improved range and power efficiency.
- Supports an IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other colocated wireless technologies such as GPS, WIMAX, LTE, Bluetooth, and UWB.
- Integrated ARM Cortex-M3 processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption while maintaining the ability to field upgrade with future features. On-chip memory includes 448 KB SRAM and 256 KB ROM.

- USB 2.0 with Link Power Management (LPM) for low power standby application.
 - SDIO out of band low power application.
 - Integrated One Time Programmable (OTP) memory to save configuration settings.
 - Single stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 150 Mbps for typical upper-layer throughput in excess of 90 Mbps.
 - Supports the IEEE 802.11n RX space-time block coding (STBC) and low-density parity check (LDPC) options for improved range and power efficiency.
- Package options:**
- 7 mm × 7 mm, 56-pin QFN package.

Figure 1.CYW43143 High-Level Block Diagram



IoT Resources

Cypress provides a wealth of data at <http://www.cypress.com/internet-things-iot> to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (<http://community.cypress.com/>).

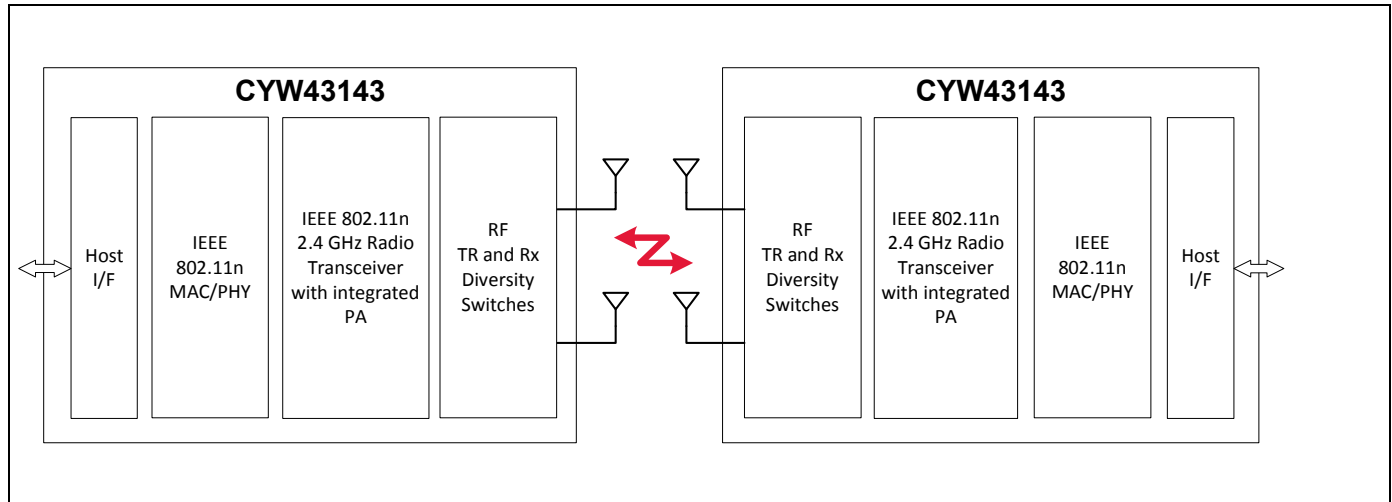
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1. Introduction

The Cypress CYW43143 single-chip device provides the highest level of integration for wireless systems with integrated IEEE 802.11b/g/n (MAC/PHY/radio). It provides a small form-factor solution with minimal external components to drive down the cost for mass volumes and allows for wireless media client flexibility in size, form, and function.

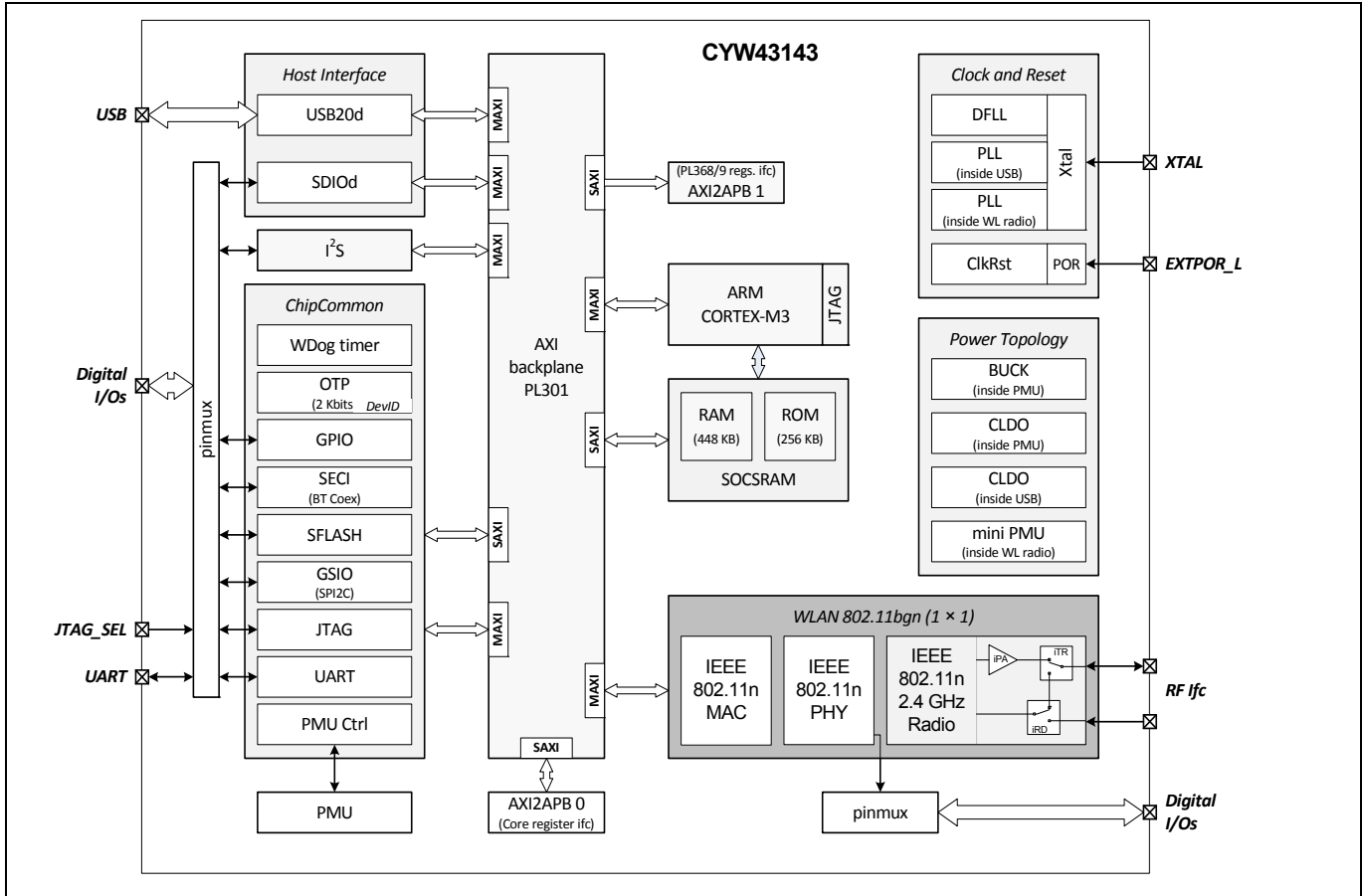
Figure 1. CYW43143 System Diagram Showing Two Antennas and a Single Stream



Employing a native 32-bit bus with a Direct Memory Access (DMA) architecture, the CYW43143 offers significant performance improvements in both transfer rates and CPU utilization. Flexible support for a variety of system bus interfaces is provided, including USB and SDIO devices.

Figure 2 shows a block diagram of the device.

Figure 2. CYW43143 Functional Block Diagram



2. Power Management and Resets

2.1 Power Management

The CYW43143 includes an internal Power Management Unit (PMU). The PMU takes care of powering up the chip, and also enables and disables clocks based on clock requests sent from CYW43143 internal blocks.

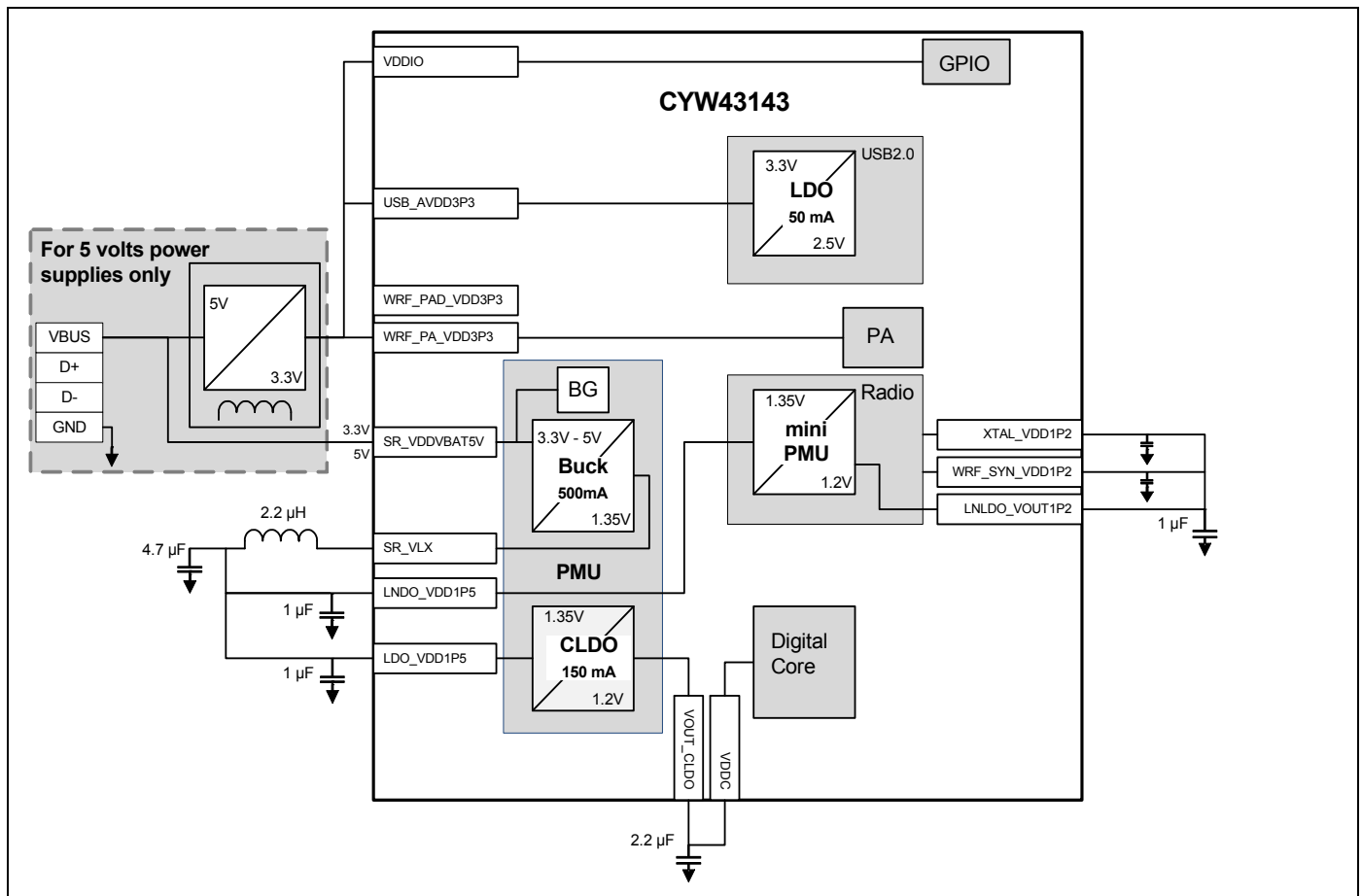
2.2 Power Topology

The CYW43143 contains a high-efficiency power topology to convert input supply voltages to the supply voltages required by the device's internal blocks. A CBUCK switching regulator is used to convert the input supply to 1.35V. Internal LDOs perform a low-noise conversion from 1.35V to 1.2V. As shown in Figure 3 on page 6, the CYW43143 supports two power supply configurations:

- A 3.3V power supply, connected to SR_VDDBAT5V, WRF_PA_VDD3P3, and WRF_PAD_VDD3P3.
- A 5V power supply connected to SR_VDDBAT5V, WRF_PA_VDD3P3, and WRF_PAD_VDD3P3 connected to 3.3V. The latter can be obtained through a DC-DC conversion as shown in Figure 3 on page 6.

The default VDDIO supply of the BCM43143 is 3.3V. In SDIO mode, the BCM43143 supports an SDIO interface specific voltage range of 1.8V to 3.3V. Refer to pin 46 description in Table 4 on page 18. All VDDIO pins other than pin 46 remain at 3.3V as described in Table 4 on page 18.

Figure 3. Power Topology with the VDD33 (3.3V) Main Supply



2.3 Reset and Low-Power Off Mode

Full-chip reset is achieved by switching off the 3.3V VDDIO voltage to pins 1, 25, 37, and 53. This puts the chip in reset and low-power off mode; in this mode the internal CBUCK switcher is shut down, bringing the total typical current consumption down to less than 100 µA. The device must be kept in reset/low-power off mode for at least 25 ms.

3. WLAN Global Functions

3.1 GPIO Interface

There are 19 General-Purpose I/O (GPIO) pins provided on the CYW43143. GPIOs 0–18 are multiplexed with the JTAG, SDIO, I²S, SFlash, and Serial Enhanced Coexistence Interface (SECI) functions. These pins can be used to interface to various external devices. Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. A programmable internal pull-up/pull-down resistor is included on each GPIO. If a GPIO output enable is not asserted, and the corresponding GPIO signal is not being driven externally, the GPIO state is determined by its programmable resistor.

3.2 OTP

The CYW43143 has 2 Kbits of on-chip One-Time Programmable (OTP) memory that can be used for non-volatile storage of WLAN information such as a MAC address and other hardware-specific board and interface configuration parameters.

3.3 JTAG Interface

The CYW43143 supports the IEEE 1149.1 JTAG boundary-scan standard for testing a packaged device on a manufactured board. The JTAG interface is enabled by driving the JTAG_SEL pin high.

3.4 Crystal Oscillator

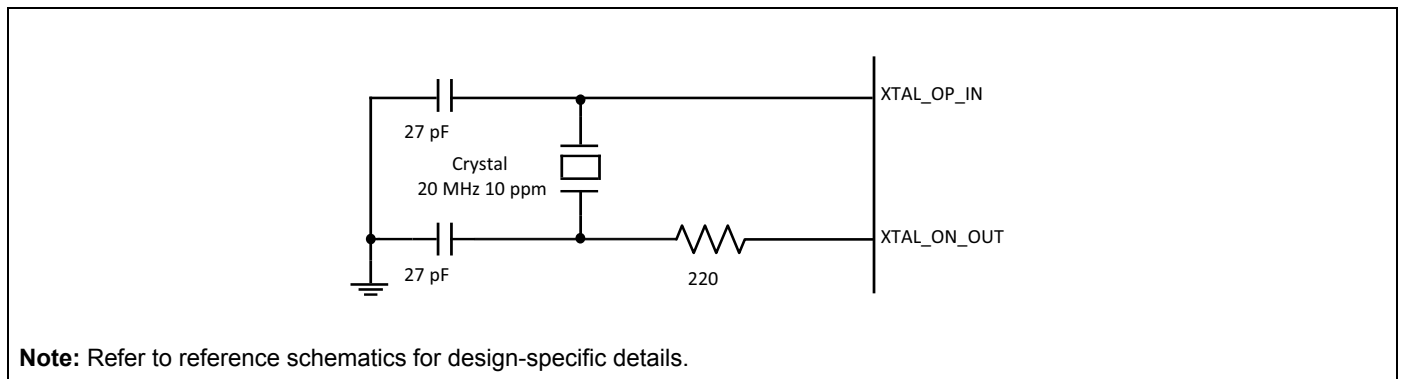
Table 2 lists the requirements for the crystal oscillator.

Table 2. Crystal Oscillator Requirements

| Parameter | Value |
|---------------------|---|
| Frequency | 20 MHz |
| Mode | AT cut, fundamental |
| Load capacitance | 16 pF |
| ESR | 50Ω maximum |
| Frequency stability | ±10 ppm at 25°C ±10 ppm at 0°C to +85°C |
| Aging | ±3 ppm/year maximum the first year, ±1 ppm thereafter |
| Drive level | 300 μW maximum |
| Q-factor | 40,000 minimum |
| Shunt capacitance | < 5 pF |

Figure 4 shows the recommended oscillator configuration.

Figure 4. Recommended Oscillator Configuration



Note: The component values referenced in Figure 4 are only recommended values and the correct values will have to be characterized on a per board basis. Please see the reference board schematic for the correct characterized values.

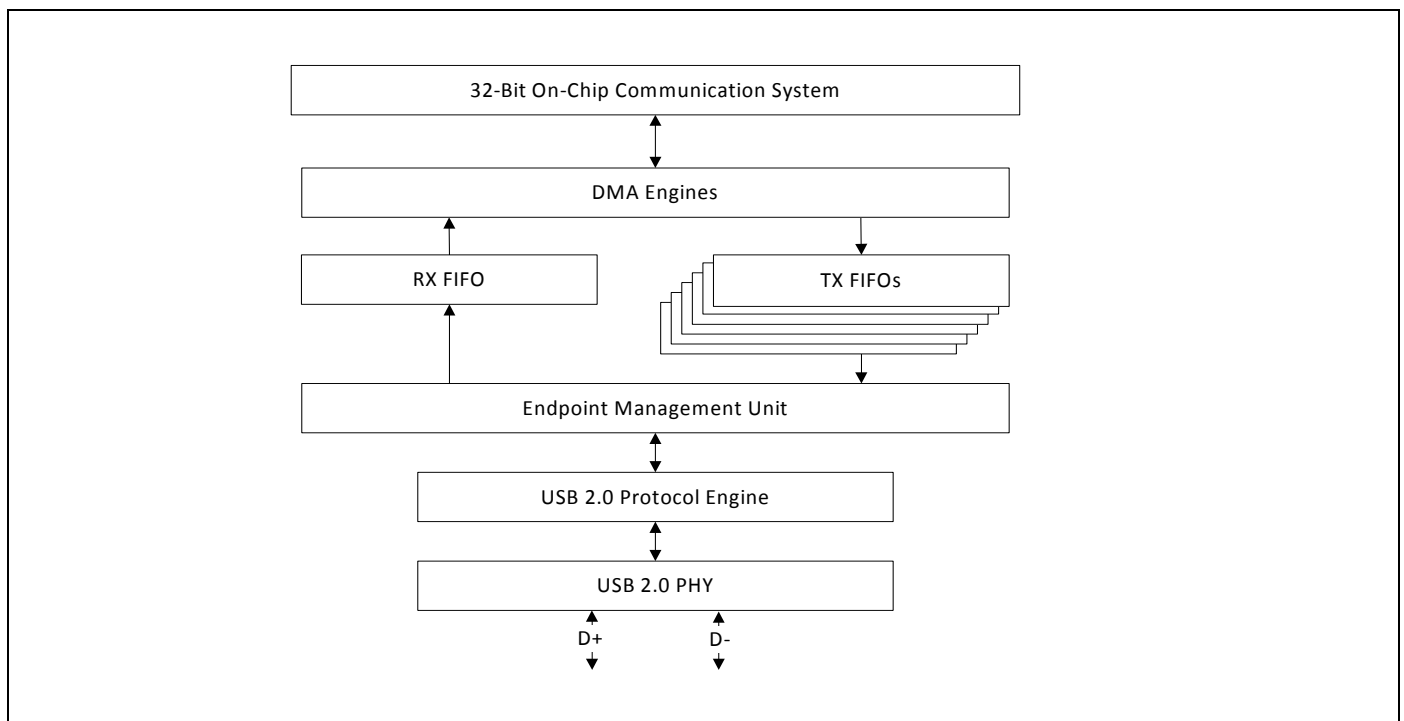
4. WLAN USB 2.0 Host Interface

The CYW43143 USB interface can be set to operate as a USB 2.0 port. Features include the following:

- A USB 2.0 protocol engine that supports the following:
 - A Parallel Interface Engine (PIE) between packet buffers and USB transceiver
 - Up to nine endpoints, including Configurable Control Endpoint 0
- Separate endpoint packet buffers with a 512-byte FIFO buffer each
- Host-to-device communication for bulk, control, and interrupt transfers
- Configuration and status registers

Figure 5 shows the blocks in the device core.

Figure 5. WLAN USB 2.0 Host Interface Block Diagram



The USB 2.0 PHY handles the USB protocol and the serial signaling interface between the host and device. It is primarily responsible for data transmission and recovery. On the transmit side, data is encoded, along with a clock, using the NRZI scheme with bit stuffing to ensure that the receiver detects a transition in the data stream. A SYNC field that precedes each packet enables the receiver to synchronize the data and clock recovery circuits. On the receive side, the serial data is deserialized, unstuffed, and checked for errors. The recovered data and clock are then shifted to the clock domain that is compatible with the internal bus logic.

The endpoint management unit contains the PIE control logic and the endpoint logic. The PIE interfaces between the packet buffers and the USB transceiver. It handles packet identification (PID), USB packets, and transactions.

The endpoint logic contains nine uniquely addressable endpoints. These endpoints are the source or sink of communication flow between the host and the device. Endpoint zero is used as a default control port for both the input and output directions. The USB system software uses this default control method to initialize and configure the device information and allows USB status and control access. Endpoint zero is always accessible after a device is attached, powered, and reset.

Endpoints are supported by 512-byte FIFO buffers, one for each IN endpoint and one shared by all OUT endpoints. Both TX and RX data transfers support a DMA burst of 4, which guarantees low latency and maximum throughput performance. The RX FIFO can never overflow by design. The maximum USB packet size cannot be more than 512 bytes.

4.1 Link Power Management (LPM) Support

The USB 2.0 host interface supports a power management feature called Link Power Management (LPM) which is similar to the existing suspend/resume, but has transitional latencies of tens of microseconds between power states (instead of three to greater

than 20 millisecond latencies of the USB 2.0 suspend/resume). LPM simply adds a new feature and bus state that co-exists with the USB 2.0 defined suspend/resume.

4.2 I²S Interface

The I²S interface for audio supports slave mode transmit 2.1 or 5.1 channel operation. The I²S signals are:

- I²S bit clock: I2S_BITCLK
- I²S Word Select: I2S_WS
- I²S Data Out: I2S_SDOOUT

I2S_BITCLK and I2S_WS are inputs, while I2S_SDOOUT is an output. Channel word lengths of 16 bits, 20 bits, 24 bits, and 32 bits are supported, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I2S_WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I2S_WS is low, and right-channel data is transmitted when I2S_WS is high. An embedded 128 x 32 bits single port SRAM for data processing enhances the performance of the interface.

The bit depth of I²S is 16, 20, 24, and 32.

Variable sampling rates are also supported:

- 8k, 12k, 16k, 24k, 32k, 48k, 96k with a 12.288 MHz master clock used by the external master receiver and/or controller
- 22.05k, 44.1k, 88.2k with a 11.2896 MHz master clock used by the external master receiver and/or controller
- 96k with a 24.567 MHz master clock used by the external master receiver and/or controller

The BCM43143 needs an external clock source input on the slave clock pin for the I²S interface. The slave clock frequency is dependent upon the audio sample rate and the external I²S codec.

5. SDIO Interface

The SDIO interface is enabled by a strapping option (see [Table 5 on page 21](#) for details). The CYW43143 supports all of the SDIO version 2.0 modes:

- 1-bit SDIO-SPI mode (25 Mbps)
- 1-bit SDIO-SD mode (25 Mbps)
- 4-bit SDIO-SD default speed mode (100 Mbps)
- 4-bit SDIO-SD high speed mode (200 Mbps).

The SDIO interface supports the full clock range from 0 to 50 MHz. The chip has the ability to stop the SDIO clock between transactions to reduce power consumption. As an option, the GPIO_4 or the GPIO_16 pin can be mapped to provide an SDIO Interrupt signal. This out-of-band interrupt is hardware generated and is always valid (unlike the SDIO in-band interrupt, which is signalled only when data is not driven on SDIO lines). The ability to force control of the gated clocks from within the WLAN chip is also provided. Three functions are supported:

- Function 0 standard SDIO function. Maximum BlockSize/ByteCount = 32 bytes.
- Function 1 backplane function to access the internal System-on-a-Chip (SoC) address space. Maximum BlockSize/ ByteCount = 64 bytes.
- Function 2 WLAN function for efficient WLAN packet transfer through DMA. Maximum BlockSize/ByteCount = 512 bytes.

6. Wireless LAN MAC and PHY

6.1 IEEE 802.11n MAC Description

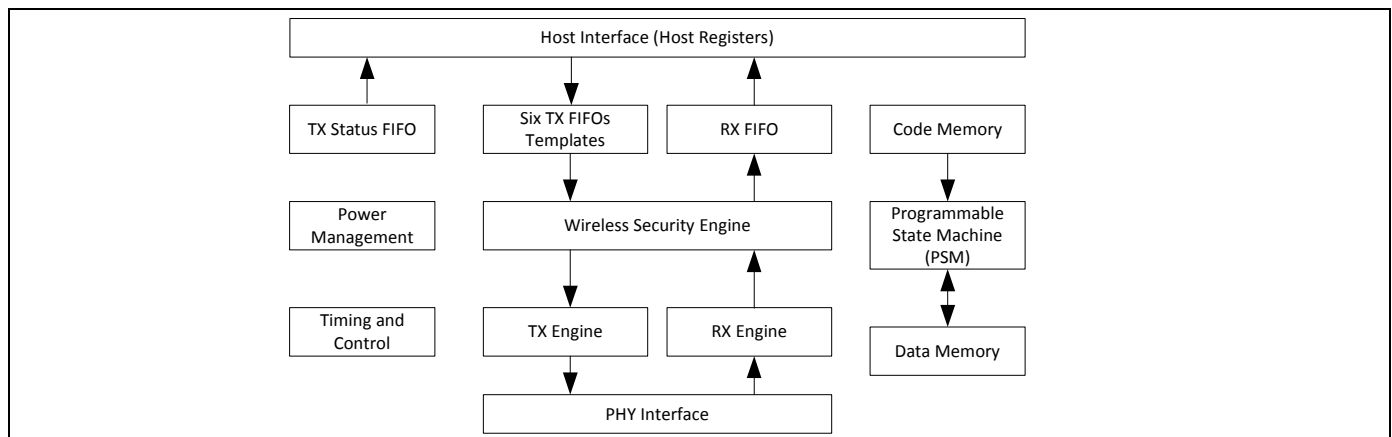
The IEEE 802.11n MAC features include:

- Enhanced MAC for supporting 802.11n features
- Programmable Access Point (AP) or Station (STA) functionality
- Programmable mode selection as Independent Basic Service Set (IBSS) or infrastructure
- Aggregated MAC Protocol Data Unit (MPDU) support for High Throughput (HT)
- Passive scanning
- Network Allocation Vector (NAV), Interframe Space (IFS), and Timing Synchronization Function (TSF) functionality
- RTS/CTS procedure support
- Transmission of response frames (ACK/CTS)
- Address filtering of receive frames as specified by IBSS rules
- Multirate support
- Programmable Target Beacon Transmission Time (TBTT), beacon transmission/cancellation, and Announcement Traffic Indication Message (ATIM) window
- Coordination Function (CF) conformance: Setting a NAV for neighborhood Point Coordination Function (PCF) operation
- Security through a variety of encryption schemes including WEP, TKIP, AES, WPA, WAP2, and IEEE 802.1X
- Power management
- Statistics counters for MIB support

The MAC core supports the transmission and reception of packet sequences, together with related timing, without any packet-by-packet driver interaction. Time-critical tasks requiring response times of only a few milliseconds are handled in the MAC core. This achieves the required medium timing while minimizing driver complexity. Also, the MAC driver processes incoming packets that have been buffered in the MAC core in bursts, enabling high bandwidth performance.

The MAC driver interacts with the MAC core to prepare transmit packet queues and to analyze and forward received packets to upper software layers. The internal blocks of the MAC core are connected to a Programmable State Machine (PSM) through the host interface that connects to the internal bus (see [Figure 6 on page 11](#)).

Figure 6. Enhanced MAC Block Diagram



The host interface consists of registers for controlling and monitoring the status of the MAC core and interfacing with the TX/RX FIFOs. For transmission, 32 KB of FIFO buffering is available that can be dynamically allocated to six transmit queues plus template space for beacons, ACKs, and probe responses. Whenever the host has a frame to transmit, the host queues the frame into one of the transmit FIFOs with a TX descriptor containing TX control information. The PSM schedules the transmission on the medium depending

on the frame type, transmission rules in the IEEE 802.11™ protocol, and the current medium occupancy scenario. After the transmission completes, a TX status is returned to the host, informing the host of the transmission.

The MAC contains a 10 KB RX FIFO. Received frames are sent to the host along with RX descriptors that contain additional frame reception information.

The power management block maintains power management state information of the core (and of the associated STAs in the case of an AP) to help with dynamic frame transmission decisions by the core.

The wireless security engine performs the required encryption/decryption on the TX/RX frames. This block supports separate transmit and receive keys with four shared keys and 50 link-specific keys. The link-specific keys are used to establish a secure link between any two network nodes. The wireless security engine supports the following encryption schemes that can be selected on a per-destination basis:

- None: The wireless security engine acts as a pass-through
- WEP: 40-bit secure key and 24-bit IV as defined in IEEE Std. 802.11-2007
- WEP128: 104-bit secure key and 24-bit IV
- TKIP: IEEE Std. 802.11-2007
- AES: IEEE Std. 802.11-2007

The transmit engine is responsible for the byte flow from the TX FIFO to the PHY interface through the encryption engine and the addition of a CRC-32 Frame Check Sequence (FCS) as required by IEEE 802.11-2007. Similarly, the receive engine is responsible for byte flow from the PHY interface to the RX FIFO through the decryption engine and for detection of errors in the RX frame.

The timing block performs the TSF, NAV, and IFS functionality as described in IEEE Std. 802.11-2007.

The Programmable State Machine (PSM) coordinates the operation of different hardware blocks required for both transmission and reception. The PSM also maintains the statistics counters required for MIB support.

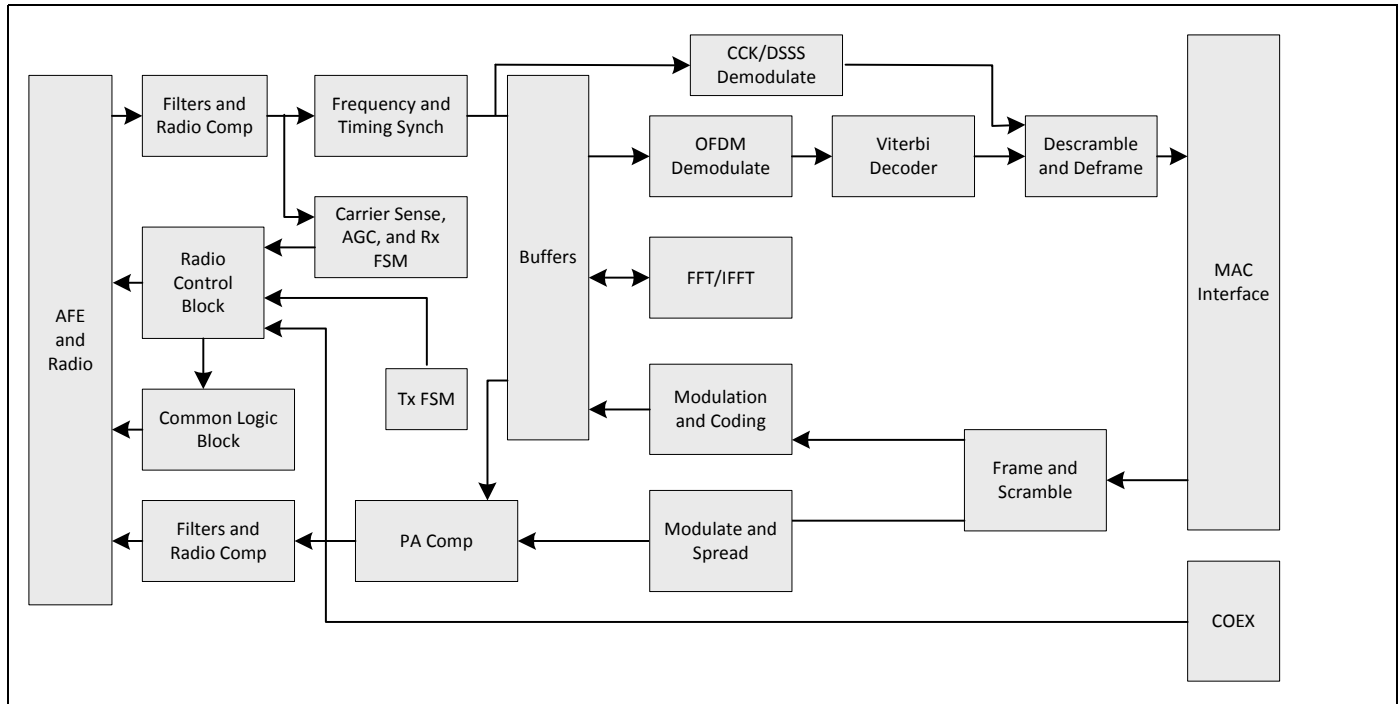
6.2 IEEE 802.11n PHY Description

The PHY supports:

- Programmable data rates from MCS 0–7 in 20 MHz and 40 MHz channels, as specified in 802.11n.
- Short Guard Interval (SGI) and optional reception of two space-time block encoded streams.
- All scrambling, encoding, forward error correction, and modulation in the transmit direction, and inverse operations in the receive direction.
- Advanced digital signal processing technology for best-in-class receive sensitivity.
- Both mixed-mode and optional greenfield preamble of 802.11n.
- Both long and optional short IEEE 802.11b preambles.
- Closed-Loop transmit power control.
- Per-packet receive antenna diversity.
- Automatic Gain Control (AGC).
- Available per-packet channel quality and signal strength measurements.

The CYW43143 PHY provides baseband processing at all mandatory 802.11n data rates up to 150 Mbps, and the legacy rates specified in IEEE 802.11b/g, including 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbps. This core acts as an intermediary between the MAC and the 2.4 GHz radio, converting back and forth between packets and baseband waveforms.

Figure 7. PHY Block Diagram



6.3 Single-Band Radio Transceiver

The CYW43143 has a 2.4 GHz radio transceiver that ensures low power consumption and robust communication in 20 MHz and 40 MHz channel bandwidths as specified in IEEE 802.11n.

6.3.1 Receiver Path

The CYW43143 has a wide dynamic range, direct conversion receiver. It employs high-order, on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The excellent noise figure of the receiver makes an external LNA unnecessary.

6.3.2 Transmitter Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band. Linear on-chip power amplifiers are included, which are capable of delivering a nominal output power exceeding +15 dBm while meeting the IEEE 802.11n specification. The TX gain has 128 steps of 0.25 dB per step.

6.3.3 Calibration

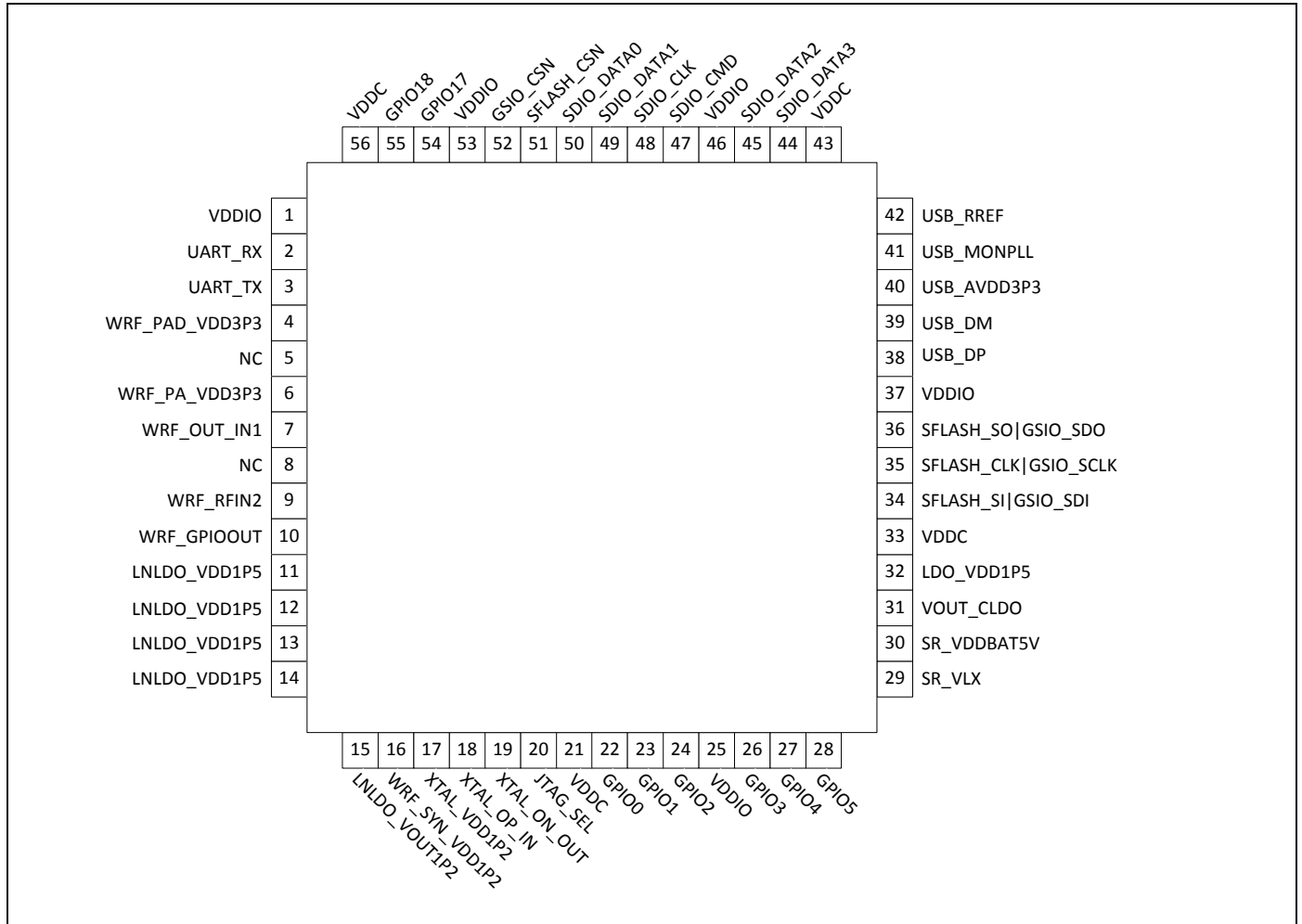
The CYW43143 features dynamic on-chip calibration, eliminating process variation across components. This enables the device to be used in high-volume applications because calibration routines are not required during manufacturing. These calibration routines are performed periodically in the course of normal radio operation.

7. Pin Assignments

7.1 56-Pin QFN Assignments

The 56-pin QFN package pin assignments are shown in Figure 8.

Figure 8. CYW43143 56-Pin QFN Package



7.1.1 56-Pin QFN Signals

Pin Assignments by Pin Number

Table 3. Pin Assignments by Pin Number

| Pin | Signal Name |
|-----|----------------|
| 1 | VDDIO |
| 2 | UART_RX |
| 3 | UART_TX |
| 4 | WRF_PAD_VDD3P3 |
| 5 | GND |
| 6 | WRF_PA_VDD3P3 |

| Pin | Signal Name |
|-----|----------------------|
| 7 | WRF_OUT_IN1 |
| 8 | GND |
| 9 | WRF_RFIN2 |
| 10 | WRF_GPIOOUT |
| 11 | LNLDO_VDD1P5 |
| 12 | LNLDO_VDD1P5 |
| 13 | LNLDO_VDD1P5 |
| 14 | LNLDO_VDD1P5 |
| 15 | LNLDO_VOUT1P2 |
| 16 | WRF_SYN_VDD1P2 |
| 17 | XTAL_VDD1P2 |
| 18 | XTAL_OP_IN |
| 19 | XTAL_ON_OUT |
| 20 | JTAG_SEL |
| 21 | VDDC |
| 22 | GPIO0 |
| 23 | GPIO1 |
| 24 | GPIO2 |
| 25 | VDDIO |
| 26 | GPIO3 |
| 27 | GPIO4 |
| 28 | GPIO5 |
| 29 | SR_VLX |
| 30 | SR_VDDBAT5V |
| 31 | VOUT_CLDO |
| 32 | LDO_VDD1P5 |
| 33 | VDDC |
| 34 | SFLASH_SI GSIO_SDI |
| 35 | SFLASH_CLK GSIO_SCLK |
| 36 | SFLASH_SO GSIO_SDO |
| 37 | VDDIO |
| 38 | USB_DP |
| 39 | USB_DM |
| 40 | USB_AVDD3P3 |
| 41 | USB_MONPLL |
| 42 | USB_RREF |
| 43 | VDDC |
| 44 | SDIO_DATA3 |
| 45 | SDIO_DATA2 |
| 46 | VDDIO |
| 47 | SDIO_CMD |

| Pin | Signal Name |
|-----|-------------|
| 48 | SDIO_CLK |
| 49 | SDIO_DATA1 |
| 50 | SDIO_DATA0 |
| 51 | SFLASH_CSN |
| 52 | GSIO_CSN |
| 53 | VDDIO |
| 54 | GPIO17 |
| 55 | GPIO18 |
| 56 | VDDC |

Pin Assignments by Pin Name

Table 4. Pin Assignments by Signal Name

| Signal Name | Pin |
|----------------------|-----|
| GPIO0 | 22 |
| GPIO1 | 23 |
| GPIO2 | 24 |
| GPIO3 | 26 |
| GPIO4 | 27 |
| GPIO5 | 28 |
| GPIO17 | 54 |
| GPIO18 | 55 |
| GSIO_CSN | 52 |
| JTAG_SEL | 20 |
| LDO_VDD1P5 | 32 |
| LNLDO_VDD1P5 | 11 |
| LNLDO_VDD1P5 | 12 |
| LNLDO_VDD1P5 | 13 |
| LNLDO_VDD1P5 | 14 |
| LNLDO_VOUT1P2 | 15 |
| GND | 5 |
| GND | 8 |
| SDIO_CLK | 48 |
| SDIO_CMD | 47 |
| SDIO_DATA0 | 50 |
| SDIO_DATA1 | 49 |
| SDIO_DATA2 | 45 |
| SDIO_DATA3 | 44 |
| SFLASH_CLK GSIO_SCLK | 35 |
| SFLASH_CSN | 51 |
| SFLASH_SI GSIO_SDI | 34 |
| SFLASH_SO GSIO_SDO | 36 |
| SR_VDDBAT5V | 30 |
| SR_VLX | 29 |
| UART_RX | 2 |
| UART_TX | 3 |
| USB_AVDD3P3 | 40 |
| USB_DM | 39 |
| USB_DP | 38 |
| USB_MONPLL | 41 |
| USB_RREF | 42 |
| VDDC | 21 |
| VDDC | 33 |

| Signal Name | Pin |
|----------------|-----|
| VDDC | 43 |
| VDDC | 56 |
| VDDIO | 1 |
| VDDIO | 25 |
| VDDIO | 37 |
| VDDIO | 46 |
| VDDIO | 53 |
| VOUT_CLDO | 31 |
| WRF_GPIOOUT | 10 |
| WRF_OUT_IN1 | 7 |
| WRF_PA_VDD3P3 | 6 |
| WRF_PAD_VDD3P3 | 4 |
| WRF_RFIN2 | 9 |
| WRF_SYN_VDD1P2 | 16 |
| XTAL_ON_OUT | 19 |
| XTAL_OP_IN | 18 |
| XTAL_VDD1P2 | 17 |

8. Signal and Pin Descriptions

8.1 Package Signal Descriptions

The signal name, type, and description of each pin in the CYW43143 56-pin QFN package is listed in Table 4. The symbols shown in the Type column indicate pin directions (I/O = bidirectional, I = input, O = output, and OD = open drain output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any. Resistor strapping options are defined in Table 5 on page 21.

Table 4. CYW43143 Signal Descriptions

| Pin | Signal | Type | Description |
|---|--------------------|------|--|
| SDIO Bus Interface | | | |
| 48 | SDIO_CLK | I/O | SDIO clock When not used as SDIO this is a general purpose GPIO pin (GPIO12) or an I ² S Audio Interface signal (I2S_WS) |
| 47 | SDIO_CMD | I/O | SDIO bus command line When not used as SDIO this is a general purpose GPIO pin (GPIO11) or an I ² S Audio Interface signal (I2S_BITCLK) |
| 50 | SDIO_DATA0 | I/O | SDIO data line 0 When not used as SDIO this is a general purpose GPIO pin (GPIO14) |
| 49 | SDIO_DATA1 | I/O | SDIO data line 1 When not used as SDIO this is a general purpose GPIO pin (GPIO13) or an I ² S Audio Interface signal (I2S_SDOUT) |
| 45 | SDIO_DATA2 | I/O | SDIO data line 2 When not used as SDIO this is a general purpose GPIO pin (GPIO10) |
| 44 | SDIO_DATA3 | I/O | SDIO data line 3 When not used as SDIO this is a general purpose GPIO pin (GPIO9) |
| USB Interface | | | |
| 39 | USB_DM | I/O | USB data negative |
| 38 | USB_DP | I/O | USB data positive |
| 41 | USB_MONPLL | – | USB reserved pin for Diagnostic purposes only |
| 42 | USB_RREF | – | USB bandgap reference resistor/capacitor, tie this pin in parallel through a 100 pF capacitor and a 4 kΩ resistor to ground |
| WLAN RF Signal Interface | | | |
| 7 | WRF_OUT_IN1 | I/O | 2.4 GHz RF output, 2.4 GHz RF input 1 |
| 9 | WRF_RFIN2 | I | 2.4 GHz RF input 2 |
| 10 | WRF_GPIOOUT | O | WLAN reference output. Connect to ground through a 15 kΩ, 1% resistor. |
| I²S Audio Interface | | | |
| 47 | I2S_BITCLK | I/O | I ² S serial bit clock, only available when no SDIO I/F |
| 48 | I2S_WS | I/O | I ² S word select, only available when no SDIO I/F |
| 49 | I2S_SDOUT | I/O | I ² S serial data out, only available when no SDIO I/F |
| Serial Flash Interface and SPI/BSC Interface | | | |
| 51 | SFLASH_CSN | I/O | Serial flash chip select. When not used as SFLASH, this is a general purpose GPIO pin (GPIO15) |
| 34 | SFLASH_SI GSIO_SDI | I/O | This pin is muxed with: <ul style="list-style-type: none"> Serial flash data in SPI/BSC data in When not used as SFLASH or GSIO this is a general purpose GPIO pin (GPIO6) |

Table 4. CYW43143 Signal Descriptions (Cont.)

| Pin | Signal | Type | Description |
|------------------|--|----------|--|
| 36 | SFLASH_SO GSIO_SDO | I/O | This pin is muxed with: <ul style="list-style-type: none"> Serial flash data out SPI/BSC data out When not used as SFLASH or GSIO this is a general purpose GPIO pin (GPIO8) |
| 35 | SFLASH_CLK GSIO_SCLK | I/O | This pin is muxed with: <ul style="list-style-type: none"> Serial flash clock SPI/BSC clock When not used as SFLASH or GSIO this is a general purpose GPIO pin (GPIO7) |
| 52 | GSIO_CSN | I/O | SPI/BSC chip select. When not used as GSIO this is a general purpose GPIO pin (GPIO16). |
| GPIO Pins | | | |
| 22 | GPIO0 TDI BTCX_RF_ACTIVE SECI_IN0 | I/O | This pin is muxed with: <ul style="list-style-type: none"> GPIO0, a general purpose I/O pin JTAG test data in Legacy BT coexistence RF Active SECI in0 |
| 23 | GPIO1 TDO BTCX_TX_CONF SECI_OUT | I/O | This pin is muxed with: <ul style="list-style-type: none"> GPIO1, a general purpose I/O pin JTAG test data out Legacy BT coexistence TX Conf SECI out |
| 24 | GPIO2 TCK BTCX_STATUS SECI_AUX0 | I/O | This pin is muxed with: <ul style="list-style-type: none"> GPIO2, a general purpose I/O pin JTAG test clock Legacy BT coexistence Status SECI aux0 |
| 26 | GPIO3 TRST-L BTCX_PRISEL SECI_IN1 | I/O | This pin is muxed with: <ul style="list-style-type: none"> GPIO3, a general purpose I/O pin JTAG test reset low Legacy BT coexistence Priority Select SECI in1 |
| 27 | GPIO4 TMS BTCX_FREQ | I/O | This pin is muxed with: <ul style="list-style-type: none"> GPIO4, a general purpose I/O pin JTAG test mode select Legacy BT coexistence FREQ |
| 28 | GPIO5 EXTPOR_L | I/O (PU) | This pin is muxed with: <ul style="list-style-type: none"> GPIO5, a general purpose I/O pin External power-on reset low, when JTAG_SEL high |
| 54 | GPIO17 | I/O (PD) | General purpose I/O pin |
| 55 | GPIO18 | I/O (PD) | General purpose I/O pin |

Table 4. CYW43143 Signal Descriptions (Cont.)

| Pin | Signal | Type | Description |
|--|----------------|----------|---|
| UART Interface | | | |
| 2 | UART_RX | I/O (PD) | UART receive data (SW debug) |
| 3 | UART_TX | I/O (PU) | UART transmit data (SW debug) |
| Crystal Oscillator | | | |
| 19 | XTAL_ON_OUT | O | XTAL oscillator output. Connect a 20 MHz, 10 ppm crystal between the XTAL_ON_OUT and XTAL_OP_IN pins |
| 18 | XTAL_OP_IN | I | XTAL oscillator input |
| Test Pins | | | |
| 20 | JTAG_SEL | I (PD) | JTAG select |
| Strap Pins | | | |
| 2 | UART_RX | I/O (PD) | Strap RemapToROM[1] |
| 3 | UART_TX | I/O (PU) | Strap RemapToROM[0] |
| 34 | SFLASH_SI | I/O (PD) | Strap SDIOHighDrive |
| 54 | GPIO17 | I/O (PD) | Strap SDIOEnabled |
| 55 | GPIO18 | I/O (PD) | Strap SDIOIso |
| Integrated Voltage Regulators | | | |
| 11, 12, 13, 14 | LNLDO_VDD1P5 | PWR | LNLDO 1.5V input |
| 15 | LNLDO_VOUT1P2 | PWR | LNLDO 1.2V output |
| 30 | SR_VDDBAT5V | PWR | VBAT power input |
| 29 | SR_VLX | PWR | CBUCK switching regulator output |
| 31 | VOUT_CLDO | PWR | Output of core LDO |
| 32 | LDO_VDD1P5 | PWR | Input of core LDO |
| WLAN Power Supplies | | | |
| 40 | USB_AVDD3P3 | PWR | USB 3.3V input |
| 16 | WRF_SYN_VDD1P2 | PWR | RF synthesizer VDD 1.2V input |
| 6 | WRF_PA_VDD3P3 | PWR | WLAN PA 3.3V supply |
| 4 | WRF_PAD_VDD3P3 | PWR | WLAN PA driver 3.3V supply |
| 17 | XTAL_VDD1P2 | PWR | XTAL oscillator 1.2V supply |
| Miscellaneous Power Supplies and Ground | | | |
| 21, 33, 43, 56 | VDDC | PWR | Core supply for WLAN |
| 1, 25, 37, 53 | VDDIO | PWR | I/O supply for pads (3.3V) |
| 46 | VDDIO | PWR | I/O supply for SDIO pads (1.8V to 3.3V). Can only be 3.3V when USB is used. |
| H | GND_SLUG | GND | Ground |
| 5, 8 | GND | GND | Ground |

8.2 Strapping Options

The pins listed in [Table 5](#) are sampled at Power-On Reset (POR) to determine the various operating modes. Sampling occurs within a few milliseconds following internal POR or deassertion of external POR. After POR, each pin assumes the function specified in the signal descriptions table. Each pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND (use 10 kΩ or less)¹.

1. CYW43143 reference board schematics can be obtained through your Cypress representative.

Table 5. Strapping Options

| Signal Name | Mode | Default | Description |
|--------------------|-----------------|---------|---|
| [UART_RX, UART_TX] | RemapToROM[1:0] | [PD,PU] | 00 = Boot from SRAM, ARMCM3 in reset, no SFLASH connected 01 = Boot from ROM, no SFLASH connected (default) 10 = Boot from SFLASH 11 = Invalid |
| GPIO17 | SDIOEnabled | PD | 0 = USB Enabled, SDIO pins can be GPIO or I ² S (default) 1 = SDIO Enabled |
| GPIO18 | SDIOIso | PD | 0 = SDIO pads are not in Isolation mode (default) 1 = Keep SDIO pads in Isolation mode |
| SFLASH_SI | SDIOHighDrive | PD | 0 = SDIO pins drive strength set by SDIOd core or PMU Chip Control (= default) 1 = SDIO pins drive strength set by SDIOd core to either 12 mA or 16 mA |

9. Electrical Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

9.1 Absolute Maximum Ratings

Caution! These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect the long-term reliability of the device.

Table 6. Absolute Maximum Ratings

| Rating | Symbol | Minimum | Maximum | Unit |
|--|----------------------------------|---------|-----------------|------|
| DC supply for CBUCK switching regulator | SR_VDDBAT5V | -0.5 | 5.5 | V |
| DC supply voltage for the WL PA/PA driver | WRF_PA_VDD3P3, WRF_PAD_VDD3P3 | -0.5 | 3.8 | V |
| DC supply voltage for I/O | VDDIO | -0.5 | 3.8 | V |
| DC supply voltage for the CYW43143 core | VDDC | -0.5 | 1.32 | V |
| DC supply voltage for CYW43143 RF blocks | WRF_SYN_VDD1P2, XTAL_VDD1P2 | -0.5 | 1.32 | V |
| DC input supply voltage for CLDO and LNLDO | LDO_VDD1P5, LNLDO_ VDD1P5 | -0.5 | 2.1 | V |
| Maximum junction temperature | T _{J_MAX} | - | 125 | °C |
| Operating humidity | - | - | 85 | % |
| Ambient operating temperature | - | - | 65 ^a | °C |
| Storage temperature | T _{STG} | -40 | 125 | °C |
| Storage humidity | - | - | 60 | % |
| ESD protection (HBM) | V _{ESD} | - | 2000 | V |

a. On a 1s1P JEDEC board, not exceeding T_{J_MAX}, see [Section 14.: "Thermal Information,"](#) on page 39.

9.2 Recommended Operating Conditions and DC Characteristics

Table 7. Guaranteed Operating Conditions and DC Characteristics

| Element | Parameter | Value | | | Unit |
|--|----------------------------------|---------------|---------|---------------|------|
| | | Minimum | Typical | Maximum | |
| DC supply for CBUCK switching regulator | SR_VDDBAT5V | 2.3 | 3.6 | 5.25 | V |
| DC supply voltage for WL PA/PA driver | WRF_PA_VDD3P3, WRF_PAD_VDD3P3 | 2.97 | 3.3 | 3.63 | V |
| DC supply voltage for core | VDDC | 1.14 | 1.2 | 1.26 | V |
| DC supply voltage for RF blocks in chip | VDDRF | 1.14 | 1.2 | 1.26 | V |
| SDIO Interface I/O Pins^a | | | | | |
| Input high voltage | VIH | 0.625 × VDDIO | - | - | V |
| Input low voltage | VIL | - | - | 0.25 × VDDIO | V |
| Output high voltage @ 2 mA | VOH | 0.75 × VDDIO | - | - | V |
| Output low voltage @ 2 mA | VOL | - | - | 0.125 × VDDIO | V |
| Other Digital I/O Pins | | | | | |
| Input low voltage | VIL | - | - | 0.8 | V |

Table 7. Guaranteed Operating Conditions and DC Characteristics (Cont.)

| Element | Parameter | Value | | | Unit |
|-----------------------------------|-----------|--------------|---------|---------|------|
| | | Minimum | Typical | Maximum | |
| Input high voltage | VIH | 2.0 | – | – | V |
| Output low voltage @ 2 mA | VOL | – | – | 0.4 | V |
| Output high voltage @ 2 mA | VOH | VDDIO – 0.4V | – | – | V |
| RF Switch Control I/O Pins | | | | | |
| Input low voltage | VIL | – | – | 0.8 | V |
| Input high voltage | VIH | 2.0 | – | – | V |
| Output low voltage @ 2 mA | VOL | – | – | 0.4 | V |
| Output high voltage @ 2 mA | VOH | VDDIO – 0.4V | – | – | V |
| Input capacitance | Cin | – | – | 5 | pf |

a. VDDIO voltage tolerance is ±10%; for SDIO 1.8V levels (VDDIO at pin 46 = 1.8V ±10%), the maximum SDIO clock frequency should be limited to 25 MHz in high-speed mode only.

9.3 WLAN Current Consumption

The WLAN current consumption measurements are shown in [Table 8](#) through [Table 9](#) on page 24.

Table 8. WLAN Current Consumption in SDIO Mode using SR_VDDBAT5V^a

| Host Interface SDIO | VDDIO | SR_VDDBAT5V | WRF_PA_VDD3P3 | WRF_PAD_VDD3P3 | USB_AVDD3P3 | I_Total | P_Total |
|--|-------|-------------|---------------|----------------|-------------|---------|---------|
| | mA | | | | | | mW |
| OFF (Low power off mode: VDDIO switched off) | 0 | 0.07 | 0 | 0 | 0 | 0.07 | 0.2 |
| Sleep ^b | 1 | 2 | 0 | 1 | 1 | < 5 | < 17 |
| Power save ^c | 1 | 3 | 0 | 1 | 1 | < 6 | < 20 |
| RX (Listen), 2.4 GHz HT 20 ^d | 1 | 40 | 0 | 1 | 0 | 42 | 139 |
| RX (Active), 2.4 GHz HT 20 ^{e,f} | 2 | 65 | 0 | 1 | 0 | 68 | 224 |
| TX CCK (20 dBm @ Chip port, 2.4 GHz HT 20) ^g | 1 | 56 | 329 | 30 | 0 | 416 | 1373 |
| TX OFDM, 54 Mbps (–20 dBm @ Chip port, 2.4 GHz HT 20) ^g | 2 | 58 | 295 | 30 | 0 | 385 | 1265 |
| TX MCS7 (18 dBm @ Chip port, 2.4 GHz HT20) ^g | 2 | 72 | 249 | 24 | 0 | 347 | 1145 |
| TX MCS7 (18 dBm @ Chip port, 2.4 GHz HT40) ^g | 2 | 78 | 272 | 25 | 0 | 377 | 1244 |

- a. Typical numbers, measured at 3.3V, 25°C.
- b. Inter-beacon sleep.
- c. Beacon interval = 102.4 ms, DTIM = 3, Beacon duration = 1 ms @ 1 Mbps. Integrated sleep + wake up + Beacon RX current over 3 DTIM intervals.
- d. Carrier sense (CCA) when no carrier present.
- e. Carrier sense (CS) detect/packet RX.
- f. Applicable to all supported rates.
- g. Duty cycle is 100%.

Table 9. WLAN Current Consumption in USB mode using VDD33^a

| | VDDIO | SR_VDDBAT5V | WRF_PA_VDD3P3 | WRF_PAD_VDD3P3 | USB_AVDD3P3 | I_Total | P_Total |
|--|-------|-------------|---------------|----------------|-------------|---------|---------|
| Host Interface USB | mA | | | | | | mW |
| OFF (Low power off mode: VDDIO switched off) | 0 | 0.07 | 0 | 0 | 0 | 0.07 | 0.2 |
| Sleep ^b | 0.4 | 2 | 0 | 1 | 5.6 | < 9 | < 30 |
| Power save ^c | 0.4 | 3 | 0 | 1 | 5.6 | < 10 | < 33 |
| RX (Listen), 2.4 GHz HT 20 ^d | 0.4 | 45 | 0 | 1 | 22 | 68 | 226 |
| RX (Active), 2.4 GHz HT 20 ^{e,f} | 0.4 | 70 | 0 | 1 | 23 | 94 | 312 |
| TX CCK (20 dBm @ Chip port, 2.4 GHz HT 20) ^g | 0.5 | 55 | 320 | 30 | 21 | 427 | 1407 |
| TX OFDM, 54 Mbps (-20 dBm @ Chip port, 2.4 GHz HT 20) ^g | 0.4 | 59 | 265 | 30 | 21 | 376 | 1239 |
| TX MCS7 (18 dBm @ Chip port, 2.4 GHz HT20) ^g | 0.6 | 74 | 248 | 24 | 21 | 368 | 1213 |
| TX MCS7 (18 dBm @ Chip port, 2.4 GHz HT40) ^g | 1.6 | 80 | 272 | 25 | 21 | 400 | 1319 |

- a. Typical numbers, measured at 3.3V, 25°C.
- b. Inter-beacon sleep.
- c. Beacon interval = 102.4 ms, DTIM = 3, Beacon duration = 1 ms @ 1 Mbps.
Integrated sleep + wake up + Beacon RX current over 3 DTIM intervals.
- d. Carrier sense (CCA) when no carrier present.
- e. Carrier sense (CS) detect/packet RX.
- f. Applicable to all supported rates.
- g. Duty cycle is 100%.

10. Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization. Functional operation is not guaranteed outside of the specification limits provided in this section.

10.1 Core Buck Switching Regulator

Table 10. Core Buck Switching Regulator (CBUCK) Specifications

| Specification | Notes | Min | Typ | Max | Units |
|--|--|-------------------|------|------------------|-------|
| Input supply voltage (DC) | DC voltage range inclusive of disturbances. | 2.3 | 3.6 | 5.25 | V |
| Input supply voltage (spikes) | Up to 10 seconds cumulative duration over 7 years lifetime. 10 ms maximum pulse width. | – | – | 5.5 | V |
| PWM mode switching frequency | CCM: Load > 100 mA SR_VDDBAT5V = 3.6V | 2 | 4 | 6 | MHz |
| PWM output current | – | – | – | 500 ^a | mA |
| Output current limit | – | – | 1390 | – | mA |
| Output voltage range | Programmable, 30 mV steps Default = 1.35V | 1.2 | 1.35 | 1.5 | V |
| PWM output voltage DC accuracy | Includes load and line regulation. Forced PWM mode | –4 | – | 4 | % |
| PWM ripple voltage, static | Measure with 20 MHz bandwidth limit. | – | 7 | 20 | mVpp |
| PWM mode peak efficiency | Peak Efficiency at 200 mA load | 78 | 84 | – | % |
| PFM mode efficiency | 5 mA load current | – | 65 | – | % |
| Low Power Operating mode (LPOM) efficiency | 5 mA load current | – | 80 | – | % |
| Start-up time from power down | VDDIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V | – | – | 850 | µs |
| External inductor | 0603 size, ±30%, 0.26 ±25% ohms | 1.2 | 2.2 | 3.3 | µH |
| External output capacitor | Ceramic, X5R, 0402, ESR <30mΩ at 4 MHz, ±20%, 6.3V | 2.53 ^b | 4.7 | 10 | µF |
| External input capacitor | For SR_VDDBAT5V pin, Ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V, 4.7 µF | 0.76 ^b | 4.7 | – | µF |
| Operating junction temperature | – | –40 | 50 | 125 | °C |
| Input supply voltage ramp-up time | 0 to 4.3V | 40 | – | – | µs |

a. 500 mA TT junction temp 110°C. Derate to 372 mA for $T_j > 125^\circ\text{C}$.

b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

10.2 CLDO

Table 11. CLDO Specifications

| Specification | Notes | Min | Typ | Max | Units |
|-------------------------------------|--|-------------------|------|-------|-------------|
| Input supply voltage (V_{in}) | Min = $1.2 + 0.1V = 1.3V$ Dropout voltage requirement must be met under maximum load. | 1.2 | 1.35 | 1.5 | V |
| Output current ^a | – | – | – | 150 | mA |
| Output voltage (V_o) | Programmable in 25 mV steps. Default = 1.2V | 1.1 | 1.2 | 1.275 | V |
| Dropout voltage | At max load | – | – | 100 | mV |
| Output voltage DC accuracy | Includes line/load regulation | –4 | – | +4 | % |
| Quiescent current | No load | – | 10 | – | μA |
| Line regulation | V_{in} from ($V_o + 0.1V$) to 1.5V, maximum load | – | – | +1.1 | $\%V_o/V$ |
| Load regulation | Load from 1 mA to 150 mA | – | – | 0.02 | $\%V_o/mA$ |
| Leakage current ^b | Power-down | – | – | 10 | μA |
| Power supply rejection ratio (PSRR) | @1 kHz $V_{in} \geq 1.35V$ $C_o = 2.2 \mu F$ | 20 | – | – | dB |
| PMU start-up time | SR_VDDBAT5V up and stable. Time from the VDDIO rising edge to the CLDO reaching 1.2V. | – | – | 850 | μs |
| LDO turn-on time | LDO turn-on time when rest of the chip is up | – | – | 180 | μs |
| In-rush current during turn-on | Measured when the output capacitor is fully discharged. | – | – | 150 | mA |
| External output capacitor, C_o | Total ESR: 30–200 m Ω | 1.67 ^c | 1 | – | μF |
| External input capacitor | Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 m Ω –200 m Ω | – | 1 | 2.2 | μF |
| Operating temperature | Junction temperature | –40 | 50 | 125 | $^{\circ}C$ |

a. Output current is measured at 125 $^{\circ}C$ junction temperature.

b. Leakage current is measured by 85 $^{\circ}C$ junction temperature.

c. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

10.3 LNLDO

Table 12. LNLDO Specifications

| Specification | Notes | Min | Typ | Max | Units |
|-----------------------------------|---|------|------|-------|-----------|
| Input supply voltage (V_{in}) | Min = $1.2V_o + 0.1V = 1.3V$ Dropout voltage requirement must be met under maximum load. | 1.3 | 1.35 | 1.5 | V |
| Output Current | – | – | – | 100 | mA |
| Output voltage (V_o) | Programmable in 25 mV steps. Default = 1.2V | 1.1 | 1.2 | 1.275 | V |
| Dropout Voltage | At maximum load | – | – | 100 | mV |
| Output voltage DC accuracy | includes line/load regulation | –4 | – | +4 | % |
| Quiescent current | No load | – | 44 | – | μA |
| Line regulation | V_{in} from ($V_o + 0.1V$) to 1.5V, maximum load | –0.3 | – | +0.3 | $\%V_o/V$ |

Table 12. LNLDO Specifications

| Specification | Notes | Min | Typ | Max | Units |
|---|---|-------------------|------|----------|----------------------|
| Load regulation | Load from 1 mA to 300 mA | – | 0.02 | 0.05 | %V _o /mA |
| Transient undershoot | – | – | – | TBD | mV |
| Transient overshoot | – | – | – | TBD | mV |
| Leakage current | Power-down | – | – | 10 | μA |
| Output noise | @30 kHz, 60 mA load C _o = 1 μF @100 kHz, 60 mA load C _o = 1 μF | – | – | 60 30 | nV/rt Hz nV/rt Hz |
| PSRR | @ 1kHz, Input > 1.3V, C _o = 1 μF, V _o = 1.2V | 20 | – | – | dB |
| PMU start-up time | From power-down | – | – | 850 | μs |
| LDO Turn-on Time | LDO turn-on time when rest of chip is up | – | – | 180 | μs |
| In-rush current during turn-on | Measured when the output capacitor is fully discharged. | – | – | 150 | mA |
| External output capacitor (C _o) | Total ESR (trace/capacitor): 30 mΩ–200 mΩ | 0.74 ^a | 1 | 2.2 | μF |
| External input capacitor | Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ | – | 1 | 2.2 | μF |
| Operating temperature | Junction temperature | –40 | 50 | 125 | °C |

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

11. WLAN Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

11.1 2.4 GHz Band General RF Specifications

Table 13. 2.4 GHz Band General RF Specifications

| Item | Condition | Minimum | Typical | Maximum | Unit |
|-------------------|------------------------|---------|---------|---------|------|
| TX/RX switch time | Including TX ramp down | – | 5 | 10 | μs |
| RX/TX switch time | Including TX ramp up | – | 5 | 5 | μs |

11.2 2.4 GHz Band Receiver RF Specifications

The receiver specifications including sensitivity are shown in [Table 14](#) and [Table 15 on page 28](#).

Table 14. 2.4 GHz Band Receiver RF Specifications

| Characteristic | Condition | Minimum | Typical | Maximum | Unit |
|--|--|---------|---------|---------|------|
| Cascaded noise figure | – | – | 4 | – | dB |
| Maximum receive level ^a | @ 1, 2 Mbps | –4 | – | – | dBm |
| | @ 5.5, 11 Mbps | –10 | – | – | dBm |
| | @ 54 Mbps | –10 | – | – | dBm |
| Adjacent channel power rejection • DSSS at 11 Mbps ^b | RX = –70 dBm | 35 | – | – | dB |
| Return loss | Z _o = 50Ω, across dynamic range | TBD | TBD | TBD | dB |
| Maximum receiver gain | – | – | >90 | – | dB |

a. When using a suitable external RF switch.

b. Difference between interfering and desired signal (>25 MHz apart) at 8% PER for 1024-octet Physical-Layer Service Data Units (PSDUs) with desired signal level as specified.

Table 15. 2.4 GHz Receiver Sensitivity

| Rate/Modulation | Typical Receive Sensitivity ^{a b} (dBm) |
|-----------------------|--|
| 1 Mbps DSSS | –97 |
| 2 Mbps DSSS | –95 |
| 5.5 Mbps CCK | –91 |
| 11 Mbps CCK | –89 |
| 6 Mbps OFDM | –91 |
| 9 Mbps OFDM | –90 |
| 12 Mbps OFDM | –88 |
| 18 Mbps OFDM | –86 |
| 24 Mbps OFDM | –84 |
| 36 Mbps OFDM | –81 |
| 48 Mbps OFDM | –78 |
| 54 Mbps OFDM | –76 |
| MCS0 (20 MHz channel) | –91 |
| MCS1 (20 MHz channel) | –88 |

Table 15. 2.4 GHz Receiver Sensitivity

| Rate/Modulation | Typical Receive Sensitivity ^{a b} (dBm) |
|-----------------------|--|
| MCS2 (20 MHz channel) | -86 |
| MCS3 (20 MHz channel) | -83 |
| MCS4 (20 MHz channel) | -81 |
| MCS5 (20 MHz channel) | -77 |
| MCS6 (20 MHz channel) | -75 |
| MCS7 (20 MHz channel) | -73 |
| MCS0 (40 MHz channel) | -90 |
| MCS1 (40 MHz channel) | -86 |
| MCS2 (40 MHz channel) | -84 |
| MCS3 (40 MHz channel) | -82 |
| MCS4 (40 MHz channel) | -78 |
| MCS5 (40 MHz channel) | -74 |
| MCS6 (40 MHz channel) | -72 |
| MCS7 (40 MHz channel) | -70 |

- a. Values are measured at the input of the CYW43143. Thus, they include insertion losses from the integrated baluns and integrated T/R switches, but exclude losses from the external circuits. For the 1, 2, 5.5, and 11 Mbps rates, sensitivity is defined as an 8% packet error rate (PER) for 1000-octet PSDUs. For 11g rates (6 Mbps OFDM up to 54 MBps OFDM), sensitivity is defined as a 10% packet error rate (PER) for 1000-octet PSDUs. For 11n rates (MCS0 to MCS7), sensitivity numbers are provide for 10% PER and 4000byte packets.
- b. Sensitivity levels at Vcc=3.3V±6%; at Vcc=3.3 ±10%, sensitivity levels may be degraded.

11.3 2.4 GHz Band Transmitter RF Specifications

Table 16. 2.4 GHz Band Transmitter RF Specifications

| Characteristic | Condition | Min. | Typ. | Max. | Unit | |
|--|----------------|--|------|------|------|-----|
| RF output frequency range | – | 2400 | – | 2500 | MHz | |
| Chip output power ^a (EVM and ACPR compliant, Vcc=3.3V ±6% ^b) | 20 MHz channel | DSSS/CCK rates 1, 2, 5.5, and 11 Mbit/s | – | – | 21.0 | dBm |
| | | 802.11g rates 6, 9, 12, 18, 24, and 36 Mpps | – | – | 20.0 | |
| | | 802.11g rate 48 Mbps | – | – | 19.0 | |
| | | 802.11g rate 56 Mbps | – | – | 18.0 | |
| | | OFDM rates MCS0-MCS5 | – | – | 20.0 | |
| | | OFDM rate MCS6 | – | – | 19.0 | |
| | | OFDM rate MCS7 | – | – | 18.0 | |
| | 40 MHz channel | OFDM rates MCS0- MCS4 | – | – | 19.5 | |
| | | OFDM rate MCS5 | – | – | 19.0 | |
| | | OFDM rate MCS6 | – | – | 18.0 | |
| | OFDM rate MCS7 | – | – | 17.0 | | |

Table 16. 2.4 GHz Band Transmitter RF Specifications (Cont.)

| Characteristic | Condition | Min. | Typ. | Max. | Unit |
|--|---|------|------|------|-----------------|
| Gain flatness | Maximum gain | – | – | 2 | dB |
| Output IP3 | Maximum gain | – | 37 | – | dBm |
| Output P1dB | – | – | 27 | – | dBm |
| Carrier suppression | – | 15 | – | – | dBr |
| CCK TX spectrum mask @ maximum gain | $f_c - 22 \text{ MHz} < f < f_c - 11 \text{ MHz}$ | – | – | –30 | dBr |
| | $f_c + 11 \text{ MHz} < f < f_c + 22 \text{ MHz}$ | – | – | –30 | dBr |
| | $f < f_c - 22 \text{ MHz}$; and $f > f_c + 22 \text{ MHz}$ | – | – | –50 | dBr |
| OFDM TX spectrum mask (chip output power = 16 dBm) | $f < f_c - 11 \text{ MHz}$ and $f > f_c + 11 \text{ MHz}$ | – | – | –26 | dBc |
| | $f < f_c - 20 \text{ MHz}$ and $f > f_c + 20 \text{ MHz}$ | – | – | –35 | dBr |
| | $f < f_c - 30 \text{ MHz}$ and $f > f_c + 30 \text{ MHz}$ | – | – | –40 | dBr |
| TX modulation accuracy (i.e. EVM) at maximum gain | IEEE 802.11b mode | – | – | 35% | – |
| | IEEE 802.11g mode QAM64 54 Mbps | – | – | 5% | – |
| Gain control step size | – | – | 0.25 | – | dB/step |
| Amplitude balance ^c | DC input | –1 | – | 1 | dB |
| Phase balance | DC input | –1.5 | – | 1.5 | ° |
| Baseband differential input voltage | Shaped pulse | – | 0.6 | – | V _{pp} |
| TX power ramp up | 90% of final power | – | – | 2 | μsec |
| TX power ramp down | 10% of final power | – | – | 2 | μsec |

- a. Power control will back off output power by 1.5 dB ensuring EVM and ACPR limits are always met.
- b. Linear output power at 3.3V ±10% supply voltage may be degraded and EVM/ACPR compliant output power may be lower than listed.
- c. At a 3 MHz offset from the carrier frequency.

11.4 2.4 GHz Band Local Oscillator Specifications

Table 17. 2.4 GHz Band Local Oscillator Specifications

| Characteristic | Condition | Minimum | Typical | Maximum | Unit |
|--|-----------|---------|----------------------|---------|--------|
| VCO frequency range | – | 2412 | – | 2484 | MHz |
| Reference input frequency range | – | – | Various ^a | – | MHz |
| Reference spurs | – | – | – | –34 | dBc |
| Local oscillator phase noise, single-sided from 1–300 kHz offset | – | – | – | –86.5 | dBc/Hz |
| Clock frequency tolerance | – | – | – | ±20 | ppm |

- a. Reference supported frequencies range from 12 MHz to 52 MHz.

12. Antenna Specifications

12.1 Voltage Standing Wave Ratio

The Voltage Standing Wave Ratio (VSWR) into the antenna should be less than 2.5:1.

13. Timing Characteristics

13.1 Power Sequence Timing

The recommended power-up sequence is to bring up the power supplies in the order of the rated voltage. This power-up sequence minimizes the possibility of a latchup condition.

In the case of a 3.3V supply (see [Figure 1](#)), the 3.3V supplied to SR_VDDBAT5V, WRF_PA_VDD3P3, WRF_PAD_VDD3P3, USB_A_VDD3P3, and VDDIO can ramp at the same time.

In the case of a 5V supply (see [Figure 2 on page 32](#)), the 5V first ramps on SR_VDDBAT5V, followed by bring-up of the 3.3V supply to WRF_PA_VDD3P3, WRF_PAD_VDD3P3, USB_AVDD3P3, and VDDIO. The power-up timing parameters for both configurations are shown in [Table 18 on page 33](#).

Figure 1. Power-Up Sequence Timing—3V Supply

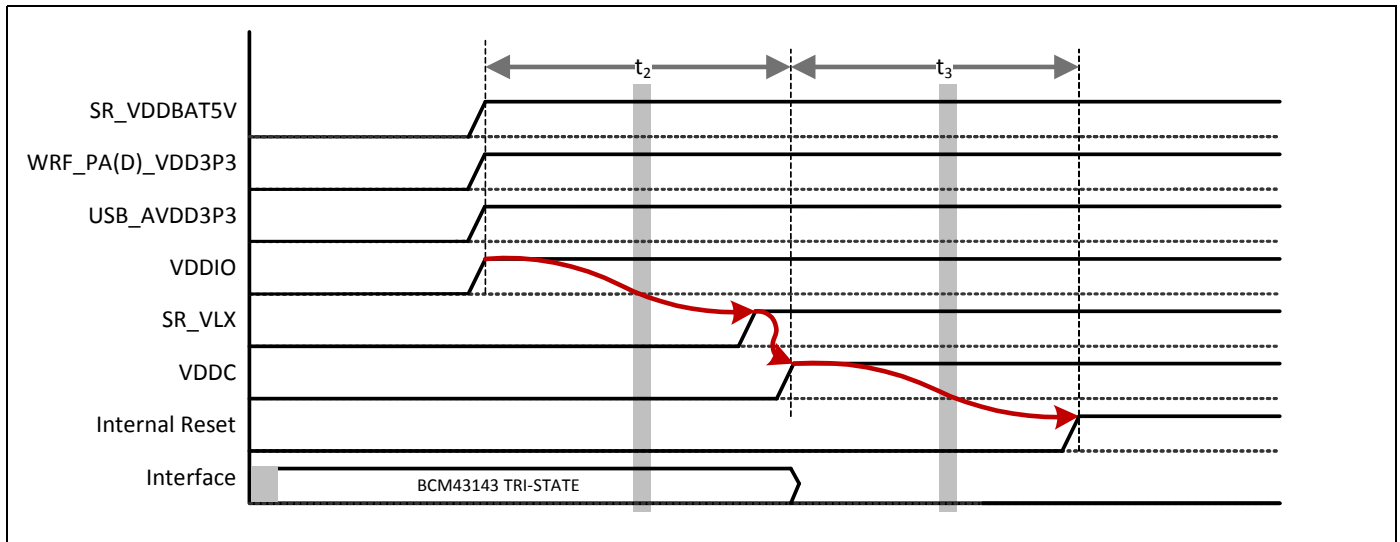


Figure 2. Power-Up Sequence Timing—5V Supply with External DC-DC Conversion

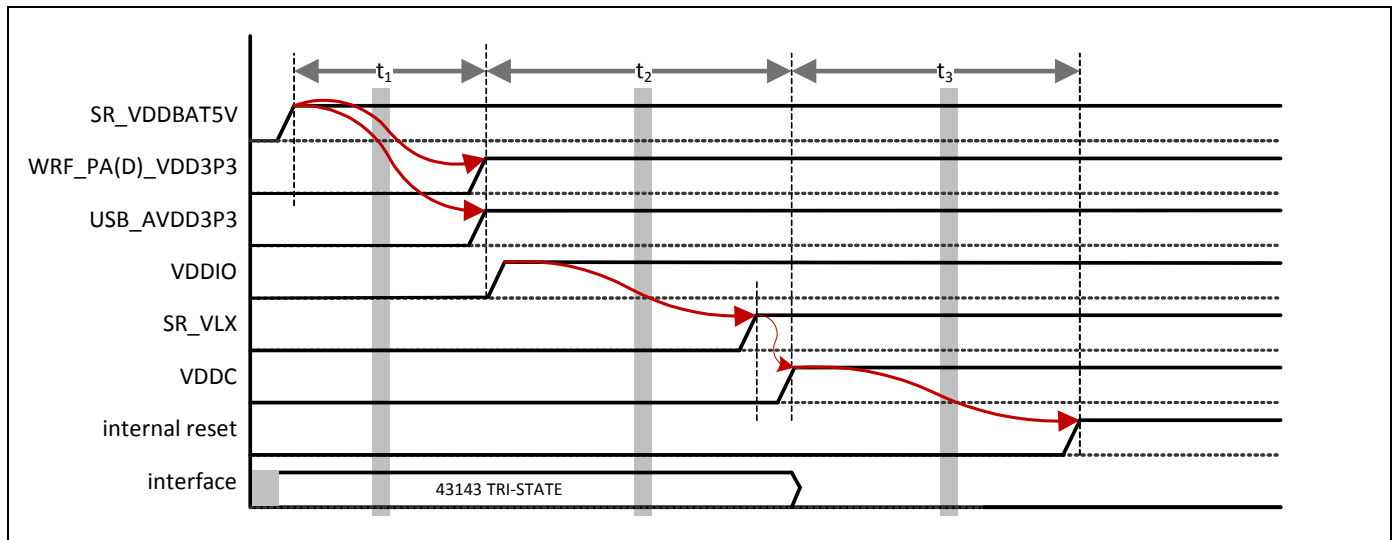


Table 18. Power-Up Timing Parameters

| Symbol | Description | Minimum | Typical | Maximum | Unit |
|--------|---|----------------|-----------------|---------|---------|
| t_1 | SR_VDDBAT5V to 3P3 active | 0 ^a | 50 ^b | – | μ s |
| t_2 | Time from VDDIO rising edge to VDDC reaching 1.2V | – | – | 850 | μ s |
| t_3 | Time from VDDC reaching 1.2V to internal reset deactivation | 30 | 35 | 50 | ms |

- a. In the case of the 3.3V power supply, $t_1 = 0$ for SR_VDDBAT5V, WRF_PA_VDD3P3, and WRF_PAD_VDD3P3.
- b. In the case of the 5V power supply, SR_VDD_BAT5V is directly connected to 5V, but the connection to WRF_PA_VDD3P3, WRF_PAD_VDD3P3, and VDDIO must be made through a DC-DC converter chip to convert 5V to 3V3. Since the converter chip introduces a delay in the ramp-up time, $t_1 = 50 \mu$ s (nominal). The actual value of t_1 will vary slightly based on the particular DC-DC converter chip used in the design.

13.2 Serial Flash Timing

Figure 3. Serial Flash Timing Diagram (STMicroelectronics-Compatible)

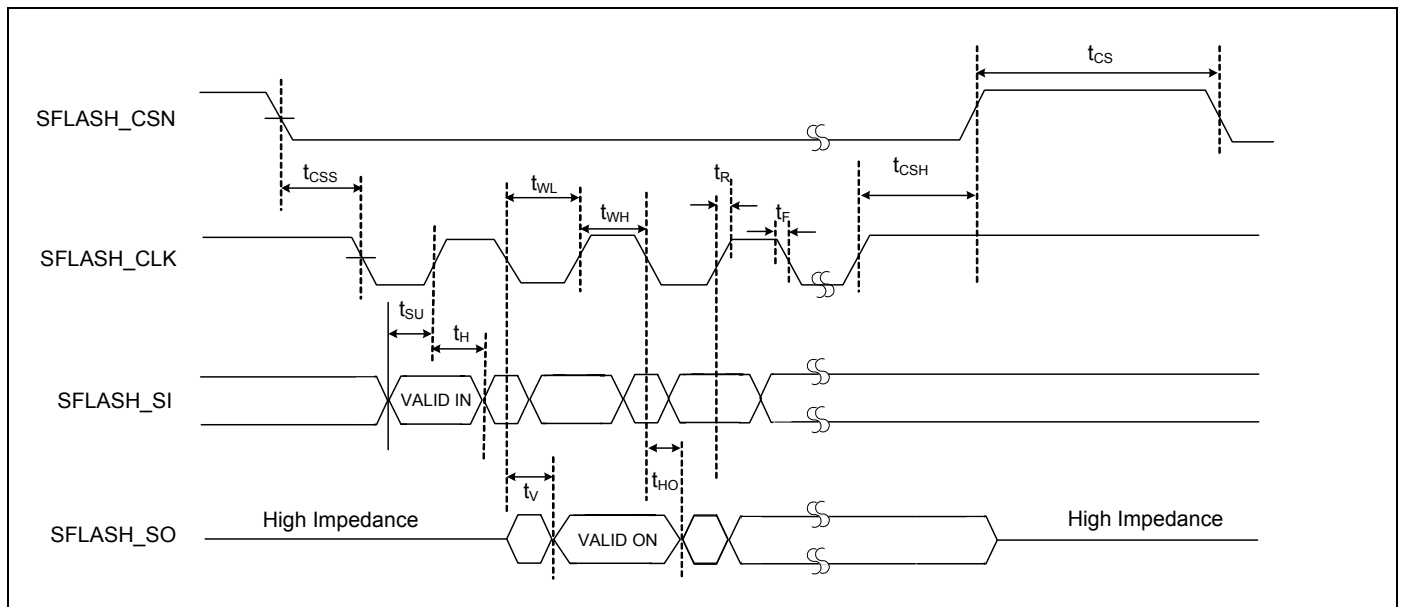


Table 19. Serial Flash Timing

| Parameter | Descriptions | Minimum | Typical | Maximum | Units |
|--------------|--|---------|---------|---------|-------|
| f_{SCK} | Serial flash clock frequency | – | 12.5 | 49.2 | MHz |
| t_{WH} | Serial flash clock high time | 9 | – | – | ns |
| t_{WL} | Serial flash clock low time | 9 | – | – | ns |
| t_R, t_F^a | Clock rise and fall times ^b | TBD | – | – | V/ns |
| t_{CSS} | Chip select active setup time | 5 | – | – | ns |
| t_{CS} | Chip select deselect time | 100 | – | – | ns |
| t_{CSH} | Chip select hold time | 5 | – | – | ns |
| t_{SU} | Data input setup time | 2 | – | – | ns |
| t_H | Data input hold time | 5 | – | – | ns |
| t_{HO} | Data output hold time | 0 | – | – | ns |
| t_V | Clock low to output valid | – | – | 8 | ns |

- a. t_R and t_F are expressed as a slew-rate.
- b. Peak-to-peak

13.3 I²S Slave Mode Tx Timing

In I²S slave mode, the serial clock (I2S_BITCLK) input speed can vary up to a maximum of 12.288 MHz.

I²S Slave mode timing is illustrated in Figure 4.

Figure 4. I²S Slave Mode Timing

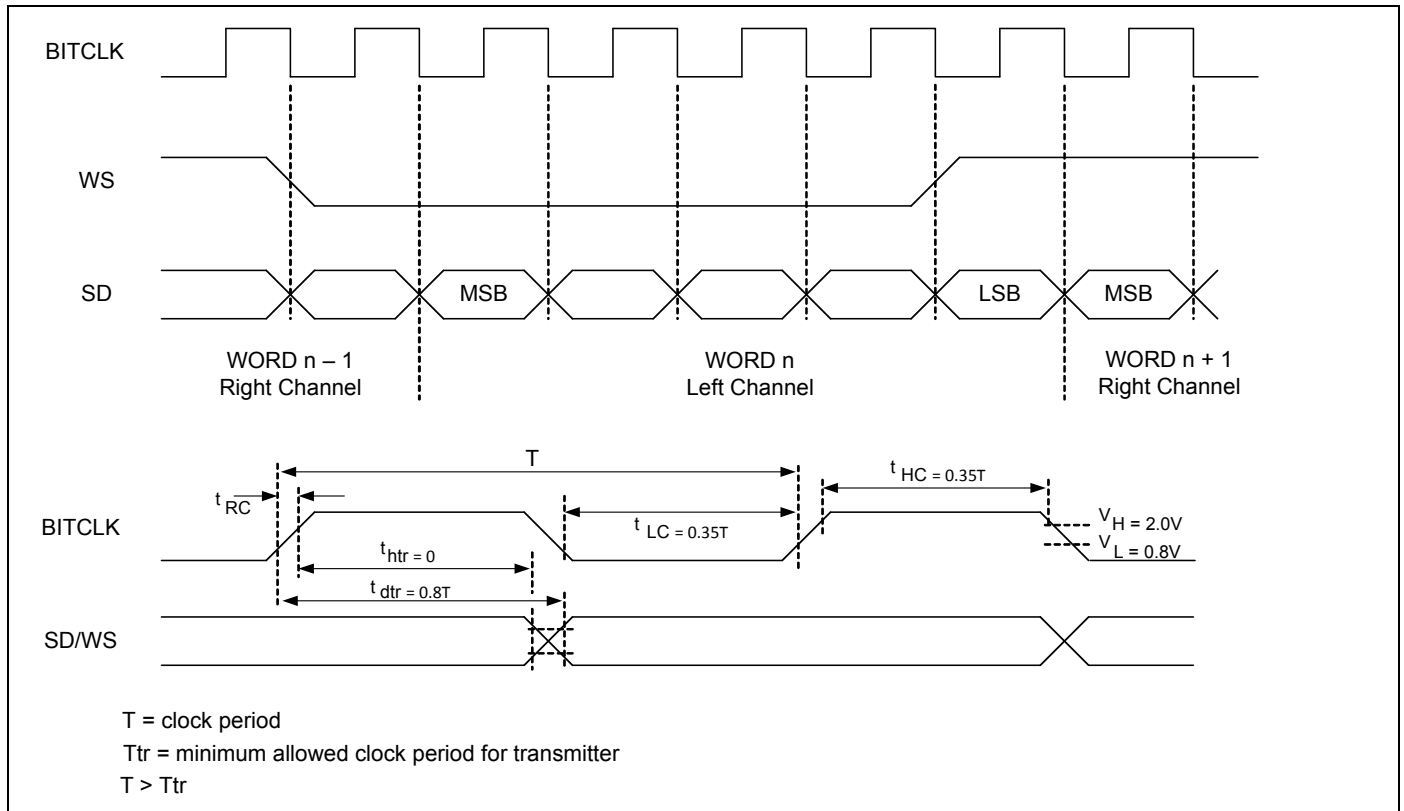


Table 20. Timing for I²S Transmitters and Receivers

| Parameter | Transmitter | | | | Receiver | |
|--|-------------|--------------------------|---------------|---------|-------------|--------------------------|
| | Lower Limit | | Upper Limit | | Lower Limit | |
| | Min | Max | Min | Max | Min | Max |
| Clock period T | T_{tr} | | | | T_{tr} | |
| Slave Mode: Clock accepted by transmitter or receiver: HIGH t_{HC} LOW t_{LC} rise time t_{RC} | | $0.35 T_r$ $0.35 T_r$ | $0.15 T_{tr}$ | | | $0.35 T_r$ $0.35 T_r$ |
| Transmitter: delay t_{dtr} hold time t_{htr} | 0 | | | $0.8 T$ | | |

Table 20. Timing for I²S Transmitters and Receivers

| Parameter | Transmitter | | | | Receiver | |
|--|-------------|-----|-------------|-----|-------------|----------------|
| | Lower Limit | | Upper Limit | | Lower Limit | |
| | Min | Max | Min | Max | Min | Max |
| Receiver: setup time t_{sr} hold time t_{hr} | | | | | | $0.2 T_r$ 0 |

13.4 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 5 and Table 21.

Figure 5. SDIO Bus Timing (Default Mode)

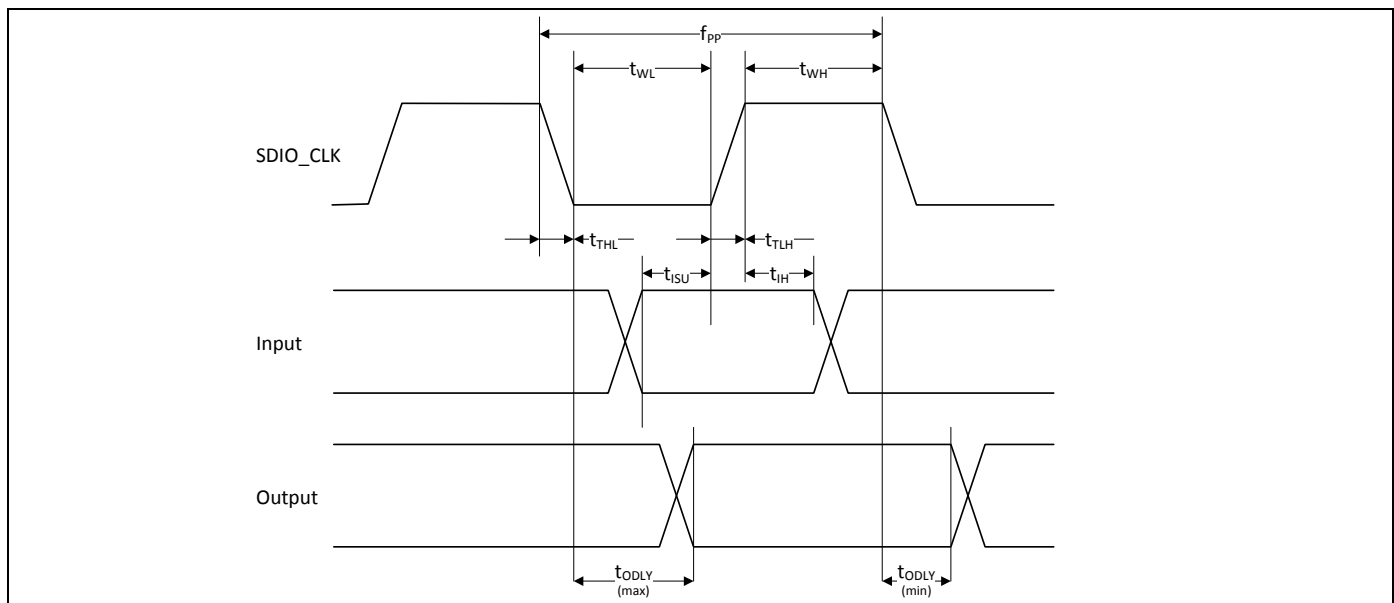


Table 21. SDIO Bus Timing^a Parameters (Default Mode)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|--------|---------|---------|---------|------|
| SDIO CLK (All values are referred to minimum VIH and maximum VIL^b) | | | | | |
| Frequency – data transfer mode | fPP | 0 | – | 25 | MHz |
| Frequency – identification mode | fOD | 0 | – | 400 | kHz |
| Clock low time | tWL | 10 | – | – | ns |
| Clock high time | tWH | 10 | – | – | ns |
| Clock rise time | tTLH | – | – | 10 | ns |
| Clock low time | tTHL | – | – | 10 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup time | tISU | 5 | – | – | ns |
| Input hold time | tIH | 5 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – data transfer mode | tODLY | 0 | – | 14 | ns |
| Output delay time – identification mode | tODLY | 0 | – | 50 | ns |

- a. Timing is based on $CL \leq 40$ pF load on CMD and data.
- b. $\min(V_{ih}) = 0.7 \times VDDIO_SD$ and $\max(V_{il}) = 0.2 \times VDDIO_SD$.

13.5 SDIO High Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 6 and Table 22 on page 36.

Figure 6. SDIO Bus Timing (High-Speed Mode)

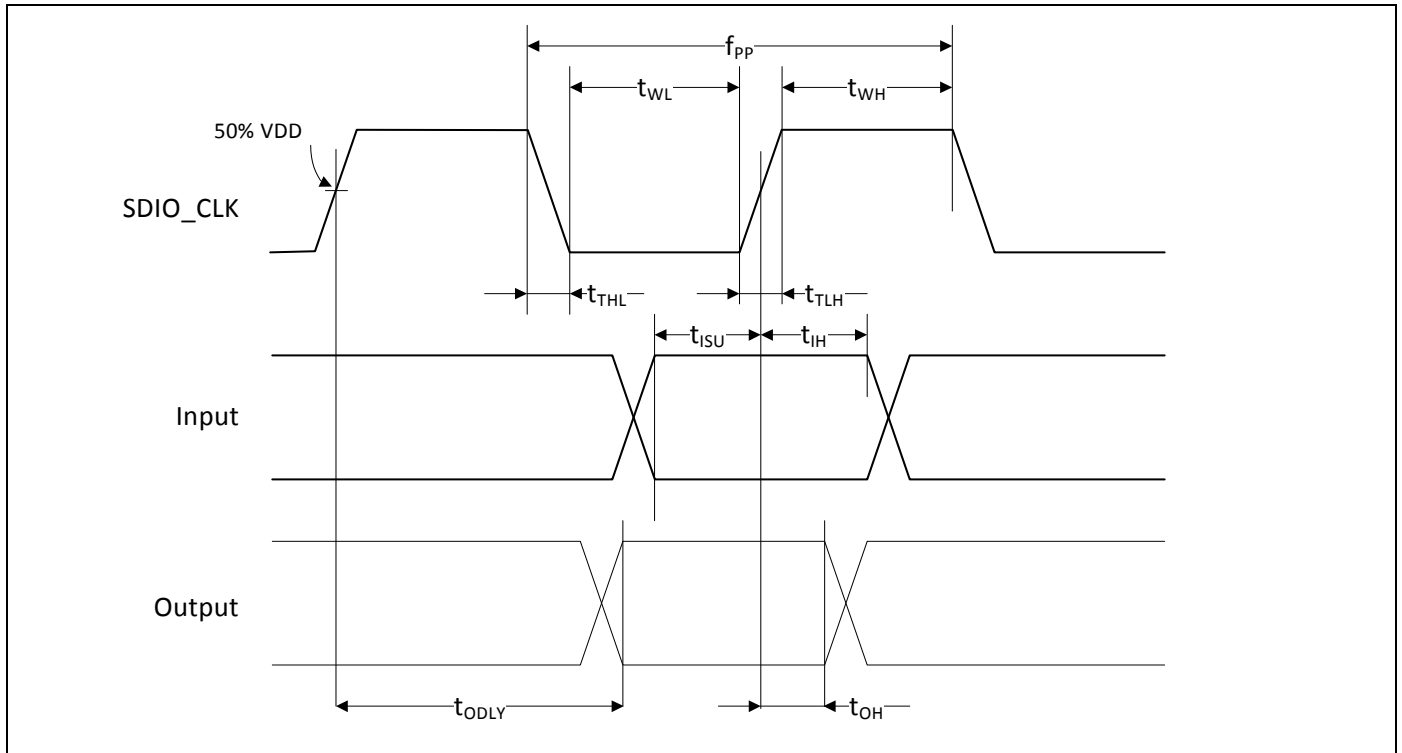


Table 22. SDIO Bus Timing^a Parameters (High-Speed Mode)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|-------------------|---------|---------|-----------------|------|
| SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b) | | | | | |
| Frequency – data transfer mode | f _{PP} | 0 | – | 50 ^c | MHz |
| Frequency – identification mode | f _{OD} | 0 | – | 400 | kHz |
| Clock low time | t _{WL} | 7 | – | – | ns |
| Clock high time | t _{WH} | 7 | – | – | ns |
| Clock rise time | t _{TLH} | – | – | 3 | ns |
| Clock low time | t _{THL} | – | – | 3 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup time | t _{ISU} | 6 | – | – | ns |
| Input hold time | t _{IH} | 2 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – data transfer mode | t _{ODLY} | – | – | 14 | ns |
| Output hold time | t _{OH} | 2.5 | – | – | ns |
| Total system capacitance (each line) | CL | – | – | 40 | pF |

- a. Timing is based on CL ≤40 pF load on CMD and data.
- b. $\min(V_{ih}) = 0.7 \times VDDIO_SD$ and $\max(V_{il}) = 0.2 \times VDDIO_SD$.
- c. 0 - 46 MHz when running at 1.8V.

13.6 USB Parameters

Table 23. USB Parameters

| Parameter | Symbol | Comments | Minimum | Typical | Maximum | Unit |
|--|-----------------------------|---|---------|---------|---------|-------|
| General | | | | | | |
| Baud rate | BPS | – | – | 2.5 | – | Gbaud |
| Reference frequency | Fref | From crystal oscillator | – | 100 | – | MHz |
| Reference clock amplitude | Vref | LVPECL, AC coupled | 1 | – | – | V |
| Receiver | | | | | | |
| Differential termination | ZRX-DIFF-DC | Differential termination | 80 | 100 | 120 | Ω |
| DC impedance | ZRX-DC | DC common-mode impedance | 40 | 50 | 60 | Ω |
| Powered down termination | ZRX-HIGH-IMP-DC | Power-down high impedance (singled ended to ground) | 200k | – | – | Ω |
| Input voltage | VRX-DIFFp-p | AC coupled, differential p-p | 175 | – | 1200 | mV |
| Jitter tolerance | TRX-EYE | Minimum receiver eye width | 0.4 | – | – | UI |
| Differential return loss | RLRX-DIFF | Differential return loss | 12 | – | – | dB |
| Common-mode return loss | RLRX-CM | Common-mode return loss | 11 | – | – | dB |
| Unexpected electrical idle enter detect threshold integration time | TRX-IDEL-DET-DIFF-ENTERTIME | An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition. | – | – | 10 | ms |
| Signal detect threshold | VRX-IDLE-DET-DIFFp-p | Electrical idle detect threshold | 65 | – | 175 | mV |
| Transmitter | | | | | | |
| Output voltage | VTX-DIFFp-p | Differential p-p, programmable in 16 steps | 0 | – | 1200 | mV |
| Output voltage rise time | VTX-RISE | 20% to 80% | 0.125 | – | – | UI |
| Output voltage fall time | VTX-FALL | 80% to 20% | 0.125 | – | – | UI |
| De-emphasis (a1) | VTX-DE-RATIO | Programmable in 16 steps | 0 | – | 40 | % |
| RX detection voltage swing | VTX-RCV-DETECT | The amount of voltage change allowed during receiver detection. | – | – | 600 | mV |
| AC peak common-mode voltage | VTX-CM-Acp | AC peak common-mode ripple | – | – | 20 | mV |
| Absolute delta of DC common-mode voltage during L0 and electrical idle | VTX-CM-DC-ACTIVE-IDLE-DELTA | Absolute delta of DC common-mode voltage during L0 and electrical idle. | 0 | – | 100 | mV |

Table 23. USB Parameters (Cont.)

| Parameter | Symbol | Comments | Minimum | Typical | Maximum | Unit |
|--|----------------------|--|---------|---------|---------|----------|
| Absolute delta of DC common-mode voltage between D+ and D- | VTX-CM-DC-LINE-DELTA | DC offset between D+ and D- | 0 | – | 25 | mV |
| Electrical idle differential peak output voltage | VTX-IDLE-DIFFp | Peak-to-peak voltage | 0 | – | 20 | mV |
| TX short circuit current | ITX-SHORT | Current limit when TX output is shorted to ground. | – | – | 90 | mA |
| Differential termination | ZTX-DIFF-DC | Differential termination | 80 | 100 | 120 | Ω |
| Differential return loss | RLTX-DIFF | Differential return loss | 8 | – | – | dB |
| Common-mode return loss | RLTX-CM | Common-mode return loss | 8 | – | – | dB |
| TX eye width | TTX-EYE | Minimum TX eye width | 0.7 | – | – | UI |

14. Thermal Information

Table 24. 56-pin QFN Thermal Characteristics^a

| Air Velocity m/s | Power W | T _{J_MAX} °C | T _t °C | θ _{JA} , °C/W | Ψ _{JT} °C/W |
|------------------|---------|-----------------------|-------------------|------------------------|----------------------|
| 0 | 1.166 | 110.3 | 105.2 | 37.95 | 4.37 |

a. 1s1P JEDEC board, package only, no heat sink, TA = 65°C. P = 1.061W (PA on).

Note:

- Ambient air temperature is 1 mm above the heat shield on top of the chip.
- Ambient air temperature: TA = 65°C, subject to absolute junction maximum temperature at 125°C.
- The CYW43143 is designed and rated for operation at a maximum junction temperature not to exceed 125°C.

14.1 Junction Temperature Estimation and Ψ_{JT} Versus θ_{JC}

Package thermal characterization parameter Psi-J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

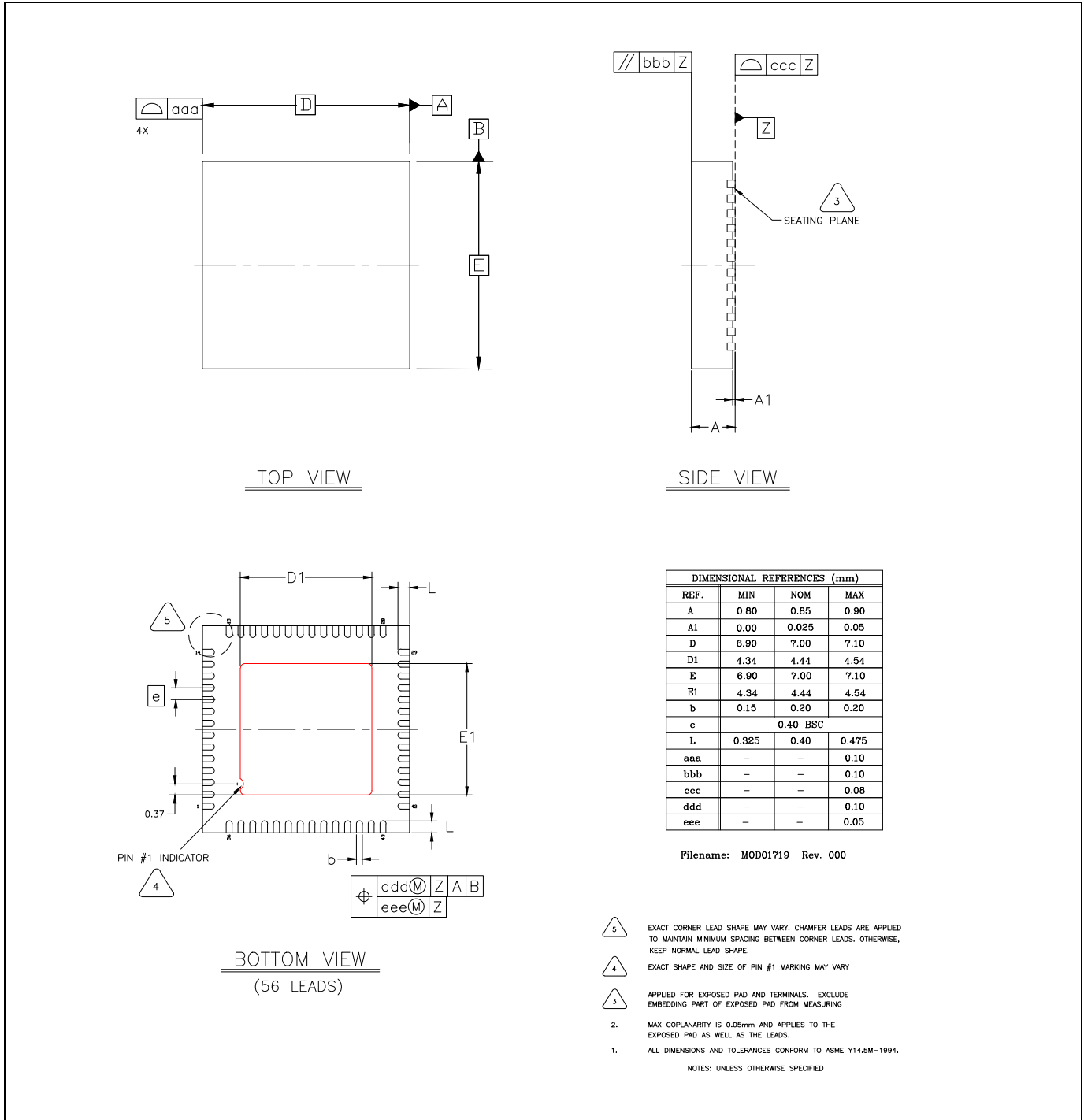
$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

15. Package Information

Figure 7. 7 mm × 7 mm, 56-pin QFN package



16. Ordering Information

Table 25. Ordering Information

| Part Number | Package | Ambient Temperature |
|--------------|--|-------------------------|
| BCM43143KMLG | 7 mm × 7 mm, 56-pin QFN (RoHs compliant) | 0 to 65°C (32 to 149°F) |

Document History

| Document Title: CYW43143 Single-Chip IEEE 802.11b/g/n MAC/PHY/Radio with USB/SDIO Host Interface | | | | |
|--|-----|-----------------|-----------------|--|
| Document Number: 002-15045 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | - | - | 04/26/12 | 43143-DS100-R: Initial release |
| *A | - | - | 06/03/13 | 43143-DS101-R: Added: <ul style="list-style-type: none"> • Various features on cover, reorganized feature lists. • “Link Power Management (LPM) Support” on page 16. • “I2S Interface” on page 17. • “Serial Flash Timing” on page 47. • “I2S Slave Mode Tx Timing” on page 48. • Updated: <ul style="list-style-type: none"> • Figure 1 on page 2. • Figure 3 on page 11. • Figure 4 on page 13. • Note in “Crystal Oscillator” on page 15. • Figure 9 on page 24. • Table 2 on page 25. • Table 3 on page 26. • Table 4 on page 28. • Table 5 on page 32. • Table 6 on page 33. • Table 7 on page 34. • Table 9 on page 36. • Table 10 on page 37. • Table 11 on page 39. • Note in Section 14: “Thermal Information,” on page 56. • Table 24 on page 56 |
| *B | - | - | 06/25/13 | 43143-DS102-R: Updated <ul style="list-style-type: none"> • Table 7 on page 34. |
| *C | - | - | 02/24/14 | 43143-DS103-R: Updated: <ul style="list-style-type: none"> • “Reset and Low-Power Off Mode” on page 12 • Table 6: “Absolute Maximum Ratings,” on page 30 • Table 8: “WLAN Current Consumption in SDIO Mode using SR_VDDBAT5V,” on page 32 • Table 9: “WLAN Current Consumption in USB mode using VDD33,” on page 33 • Table 16: “2.4 GHz Band Transmitter RF Specifications,” on page 40 • Section 14: “Thermal Information,” on page 53 |

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|--|---------|----------|------------|--|
| Document Number: 002-15045 | | | | |
| *D | - | - | 11/14/14 | 43143-DS104-R: Updated: <ul style="list-style-type: none"> Table7:“Guaranteed Operating Conditions and DC Characteristics,” on page32. Table8:“WLAN Current Consumption in SDIO Mode using SR_VDDBAT5V,” on page33. Table9:“WLAN Current Consumption in USB mode using VDD33,” on page34. |
| *E | 5448745 | UTSV | 09/28/2016 | Migrated to Cypress Template |
| *F | 5255423 | AESATMP7 | 04/20/2017 | Updated Cypress Logo and Copyright. |

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