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Ste B101
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(505) 255-9182

Total Ionizing Dose (TID), Radiation Lot Acceptance Test (RLAT) Report for Cypress Semiconductor CYRS15B102 Serial SPI FRAM 2-Mbit (256K X 8)

Date: 3 June 2021 Revision: Original

Purchase Order: Cypress Semiconductor 6400000060

Prepared By: _____ 3 June 2021

T^2 Research Date

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Executive Summary

Radiation Lot Acceptance Testing (RLAT) for Total Ionizing Dose (TID) was performed on 2Mb Cypress Semiconductor CYRS15B102 FRAMs, fab (diffusion) lot 8481131. Irradiation and testing was performed in accordance with MIL-STD 883H Method 1019.8 Condition A. Radiation induced changes were evaluated using KTL statistics with Probability of Survival (Ps) of 99% and Confidence Level of 90%.

"ON-SITE RLAT Tests" were performed before and immediately after the parts were exposed to radiation. These consisted of functional tests as well as DC parametric measurements of standby current (Idd_StdBy) and Deep Power Down current (Idd_DPD). All parameters monitored on-site stayed well within spec sheet limits up to 175K rad(Si)

"PRODUCTION RLAT Tests" were performed pre- and post-irradiation at the subcon assembly/test facility (Micross Components in Orlando, FL). After irradiation and on-site testing the parts were transported to the Micross facility using the TM1019 dry ice procedure.

All devices passed post irradiation On-Site tests as well as the full suite of AC, parametric and functional tests performed on the production tester.

The lot passed RLAT analysis to 175K rad(Si) Testing was performed by Mr. Jake Tausch of JD Instruments.

1.0 PART DESCRIPTION

Total Ionizing Dose (TID) Testing was performed by JD Instruments on one lot of 2Mb QDR FRAMs (CYRS15B102). A total of 8 devices were used for this testing. Seven devices were irradiated and one device was used as control/reference. All parts were serialized by the manufacturer.

These devices have the architecture shown in Figure 1.

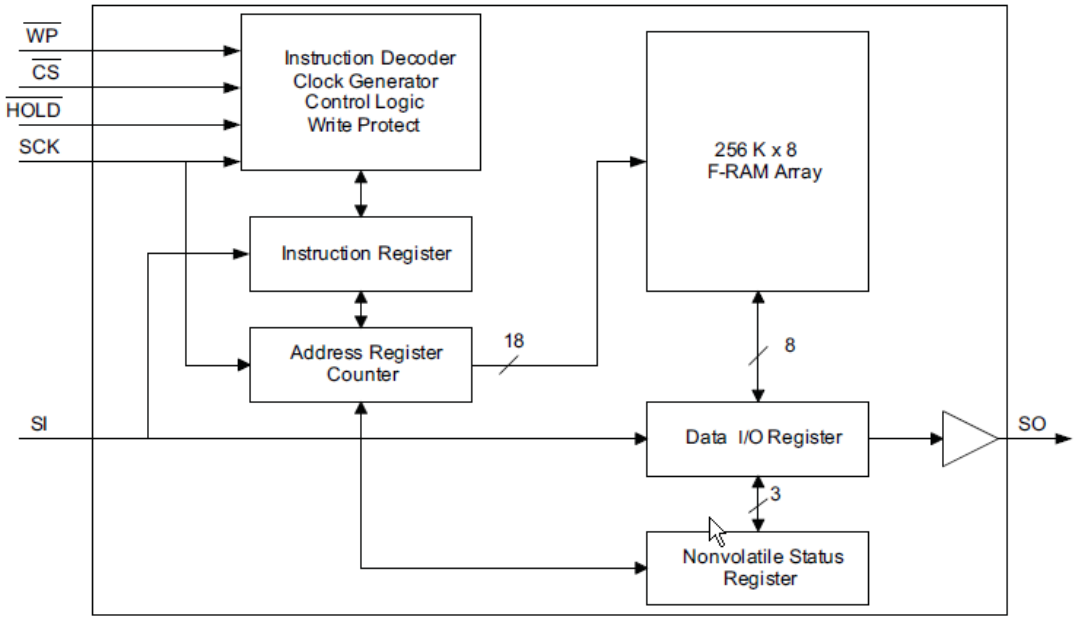

Fig 1. Functional Diagram of CYRS15B102 FRAMs

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Devices were provided in 16 pin Ceramic SOP packages with the pinout shown in Figure 2.

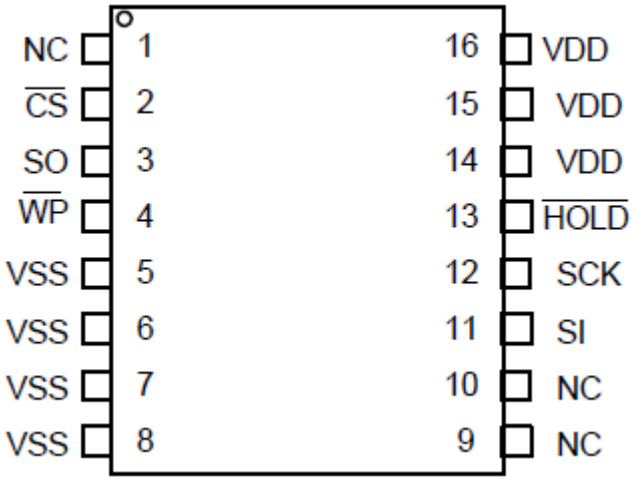

Figure 2. DUT PinOut

2.0 TEST DESCRIPTION

A special bias board was designed that held 6 DUTs. A picture of one of the boards is shown in Figure 3. Device sockets were arranged in a 2 X 3 matrix such that the center of the DUTs were contained in a square measuring 1-1/2" x 1-1/2".

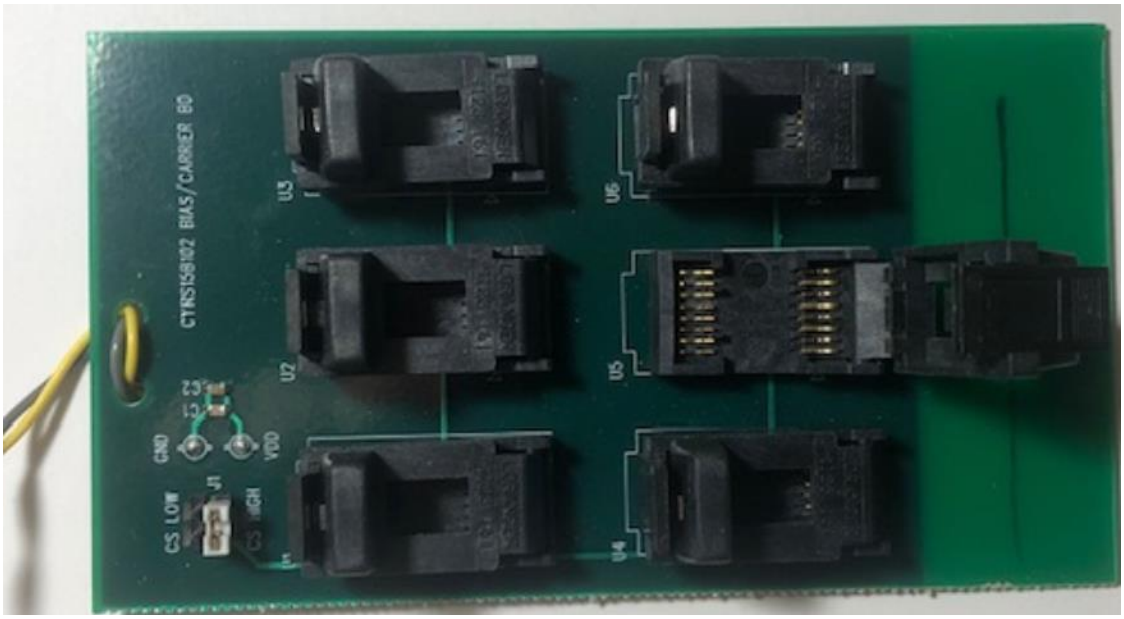

Figure 3. Six Position Bias Board

Parts were tested using a single irradiation to 175K rad(Si). During irradiation parts were biased in a static condition with 3.2V on Vdd, CS*, HOLD* and WP* pins. All other pins were grounded.

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Parts were installed into 2 bias-boards and placed in lead-aluminum boxes. These boxes were placed around the shroud that surrounds the Co-60 slug at the radiation facility. A generic picture of this arrangement is shown in figure 4.

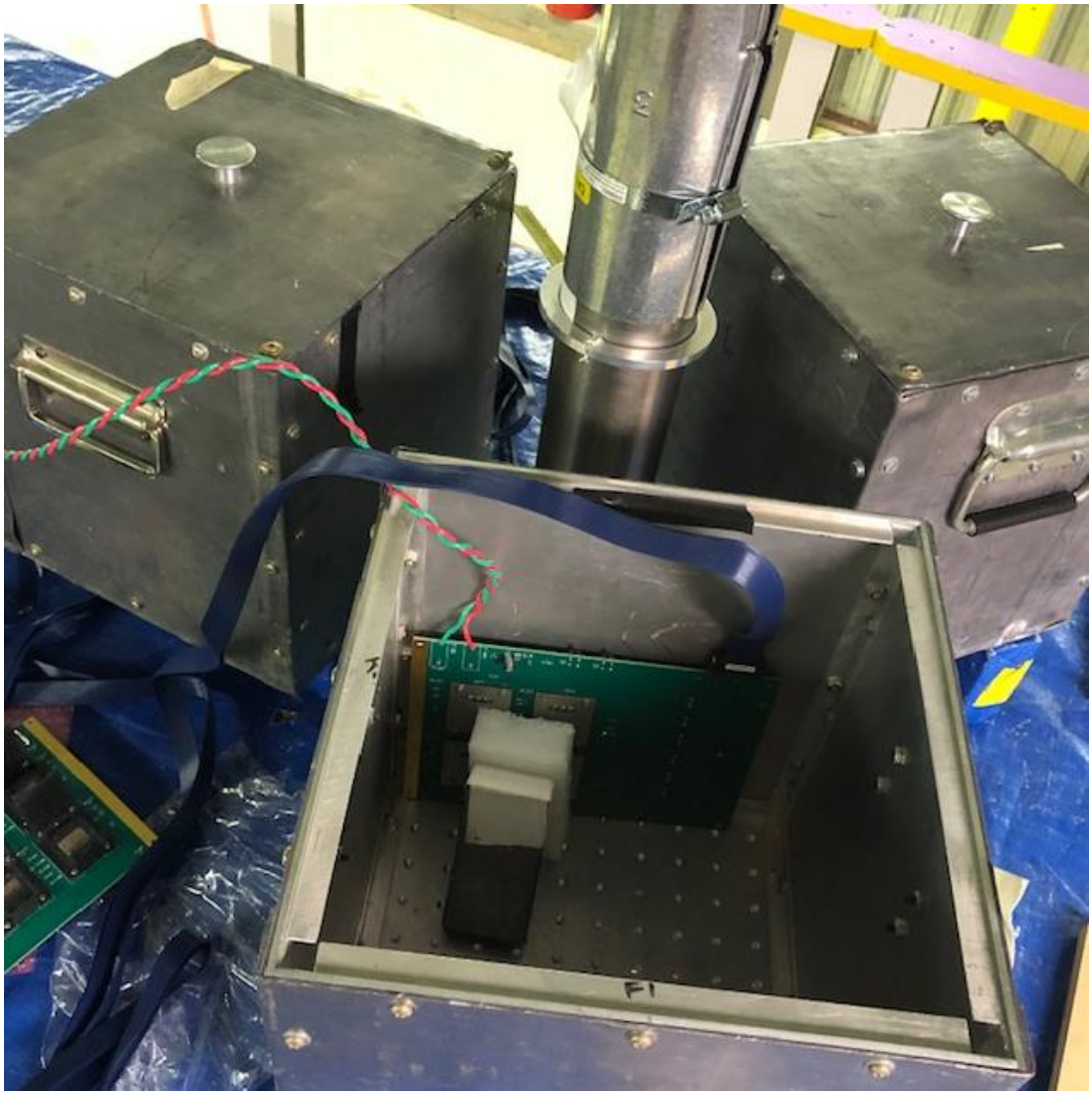

Figure 4. Lead-Aluminum Boxes Surrounding the Co-60 Shroud

These parts were irradiated to 175K rad(Si) using one exposure. Dose rates of 50.8 rad(Si)/sec were measured using a calibrated meter as detailed in Attachment A. Measurements indicated less than +/-1% variation in dose rate across the exposure pattern.

2.1 ON-SITE RLAT TESTS

Tests performed on-site at the radiation facility included functional testing and measurements of Idd_StdBy and Idd_DPD.

Irradiations were performed with devices biased to their maximum supply voltage (Vdd = 3.6V). Parametric and functional testing was performed with devices biased to their nominal voltages (Vdd = 3.2V).

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This was considered the worst case combination of bias conditions since more radiation damage will be induced at a higher bias.

The part "traveler" that documented irradiation and test times is shown in Appendix B.

2.2 PRODUCTION RLAT TESTS

The full suite of production tests were performed on these devices both pre- and post-irradiation.

3.0 Lot Acceptance Technique

Parameters were measured and recorded in an excel format spread sheet. The measured values at each radiation step were analyzed using the Radiation Lot Acceptance Test (RLAT) "variables method" (see MIL-HDBK-814, Appendix Section 50, especially Table IXB).

In the RLAT variables method the average (Avg) and standard deviation (Std) of each parameter are calculated for the group of parts being irradiated. A value is then calculated and compared to the part limits using this average and standard deviation along with a one sided tolerance factor, KTL.

For parameters where the limit is higher than measured values the lot is acceptable if

$$Avg + KTL * Std < Limit \qquad \text{(eq. 1)}$$

For parameters where the limit is lower than measured values the lot is acceptable if

$$Avg - KTL * Std > Limit \qquad \text{(eq. 2)}$$

Values for KTL vary depending on sample size, Probability of Survival (Ps) and confidence level. For this test, with a radiation sample size of 7, Ps of 0.99 and a confidence level of 0.9, the value for KTL was 3.972 (MIL-HDBK-814, Table IXB).

4.0 ON-SITE RLAT Analysis Results

4.1 Functional Testing

FRAM memory cells have "destructive" READ cycles. This means data stored in a cell is erased as a result of each read. Therefore, FRAM memories are designed so that data is automatically re-written into each cell every time it is read.

With this in mind a special test sequence was devised to evaluate data retention and the ability to write/read after radiation. Specifically, a checkerboard pattern was written into memory before radiation began. After irradiation this pattern was read twice, the first time to see whether data was preserved during radiation and the second time to see whether the automatic re-write was performed successfully. An alternate pattern (All 1's) was then written-to and read-from memory. Finally, the checkerboard pattern was written-to and read-from memory. The exact sequence is shown in Fig 5.

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1. READ (Checkerboard) pattern – Record Errors
2. READ (Checkerboard) pattern – Record Errors
3. WRITE All 1's pattern
4. READ All 1's pattern – Record Errors
5. WRITE Checkerboard pattern
6. READ Checkerboard pattern – Record Errors
7. (Repeat 5/6 above if errors detected in step 6)
8. (Repeat 5/6 above if errors detected in step 7)

Fig 5. FUNCTIONAL TEST SEQUENCE

No memory bits on any device ever failed this test sequence post irradiation. This lot passed functional testing at 175K rad(Si).

4.1 Idd_StdBy

Power supply current was measured with Vdd = 3.2V and parts in static conditions. Figure 6 shows how these currents behaved with radiation.

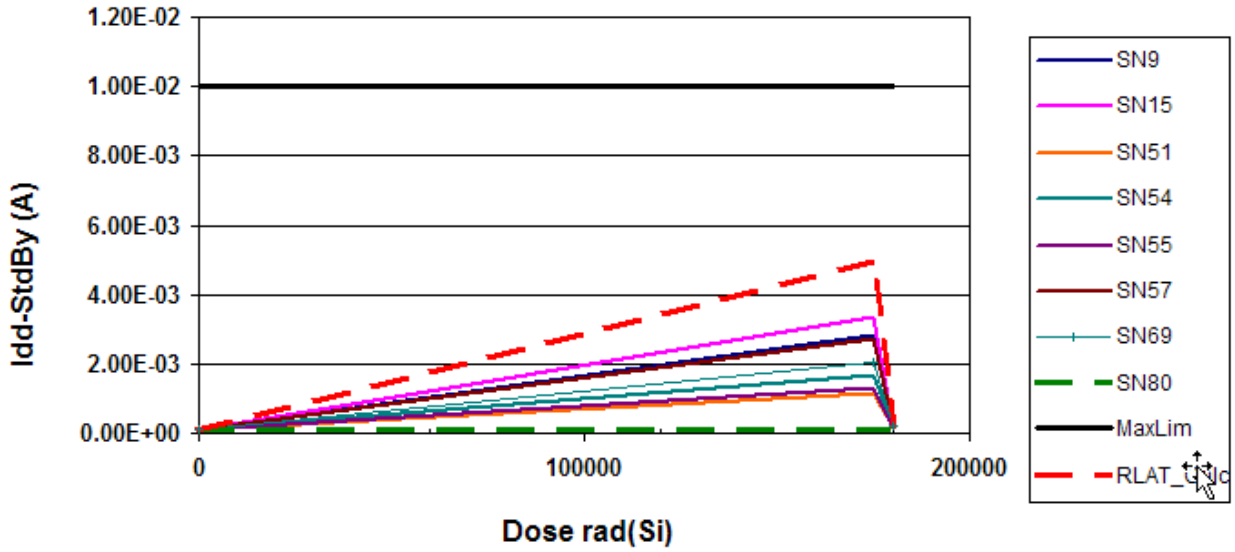

Figure 6. Idd_StdBy

This plot shows results for pre-radiation measurements, measurements immediately after parts were irradiated to 175K rad(Si) and also measurements made 1 week later, after the parts had been shipped to Micross for post-radiation characterization and returned.

In this plot the limit for Idd_StdBy is plotted as a bold, solid black line at 10mA. Measurements made on the reference device (SN80) are plotted as a bold, dashed green line. Individual DUT measurements are plotted as solid lines of various colors as shown in the legend. The RLAT value for these measurements is plotted as a bold, dashed red line. Of special interest is the fact that the RLAT value for this parameter had almost returned to pre-radiation levels after the one week anneal.

This lot of parts passed RLAT analysis for this parameter.

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4.2 Idd_DPD

Idd_DPD is not a parameter with specified limits for radiation environments, but the results of these measurements are shown in Figure 7 for completeness.

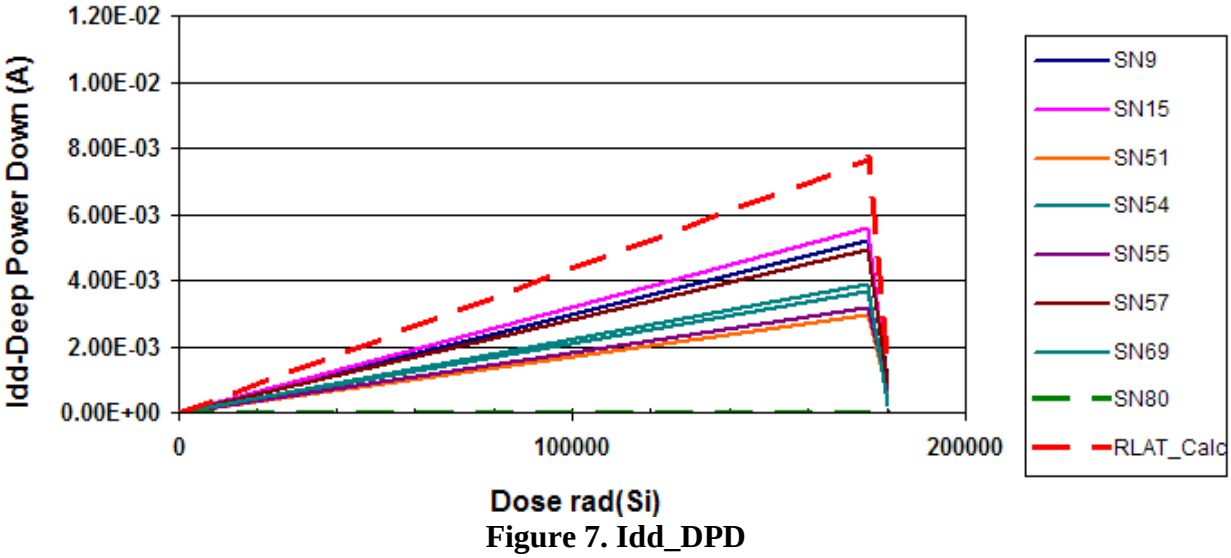

Figure 7. Idd_DPD

5.0 PRODUCTION RLAT Analysis Results

5.1 PRODUCTION AC RESULTS

A full suite of AC tests were performed pre- and post-irradiation on these parts. These tests included many variations of bias conditions, test patterns, reference voltages, threshold voltages for output rise/fall measurements, etc. These were not parametric tests so the result of each test was a simple pass/fail. As shown in Figure 8, all devices passed every AC test post radiation. Therefore this lot of parts passed production limits at 175K rad(Si).

DUT	D/C	Lot	Wafer	SN	Read Config	WPEN_WP_SPI	HOLD_SPI	WREN_WRDI_SPI	StatReg_Check_SPI	TREC_Min_SPI	TPU_Min_SPI	Block_Protect_SPI
1	2041	8481131	18	9	P	P	P	P	P	P	P	P
2	2041	8481131	18	15	P	P	P	P	P	P	P	P
3	2041	8481131	18	51	P	P	P	P	P	P	P	P
4	2041	8481131	18	54	P	P	P	P	P	P	P	P
5	2041	8481131	18	55	P	P	P	P	P	P	P	P
6	2041	8481131	18	57	P	P	P	P	P	P	P	P
7	2041	8481131	18	69	P	P	P	P	P	P	P	P

DUT	D/C	Lot	Wafer	SN	Bounce_Lo_Hi_SPI	Lo_Data_Ret_55_CLDO_SPI	Hi_Data_Ret_55_CLDO_SPI	Internal_Row_NV_SPI	Internal_CKBD_NV_SPI	Final_Read_Solid_00_SPI
1	2041	8481131	18	9	P	P	P	P	P	P
2	2041	8481131	18	15	P	P	P	P	P	P
3	2041	8481131	18	51	P	P	P	P	P	P
4	2041	8481131	18	54	P	P	P	P	P	P
5	2041	8481131	18	55	P	P	P	P	P	P
6	2041	8481131	18	57	P	P	P	P	P	P
7	2041	8481131	18	69	P	P	P	P	P	P

Figure 8. Post Radiation Production AC Test Results

5.2 PRODUCTION RLAT DC RESULTS

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Figure 9 shows the complete set of DC parameters measured on these devices post irradiation along with KTL calculations and limits.

DUT	D/C	Lot	Wafer	SN	IDD_DSMax_SPI	IIH_SB_SPI	IIH_WB_SPI	IIH_D_SPI	IIH_C_SPI	IIH_HOLDB_SPI	IIL_SB_SPI	IIL_WB_SPI
1	2041	8481131	18	9	2.05E-03	4.58E-06	4.20E-06	9.12E-09	2.04E-08	5.76E-06	7.30E-08	8.10E-08
2	2041	8481131	18	15	1.97E-03	7.87E-06	5.18E-06	2.28E-08	1.67E-08	8.41E-06	2.70E-08	1.17E-08
3	2041	8481131	18	51	1.61E-03	2.63E-06	1.82E-06	2.16E-09	1.86E-08	2.48E-06	4.40E-08	1.17E-08
4	2041	8481131	18	54	1.77E-03	3.12E-06	2.90E-06	1.28E-09	1.04E-08	3.18E-06	1.50E-08	2.54E-08
5	2041	8481131	18	55	1.67E-03	3.18E-06	2.17E-06	1.16E-08	1.54E-08	2.82E-06	1.95E-08	2.42E-08
6	2041	8481131	18	57	2.18E-03	6.62E-06	5.82E-06	1.91E-08	2.36E-08	7.42E-06	7.00E-08	2.04E-08
7	2041	8481131	18	69	1.83E-03	4.10E-06	4.37E-06	1.09E-08	9.30E-09	6.51E-06	1.06E-09	1.34E-08
				KTL	2.69E-03	1.24E-05	9.82E-06	4.27E-08	3.69E-08	1.47E-05	1.46E-07	1.24E-07
				MIN	40uA	-10uA	-10uA	-10uA	-10uA	-10uA	-10uA	-10uA
				MAX	10mA	10uA	10uA	10uA	10uA	10uA	10uA	10uA

DUT	D/C	Lot	Wafer	SN	IIL_D_SPI	IIL_C_SPI	IIL_HOLDB_SPI	IOH_Q_SPI	IOL_Q_SPI	VOH1_SPI	VOH2_LV_SPI	VOL1_SPI	VOL2_Max_SPI
1	2041	8481131	18	9	7.70E-09	1.06E-09	7.70E-08	7.70E-08	1.37E-09	2.34E+00	1.96E+00	6.90E-01	5.00E-02
2	2041	8481131	18	15	1.03E-08	1.02E-08	9.00E-08	5.20E-08	3.25E-09	2.34E+00	1.96E+00	6.90E-01	5.00E-02
3	2041	8481131	18	51	4.00E-09	4.40E-10	2.10E-08	2.40E-08	1.10E-09	2.34E+00	1.96E+00	6.80E-01	5.00E-02
4	2041	8481131	18	54	2.87E-09	3.65E-09	5.70E-08	4.50E-08	1.00E-10	2.34E+00	1.96E+00	6.80E-01	5.00E-02
5	2041	8481131	18	55	9.60E-09	1.01E-08	5.80E-08	5.10E-08	7.00E-10	2.34E+00	1.96E+00	6.80E-01	5.00E-02
6	2041	8481131	18	57	9.50E-09	9.50E-09	3.94E-08	5.86E-08	2.60E-09	2.34E+00	1.96E+00	6.80E-01	5.00E-02
7	2041	8481131	18	69	2.10E-09	6.20E-10	2.75E-08	1.00E-07	1.06E-08	2.34E+00	1.96E+00	6.80E-01	5.00E-02
				KTL	2.05E-08	2.36E-08	1.53E-07	1.55E-07	1.71E-08	2.34E+00	1.96E+00	7.02E-01	5.00E-02
				MIN	-10uA	-10uA	-10uA	-10uA	-10uA	2.13V	1.773V	0.54V	0.04V
				MAX	10uA	10uA	10uA	10uA	10uA	3.73V	2.97V	0.94V	0.241V

Figure 9. Post Radiation Production DC Test Results

In these tables the KTL value calculated for each parameter is shown in the yellow highlighted cell. Min and Max limits are printed just below the KTL calculation with the appropriate limit for this comparison highlighted. The green used to highlight the limit cells indicates that the group passed KTL analysis for every parameter.

This lot of parts passed production RLAT analysis after irradiation.

6.0 Conclusions

This fab lot of CYRS15B102 devices passed RLAT analysis to 175K rad(Si) on all parameters after the application of 99/90 KTL statistics.

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Appendix A. Calibration Information

A.1 Test Equipment - Test stimulus and parametric measurements were provided by an Algorithmic Test Vector (ATV) and a Parametric Work Station (PWS), both manufactured by JD Instruments. Both units have calibration traceable to NIST.

A.2 Radiation Source –Calibration letter below.

DEPARTMENT OF THE AIR FORCE
AIR FORCE RESEARCH LABORATORY (AFMC)

MEMORANDUM FOR JD Instruments

FROM: AFRL/RVSE
Bldg 914
3550 Aberdeen Ave SE
Kirtland AFB NM 87117

SUBJECT: Calculating the Dose Rate at the Air Force Research Laboratory Cobalt-60 Irradiator

1. The dose rate for JDI parts was measured and calculated using a calibrated/certified ion chamber. The instrumentation that was used was manufactured by Radcal Corporation, in Monrovia, California. The Control Unit for the ion chamber is a 2026, serial number 26-1626, and an ion chamber used for the measurement was a 20X6-0.18, serial number 32400. Certification records can be provided upon request.

2. The ion chamber was placed from the source where the DUTs (Device Under Test) would be located. The dose rate was measured and corrected for temperature/barometric pressure, probe amplification, and for deposited dose in Silicon. The source is a panoramic irradiator and hosed in a large volume area where back scatter is not possible due to the distances to any interactive materials, however in order to maintain MIL-STD-883 the measurements and tests were attained inside a Pb/Al box.

3. If there are any questions concerning the calculated exposure for this test, please contact the Radiation Safety Officers; Mr. Richard Netzer, AFRL/RVSE at 505-846-6889 (Richard.netzer@kirtland.af.mil) or Mr. William Kemp, SAIC, at 505-314-3542 (William.t.kemp@saic.com).

RICHARD NETZER, GS-12, USAF
Laboratory Manager, EF Section
Space Electronics Branch, AFRL/RVSEF

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Appendix B. Part Traveler

JDI Rad Test Part Traveller - Dry Ice Shipment Option

Customer:	Micross
Part Type:	CYRS15B102Q 2M FRAM
Test Type:	RLAT
Micross Job#:	MO162467
CY Fab Lot#:	8481131

DUT	D/C	Lot	Wafer	SN	Received Date	PreRad Char	TID Test					Remote Facility				
							Time					Unpack			Finish Test	
							Date	Start Rad	Stop Rad	Last Test	Package	Temp °C	Date	Time	Temp °C	Date	Time
1	2041	8481131	18	9	5/18/2021	5/24/2021	5/26/2021	13:26	14:23	14:34	14:47	-79	5/27/2021	9:20	-72.5	5/27/2021	9:37
2	2041	8481131	18	15	5/18/2021	5/24/2021	5/26/2021	13:26	14:23	14:32	14:47	-79	5/27/2021	9:20	-72.5	5/27/2021	9:39
3	2041	8481131	18	51	5/18/2021	5/24/2021	5/26/2021	13:26	14:23	14:43	14:47	-79	5/27/2021	9:20	-72.5	5/27/2021	9:43
4	2041	8481131	18	54	5/18/2021	5/24/2021	5/26/2021	13:26	14:23	14:42	14:47	-79	5/27/2021	9:20	-72.5	5/27/2021	9:45
5	2041	8481131	18	55	5/18/2021	5/24/2021	5/26/2021	13:26	14:23	14:40	14:47	-79	5/27/2021	9:20	-72.5	5/27/2021	9:47
6	2041	8481131	18	57	5/18/2021	5/24/2021	5/26/2021	13:26	14:23	14:45	14:47	-79	5/27/2021	9:20	-72.5	5/27/2021	9:54
7	2041	8481131	18	69	5/18/2021	5/24/2021	5/26/2021	13:26	14:23	14:44	14:47	-79	5/27/2021	9:20	-72.5	5/27/2021	9:20

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