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Heavy Ion, Single Event Effects (SEE) Final Report for Cypress Semiconductor CYRS15B102 Serial SPI FRAM 2-Mbit (256K X 8)

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1.0 Test Overview

Heavy ion radiation testing was performed on July 31-Aug 1, 2021 at the Texas A&M Cyclotron facility (TAMU). The purpose of this testing was to determine the FRAM and SEFI upset rates in these devices and whether latchup occurred when they were exposed to heavy ion radiation.

These parts were provided in 16 pin Ceramic SOP packages. Lids of the devices were removed and taped on to allow exposure of bare die for SEE testing.

The memory elements in these devices are ferroelectric storage cells that retain their information even when power is removed. Therefore they are a type of non-volatile memory. Classic memory upset testing consists of loading a pattern into memory, irradiating to some fluence and then reading the stored pattern. Any random upsets will then show how sensitive the storage cells are to heavy ion radiation. This type of test was performed on these devices with results showing the ferroelectric cells are extremely resistant to heavy ion radiation.

On the other hand, the process of reading information stored in a ferroelectric cell erases its contents. Therefore, internal to the part, a functional "read" of memory actually consists of a "read" and an immediate "re-write". This read/re-write process involves CMOS analog and digital circuitry which is, itself, sensitive to heavy ion strikes. Thus the act of reading memory in a heavy ion environment introduces a secondary way that stored information can be corrupted. Tests were included to measure upsets caused in this manner.

It should also be noted that these are serial parts so there were only 6 I/O pins. Operations were performed on the part by shifting information into/out-of the DUT on an 8 bit (1 byte) basis. For instance, a READ operation was performed by pulling the DUT chip-select (CS*) pin low and shifting in a 1 byte "READ" command followed by 3 bytes of starting address. Information from the desired address would then be shifted out of the device on succeeding clocks. As long as the CS* pin was held low an internal address counter would automatically increment thru memory and information from the memory would continue to be shifted out. Thus, the device would perform an "extended READ" where all memory contents could be read with one READ command. This extended read operation is of special importance since this is how boot memory is loaded into FPGAs.

This was a qualification test using multiple devices from one manufacturing lot to verify similar behavior across all devices.

Upset testing was performed at room temperature with Vdd = 2.0V. Latchup testing was performed with Vdd = 3.6V and at various temperatures up to 126^0C.

No parts ever latched, even when exposed to 1E7 ions/cm^2 at 115^0C with ions having an LET of 114.4 Mev*cm^2/mg. One device latched when exposed at 125^0C.

Memory storage bits in this technology (ferro-electric) are very resistant to heavy ion radiation. All errors were caused by functional failures in the CMOS control circuitry. A technique was identified that would clear upsets in CMOS logic before a READ operation

2.0 Test Procedure

Three types of functional tests were performed on these parts:

1) Memory was loaded with a pattern, the part irradiated to some fluence, and the pattern read out of the part to see how many bits had been upset. In the run log these tests were labeled, "StdBy-Rad-Read".
2) Memory was loaded with a pattern and the part was irradiated to some fluence. Then operations were performed on the part prior to reading to see if upsets could be cleared from the CMOS circuitry. Two techniques were used:
    a. Power cycle the part before reading. CMOS circuitry is completely initialized every time power is applied. In the run log these tests were labeled, "StdBy-Rad-PwrCyc/Read".
    b. Program the part into Deep Power Down (DPD) and then back to normal StandBy before reading. Most CMOS circuitry is powered down in DPD mode and CMOS circuitry is initialized when returning to normal StandBy. The question was whether this initialization was as complete as when power is first applied. In the run log these tests were labeled, "StdBy-Rad_Sleep/Wake/Read".
3) Memory was loaded with a pattern and continuously read while being irradiated. Reads of memory are destructive for this technology so a repeated read was actually a read/write operation at the cell level. In the run log these tests were labeled, "Continuous READ CB".

Idd was continuously monitored to see if supply current to the part ever changed.

Figure 1 shows the block diagram for this part.

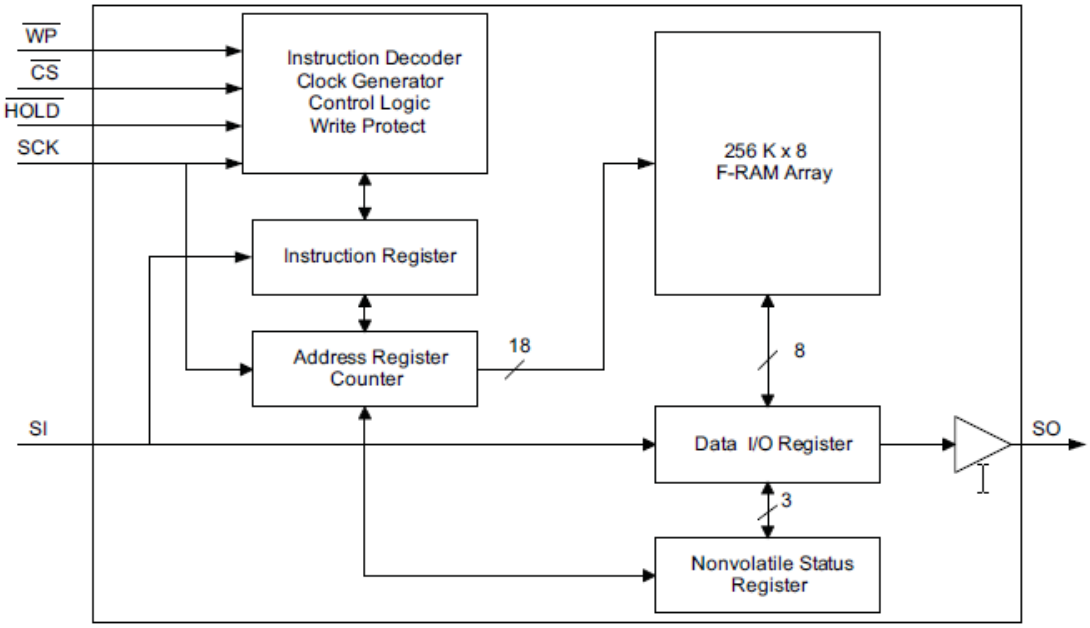

Figure 1. Cypress CYRS15B102, 2Mb FRAM

Parts were provided in 16 pin ceramic SOC packages with pinout as shown in Figure 2.

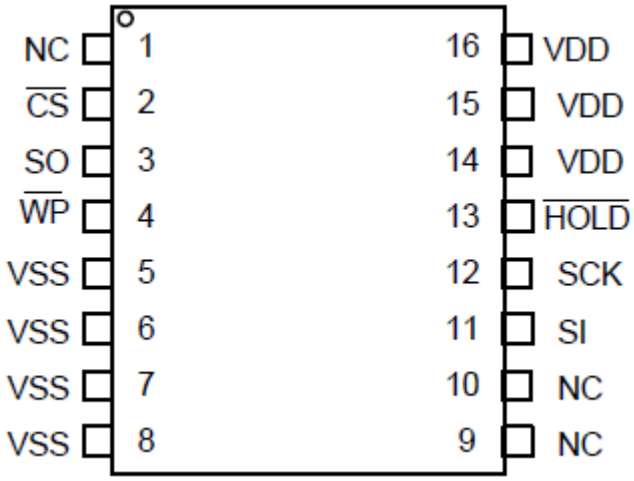

Figure 2. 16 Pin Ceramic SOC Package and PinOut for CYRS15B102, 2Mb FRAM

DUTs were mounted on small carrier cards for ease of handling and inserted into sockets on the test card. The DUT was heated by installing a heater strip underneath the DUT as shown in Figure 3.

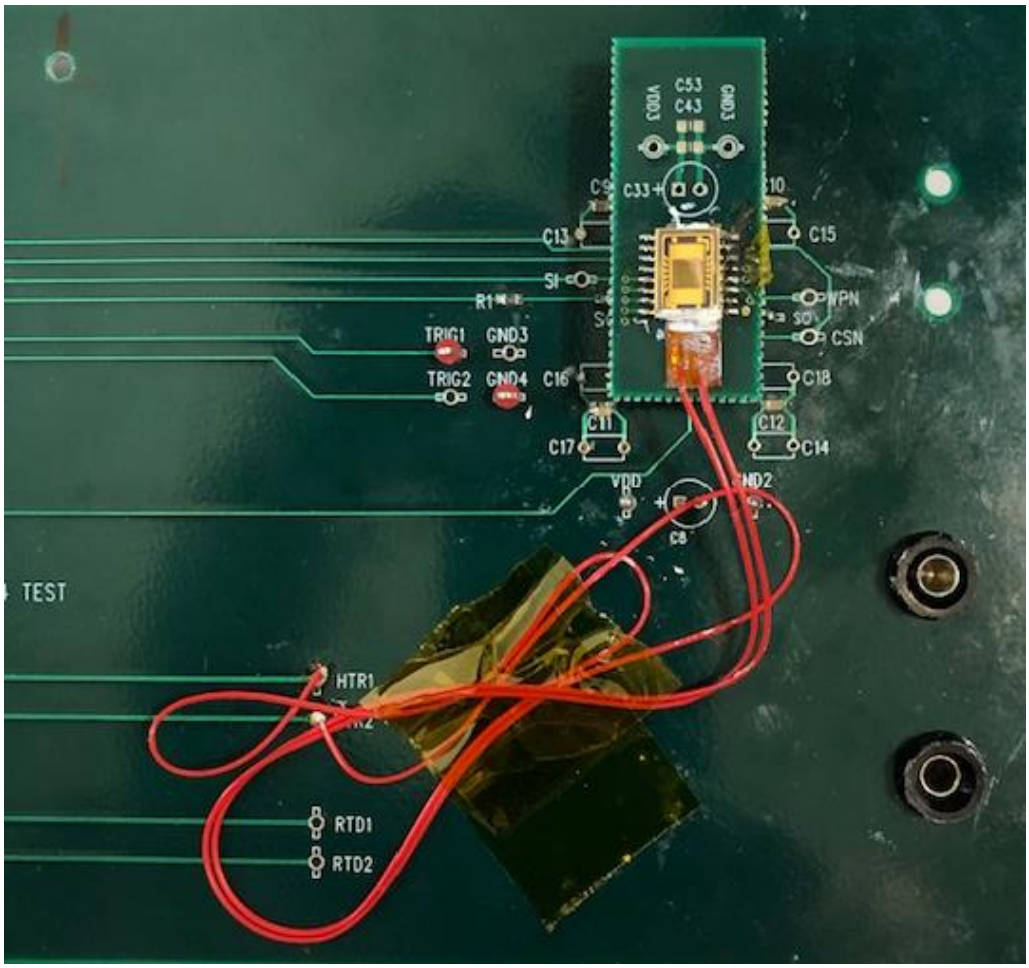

Figure 3. De-Lidded DUT on Carrier Card with Heat Strip Underneath

DUT temperature was monitored using an IR temperature sensor as shown in figure 4.

Figure 4. I.R. Temperature Sensor

2.1 Parts Identification

Parts were provided with serial numbers permanently printed on the metal lids. This number was logged into the test run log and used for traceability and reporting.

2.2 Parts Handling and Storage

These parts are considered sensitive to electrostatic discharge (ESD) and were handled accordingly.

2.3 Test Facility

An overview of the TAMU cyclotron facility is shown in figure 5. Devices were mounted to a test board positioned in air in front of the beam exit at the "radiation effects facility" location shown in the figure.

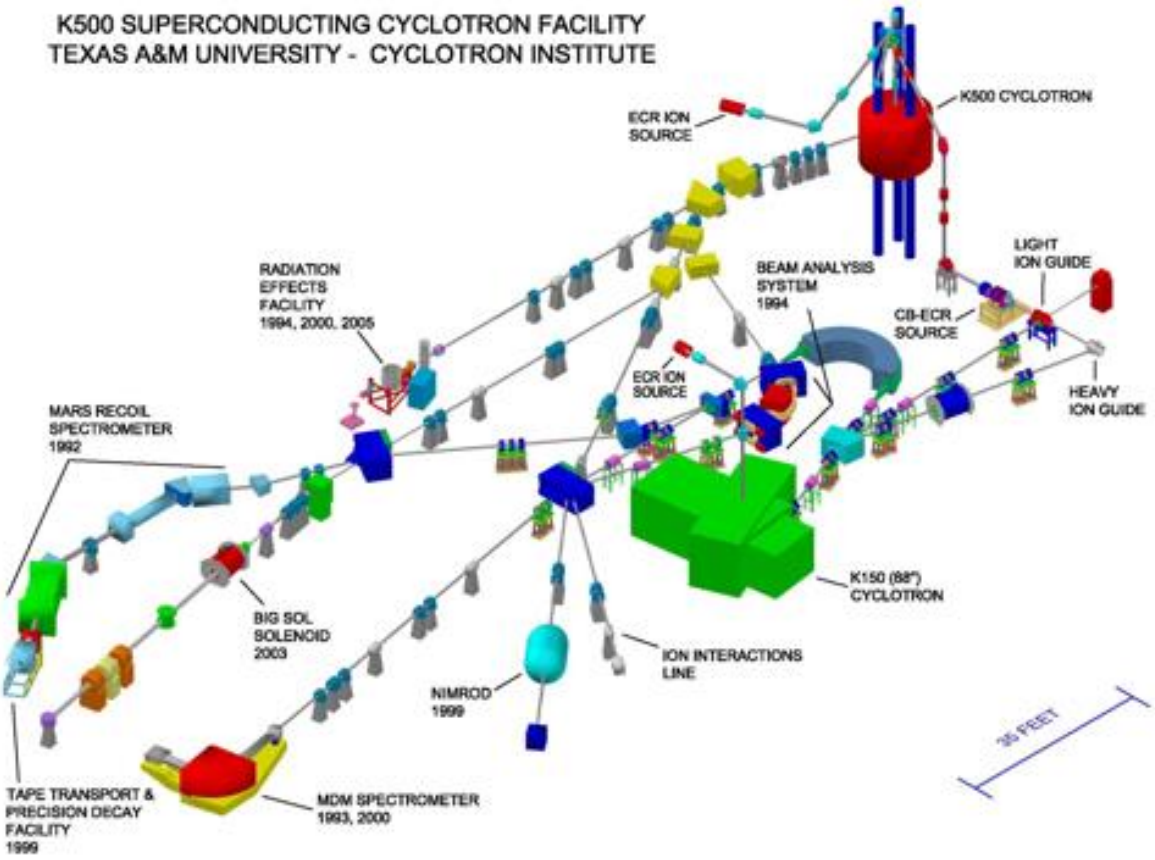

Figure 5. Overview of Texas A&M Cyclotron Facility (TAMU)

All irradiations were performed using the 15MEV tuning of the cyclotron. Figure 6 shows ions available for this tuning

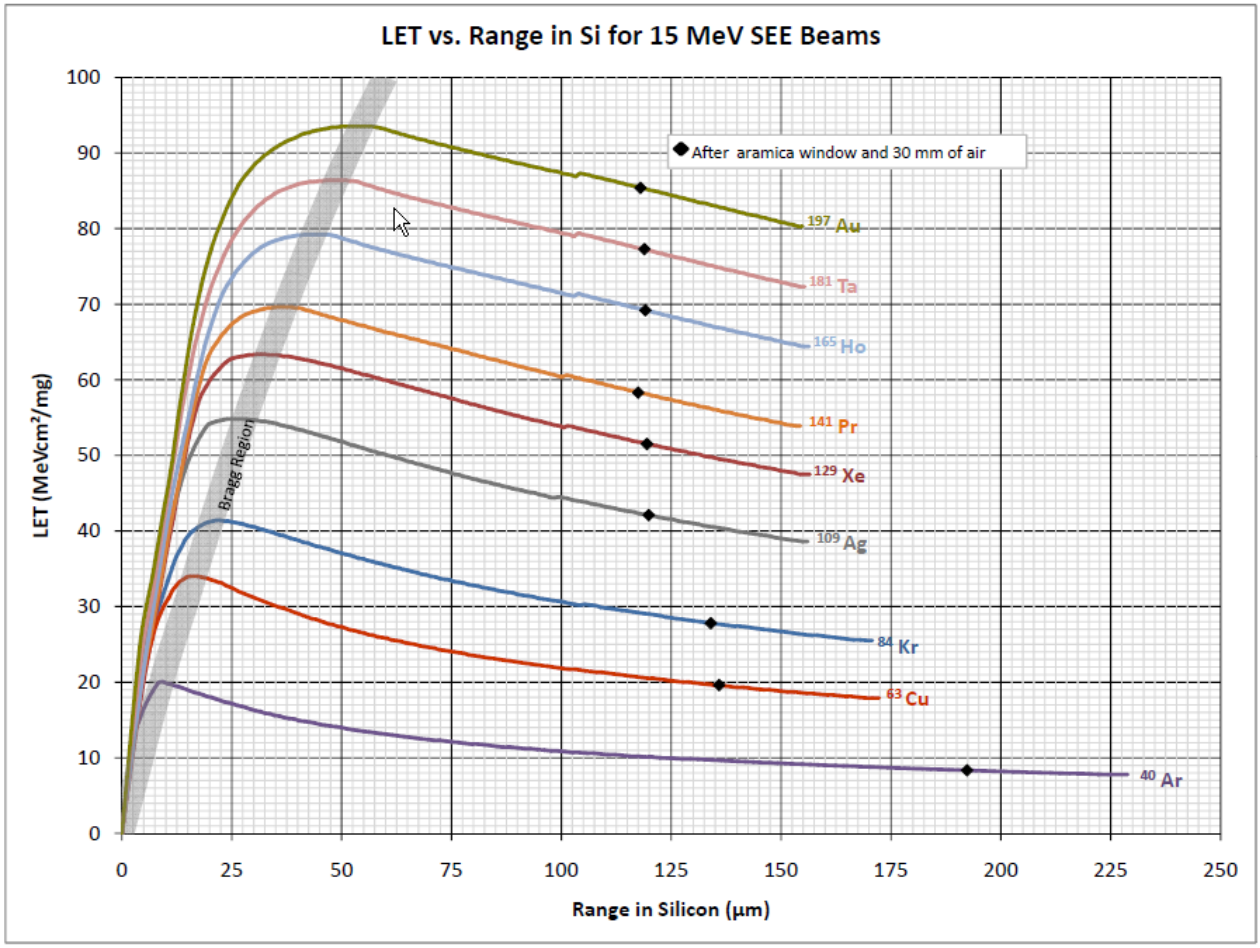

Figure 6. TAMU Ions Available with 15MeV Tuning

For this test the following ions were used:

ION	LET ($MeVcm^2/mg$)
^{129}XE	53.1 -> 61 (LET can be effectively doubled by tilting DUT 60^0)
^{84}KR	29.1 -> 41
^{40}AR	8.3 -> 15

2.4 Specific Test Requirements

2.4.1 Test Fixtures

Each DUT was permanently mounted to a small carrier card and inserted into a socket on the test card. The test card was then mounted in front of the ion beam exit window. Figure 7 is an overview of the test board.

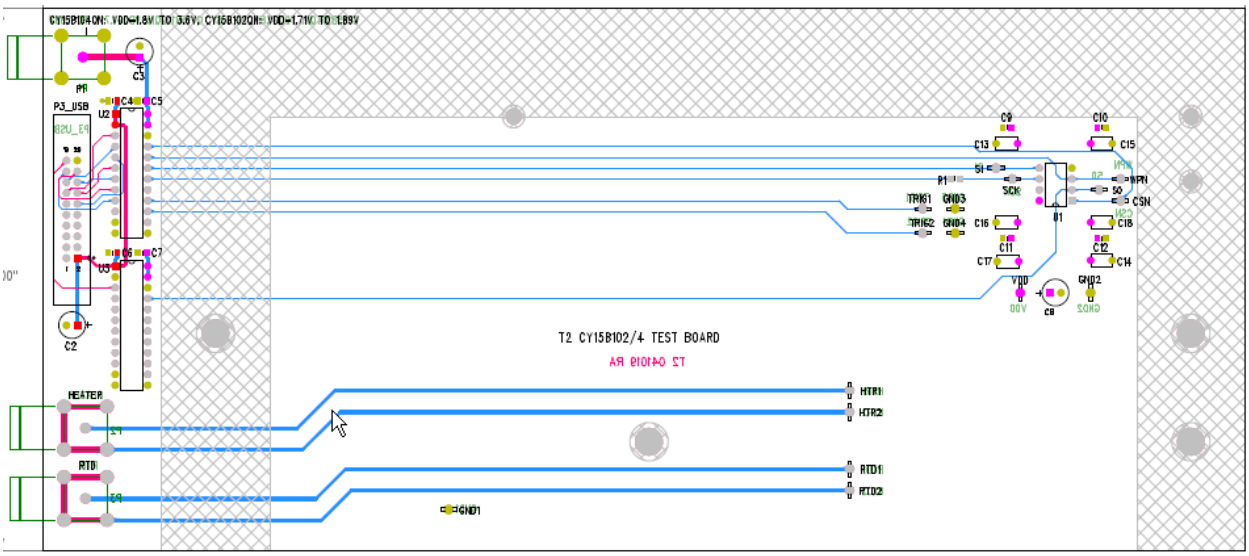

Figure 7. Test Board

2.4.2 Cabling

Devices were tested for both latchup and memory upset during this campaign. Cabling was provided to supply power to the DUT. A USB cable connected to special circuitry on the test board for functional testing of the DUT.

2.4.3 Test Procedure

Testing was performed at various temperatures between 20.2^{0}C of 125^{0}C. DUT temperature was measured using an IR thermometer before and after each run with elevated temperature.

2.4.4 Data Collection

Major test information was recorded in a "run log" spreadsheet. Figure 8 shows the data associated with one run. The complete run log is shown in Attachment A.

Run#	Start Time	DUT#	Test Type	Vdd	Temp	Idd-StdBy	#Bit Errs	#SEFI Errs	Dose	Ion	LET	Fluence	Flux	BitXS	SEFIXS	Comment
1	1714	83	StdBy-Rad-Read	2	20.2C	82uA	0	0	47	Kr	29.1	1.00E+05	4.97E+03	0	0	

Figure 8. SEE Partial Run Log For Cypress CYRS15B102, 2Mb FRAM

Detailed failure results were also collected as ascii text. Figure 9 shows a portion of the detailed failure log for run 3 which was a static CB test similar the one shown in the partial runlog above.

```
RUN Number = 3
DUT Number = 1
Addr = 0x00000, Exp = 0X55, Read = 0X56
Addr = 0x00001, Exp = 0XAA, Read = 0XBF
Addr = 0x00002, Exp = 0X55, Read = 0X8C
Addr = 0x00003, Exp = 0XAA, Read = 0XBA
Addr = 0x00004, Exp = 0X55, Read = 0XC5
Addr = 0x00005, Exp = 0XAA, Read = 0XEA
Addr = 0x00006, Exp = 0X55, Read = 0XE1
Addr = 0x00007, Exp = 0XAA, Read = 0XEB
Addr = 0x00008, Exp = 0X55, Read = 0X56
Addr = 0x00009, Exp = 0XAA, Read = 0XC2
Addr = 0x0000A, Exp = 0X55, Read = 0X07
Addr = 0x0000B, Exp = 0XAA, Read = 0XD2
Addr = 0x0000C, Exp = 0X55, Read = 0XD7
Addr = 0x0000D, Exp = 0XAA, Read = 0XF3
Addr = 0x0000F, Exp = 0XAA, Read = 0X82
Addr = 0x00010, Exp = 0X55, Read = 0XD2
                "
        (Errors continue)
                "
Addr = 0x0007F, Exp = 0XAA, Read = 0XEB
```

Figure 9. Portion of Detailed Error Log for Run 3, Static CB

The error sequence given in figure 9 with error addresses between 0x00000 and 0x0007F was repeatedly seen over the course of the SEU testing.

3.0 Test Results

3.1 SEL

Nine SEL tests were performed on 4 DUTs. All SEL testing was performed with Vdd = 3.6V, at an effective LET of 114.4 MeVcm^2/mg and at various temperatures. Each SEL run was done to a total fluence of 1.0x10^7 ions/ cm^2. Figure 10 shows the portion of the run log associated with these tests.

Run#	DUT#	Test Type	Vdd	Temp	Idd-StdBy	Dose	Fluence	Flux	Comment
64	83	SEL	3.6	125C	860uA	18000	1.0E+07	40000	7X jumps >100mA & back to 900uA
65	83	SEL	"	105C	400uA	18330	1.0E+07	37000	1X jump over 50mA then back immed
66	83	SEL	"	115C	533uA	18320	1.0E+07	41700	No current jumps.
67	83	SEL DPD	"	115C	18uA	18330	1.0E+07	47000	No current jumps, DUT is kicked out of DPD immediately when prog
68	83	SEL	"	125C	860uA	18335	1.0E+07	48300	1X jump over 50mA then back immed
76	75	SEL	"	115C	533uA	18000	1.0E+07	50000	No current jumps
77	75	SEL	"	125C	802uA	18750	1.0E+07	44000	24 jumps >50mA, some to 154mA. 1 True latch to 124mA that persisted
84	80	SEL	"	115C	6.3mA	18340	1.0E+07	40000	27 current spikes over 50mA, Idd-StdBy was high - SUSPECT PART
85	79	SEL	"	115C	490uA	18000	1.0E+07	40000	1 current jump over 50mA

Figure 10. Portion of Error Log for SEL Tests

Over the course of SEL testing there was only one true latch and this occurred at a temperature of 125^{0}C. No latches occurred in any device when they were heated to 115^{0}C.

When devices were irradiated at 125^{0}C there were many instances where Idd would abruptly increase and then return to a low level. The frequency of these jumps was much less at 115^{0}C. One DUT (SN80) had a much higher standby Idd prior to radiation which may have been due to

damage in the de-lidding process. This one part had many more current jumps at 115^0C than the other parts but this was attributed to whatever caused it's higher standby current.

Because there were no latches and very few current jumps at a Vdd of 3.6V, die temperature of 115^0C and LET of 114.4 MeVcm^2/mg this was identified as a valid specification limit for parts from this manufacturing lot.

3.2 Temporary Current Increases

In addition to the current jumps seen during SEL testing there were 5 runs where temporary increases in Idd were observed. Summary of information from these runs is shown in figure 11.

Run#	DUT#	Test Type	Vdd	Temp	Ion	LET	Fluence	Flux	Comment
25	75	StdBy-Rad-Read	2	20.2C	Kr	29.1	5.00E+06	2.00E+04	Current jumped to 18mA & was reset by going to DPD
27	75	StdBy-Rad_Sleep/Wake/Read	"	"	"	29.1	5.00E+06	2.42E+03	Current jumped to 18mA & was reset by going to DPD
30	75	StdBy-Rad-Read	"	"	Ar	15	5.00E+06	2.20E+04	Current jumped
40	73	StdBy-Rad-PwrCyc/Read	"	"	"	15	5.00E+06	2.10E+04	Current jumped to 18mA & was reset by going to DPD
43	83	StdBy-Rad-PwrCyc/Read	"	"	"	15	5.00E+06	2.10E+04	Current jumped to 18mA & was reset by going to DPD

Figure 11. Portion of Error Log Showing Temporary increases in Idd

This increase did not affect part operation. In run #30 the DUT was read immediately after the end of radiation and worked properly. The fact that the increased current was reset in the other runs indicates that the increased current was occurring in the portion of the circuit that was powered down & reset by programming the part into DPD and then back to standby. The fact that the increase was only to 18mA meant that this was not classified as a latchup.

3.3 Bit Upset Cross-Sections, Normal Operation

In normal operation a memory will be loaded with information, power will be maintained constantly and the part will be periodically read. During this campaign parts were tested using this profile and the associated runs were labeled "StdBy-Rad-Read". Figure 12 shows the resultant bit upset cross-sections when parts were tested using this profile.

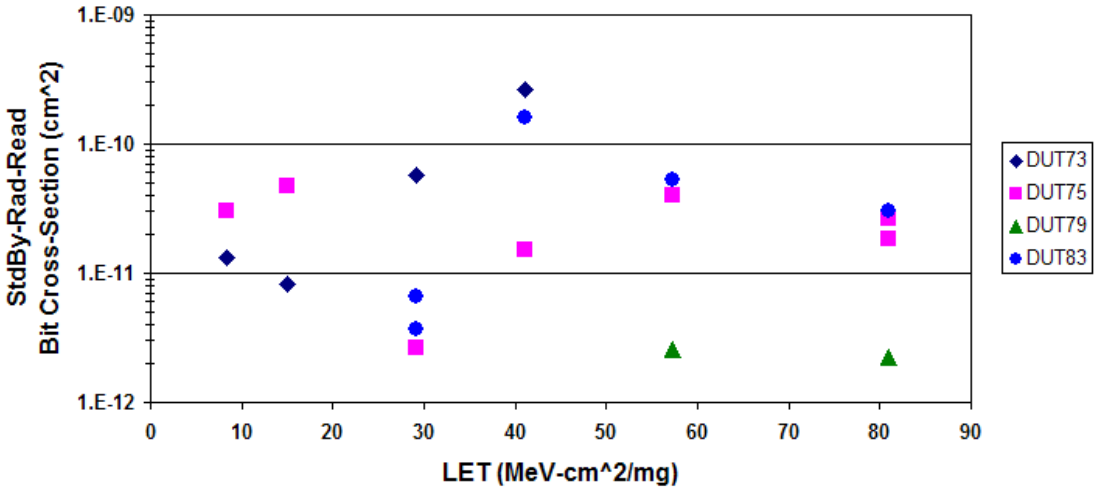

Figure 12. Bit Upset Cross-Sections, Normal Operation

This plot is somewhat confusing until the effects of radiation on supporting CMOS circuitry is considered.

First, as was mentioned earlier, many radiation runs would result in a large number of errors at addresses in the range of 0x00000 -> 0x0007F. Instead of being a large number of memory upsets this should be considered a single SEFI upset. The reason this large block of upset addresses always occurred at the beginning of memory is not understood at this point and should be investigated further.

The second phenomena observed was that some errors would be stable when repeatedly read after radiation but would then disappear when power was cycled. For instance, the error pattern read immediately after the run #30 radiation is shown in figure 13. This same pattern was read several times and did not change. Then power was cycled to the part and all the errors in red disappeared, leaving only the errors in the address range 0x00000 -> 0x0007F.

```
RUN Number = 30
DUT Number = CYRS15B102
Addr = 0x00000, Exp = 0X55, Read = 0X00
Addr = 0x00001, Exp = 0XAA, Read = 0XE8
Addr = 0x00002, Exp = 0X55, Read = 0X08
Addr = 0x00003, Exp = 0XAA, Read = 0X08
Addr = 0x00004, Exp = 0X55, Read = 0X00
Addr = 0x00005, Exp = 0XAA, Read = 0X00
Addr = 0x00006, Exp = 0X55, Read = 0X00
          -
    Address Sequence Continues
          -
Addr = 0x0007D, Exp = 0XAA, Read = 0X06
Addr = 0x0007E, Exp = 0X55, Read = 0X80
Addr = 0x0007F, Exp = 0XAA, Read = 0X01
Addr = 0x2B1A8, Exp = 0X55, Read = 0X5D
Addr = 0x2B1AB, Exp = 0XAA, Read = 0X9A
Addr = 0x32259, Exp = 0XAA, Read = 0X4A
Addr = 0x3225A, Exp = 0X55, Read = 0XAB
Addr = 0x3225B, Exp = 0XAA, Read = 0XD4
```

Figure 13. Upset Pattern Immediately after Run 30

This behavior seems to indicate there was some upset in the CMOS circuitry that could be reset by re-initializing the part.

Various versions of this phenomenon were observed over the course of testing. Another typical profile was when the DUT would be re-written immediately after the static test but before power cycling. After this write the memory could be read with no errors. However, after subsequent power cycling some errors would be detected. This profile seems to indicate that there was some upset in memory decode logic which was reset by power cycling.

Writing after power cycling would always result in proper initialization of the memory pattern.

3.4 Re-Initialization Tests

These devices go through an initialization sequence at power-on when Vdd rises above ~1.5V. This same initialization sequence is performed whenever a part is returning from Deep Power Down (DPD) to normal standby. The initialization consists of reading configuration information from special non-volatile memory and programming various internal control latches and registers.

The upset behavior described above seemed to be the result of upsets occurring in CMOS circuitry and then being permanently written into FRAM memory as part of the read cycle. The question was whether these CMOS upsets could be partially or completely cleared by re-initializing the DUTs after radiation but before reading memory.

Two test sequences were devised to investigate this. In the first sequence parts were programmed into DPD (sleep) and then back to normal standby. In the second sequence power would be cycled to the part after radiation but prior to reading. Two initialization sequences were used to determine whether a complete power cycle would have better results than the DPD-StandBy programming sequence.

The results for tests using these 2 sequences are shown in figures 14 and 15. Figure 14 shows the results when the parts were programmed into and out of DPD. Figure 15 shows the results when power was cycled. Note that the SEFI failure persisted through both sequences where there was sometimes a large block of errors between addresses 0x00000 and 0x0007F. If errors in this region are ignored then there were no additional errors in any part during any run.

Run#	DUT#	#Bit Errs	Dose	Ion	LET	Fluence	Flux	Bit Cross-Section	Bit Cross-Section Outside Addr 0x00000->0x0007F	Comment
7	83	400	2328	Kr	29.1	5.00E+06	2.00E+04	3.81E-11	0	Failures at 0x00 -> 0x07F Only
16	73	498	657	"	41	1.00E+06	2.16E+04	2.37E-10	0	Failures at 0x00 -> 0x07F Only
27	75	500	2328	"	29.1	5.00E+06	2.42E+03	4.77E-11	0	Failures at 0x00 -> 0x07F Only
28	75	433	1200	Ar	15	5.00E+06	2.10E+04	4.13E-11	0	Failures at 0x00 -> 0x07F Only
37	75	0	668	"	8.3	5.00E+06	2.10E+04	0.00E+00	0	
47	83	0	668	"	8.3	5.00E+06	2.33E+04	0.00E+00	0	
53	73	464	4583	Xe	57.2	5.00E+06	2.50E+04	4.43E-11	0	Failures at 0x00 -> 0x07F Only
57	73	0	3887	"	81	3.00E+06	1.30E+04	0.00E+00	0	
58	83	322	3891	"	81	3.00E+06	1.30E+04	5.12E-11	0	Failures at 0x00 -> 0x07F Only
63	83	0	2758	"	57.2	3.00E+06	2.35E+04	0.00E+00	0	
71	75	432	3882	"	81	3.00E+06	2.40E+04	6.87E-11	0	Failures at 0x00 -> 0x07F Only
75	75	420	2758	"	57.2	3.00E+06	2.20E+04	6.68E-11	0	Failures at 0x00 -> 0x07F Only
79	79	507	2739	"	57.2	3.00E+06	4.40E+04	8.06E-11	0	Failures at 0x00 -> 0x07F Only
83	79	500	3899	"	81	3.00E+06	3.66E+04	7.95E-11	0	Failures at 0x00 -> 0x07F Only

Figure 14. Run log for "StdBy-Rad_Sleep/Wake/Read"

Run#	DUT#	#Bit Errs	Dose	Ion	LET	Fluence	Flux	Bit Cross-Section	Bit Cross-Section Outside Addr 0x00000->0x0007F	Comment
8	83	0	2332	Kr	29.1	5.00E+06	1.98E+04	0.00E+00	0	
17	73	0	658	"	41	1.00E+06	2.28E+04	0.00E+00	0	
18	73	492	659	"	41	1.00E+06	2.16E+04	2.35E-10	0	Failures at 0x00 -> 0x07F Only
22	75	498	3302	"	41	5.00E+06	2.00E+04	4.75E-11	0	Failures at 0x00 -> 0x07F Only
26	75	0	2331	"	29.1	5.00E+06	1.88E+04	0.00E+00	0	
29	75	500	1200	Ar	15	5.00E+06	2.09E+04	4.77E-11	0	Failures at 0x00 -> 0x07F Only
36	75	0	666	"	8.3	5.00E+06	2.30E+04	0.00E+00	0	
39	73	0	666		8.3	5.00E+06	2.30E+04	0.00E+00	0	
40	73	506	1204	"	15	5.00E+06	2.10E+04	4.83E-11	0	Failures at 0x00 -> 0x07F Only
43	83	406	1200	"	15	5.00E+06	2.10E+04	3.87E-11	0	Failures at 0x00 -> 0x07F Only

Figure 15. Run log for "StdBy-Rad-PwrCyc/Read"

3.5 Continuous READ Errors

Continuous read tests were performed by loading memories with a checkerboard pattern and then repeatedly reading the entire memory while the device was being irradiated. Reads were performed using an "extended read" protocol. For this type of operation a "READ" command is shifted into the DUT followed by 3 bytes of starting address. Data from the starting address immediately begins appearing at the DUT output on succeeding clocks. As long as the DUT continues to receive clocks and its chips select (CS*) pin is held low it will continue to output data from successive addresses. Internal circuitry increments the address being read. (Note: this is the type of read performed for "boot ROM" operations.)

For the continuous read test an extended read operation would be used to read all data stored in DUT memory. After data from all addresses had been read and the extended read terminated then another extended read operation would be started.

One type of SEFI that occurred frequently while doing these tests was that the DUT would stop outputting valid information and all subsequent data from that extended read would be interpreted as 0xFF. Data would be good on the following read. Error data from the entire run was logged in ASCII files so this type of SEFI could be identified.

ASCII data also permitted the identification of memory clusters that had been upset. Previous FXR testing suggested that data internal to these DUTs is organized in 64 bit chunks (8 bytes). Thus, if an upset occurred during a read/re-write operation it could affect memory at up to 8 contiguous addresses.

At the conclusion of the radiation exposure the DUTs would be read one last time to see how many errors had been generated in memory over the course of the radiation.

A summary of the run log for the read continuous tests is shown in figure 16. Note that the number of times the extended read was terminated and the number of occurrences of 8 sequential addresses was added by hand after analyzing the ASCII files of error log data.

Run#	DUT#	#Bit Errs	# Read Term SEFI	# 8-Addr Errs	LET	Fluence	Flux	Bit X-Sect	Read Term X-Sect	Chunk Err X-Sect
9	83	29	3	2	29.1	1.0E+05	9.5E+02	1.38E-10	3.00E-05	2.00E-05
10	"	241	5	6	41	1.0E+05	1.1E+03	1.15E-09	5.00E-05	6.00E-05
23	75	89	6	5	41	1.0E+05	9.7E+02	4.24E-10	6.00E-05	5.00E-05
24	"	202	3	6	29.1	1.0E+05	9.1E+02	9.63E-10	3.00E-05	6.00E-05
31	"	119	2		15	1.0E+05	9.4E+03	5.67E-10	2.00E-05	
32	"	159	3	3	15	1.0E+05	1.2E+03	7.58E-10	3.00E-05	3.00E-05
33	"	84	2		8.3	1.0E+05	6.2E+03	4.01E-10	2.00E-05	
34	"	105	3	4	8.3	6.0E+05	1.4E+03	8.34E-11	5.00E-06	6.67E-06
44	83	99	1	0	15	1.0E+05	1.1E+03	4.72E-10	1.00E-05	0.00E+00
45	"	115	2	2	8.3	1.0E+05	1.3E+03	5.48E-10	2.00E-05	2.00E-05
48	73	12	1	1	8.3	5.0E+05	2.2E+03	1.14E-11	2.00E-06	2.00E-06
49	"	187	0	5	15	1.0E+05	1.5E+03	8.92E-10	0.00E+00	5.00E-05
54	"	201	6	10	57.2	1.0E+05	1.4E+03	9.58E-10	6.00E-05	1.00E-04
55	"	152	11		81	1.0E+05	1.4E+03	7.25E-10	1.10E-04	
60	83	134	8		81	1.0E+05	1.7E+03	6.39E-10	8.00E-05	
61	"	160	3	7	57.2	1.0E+05	1.7E+03	7.63E-10	3.00E-05	7.00E-05
72	75	187	11	11	81	1.0E+05	2.3E+03	8.92E-10	1.10E-04	1.10E-04
73	"	194	5		57.2	1.0E+05	2.3E+03	9.25E-10	5.00E-05	
80	79	96	7		57.2	1.0E+05	2.3E+03	4.58E-10	7.00E-05	
81	"	162	7	7	81	1.0E+05	2.1E+03	7.72E-10	7.00E-05	7.00E-05

Figure 16. Run log for Read Continuous Tests

This information can be plotted as follows. First, the bit upset cross-sections for all runs is shown in Figure 17.

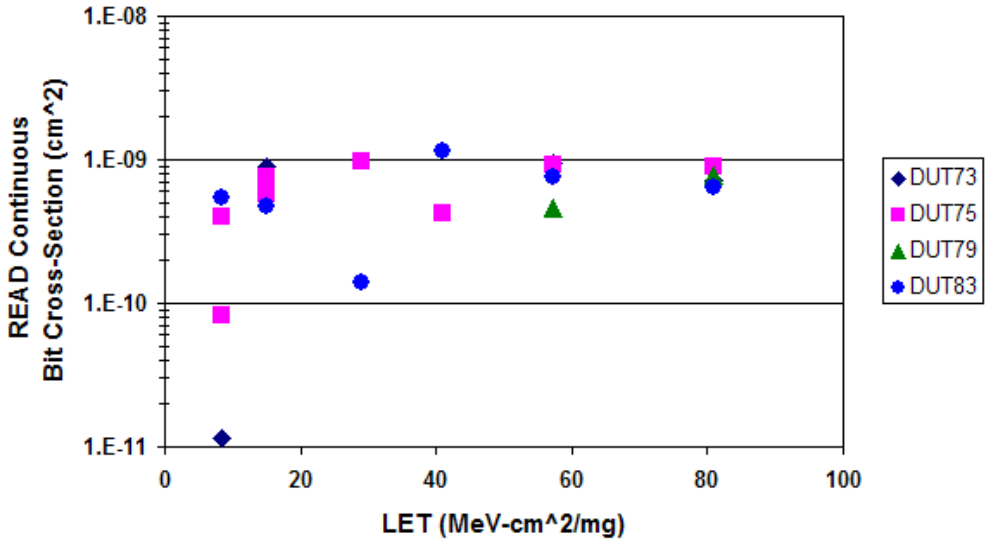

Figure 17. Bit Upset Cross-Sections for READ CONTINUOUS Tests

Figure 18 is a plot of device cross-sections for the READ TERMINATE SEFIs.

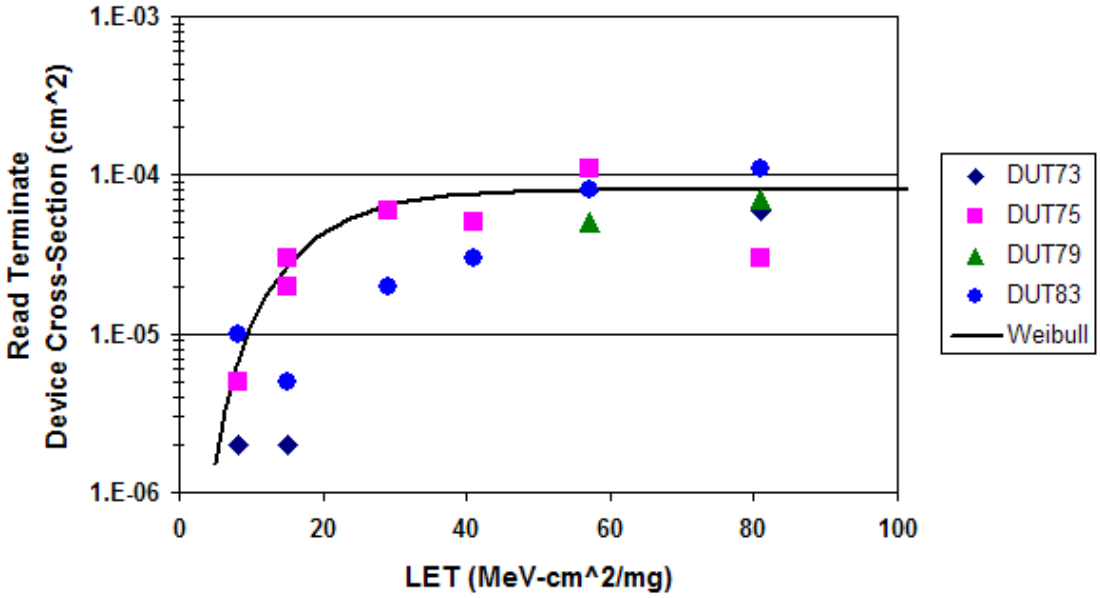

Figure 18. Device Cross-Sections for "READ TERMINATE" SEFIs

A Weibull curve for this type of SEFI is included on the plot. Parameters for this curve are shown in figure 19 below:

Onset LET – 2.5 MeV-cm^2/mg
Power - 1.9
Width - 28
Saturation - 8e-5 cm^2

Figure 19. Weibull Parameters for Read Terminate SEFI Errors

Figure 20 is a plot of device cross-sections for the occurrence of "8-Address" upsets. A Weibull curve is also shown on this plot using the same parameters listed above.

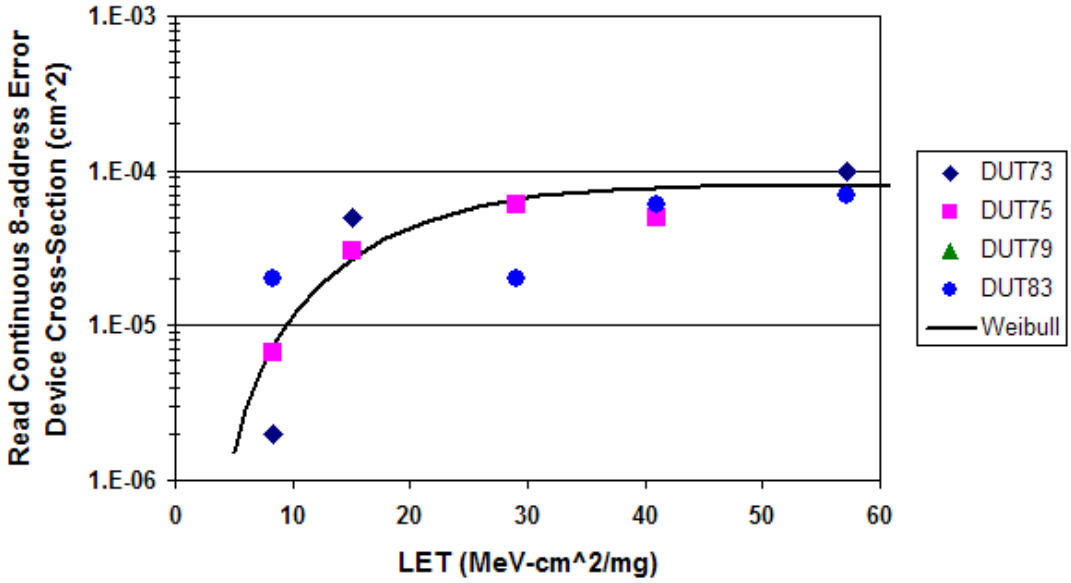

Figure 20. Device Cross-Sections for "8-Address" Upsets

4.0 Analysis

CREME96 was used along with the above listed Weibull parameters to calculate the rate of occurrence for SEFIs in several orbits. The results of these simulations are shown in figure 21. Copies of the print-outs from the CREME96 runs are included in Attachment B.

Orbit	Upsets/Day
Space Station, Worst Day	0.00542
Geosynchronous, Solar Min	0.000134

Figure 21. SEFI Upset Rates for Several Orbits

Thus, if one of these parts was continuously read while in Geosynchronous orbit during Solar Min conditions there would be one SEFI every 7,462 days on average.

Even if "Worst Day" conditions are assumed there would only be an average probability of 0.54% that a SEFI would occur in Space Station orbit during that day.

5.0 Conclusions

These parts appear to be latchup immune up to a temperature of 115^0C when irradiated with 10^7 ions/cm^2 with ions having an LET of 114.4 MeV-cm^2/mg. This manufacturing lot of CYRS15B102 devices passes this parameter to this level.

Actual memory cells are very resistant to heavy ion radiation. Over the entire campaign no errors were detected that were clearly memory cell upsets. Only errors associated with logic upsets have been found.

A technique was identified (either power cycling of DPD mode cycling) which will eliminate all errors in memory with the possible exception of memory in the range of 0x00000 to 0x0007F.

6.0 Recommendations for Improvement

1. All testing in this campaign used very high flux (10,000 ions/cm^2/sec typical) because of the low error rates in these devices. This might have affected the SEFI upset rates. Further testing using lower flux could validate these measurements.

2. Static CB testing was not adequate to determine cross-section of the SEFI upsets for memories in the 0x00000 -> 0x0007F address range. Further testing is recommended to characterize this phenomenon and to change the starting address for read / write operations.

Attachment A. RUN LOG

Run#	StartTime	DUT#	TestType	Vdd	Temp	Idd-StdBy	#BitErrs	#SEFI	ErrS	Dose	Ion	LET	Fluence	Flux	BitXS	SEFI XS	Comment
1	1714	83	StdBy-Rad-Read	2	20.2C	82uA	0	0		47	Kr	29.1	1.00E+05	4.97E+03	0	0	
2	1718	83	"	"	"	"	1			467	"	29.1	1.00E+06	4765	4.77E-13		
3	1724	83	"	"	"	"	340	0		1479	"	29.1	3.17E+06	9.89E+03	5.11E-11	0	Failures at 0x00 -> 0x07F Only
4	1535	83	"	"	"	"	0	0		926	"	29.1	2.00E+06	10480	0	0	
5	1542	83	"	"	"	"	23	0			"	29.1	3.00E+06		3.86E-12		Power Cycle before Radiation
5B	1545	83	"	"	"	"	12	0			"	29.1	4.00E+06		1.43E-12		# Errs went down!
5C	1550	83	"	"	"	"		1		2328	"	29.1	5.00E+06	1.00E+04	0	2E-07	
6	1559	83	"	"	"	"	70	0		2328	"	29.1	5.00E+06	3.00E+04	6.68E-12		2 Clusters of errors
7	1807	83	StdBy-Rad_Sleep/Wake/Read	"	"	"	400	0		2328	"	29.1	5.00E+06	2.00E+04	2.44E-09	0	All failures at sequential addresses: 0x00 -> 0x07
8	1814	83	StdBy-Rad-PwrCyc/Read	"	"	"	0	0		2332	"	29.1	5.00E+06	1.98E+04	0	0	No Errors at 5e6 with power cycle before read!
9	1822	83	Countinuous READCB	"	"	"	29			46	"	29.1	1.00E+05	9.52E+02	1.38E-10		
10	1836	83	Continuous READCB	"	"	"	241	5		66	"	41	1.00E+05	1.14E+03	1.15E-09	5E-05	
11	1842	83	StdBy-Rad-PwrCyc/Read	"	"	"		1		3302	"	41	5.00E+06	1.99E+04	0	2E-07	All failures at sequential addresses: 0x00 -> 0x07
12	1853	83	"	"	"	"		1		3295	"	41	5.00E+06	2.00E+04	0	2E-07	All failures at sequential addresses: 0x00 -> 0x08
13	1903	83	StdBy-Rad-Read	"	"	"	332	0		650	"	41	1.00E+06	1.99E+04	1.58E-10		6 bursts of 2 - 4 - 8 addresses
14	1915	73	StdBy-Rad-Read	"	"	"	547			661	"	41	1.00E+06	2.20E+04	2.61E-10		2 Bursts, first is at 00 -> 7F
15	1927	73	StdBy-Rad-PwrCyc/Read	"	"	"	0	0		857	"	41	1.00E+06	2.17E+04	0		No Errors with Pwr Cycle
16	1932	73	StdBy-Rad Sleep/Wake/Read	"	"	"	498	0		857	"	41	1.00E+06	2.16E+04	2.37E-10		All failures at sequential addresses: 0x00 -> 0x07
17	1935	73	StdBy-Rad-PwrCyc/Read	"	"	"	0	0		858	"	41	1.00E+06	2.28E+04	0		No Errors with Pwr Cycle
18	1939	73	StdBy-Rad-PwrCyc/Read	"	"	"	492			859	"	41	1.00E+06	2.16E+04	2.35E-10		All failures at sequential addresses: 0x00 -> 0x07
19	1948	73	StdBy-Rad-Read	"	"	"	0	0		918	"	29.1	2.00E+06	2.34E+04	0		No errors
20	1953	73	StdBy-Rad-Read	"	"	"	358			1403	"	29.1	3.00E+06	2.32E+04	5.69E-11		All failures at sequential addresses: 0x00 -> 0x07
21	2005	75	StdBy-Rad-Read	"	"	"	32	0		861	"	41	1.00E+06	2.05E+04	1.53E-11		All failures at sequential addresses: 0x00 -> 0x07
22	2011	75	StdBy-Rad-PwrCyc/Read	"	"	"	498	0		3302	"	41	5.00E+06	2.00E+04	4.75E-11		All failures at sequential addresses: 0x00 -> 0x07
23	2025	75	Countinuous READCB	"	"	"	89	6		65	"	41	1.00E+05	9.73E+02	4.24E-10	6E-05	
24	2034	75	Countinuous READCB	"	"	"	202	3		46	"	29.1	1.00E+05	9.13E+02	9.83E-10	3E-05	109 errors after pwr cycle (202 after rad)
25	2041	75	StdBy-Rad-Read	"	"	"	28	0	2.30E+03	"	"	29.1	5.00E+06	2.00E+04	2.67E-12		All failures at sequential addresses: 0x00 -> 0x07, Current jumped to 18mA & was reset bygoing to DPD
26	2049	75	StdBy-Rad-PwrCyc/Read	"	"	"	0	0		2331	"	29.1	5.00E+06	1.88E+04	0		NO ERRORS
27	2057	75	StdBy-Rad_Sleep/Wake/Read	"	"	"	500	0		2328	"	29.1	5.00E+06	2.42E+03	4.77E-11		All failures at sequential addresses: 0x00 -> 0x07, Current jumped to 18mA & was reset bygoing to DPD
28	2131	75	StdBy-Rad_Sleep/Wake/Read	"	"	"	433	0		1200	Ar	15	5.00E+06	2.10E+04	4.13E-11		All failures at sequential addresses: 0x00 -> 0x07
29	2139	75	StdBy-Rad-PwrCyc/Read	"	"	"	500	0		1200	"	15	5.00E+06	2.09E+04	4.77E-11		All failures at sequential addresses: 0x00 -> 0x07
30	2145	75	StdBy-Rad-Read	"	"	"	489	0		1200	"	15	5.00E+06	2.20E+04	4.86E-11		Some failures cleared after pwr cycle, then All failures at sequential addresses: 0x00 -> 0x07, Current
31	2159	75	Countinuous READCB	"	"	"	119	2		23	"	15	1.00E+05	9.43E+03	5.87E-10	2E-05	
32	2204	75	Countinuous READCB	"	"	"	159	3		24	"	15	1.00E+05	1.25E+03	7.58E-10	3E-05	
33	2220	75	Countinuous READCB	"	"	"	84	2		151	"	8.3	1.00E+05	8.20E+03	4.01E-10	2E-05	
34	2224	75	Countinuous READCB	"	"	"	105	3		66	"	8.3	6.00E+05	1.42E+03	8.34E-11	5E-06	
35	2235	75	StdBy-Rad-Read	"	"	"	321	0		866	"	8.3	5.00E+06	1.00E+04	3.06E-11	0	
36	2245	75	StdBy-Rad-PwrCyc/Read	"	"	"	0	0		866	"	8.3	5.00E+06	2.30E+04	0	0	
37	2251	75	StdBy-Rad Sleep/Wake/Read	"	"	"	0	0		868	"	8.3	5.00E+06	2.10E+04	0	0	
38	2300	73	StdBy-Rad-Read	"	"	"	139	0		866	"	8.3	5.00E+06	2.16E+04	1.33E-11	0	After pwr cycle then 0x00->0x07 Plus 1 error
39	2309	73	StdBy-Rad-PwrCyc/Read	"	"	"	0	0		866	"	8.3	5.00E+06	2.30E+04	0	0	
40	2316	73	StdBy-Rad-PwrCyc/Read	"	"	"	506	0		1204	"	15	5.00E+06	2.10E+04	4.83E-11	0	All failures at sequential addresses: 0x00 -> 0x07, Current jumped to 18mA & was reset bygoing to DPD
41	2328	73	StdBy-Rad-Read	"	"	"	87	0		1200	"	15	5.00E+06	2.20E+04	8.3E-12	0	Errs not at 0x00->
42	2338	83	StdBy-Rad-Read	"	"	"	0	0		1200	"	15	5.00E+06	2.20E+04	0	0	
43	2344	83	StdBy-Rad-PwrCyc/Read	"	"	"	408	0		1200	"	15	5.00E+06	2.10E+04	3.87E-11	0	All failures at sequential addresses: 0x00 -> 0x07, Current jumped to 18mA & was reset bygoing to DPD
44	2349	83	Countinuous READCB	"	"	"	99	2		24	"	15	1.00E+05	1.10E+03	4.72E-10	2E-05	
45	2354	83	Countinuous READCB	"	"	"	115	2		13	"	8.3	1.00E+05	1.27E+03	5.48E-10	2E-05	
46	1	83	StdBy-Rad-Read	"	"	"	0	0		867	"	8.3	5.00E+06	2.25E+04	0	0	
47	4	83	StdBy-Rad Sleep/Wake/Read	"	"	"	0	0		868	"	8.3	5.00E+06	2.33E+04	0	0	
48	14	73	Countinuous READCB	"	"	"	12	1		66	"	8.3	5.00E+05	2.20E+03	1.14E-11	2E-06	
49	22	73	Countinuous READCB	"	"	"	187	0		24	"	15	1.00E+05	1.50E+03	8.92E-10	0	1 Bit error after power cycle!!

Run#	Start Time	DUT#	Test Type	Vdd	Temp	Idd-StdBy	#Bit Errs	#SEFI Errs	Dose	Ion	LET	Fluence	Flux	Bit XS	SEFI XS	Comment
50	100	73	StdByRad-Read	"	"	"	0	0	907	Xe	57.2	9.90E+05	2.60E+04	0	0	
51	108	73	StdByRad-Read	"	"	"	11	0	4586	"	57.2	5.00E+06	2.35E+04	1.05E-12	0	Failures at 0x00 -> 0x07 + 1 address
52	115	73	StdByRad-Read	"	"	"	551	0	4595	"	57.2	5.00E+06	2.50E+04	5.25E-11	0	Failures at 0x00 -> ox7F + 5 more, only 0x00 -> 0x7F
53	120	73	StdByRad_Sleep/Wake/Read	"	"	"	484	0	4583	"	57.2	5.00E+06	2.50E+04	4.43E-11	0	All failures at sequential addresses: 0x00 -> 0x07F
54	125	73	Countinuous READ CB	"	"	"	201	6	91	"	57.2	1.00E+05	1.40E+03	8.58E-10	6E-05	Errs reduced to 56 after pwr cycle
55	130	73	Countinuous READ CB	"	"	"	152	11	129	"	81	1.00E+05	1.40E+03	7.25E-10	1.10E-04	
56	141	73	StdByRad-Read	"	"	"	34	0	3885	"	81	3.00E+06	1.33E+04	5.4E-12	0	Failures at 0x00 -> 0x07
57	149	73	StdByRad_Sleep/Wake/Read	"	"	"	0	0	3887	"	81	3.00E+06	1.30E+04	0	0	
58	205	83	StdByRad_Sleep/Wake/Read	"	"	"	322	0	3891	"	81	3.00E+06	1.30E+04	5.12E-11	0	Failures at 0x00 -> 0x07F Only
59	214	83	StdByRad-Read	"	"	"	193	0	3891	"	81	3.00E+06	1.30E+04	3.07E-11	0	Failures at 0x00 -> 0x07F Only
60	225	83	Countinuous READ CB	"	"	"	134	8	130	"	81	1.00E+05	1.70E+03	6.39E-10	8E-05	92 errs after pwr cyc
61	228	83	Countinuous READ CB	"	"	"	160	3	92	"	57.2	1.00E+05	1.70E+03	7.63E-10	3E-05	55 errs after pwr cyc
62	232	83	StdByRad-Read	"	"	"	4	0	2751	"	57.2	3.00E+06	2.50E+04	6.38E-13	0	0 errs after pwr cyc
63	237	83	StdByRad_Sleep/Wake/Read	"	"	"	0	0	2758	"	57.2	3.00E+06	2.35E+04	0	0	
64	250	83	SEL	3.6	125C	860uA	1719	0	18000	"	114.4	1.00E+07	4.00E+04	8.25E-11	0	7X jumps > 100mA & back to 900uA, 0x00 -> 0x7f +
65	330	83	SEL	"	105C	400uA	448	0	18330	"	114.4	1.00E+07	3.70E+04	2.14E-11	0	1X jump over 50mA then back immed, 0x00 -> 0x7f
66	345	83	SEL	"	115C	533uA	445	0	18320	"	114.4	1.00E+07	4.17E+04	2.12E-11	0	no current jumps
67	356	83	SEL DPD	"	115C	18uA		0	18330	"	114.4	1.00E+07	4.70E+04		0	No current jumps, DUT is kicked out of DPD
68	410	83	SEL	"	125C	860uA	3538	0	18335	"	114.4	1.00E+07	48300	1.69E-10		1X jump over 50mA then back immed
69	434	75	StdByRad-Read	2	20.2C	83uA	185	0	3882	"	81	3.00E+06	2.30E+04	2.62E-11		no Errs after re-write
70	441	75	StdByRad-Read	"	"	"	115	0	3882	"	81	3.00E+06	2.30E+04	1.83E-11		
71	446	75	StdByRad_Sleep/Wake/Read	"	"	"	432	0	3882	"	81	3.00E+06	2.40E+04	8.87E-11		Failures at 0x00 -> 0x07F Only
72	451	75	Countinuous READ CB	"	"	"	187	11	129	"	81	1.00E+05	2.30E+03	8.92E-10	0.000011	Errs cleared with re-write
73	457	75	Countinuous READ CB	"	"	"	194	5	91	"	57.2	1.00E+05	2.30E+03	9.25E-10	5E-05	Errs cleared with re-write
74	500	75	StdByRad-Read	"	"	"	250	0	2756	"	57.2	3.00E+06	2.10E+04	3.97E-11		
75	505	75	StdByRad_Sleep/Wake/Read	"	"	"	420	0	2758	"	57.2	3.00E+06	2.20E+04	6.68E-11		Failures at 0x00 -> 0x07F Only
76	520	75	SEL	3.6	115C	533uA	607	0	1.80E-04	"	114.4	1.00E+07	5.00E+04	2.89E-11		All errs cleared with re-write
77	540	75	SEL	"	125C	802uA	548	0	18750	"	114.4	1.00E+07	4.40E+04	2.6E-11		24 jumps > 50mA, some to 154mA. 1 True latch to
78	558	79	StdByRad-Read	2	20.2C	81uA	16	0	2745	"	57.2	3.00E+06	4.10E+04	2.54E-12	0	Failures at 0x00 -> 0x04
79	603	79	StdByRad_Sleep/Wake/Read	"	"	"	507	0	2739	"	57.2	3.00E+06	4.40E+04	8.06E-11		Failures at 0x00 -> 0x07F Only
80	505	79	Countinuous READ CB	"	"	"	96	7	90	"	57.2	1.00E+05	2.33E+03	4.58E-10	7E-05	
81	512	79	Countinuous READ CB	"	"	"	162	7	128	"	81	1.00E+05	2.10E+03	7.72E-10	7E-05	
82	515	79	StdByRad-Read	"	"	"	14	0	3888	"	81	3.00E+06	4.60E+04	2.23E-12		All errs cleared on rewrite
83	519	79	StdByRad_Sleep/Wake/Read	"	"	"	500	0	3899	"	81	3.00E+06	3.88E+04	7.95E-11		Failures at 0x00 -> 0x07F Only
84	600	80	SEL	3.6	115C	6.3mA	28000	0	18340	"	114.4	1.00E+07	4.00E+04	1.34E-09		27 current jumps over 50mA - SUSPECT PART
85	740	79	SEL	3.6	115C	490uA					114.4	1.00E+07				1 current jump over 50mA.

Attachment B – CRÈME Analysis

CYRS15B102 (CREME96 Heavy ion upset data)

HUP for LET spectrum '7c1049_GEO_Solar_Min.let'

CYRS15B102.hup — Creme 96 Heavy Ion Upset File, 1Kb

File contents

```
15 CYRS15B102.HUP                                                          21010
%Created by CREME96:HI_UPSET_DRIVER Version  210 on  20210812 at 154555.4
%Input Integral LET Spectrum File: 7c1049_GEO_Solar_Min.let
%Created by CREME96:LETSPEC_DRIVER Version  210 on  20100727 at 212617.7
%ZMIN =  1 ZMAX = 92 LETMIN = 1.00E+00 LETMAX = 1.10E+05 MeV-cm2/g LBINS = 1002
%EMINCUT = 1.00E-01 MeV/nuc
%TARGET MATERIAL = SILICON
%Input File to LETSPEC_DRIVER: 7c1049_GEO_Solar_Min.tfx
%Created by CREME96:TRANSPORT_DRIVER Version  210 on  20100727 at 212526.2
%ZMIN =  1 ZMAX = 92  EMIN = 1.0000E-01 EMAX = 1.0000E+05 MeV/nuc  MBINS = 1002
%Thickness =   100.0000 mils      ALUMINUM
%Input File to TRANSPORT_DRIVER: input.flx
%Created by CREME96:FLUX_DRIVER Version  210 on  20100727 at 212417.0
%ZMIN =  1 ZMAX = 92
%IMODE  =   0 SOLAR-QUIET MODE: YEAR =  1977.0000
%ITRANS =   0 GEOSYNCH/NEAR-EARTH INTERPLANETARY FLUXES

 REPORT NO.    1:   CYRS15B102 T O D O
 RPP Dimensions: X =   89.40000  Y =   89.40000  Z =    2.00000 microns.
 Funnel length =    0.00000 microns.
 CROSS-SECTION INPUT   4  WEIBULL FIT:
     ONSET   =     2.500 MeV-cm2/milligram
     WIDTH   =    28.000 MeV-cm2/milligram
     POWER   =     1.900 (dimensionless)
     PLATEAU =  8000.000 square microns/bit
 Number of bits =   1.00000E+00
 Rates:      SEEs/bit/second     /bit/day    /device/second    /device/day
 *****   1     1.55279E-09     1.34161E-04     1.55279E-09     1.34161E-04
```

CYRS15B102 (CREME96 Heavy ion upset data)

HUP for LET spectrum 'ss_Worst_Day.let'

CYRS15B102.hup — Creme 96 Heavy Ion Upset File, 2Kb

File contents

```
20 CYRS15B102.HUP                                                          21010
%Created by CREME96:HI_UPSET_DRIVER Version  210 on  20210812 at 155209.9
%Input Integral LET Spectrum File: ss_Worst_Day.let
%Created by CREME96:LETSPEC_DRIVER Version  210 on  20111220 at 132934.8
%ZMIN =  1 ZMAX = 28 LETMIN = 1.00E+00 LETMAX = 1.10E+05 MeV-cm2/g LBINS = 1002
%EMINCUT = 1.00E-01 MeV/nuc
%TARGET MATERIAL = SILICON
%Input File to LETSPEC_DRIVER: ss_Worst_Day.tfx
%Created by CREME96:TRANSPORT_DRIVER Version  210 on  20111220 at 132839.3
%ZMIN =  1 ZMAX = 92  EMIN = 1.0000E-01 EMAX = 1.0000E+05 MeV/nuc  MBINS = 1002
%Thickness =   100.0000 mils      ALUMINUM
%Input File to TRANSPORT_DRIVER: ss_Worst_Day.flx
%Created by CREME96:FLUX_DRIVER Version  210 on  20111220 at 132732.5
%ZMIN =  1 ZMAX = 92
%IMODE  =   1 WORST-DAY SOLAR ENERGETIC PARTICLE MODEL
%ITRANS =   1 INSIDE MAGNETOSPHERE/NO TRAPPED FLUXES
%INPUT GEOMAGNETIC TRANSMISSION FILE: 7c1049_mem.gtf
%Created by CREME96:GTRANS_DRIVER Version  210 on  20100727 at 211855.6
%Incl =  51.600 deg  Apo = 0.4500E+03 Peri = 0.4500E+03 km   0.00   0.00   0.00
%ISTORM = 0 IPRECALC = 1  Grid Epoch = 1980.0   L Bin: 0.0000E+00 0.1000E+07
%Relative dwell time = 0.1000E+01

 REPORT NO.    1:   CYRS15B102 T O D O
 RPP Dimensions: X =   89.40000  Y =   89.40000  Z =    2.00000 microns.
 Funnel length =    0.00000 microns.
 CROSS-SECTION INPUT   4  WEIBULL FIT:
     ONSET   =     2.500 MeV-cm2/milligram
     WIDTH   =    28.000 MeV-cm2/milligram
     POWER   =     1.900 (dimensionless)
     PLATEAU =  8000.000 square microns/bit
 Number of bits =   1.00000E+00
 Rates:      SEEs/bit/second     /bit/day    /device/second    /device/day
 *****   1     6.26950E-08     5.41685E-03     6.26950E-08     5.41685E-03
%! WORST-DAY TOTAL =  4.063E-03 SEEs/bit =  4.063E-03 SEEs/device in 18 hours
```