EZ-PD™ PAG2S-PS integrated USB PD and synchronous-rectification controller

General description

EZ-PD™ PAG2S-PS CYPAS213 is an integrated secondary-side controller with USB Power Delivery controller and synchronous-rectifier. EZ-PD™ PAG2S-PS is targeted towards USB-C power adapters, it fits well into high-efficiency AC-DC flyback designs with USB Power Delivery, Qualcomm Quick Charge, and other standard charging protocols. EZ-PD™ PAG2S-PS also supports USB Power Delivery Extended Power Range (EPR) mode.

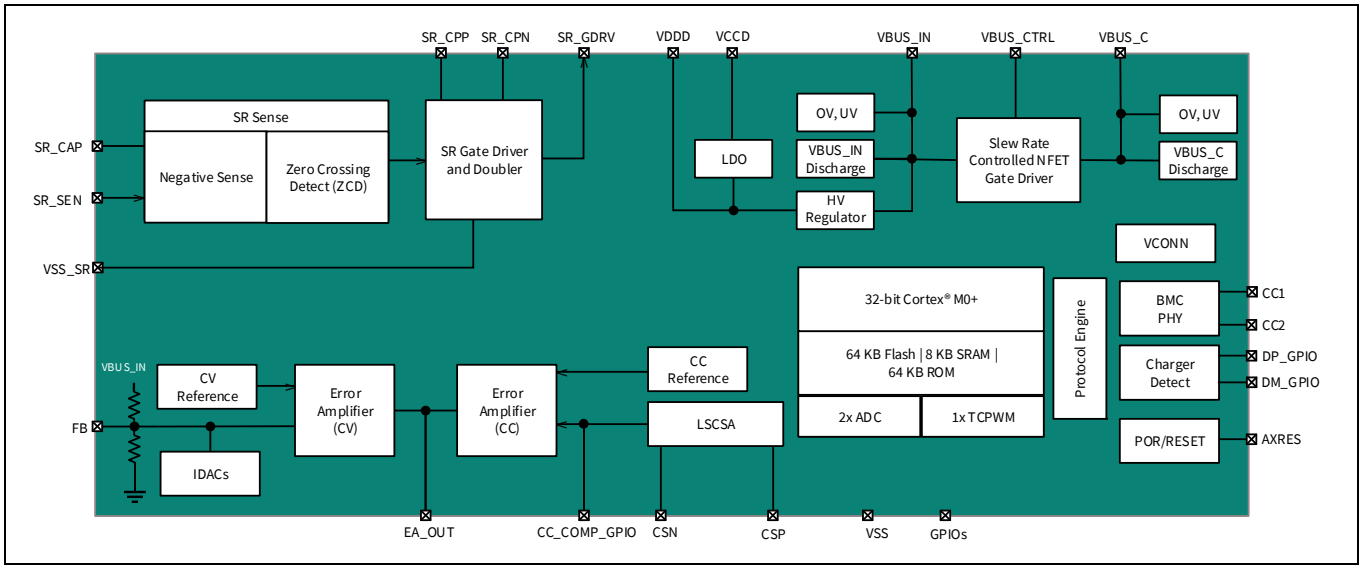
Applications

- USB-C chargers and adapters
- USB-C chargers and adapters with EPR
- Power adapters supporting both USB PD and legacy charging

Features

- Integrates secondary-side synchronous rectifier (SR) controller and charging port controller. SR controller has a turn-on propagation delay of typical 40 ns and a turn-off propagation delay of typical 25 ns.
- Supports synchronous rectification in quasi-resonant (QR), critical conduction mode (CrCM), discontinuous conduction mode (DCM), and continuous conduction code (CCM) and supports switching frequency up to 300 kHz
- SR driver works with both standard MOSFET and logic level MOSFET
- SR driver supports differentiation between primary turn-on versus resonance oscillation to avoid false turn-on of SR gate-driver
- USB PD 3.1 compliant with extended power range (EPR) support of up to 28 V VBUS
- Supports USB PD 2.0, PD 3.0 with programmable power supply (PPS), QC5.0, QC4+, QC 4.0, QC 3.0, QC 2.0, Samsung AFC, Apple Charging, and Battery Charging (BC) V1.2 charging protocols
- Integrates low-side current sense amplifier (LSCSA), 2x VBUS discharge FETs, and an NFET gate driver to drive the load switch and VCONN FETs to support EMCA cables
- Configurable VBUS overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), short-circuit protection (SCP), and system overtemperature protection (OTP)
- Protects against accidental VBUS to CC short; electrostatic discharge (ESD) protection on CC, VBUS, DP/DM lines, and overvoltage on DP/DM lines
- Integrates a 32-bit Cortex® M0+ with 64 KB flash, 8 KB SRAM, and 64 KB ROM
- 24-pin SOIC and 32-pin QFN packages with –40°C to +150°C junction temperature range

Functional block diagram



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1 Application overview

Figure 1 shows a power adapter application diagram implementing a primary side-controlled synchronous flyback system. In this system, EZ-PD™ PAG2S-PS engages the internal error amplifier (EA) to take the feedback from the secondary side and pass it on to the primary controller over an isolation barrier like an optoisolator. The primary side controller can be any standard flyback controller. In this topology, EZ-PD™ PAG2S-PS integrates three key features: secondary side rectification, charging protocol control, and fault protection.

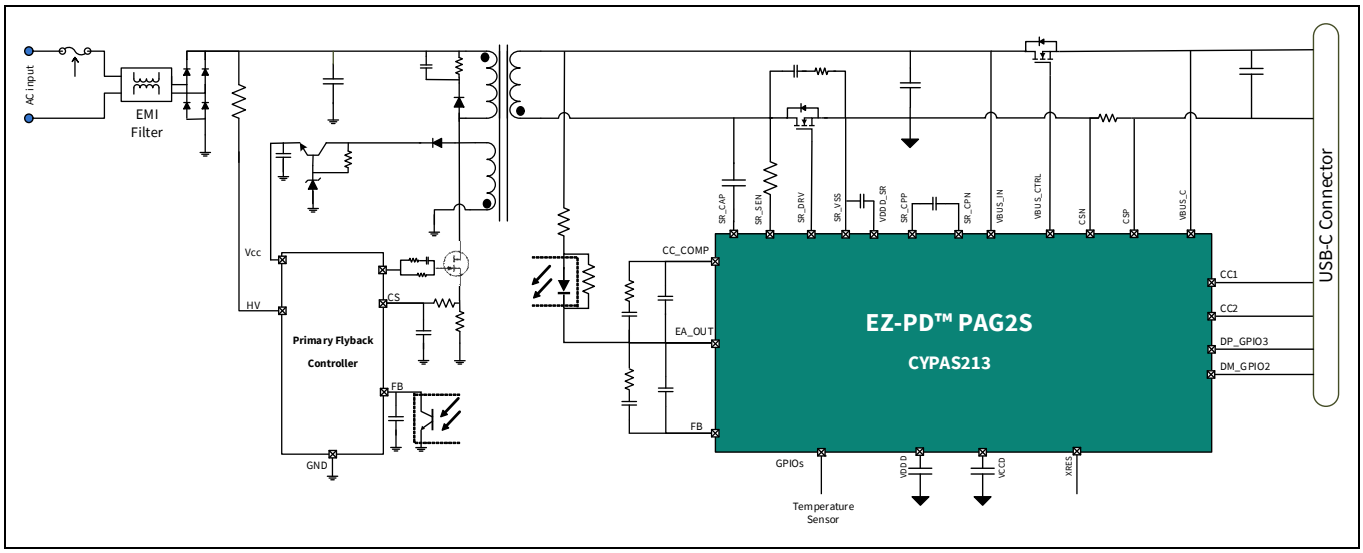


Figure 1 USB PD adapter with primary side flyback control

2 Pinouts

2.1 Pin definitions

Table 1 32-pin QFN pin description

Pin number	Pin name	Pin description
1	VCCD	1.8 V core voltage LDO output
2	VDDD	3.0 V to 5.5 V internal LDO output
3	VSS	Ground
4	VDDD_SR	V_{DDD} supply for sync rectifier driver
5	SR_CPN	Synchronous-rectification doubler capacitor negative pin
6	SR_CPP	Synchronous-rectification doubler capacitor positive pin
7	VSS_SR	Ground for sync rectifier driver
8	SR_GDRV	Synchronous-rectifier NFET gate driver
9	SR_SEN	Synchronous-rectifier NFET drain terminal sensing
10	SR_CAP	Synchronous-rectifier NFET high frequency sensing input for fast zero crossing detect (ZCD)
11	DNU	Do Not Use
12	GPIO0	GPIO
13	GPIO1	
14	DM_GPIO2	USB D–/GPIO/SWD_DAT
15	DP_GPIO3	USB D+/GPIO/SWD_CLK
16	GPIO4	Not connected
17	XRES	External reset input
18	GPIO5	GPIO
19	GPIO6	GPIO/TCPWM
20	GPIO7	GPIO
21	CC2	Power Delivery Communication Channel 2
22	CC1	Power Delivery Communication Channel 1
23	CSN	Low-side current sense amplifier negative input
24	CSP	Low-side current sense amplifier positive input
25	VBUS_C	USB Type-C VBUS monitor input
26	VBUS_CTRL	Load switch NFET gate control
27	EA_OUT	Error amplifier output
28	FB	Error amplifier feedback
29	CC_COMP_GPIO8	Pin for constant current mode compensation capacitor/GPIO/TCPWM
30	CC_COMP_GPIO9	
31	VSS	Ground
32	VBUS_IN	3.3 V to 30 V power source input for regulator

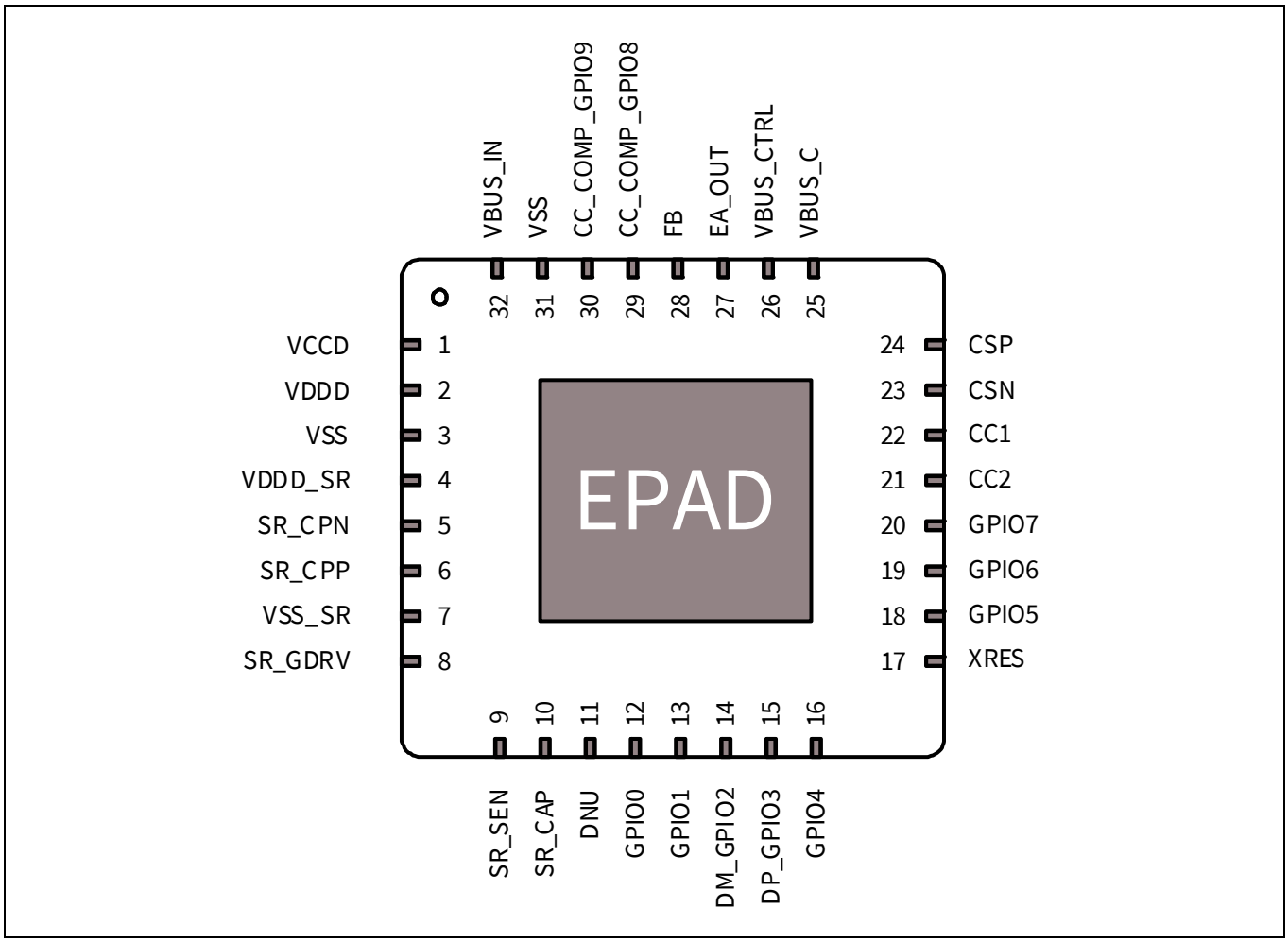


Figure 2 32-pin QFN pin map

Table 2 24-pin SOIC pin description

Pin number	Pin name	Pin description
1	CC_COMP_GPIO0	Compensation pin/GPIO/TCPWM
2	VBUS_IN	Power source input for regulator
3	VCCD	1.8 V core voltage LDO output
4	VDDD	3.0 V to 5.5 V internal LDO output
5	VSS	Ground
6	VDDD_SR	VDDD supply for sync rectifier driver
7	SR_CPN	Synchronous-rectification doubler capacitor negative pin
8	SR_CPP	Synchronous-rectification doubler capacitor positive pin
9	VSS_SR	Ground for sync rectifier driver
10	SR_GDRV	Synchronous-rectifier NFET gate driver
11	SR_SEN	Synchronous-rectifier NFET drain terminal sensing
12	SR_CAP	Synchronous-rectifier NFET high frequency sensing input for fast ZCD
13	DM_GPIO1	USB D–/GPIO/SWD_DAT
14	DP_GPIO2	USB D+/GPIO/SWD_CLK
15	GPIO3	External reset input/GPIO
16	CC2	Power Delivery Communication Channel 2
17	CC1	Power Delivery Communication Channel 1
18	CSN	Low-side current sense amplifier negative input
19	CSP	Low-side current sense amplifier positive input
20	VBUS_C	USB Type-C VBUS monitor input
21	VBUS_CTRL	Load switch NFET gate control
22	EA_OUT	Error amplifier output
23	FB	Error amplifier feedback
24	CC_COMP_GPIO4	Compensation pin/GPIO

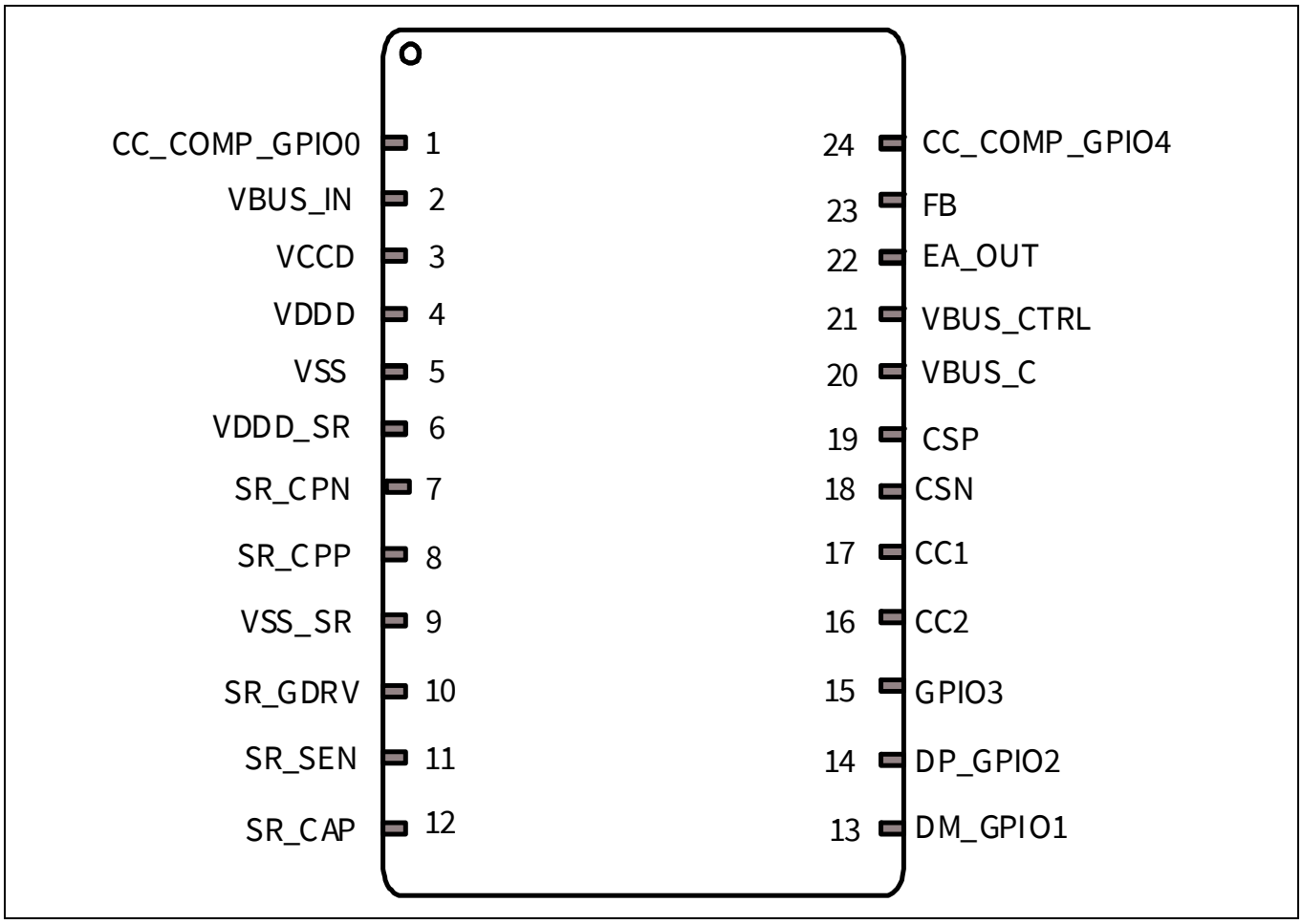


Figure 3 24-pin SOIC pin map

2.2 Pin description

2.2.1 SR_GDRV, SR_VSS, SR_SEN, SR_CPP, SR_CPN, SR_CAP

EZ-PD™ PAG2S-PS senses the voltage across the synchronous rectifier NFET and appropriately controls the gate driver to achieve optimum efficiency, it supports both standard NFET and logic level NFET. EZ-PD™ PAG2S-PS supports synchronous rectification in QR/CrCM, valley switching, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The SR sense block supports negative sense detect and ZCD. For CCM mode, fast detection of SR_DRAIN crossing 0 V is done via SR_CAP pin by coupling SR_DRAIN to SR_CAP via a 10 pF capacitor.

The gate driver (SR_GDRV) can be driven to internal VDDD or twice VDDD to achieve lower RDS-On of the external NFET. The Gate Driver can be driven to twice of VDDD using an internal doubler circuit, with the doubler capacitor connected across SR_CPP and SR_CPN pins. The source terminal of the SR FET shall be connected to the SR_VSS pin. SR block implements an adaptive voltage doubler, wherein the voltage doubler feature is enabled or disabled on-the-fly based on the SR_GDRV pulse width and a configurable firmware parameter. The voltage at the drain node of the external NFET is sensed via SR_SEN using a resistive divider.

2.2.2 FB, EA_OUT, CC_COMP_GPIOx

EZ-PD™ PAG2S-PS integrates two error amplifier blocks that handle secondary output sensing and feedback for both constant voltage and constant current modes of operation. The error amplifier output can be used to regulate the current drawn through the external optocoupler. The negative input of the error amplifier is the feedback (FB) pin and the positive input is an internal voltage reference. Based on the desired VBUS output, the voltage at the FB pin will be varied using internal current source/sink IDACs. An external compensation network is required between the FB pin and EA_OUT pin, as shown in the application diagram (see **Figure 1**). The constant current operation makes use of an internal low-side current sense amplifier (LSCSA), the output of which feeds into an independent error amplifier as shown in the functional block diagram. Constant current mode regulation requires an external compensation network between CC_COMP_GPIOx and EA_OUT as shown in **Figure 1**. EZ-PD™ PAG2S-PS error amplifier can ensure constant voltage regulation from 3.3 V to 28 V range and constant current regulation from 1 A to 5 A as required by the USB PD PPS EPR specification.

2.2.3 VBUS_IN, VDDD, VCCD

EZ-PD™ PAG2S-PS integrates a high-voltage regulator, which is powered from the VBUS_IN rail, the output of the regulator powers the VDDD rail. The input to the regulator can range from 3.3 V minimum to 30 V maximum. This regulator is intended to deliver EZ-PD™ PAG2S-PS current consumption and is not expected to drive any external loads or ICs. EZ-PD™ PAG2S-PS also has an internal configurable discharge path for the VBUS_IN rail, which is used to discharge the VBUS rail during negative voltage transitions. The discharge resistor strength is configurable through firmware settings.

The regulated supply VDDD is either used to directly power some internal analog blocks or further regulated down to 1.8 V VCCD, which powers the majority of the core. VDDD and VCCD are brought out onto pins to connect external capacitors for regulator stability and these are not meant to be used as power supplies.

2.2.4 VBUS_C, VBUS_CTRL

VBUS_C is used to monitor the voltage at the Type-C connector. VBUS_C has an internal configurable discharge path, which is used to discharge the VBUS_C rail during negative voltage transitions. The discharge resistor strength is configurable through firmware settings. The load switch is between VBUS_IN and VBUS_C. EZ-PD™ PAG2S-PS integrates an NFET gate driver to control this load switch. VBUS_CTRL is the output of this gate driver. There is an optional slow turn-on feature which is meant to avoid the sudden in-rush current.

2.2.5 CSP, CSN

EZ-PD™ PAG2S-PS integrates a low-side current sense amplifier (LSCSA) to monitor the load current. CSP is the positive input pin for the LSCSA and CSN is the negative input. Suggested Rsense for LSCSA is 5 mΩ.

2.2.6 CC1, CC2

CC1 and CC2 are the communication channels for the USB PD protocol. EZ-PD™ PAG2S-PS integrates a USB PD transceiver consisting of a transmitter (TX) and receiver (RX) that communicate Biphase Mark Code (BMC) encoded data over the Configuration Channel (CC) channels as per the USB PD standard. All communication is half-duplex. The physical layer implements collision avoidance to minimize communication errors on the channel. This block includes all termination resistors (Rp) and their switches as required by the USB PD specification.

To support active cable applications, EZ-PD™ PAG2S-PS also integrates VCONN FETs to power CC lines. An external 390-pF capacitor is required on both the CC1 and CC2 pins.

2.2.7 DP_GPIOx, DM_GPIOx

The DP and DM lines are the standard USB D+ and D– lines. EZ-PD™ PAG2S-PS integrates a charge detect block, which handles legacy charging protocols such as BC 1.2, Quick Charge, Apple Charging, and Samsung AFC. This block integrates all the terminations required for these charging protocols and no external components are required. When legacy charging is not required in the system, the same DP and DM lines can be re-used as standard GPIOs. Charger detect block also supports impedance detection on DP/DM lines.

2.2.8 GPIOx, XRES

EZ-PD™ PAG2S-PS has multiple GPIOs, out of which some are dedicated GPIOs and the rest are multiplexed with other functionalities. These GPIOs support multiple drive modes and configurable threshold options. During power-on and reset, the GPIOs are forced to the tristate so as not to crowbar any inputs and/or cause excess turn-on current.

The XRES pin can be used to initiate a reset, this pin is internally pulled high and needs to be pulled low externally to trigger a reset.

3 Functional description

3.1 Modes of operation - SR

EZ-PD™ PAG2S-PS supports synchronous rectification in both DCM and CCM modes. The SR sense block supports negative sense detect and ZCD. **Figure 4**, **Figure 5**, and **Figure 6** show SR_GDRV functionality in QR/CrCM, valley switching, and CCM modes. SR controller has a turn-on propagation delay of typical 40 ns and a turn-off propagation delay of typical 25 ns.

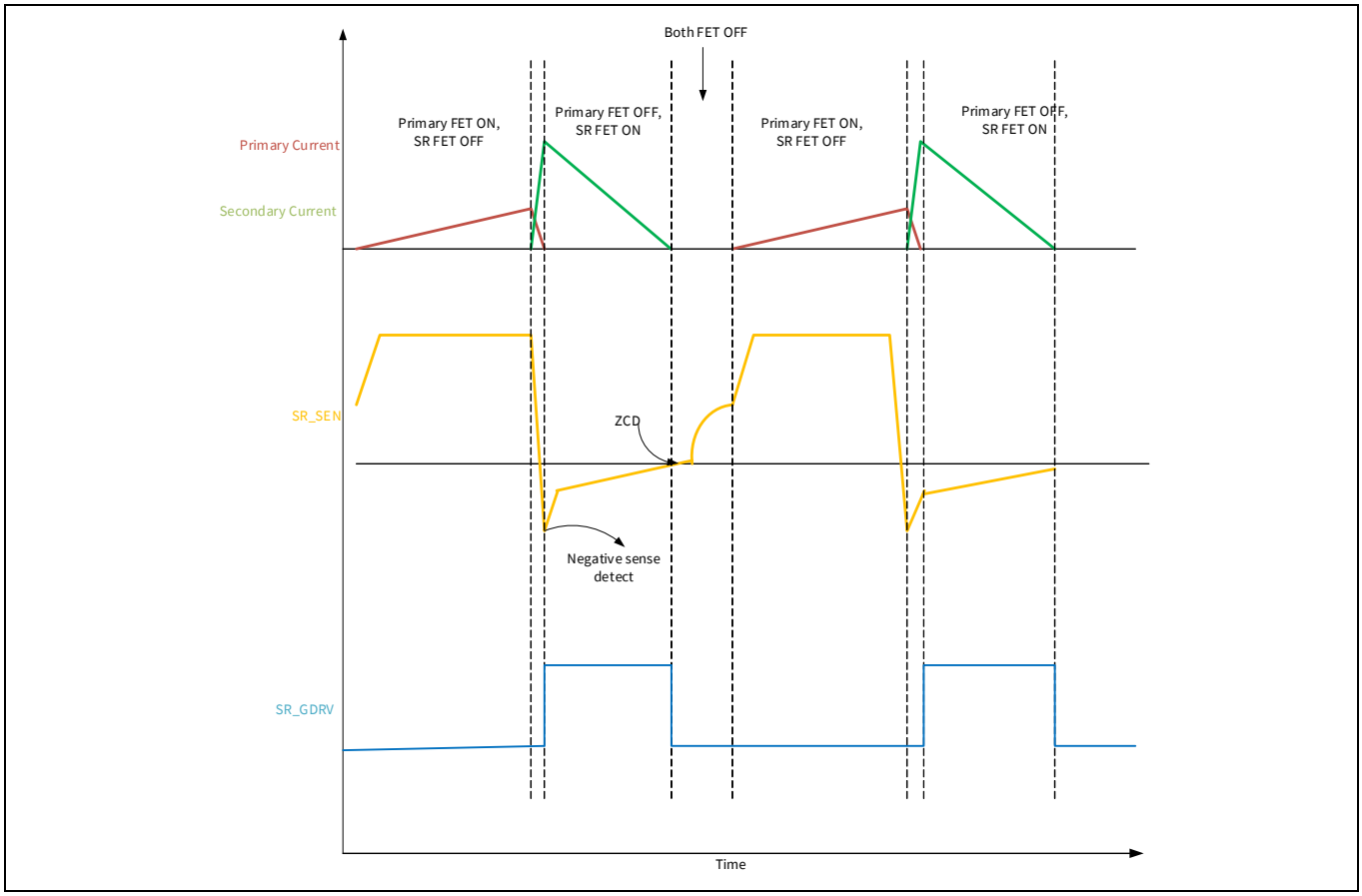


Figure 4 SR_SEN and SR_GDRV in QR/CrCM mode

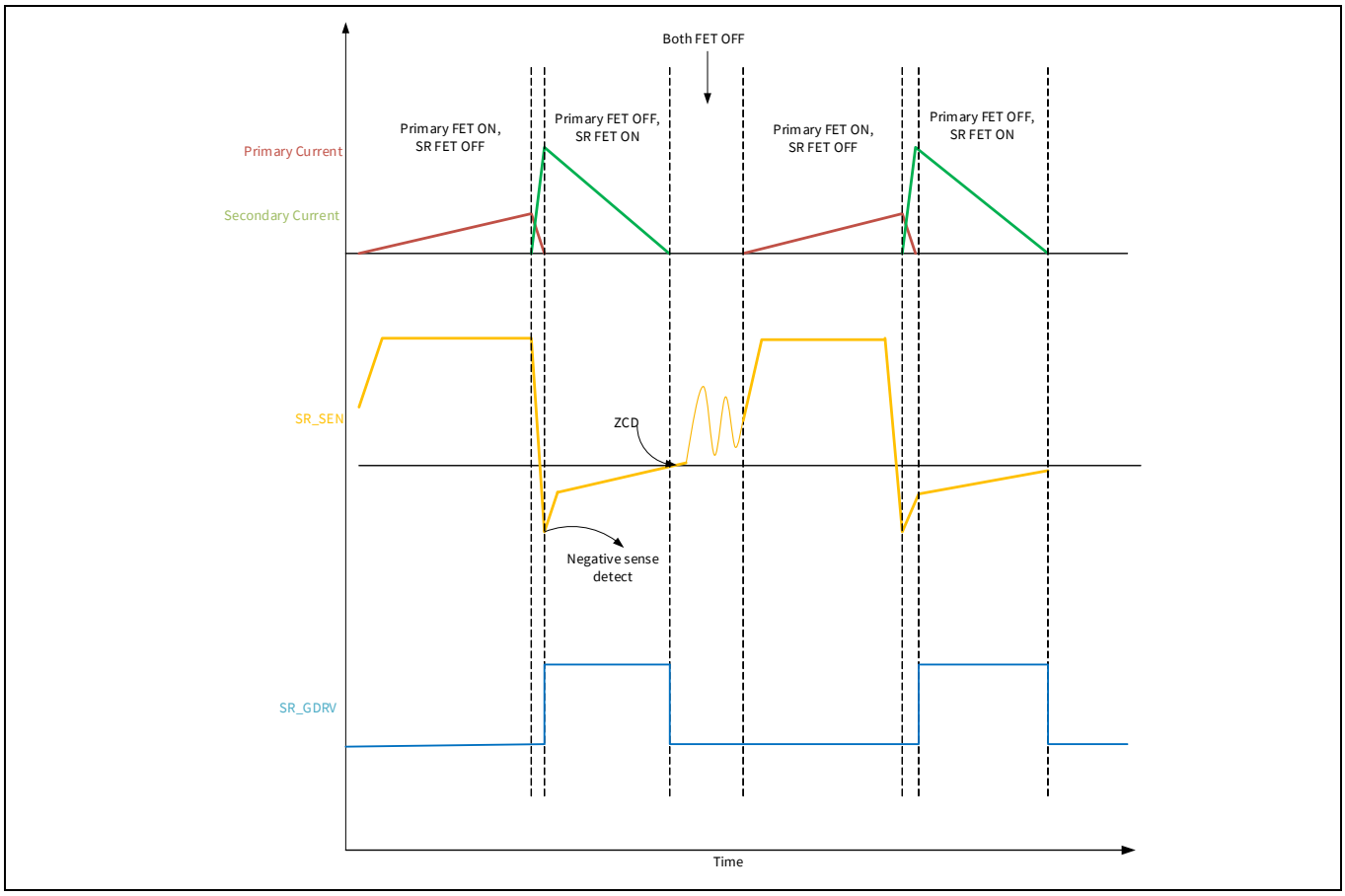


Figure 5 SR_SEN and SR_GDRV in DCM/Valley switching mode

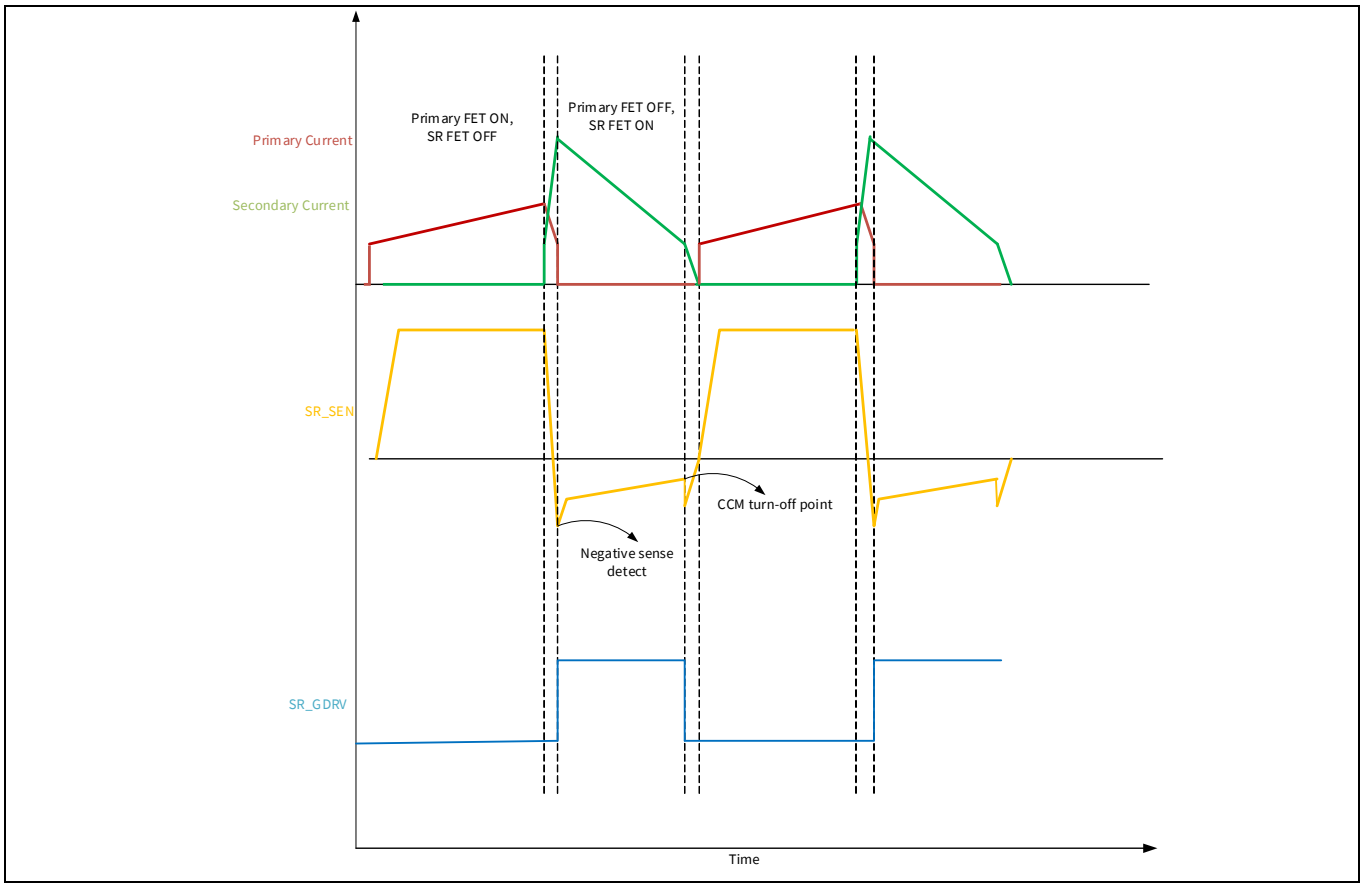


Figure 6 SR_SEN and SR_GDRV in CCM mode

The voltage at the drain node of the external NFET is sensed on the SR_SEN pin connected via an external resistor. The external resistor is needed to restrict voltage at the SR_SEN pin below 34 V. The external resistance on the SR_SEN pin depends on the turns ratio of the power transformer. **Table 3** provides the external resistor values required for different turns ratio.

Table 3 External resistance on SR_SEN vs turns ratio

Primary: Secondary turns ratio	Rext (Ohms)
3:1	20k
4:1	20k
5:1	20k
6:1	12k
7:1	12k
8:1	12k
9:1	12k
10:1	12k
11:1	12k
12:1	12k
13:1	12k
14:1	12k
15:1	12k

3.1.1 SR_SEN false negative sense detection

The SR sense block monitors for the negative sense detect to turn on SR_GRDV. There is a chance of a false negative sense detect during secondary resonance. To avoid this, EZ-PD™ PAG2S-PS implements a proprietary voltage-second balance mechanism. In this mechanism, the SR block does an integral of the SR_SEN voltage once it crosses the VBUS level and compares this voltage against an internal reference. **Figure 7** shows that the negative sense is considered valid only when the SR_SEN integral voltage crosses the reference voltage. The reference voltage is firmware configurable and can be modified as needed based on system parameters.

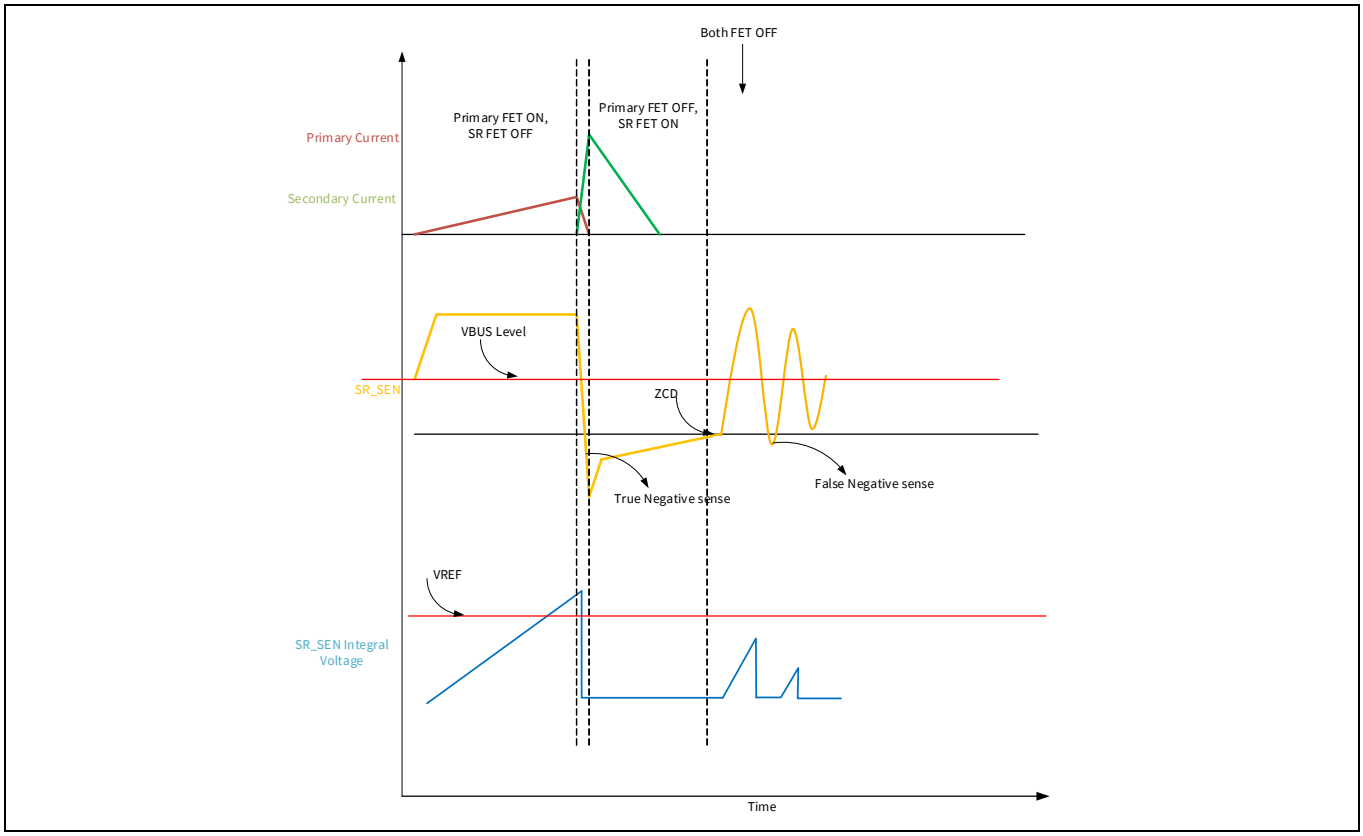


Figure 7 SR_SEN negative sense detection

3.2 Fault protection

3.2.1 VBUS OVP, UVP, OCP, and SCP

VBUS undervoltage and overvoltage faults are monitored using internal VBUS_IN/VBUS_C resistor dividers. VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers. The fault thresholds and response mechanisms are firmware configurable.

3.2.2 OTP

Over-temperature monitoring is done using an external thermistor and internal ADC. The thermistor can be connected to any free GPIO. EZ-PD™ PAG2S-PS has integrated 8-bit SAR ADC, this is available for general purpose analog to digital conversions. The fault thresholds and response mechanisms are firmware configurable.

3.2.3 ESD, CC OVP, and DP/DM OVP

EZ-PD™ PAG2S-PS offers ESD protection on all the pins. Further, the chip integrates protection against accidental short of CC pins to high voltage VBUS_C rail and also protects against over-voltage on DP/DM pins.

3.3 Power modes

EZ-PD™ PAG2S-PS supports multiple power modes - Active, Sleep, and DeepSleep. Transitions between these modes is handled by the application firmware depending on the operating conditions.

3.4 MCU subsystem

EZ-PD™ PAG2S-PS integrates a 32-bit Cortex®-M0+ MCU with 64KB flash, 8 KB SRAM, and 64 KB ROM. EZ-PD™ PAG2S-PS also supports 1x TCPWM and 2x ADC.

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

Parameter	Description	Min	Typ	Max	Unit
$V_{BUS\_IN\_MAX}$	Maximum input supply voltage	–0.3	–	34	V
V_{DDD_MAX}	V_{DDD} supply voltage	–		6	
V_SR_DRAIN_MAX	Voltage on SR_SEN pin			34	
$V_{CC\_PIN\_ABS}$	Voltage on CC1, CC2 pins				
V_{GPIO_ABS}	GPIO voltage	–0.5		V_{DDD} + 0.5	
I_{GPIO_ABS}	Current per GPIO	–		25	mA
I_LU	Pin current for latch-up	–100		100	
ESD_HBM	Electrostatic discharge human body model	–		2000	V
ESD_CDM	Electrostatic discharge charged device model			500	

4.2 Device-level specifications

Table 5 Device-level specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Memory size						
FLASH_SIZE	Flash memory size	–	64	–	KB	SONOS Flash amount (bytes)
SRAM_SIZE	SRAM memory size		8			SRAM amount (bytes)
SROM_SIZE	SROM memory size		64			
Silicon power						
VDDD_REG	VDDD output with VBUS 5.5 V to 30 V	4.6	5	5.4	V	–
VDDD_MIN	VDDD output with VBUS 3.15 V to 5.5 V	VBUS – 0.33	–	–		
VBUS_IN	Power supply input voltage	3.15		30.0		
VCCD	Output voltage for core logic	–	1.8	–		
VDDWRITE	Supply voltage for flash write	3	–	5.5		
Cefc	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic or better
Cexc	Power supply capacitor for VDDD	4	4.7	–	µF	
Cexv	Power supply decoupling capacitor for VBUS_IN	–	1			
Cexcpp	Capacitor between SR_CPP and SR_CPN pins	0.1	–			
Igpio_abs	Current per GPIO	–		25	mA	Absolute maximum

Table 5 Device-level specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Tsleep	Wakeup from Sleep mode		0		µs	–
Tdeepsleep	Wakeup from Deep Sleep mode		35			–
IDD_A	Active current from VBUS_IN (Type-C Attached)		25.0			VBUS_IN = 11 V, TA = 25°C, CC1/CC2 in Tx or Rx, CPU at 24 MHz, SR/PWM at 100 kHz EA/ADC/CSA/UVOV blocks ON
IDD_A2	Current from VBUS_IN (Type-C attached) in SR mode	–	9.0	–	mA	VBUS_IN = 28 V, TA = 25°C, Clock at 12 MHz, SR at 100 kHz, SR Cap = 3 nF, No toggling on CC
IDD_A4	Current from VBUS_IN (Type-C attached) in Low power SR mode		3			VBUS_IN = 28 V, TA = 25°C, Deep Sleep, SR mode, No toggling on CC
IDD_DS2_UA	Deep Sleep current from VBUS_IN (Type-C unattached) in SR mode		400		µA	VBUS_in = 5 V, TA = 25°C, Type-C unattached, SR mode, DFP mode
L_SEC	Secondary side inductor	3	–		µH	Secondary side inductor

4.3 Functional block specifications

Table 6 Functional block specifications

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Synchronous rectifier						
VCPP1	Voltage doubler output voltage with VBUS = 3.3 V–5.5 V	5	–	–	V	–
VCPP2	Voltage doubler output voltage with VBUS = 5.5 V–30 V	9		11		
TR_SR	Rise time (1 V to VOH – 1 V) of sync-rectifier gate driver output with CL = 3nF, including (with and without double bypass mode)	–		75	ns	
TF_SR1	Fall time (VOH – 1 V to 1 V) of sync-rectifier gate driver output with CL = 3 nF, (with doubler mode)		25	50		
TF_SR2	Fall time (VOH – 1 V to 1 V) of sync-rectifier gate driver output with CL = 3 nF, (with doubler bypass mode)		15	30		
VTRIP_NSN_100	Negative sense trip voltage to turn-ON secondary switch	50	100	150	mV	
VTRIP_ZCD	Negative sense trip voltage to turn-OFF secondary switch	–8	–5	–3		
VTRIP_ZCDF	Trip voltage to turn-OFF secondary switch through Fast ZCD	0	7	10		
TD_ON	Turn on propagation delay from SR_DRAIN at 100 mV to SR_GDRV reaching 1 V	–	40	80	ns	
TD_OFF	Turn off propagation delay from SR_DRAIN step change (from –50 mV to +300 mV in 5 ns) to SR_GDRV output reaching VOH – 1 V.	–	25	40		
IO_SRC_SNK	Output peak current (Source and sink)	–	1	–	A	

Table 6 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
TR_SR1	Rise time (1 V to VOH – 1 V) of sync-rectifier gate driver output with CL = 3 nF, including (with doubler mode)	–	–	75	ns	–
TR_SR2	Rise time (1 V to VOH – 1 V) of sync-rectifier gate driver output with CL = 3 nF, including (with doubler bypass mode)	–	–	30	ns	
GPIO						
I_LU	Latch up current limits	–100	–	100	mA	–
RPU	Pull-up resistor value	3.5	5.6	8.5	kΩ	
RPD	Pull-down resistor value					
IIL	Input leakage current (Absolute value)	–	–	2	nA	+25°C TA, 3 V VDDD
CPIN_A	Max pin capacitance			22	pF	Capacitance on DP, DM pins
CPIN	Max pin capacitance		3	7		All VDDD, all other GPIOs
Voh	Output voltage high level	VDDD – 0.6	–	–	V	Ioh = -4 mA
Vol	Output voltage low level	–		0.6		Iol = 10 mA
Vih_CMOS	Input voltage high threshold	0.7 × VDDD		–		–
Vil_CMOS	Input voltage low threshold	–		0.3 × VDDD		
Vih_TTL	LVTTL input	2		–		
Vil_TTL	LVTTL input	–		0.8		
Vhysttl	Input hysteresis LVTTL	80	–	–	mV	
Vhyscmos	Input hysteresis CMOS	0.1 × VDDD				
IDIODE	Current through protection diode to VDDD/VSS	–		100	µA	
TriseF	Rise time in Fast Strong mode	1		15	ns	Cload = 25 pF
TfallF	Fall time in Fast Strong mode			15		–
TriseS	Rise time in Slow Strong mode	10		70		
TfallS	Fall time in Slow Strong mode					

Table 6 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
FGPIO_OUT1	GPIO Fout; 2.85 V ≤ VDDD ≤ 5.5 V. Fast Strong mode.	–	–	28	MHz	–
FGPIO_OUT2	GPIO Fout; 2.85 V ≤ VDDD ≤ 5.5 V. Slow Strong mode.			6		
FGPIO_IN	GPIO input operating frequency; 2.85 V ≤ VDDD ≤ 5.5 V			28		
Flash macro						
FLASH_ERASE	Row erase time	–	–	15.5	ms	–
FLASH_WRITE	Row (Block) write time (Erase and program)			20		
FLASH_DR	Flash data retention	15		–	Years	25°C to 55°C, all VDDD
FLASH_ENPB	Flash write endurance	100K			Cycles	25°C to 85°C, all VDDD
FLASH_ENPB1	Flash write endurance	10K				25°C to 125°C, all VDDD
FLASH_ROW_PGM	Row program time after erase	–		7	ms	–
TBULKERASE	Bulk erase time (32KB)	–		35		
TDEVPROG	Total device program time	–		7.5	s	
FRET1	Flash retention, TA ≤ 55°C, 100K P/E cycles	15		–	Years	
FRET2	Flash retention, TA ≤ 85°C, 10K P/E cycles	10				
FRET3	Flash retention, TA ≤ 105°C, 10K P/E cycles	3				
SWD						
F_swdclk1	All VDDD	–	–	14	MHz	–
T_swdi_setup	T = 1/f SWDCLK	0.25 × T		–	ns	
T_swdi_hold						
T_swdo_valid		–		0.50 × T		
T_swdo_hold		1		–		
ILO / IMO / POR						
FIMO	IMO frequency	24	36	48	MHz	–
IMO_STL	IMO settling time when trim register is changed	–	–	200	ns	25°C TA, All VDDD, 48 MHz ≥ FIMO ≥ 24 MHz
FCPU	CPU input frequency			48	MHz	–
FILO	ILO frequency	15	40	80	kHz	

Table 6 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SR_POWER_UP	Power supply slew rate during power up	–		67	V/ms	
Fimotol	Frequency variation at 24 and 48 MHz (trimmed)	–2		2	%	
TSTARTIMO	IMO start-up time			7	µs	
TSTARTILO1	ILO start-up time	–		2	ms	
EXTCLKFREQ	External clock input frequency			16	MHz	
EXTCLKDUTY	Duty cycle; measured at VDD/2	45	–	55	%	–
TCLKSWITCH	System clock source switching time	3		4	Periods	
$V_{RISEIPOR}$	Power-on-reset (POR) rising trip voltage	0.72		1.5	V	
$V_{FALLIPOR}$	Power-on-reset (POR) falling trip voltage	0.62		1.4		
VDDD_BOD	Brown-out-detect (BOD) trip voltage active/ sleep modes	2.34		3		
VCCD_BOD		1.64		2		
VCCD_BOD_DPSLP		1.1		2		
Timer						
SYS_TIM_RES	Sys timer resolution	–	16	–	bits	–
WDT_RES	Watchdog timer resolution		16		bits	
TCPWM						
TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS
TPWMEXT	Output trigger pulse widths	2/Fc		–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
TCRES	Resolution of counter	1/Fc				Minimum time between successive counts
PWMRES	PWM resolution					Minimum pulse width of PWM output
PD transceiver						
vSwing	Transmitter output high voltage	1.05	–	1.2	V	–
vSwing_low	Transmitter output low voltage	–		0.075		
zDriver	Transmitter output impedance	33		75	Ω	

Table 6 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Idac_std	Source current for USB standard advertisement	64		96	µA	
Idac_1p5a	Source current for 1.5 A @ 5 V advertisement	166		194		
Idac_3a	Source current for 3 A @ 5 V advertisement	304		356		
zOPEN	CC impedance to ground when disabled	108		–	kΩ	
DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15	–	0.25	V	–
DFP_1.5A_0p4	CC voltages on DFP side - 1.5 A	0.35		0.5		
DFP_3A_0p8	CC Voltages on DFP side - 3 A	0.75		0.85		
DFP_3A_2p6	CC voltages on DFP side - 3 A	2		2.75		
Vattach_ds	Deep sleep attach threshold	0.30		0.6	–	
Rattach_ds	Deep sleep pull-up resistor	10		50	kΩ	
LS-CSA DC specifications						
Csa_Acc1	CSA accuracy with 5 mV < Vsense < 10 mV	–0.75	–	0.75	mV	–
Csa_Acc2	CSA accuracy with 10 mV < Vsense < 15 mV					
Csa_Acc3	CSA accuracy with 15 mV < Vsense < 25 mV					
Csa_Acc4	CSA accuracy with Vsense = 50 mV					
SCP_6A	Short circuit current detect @ 6 A	5.4	6	6.6	A	
SCP_10A	Short circuit current detect @ 10 A	9	10	11		
SCP_20A	Short circuit current detect @ 20 A	18	20	22		
OCP Threshold	OCP Trip with 5 mΩ and current > 4 A	117	130	143	%	
Av	Nominal gain values supported: 40, 60	30	–	60	V/V	

Table 6 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
LS-CSA AC specifications						
Tscp_gate	Delay from SCP threshold trip to external NFET power gate turn off	–	2.5	–	µs	1nF NFET gate capacitance, VBUS_IN = 28 V
Tscp_gate_1			7.5			3nF NFET gate capacitance, VBUS_IN = 28 V
UVOV						
VTHOV	Over-voltage threshold accuracy, 4 V to 30 V	–3	–	3	%	–
VTHUV1	Under-voltage threshold accuracy, 3 V to 4 V	–4		4		
VTHUV2	Under-voltage threshold accuracy, 4 V to 30 V	–3		3		
VBUS gate driver DC specs						
GD_VGS	Gate to source overdrive during ON condition	5	–	10	V	NFET driver is ON
GD_Rpd	Resistance when pull-down enabled	–		2	KΩ	Applicable on VBUS_CTRL to turn-off external NFET
GD_drv	Programmable typical gate current	0.3		9.75	µA	Gate driver output current
VBUS gate driver AC specs						
Ton	VBUS_ctrl Low to High (1 V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	VBUS_in = 5 V
Toff	VBUS_ctrl High to Low (90% to 10%) with 3 nF external capacitance	–	7.5	–	µs	VBUS_in = 28 V
VBUS discharge						
R1	NMOS ON resistance for DS = 1 on VBUS_IN	1000	–	4000	Ω	Measured at 0.5 V
R2	NMOS ON resistance for DS = 2 on VBUS_IN	500		2000		
R4	NMOS ON resistance for DS = 4 on VBUS_IN	250		1000		
R8	NMOS ON resistance for DS = 8 on VBUS_IN	125		500		
R16	NMOS ON resistance for DS = 16 on VBUS_IN	62.5		250		
R32	NMOS ON resistance for DS = 32 on VBUS_IN	31.25		150		

Table 6 Functional block specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Vbus_stop_error	Error percentage of final VBUS value from setting	–	–	10	%	When VBUS is discharged to 5 V
R1A	NMOS ON resistance for DS = 1 on VBUS_C	1000		2000	Ω	Measured at 0.5 V
R127A	NMOS ON resistance for DS = 127 on VBUS_C	6.5		38		
Voltage regulation DC specifications						
VOUT	Typical VBUS_IN output voltage range	3.3	–	28	V	–
VR	VBUS voltage regulation accuracy	–	±3	±5	%	
Ika_off	Off-state cathode current		2.2	10	µA	
Ika_on	Current through EA_OUT pin when in sink mode for optocoupler application		–	5	mA	
VBUS regulator specifications						
VOLTAGE_DETECT	Voltage detect threshold voltage on VBUS_IN	1.65	2.1	2.4	V	–
Tstart	Total startup time for the regulator supply outputs with 4.7 µF load capacitance	–	50	200	µs	
ADC DC specifications						
Resolution	ADC resolution	–	8	–	bits	–
INL	Integral non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
INL	Integral non-linearity	–1.5		1.5		Reference voltage generated from bandgap
VREF_ADC1	Reference voltage of ADC	VDDDmin		VDDDmax	V	Reference voltage generated from VDDD
VREF_ADC2		1.96	2	2.04		Reference voltage generated from bandgap
VCONN switch specifications						
VCONN_OUT	VCONN minimum output voltage with 20 mA load current with Vbus = 5 V–30 V	4.5	–	–	V	–
Ileak	Connector side pin leakage current	–		10	µA	

Table 6 Functional block specifications *(continued)*

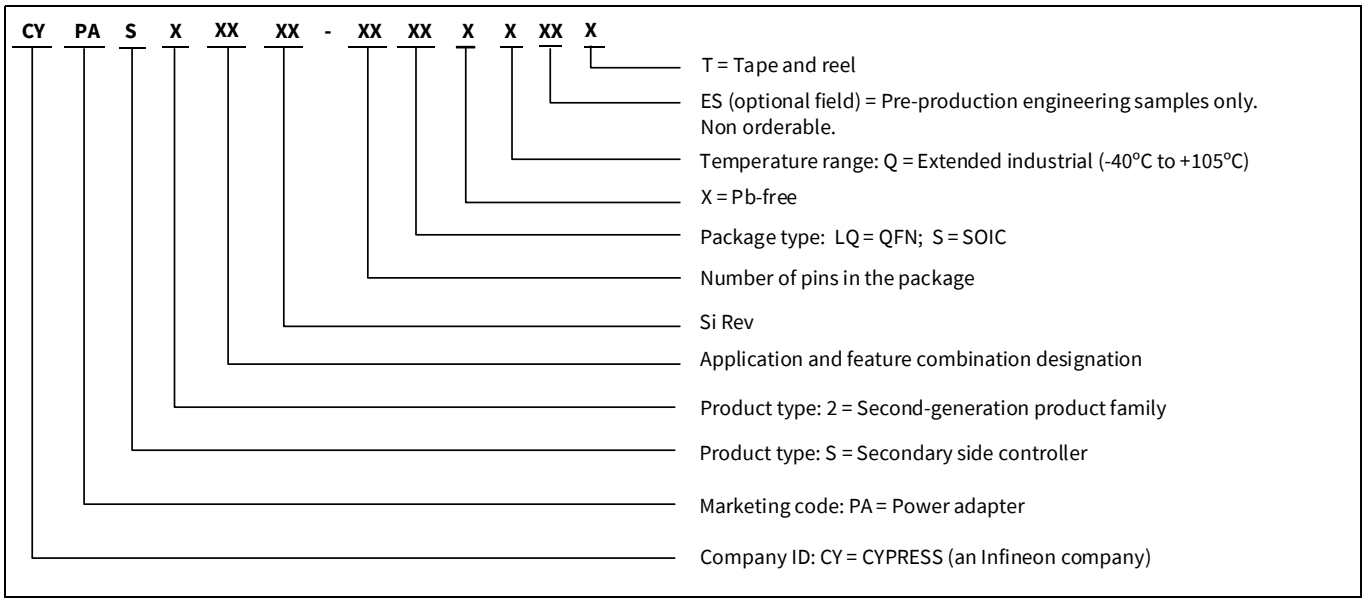
Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VCONN switch AC specifications						
Ton	Switch turn-on time	–	–	600	µs	–
Toff	Switch turn-off time			10		

5 Ordering information

Table 7 EZ-PD™ PAG2S-PS ordering information

MPN	Application	Package type	Si ID	Si Rev
CYPAS213A1-24SXQ	USB PD adapter - Primary side flyback control	24-pin SOIC	3B02	A1
CYPAS213A1-24SXQT				
CYPAS213A1-32LQXQ		32-pin QFN	3B12	
CYPAS213A1-32LQXQT				

5.1 Ordering code definitions



6 Packaging

Table 8 Package characteristics

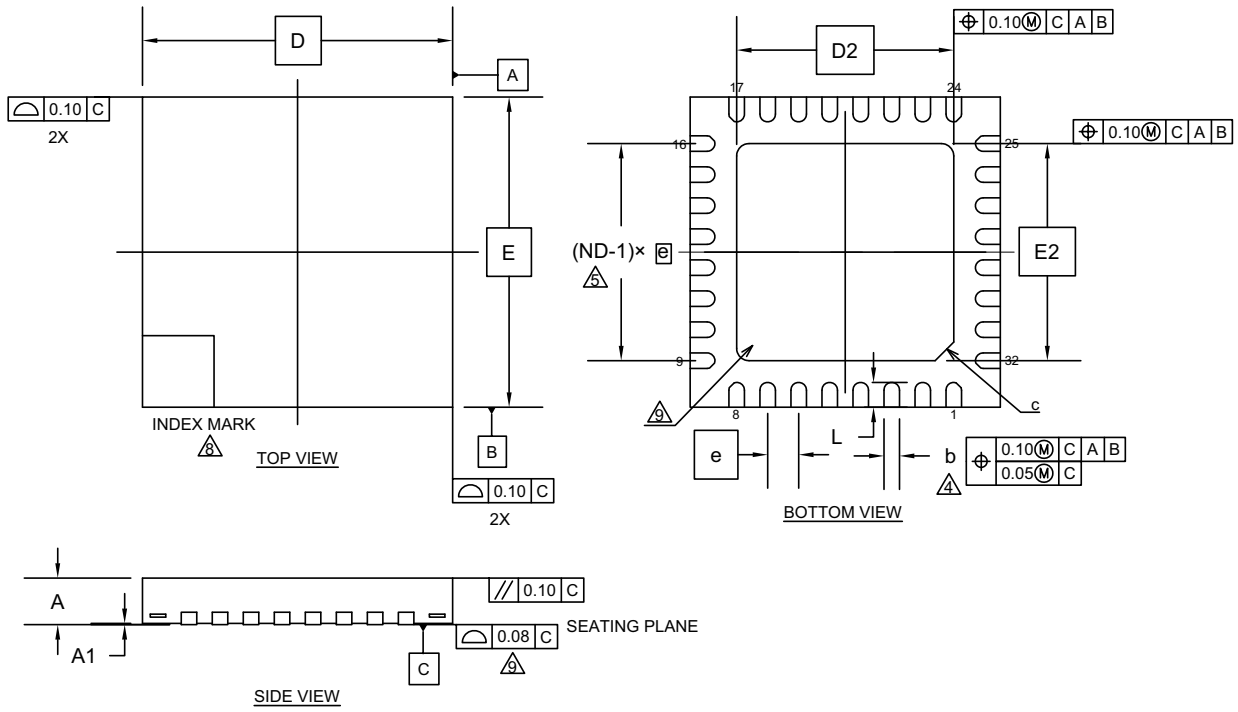
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Extended industrial	–40	–	105	°C
T_J	Operating junction temperature				150	
T_{JA}	Package Theta-JA for 32-pin QFN	–	–	23.4	–	°C/W
T_{JA}	Package Theta-JA for 24-pin SOIC			68.9		
T_{JB}	Package Theta-JB for 32-pin QFN			4.85		
T_{JB}	Package Theta-JB for 24-pin SOIC			64.1		
T_{JC}	Package Theta-JC for 32-pin QFN			27.2		
T_{JC}	Package Theta-JC for 24-pin SOIC			35.6		

Table 9 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
24-pin SOIC	260°C	30 seconds
32-pin QFN		

Table 10 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin SOIC	MSL3
32-pin QFN	



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.80
A_1	0.00	——	0.05
D	5.00 BSC		
E	5.00 BSC		
b	0.18	0.25	0.30
D_2	3.50 BSC		
E_2	3.50 BSC		
e	0.50 BSC		
c	0.30 REF		
L	0.35	0.40	0.45

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF : N/A

002-15160 Rev. **

Figure 8 32-lead QFN ((5.0 × 5.0 × 0.8 mm) WNP032 3.5 × 3.5 mm E-pad (Sawn)) package outline (PG-VQFN-32), 002-15160

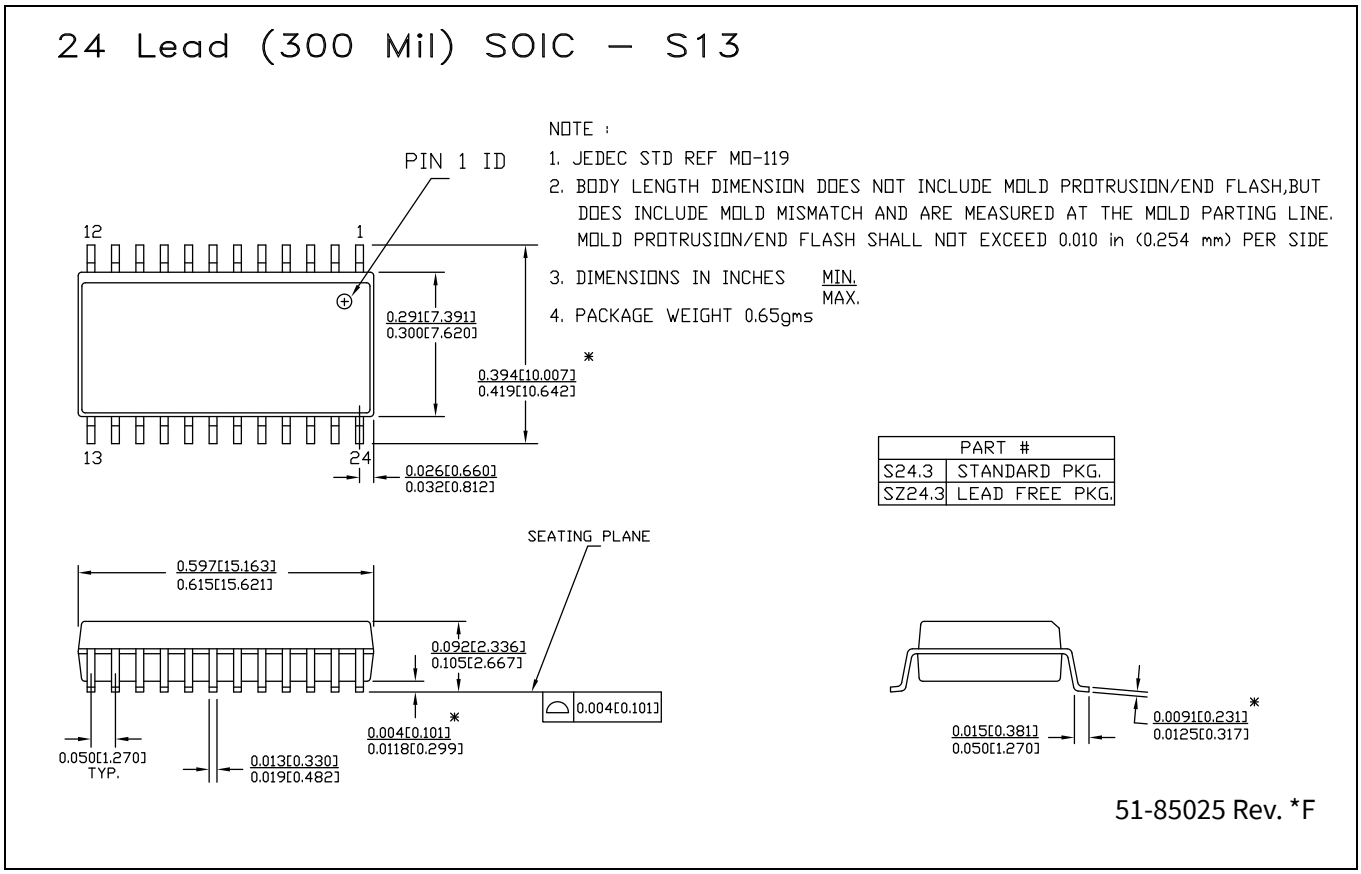


Figure 9 24-lead SOIC (0.615 × 0.300 × 0.0932 inches) package outline (PG-DSO-24), 51-85025

7 Acronyms

Table 11 Acronyms used in this document

Acronym	Description
ACF	active clamp flyback
ADC	analog-to-digital converter
Arm®	advanced RISC machine, a CPU architecture
BOD	brown out detect
BMC	biphase mark code
CC	constant current
CCM	continuous conduction mode
CPU	central processing unit
CrCM	critical conduction mode
CS	current sense
CSN	current sense negative
CSP	current sense positive
DCM	discontinuous conduction mode
DFP	downstream facing port
DP	data plus
DM	data minus
EA	error amplifier
EMI	electromagnetic interference
EPR	extended power range
ESD	electrostatic discharge
FB	feedback
FS	full-speed
GPIO	general-purpose input/output
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LSCSA	low-side current sense amplifier
LVTTL	low-voltage transistor-transistor logic
NMOS	N-type metal-oxide-semiconductor
OCP	overcurrent protection
OVP	overvoltage protection
PD	Power Delivery
PHY	physical layer
POR	power-on reset
PPS	programmable power supply
PWM	pulse-width modulator

Table 11 Acronyms used in this document *(continued)*

Acronym	Description
QR	quasi-resonant
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
SPI	serial peripheral interface, a communications protocol
SR	synchronous rectifier
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
USB	Universal Serial Bus
WDT	watchdog timer
XRES	external reset I/O pin
ZCD	zero crossing defect
ZVS	zero voltage switching

8 Document conventions

8.1 Units of measure

Table 12 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
*B	2023-10-10	Post to external web.
*C	2023-12-20	Updated TR_SR from 60 ns to 75 ns in **Table 6** Functional block specifications.

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