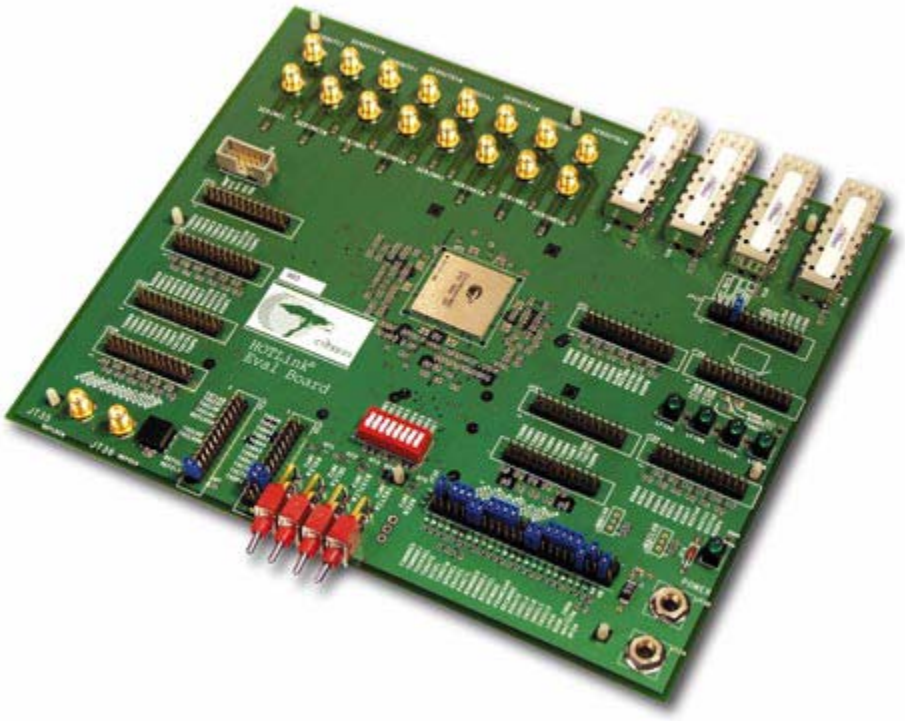
CYP15G0401DXB Evaluation Board
User's Guide



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1. Overview

The CYP15G0401DXB Quad HOTLink II™ Transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 195-to-1500 MBaud per serial link. The multiple channels in each device may be combined to allow transport of wide buses across significant distances with minimal concern for offsets in clock phase or link delay.

This document describes the operation and interface of the CYP15G0401DXB evaluation board. The evaluation board allows users to become familiar with the functionality of the CYP15G0401DXB.

2. Kit Contents

- CYP15G0401DXB-EVAL (The Eval Board)
- *Dear Customer* Letter
- A CD containing
  - CYP15G0401DXB Data Sheet
  - CYP15G0401DXB Evaluation Board User's guide
  - HOTLink II Application Notes
  - CYP15G0401_EVAL.PDA file for DG2020 parallel data generator
  - BSDL Model.

3. Features of the CYP15G0401DXB

- Second generation HOTLink® technology
- GbE, FC, ESCON®, DVB-ASI, SMPTE259 (Level C and level D) and SMPTE292 compliant
- 8B/10B-coded or 10-bit unencoded
- 8-bit encoded data transport
- 10-bit unencoded data transport
- Selectable parity check/generate
- Selectable multi-channel bonding options
  - Four 8-bit channels
  - Two 16-bit channels
  - One 32-bit channel
  - N x 32-bit channel support (interchip)
- Selectable input clocking options
- Selectable output clocking options
- MultiFrame™ receive framer provides alignment to
  - Bit, byte, half-word, word, multi-word
  - COMMA or Full K28.5 detect
  - Single or Multi-byte framer for byte alignment
  - Low-latency option
- Skew alignment support for multiple bytes of offset
- Synchronous LVTTL parallel input interface
- Synchronous LVTTL parallel output interface
- 195- to 1500-MBaud serial signaling rate
- Internal PLLs with *no* external PLL components
- Dual differential PECL-compatible serial inputs per channel
- Dual differential PECL-compatible serial outputs per channel

4. Functional Description of CYP15G0401DXB

Figure 1 shows the block diagram of CYP15G0401DXB, which has four pairs of transmit and receive channels (A,B,C,D).

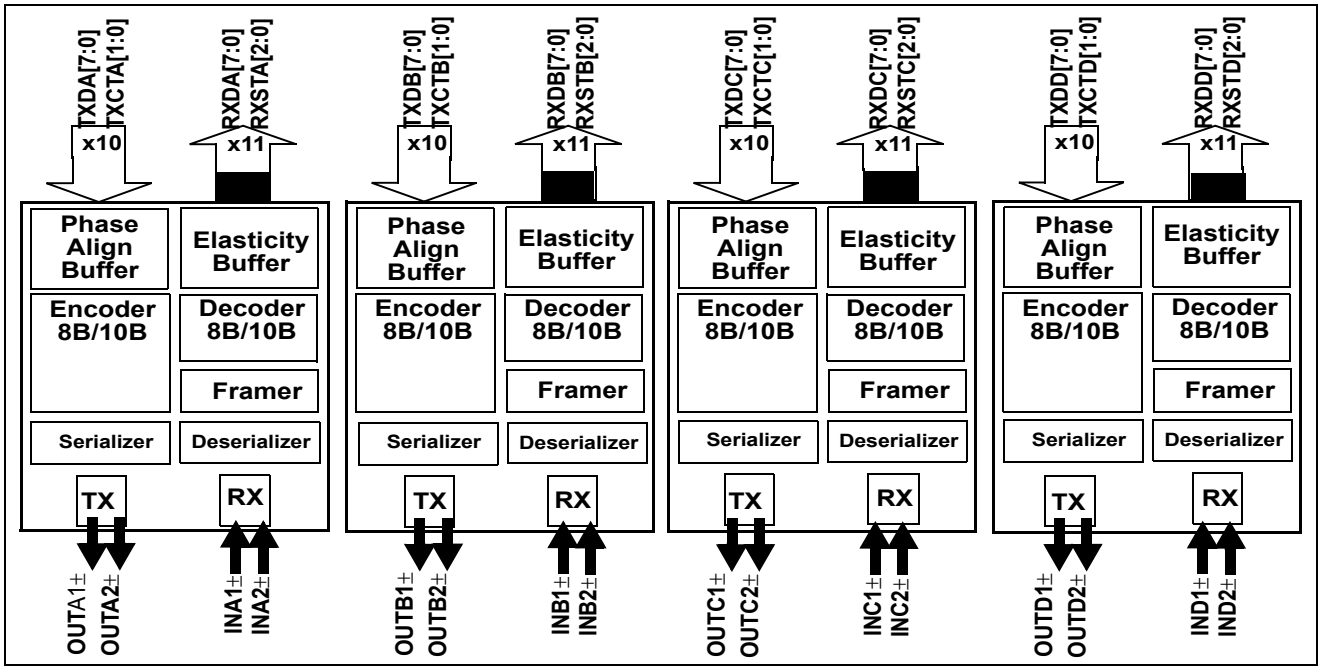

Figure 1. CYP15G0401DXB HOTLink II Block Diagram

Each of the four modules in *Figure 1* represents a transceiver channel. The left side of the transceiver represents the transmitter side mainly composed of phase-align buffer, 8B/10B encoder and serializer. The right side of the transceiver is the receiver composed of deserializer, framer, 8B/10B decoder and elasticity buffer.

Figure 2 shows the transmitter section of CYP15G0401DXB in more detail. The diagram highlights channel A in black. The building blocks of the channel include the phase-align buffer, the 8B/10B encoder and the serializer (shifter).

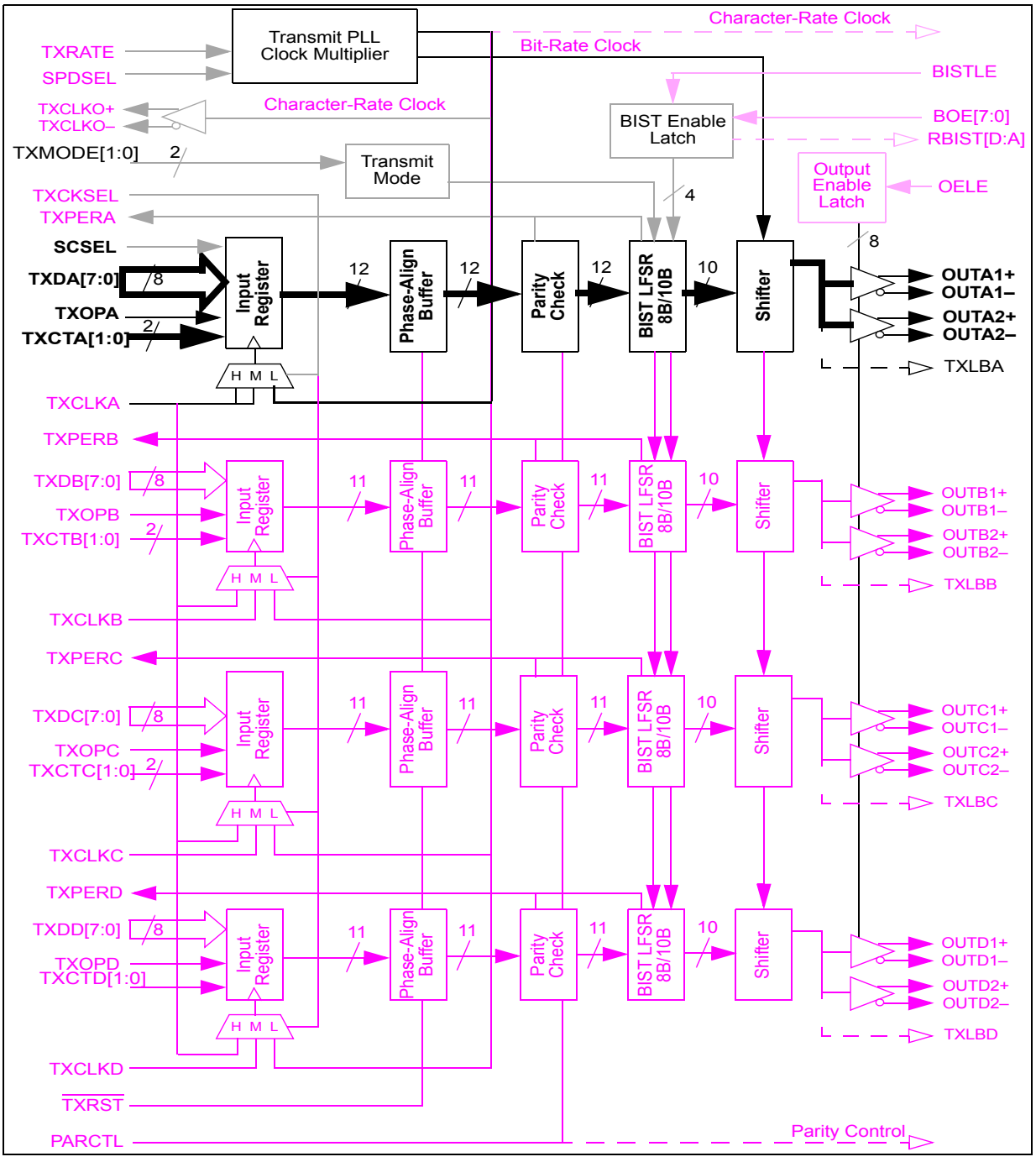

Figure 2. CYP15G0401DXB Transmitter Section Block Diagram

Figure 3 shows the receive section of the CYP15G0401DXB. Channel A has been highlighted black in the diagram. The serial data input passes through the clock and data recovery PLL, the deserializer, the framer, the 10B/8B decoder, and the elasticity buffer.

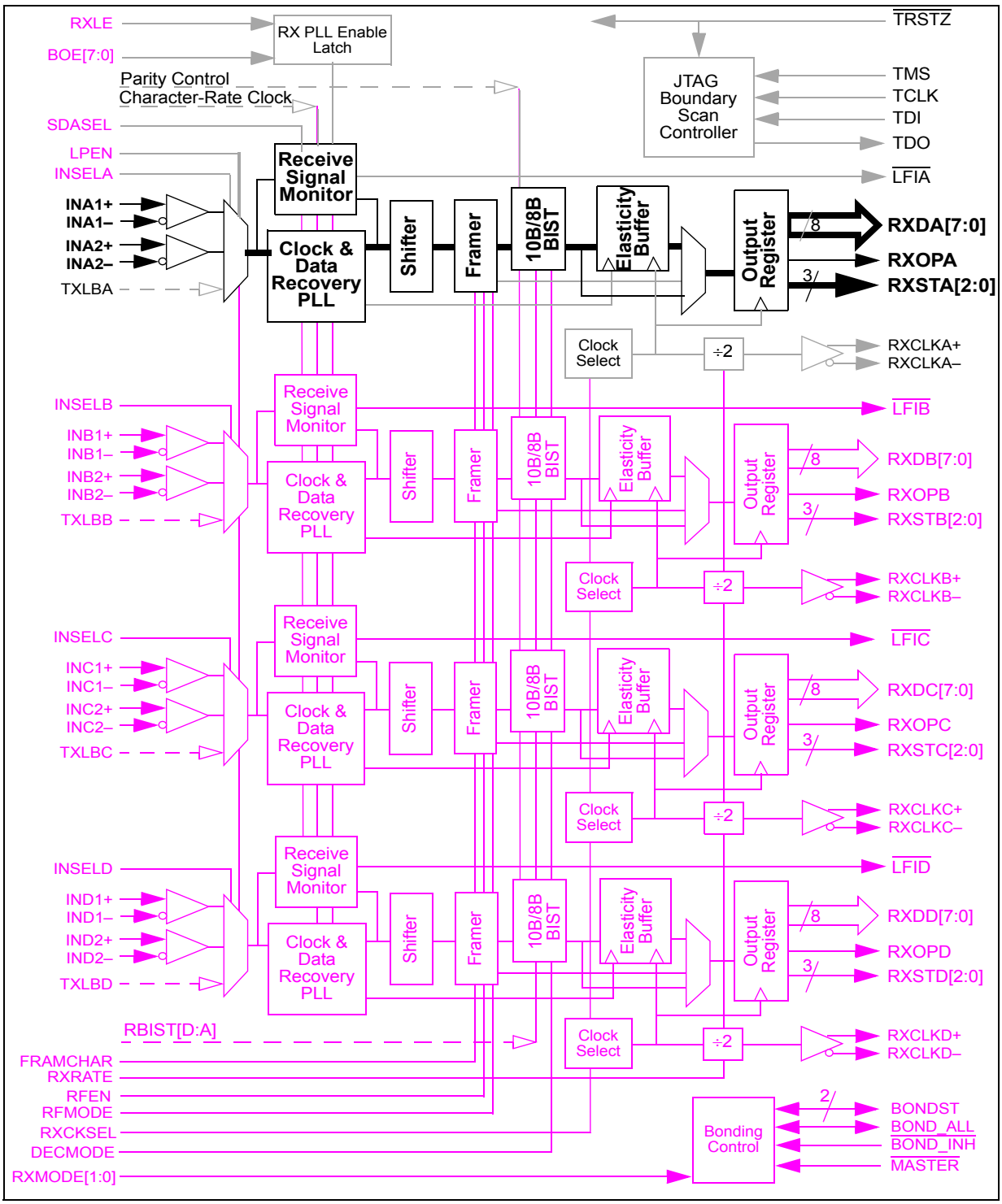

Figure 3. CYP15G0401DXB Receiver Section Block Diagram

5. Board Layout, Photograph and Pin Descriptions

Figure 4 is the top view of CYP15G0401DXB board.

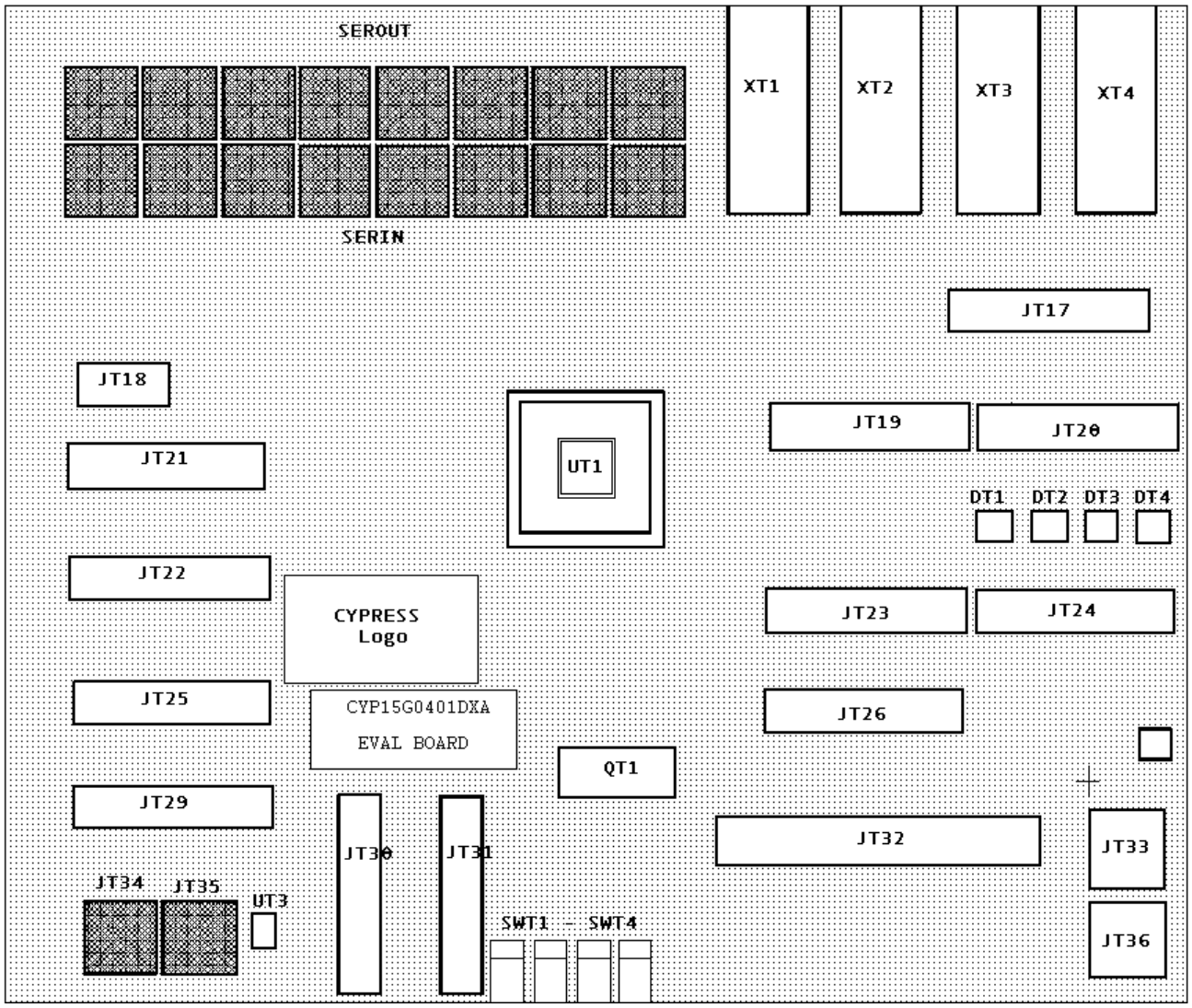

Figure 4. Top View of the CYP15G0401DXB Evaluation Board

Figure 5 shows the different connectors and pins of the CYP15G0401DXB evaluation board.

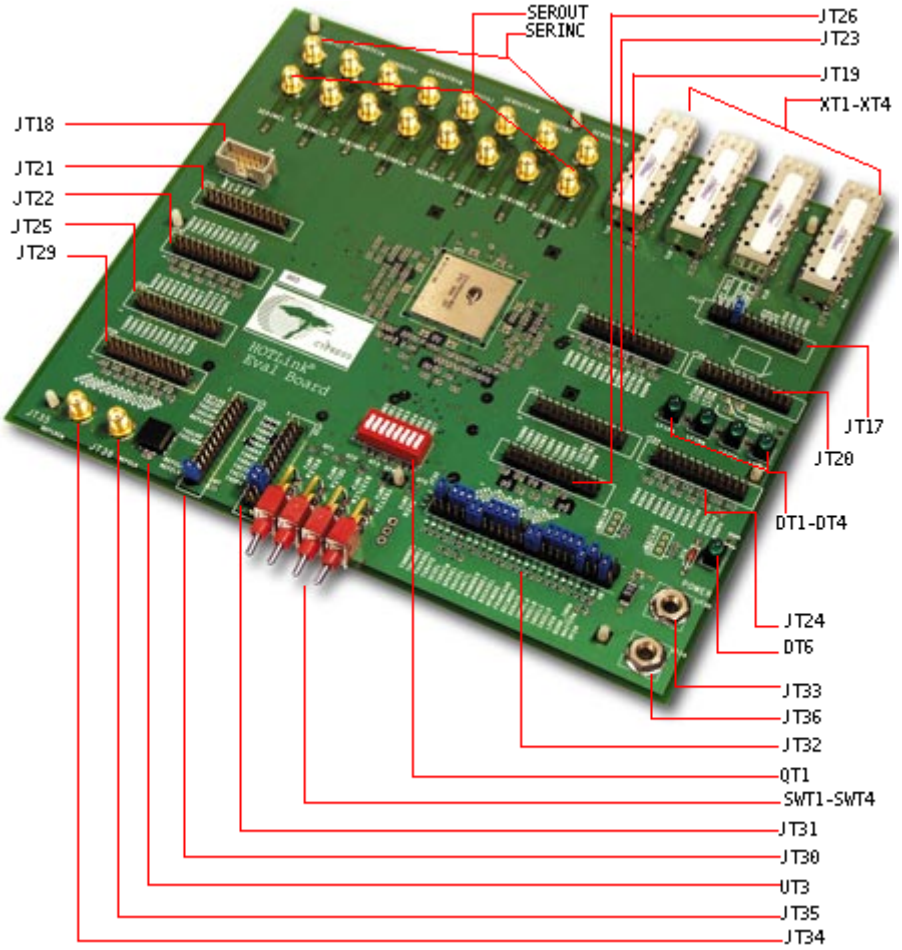

Figure 5. Photograph of the Board with the Connectors Numbered

Table 1 gives a brief description of the connectors of the evaluation board.

Table 1. Description of Connectors of the CYP15G0401DXB Evaluation Board

Connectors	Signals	Description
SEROUT	SEROUTx1± (x = A, B, C, or D) [Negative end denoted by '*' symbol as suffix]	SMA Connectors for SEROUT± (one pair per primary output) • CML compatible primary differential serial data outputs • Routed through 50-ohm impedance • AC coupling capacitors present
SERIN	SERINx1± (x = A, B, C, or D) [Negative end denoted by '*' symbol as suffix]	SMA Connectors for SERIN± (one pair per primary input) • PECL compatible primary differential serial data inputs • Routed through 50-ohm impedance • AC coupling capacitors present • 100-ohm differential load present
JT26	TXPERx, RXCLKx*, RX-CLKx (x = A, B, C or D)	LVTTL outputs

Table 1. Description of Connectors of the CYP15G0401DXB Evaluation Board (continued)

Connectors	Signals	Description
JT31	TXDA[7:0] TXCTA[1:0] TXOPA	LVTTL Input TXDA[7:0] • Transmit data input for channel A TXCTA[1:0] • Transmit control signals for channel A TXOPA • Transmit path odd parity for channel A
JT24	RXDA[7:0] RXSTA[2:0] RXOPA	LVTTL Output RXDA[7:0] • Receive data Input for channel A RXSTA[2:0] • Receive parallel status output for channel A RXOPA • Receive path odd parity for channel A
JT23	TXDB[7:0] TXCTB[1:0] TXOPB	LVTTL Input TXDB[7:0] • Transmit data input for channel B TXCTB[1:0] • Transmit control signals for channel B TXOPB • Transmit path odd parity for channel B
JT19	RXDB[7:0] RXSTB[2:0] RXOPB	LVTTL Output RXDB[7:0] • Receive data Input for channel B RXSTB[2:0] • Receive parallel status output for channel B RXOPB • Receive path odd parity for channel B
JT21	TXDC[7:0] TXCTC[1:0] TXOPC	LVTTL Input TXDC[7:0] • Transmit data input for channel C TXCTC[1:0] • Transmit control signals for channel C TXOPC • Transmit path odd parity for channel C
JT22	RXDC[7:0] RXSTC[2:0] RXOPC	LVTTL Output RXDC[7:0] • Receive data Input for channel C RXSTC[2:0] • Receive parallel status output for channel C RXOPC • Receive path odd parity for channel C
JT25	TXDD[7:0] TXCTD[1:0] TXOPD	LVTTL Input TXDD[7:0] • Transmit data input for channel D TXCTD[1:0] • Transmit control signals for channel D TXOPD • Transmit path odd parity for channel D

Table 1. Description of Connectors of the CYP15G0401DXB Evaluation Board (continued)

Connectors	Signals	Description
JT29	RXDD[7:0] RXSTD[2:0] RXOPD	LVTTL Output RXDD[7:0] • Receive data Input for channel D RXSTD[2:0] • Receive parallel status output for channel D RXOPD • Receive path odd parity for channel D
XT1 - XT4	Optical Modules	Option for Small Form-Factor Pluggable (SFP) optical modules. The optical modules make use of the secondary input (INx2±) and secondary output (OUTx2±) in each transceiver channel.
JT17	Optical Controls	Controls for the optical modules
DT1 - DT4	LFIx*	• Link Fault Indication output LEDs • Signal active LOW. LED is lit when signal is active. • Logical OR of four internal conditions: — Received serial data frequency outside expected range — Analog amplitude below expected levels — Transition density lower than expected — Receive channel disabled
JT20	BONDST[1:0] BOND_ALL LFIx* headers	BONDST[1:0] and BOND_ALL • Open drain bidirectional channel bonding controls • Provision for external 75-ohm pull-up resistor to be connected to V_{CC} • BONDST[1:0] and BOND_ALL are used when multiple devices are bonded together LFIx* • Headers to probe LFI status for each channel
Power		
DT6	Power Indicator	Indicates if the power supply is ON. The LED glows when the power supply goes ON.
JT33	V_{CC}	Banana Jack • +3.3 V DC
JT36	GND	Banana Jack • Ground
JT32	RX and TX side control signals	Please refer to the *Table 2* for more details.
QT1	BOE[7:0]	• BIST, serial output, and receive channel enable latch input switches • LVTTL Input
SWT1 - SWT3	RXLE OELE BISTLE	RXLE (Receive channel enable latch enable) • Active HIGH OELE (Serial output driver enable latch enable) • Active HIGH BISTLE (Transmit and receive BIST latch enable) • Active HIGH
SWT4	$\overline{\text{TRSTZ}}$	"Press and release" switch for global device reset

Table 1. Description of Connectors of the CYP15G0401DXB Evaluation Board (continued)

Connectors	Signals	Description
JT30	Clock inputs and outputs	TXCLKA, TXCLKB, TXCLKC and TXCLKD • Parallel LVTTL input clocks for each channel TXCLKO, TXCLKO* • Buffered version of internal character rate clock. • LVTTL output REFCLK - INT/EXT Selector • Jumper selector for selecting REFCLK as either onboard or external
UT3	Onboard Clock	125-MHz clock
JT35	REFCLK	External differential Reference clock input SMA connectors
JT34	REFCLK*	
JT18	JTAG Interface	Standard JTAG Interface. CYP15G0401DXB does not have a dedicated JTAG reset. It has an inbuilt power-on-reset circuit for resetting the JTAG logic.

Table 2 gives a detailed description of all the control pins in JT32.

Many of the static control signals are of nonstandard 3-level select. This means that they operate at three voltage levels, which are termed as

- HIGH (Direct connection to V_{CC})
- MID (Open or allowed to float)
- LOW (Direct connection to V_{SS}, i.e., GND).

Table 2. Description of Control Pins in JT32

Pin Name	Characteristics
TXMODE0, TXMODE1	Transmit mode (2 inputs) 3-Level Select • Configure LL for Encoder bypass • LM and LH are reserved for testing • All other combinations along with the selection of SCSEL are for encoder control. (Please refer to the data-sheet for more details)
TXCKSEL	Transmit Clock Select (1 input) 3-Level Select • When L, REFCLK is used by all the input registers. • When M, TXCLKx is used. • When H, TXCLKA is used by all the input registers.
TXRATE	LVTTL Input • When H, the transmit PLL multiplies REFCLK by 20 to generate the bit rate clock. • When L, the transmit PLL multiplies REFCLK by 10 to generate the bit rate clock.
SCSEL	Special Character Select LVTTL Input Used with the TXMODE[1:0] to • Either encode special characters • Or initiate a word sync sequence
TXRST*	Transmit Clock Phase Align Buffer Reset • Active LOW

Table 2. Description of Control Pins in JT32 (continued)

Pin Name	Characteristics
SPDSEL	Serial Rate Select 3-Level Select • LOW = 195–400 MBd • MID = 400–800 MBd • HIGH = 800–1500 MBd
SDASEL	Signal Detect Amplitude Level Select 3-Level Select • LOW = 140 mV peak-peak differential • MID = 280 mV peak-peak differential • HIGH = 420 mV peak-peak differential
PARCTL	Parity check/generate control 3-Level Select • LOW = Parity checking is disabled • MID or HIGH = Parity checking enabled. Please refer to data sheet for further details.
RXMODE0, RXMODE1	Receive Operating Mode. • LL & LH for independent mode • ML & MH for dual channel bonding mode • HL & HH for quad channel bonding mode • LM, MM & HM are reserved for test
RXCKSEL	Receive Clock Mode. 3-Level Select • L: Output register is clocked by REFCLK. — RXCLK± presents a buffered/delayed form of REFCLK. • M: Output register is clocked by the recovered clock. — RXCLK+ follows the recovered clock as selected by RXRATE. — The elasticity buffer is bypassed. • H: Clocking option for dual and quad channel bonding modes. Please refer to data sheet for more details.
RFMODE	Reframe Mode Select. 3-Level Select • Works in conjunction with the presently enabled channel bonding mode and the type of framing character selected. Please refer to the data sheet for CYP15G0401DXB for detailed information.
FRAMCHAR	Framing Character Select. 3-Level Select
DECMODE	Decoder Mode Select. 3-Level Select Please refer to the data sheet for CYP15G0401DXB for detailed information.
RXRATE	Receive Clock Rate Select. 3-Level Select LVTTL Input
INSELA, INSELB, INSELC, INSELD	Receive Input Selector. 2-Level Select LVTTL Input • HIGH - INx1± input is passed into the CDR circuit • LOW - INx2± input is passed into the CDR circuit For example, if INSELA is selected as HIGH, INA1± input will be passed into the receiver.

Table 2. Description of Control Pins in JT32 (continued)

Pin Name	Characteristics
LPEN	All-Channel Loop-Back-Enable. LVTTL Input. Active HIGH When HIGH • Transmit serial data is internally routed to receive serial data • All external serial data inputs are ignored
BOND_INH*	Parallel Bond Inhibit. LVTTL Input Active LOW
MASTER*	Master Device Select for Multi-Device Channel Bonding LVTTL Input
RFEN	Reframe Enable for all channels. Active HIGH

6. Test Modes

The different test modes discussed in this document are BIST, parallel data and channel bonding test mode.

BIST Mode

CYP15G0401DXB has the Built-In Self-Test (BIST) capability. Each transmit and receive channel contains independent BIST Pattern Generator and Checker.

Figure 6 shows the BIST mode operation.

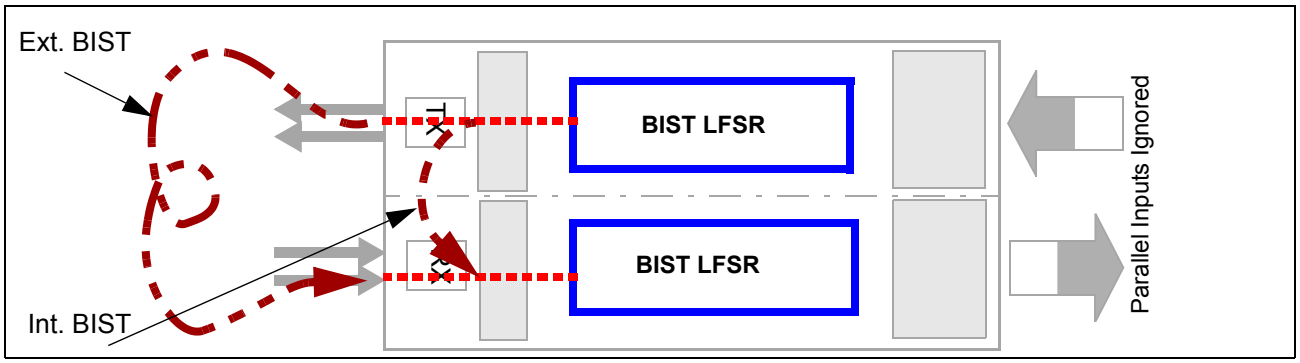

Figure 6. The BIST Mode Operation

Two versions of BIST will be described in these sections:

- BIST internal loopback mode
- BIST external loopback mode.

Parallel Data Test Mode

The variations discussed in this document, for this mode, are

- Parallel in – parallel out mode (Encoded)
- Parallel in – parallel out mode (Unencoded)
- Parallel in – serial out mode. (Testing the transmit side)
- Different clock source (i.e., internal vs. external; different frequency mode, etc.).

Channel Bonding Test Mode

Two variations discussed in this document, for this mode are

- Dual bond receive channels
- Quad bond receive channels.

The detailed description will be comprised of

- Equipment Required (Equipment, Cable, etc.)
- Test Set-up
- Result Verification
- Operational Variations.

6.1 Adjusting Settings on the Board

To successfully run any test, the REFCLK INT/EXT selector, QT1 (BOE[0:7]), JT32 (control signals) and SWT1-SWT3 (toggle switches for RXLE, OELE and BISTLE) on the board must be correctly configured. This section of the user's guide gives some directions on how to read the settings on the board. Shown in *Figure 7* is an illustration of the control switches that you may use in the test set-up.

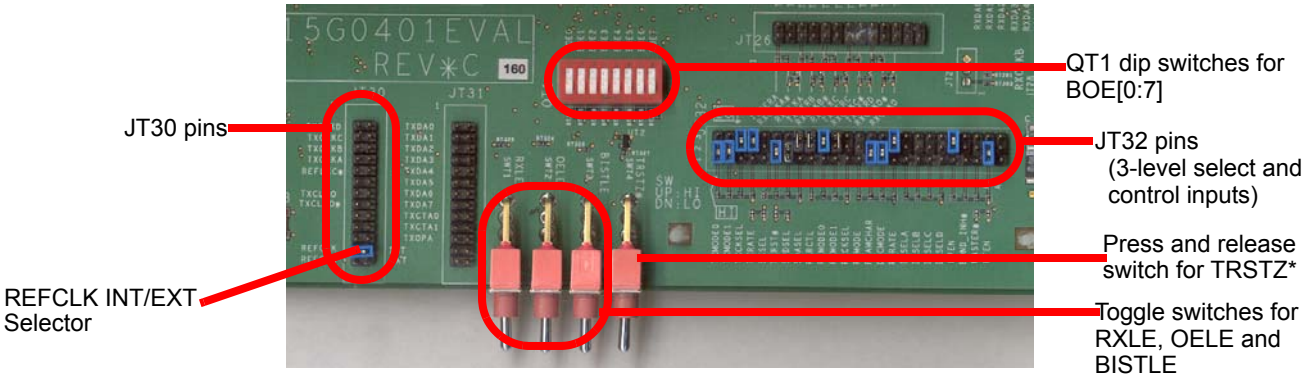

Figure 7. Control Switches for Test Set-up

To run the board either on the internal or external clock, configure the REFCLK selector on JT30 shown in *Figure 8* accordingly. Amongst the two pins in the right column one pin marks INT (internal) and another marks EXT (external). To switch from one clock mode to another, simply remove the shunt on the REFCLK pin and replace it onto the desired pin. Ensure the board does not run on both internal and external clock at the same time.

(Note: External clock input SMAs are located at JT34 and JT35. For single ended REFCLK apply an LVTTL clock signal to REFCLK input in JT35 and leave REFCLK*(JT34) input floating)

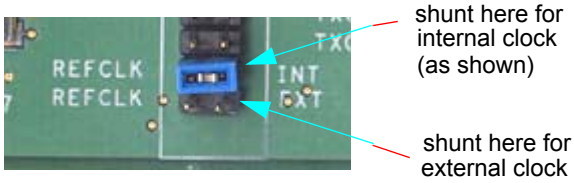

Figure 8. Controlling REFCLK Settings

The 2-level dip switches on QT1 for BOE[7:0] are configured HIGH or LOW as illustrated in *Figure 9*.

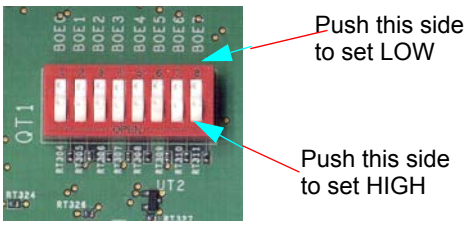

Figure 9. Controlling QT1 Dip Switch Settings

JT32 pins have 3-level inputs. Identify the row of the JT32 pins using row numbers on the silkscreen. A HIGH setting is achieved by placing a shunt across rows 1 and 2. A LOW setting is achieved by placing a shunt across rows 2 and 3. A MID setting is achieved when there is no shunt placed and the pins are left open. To change settings on a pin, remove the shunt from the original position and follow the instructions on *Table 3*. This is illustrated in *Figure 10*.

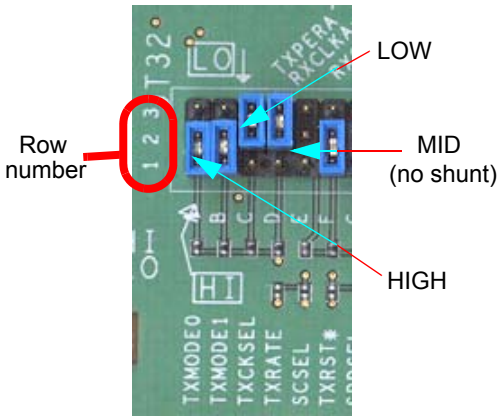

Figure 10. Controlling JT32 Pin Settings

Table 3. The High, Mid, and Low Levels on JT32

	Instruction
High	Place a shunt across row 1 and 2
Mid	Do not place any shunt
Low	Place a shunt across row 2 and 3

Another set of control inputs on the board are the three toggle switches that look similar to the one in *Figure 11*. RXLE, OELE and BISTLE are important control signals on these pins. To change their settings, follow the instructions in *Table 4*.

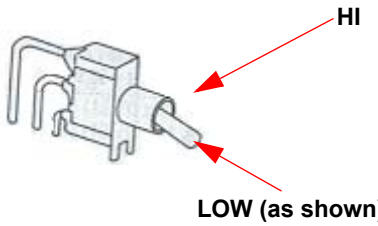

Figure 11. Controlling 3-Level Toggle Switch Settings

Table 4. The High, Mid, and Low Levels on the Toggle Switches

	Instruction
High	Lift the lever to the top-most position
Low	Press the lever down to the bottom-most position

The switch for TRSTZ* (SWT4) looks similar in appearance to the switch shown in *Figure 11*, but has a different operation. Unlike the other switches for latch enables, this switch is a "Press and Release" switch. When this switch is pressed down and released the entire device is reset.

6.2 BIST Test Set-up

6.2.1 BIST Internal Loopback Mode

6.2.1.1 Equipment Required

Equipment needed:

- CYP15G0401DXB evaluation board
- Instrument grade power supply 3-amp current limit @ 3.3V
- Oscilloscope (500 MHz or better)
- Digital signal analyzer (to observe eye diagrams)
- Multimeter

Cable Needed:

- SMA to SMA coaxial cables
- Power supply cables (banana plug cables)

6.2.1.2 Test Equipment Set-up

Figure 12 shows the test set-up of BIST. The signal analyzer in the diagram is optional.

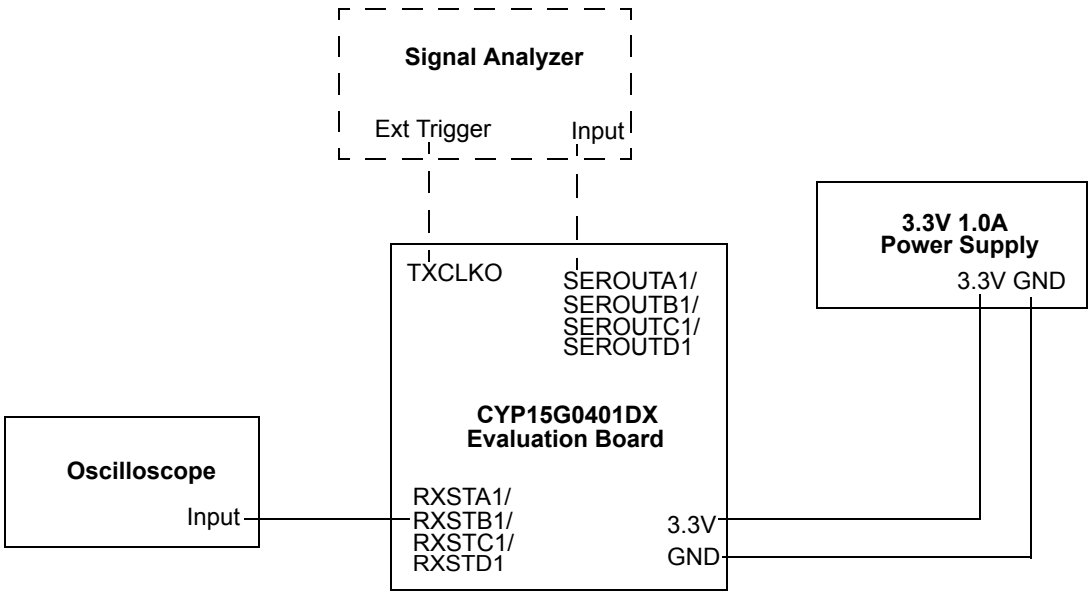

Figure 12. Pictorial Representation of the Internal BIST Set-up

6.2.1.3 Test Set-up

The intention of this set-up is to test CYP15G0401DXB in BIST mode. The purpose of this test is to transmit BIST data across all channels and receive the same BIST data across all channels by looping the serial out data to serial in data internally.

Follow the procedure below for the test set-up.

1. Select internal clocking mode by placing the shunt across INT selection on JT30.
2. Configure the JT32 pins using the following settings in *Table 5* by adjusting their shunt position:

Table 5. The Levels of Different Static Signals on JT32 for BIST Mode

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	PARCTL	LOW	INSELA	HIGH
TXMODE1	MID	RXMODE0	LOW	INSELB	HIGH
TXCKSEL	LOW	RXMODE1	LOW	INSELC	HIGH
TXRATE	LOW	RXCKSEL	LOW	INSELD	HIGH
SCSEL	LOW	RFMODE	MID	LPEN	HIGH
TXRST*	HIGH	FRAMCHAR	HIGH	BOND_INH*	LOW
SPDSEL	HIGH	DECMODE	HIGH	MASTER*	MID
SDASEL	LOW	RXRATE	LOW	RFEN	HIGH

The values of the TXMODE[1:0] have been selected for TX Mode 3.

The FRAMECHAR value is HIGH to select K28.5 characters as the framing character.

RFMODE is set MID which means that the Cypress-mode multibyte framer is selected.

RFEN is HIGH which implies that the framer selected by the RFMODE is enabled.

Parity Generation is disabled as PARCTL is LOW.

LPEN is HIGH, which indicates that the internal loopback mode is enabled.

INSEL is HIGH, which means that the IN1± are selected.

3. Ensure that RXLE, OELE and BISTLE are all pulled to LOW and all BOEs to HIGH.
4. Adjust the power supply to 3.3 volts and 3 amps limit.
5. Apply power to the board.
6. Verify that the power supply LED (DT6) is on.
7. Press down and release TRSTZ* (SW4), which will reset the board.
8. Verify that all LFIx* LEDs are ON, indicating line faults on all channels.
9. Pull RXLE and OELE HIGH, and BISTLE to LOW after deassertion of TRSTZ*
10. Enable necessary transmit and receive channels by keeping the corresponding BOEs HIGH as shown in *Table 6*. If you wish to enable all the channels, simply set all the BOEs to HIGH.

Table 6. Channel Enabling Controls

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[7]	OUTD2±	Transmit D	X
BOE[6]	OUTD1±	Receive D	Receive D
BOE[5]	OUTC2±	Transmit C	X
BOE[4]	OUTC1±	Receive C	Receive C
BOE[3]	OUTB2±	Transmit B	X
BOE[2]	OUTB1±	Receive B	Receive B
BOE[1]	OUTA2±	Transmit A	X
BOE[0]	OUTA1±	Receive A	Receive A

11. Push RXLE and OELE to LOW. The corresponding transmit and receive channels should be enabled at this point.
12. At this point, the RXLE, OELE, and BISTLE will be closed (pushed LOW). Now pull the BISTLE HIGH.
13. Then close (LOW) the corresponding BOEs switches for those channels in which BIST is desired. Please refer to *Table 6* for details. If you wish to enable BIST on all the channels, simply set all the BOEs to LOW.
14. Push the BISTLE switch to LOW.
15. Verify that the LFIx* LEDs (DT1-DT4) for the corresponding channels are OFF while the power supply LED (DT6) is still on.
16. The board should already in BIST mode at this time. Verify the oscilloscope display on RXSTA1 matches with the waveform in *Figure 13*.

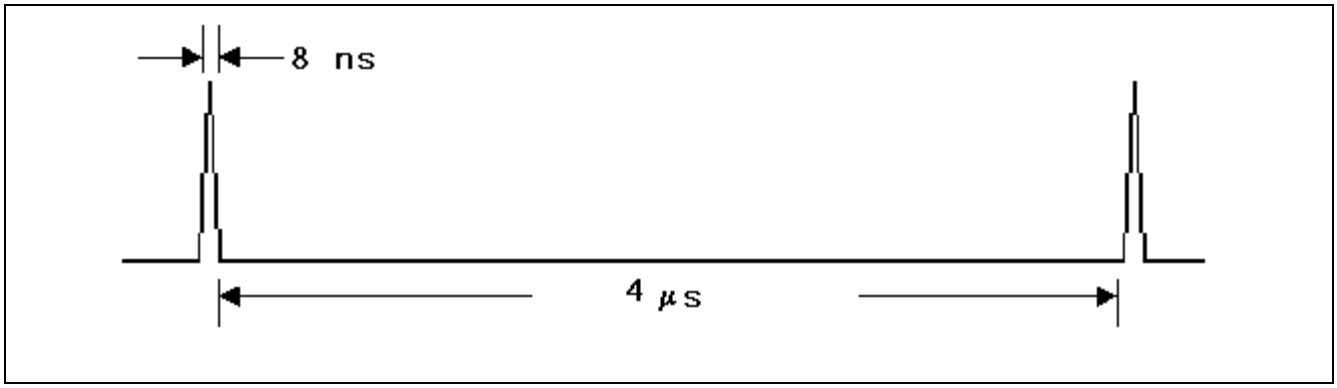

Figure 13. Signal on RXSTx1 when BIST is Successful

17. Repeat observing the RXSTx1 waveforms from all the other active channels (B, C, D). RXSTA1, RXSTB1, RXSTC1, and RXSTD1 are all located on the sockets JT24, JT19, JT22, and JT29 respectively.
18. Verify that RXSTx2 is always at logic-0 to indicate that there is no BIST error for all 4 channels. RXSTx2 pin is next to the RXSTx1 pin.
19. With the completion of the above, BIST is successful. The following steps are optional.

20.Check the BIST serial out data as an eye diagram by following the procedure below.

- Change LPEN to LOW on the JT32. Notice that LFIx* LEDs will go ON.
- Connect a pair of serial output (SEROUTx1/SEROUTx1*) to the digital signal analyzer using SMA cables.
- Trigger the signal analyzer by connecting a jumper-to-SMA cable from TXCLKO on JT30 to the trigger input of the analyzer.
- Verify on the signal analyzer that the eye diagram looks as shown in *Figure 14*. Make sure that the eye width is equal to 1-bit period.

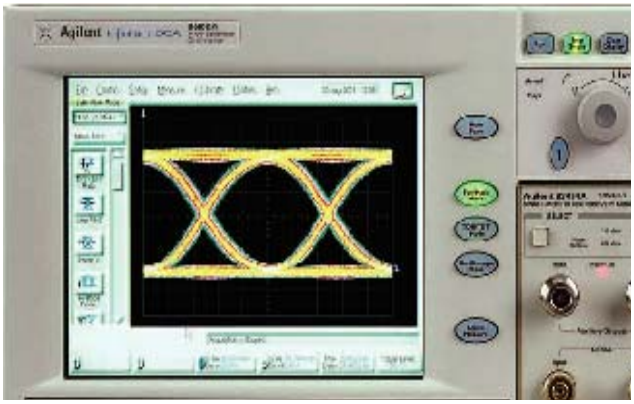

Figure 14. The Eye Diagram through the Signal Analyzer

6.2.2 BIST External Loopback Mode

6.2.2.1 Equipment Required

Equipment needed is the same as mentioned in *Section 6.2.1.1* on page 17.

6.2.2.2 Test Set-up

Retain the test set-up for the Internal BIST set-up as described in Section 6.2.1.3 and make the following changes in the procedures below.

1. Before performing the test, loop a coaxial cable from INx1± to OUTx1± as shown in *Figure 15*.
2. Continue with step 1 mentioned in Section 6.2.1.3.
3. Configure the JT32 pins using the same settings mentioned in step 2 of Section 6.2.1.3, except for the following change. Change LPEN from HIGH to LOW in *Table 5*.
4. Continue with all other subsequent steps in 6.2.1.3.

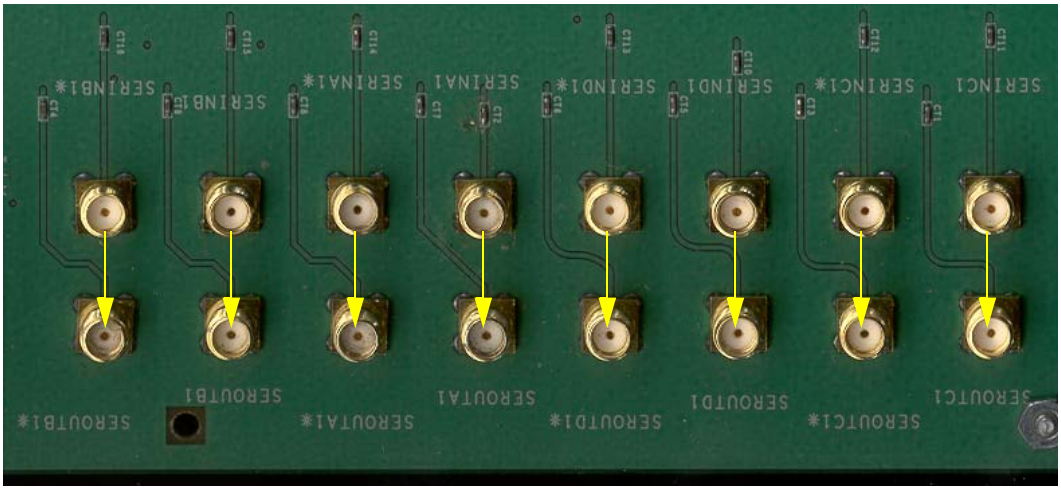

Figure 15. Coaxial Cable Connection for External BIST Mode

6.3 Parallel Data Test Mode

6.3.1 Individual Channel Mode

6.3.1.1 Equipment Required

Equipment needed:

- CYP15G0401DXB Eval Board
- Instrument Grade Power Supply 3 Amp @ 3.3V
- Parallel Data Generator: DG2020 from Tektronix (settings will be provided by Cypress) or equivalent
- Logic Analyzer: TDA700 series from Tektronix or equivalent.
- Multimeter.

Cable needed:

- 2 SMA-to-SMA coaxial cables
- Power supply cables
- DG2020 cables with right connectors
- Logic Analyzer cables with right connectors.

6.3.1.2 Parallel In Parallel Out Test Set-up

Follow the procedure below for the test set-up.

1. Load the Cypress supplied file CY15G0401_EVAL.PDA in DG2020 data generator. If you are using your own data generator, use a similar waveform, as shown in *Figure 16*.

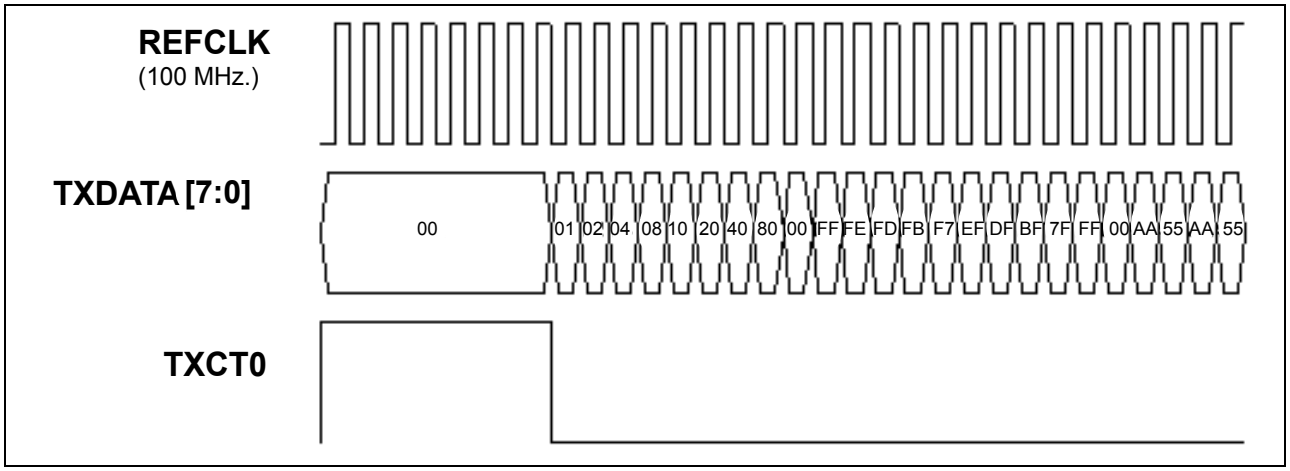

Figure 16. Generated Clock, Data and Control Signal from DG2020

Note: The outputs of the DG2020 for this PDA file are mapped to POD-A bits 0-11. The outputs may need to be remapped for a particular test set-up. Consult the user's manual for setting up the DG2020.

2. Connect the TXDATA lines of the data generator to JT21 (TXDATA[7:0] to TXDC[7:0] respectively). Connect TXCT0 to TXCTC0. Ground TXCTC1 on JT21 (shunt across pin 19 and pin 20).
3. Connect the Logic Analyzer TDA700 to read the following receive data lines on JT22, RXDC[7:0] and RXSTC[2:0].
4. Connect the REFCLK output of the DG2020 to JT35, REFCLK input. Place a shunt across pin 25 and pin 26 (EXT) on JT30. This means that the external clock will be used by CYP15G0401DXB.
5. Connect a clock input of the logic analyzer to RXCLKC on JT26. The clocking of the logic analyzer needs to set to external. On the TLA 700 series logic analyzer this is done in the "SETUP" window. After selecting external clocking press the "MORE" button to customize your clock's settings. Your clock definition needs to be changed to the clock input that you are using.
6. Configure the shunts on JT32 as listed in *Table 7*.

Table 7. Settings on JT32 for Independent Channel Parallel-in and Parallel-out Mode (Encoded)

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	PARCTL	LOW	INSELA	HIGH
TXMODE1	MID	RXMODE0	LOW	INSELB	HIGH
TXCKSEL	LOW	RXMODE1	LOW	INSELC	HIGH
TXRATE	LOW	RXCKSEL	LOW	INSELD	HIGH
SCSEL	LOW	RFMODE	MID	LPEN	HIGH
TXRST*	HIGH	FRAMCHAR	HIGH	BOND_INH*	LOW
SPDSEL	HIGH	DECMODE	HIGH	MASTER*	MID
SDASEL	LOW	RXRATE	LOW	RFEN	HIGH

7. Adjust the power supply to 3.3V and 3 amps limit.
8. Apply power to the board.
9. Verify that the power supply LED (DT6) is on.
10. Press down and release TRSTZ* (SW4), which will reset the board.
11. Pull RXLE and OELE HIGH, and BISTLE to LOW after deassertion of TRSTZ*
12. Enable necessary transmit and receive channels by keeping the corresponding BOEs HIGH as shown in *Table 6*. If you wish to enable all the channels, simply set all the BOEs to HIGH.
13. Push RXLE and OELE to LOW. The corresponding transmit and receive channels should be enabled at this point.
14. Start transmitting data from the data generator making sure it is in REPEAT mode.

The following steps are done for result verification:

1. After the Logic analyzer has acquired the data it will pause and display the data received. Compare the data with the transmitted data.The data should be same as the transmitted data except for the period when TXCTC0 is 1, when the 00h input will give BCh output, which is the K28.5 sequence.
2. Repeat the procedure for channels A,B,D.

6.3.1.3 Unencoded Mode

In unencoded mode the 8B/10B encoder is bypassed in the transmit side and the 10B/8B decoder is bypassed in the receive side. The settings for unencoded mode (parallel-in and parallel-out) with multi-byte framing enabled is shown in *Table 8*. Please note that these variations are applicable to the Dual Bond and the Quad Bond mode.

The DG2020 data pattern provided by Cypress does not contain any framing patterns for the unencoded mode. In order for HOTLink to frame the data properly, two consecutive K28.5's need to be added to the DG2020 pattern.

This can be accomplished by extending the data pattern by 2 clock cycles. Add the two 10-bit K28.5 characters as shown in *Figure 17*.

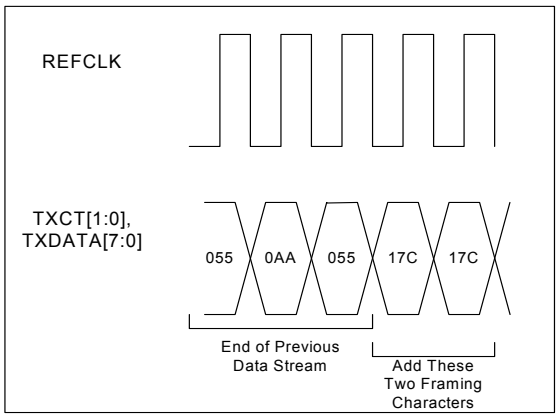

Figure 17. Adding Two Framing Characters to Data Stream

Table 8. Settings on JT32 for Independent Channel Parallel-in and Parallel-out Mode (Unencoded)

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	PARCTL	LOW	INSELA	HIGH
TXMODE1	LOW	RXMODE0	LOW	INSELB	HIGH
TXCKSEL	LOW	RXMODE1	LOW	INSELC	HIGH
TXRATE	LOW	RXCKSEL	MID	INSELD	HIGH
SCSEL	LOW	RFMODE	MID	LPEN	HIGH
TXRST*	HIGH	FRAMCHAR	HIGH	BOND_INH*	LOW
SPDSEL	HIGH	DECMODE	LOW	MASTER*	MID
SDASEL	LOW	RXRATE	LOW	RFEN	HIGH

- The output registers are assigned in a different sequence when the DECMODE is LOW, i.e., when the decoder is bypassed, than when the DECMODE is not equal to LOW. *Table 9* shows the sequence in which the bits are arranged from LSB to MSB.

Table 9. Output Register Bit Assignments

Signal Name	DECMODE = LOW	DECMODE = MID or HIGH
RXSTx[2]	COMDETx	RXSTx[2]
RXSTx[1]	DOUTx[0]	RXSTx[1]
RXSTx[0]	DOUTx[1]	RXSTx[0]
RXDx[0]	DOUTx[2]	RXDx[0]
RXDx[1]	DOUTx[3]	RXDx[1]
RXDx[2]	DOUTx[4]	RXDx[2]
RXDx[3]	DOUTx[5]	RXDx[3]
RXDx[4]	DOUTx[6]	RXDx[4]
RXDx[5]	DOUTx[7]	RXDx[5]
RXDx[6]	DOUTx[8]	RXDx[6]
RXDx[7]	DOUTx[9]	RXDx[7]

Note that when DECMODE is LOW, i.e., the decoder is bypassed, the signal RXSTx[1] corresponds to the LSB of the 10-bit data, unlike when the decoder is not bypassed (DECMODE = MID or HIGH), the signal RXDx[0] corresponds to the LSB of the 8-bit data.

Similarly, when the DECMODE is LOW, the signal RXDx[7] corresponds to the MSB of the 10-bit data. When the decoder is not bypassed, RXDx[7] is the MSB of the 8-bit data.

This warrants the change in the way the data is viewed in the logic analyzer.

The input register bit assignments for the 10-bit unencoded data is shown in *Table 10*. Note that TXDx[0] corresponds to the LSB of the 10-bit value. TXCTx[1] corresponds to the MSB of the 10-bit value.

Table 10.Input Register Bit Assignments

Signal Name	Unencoded
TXDx[0] (LSB)	DINx[0]
TXDx[1]	DINx[1]
TXDx[2]	DINx[2]
TXDx[3]	DINx[3]
TXDx[4]	DINx[4]
TXDx[5]	DINx[5]
TXDx[6]	DINx[6]
TXDx[7]	DINx[7]
TXCTx[0]	DINx[8]
TXCTx[1] (MSB)	DINx[9]

In order to lock the receive CDR PLL, the data transition should be HIGH when doing the unencoded mode test. For minimum jitter, the data should not contain more than 5 consecutive 0s or 1s.

6.3.1.4 Parallel In - Serial Out Mode

The test set-up for parallel In serial out mode is similar to that of the parallel in parallel out mode described in *Section 6.3.1.2* on page 21. The following are some of the changes. Please note that these variations are applicable to the Dual Bond and the Quad Bond mode.

- Change LPEN to LOW on the JT32.
- Connect a pair of serial output to the digital signal analyzer using SMA cable.
- Trigger the signal analyzer by connecting a jumper-to-SMA cable from TXCLKO on JT30 to the trigger input on the analyzer.

6.3.1.5 Different Clock Signal

The test set-up for using a TXCLKx to latch the parallel data into the device instead of REFCLK is similar to that of the parallel-in parallel-out mode described in *Section 6.3.1.2* on page 21. The following are some of the changes that need to be made.

1. Changing the transmit clock select.
   - By changing TXCKSEL on JT32 to MID, parallel data can be latched into the input registers by using TXCLKx instead of the reference clock. A clock should be connected to TXCLKx input and this clock should be synchronous in frequency to REFCLK. Please refer to *Table 2:* Description of Control Pins in JT32 *on page 13* to locate TXCLKx signals in the board.
2. Once dataflow has started, move TXRST* jumper in JT32 from HIGH to LOW and then back to HIGH. This will reset the phase align buffer to absorb the phase differences between the TXCLKx and REFCLK.

6.3.2 Dual Bond Receive Channels

6.3.2.1 Equipment Required

Equipment needed is the same as mentioned in *Section 6.3.1.1* on page 21.

6.3.2.2 Test Set-up

For the dual channel bonding

- RXMODE1 must be MID.
- DECMODE must be MID or HIGH.

Follow the procedure below for test set-up:

1. Change RXMODE1 to MID by placing the shunt appropriately. Make sure that the signals in JT32 look as follows.

Table 11.Settings on JT32 for Dual Bond Parallel-in and Parallel-out Mode (Encoded)

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	PARCTL	LOW	INSELA	HIGH
TXMODE1	MID	RXMODE0	LOW	INSELB	HIGH
TXCKSEL	LOW	RXMODE1	MID	INSELC	HIGH
TXRATE	LOW	RXCKSEL	LOW	INSELD	HIGH
SCSEL	LOW	RFMODE	MID	LPEN	HIGH
TXRST*	HIGH	FRAMCHAR	HIGH	BOND_INH*	LOW
SPDSEL	HIGH	DECMODE	HIGH	MASTER*	MID
SDASEL	LOW	RXRATE	LOW	RFEN	HIGH

3. Copy the DG2020 PODA output to PODB.
4. Connect the PODB TXDATA lines of the data generator to JT25 (TXDATA[7:0] to (TXDD0-TXDD7) respectively). Connect TXCTD to TXCTD0. Ground TXCTD1 on JT25 (shunt across pin 19 and pin 20).
5. Connect the logic Analyzer TDA700 to read the following receive data lines on
   — JT22, RXDC[7:0] and RXSTC[2:0].
   — JT29, RXDD[7:0] and RXSTD[2:0].
6. Continue with all the steps starting with step 4 of *Section 6.3.1.2* on page 21, replacing step 7 with step 1 of this section.

Result Verification

1. Follow the verification steps in *Section 6.3.1.2* on page 21.
2. Repeat the procedure for channels A&B bonded together.

6.3.3 Quad Bond Receive Channels

6.3.3.1 Equipment Required

Equipment needed is the same as mentioned in *Section 6.3.1.1* on page 21.

6.3.3.2 Test Set-up

For quad channel bonding

- RXMODE1 must be HIGH.
- DECMODE must be MID or HIGH.

Follow the procedure below for test set-up:

Table 12.Settings on JT32 for Quad Bond Parallel-in and Parallel-out Mode (Encoded)

Signal	Level	Signal	Level	Signal	Level
TXMODE0	LOW	PARCTL	LOW	INSELA	HIGH
TXMODE1	MID	RXMODE0	LOW	INSELB	HIGH
TXCKSEL	LOW	RXMODE1	HIGH	INSELC	HIGH
TXRATE	LOW	RXCKSEL	LOW	INSELD	HIGH
SCSEL	LOW	RFMODE	MID	LPEN	HIGH
TXRST*	HIGH	FRAMCHAR	HIGH	BOND_INH*	LOW
SPDSEL	HIGH	DECMODE	HIGH	MASTER*	MID
SDASEL	LOW	RXRATE	LOW	RFEN	HIGH

1. Apply the settings shown in *Table 12* for the signals in JT32.
2. Apply output from DG2020 to all the four transmit channels. The input to all the transmit channels can be same or different Connect the appropriate control signals.
3. Connect the logic Analyzer TDA700 to read the following receive data lines on
   - JT24, RXDA[7:0] and RXSTA[2:0].
   - JT19, RXDB[7:0] and RXSTB[2:0].
   - JT22, RXDC[7:0] and RXSTC[2:0].
   - JT29, RXDD[7:0] and RXSTD[2:0].
4. Continue with all the steps starting with step 4 of *Section 6.3.1.2* on page 21, replacing step 7 with step 1 of this section.

6.3.3.3 Result Verification

1. Follow the verification steps in *Section 6.3.1.2* on page 21.

7. Schematic Diagram, PCB Layout and BOM (Bill of Material)

Figure 18 to *Figure 23* in Appendix A shows the schematic diagram of the CYP15G0401DXB evaluation board.

Figure 26 to *Figure 33* in Appendix B shows the PCB layout of each layer of the CYP15G0401DXB evaluation board.

The Bill of Material (BOM) of the evaluation board is listed in Appendix C in *Table 14*.

Table 13.Operation Specification of CYP15G0401DXB Eval Board

Description	Min.	Max.	Unit
Operating Voltage	3	3.3	V
Operating Current		1.76	A
Operating Temperature	0	70	°C

Appendix A: Schematic Diagram of CYP15G0401DXB Evaluation Board

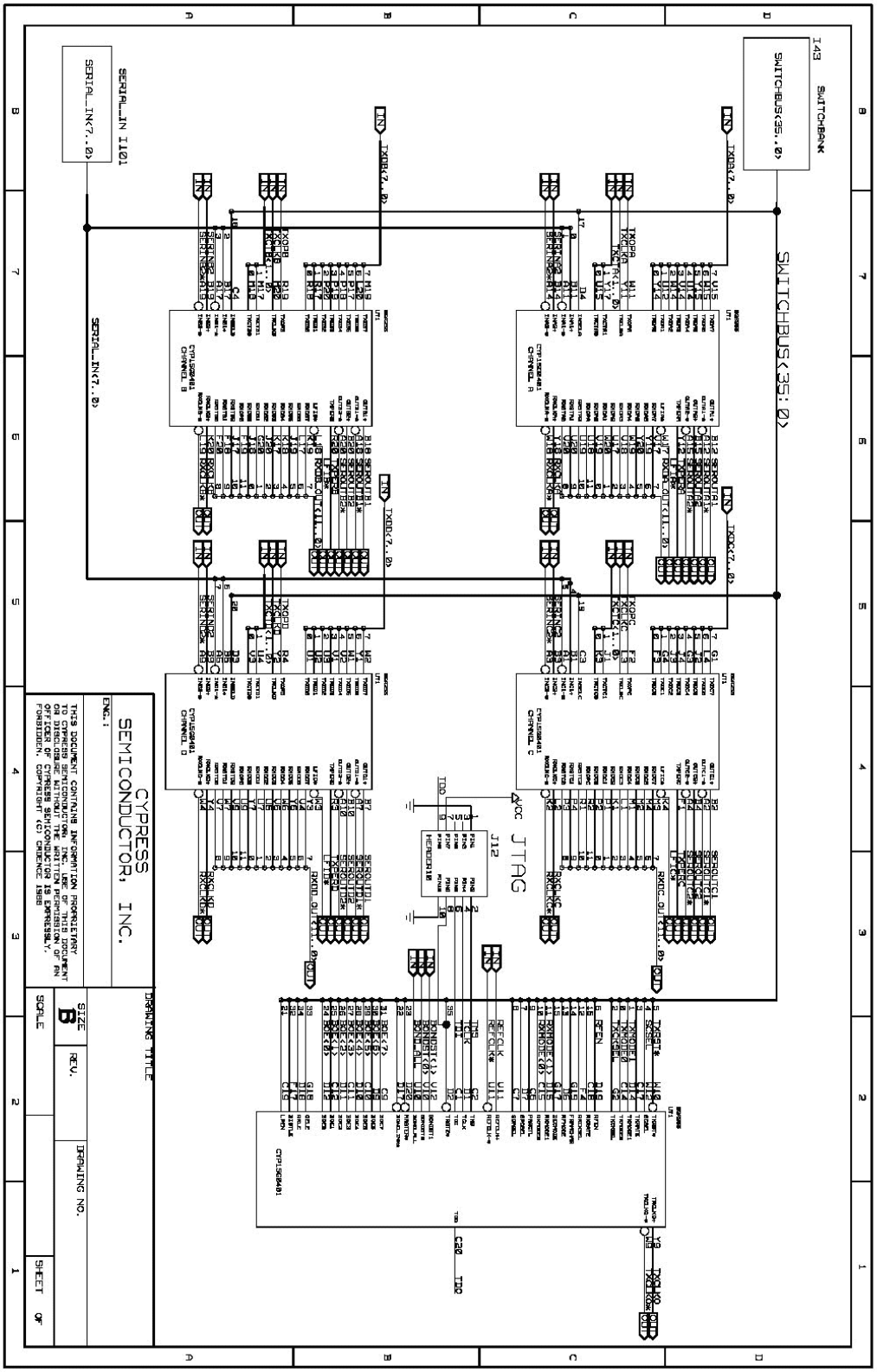

Figure 18. CYP15G0401DXB Eval Board Top-level Schematic

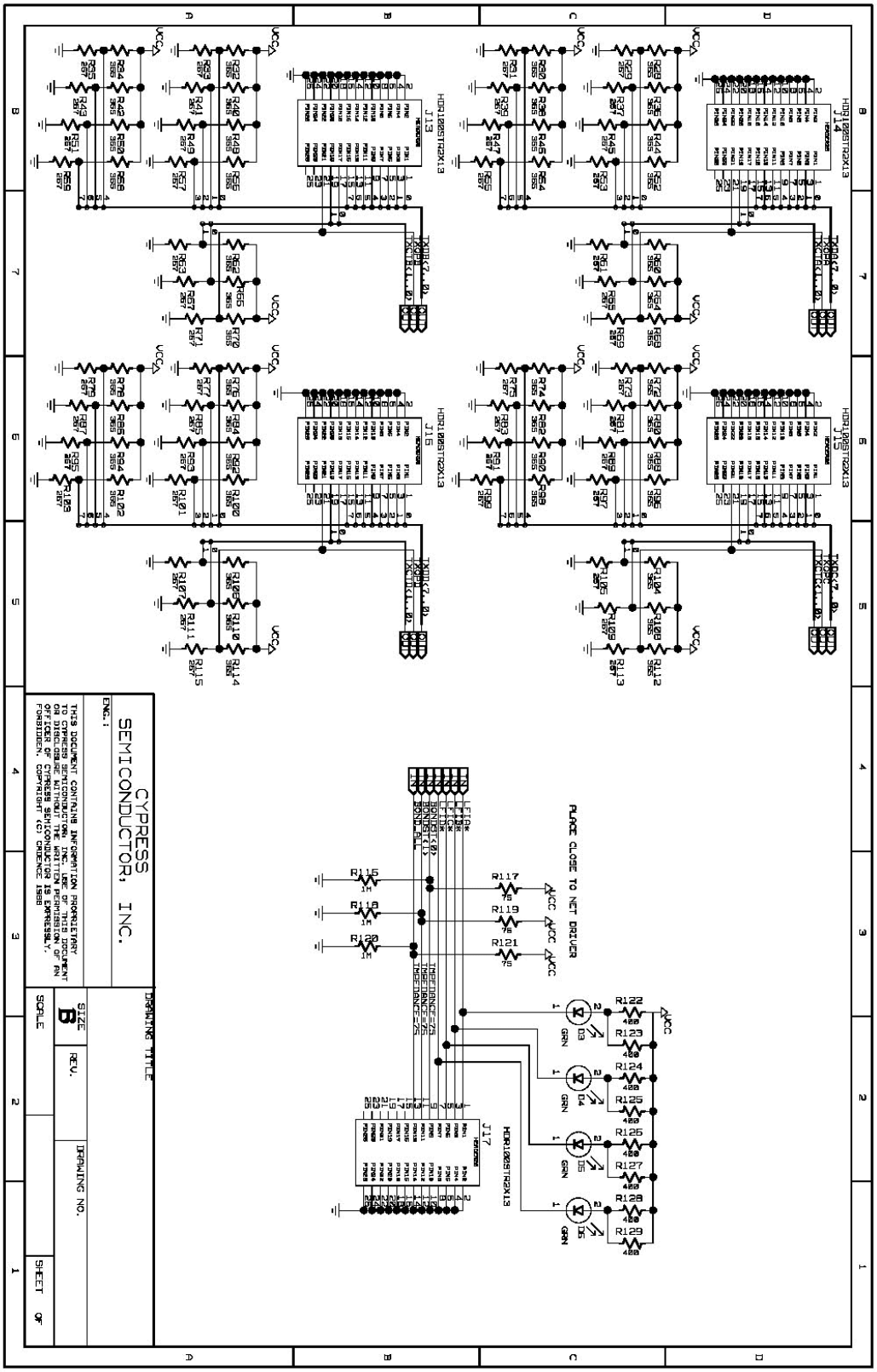

Figure 19. CYP15G0401DXB Eval Board Terminated Transmitter Input Blocks

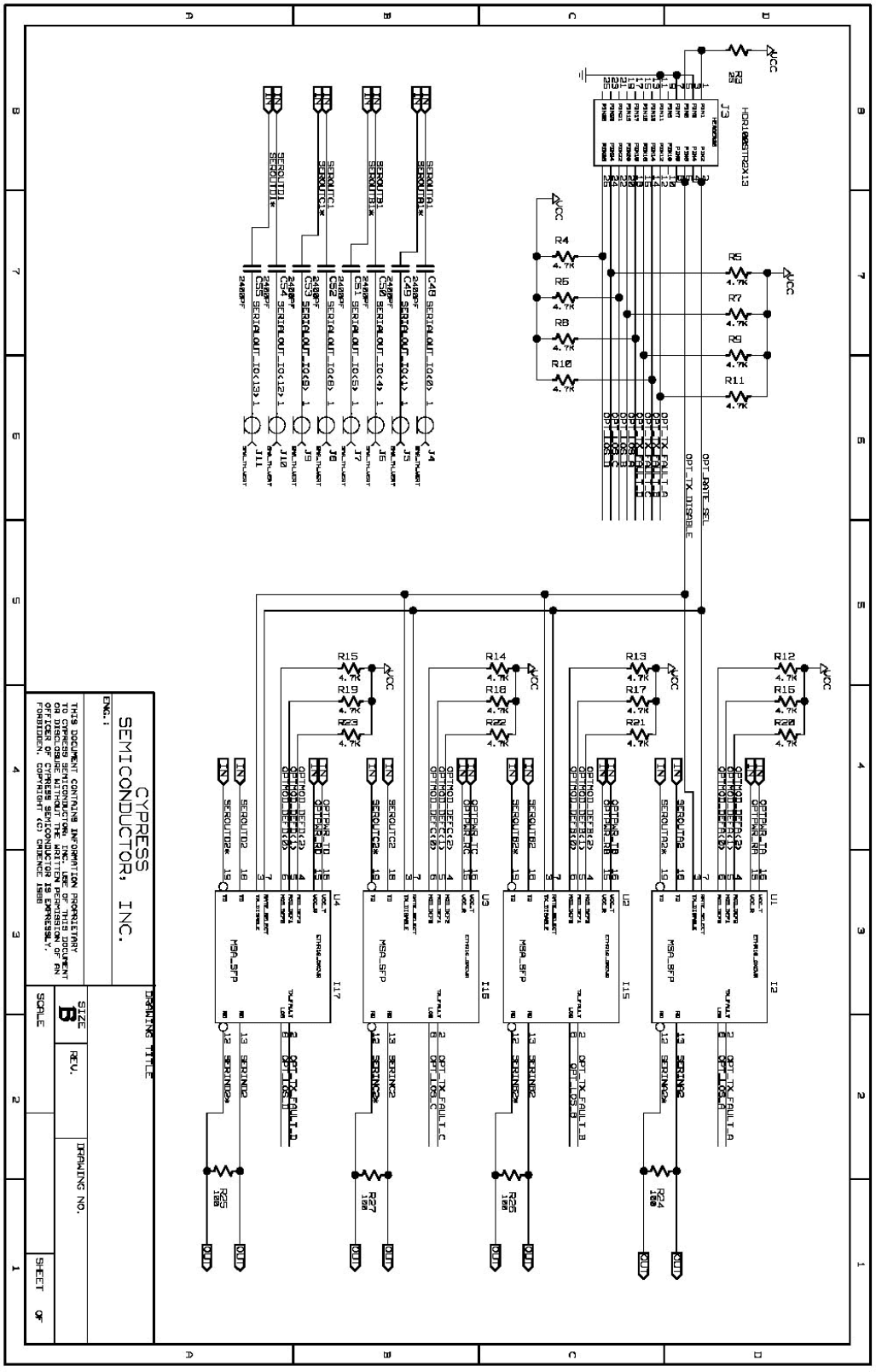

Figure 20. CYP15G0401DXB Eval Board Padded AC-coupled Transmitter Output Blocks

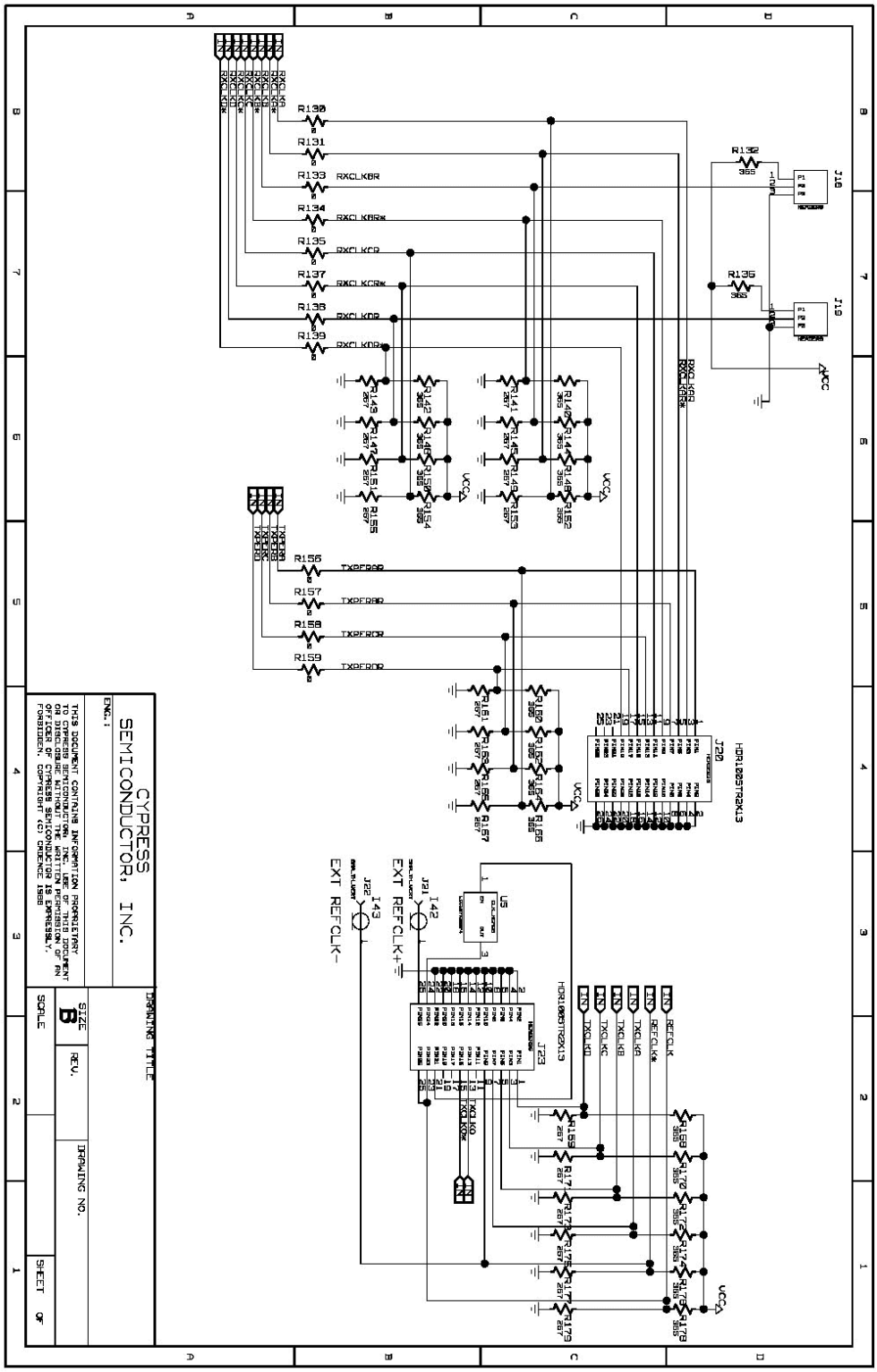

Figure 21. CYP15G0401DXB Eval Board Transmit and Receive Clock Schematics

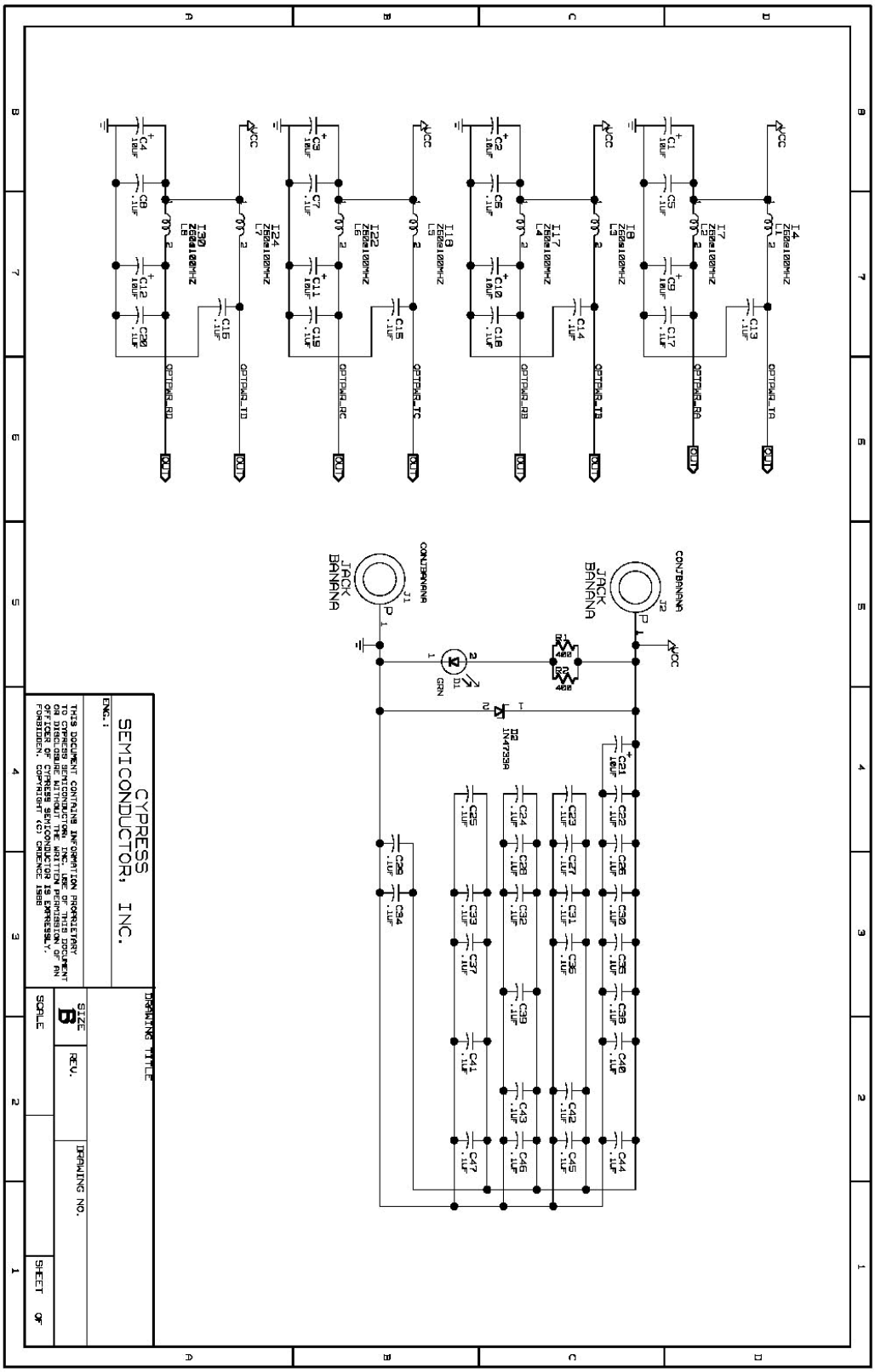

Figure 22. CYP15G0401DXB Eval Board Input Power Schematics

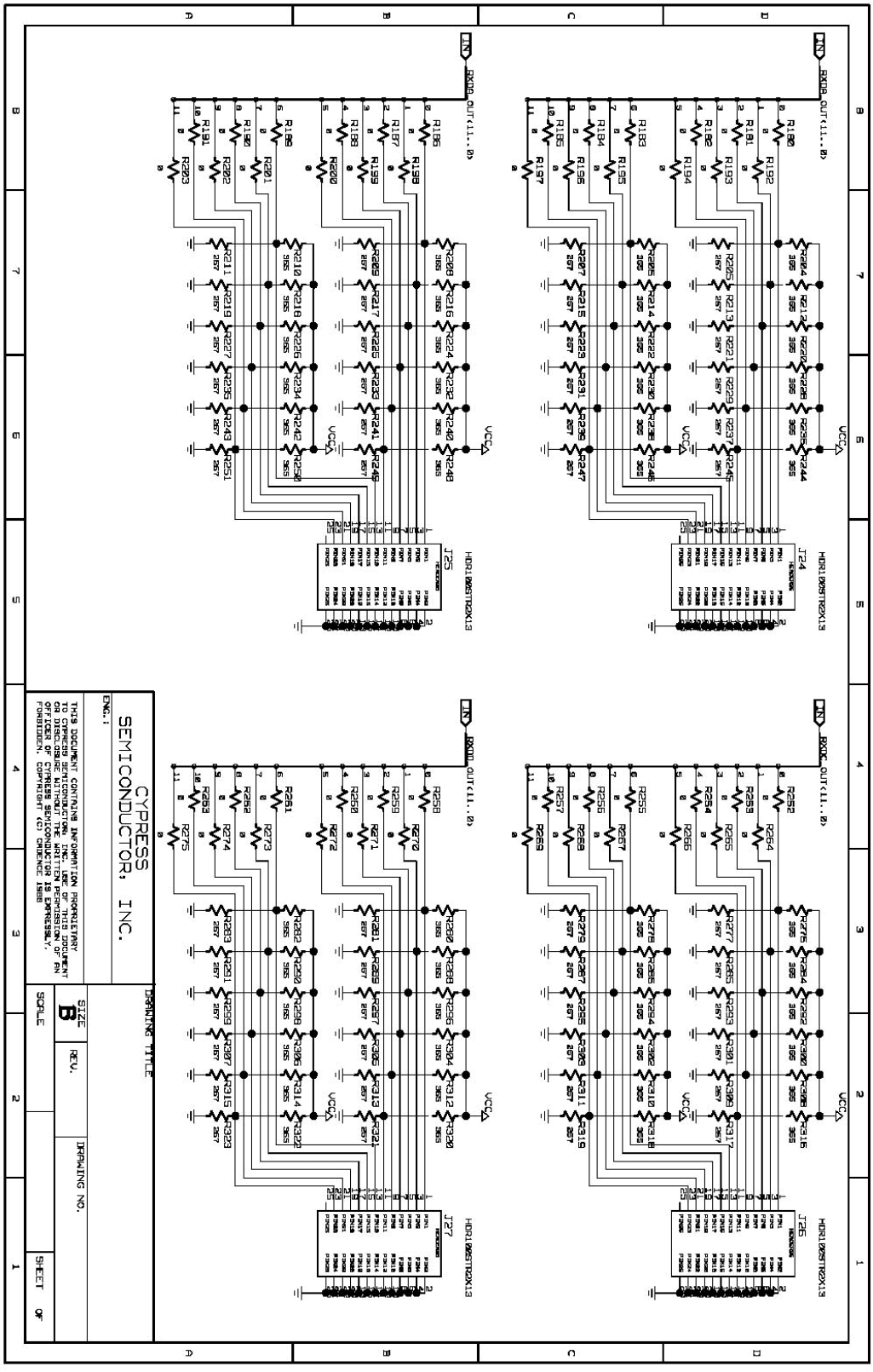

Figure 23. CYP15G0401DXB Eval Board Terminated Receiver Output Blocks

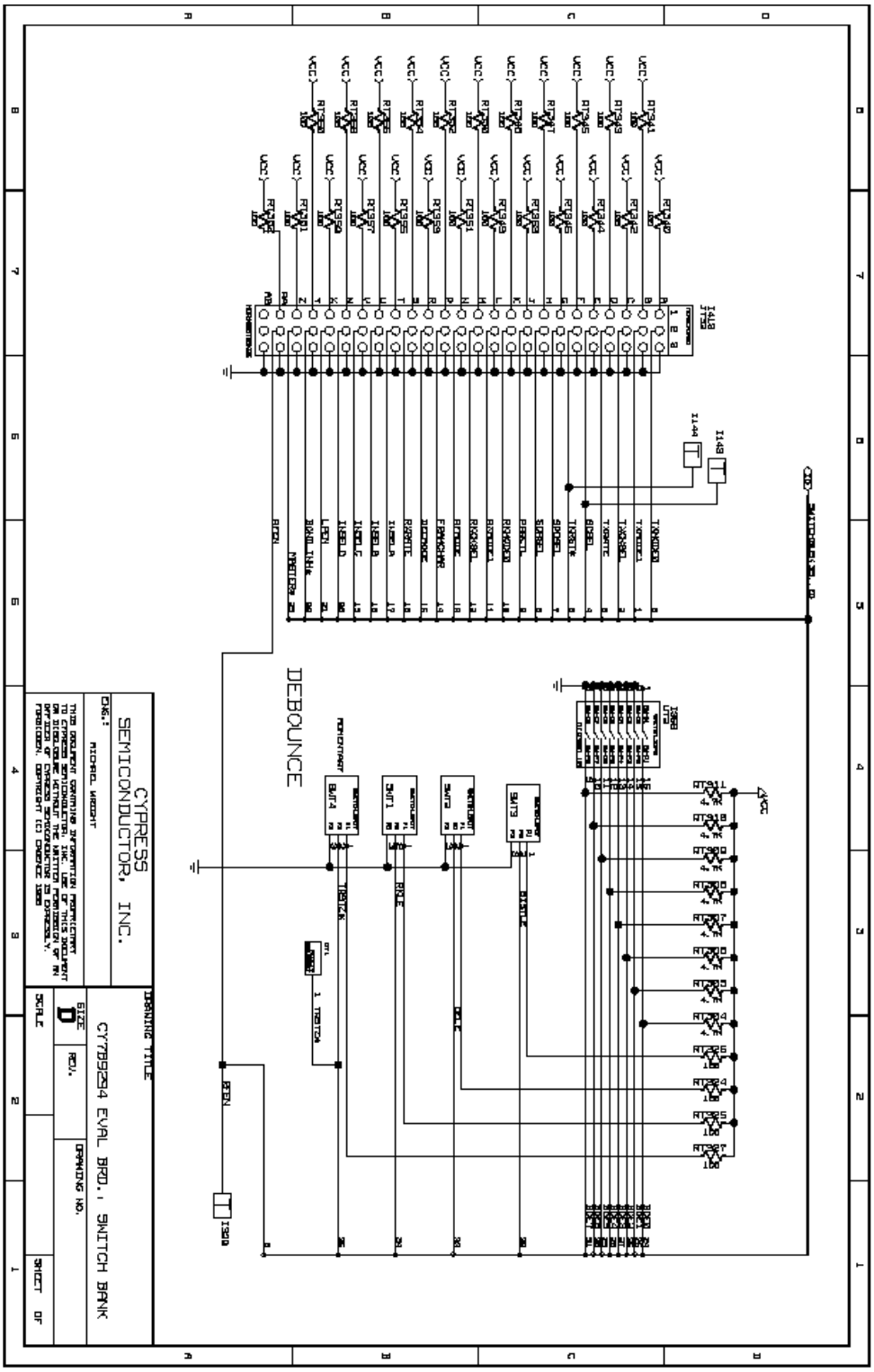

Figure 24. CYP15G0401DXB Eval Board Switch Bank

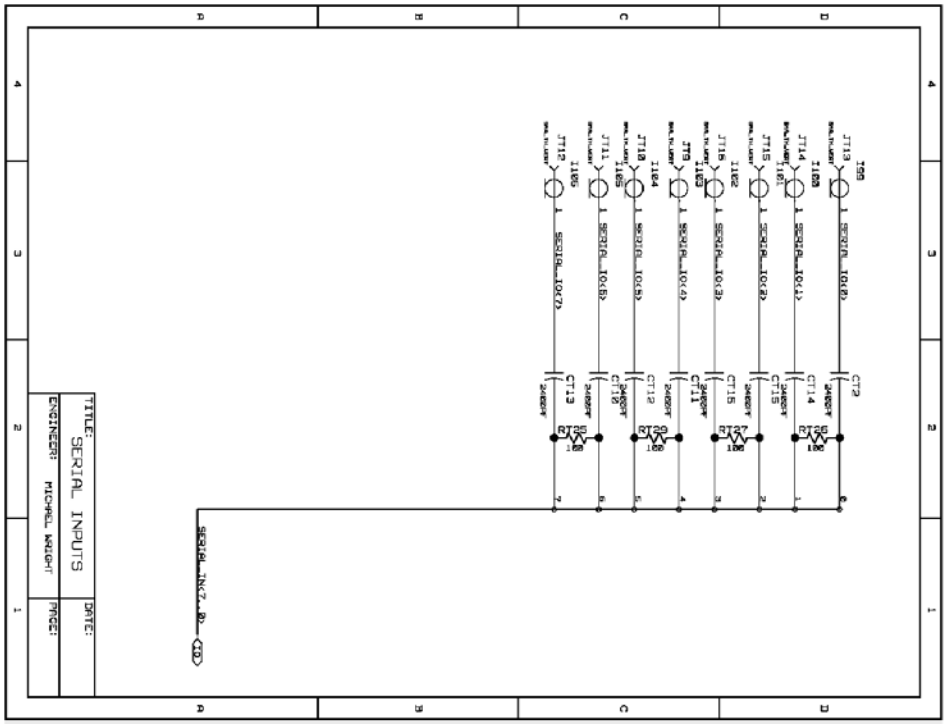

Figure 25. CYP15G0401DXB Eval Board Serial Inputs

Appendix B: PCB Layout for CYP15G0401DXB Evaluation Board

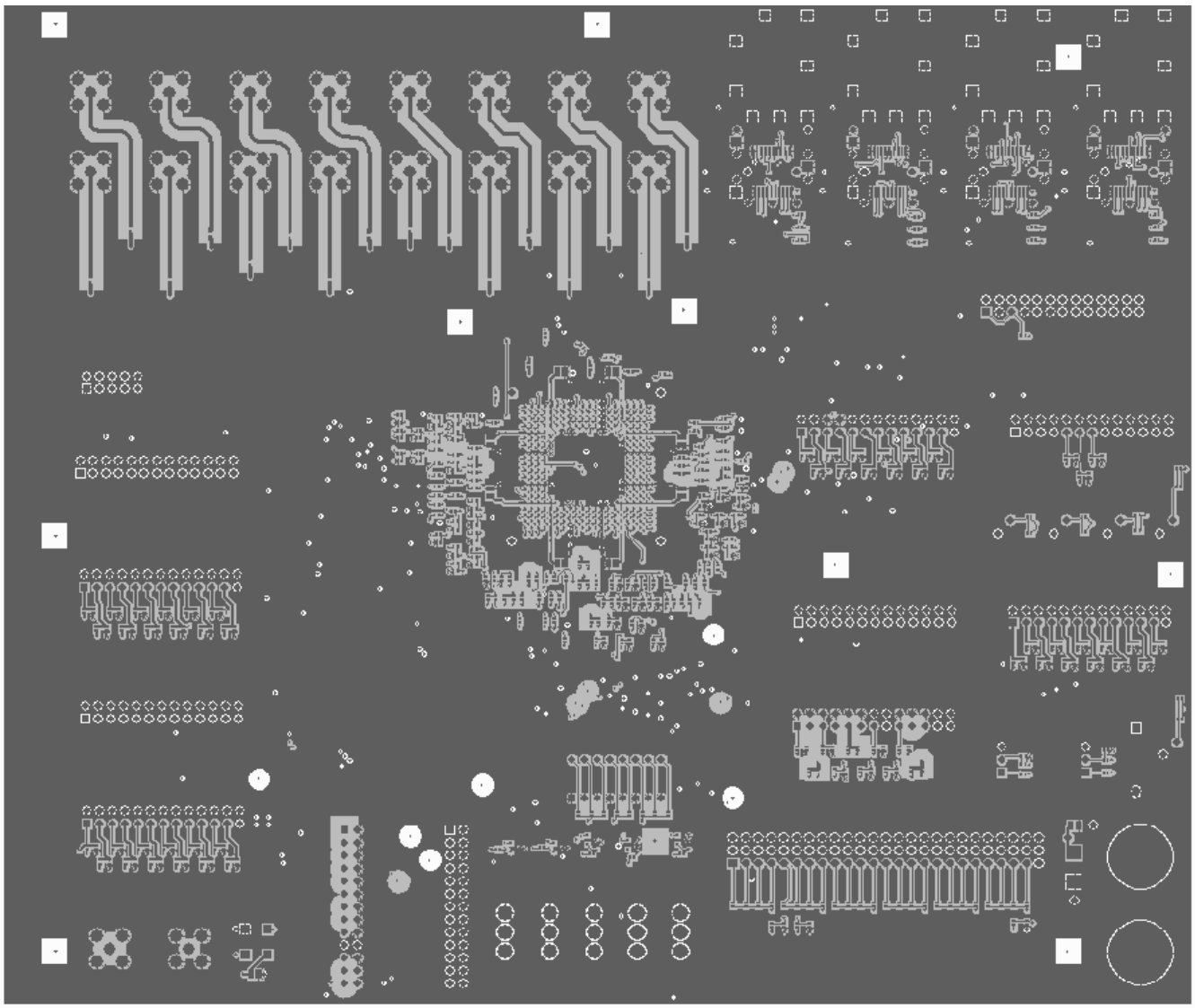

Figure 26. CYP15G0401DXB Eval Board Top Layer

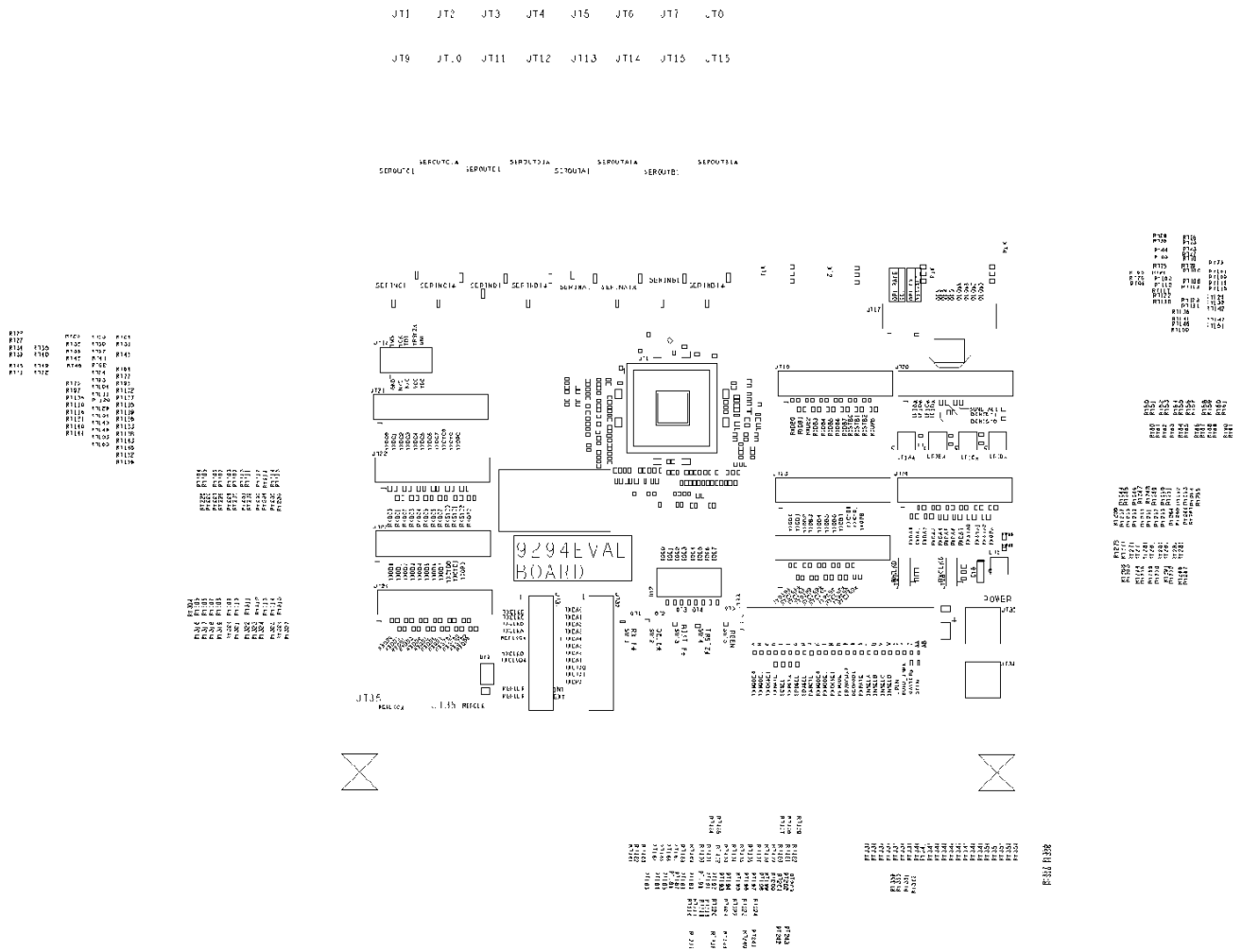

Figure 27. CYP15G0401DXB Eval Board Top Silk Layer

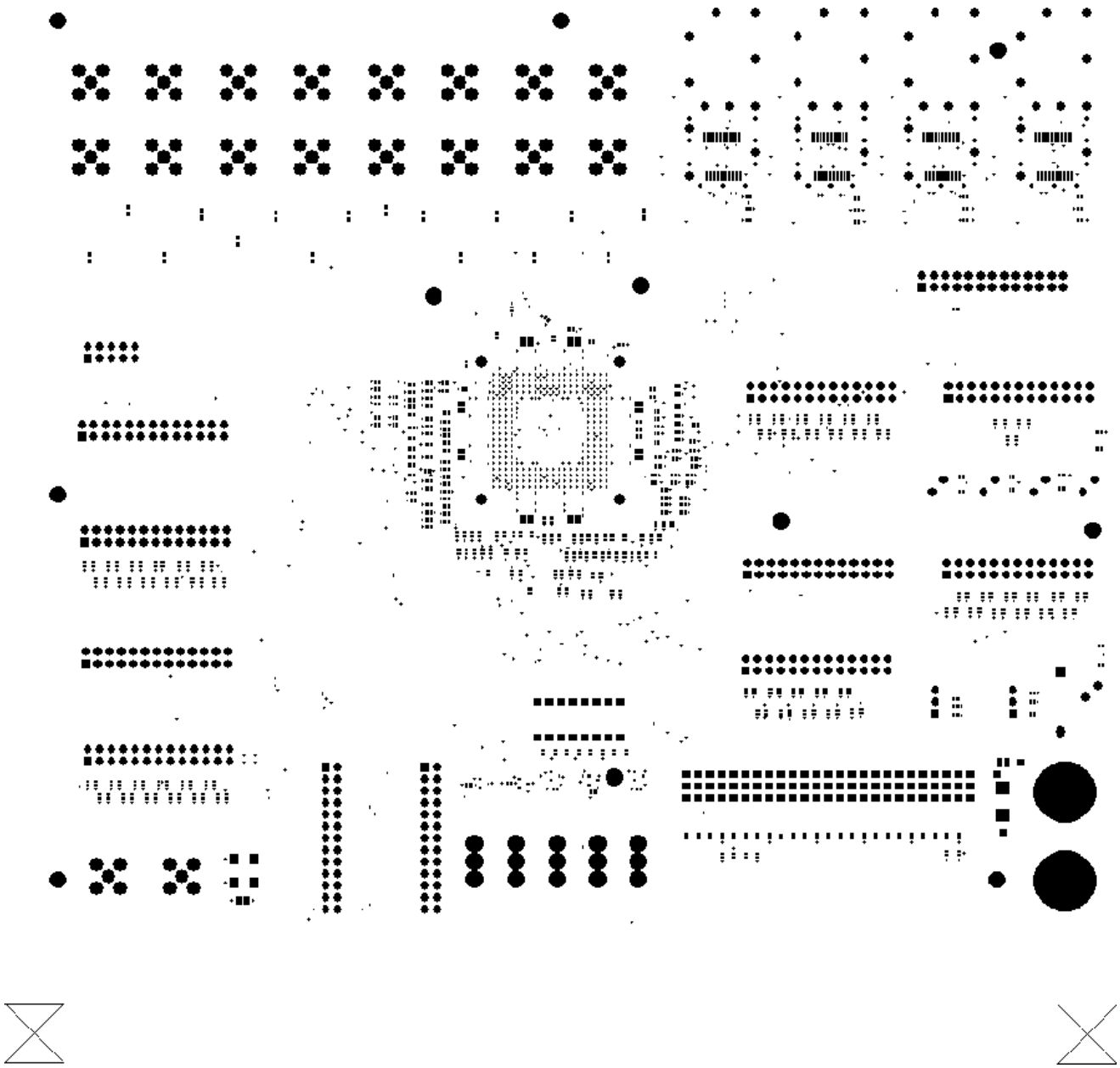

Figure 28. CYP15G0401DXB Eval Board Top Solder Mask Layer

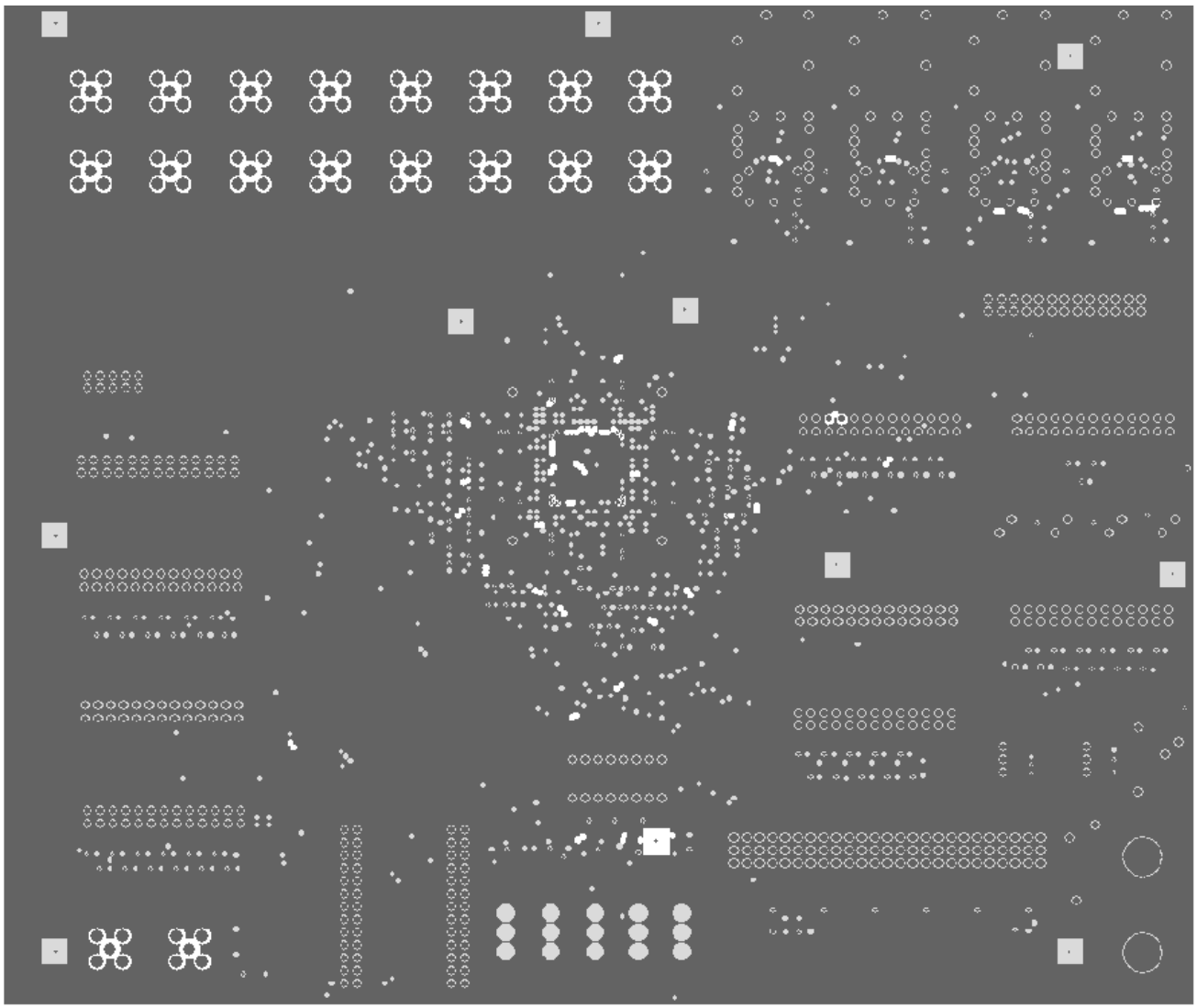

Figure 29. CYP15G0401DXB Eval Board Power Plane Layout

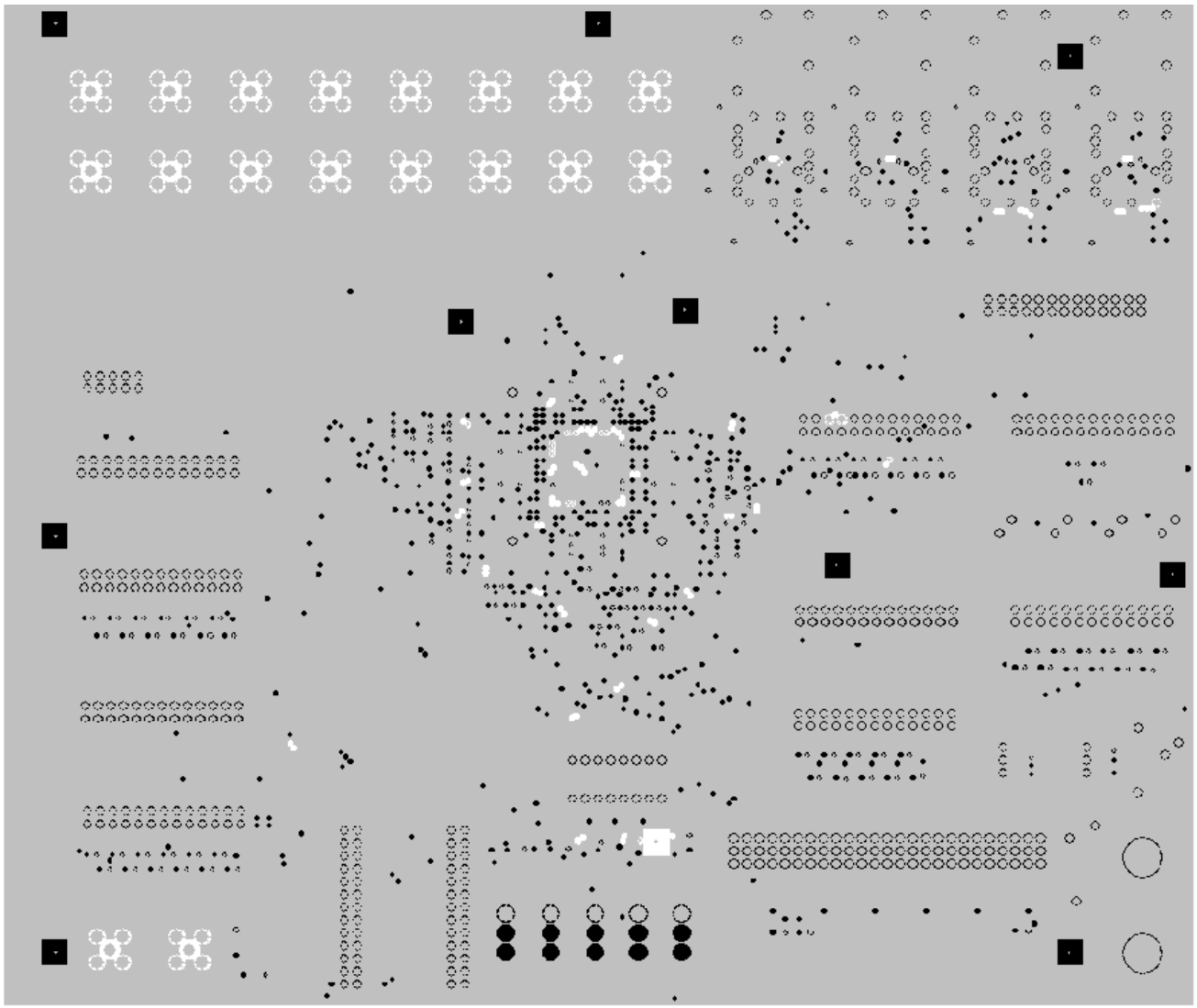

Figure 30. CYP15G0401DXB Eval Board Ground Plane Layout

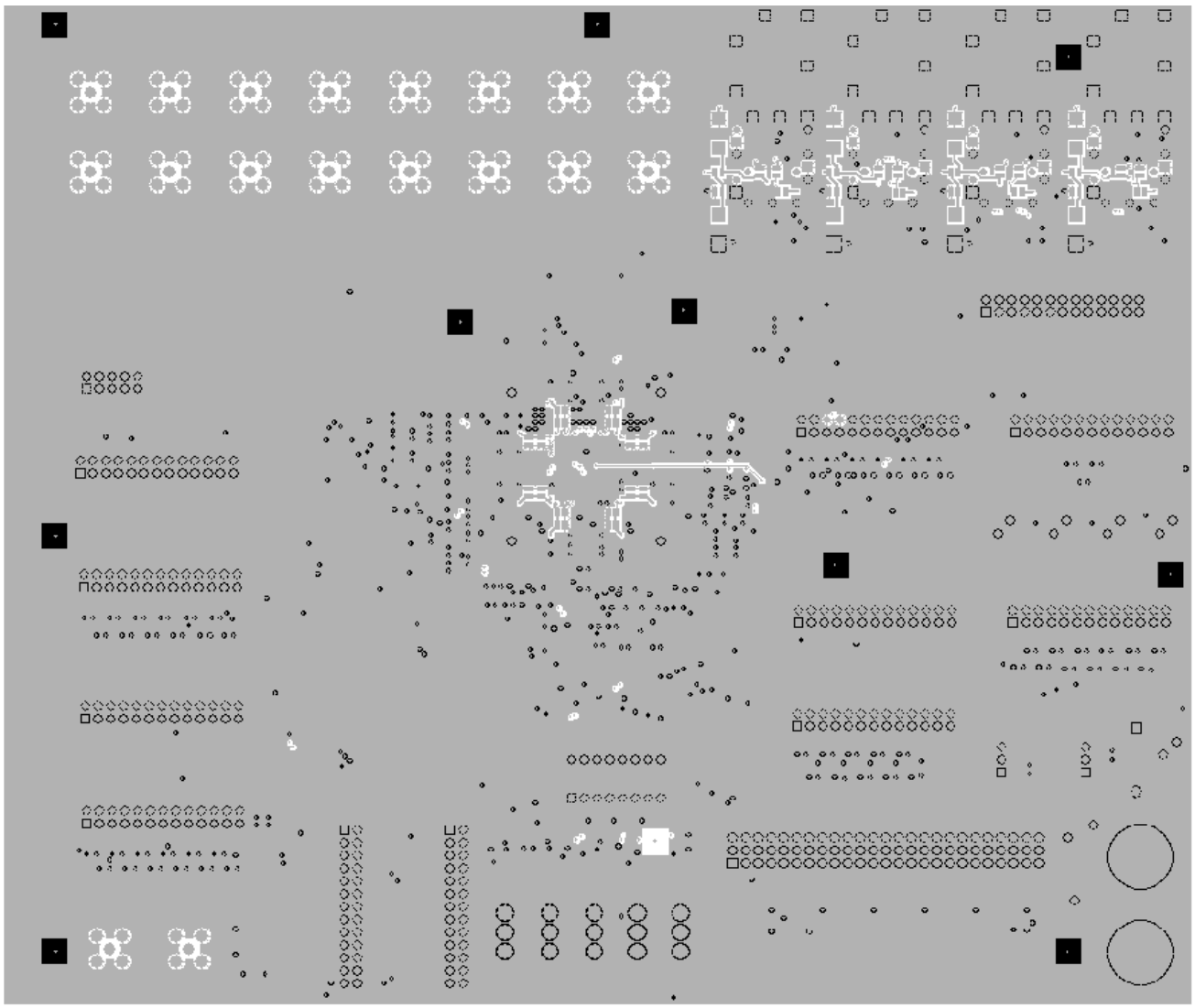

Figure 31. CYP15G0401DXB Eval Board Bottom Layer Layout

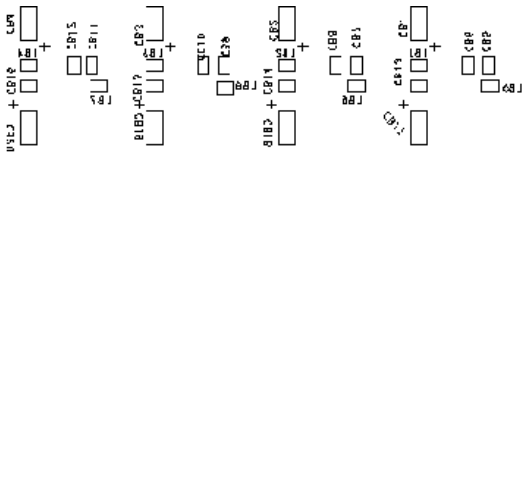

Figure 32. CYP15G0401DXB Eval Board Bottom Silk Layer Layout

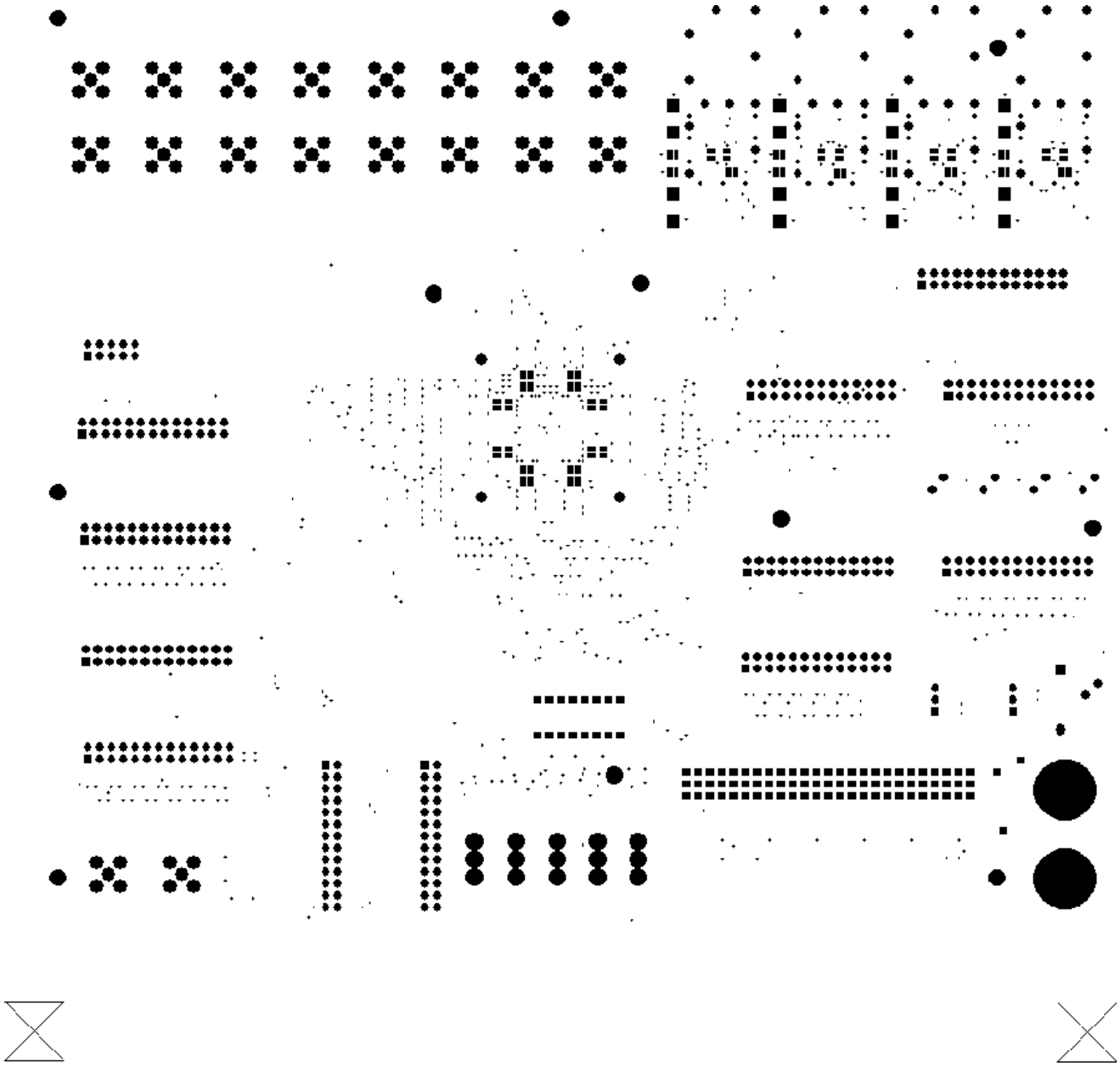

Figure 33. CYP15G0401DXB Eval Board Bottom Solder Mask Layout

Appendix C: Bill Of Material (BOM) CYP15G0401DXB Evaluation Board

Table 14.CYP15G0401DXB Eval Board Bill Of Material

Part Name	Ref Des	Manufacturer	MAN_PN	Qty
CAP-.1UF	CB5-CB16,CB21-CB36,CT17-CT25,CT27	VISHAY	VJ0805Y104KXJAT	38
CAP-SMDC0805V 2400pF	CT1-CT16	DIELECTRIC LABORATORIES	C08BLBB1X5UX	16
CAPPOL-10UF	CB1-CB4,CB17-CB20,CT26	VISHAY	293D106X9010C2T	9
CLK_HCMOS-LCC19 7X295P4	UT3	CONNOR WINFIELD	HSM923-125.00MHZ	1
CY7B9294V_BGA25 6SKT-BGA256SKT	UT1	CYPRESS	CYP15G0401DXB	1
ECONORESET_SOT23	UT2	DALLAS	DS1818R-10	1
ETHR1G_OXCVR-MSA_SFP	XT1-XT4	STRATOS LIGHTWAVE	437-001	4
HEADER10-HDR100 STR2X5	JT18	DIGIKEY	MHB10K-ND	1
HEADER26-HDR100 STR2X5	JT17,JT19-JT26,JT29-JT31	DIGIKEY	S2011-13-ND	12
HEADER3-HDR100STR1X3 DO NOT POPULATE	JT27,JT28	–	–	2
HEADER3X25-HDR100STR3X25	JT32	DIGIKEY	S2011-25-ND	1
INDUCTOR-Z60	LB1-LB8	VISHAY	ILBB-0805 80 25%	8
JACK-BASE-CONJB ANANA	JT33,JT36	DIGIKEY	J147-ND	2
LED-GRN	DT1-DT4,DT6	DIGIKEY	67-1316-ND	5
RES0402-0	RT34,RT36,RT37,RT41,RT44,RT51-RT55,RT70,RT71,RT73,RT78,RT81,RT84,RT86,RT103-RT105,RT110-RT113,RT115,RT118,RT119,RT124,RT128,RT129,RT150,RT156,RT165-RT167,RT173-RT177,RT180,RT185-RT190,RT195-RT198,RT207-RT211,RT224-RT226,RT245,RT364-RT369	VISHAY	CRCW0402000RT2	66
RES0402-100	RT21,RT22,RT23-RT29, RT324-RT327,RT340-RT363	VISHAY	CRCW04021000FB02	37
RES0402-1M DO NOT POPULATE	RT75,RT77,RT107, RT364-RT369	–	–	8
RES0402-267	RT35,RT38-RT40, RT47-RT50,RT59,RT61, RT63,RT65,RT67,RT69,RT75, RT77,RT79,RT80,RT85,RT89, RT91,RT93,RT95,RT97,RT99, RT101,RT102,RT107,RT108, RT117,RT121,RT125-RT127, RT138-RT142,RT149,RT151, RT152,RT157-RT159,RT163, RT164,RT168,RT169,RT171, RT179,RT182,RT184,RT192, RT194,RT200,RT202,RT204,	VISHAY	CRCW04022670FB02	112

Table 14.CYP15G0401DXB Eval Board Bill Of Material (continued)

Part Name	Ref Des	Manufacturer	MAN_PN	Qty
RES0402-267 (continued)	RT206,RT213,RT215,RT217, RT219,RT221,RT223,RT228, RT230,RT232,RT234,RT236, RT238,RT240,RT242,RT244, RT247,RT249,RT251,RT253, RT255,RT257,RT259,RT261, RT263,RT265,RT267,RT269, RT271,RT273,RT275,RT279, RT281,RT283,RT285,RT287-RT289,RT293,RT296,RT298, RT299,RT301,RT313,RT315, RT317,RT319,RT321,RT323, RT329,RT331,RT333,RT335, RT337,RT339	VISHAY	CRCW04022670FB02	112
RES0402-365	RT30-RT33,RT42,RT43, RT45,RT46,RT56-RT58,RT60,RT62,RT64,RT66,RT68,RT72,RT82,RT83,RT87,RT88,RT90,RT92,RT94,RT96,RT98, RT109,RT116,RT120,RT122,RT123,RT130-RT132,RT134,RT137,RT144,RT146,RT148,RT153-RT155,RT160-RT162,RT170,RT172,RT178,RT181,RT183,RT191,RT193,RT199,RT201,RT203, RT205,RT212,RT214,RT216,RT218,RT220,RT222,RT227,RT229,RT231,RT233,RT235,RT237, RT239,RT241,RT243,RT246,RT248,RT250,RT252,RT254,RT256,RT258,RT260,RT262,RT264, RT266,RT268,RT270,RT272,RT274,RT278,RT280,RT282,RT284,RT286,RT290-RT292,RT294, RT295,RT297,RT300,RT302,RT303,RT312,RT314,RT316,RT318,RT320,RT322,RT328,RT330, RT332,RT334,RT336,RT338	VISHAY	CRCW04023650FB02	112
RES0402-4.7K	RT1-RT20,RT304-RT311	VISHAY	CRCW0402472JRT2	28
RES0402-390	RT100,RT114,RT133,RT135,RT136,RT143,RT145,RT147,RT276,RT277	VISHAY	CRCW0402391JRT2	10
RES0402-75	RT74,RT76,RT106	VISHAY	CRCW0402750FB02	3
SMA_THRU-SMA_TH_VERT	JT1-JT16,JT34,JT35	DIGIKEY	ARFX1231-ND	18
SWITCH_DIP8-DIP300_16	QT1	GRAYHILL	76SB08S	1
SWITCH_SPDT	SWT1-SWT3	DIGIKEY	CKN-1078-ND	3
SWITCH_SPDT	SWT4	DIGIKEY	CKN-1079-ND	1
ZENER-5.1V	DT5	DIGIKEY	1N4733ADICT-ND	1

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UG002_B approved kkv 8/12/03