



## CYBL1XXXX Family

# Programmable Radio-on-Chip With BLE (PRoC<sup>®</sup> BLE) Registers Technical Reference Manual (TRM)

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Book 2 of 2

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# Register Mapping



The Register Mapping section discusses the registers and lists all the registers in mapping tables, in address order.

## Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Example	Description
'x' in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset

# 1 BLE Link Layer (BLELL) Registers



This section discusses the BLELL registers. It lists all the registers in mapping tables, in address order.

## 1.1 Register Details

Register Name	Address
<a href="#">BLE_BLELL_COMMAND_REGISTER</a>	0x402E1000
<a href="#">BLE_BLELL_EVENT_INTR</a>	0x402E1008
<a href="#">BLE_BLELL_EVENT_ENABLE</a>	0x402E1010
<a href="#">BLE_BLELL_ADV_PARAMS</a>	0x402E1018
<a href="#">BLE_BLELL_ADV_INTERVAL_TIMEOUT</a>	0x402E101C
<a href="#">BLE_BLELL_ADV_INTR</a>	0x402E1020
<a href="#">BLE_BLELL_ADV_NEXT_INSTANT</a>	0x402E1024
<a href="#">BLE_BLELL_SCAN_INTERVAL</a>	0x402E1028
<a href="#">BLE_BLELL_SCAN_WINDOW</a>	0x402E102C
<a href="#">BLE_BLELL_SCAN_PARAM</a>	0x402E1030
<a href="#">BLE_BLELL_SCAN_INTR</a>	0x402E1038
<a href="#">BLE_BLELL_SCAN_NEXT_INSTANT</a>	0x402E103C
<a href="#">BLE_BLELL_INIT_INTERVAL</a>	0x402E1040
<a href="#">BLE_BLELL_INIT_WINDOW</a>	0x402E1044
<a href="#">BLE_BLELL_INIT_PARAM</a>	0x402E1048
<a href="#">BLE_BLELL_INIT_INTR</a>	0x402E1050
<a href="#">BLE_BLELL_INIT_NEXT_INSTANT</a>	0x402E1054
<a href="#">BLE_BLELL_DEVICE_RAND_ADDR_L</a>	0x402E1058
<a href="#">BLE_BLELL_DEVICE_RAND_ADDR_M</a>	0x402E105C
<a href="#">BLE_BLELL_DEVICE_RAND_ADDR_H</a>	0x402E1060
<a href="#">BLE_BLELL_PEER_ADDR_L</a>	0x402E1068
<a href="#">BLE_BLELL_PEER_ADDR_M</a>	0x402E106C
<a href="#">BLE_BLELL_PEER_ADDR_H</a>	0x402E1070
<a href="#">BLE_BLELL_WL_ADDR_TYPE</a>	0x402E1078
<a href="#">BLE_BLELL_WL_ENABLE</a>	0x402E107C
<a href="#">BLE_BLELL_TRANSMIT_WINDOW_OFFSET</a>	0x402E1080
<a href="#">BLE_BLELL_TRANSMIT_WINDOW_SIZE</a>	0x402E1084

Register Name	Address
BLE_BLELL_DATA_CHANNELS_L0	0x402E1088
BLE_BLELL_DATA_CHANNELS_M0	0x402E108C
BLE_BLELL_DATA_CHANNELS_H0	0x402E1090
BLE_BLELL_DATA_CHANNELS_L1	0x402E1098
BLE_BLELL_DATA_CHANNELS_M1	0x402E109C
BLE_BLELL_DATA_CHANNELS_H1	0x402E10A0
BLE_BLELL_CONN_INTR	0x402E10A8
BLE_BLELL_CONN_STATUS	0x402E10AC
BLE_BLELL_CONN_INDEX	0x402E10B0
BLE_BLELL_WAKEUP_CONFIG	0x402E10B8
BLE_BLELL_WAKEUP_CONTROL	0x402E10C0
BLE_BLELL_CLOCK_CONFIG	0x402E10C4
BLE_BLELL_TIM_COUNTER_L	0x402E10C8
BLE_BLELL_POC_REG__TIM_CONTROL	0x402E10D8
BLE_BLELL_ADV_TX_DATA_FIFO	0x402E10E0
BLE_BLELL_ADV_SCN_RSP_TX_FIFO	0x402E10E8
BLE_BLELL_INIT_SCN_ADV_RX_FIFO	0x402E10F8
BLE_BLELL_CONN_INTERVAL	0x402E1100
BLE_BLELL_SUP_TIMEOUT	0x402E1104
BLE_BLELL_SLAVE_LATENCY	0x402E1108
BLE_BLELL_CE_LENGTH	0x402E110C
BLE_BLELL_PDU_ACCESS_ADDR_L_REGISTER	0x402E1110
BLE_BLELL_PDU_ACCESS_ADDR_H_REGISTER	0x402E1114
BLE_BLELL_CONN_CE_INSTANT	0x402E1118
BLE_BLELL_CE_CNFG_STS_REGISTER	0x402E111C
BLE_BLELL_NEXT_CE_INSTANT	0x402E1120
BLE_BLELL_CONN_CE_COUNTER	0x402E1124
BLE_BLELL_DATA_LIST_SENT_UPDATE__STATUS	0x402E1128
BLE_BLELL_DATA_LIST_ACK_UPDATE__STATUS	0x402E112C
BLE_BLELL_DATA_MEM_DESCRIPTOR0	0x402E1140
BLE_BLELL_DATA_MEM_DESCRIPTOR1	0x402E1144
BLE_BLELL_DATA_MEM_DESCRIPTOR2	0x402E1148
BLE_BLELL_DATA_MEM_DESCRIPTOR3	0x402E114C
BLE_BLELL_DATA_MEM_DESCRIPTOR4	0x402E1150
BLE_BLELL_WINDOW_WIDEN_INTVL	0x402E1160
BLE_BLELL_WINDOW_WIDEN_WINOFF	0x402E1164
BLE_BLELL_LE_RF_TEST_MODE	0x402E1170
BLE_BLELL_DTM_RX_PKT_COUNT	0x402E1174
BLE_BLELL_TXRX_HOP	0x402E1188
BLE_BLELL_TX_RX_ON_DELAY	0x402E1190
BLE_BLELL_DEV_PUB_ADDR_L	0x402E11C0
BLE_BLELL_DEV_PUB_ADDR_M	0x402E11C4

Register Name	Address
BLE_BLELL_DEV_PUB_ADDR_H	0x402E11C8
BLE_BLELL_ADV_CH_TX_POWER	0x402E11CC
BLE_BLELL_OFFSET_TO_FIRST_INSTANT	0x402E11D0
BLE_BLELL_ADV_CONFIG	0x402E11D4
BLE_BLELL_SCAN_CONFIG	0x402E11D8
BLE_BLELL_INIT_CONFIG	0x402E11DC
BLE_BLELL_CONN_CONFIG	0x402E11E0
BLE_BLELL_CONN_CH_TX_POWER	0x402E11E4
BLE_BLELL_CONN_PARAM1	0x402E11E8
BLE_BLELL_CONN_PARAM2	0x402E11EC
BLE_BLELL_CONN_INTR_MASK	0x402E11F0
BLE_BLELL_SLAVE_TIMING_CONTROL	0x402E11F4
BLE_BLELL_RECEIVE_TRIG_CTRL	0x402E11F8
BLE_BLELL_DPLL_CONFIG	0x402E1258
BLE_BLELL_WHITELIST_BASE_ADDR	0x402E1340
BLE_BLELL_CONN_UPDATE_NEW_INTERVAL	0x402E13A4
BLE_BLELL_CONN_UPDATE_NEW_LATENCY	0x402E13A8
BLE_BLELL_CONN_UPDATE_NEW_SUP_TO	0x402E13AC
BLE_BLELL_CONN_UPDATE_NEW_SL_INTERVAL	0x402E13B0
BLE_BLELL_CONN_REQ_WORD0	0x402E13C0
BLE_BLELL_CONN_REQ_WORD1	0x402E13C4
BLE_BLELL_CONN_REQ_WORD2	0x402E13C8
BLE_BLELL_CONN_REQ_WORD3	0x402E13CC
BLE_BLELL_CONN_REQ_WORD4	0x402E13D0
BLE_BLELL_CONN_REQ_WORD5	0x402E13D4
BLE_BLELL_CONN_REQ_WORD6	0x402E13D8
BLE_BLELL_CONN_REQ_WORD7	0x402E13DC
BLE_BLELL_CONN_REQ_WORD8	0x402E13E0
BLE_BLELL_CONN_REQ_WORD9	0x402E13E4
BLE_BLELL_CONN_REQ_WORD10	0x402E13E8
BLE_BLELL_CONN_REQ_WORD11	0x402E13EC
BLE_BLELL_PACKET_COUNTER0	0x402E1400
BLE_BLELL_PACKET_COUNTER1	0x402E1404
BLE_BLELL_PACKET_COUNTER2	0x402E1408
BLE_BLELL_IV_MASTER0	0x402E1410
BLE_BLELL_IV_MASTER1	0x402E1414
BLE_BLELL_IV_SLAVE0	0x402E1418
BLE_BLELL_IV_SLAVE1	0x402E141C
BLE_BLELL_ENC_KEY0	0x402E1420
BLE_BLELL_ENC_KEY1	0x402E1424
BLE_BLELL_ENC_KEY2	0x402E1428
BLE_BLELL_ENC_KEY3	0x402E142C

Register Name	Address
BLE_BLELL_ENC_KEY4	0x402E1430
BLE_BLELL_ENC_KEY5	0x402E1434
BLE_BLELL_ENC_KEY6	0x402E1438
BLE_BLELL_ENC_KEY7	0x402E143C
BLE_BLELL_DATA0	0x402E1440
BLE_BLELL_DATA1	0x402E1444
BLE_BLELL_DATA2	0x402E1448
BLE_BLELL_DATA3	0x402E144C
BLE_BLELL_DATA4	0x402E1450
BLE_BLELL_DATA5	0x402E1454
BLE_BLELL_DATA6	0x402E1458
BLE_BLELL_DATA7	0x402E145C
BLE_BLELL_DATA8	0x402E1460
BLE_BLELL_DATA9	0x402E1464
BLE_BLELL_DATA10	0x402E1468
BLE_BLELL_DATA11	0x402E146C
BLE_BLELL_DATA12	0x402E1470
BLE_BLELL_DATA13	0x402E1474
BLE_BLELL_MIC_IN0	0x402E1478
BLE_BLELL_MIC_IN1	0x402E147C
BLE_BLELL_MIC_OUT0	0x402E1480
BLE_BLELL_MIC_OUT1	0x402E1484
BLE_BLELL_ENC_PARAMS	0x402E1488
BLE_BLELL_ENC_CONFIG	0x402E1490
BLE_BLELL_ENC_INTR_EN	0x402E1498
BLE_BLELL_ENC_INTR	0x402E14A0
BLE_BLELL_CONN_TXMEM_BASE_ADDR	0x402E1600
BLE_BLELL_CONN_RXMEM_BASE_ADDR	0x402E1800
BLE_BLELL_PDU_RESP_TIMER	0x402E1A04
BLE_BLELL_NEXT_RESP_TIMER_EXP	0x402E1A08
BLE_BLELL_NEXT_SUP_TO	0x402E1A0C
BLE_BLELL_LLH_FEATURE_CONFIG	0x402E1A10
BLE_BLELL_WIN_MIN_STEP_SIZE	0x402E1A14
BLE_BLELL_SLV_WIN_ADJ	0x402E1A18
BLE_BLELL_SL_CONN_INTERVAL	0x402E1A1C
BLE_BLELL_LE_PING_TIMER_ADDR	0x402E1A20
BLE_BLELL_LE_PING_TIMER_OFFSET	0x402E1A24
BLE_BLELL_LE_PING_TIMER_NEXT_EXP	0x402E1A28
BLE_BLELL_LE_PING_TIMER_WRAP_COUNT	0x402E1A2C
BLE_BLELL_TX_EN_EXT_DELAY	0x402E1E00
BLE_BLELL_TX_RX_SYNTH_DELAY	0x402E1E04



## 1.1.1 BLE\_BLELL\_COMMAND\_REGISTER

Instruction Register

Address: 0x402E1000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	COMMAND [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits      Name      Description

## 1.1.1 BLE\_BLELL\_COMMAND\_REGISTER (continued)

7 : 0	COMMAND	<p>8-bit command from firmware to the link layer controller. See below for the list of instructions and their opcodes. The instruction results in the link layer hardware starting/stopping an operation.</p> <p>Notes on use</p> <p>Few of the commands will require other configuration registers to be set, before the command is written. Refer to the description below for details of the registers to be set before setting these instructions.</p> <hr/> <p>Command Opcode Description</p> <p>START_ADV - 0x40: Start Advertiser operation. The associated Advertiser configuration registers are programmed before the command is issued. [refer to llh_set_adv_parameters function in lec_llh/simulation/llh_driver/ll_hardware_api.c file]</p> <p>STOP_ADV - 0x41: Stop advertiser operation.</p> <p>START_SCAN - 0x42: Start scanner operation. The associated configuration registers must be programmed before the command is issued. [refer to llh_set_scan_parameters function in lec_llh/simulation/llh_driver/ll_hardware_api.c file]</p> <p>STOP_SCAN - 0x43: Stop the scanner operation.</p> <p>START_INIT - 0x44: Start connection creation operation. The associated configuration registers must be programmed before the command is issued. [refer to create_connection function in lec_llh/simulation/llh_driver/ll_hardware_api.c file]</p> <p>STOP_INIT - 0x45: Cancel connection creation operation.</p> <p>DTM_TX_START - 0x46: Start Direct Test Mode Transmit Test. The associated configuration registers must be programmed before the command is issued. [refer to dtm_tx_test function in lec_llh/simulation/llh_driver/ll_hardware_api.c file]</p> <p>DTM_RX_START - 0x47: Start Direct Test Mode Receive Test. The associated configuration registers must be programmed before the command is issued. [refer to dtm_rx_test function in lec_llh/simulation/llh_driver/ll_hardware_api.c file]</p> <p>DTM_STOP - 0x48: Stop Direct Test Mode.</p> <p>UPDATE_CHAN_MAP - 0x4B: Update channel map for the connection.</p> <p>UPDATE_CONN_PROC - 0x4C: Start connection update procedure for the connection.</p> <p>PACKET_RECEIVED - 0x4D: Indicates a received connection packet is read by firmware from connection receive FIFO.</p> <p>ENTER_DSM - 0x50: Enter deep sleep mode.</p> <p>CORE_CLK_OFF - 0x51: Enter sleep mode.</p> <p>CORE_CLK_ON - 0x52: Exit sleep mode</p> <p>ENC_CLK_ON - 0x53: Turn on clock to encryption block</p> <p>ENC_CLK_OFF - 0x54: Turn off clock to encryption block</p> <p>ADV_CLK_ON - 0x55: Turn on clock to advertiser block in NAP mode.</p> <p>ADV_CLK_OFF - 0x56: Turn off clock to advertiser block in NAP mode.</p> <p>SCAN_CLK_ON - 0x57: Turn on clock to scanner block in NAP mode.</p> <p>SCAN_CLK_OFF - 0x58: Turn off clock to scanner block in NAP mode.</p> <p>INIT_CLK_ON - 0x59: Turn on clock to initiator block in NAP mode.</p> <p>INIT_CLK_OFF - 0x5a: Turn off clock to initiator block in NAP mode.</p> <p>CONN_CLK_ON - 0x5b: Turn on clock to connection block in NAP mode.</p> <p>CONN_CLK_OFF - 0x5c: Turn off clock to connection block in NAP mode.</p> <p>UPDATE_CONN - 0x68: Update connection parameters. Deprecated.</p> <p>KILL_CONN - 0x70: Kill connection immediately.</p> <p>KILL_CONN_AFTER_TX - 0x71: Kill connection after a transmit operation is over.</p> <p>RESP_TIMER_ON - 0x72: Start PDU response timer. The PDU_RESP_TIMER register must be programmed with timeout value before issuing this command.</p> <p>RESP_TIMER_OFF - 0x73: Stop PDU response timer.</p> <p>RESET_READ_PTR - 0x74: Reset the white list memory read pointer to 0.</p> <p>CONN_PING_TIMER_ON - 0x75: Start connection ping timer</p> <p>CONN_PING_TIMER_OFF - 0x76: Stop connection ping timer</p> <p>SOFT_RESET - 0x80: Software reset. Resets all the hardware registers (except a few registers related to radio initialization).</p> <p>RESET_US_COUNTER - 0xC3: Reset microsecond counter</p> <p>Default Value: 0</p>
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## 1.1.2 BLE\_BLELL\_EVENT\_INTR

Event(Interrupt) status and Clear register

Address: 0x402E1008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	RW1C	RW1C	R	R	R	R
HW Access	None	RW	RW	RW	RW	RW	RW	RW
Name	None	ENC_INTR	DSM_INTR	SM_INTR	CONN_INTR	INIT_INTR	SCAN_INTR	ADV_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	ENC_INTR	Encryption module interrupt. Default Value: 0
5	DSM_INTR	Read: Deep sleep mode exit interrupt. This bit is set, when link layer hardware exits from deep sleep mode. Write: Clear deep sleep mode exit interrupt. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
4	SM_INTR	Read: Sleep-mode-exit interrupt. This bit is set, when link layer hardware exits from sleep mode. Write: Clear sleep-mode-exit interrupt. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
3	CONN_INTR	Connection interrupt. If bit is set to 1, it indicates an event occurred in the connection operation. This interrupt is aggregation of interrupts for all the connections. The source of the event for the specific connection, needs to be read from the CONN_INTR register specific to the connection. This bit is cleared, when firmware clears ALL interrupts by writing to the CONN_INTR register. Default Value: 0

### 1.1.2 BLE\_BLELL\_EVENT\_INTR (continued)

2	INIT_INTR	Initiator interrupt. If bit is set to 1, it indicates an event occurred in the initiating procedure. The source of the event needs to be read from the INIT_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the INIT_INTR register. Default Value: 0
1	SCAN_INTR	Scanner interrupt. If bit is set to 1, it indicates an event occurred in the scanning procedure. The source of the event needs to be read from the SCAN_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the SCAN_INTR register. Default Value: 0
0	ADV_INTR	Advertiser interrupt. If bit is set to 1, it indicates an event occurred in the advertising procedure. The source of the event needs to be read from the ADV_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the ADV_INTR register. Default Value: 0

### 1.1.3 BLE\_BLELL\_EVENT\_ENABLE

Event indications enable.

Address: 0x402E1010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	ENC_INT_EN	DSM_INT_EN	SM_INT_EN	CONN_INT_EN	INIT_INT_EN	SCN_INT_EN	ADV_INT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	ENC_INT_EN	Encryption module interrupt enable. 1 Enable encryption module interrupt to firmware. 0 disable encryption module interrupt to firmware. Default Value: 0
5	DSM_INT_EN	Deep Sleep-mode-exit interrupt enable. 1 enable deep sleep mode exit event to interrupt the firmware. 0 disable deep sleep mode exit interrupt to firmware. Default Value: 0
4	SM_INT_EN	Sleep-mode-exit interrupt enable. 1 enable sleep mode exit event to interrupt the firmware. 0 disable sleep mode exit interrupt to firmware. Default Value: 0
3	CONN_INT_EN	Connection interrupt enable. 1 enable connection procedure to interrupt the firmware. 0 disable connection procedure interrupt to firmware. Default Value: 0

### 1.1.3 BLE\_BLELL\_EVENT\_ENABLE (continued)

2	INIT_INT_EN	Initiator interrupt enable. 1 enable initiator procedure to interrupt the firmware. 0 disable initiator procedure interrupt to firmware. Default Value: 0
1	SCN_INT_EN	Scanner interrupt enable. 1 enable scan procedure to interrupt the firmware. 0 disable scan procedure interrupt to firmware. Default Value: 0
0	ADV_INT_EN	Advertiser interrupt enable. 1 enable advertiser procedure to interrupt the firmware. 0 disable advertiser procedure interrupt to firmware. Default Value: 0



## 1.1.4 BLE\_BLELL\_ADV\_PARAMS

Advertising parameters register.

Address: 0x402E1018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW		RW		RW
HW Access	R			R		R		R
Name	ADV_CHANNEL_MAP [7:5]			ADV_FILT_POLICY [4:3]		ADV_TYPE [2:1]		TX_ADDR

  

Bits	15	14	13	12	11	10	9	8
SW Access	R	None				RW	None	RW
HW Access	RW	None				R	None	R
Name	RCV_TX_A DDR	None [14:11]				ADV_LOW_ DUTY_CYC LE	None	RX_ADDR

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	RCV_TX_ADDR	Transmit address field of the received packet extracted from the receive packet. This field is used by firmware to report peer_addr_type parameter in the connection complete event. Default Value: 0
10	ADV_LOW_DUTY_CYCLE	This bit field is used to specify to the Controller the Low Duty Cycle connectable directed advertising variant being used. 1 Low Duty Cycle Connectable Directed Advertising. 0 High Duty Cycle Connectable Directed Advertising. Default Value: 0
8	RX_ADDR	Peer addresses type. This is the Direct_Address_type field programmed, only if ADV_DIRECT_IND type is sent. 1 Rx addr type is random. 0 Rx addr type is public Default Value: 0

### 1.1.4 BLE\_BLELL\_ADV\_PARAMS (continued)

7 : 5	ADV_CHANNEL_MAP	Advertising channel map indicates the advertising channels used for advertising. By setting the bit, corresponding channel is enabled for use. Atleast one channel bit should be set. 7 - enable channel 39. 6 - enable channel 38. 5 - enable channel 37. Default Value: 7
4 : 3	ADV_FILTER_POLICY	Advertising filter policy. The set of devices that the advertising procedure uses for device filtering is called the White List. 0x0 - Allow scan request from any device, allow connect request from any device. 0x1 - Allow scan request from devices in white list only, allow connect request from any device. 0x2 - Allow scan request from any device, allow connect request from devices in white list only. 0x3 - Allow scan request from devices in white list only, allow connect request from devices in white list only. Default Value: 0
2 : 1	ADV_TYPE	The Advertising type is used to determine the packet type that is used for advertising when advertising is enabled. 0x0 - Connectable undirected advertising. (adv_ind) 0x1 - Connectable directed advertising (adv_direct_ind). 0x2 - Discoverable undirected advertising (adv_discover_ind) 0x3 - Non connectable undirected advertising (adv_nonconn_ind). Default Value: 0
0	TX_ADDR	Device own address type. 1 - Address type is random. 0 - Address type is public. Default Value: 0

## 1.1.5 BLE\_BLELL\_ADV\_INTERVAL\_TIMEOUT

Advertising interval register.

Address: 0x402E101C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADV_INTERVAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	ADV_INTERVAL [14:8]						
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 0	ADV_INTERVAL	<p>Range: 0x0020 to 0x4000 (For ADV_IND)</p> <p>0x00A0 to 0x4000 (For ADV_SCAN_IND and NONCONN_IND)</p> <p>Invalid for ADV_DIRECT_IND</p> <p>Time = N * 0.625 msec</p> <p>Time Range: 20 ms to 10.24 sec.</p> <p>For directed advertising, firmware programs the default value of 1.28 seconds.</p> <p>Default Value: 32</p>

## 1.1.6 BLE\_BLELL\_ADV\_INTR

Advertising interrupt status and Clear register

Address: 0x402E1020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ADV_TIMEOUT	SLV_CONNECTED	CONN_REQ_RX_INTR	SCAN_REQ_RX_INTR	SCAN_RSP_TX_INTR	ADV_TX_INTR	ADV_CLOSE_INTR	ADV_START_INTR

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							ADV_ON

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	ADV_ON	Advertiser procedure is ON in hardware. Indicates that advertiser procedure is ON in hardware. 1 - ON 0 - OFF Default Value: 0
7	ADV_TIMEOUT	If this bit is set it indicates that the directed advertising event has timed out after 1.28 seconds. Applicable in adv_direct_ind advertising. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
6	SLV_CONNECTED	If this bit is set it indicates that connection is created as slave. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
5	CONN_REQ_RX_INTR	If this bit is set it indicates connect request packet is received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

### 1.1.6 BLE\_BLELL\_ADV\_INTR (continued)

4	SCAN_REQ_RX_INTR	If this bit is set it indicates scan request packet received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
3	SCAN_RSP_TX_INTR	If this bit is set it indicates scan response packet transmitted in response to previous scan request packet received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
2	ADV_TX_INTR	If this bit is set it indicates ADV packet is transmitted. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
1	ADV_CLOSE_INTR	If this bit is set it indicates current advertising event is closed. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	ADV_STRT_INTR	If this bit is set it indicates a new advertising event started after interval expiry. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

## 1.1.7 BLE\_BLELL\_ADV\_NEXT\_INSTANT

Advertising next instant.

Address: 0x402E1024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ADV_NEXT_INSTANT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ADV_NEXT_INSTANT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_NEXT_INSTANT	Shows the next start of advertising event with reference to the internal reference clock. Default Value: 0



## 1.1.8 BLE\_BLELL\_SCAN\_INTERVAL

Scan Interval Register

Address: 0x402E1028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_INTERVAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCAN_INTERVAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_INTERVAL	<p>Scan interval register. Interval between two consecutive scanning events. Firmware sets the scanning interval value to this register before issuing start scan command.</p> <p>Range: 0x0004 to 0x4000</p> <p>Default: 0x0010 (10 ms)</p> <p>Time = N * 0.625 msec</p> <p>Time Range: 2.5 msec to 10.24 sec.</p> <p>Default Value: 16</p>

## 1.1.9 BLE\_BLELL\_SCAN\_WINDOW

Scan window Register

Address: 0x402E102C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_WINDOW [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCAN_WINDOW [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_WINDOW	<p>Duration of scan in a scanning event, which should be less than or equal to scan interval value. Firmware sets the scan window value to this register before issuing start scan command.</p> <p>Range: 0x0004 to 0x4000</p> <p>Default: 0x0010 (10 ms)</p> <p>Time = N * 0.625 msec</p> <p>Time Range: 2.5 msec to 10.24 sec.</p> <p>Default Value: 16</p>

## 1.1.10 BLE\_BLELL\_SCAN\_PARAM

Scanning parameters register

Address: 0x402E1030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW		RW		RW
HW Access	None		R	R		R		R
Name	None [7:6]		DUP_FILT_EN	SCAN_FILT_POLICY [4:3]		SCAN_TYPE [2:1]		TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DUP_FILT_EN	Filter duplicate packets. 1- Duplicate filtering enabled. 0- Duplicate filtering not enabled. This field is derived from the LE_set_scan_enable command. Default Value: 0
4 : 3	SCAN_FILT_POLICY	The scanner filter policy determines how the scanner processes advertising packets. 0x00 - Accept advertising packets from any device. 0x01 - Accept advertising packets from only devices in the whitelist. 0x10 - RFU 0x11 - RFU Adv_direct_ind packets which are not addressed to this device are ignored. Default Value: 0
2 : 1	SCAN_TYPE	0x00 - passive scanning.(default) 0x01 - active scanning. 0x10 - RFU 0x11 - RFU Default Value: 0

### 1.1.10 BLE\_BLELL\_SCAN\_PARAM (continued)

0	TX_ADDR	Devices own address type. 1 - addr type is random. 0 - addr type is public. Default Value: 0
---	---------	---

## 1.1.11 BLE\_BLELL\_SCAN\_INTR

Scan interrupt status and Clear register

Address: 0x402E1038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW	RW	RW	RW	RW
Name	None [7:5]			SCAN_RSP_RX_INTR	ADV_RX_INTR	SCAN_TX_INTR	SCAN_CLOSE_INTR	SCAN_STATUS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							SCAN_ON

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	SCAN_ON	Scan procedure status. 1 scan procedure is active. 0 scan procedure is not active. Default Value: 0
4	SCAN_RSP_RX_INTR	If this bit is set it indicates SCAN_RSP packet is received. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. Write to the register with this bit set to 1, clears the interrupt source. NOTE: This interrupt is generated while active scanning upon receiving scan response packet. Default Value: 0
3	ADV_RX_INTR	If this bit is set it indicates ADV packet received. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is generated while active/passive scanning upon receiving adv packets. Default Value: 0
2	SCAN_TX_INTR	If this bit is set it indicates scan request packet is transmitted. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

### 1.1.11 BLE\_BLELL\_SCAN\_INTR (continued)

1	SCAN_CLOSE_INTR	<p>If this bit is set it indicates scan window is closed.</p> <p>Write to the register with this bit set to 1, clears the interrupt source.</p> <p>Default Value: 0</p>
0	SCAN_STRT_INTR	<p>If this bit is set it indicates scan window is opened.</p> <p>Write to the register with this bit set to 1, clears the interrupt source.</p> <p>Default Value: 0</p>

## 1.1.12 BLE\_BLELL\_SCAN\_NEXT\_INSTANT

Advertising next instant.

Address: 0x402E103C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_SCAN_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_SCAN_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_SCAN_INSTANT	Shows the instant with respect to internal reference clock of resolution 625 us at which next scanning event begins. Default Value: 0



## 1.1.13 BLE\_BLELL\_INIT\_INTERVAL

Initiator Interval Register

Address: 0x402E1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_INTERVAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_INTERVAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_SCAN_INTERVAL	Initiator interval register. Firmware sets the initiators scanning interval value to this register before issuing create connection command. Interval between two consecutive scanning events. Range: 0x0004 to 0x4000 Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. Default Value: 0

## 1.1.14 BLE\_BLELL\_INIT\_WINDOW

Initiator window Register

Address: 0x402E1044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_WINDOW [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_WINDOW [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_SCAN_WINDOW	Duration of scan in a scanning event, which should be less than or equal to scan interval value. Firmware sets the scan window value to this register before issuing create connection command. Range: 0x0004 to 0x4000 Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. Default Value: 0

## 1.1.15 BLE\_BLELL\_INIT\_PARAM

Initiator parameters register

Address: 0x402E1048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	None	RW	RW
HW Access	None				R	None	R	R
Name	None [7:4]				INIT_FILT_POLICY	None	RX_ADDR_RX_TX_ADDR	TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	INIT_FILT_POLICY	The Initiator_Filter_Policy is used to determine whether the White List is used or not. 0 - White list is not used to determine which advertiser to connect to. Instead the Peer_Address_Type and Peer Address fields are used to specify the address type and address of the advertising device to connect to. 1 - White list is used to determine the advertising device to connect to. Peer_Address_Type and Peer_Address fields are ignored when whitelist is used. Default Value: 0
1	RX_ADDR_RX_TX_ADDR	Peer address type. The rx_addr field is updated by the receiver with the address type of the received connectable advertising packet. 1 - addr type is random. 0 - addr type is public. Default Value: 0
0	TX_ADDR	Device own address type. 1 - addr type is random. 0 - addr type is public. Default Value: 0

## 1.1.16 BLE\_BLELL\_INIT\_INTR

Scan interrupt status and Clear register

Address: 0x402E1050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW	None	RW	RW	RW
Name	None [7:5]			MASTER_CONN_CREATED	None	INIT_TX_START_INTR	INIT_CLOSE_WINDOW_INTR	INIT_INTERVAL_EXPIRE_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	MASTER_CONN_CREATED	If this bit is set it indicates connection is created as master. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
2	INIT_TX_START_INTR	If this bit is set it indicates initiator packet (CONREQ) transmission has started. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
1	INIT_CLOSE_WINDOW_INTR	If this bit is set it indicates initiator scan window has finished. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	INIT_INTERVAL_EXPIRE_INTR	If this bit is set it indicates initiator scan window has started. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

## 1.1.17 BLE\_BLELL\_INIT\_NEXT\_INSTANT

Initiator next instant.

Address: 0x402E1054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	INIT_NEXT_INSTANT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	INIT_NEXT_INSTANT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_NEXT_INSTANT	Shows the instant with respect to internal reference clock of resolution 625 us at which next initiator scanning event begins. Default Value: 0

## 1.1.18 BLE\_BLELL\_DEVICE RAND\_ADDR\_L

Lower 16 bit random address of the device.

Address: 0x402E1058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_L [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_L [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_L	Lower 16 bit of 48-bit random address of the device. Default Value: 0

## 1.1.19 BLE\_BLELL\_DEVICE\_RAND\_ADDR\_M

Middle 16 bit random address of the device.

Address: 0x402E105C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_M	Middle 16 bit of 48-bit random address of the device. Default Value: 0



## 1.1.20 BLE\_BLELL\_DEVICE\_RAND\_ADDR\_H

Higher 16 bit random address of the device.

Address: 0x402E1060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_H [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_H [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_H	Higher 16 bit of 48-bit random address of the device. Default Value: 0

## 1.1.21 BLE\_BLELL\_PEER\_ADDR\_L

Lower 16 bit address of the peer device.

Address: 0x402E1068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_L	Lower 16 bit of 48-bit address of the peer device. Default Value: 0

## 1.1.22 BLE\_BLELL\_PEER\_ADDR\_M

Middle 16 bit address of the peer device.

Address: 0x402E106C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_M	Middle 16 bit of 48-bit address of the peer device. Default Value: 0

## 1.1.23 BLE\_BLELL\_PEER\_ADDR\_H

Higher 16 bit address of the peer device.

Address: 0x402E1070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_H	<p>Higher 16 bit of 48-bit address of the peer device.</p> <p>The peer address registers are used for multiple purposes. The register is written by firmware to provide the peer address to be used for a hardware procedure. When firmware reads the register, it reads back peer address values updated by hardware.</p> <p>While doing directed Advertising, the firmware writes the peer address of the device specified by the Di-rect_Address parameter of the LE_Set_Advertising_Parameters command.</p> <p>While device is configured as an initiator without white list filtering, the peer address specified in the peer_address field of the create connection command is programmed into this register, which is used by hard-ware procedures.</p> <p>While device is configured as an initiator and white list is enabled, firmware can read this register to get the address of the peer device from which connectable ADV packet was received and to which the connection is created.</p> <p>When a connection is created as a slave, the firmware can read this register to get the address of the peer de-vice to which connection is created.</p> <p>Default Value: 0</p>

## 1.1.24 BLE\_BLELL\_WL\_ADDR\_TYPE

whitelist address type

Address: 0x402E1078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_ADDR_TYPE [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WL_ADDR_TYPE	8 address type bits corresponding to the device address stored. 1 - Address type is random. 0 - Address type is public. Default Value: 0

## 1.1.25 BLE\_BLELL\_WL\_ENABLE

whitelist valid entry bit

Address: 0x402E107C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_ENABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WL_ENABLE	Stores the valid entry bit corresponding to each of the eight device address stored in the whitelist. 1 - White list entry is Valid 0 - White list entry is Invalid Default Value: 0

## 1.1.26 BLE\_BLELL\_TRANSMIT\_WINDOW\_OFFSET

Transmit window offset

Address: 0x402E1080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TX_WINDOW_OFFSET	This is used to determine the first anchor point for the master transmission, from the time of connection creation. Range: This shall be a multiple of 1.25 ms in the range of 0 ms to connInterval value. Default Value: 0



## 1.1.27 BLE\_BLELL\_TRANSMIT\_WINDOW\_SIZE

Transmit window size

Address: 0x402E1084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_SIZE [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TX_WINDOW_SIZE	window_size along with the window_offset is used to calculate the first connection point anchor point for the master. This shall be a multiple of 1.25 ms in the range of 1.25 ms to the lesser of 10 ms and (connInterval 1.25 ms). Values range from 0 to 10 ms. Default Value: 0

## 1.1.28 BLE\_BLELL\_DATA\_CHANNELS\_L0

Data channel map 0 (lower word)

Address: 0x402E1088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_L0 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_L0 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_L0	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

## 1.1.29 BLE\_BLELL\_DATA\_CHANNELS\_M0

Data channel map 0 (middle word)

Address: 0x402E108C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M0 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M0 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_M0	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (32:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

## 1.1.30 BLE\_BLELL\_DATA\_CHANNELS\_H0

Data channel map 0 (upper word)

Address: 0x402E1090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_CHANNELS_H0 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_H0	<p>This register field indicates which of the data channels are in use. This stores the information for the upper 5 (36:32) data channel indices.</p> <p>1 indicates the corresponding data channel is used and 0 indicates the channel is unused.</p> <p>Note: The Data channel map 0 and data channel map 1 are two sets of channel maps stored, common for all the connections. At any given time, only two maps can be maintained and the connections will use one of the two sets as indicated by the channel map index field in the CE_CNFG_STS registers specific to the link. Firmware must also manage to update this field along with the map.</p> <p>Default Value: 0</p>

## 1.1.31 BLE\_BLELL\_DATA\_CHANNELS\_L1

Data channel map 1 (lower word)

Address: 0x402E1098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_L1 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_L1 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_L1	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

## 1.1.32 BLE\_BLELL\_DATA\_CHANNELS\_M1

Data channel map 1 (middle word)

Address: 0x402E109C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M1 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M1 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_M1	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (32:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

### 1.1.33 BLE\_BLELL\_DATA\_CHANNELS\_H1

Data channel map 1 (upper word)

Address: 0x402E10A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_CHANNELS_H1 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_H1	<p>This register field indicates which of the data channels are in use. This stores the information for the upper 5 data channel indices.</p> <p>1 indicates the corresponding data channel is used and 0 indicates the channel is unused.</p> <p>Note: The Data channel map 0 and data channel map 1 are two sets of channel maps stored, common for all the connections. At any given time, only two maps can be maintained and the connections will use one of the two sets as indicated by the channel map index field in the CE_CNFG_STS registers specific to the link. Firmware must also manage to update this field along with the map.</p> <p>Default Value: 0</p>

## 1.1.34 BLE\_BLELL\_CONN\_INTR

Connection interrupt status and Clear register

Address: 0x402E10A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	CON_UPDT_DONE	CE_RX	CE_TX_ACK	CLOSE_CE	START_CE	MAP_UPDT_DONE	CONN_ESTB	CONN_CLOSED

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R			R		
HW Access	RW	RW	RW			RW		
Name	PING_NEARLY_EXPIRED_INTR	PING_TIMER_EXPIRED_INTR	RX_PDU_STATUS [13:11]			DISCON_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PING_NEARLY_EXPIRED_INTR	If this is set, it indicates that ping timer has nearly expired. Default Value: 0
14	PING_TIMER_EXPIRED_INTR	If this is set, it indicates that ping timer has expired. Default Value: 0
13 : 11	RX_PDU_STATUS	Status of PDU received. This information is valid along with receive interrupt. xx1 Bad Packet (packet with CRC error) 000 empty PDU 010 - new data (non-empty) PDU 110 Duplicate Packet Default Value: 0



### 1.1.34 BLE\_BLELL\_CONN\_INTR (continued)

10 : 8	DISCON_STATUS	Reason for disconnect indicates the reason the link is disconnected by hardware. 001 - connection failed to be established 010 - supervision timeout 011 - kill connection by host 100 - kill connection after ACK transmitted 101 - PDU response timer expired Default Value: 0
7	CON_UPDT_DONE	This bit is set when the last connection event with previous connection parameters is reached. The bit is set immediately after the receive operation at the anchor point of the last connection event. If this bit is written with 1, it clears the connection updated interrupt. Default Value: 0
6	CE_RX	If this bit is set it indicates that a packet is received in the connection event. If this bit is written with 1, it clears the connection event received interrupt. Default Value: 0
5	CE_TX_ACK	If this bit is set it indicates that the connection event transmission acknowledgement is received for the previous non-empty packet transmitted. If this bit is written with 1, it clears the ce transmission acknowledgement interrupt. Default Value: 0
4	CLOSE_CE	If this bit is set it indicates that the connection event closed interrupt has happened. If this bit is written with 1, it clears the connection event closed interrupt. Default Value: 0
3	START_CE	If this bit is set it indicates that the connection event started interrupt has happened. If this bit is written with 1, it clears the connection event started interrupt. Default Value: 0
2	MAP_UPDT_DONE	If this bit is set it indicates that the channel map update is completed at the instant specified by the firmware. If this bit is written with 1, it clears the map update done interrupt. Default Value: 0
1	CONN_ESTB	If this bit is set it indicates that the connection has been established. The bit is also set when a connection update procedure is completed, at the start of the first anchor point with the updated parameters. If this bit is written with 1, it clears the connection established interrupt. Default Value: 0
0	CONN_CLOSED	If this bit is set it indicates that the link is disconnected. If this bit is written with 1, it clears the connection updated interrupt. Default Value: 0

## 1.1.35 BLE\_BLELL\_CONN\_STATUS

Connection channel status

Address: 0x402E10AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	RW				None			
Name	RECEIVE_PACKET_COUNT [15:12]				None [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	RECEIVE_PACKET_COUNT	<p>This field stores the count for the number of receive packets in the receive FIFO that are still not ready by firmware.</p> <p>The counter value is incremented by hardware for every good packet it stores in the FIFO. After firmware reads a packet, it decrements the counter by issuing the PACKET_RECEIVED command from the commander.</p> <p>Default Value: 0</p>

## 1.1.36 BLE\_BLELL\_CONN\_INDEX

Connection Index register

Address: 0x402E10B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_INDEX [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_INDEX [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_INDEX	This field is used to index the multiple connections existing. Range is 0 to maximum number of connections supported. For a single connection device, conn_index is 0. Default Value: 0

## 1.1.37 BLE\_BLELL\_WAKEUP\_CONFIG

Wakeup configuration

Address: 0x402E10B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OSC_STARTUP_DELAY [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW						None	
HW Access	R						None	
Name	DSM_OFFSET_TO_WAKEUP_INSTANT [15:10]						None [9:8]	
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 10	DSM_OFFSET_TO_WAKEUP_INSTANT	Number of slots before the wake up instant before which the hardware needs to exit from deep sleep mode. The slot is of 0.625ms period. This is a onetime configuration field, which is used every time hardware does an auto-wakeup before the next wakeup instant. Default Value: 0
7 : 0	OSC_STARTUP_DELAY	Oscillator stabilization/startup delay. This is in X.Y for-mat where X is in terms of number of BT slots (625 us) and Y is in terms of number of clock periods of 16KHz clock input, required for RF oscillator to stabilize the clock output to the controller on its output pin, after oscillator is turned ON. In this period the clock is as-sumed to be unstable, and so the controller does not turn on the clock to internal logic till this period is over. This means, the wake up from deep sleep mode must account for this delay before the wakeup instant. Osc_startup_delay[7:5] is number of slots(625us) Osc_startup_delay[4:0] is number of clock periods of 16KHz clock (Warning: Min. value of Osc_startup_delay [4:0] sup-ported is 1 and Max. value is 9. Therefore programmable range is 1 to 9) Default Value: 0

## 1.1.38 BLE\_BLELL\_WAKEUP\_CONTROL

Wakeup control

Address: 0x402E10C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_INSTANT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WAKEUP_INSTANT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WAKEUP_INSTANT	<p>Instant, with reference to the internal 16-bit clock reference, at which the hardware must wakeup from deep sleep mode. This is calculated by firmware based on the next closest instant where a controller operation is required (like advertiser/scanner). Firmware reads the next instant of the procedures in the corresponding *_NEXT_INSTANT registers. This value is used only when hardware auto wakeup from deep sleep mode is enabled in the clock control register.</p> <p>Note: it is recommended to program wakeup_instant such a way that the actual instant to wakeup shall be at least two counts (two slots of 625 us) ahead of reference clock when entering DSM. The actual instant to wakeup is wakeup_instant dsm_offset_to_wakeup_instant osc_startup_delay, and it shall be greater than reference clock + 2</p> <p>Default Value: 0</p>

## 1.1.39 BLE\_BLELL\_CLOCK\_CONFIG

Clock control

Address: 0x402E10C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	R	R	R	R	R	R	R
Name	LLH_IDLE	PHY_CLK_GATE_EN	SYSCLK_GATE_EN	CORECLK_GATE_EN	CONN_CLK_GATE_EN	INIT_CLK_GATE_EN	SCAN_CLK_GATE_EN	ADV_CLK_GATE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None	RW	None	RW	RW	RW
HW Access	R	R	None	R	None	R	R	R
Name	DEEP_SLEEP_MODE_EN	SLEEP_MODE_DE_EN	None	SM_INTR_EN	None	SM_AUTO_WKUP_EN	LPO_SEL_EXTERNAL	LPO_CLK_FREQ_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	DEEP_SLEEP_MODE_EN	Enable deep sleep mode. 1 enable, 0 disable. Enables hardware logic related to deep sleep mode to control the deep sleep mode operation. If disabled, the related logic is not executed and hardware cannot enter deep sleep mode. Default Value: 0
14	SLEEP_MODE_EN	Enable sleep mode. 1 enable, 0 disable. Enables hardware to control sleep mode operation. Default Value: 0
12	SM_INTR_EN	Enable SM exit interrupt. 1 enable, 0 disable. Enables hardware to generate an interrupt while exiting sleep mode irrespective of whether it is initiated by hardware or firmware. The interrupt is captured and stored till it gets cleared. Disabling this bit mask the sleep mode exit event from hardware & firmware. Default Value: 0

### 1.1.39 BLE\_BLELL\_CLOCK\_CONFIG (continued)

10	SM_AUTO_WKUP_EN	<p>Enable sleep mode auto wakeup enable. 1- enable, 0 disable.</p> <p>Enables hardware to automatically wakeup from sleep mode at the instant = wakeup_instant sm_offset_to_wakeup_instant. The wakeup_instant is the field in the wakeup control register described earlier. The sm_offset_to_wakeup_instant value is the field described in the wakeup configuration register.</p> <p>Default Value: 0</p>
9	LPO_SEL_EXTERNAL	<p>Select external sleep clock. 1 External clock, 0 - internal generated clock.</p> <p>The field is used to select either the low power clock input on sleep_clk input pin(of frequency 16.384KHz) directly to run the DSM logic or to use the internal generated reference clock(of 16KHz) for the same.</p> <p>Default Value: 0</p>
8	LPO_CLK_FREQ_SEL	<p>Clock frequency select. 0 32KHz, 1 32.768KHz.</p> <p>Base frequency of the sleep_clk input used for generating the internal reference clock of approximate 16KHz frequency.</p> <p>Default Value: 0</p>
7	LLH_IDLE	<p>Indicates if hardware is doing any transmit/receive operation. This information is used by firmware to decide to program the hardware into deep sleep mode.</p> <p>1 LL hardware is idle.</p> <p>0 LL hardware is busy. In this case LL hardware will not enter deep sleep mode, even if firmware gives an enter DSM command. (In this situation hardware generates dsm exit interrupt to inform firmware that DSM entry was not successful).</p> <p>Default Value: 1</p>
6	PHY_CLK_GATE_EN	<p>Digital PHY clock enable. 1- enable, 0-disable.</p> <p>Enable the Digital PHY to shutdown the clock. When 1, it indicates that controller has an upcoming activity so PHY clock must be turned ON. When 0, it indicates inactivity in the controller.</p> <p>Default Value: 0</p>
5	SYSClk_GATE_EN	<p>Sysclk gate enable. 1- enable, 0 disable.</p> <p>Enables clock gating of system clock input to the link layer. If 1, it enables the DSM logic to control the clock gate for system clock input from pin. If 0, the DSM logic has no control and the system clock is always ON.</p> <p>Default Value: 0</p>
4	CORECLK_GATE_EN	<p>Core clock gate enable. 1 enable, 0 disable.</p> <p>Enables gating of clock to the llh_core module in hardware. If 1, the sleep mode/deep sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock is always turned ON.</p> <p>Default Value: 0</p>
3	CONN_CLK_GATE_EN	<p>Connection block clock gate enable. 1 enable, 0 disable.</p> <p>Enables gating of clock to the connection module (llh_conncb_top) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the engine. If 0, the logic has no control and clock to the module is always turned ON.</p> <p>Default Value: 0</p>
2	INIT_CLK_GATE_EN	<p>Initiator block clock gate enable. 1 enable, 0 disable.</p> <p>Enables gating of clock to the initiator module (llh_init). If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON.</p> <p>Default Value: 0</p>
1	SCAN_CLK_GATE_EN	<p>Scan block clock gate enable. 1 enable, 0 disable.</p> <p>Enables gating of clock to the scanner module (llh_scan) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON.</p> <p>Default Value: 0</p>

### 1.1.39 BLE\_BLELL\_CLOCK\_CONFIG (continued)

0	ADV_CLK_GATE_EN	Advertiser block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the advertiser module (llh_adv) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0
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## 1.1.40 BLE\_BLELL\_TIM\_COUNTER\_L

Reference Clock

Address: 0x402E10C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TIM_REF_CLOCK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TIM_REF_CLOCK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TIM_REF_CLOCK	16-bit internal reference clock. The clock is a free run-ning clock, incremented by a 0.625ms pe-riodic pulse. It is used as a reference clock to derive all the timing required as per protocol. Default Value: 0

## 1.1.41 BLE\_BLELL\_POC\_REG\_\_TIM\_CONTROL

BLE Time Control

Address: 0x402E10D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	BB_CLK_FREQ_MINUS_1 [7:3]					None [2:0]		
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 3	BB_CLK_FREQ_MINUS_1	LLH clock configuration. The clock frequency of the clock input to this design is configured in this register. This is used to derive a 1MHz clock. Default Value: 0

## 1.1.42 BLE\_BLELL\_ADV\_TX\_DATA\_FIFO

Advertising data transmit FIFO. Access ADVCH\_TX\_FIFO.

Address: 0x402E10E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ADV_TX_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ADV_TX_DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_TX_DATA	IO mapped FIFO of depth 16 (2 byte wide), to store ADV data of maximum length 31 bytes for transmitting. Firmware writes consecutive words by writing to the same address location. Note: ADV_TX_DATA_FIFO and ADV_SCN_RSP_TX_FIFO shares same physical FIFO of depth 32. 16 locations for each FIFO are allocated. Default Value: 0

## 1.1.43 BLE\_BLELL\_ADV\_SCN\_RSP\_TX\_FIFO

Advertising scan response data transmit FIFO. Access ADVCH\_TX\_FIFO.

Address: 0x402E10E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	SCAN_RSP_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	SCAN_RSP_DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_RSP_DATA	IO mapped FIFO of depth 16 (2 byte wide), to store scan response data of maximum length 31 bytes for transmitting. Firmware writes consecutive words by writing to the same location. Note: ADV_TX_DATA_FIFO and ADV_SCN_RSP_TX_FIFO shares same physical FIFO of depth 32. 16 locations for each FIFO are allocated. Default Value: 0

## 1.1.44 BLE\_BLELL\_INIT\_SCN\_ADV\_RX\_FIFO

advertising scan response data receive data FIFO. Access ADVRX\_FIFO.

Address: 0x402E10F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ADV_SCAN_RSP_RX_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ADV_SCAN_RSP_RX_DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_SCAN_RSP_RX_DATA	IO mapped FIFO of depth 64, to store ADV and SCAN_RSP header and payload received by the scanner. The RSSI value at the time of reception of this packet is also stored. Firmware reads from the same address to read out consecutive words of data. Note: The 16 bit header is first loaded to the advertise channel data receive FIFO followed by the payload data and then 16 bit RSSI. Default Value: 0

## 1.1.45 BLE\_BLELL\_CONN\_INTERVAL

Connection Interval

Address: 0x402E1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNECTION_INTERVAL	The value configured in this register determines the spacing between the connection events. This shall be a multiple of 1.25 ms in the range of 7.5 ms to 4.0 s.
	L	Default Value: 0

## 1.1.46 BLE\_BLELL\_SUP\_TIMEOUT

Supervision timeout

Address: 0x402E1104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SUPERVISION_TIMEOUT	This field defines the maximum time between two received Data packet PDUs before the connection is considered lost. This shall be a multiple of 10 ms in the range of 100 ms to 32.0 s and it shall be larger than (1+connSlaveLatency)*connInterval. Default Value: 0

## 1.1.47 BLE\_BLELL\_SLAVE\_LATENCY

Slave Latency

Address: 0x402E1108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SLAVE_LATENCY	<p>The value configured in this field defines the number of consecutive connection events that the slave device is not required to listen for master.</p> <p>The value of connSlaveLatency should not cause a Supervision Timeout.</p> <p>This shall be an integer in the range of 0 to ((connSupervision Timeout/connInterval)-1).</p> <p>connSlaveLatency shall also be less than 500.</p> <p>Default Value: 0</p>



## 1.1.48 BLE\_BLELL\_CE\_LENGTH

Connection event length

Address: 0x402E110C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONNECTION_EVENT_LENGTH [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONNECTION_EVENT_LENGTH [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
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## 1.1.48 BLE\_BLELL\_CE\_LENGTH (continued)

15 : 0	CONNECTION_EVENT_LENGTH	<p>This field defines the length of Connection event. This value is derived from the CE length HCI parameters received from the host. This determines the number of master transmit slots in a connection event, subject to either of the MD bits being set. If both MD bits are set to 0, this has no effect. Units: 625us</p> <p>Note:</p> <p>The connection event length as specified by the CE_LENGTH shall not exceed CONN_INTERVAL 1.25 ms.</p> <p>The CE-length parameter, according to the Bluetooth specification, is the length of the connection event.</p> <p>Take an example to illustrate this scenario:</p> <p>Assume a connection with interval = 100ms. that the application has put allowed 20ms of CE-length.</p> <p>Here, the CE-length can be upto 100ms (100ms - 150us to be exact).</p> <p>If the connection is maintained for 5 minutes, there could be <math>10 \times 60 \times 5 = 3000</math> connection-intervals.</p> <p>The CE-length need not be maintained constant during all the 3000 connection events.</p> <p>Here are the typical cases that determine the value of CE-length:</p> <p>(1) No data packets exchanged. we are just maintaining time and frequency synchronization. In this case, only a packet pair will be exchanged every connection interval. Here, CE-length = 1.</p> <p>(2) Average of 10 packets to be sent per connection event.</p> <p>We can pump data in multiple ways here:</p> <p>2.1: Send data at uniform rate : In this case, the CE-length will be enough to accommodate 10 packets, which will take about 7ms. As this is less than application enforced limit of 20ms, we can comfortably push all the 10 data packets in this connection interval. So data will be pumped to the other BT device at the same rate as is received from my application.</p> <p>2.2: Can send data in bursts. Assume that we accumulate data for 1 second and pump out at the end of 1 second (this is not done by our Bluetooth stack, the application needs to buffer the data). So, at 10th connection interval, we have 100 packets accumulated. We are now ready to pump this data. 100 packets take about 70 ms. This is above the application enforced 20ms. So, the hardware can pump data that can fill up 20ms. The remaining data will be deferred to the next connection interval.</p> <p>So, in this case, you would see a CE-length spread over time like this (Per connection interval): 0,0,0,0,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, and so on.</p> <p>(3) We are receiving data at the same rate as in (2). This case is to honor data sent by the other BT-device by giving it more time in the current connection interval.</p> <p>In (2) and (3) you will see non-empty packets either transmitted or received. We can also utilize the CE-length for different reasons:</p> <p>(4) A transaction is in progress, and we are expecting a response packet very soon. In this case, we may be exchanging only empty packets now, and in the next few packet-pairs.</p> <p>In this case, you will the CE-length to be large, and a non-empty packet may not be exchanged in all the slots.</p> <p>In slave mode, the connection event length (unit of 625us) will close the connection event at programmed time irrespective of MD bit received from the master or the MD bit sent from slave.</p> <p>Default Value: 0</p>
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## 1.1.49 BLE\_BLELL\_PDU\_ACCESS\_ADDR\_L\_REGISTER

Access address (lower)

Address: 0x402E1110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_LOWER_BITS [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_LOWER_BITS [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_ACCESS_ADDRES S_LOWER_BITS	This field defines the lower 16 bits of the access address for each Link layer connection between any two devices. Default Value: 0

## 1.1.50 BLE\_BLELL\_PDU\_ACCESS\_ADDR\_H\_REGISTER

Access address (upper)

Address: 0x402E1114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_HIGHER_BITS [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_HIGHER_BITS [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_ACCESS_ADDRES S_HIGHER_BITS	This field defines the higher 16 bits of the access address for each Link layer connection between any two devices. Default Value: 0

## 1.1.51 BLE\_BLELL\_CONN\_CE\_INSTANT

Connection event instant

Address: 0x402E1118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CE_INSTANT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CE_INSTANT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CE_INSTANT	This is the value of the free running Connection Event counter when the new parameters of connection update and/or Channel map update will be effective. Range : 0x0000 to 0xFFFF Default Value: 0

## 1.1.52 BLE\_BLELL\_CE\_CNFG\_STS\_REGISTER

connection configuration & status register

Address: 0x402E111C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW			
HW Access	RW	R	R	R	R			
Name	MAP_INDEX_CURR_INDEX	MD	MAS_SLV	DATA_LIST_HEAD_UP	DATA_LIST_INDEX_LAST_ACK_INDEX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				None	R	None	RW
HW Access	RW				None	RW	None	R
Name	CURRENT_PDU_INDEX [15:12]				None	CONN_ACTIVE	None	PAUSE_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	CURRENT_PDU_INDEX	The index of the transmit packet buffer that is currently in transmission/waiting for transmission. Default Value: 0
10	CONN_ACTIVE	This bit is 1 whenever the connection is active. Default Value: 0
8	PAUSE_DATA	Pause data. 1 - pause data, 0 - do not pause. Pause the data transfer on the connection. The current_pdu_index in hardware does not move to next in-dex until pause_data is cleared. Default Value: 0
7	MAP_INDEX_CURR_INDEX	Written by firmware to select the map index to be used by hardware for this connection. 1 - use channel map register set 1. 0 - use channel map register set 0. When firmware reads this field, it returns the current map index being used in hardware. Default Value: 0

### 1.1.52 BLE\_BLELL\_CE\_CNFG\_STS\_REGISTER (continued)

6	MD	MD bit set to 1 indicates device has more data to be sent. Default Value: 0
5	MAS_SLV	mas_slv bit set to 1 indicates that device is configured as a master or a slave. 1 - master, 0 - slave. Default Value: 0
4	DATA_LIST_HEAD_UP	Update the first packet buffer index ready for transmission to start/resume data transfer after a pause. The bit must be toggled every time the firmware needs to indicate the start/resume. This requires a read modify write operation. Default Value: 0
3 : 0	DATA_LIST_INDEX_LAST_ACK_INDEX	Data list index for start/resume. This field must be valid along with data_list_head_up and indicate the transmit packet buffer index at which the data is loaded. The default number of buffers in the IP is 5, but may be customized for a customer. The buffers are indexed 0 to 4. Hardware will start the next data transmission from the index indicated by this field. Default Value: 0

## 1.1.53 BLE\_BLELL\_NEXT\_CE\_INSTANT

Next connection event instant

Address: 0x402E1120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_CE_INSTANT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_CE_INSTANT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_CE_INSTANT	16-bit internal reference clock value at which the next connection event will occur on a connection. The connection index register must be programmed with index of the connection, before reading the register. Default Value: 0



## 1.1.54 BLE\_BLELL\_CONN\_CE\_COUNTER

connection event counter

Address: 0x402E1124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONNECTION_EVENT_COUNTER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONNECTION_EVENT_COUNTER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNECTION_EVENT_COUNTER	This is the free running counter, connEventCounter as defined by Bluetooth spec. Firmware will read the instantaneous Event counter from this register, during connection update and channel map update procedure. Firmware will use this value to calculate the instant from which the new parameters (for connection update and channel map update) will be effective. Default Value: 0

## 1.1.55 BLE\_BLELL\_DATA\_LIST\_SENT\_UPDATE\_\_STATUS

data list sent update and status

Address: 0x402E1128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None		R	RW			
HW Access	RW	None		RW	RW			
Name	SET_CLEAR	None [6:5]		TX_SENT_4	LIST_INDEX_TX_SENT_3_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR	<p>Write: Used to set the SENT bit in hardware for the selected packet buffer.</p> <p>1 packet queued</p> <p>When firmware has a packet to send, firmware first loads the next available packet buffer. Then the hardware SENT bit is set by writing 1 to this bit field along with the list_index field that identified the buffer index. This indicates that a packet has been queued in the data buffer for sending. This packet is now ready to be transmitted.</p> <p>The SENT bit in hardware is cleared by hardware only when it has received an acknowledgement from the remote device.</p> <p>Firmware typically does not clear the bit. However, It only clears the bit on its own if it needs to flush a packet from the buffer, without waiting to receive acknowledgement from the remote device, firmware clears BIT7 along with the list_index specified.</p> <p>Default Value: 0</p>

## 1.1.55 BLE\_BLELL\_DATA\_LIST\_SENT\_UPDATE\_\_STATUS (continued)

4	TX_SENT_4	<p>Read: Reads TX_SENT[4].</p> <p>The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer.</p> <p>The bit values are</p> <p>1 queued</p> <p>0 no packet / packet ack received by hardware</p> <p>Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving acknowledgement.</p> <p>NOTE:</p> <p>The SENT status bit and ACK status bit have to be taken together to understand the meaning of packet status. The table below describes how the two bits are sequentially updated by either hardware/firmware to complete one data transmission.</p> <table border="1"> <thead> <tr> <th>SENT</th> <th>ACK</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Buffer is empty. No packet is queued in the buffer</td> </tr> <tr> <td>1</td> <td>0</td> <td>Packet is queued by firmware.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Packet is transmitted by hardware. Hardware is waiting for acknowledgement.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Hardware has received ACK. Firmware has not yet processed the ACK.</td> </tr> <tr> <td>0</td> <td>0</td> <td>Firmware has processed the ack. The buffer is again empty.</td> </tr> </tbody> </table> <p>Default Value: 0</p>	SENT	ACK	Description	0	0	Buffer is empty. No packet is queued in the buffer	1	0	Packet is queued by firmware.	1	1	Packet is transmitted by hardware. Hardware is waiting for acknowledgement.	0	1	Hardware has received ACK. Firmware has not yet processed the ACK.	0	0	Firmware has processed the ack. The buffer is again empty.
SENT	ACK	Description																		
0	0	Buffer is empty. No packet is queued in the buffer																		
1	0	Packet is queued by firmware.																		
1	1	Packet is transmitted by hardware. Hardware is waiting for acknowledgement.																		
0	1	Hardware has received ACK. Firmware has not yet processed the ACK.																		
0	0	Firmware has processed the ack. The buffer is again empty.																		
3 : 0	LIST_INDEX__TX_SENT_3_0	<p>Write:Indicates the buffer index for which the SENT bit is being updated by firmware.</p> <p>The default number of buffers in the IP is 5. The index range is 0-4.</p> <p>Read: Reads TX_SENT[3:0].</p> <p>The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer.</p> <p>The bit values are</p> <p>1 queued</p> <p>0 no packet / packet ack received by hardware</p> <p>Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving acknowledgement.</p> <p>Default Value: 0</p>																		

## 1.1.56 BLE\_BLELL\_DATA\_LIST\_ACK\_UPDATE\_\_STATUS

data list ack update and status

Address: 0x402E112C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None		R	RW			
HW Access	RW	None		RW	RW			
Name	SET_CLEAR	None [6:5]		TX_ACK_4	LIST_INDEX__TX_ACK_3_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR	<p>Write: Firmware uses the field to clear and ACK bit in the hardware to indicate that the acknowledgement for the transmit packet has been received and processed by firmware.</p> <p>Firmware clears the ACK bit in the hardware by writing in this register only after the acknowledgement is processed successfully by firmware.</p> <p>For clearing ack for a packet transmitted in fifo-index : 3, firm-ware will write 3 in the list-index field and set this bit (BIT7) to 0.</p> <p>This is the indication that the corresponding packet buffer identified by List-Index is cleared of previous transmission and can be re-used for another packet from now on.</p> <p>The ACK bit in hardware is set by hardware when it has successfully transmitted a packet.</p> <p>Default Value: 0</p>

## 1.1.56 BLE\_BLELL\_DATA\_LIST\_ACK\_UPDATE\_\_STATUS (continued)

4	TX_ACK_4	<p>Reads TX_ACK[4]</p> <p>If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement.</p> <p>Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware.</p> <p>Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware.</p> <p>NOTE:</p> <p>The SENT status bit and ACK status bit have to be taken together to understand the meaning of packet status. The table below describes how the two bits are sequentially updated by either hardware/firmware to complete one data transmission.</p> <table> <thead> <tr> <th>SENT</th> <th>ACK</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Buffer is empty. No packet is queued in the buffer</td> </tr> <tr> <td>1</td> <td>0</td> <td>Packet is queued by firmware.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Packet is transmitted by hardware. Hardware is waiting for acknowledgement.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Hardware has received ACK. Firmware has not yet processed the ACK.</td> </tr> <tr> <td>0</td> <td>0</td> <td>Firmware has processed the ack. The buffer is again empty.</td> </tr> </tbody> </table> <p>Default Value: 0</p>	SENT	ACK	Description	0	0	Buffer is empty. No packet is queued in the buffer	1	0	Packet is queued by firmware.	1	1	Packet is transmitted by hardware. Hardware is waiting for acknowledgement.	0	1	Hardware has received ACK. Firmware has not yet processed the ACK.	0	0	Firmware has processed the ack. The buffer is again empty.
SENT	ACK	Description																		
0	0	Buffer is empty. No packet is queued in the buffer																		
1	0	Packet is queued by firmware.																		
1	1	Packet is transmitted by hardware. Hardware is waiting for acknowledgement.																		
0	1	Hardware has received ACK. Firmware has not yet processed the ACK.																		
0	0	Firmware has processed the ack. The buffer is again empty.																		
3 : 0	LIST_INDEX__TX_ACK_3_0	<p>Write: Indicates the buffer index for which the ACK bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-4.</p> <p>Read: Reads TX_ACK[3:0]</p> <p>If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement.</p> <p>Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware.</p> <p>Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware.</p> <p>Default Value: 0</p>																		

## 1.1.57 BLE\_BLELL\_DATA\_MEM\_DESCRIPTOR0

Data buffer descriptor 0 to 4

Address: 0x402E1140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

## 1.1.58 BLE\_BLELL\_DATA\_MEM\_DESCRIPTOR1

Data buffer descriptor 0 to 4

Address: 0x402E1144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

## 1.1.59 BLE\_BLELL\_DATA\_MEM\_DESCRIPTOR2

Data buffer descriptor 0 to 4

Address: 0x402E1148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0



## 1.1.60 BLE\_BLELL\_DATA\_MEM\_DESCRIPTOR3

Data buffer descriptor 0 to 4

Address: 0x402E114C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

## 1.1.61 BLE\_BLELL\_DATA\_MEM\_DESCRIPTOR4

Data buffer descriptor 0 to 4

Address: 0x402E1150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

## 1.1.62 BLE\_BLELL\_WINDOW\_WIDEN\_INTVL

Window widen for interval

Address: 0x402E1160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WINDOW_WIDEN_INTVL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WINDOW_WIDEN_INTVL [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	WINDOW_WIDEN_INTVL	<p>This value defines the increased listening time for the slave.</p> <p>The window widening shall be smaller than <math>((\text{connInterval}/2) - T_{IFS})</math> us</p> <p>This value is calculated by firmware based on the drift, the connection interval value. The value is the unit widening value for one connection interval duration. In case of slave latency, this value is accumulated till the next anchor point at which the slave will listen.</p> <p>Default Value: 10</p>

## 1.1.63 BLE\_BLELL\_WINDOW\_WIDEN\_WINOFF

Window widen for offset

Address: 0x402E1164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WINDOW_WIDEN_WINOFF [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WINDOW_WIDEN_WINOFF [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	WINDOW_WIDEN_WINOFF	This field stores the additional number of microseconds the slave must extend its listening window to listen for a master packet. This value is calculated based on the window offset value. This is used at connection setup directly. During connection setup, this value is added with window_widen_intvl register value to calculate the win-dow widening size. Default Value: 10

## 1.1.64 BLE\_BLELL\_LE\_RF\_TEST\_MODE

Direct Test Mode control

Address: 0x402E1170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	RW	R					
Name	PKT_PAYL OAD	TEST_TYP E	TEST_FREQUENCY [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW						RW	
HW Access	R						R	
Name	TEST_LENGTH [15:10]						PKT_PAYLOAD [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 10	TEST_LENGTH	0x00-0x25 Length in bytes of payload data in each packet 0x26-0xFF Reserved for future use Default Value: 0
9 : 7	PKT_PAYLOAD	Payload type as per the HCI parameter. 0x00 Pseudo-Random bit sequence 9 0x01 Pattern of alter-nating bits 11110000 0x02 Pattern of alternating bits 10101010 0x03 Pseudo-Random bit sequence 15 0x04 Pat-tern of All 1 bits 0x05 Pattern of All 0 bits 0x06 Pattern of alternating bits 00001111 0x07 Pattern of alternating bits 0101 0x08-0xFF Reserved for future use Default Value: 0
6	TEST_TYPE	1 - DTM test ON 0 - DTM test OFF Default Value: 0

## 1.1.64 BLE\_BLELL\_LE\_RF\_TEST\_MODE (continued)

5 : 0	TEST_FREQUENCY	$N = (F - 2402) / 2$ Range: 0x00 0x27. Frequency Range : 2402 MHz to 2480 MHz Default Value: 0
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## 1.1.65 BLE\_BLELL\_DTM\_RX\_PKT\_COUNT

Direct Test Mode receive packet count

Address: 0x402E1174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RX_PACKET_COUNT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RX_PACKET_COUNT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RX_PACKET_COUNT	Number of packets received in receive test mode. Default Value: 0

## 1.1.66 BLE\_BLELL\_TXRX\_HOP

Channel Address register

Address: 0x402E1188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	HOP_CH_TX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	RW						
Name	None	HOP_CH_RX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	HOP_CH_RX	Receive channel index. Channel index on which previous packet is received. Default Value: 0
6 : 0	HOP_CH_TX	Transmit channel index. Channel index on which previous packet is transmitted. Default Value: 0



## 1.1.67 BLE\_BLELL\_TX\_RX\_ON\_DELAY

Transmit/Receive data delay

Address: 0x402E1190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RXON_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TXON_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	TXON_DELAY	Transmit delay Delay from start of transmit to transmission of first bit on air. It is used to control the T_IFS. The delay is in resolution of 1 microsecond. Default Value: 0
7 : 0	RXON_DELAY	Receive delay Delay from start of receive to expected first bit of receive packet at the controller. Used to control the turn on time of radio to optimize on power. The delay is in resolution of 1 microsecond. Default Value: 0

## 1.1.68 BLE\_BLELL\_DEV\_PUB\_ADDR\_L

Device public address lower register

Address: 0x402E11C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_L [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_L [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_L	Lower 16 bit of 48-bit public address of the device. Default Value: 13330

## 1.1.69 BLE\_BLELL\_DEV\_PUB\_ADDR\_M

Device public address middle register

Address: 0x402E11C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_M [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_M [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_M	Middle 16 bit of 48-bit public address of the device. Default Value: 86

## 1.1.70 BLE\_BLELL\_DEV\_PUB\_ADDR\_H

Device public address higher register

Address: 0x402E11C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_H [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_H [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_H	Higher 16 bit of 48-bit public address of the device. Default Value: 0

## 1.1.71 BLE\_BLELL\_ADV\_CH\_TX\_POWER

Advertising channel transmit power

Address: 0x402E11CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADV_TRANSMIT_POWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADV_TRANSMIT_POWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_TRANSMIT_POWER	Size: 1 Octet (signed integer) Range: -20 = N = 10 Units: dBm Accuracy: +/- 4 dBm in general. In implementation this is a radio specific value. Default Value: 34639

## 1.1.72 BLE\_BLELL\_OFFSET\_TO\_FIRST\_INSTANT

Offset to first instant

Address: 0x402E11D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFFSET_TO_FIRST_EVENT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	OFFSET_TO_FIRST_EVENT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	OFFSET_TO_FIRST_EVENT	The offset w.r.t the internal reference clock at which instant the first event occurs. This register will give flexibility to the firmware to position the connection at a desired point with respect to the internal free running clock. It is optional to be updated by firmware. This is not updated in the current firmware. Default Value: 6

## 1.1.73 BLE\_BLELL\_ADV\_CONFIG

Advertiser configuration register

Address: 0x402E11D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	ADV_TIME OUT_EN	SLV_CONN ECTED_EN	ADV_CON N_REQ_RX _EN	ADV_SCN_ REQ_RX_E N	SCN_RSP_ TX_EN	ADV_TX_E N	ADV_CLS_ EN	ADV_STRT _EN

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW					None		RW
HW Access	R					None		R
Name	ADV_PKT_INTERVAL [15:11]					None [10:9]		ADV_RAND _DISABLE

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 11	ADV_PKT_INTERVAL	Time between the beginning of two consecutive advertising PDUs. Time = N * 0.625 msec Time Range: <=10msec. Default Value: 4
8	ADV_RAND_DISABLE	Disable randomization of adv interval. When disabled, interval is same as programmed in adv_interval register. Default Value: 0
7	ADV_TIMEOUT_EN	Enable adv_timeout interrupt. Applicable in adv_direct_ind advertising. Default Value: 1
6	SLV_CONNECTED_EN	Enable slave connected interrupt. Default Value: 1
5	ADV_CONN_REQ_RX_EN	Enable connect request packet received interrupt. Default Value: 1

### 1.1.73 BLE\_BLELL\_ADV\_CONFIG (continued)

4	ADV_SCN_REQ_RX_EN	Enable scan request packet received interrupt. Default Value: 1
3	SCN_RSP_TX_EN	Enable scan response packet transmitted interrupt. Default Value: 1
2	ADV_TX_EN	Enable adv packet transmitted interrupt. Default Value: 1
1	ADV_CLS_EN	Enable advertising event stop interrupt. Default Value: 1
0	ADV_STRT_EN	Enable advertising event start interrupt. Default Value: 1



## 1.1.74 BLE\_BLELL\_SCAN\_CONFIG

Scan configuration register

Address: 0x402E11D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			SCN_RSP_RX_EN	ADV_RX_EN	SCN_TX_EN	SCN_CLOSE_EN	SCN_START_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW			None	RW	None		
HW Access	R			None	R	None		
Name	SCAN_CHANNEL_MAP [15:13]			None	BACKOFF_ENABLE	None [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	SCAN_CHANNEL_MAP	Advertising channels that are enabled for scanning operation. Bit 15: setting 1 - enables channel 39 for use. Bit 14: setting 1 - enables channel 38 for use. Bit 13: setting 1 - enables channel 37 for use. Default Value: 7
11	BACKOFF_ENABLE	Enable random backoff feature in scanner. 1 - enable 0 - disable Default Value: 0
4	SCN_RSP_RX_EN	Enable scan_rsp packet received interrupt . Default Value: 1
3	ADV_RX_EN	Enable adv packet received interrupt . Default Value: 1
2	SCN_TX_EN	Enable scan request packet transmitted interrupt. Default Value: 1

**1.1.74 BLE\_BLELL\_SCAN\_CONFIG** (continued)

1	SCN_CLOSE_EN	Enable scan event close interrupt. Default Value: 1
0	SCN_STRT_EN	Enable scan event start interrupt. Default Value: 1

## 1.1.75 BLE\_BLELL\_INIT\_CONFIG

Initiator configuration register

Address: 0x402E11DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			CONN_CREATED	None	CONN_REQ_TX_EN	INIT_CLOSE_EN	INIT_START_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW			None				
HW Access	R			None				
Name	INIT_CHANNEL_MAP [15:13]			None [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	INIT_CHANNEL_MAP	Advertising channels that are enabled for initiator scanning operation. Bit 15: setting 1 - enables channel 39 for use. Bit 14: setting 1 - enables channel 38 for use. Bit 13: setting 1 - enables channel 37 for use. Default Value: 0
4	CONN_CREATED	Enable master connection created interrupt Default Value: 0
2	CONN_REQ_TX_EN	Enables connection request packet transmission start interrupt. Default Value: 0
1	INIT_CLOSE_EN	Enable Initiator event close interrupt. Default Value: 0
0	INIT_START_EN	Enable Initiator event start interrupt. Default Value: 0

## 1.1.76 BLE\_BLELL\_CONN\_CONFIG

Connection configuration register

Address: 0x402E11E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	RX_INTR_THRESHOLD [7:4]				RX_PKT_LIMIT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None		RW
HW Access	R	R	R	R	R	None		R
Name	CONN_REQ_1SLOT_EARLY	MASK_SUTO_AT_UPDT	EXTEND_CU_TX_WIN	SLV_MD_CONFIG	DSM_SLOT_VARIANCE	None [10:9]		MD_BIT_CLEAR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CONN_REQ_1SLOT_EARLY	This bit is used to enable extension of the Conn Request to arbiter to 1 slot early. When enabled the request length is 2 slots. 1 - Enable 0 - Disable Default Value: 1
14	MASK_SUTO_AT_UPDT	This bit is used to enable/disable masking of internal hardware supervision timeout trigger when switching from old connection parameters to new parameters. 1 - Enable 0 - Disable Default Value: 1
13	EXTEND_CU_TX_WIN	This bit is used to enable/disable extending the additional rx window on slave side during connection update in event of packet miss at the update instant. 1 - Enable 0 - Disable Default Value: 1

## 1.1.76 BLE\_BLELL\_CONN\_CONFIG (continued)

12	SLV_MD_CONFIG	<p>This bit is set to configure the MD bit control when IUT is in slave role.</p> <p>1 - MD bit will be decided on packet pending status</p> <p>0 - MD bit will be decided on packet queued in next buffer status</p> <p>This bit has effect only when CONN_CONFIG.md_bit_ctr bit is not set .</p> <p>Default Value: 0</p>
11	DSM_SLOT_VARIANCE	<p>This bit configures the DSM slot counting mode.</p> <p>0 - The DSM slot count variance with respect to actual time is less than 1 slot</p> <p>1 - The DSM slot count variance with respect to actual time is more than 1 slot that 2 slots</p> <p>Default Value: 0</p>
8	MD_BIT_CLEAR	<p>This register field indicates whether the MD (More Data) bit needs to be controlled by software or, hardware and soft-ware logic combined.</p> <p>1 - MD bit is exclusively controlled by software, ie based on status of CE_CNFG_STS_REGISTER[6] - md bit.</p> <p>0 - MD Bit in the transmitted pdu is controlled by software and hardware logic. MD bit is set in transmitted packet, only if the software has set the md bit in CE_CNFG_STS_REGISTER[6] and either of the following conditions is true,</p> <p>a) If there are packets queued for transmission.</p> <p>b) If there is an acknowledgement awaited from the remote side for the packet transmitted.</p> <p>Default Value: 1</p>
7 : 4	RX_INTR_THRESHOLD	<p>This register field allows setting a threshold for the packet received interrupt to the firmware. For example if the value programmed is 0x2 then HW will generate interrupt only on receiving the second packet.</p> <p>In any case if the received number of packets in a conn event is less than the threshold or there are still packets (less than threshold) pending in the Rx FIFO, HW will generate the interrupt at the ce_close.</p> <p>Min value possible is 1. Max value depends on the Rx FIFO capacity.</p> <p>Default Value: 1</p>
3 : 0	RX_PKT_LIMIT	<p>Defines a limit for the number of Rx packets that can be re-ceived by the LLH. Default maximum value is 0xF. Minimum value shall be 1 or no packet will be stored in the Rx FIFO.</p> <p>Default Value: 15</p>

## 1.1.77 BLE\_BLELL\_CONN\_CH\_TX\_POWER

Connection channel transmit power

Address: 0x402E11E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONNCH_TRANSMIT_POWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONNCH_TRANSMIT_POWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNCH_TRANSMIT_POWER	Transmit power to be used for all packets transmitted on the connection channel. Default Value: 0

## 1.1.78 BLE\_BLELL\_CONN\_PARAM1

Connection parameter 1

Address: 0x402E11E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW		
HW Access	RW					RW		
Name	HOP_INCREMENT_PARAM [7:3]					SCA_PARAM [2:0]		

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_L [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CRC_INIT_L	This field defines the lower byte (7:0) of the CRC initialization vector. Default Value: 0
7 : 3	HOP_INCREMENT_PARAM	Hop increment for connection channel. Default Value: 0
2 : 0	SCA_PARAM	Sleep Clock Accuracy Default Value: 0

## 1.1.79 BLE\_BLELL\_CONN\_PARAM2

Connection parameter 2

Address: 0x402E11EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_H [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_H [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CRC_INIT_H	This field defines the upper two bytes (23:8) of the CRC initialization vector. Default Value: 0



## 1.1.80 BLE\_BLELL\_CONN\_INTR\_MASK

Connection Interrupt mask

Address: 0x402E11F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CONN_UPDATE_INTR_EN	CE_RX_INT_EN	CE_TX_ACK_INT_EN	CLOSE_CE_INT_EN	START_CE_INT_EN	MAP_UPDT_INT_EN	CONN_ESTB_INT_EN	CONN_CLOSE_INT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None				RW	RW
HW Access	R	R	None				R	R
Name	PING_NEARLY_EXPIRED_INTR	PING_TIMER_EXPIRED_INTR	None [13:10]				RX_BAD_PDU_INT_EN	RX_GOOD_PDU_INT_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PING_NEARLY_EXPIRED_INTR	If this bit is set ping timer nearly expired interrupt is enabled. Default Value: 0
14	PING_TIMER_EXPIRED_INTR	If this bit is set ping timer expired interrupt is enabled. Default Value: 0
9	RX_BAD_PDU_INT_EN	If this bit is set packet receive bad pdu interrupt is enabled. Effective only when bit 6 is set. Default Value: 0
8	RX_GOOD_PDU_INT_EN	If this bit is set packet receive good pdu interrupt is enabled. Effective only when bit 6 is set. Default Value: 0
7	CONN_UPDATE_INTR_EN	If this bit is set connection update interrupt is enabled. Default Value: 0
6	CE_RX_INT_EN	If this bit is set interrupt is enabled for reception of packet in a connection event. Default Value: 0

### 1.1.80 BLE\_BLELL\_CONN\_INTR\_MASK (continued)

5	CE_TX_ACK_INT_EN	If this bit is set transmission acknowledgement interrupt is enabled: This interrupt is generated to indicate to the firmware that a non-empty packet transmitted is successfully acknowledged by the remote device. For negative acknowledgements from remote device, this interrupt indication is not generated. Default Value: 0
4	CLOSE_CE_INT_EN	If this bit is set connection event closed interrupt is enabled. Default Value: 0
3	START_CE_INT_EN	If this bit is set connection event start interrupt is enabled Default Value: 0
2	MAP_UPDT_INT_EN	If this bit is set, channel map update interrupt is enabled. Default Value: 0
1	CONN_ESTB_INT_EN	If this bit is set connection establishment interrupt is enabled. Default Value: 0
0	CONN_CL_INT_EN	If this bit is set connection closed interrupt is enabled. Default Value: 0

## 1.1.81 BLE\_BLELL\_SLAVE\_TIMING\_CONTROL

slave timing control

Address: 0x402E11F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SLAVE_TIME_SET_VAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SLAVE_TIME_ADJ_VAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SLAVE_TIME_ADJ_VAL	Timing adjust value. The internal micro second counter is adjusted to this value whenever slave receives a good access address match at connection anchor point. This will ensure the slave gets synchronized to master timing. Default Value: 190
7 : 0	SLAVE_TIME_SET_VAL	Programmable adjust value to the clock counter when slave is connected Default Value: 150

## 1.1.82 BLE\_BLELL\_RECEIVE\_TRIG\_CTRL

Receive trigger control

Address: 0x402E11F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ACC_TRIGGER_THRESHOLD [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ACC_TRIGGER_TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	ACC_TRIGGER_TIMEOUT	If access address match does not occur then within this time from the start of receive operation, the receive operation times out and stops. An internal counter value of 1usec resolution is continuously compared with the value programmed. Max value :0xFF Default Value: 0
5 : 0	ACC_TRIGGER_THRESHOLD	Access address match threshold value. Number of bits of access address that should match with the expected access address to trigger an access code match.  Max value : 32 (for 32-bit access address) Lower values may be programmed for bad radios or channels but care must be taken to ensure there are no false matches due to reduced number of bits required to match. Default Value: 0

## 1.1.83 BLE\_BLELL\_DPLL\_CONFIG

DPLL & CY Correlator configuration register

Address: 0x402E1258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DPLL_CORREL_CONFIG [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DPLL_CORREL_CONFIG [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DPLL_CORREL_CONFIG	<p>If CY_CORREL_EN is 0:</p> <p>[2:0] Read pointer correction on DPLL overflow. Optimal setting is 0x4.</p> <p>[6:4] Minimum distance from Rd ptr to Wr ptr to start read in DPLL. Optimal setting is 0x6.</p> <p>[11:8] Sets lower water mark for DPLL. Optimal setting is 0x2.</p> <p>[15:12] Sets upper water mark for DPLL. Optimal setting is 0x9.</p> <p>If CY_CORREL_EN is 1:</p> <p>[11:0] CY correl Access address compare mask for LSB 12 bits. Ideal value is 0xFFFF</p> <p>[15:12] CY correl maximum number of allowed mismatched bits in access address. Ideal value is 0x0.</p> <p>Default Value: 37600</p>

## 1.1.84 BLE\_BLELL\_WHITELIST\_BASE\_ADDR

Whitelist base address

Address: 0x402E1340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WL_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WL_BASE_ADDR	Device address values written to white list memory are written as 16-bit wide address. Default Value: 0

## 1.1.85 BLE\_BLELL\_CONN\_UPDATE\_NEW\_INTERVAL

Connection update new interval

Address: 0x402E13A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_INTERVAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_INTERVAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_INTERVAL	This register will have the new connection interval that the hardware will use after the connection update instant. Before the instant, the connection interval in the register CONN_INTERVAL will be used by hardware. Default Value: 0

## 1.1.86 BLE\_BLELL\_CONN\_UPDATE\_NEW\_LATENCY

Connection update new latency

Address: 0x402E13A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SLV_LATENCY [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SLV_LATENCY [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_SLV_LATENCY	This register will have the new slave latency parameter that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SLAVE_LATENCY will be used by hardware. Default Value: 0



## 1.1.87 BLE\_BLELL\_CONN\_UPDATE\_NEW\_SUP\_TO

Connection update new supervision timeout

Address: 0x402E13AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SUP_TO [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SUP_TO [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_SUP_TO	This register will have the new supervision timeout that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SUP_TIMEOUT will be used by hardware. Default Value: 0

## 1.1.88 BLE\_BLELL\_CONN\_UPDATE\_NEW\_SL\_INTERVAL

Connection update new Slave Latency X Conn interval Value

Address: 0x402E13B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SL_CONN_INTERVAL_VAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SL_CONN_INTERVAL_VAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SL_CONN_INTERVAL_VAL	This register will have the new Slave Latency * Conn Interval value that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SL_CONN_INTERVAL will be used by hardware. Default Value: 0

## 1.1.89 BLE\_BLELL\_CONN\_REQ\_WORD0

Connection request address word 0

Address: 0x402E13C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_LOWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_LOWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ACCESS_ADDR_LOWER	This field defines the lower 16 bits of the access address that is to be sent in the connect request packet of the initiator. Default Value: 0

## 1.1.90 BLE\_BLELL\_CONN\_REQ\_WORD1

Connection request address word 1

Address: 0x402E13C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_UPPER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_UPPER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ACCESS_ADDR_UPPER	This field defines the upper16 bits of the access address that is to be sent in the connect request packet of the initiator. Default Value: 0

## 1.1.91 BLE\_BLELL\_CONN\_REQ\_WORD2

Connection request address word 2

Address: 0x402E13C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_SIZE_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CRC_INIT_LOWER	This field defines the lower byte [7:0] of the CRC initialization value. Default Value: 0
7 : 0	TX_WINDOW_SIZE_VAL	window_size along with the window_offset is used to calculate the first connection point anchor point for the master. This shall be a multiple of 1.25 ms in the range of 1.25 ms to the lesser of 10 ms and (connInterval 1.25 ms). Values range from 0 to 10 ms. Default Value: 0

## 1.1.92 BLE\_BLELL\_CONN\_REQ\_WORD3

Connection request address word 3

Address: 0x402E13CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_UPPER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_UPPER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CRC_INIT_UPPER	This field defines the upper byte [23:8] of the CRC initialization value that is to be sent in the connect request packet of the initiator. Default Value: 0

## 1.1.93 BLE\_BLELL\_CONN\_REQ\_WORD4

Connection request address word 4

Address: 0x402E13D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TX_WINDOW_OFFSET	This is used to determine the anchor point for the master transmission. Range: This shall be a multiple of 1.25 ms in the range of 0 ms to connInterval value. Default Value: 0

## 1.1.94 BLE\_BLELL\_CONN\_REQ\_WORD5

Connection request address word 5

Address: 0x402E13D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL_VAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL_VAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNECTION_INTERVAL_VAL	The value configured in this register determines the spacing between the connection events. This shall be a multiple of 1.25 ms in the range of 7.5 ms to 4.0 s. Default Value: 0



## 1.1.95 BLE\_BLELL\_CONN\_REQ\_WORD6

Connection request address word 6

Address: 0x402E13D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY_VAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY_VAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SLAVE_LATENCY_VAL	The value configured in this field defines the number of consecutive connection events that the slave device is not required to listen for master. The value of connSlaveLatency should not cause a Supervision Timeout. This shall be an integer in the range of 0 to ((connSupervision Timeout/connInterval)-1). connSlaveLatency shall also be less than 500. Default Value: 0

## 1.1.96 BLE\_BLELL\_CONN\_REQ\_WORD7

Connection request address word 7

Address: 0x402E13DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT_VAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT_VAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SUPERVISION_TIMEOUT_VAL	This field defines the maximum time between two received Data packet PDUs before the connection is considered lost. This shall be a multiple of 10 ms in the range of 100 ms to 32.0 s and it shall be larger than (1+connSlaveLatency)*connInterval. Default Value: 0

## 1.1.97 BLE\_BLELL\_CONN\_REQ\_WORD8

Connection request address word 8

Address: 0x402E13E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_LOWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_LOWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_LOWER	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

## 1.1.98 BLE\_BLELL\_CONN\_REQ\_WORD9

Connection request address word 9

Address: 0x402E13E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_MID [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_MID [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_MID	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (31:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

## 1.1.99 BLE\_BLELL\_CONN\_REQ\_WORD10

Connection request address word 10

Address: 0x402E13E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			DATA_CHANNELS_UPPER [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_UPPER	This register field indicates which of the data channels are in use. This stores the information for the upper 5 (36:32) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

## 1.1.100 BLE\_BLELL\_CONN\_REQ\_WORD11

Connection request address word 11

Address: 0x402E13EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	RW			RW				
Name	SCA_2 [7:5]			HOP_INCREMENT_2 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 5	SCA_2	This field defines the sleep clock accuracies given in ppm. Default Value: 0
4 : 0	HOP_INCREMENT_2	This field is used for the data channel selection process. Default Value: 0

## 1.1.101 BLE\_BLELL\_PACKET\_COUNTER0

Packet counter 0

Address: 0x402E1400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PACKET_COUNTER_LOWER	Lower 16-bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0

## 1.1.102 BLE\_BLELL\_PACKET\_COUNTER1

Packet counter 1

Address: 0x402E1404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_MIDDLE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_MIDDLE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PACKET_COUNTER_MIDDLE	Middle 16-bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0



## 1.1.103 BLE\_BLELL\_PACKET\_COUNTER2

Packet counter 2

Address: 0x402E1408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_UPPER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PACKET_COUNTER_UPPER	Upper 8 bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0

## 1.1.104 BLE\_BLELL\_IV\_MASTER0

Master Initialization Vector 0

Address: 0x402E1410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_MASTER_LOWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_MASTER_LOWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_MASTER_LOWER	This is the lower 16-bits of the IVm field, which contains the masters portion of the initialization vector. Default Value: 0

## 1.1.105 BLE\_BLELL\_IV\_MASTER1

Master Initialization Vector 1

Address: 0x402E1414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_MASTER_UPPER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_MASTER_UPPER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_MASTER_UPPER	This is the upper 16-bits of the IVm field, which contains the masters portion of the initialization vector. Default Value: 0

## 1.1.106 BLE\_BLELL\_IV\_SLAVE0

Slave Initialization Vector 0

Address: 0x402E1418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_LOWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_LOWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_SLAVE_LOWER	This is the lower 16-bits of the IVs field, which contains the slaves portion of the initialization vector. Default Value: 0

## 1.1.107 BLE\_BLELL\_IV\_SLAVE1

Slave Initialization Vector 1

Address: 0x402E141C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_UPPER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_UPPER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_SLAVE_UPPER	This is the upper 16-bits of the IVs field, which contains the slaves portion of the initialization vector. Default Value: 0

## 1.1.108 BLE\_BLELL\_ENC\_KEY0

Encryption Key register 0-7

Address: 0x402E1420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

## 1.1.109 BLE\_BLELL\_ENC\_KEY1

Encryption Key register 0-7

Address: 0x402E1424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

## 1.1.110 BLE\_BLELL\_ENC\_KEY2

Encryption Key register 0-7

Address: 0x402E1428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0



## 1.1.111 BLE\_BLELL\_ENC\_KEY3

Encryption Key register 0-7

Address: 0x402E142C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

## 1.1.112 BLE\_BLELL\_ENC\_KEY4

Encryption Key register 0-7

Address: 0x402E1430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

## 1.1.113 BLE\_BLELL\_ENC\_KEY5

Encryption Key register 0-7

Address: 0x402E1434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

## 1.1.114 BLE\_BLELL\_ENC\_KEY6

Encryption Key register 0-7

Address: 0x402E1438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

## 1.1.115 BLE\_BLELL\_ENC\_KEY7

Encryption Key register 0-7

Address: 0x402E143C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

## 1.1.116 BLE\_BLELL\_DATA0

Input / Output Data register

Address: 0x402E1440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA0 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA0 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA0	Write: Bytes 1 and 0 of the input plain text to be encrypted. Read: Bytes 1 and 0 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.117 BLE\_BLELL\_DATA1

Input / Output Data register

Address: 0x402E1444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA1 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA1 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA1	Write: Bytes 3 and 2 of the input plain text to be encrypted. Read: Bytes 3 and 2 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.118 BLE\_BLELL\_DATA2

Input / Output Data register

Address: 0x402E1448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA2 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA2 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA2	Write: Bytes 5 and 4 of the input plain text to be encrypted. Read: Bytes 5 and 4 of the decrypted plain text/ encrypted text. Default Value: 0



## 1.1.119 BLE\_BLELL\_DATA3

Input / Output Data register

Address: 0x402E144C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA3 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA3 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA3	Write: Bytes 7 and 6 of the input plain text to be encrypted. Read: Bytes 7 and 6 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.120 BLE\_BLELL\_DATA4

Input / Output Data register

Address: 0x402E1450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA4	Write: Bytes 9 and 8 of the input plain text to be encrypted. Read: Bytes 9 and 8 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.121 BLE\_BLELL\_DATA5

Input / Output Data register

Address: 0x402E1454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA5 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA5	Write: Bytes 11 and 10 of the input plain text to be encrypted. Read: Bytes 11 and 10 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.122 BLE\_BLELL\_DATA6

Input / Output Data register

Address: 0x402E1458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA6 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA6 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA6	Write: Bytes 13 and 12 of the input plain text to be encrypted. Read: Bytes 13 and 12 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.123 BLE\_BLELL\_DATA7

Input / Output Data register

Address: 0x402E145C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA7 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA7 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA7	Write: Bytes 15 and 14 of the input plain text to be encrypted. Read: Bytes 15 and 14 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.124 BLE\_BLELL\_DATA8

Input / Output Data register

Address: 0x402E1460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA8 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA8 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA8	Write: Bytes 17 and 16 of the input plain text to be encrypted. Read: Bytes 17 and 16 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.125 BLE\_BLELL\_DATA9

Input / Output Data register

Address: 0x402E1464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA9 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA9 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA9	Write: Bytes 19 and 18 of the input plain text to be encrypted. Read: Bytes 19 and 18 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.126 BLE\_BLELL\_DATA10

Input / Output Data register

Address: 0x402E1468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA10 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA10 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA10	Write: Bytes 21 and 20 of the input plain text to be encrypted. Read: Bytes 21 and 20 of the decrypted plain text/ encrypted text. Default Value: 0



## 1.1.127 BLE\_BLELL\_DATA11

Input / Output Data register

Address: 0x402E146C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA11 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA11 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA11	Write: Bytes 23 and 22 of the input plain text to be encrypted. Read: Bytes 23 and 22 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.128 BLE\_BLELL\_DATA12

Input / Output Data register

Address: 0x402E1470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA12 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA12 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA12	Write: Bytes 25 and 24 of the input plain text to be encrypted. Read: Bytes 25 and 24 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.129 BLE\_BLELL\_DATA13

Input / Output Data register

Address: 0x402E1474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA13 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA13	Write: Byte 26 of the input plain text to be encrypted. Read: Byte 26 of the decrypted plain text/ encrypted text. Default Value: 0

## 1.1.130 BLE\_BLELL\_MIC\_IN0

MIC input register

Address: 0x402E1478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MIC_IN_LOWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MIC_IN_LOWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_IN_LOWER	This is the lower 16-bits of the MIC field used for CCM decryption. Default Value: 0

## 1.1.131 BLE\_BLELL\_MIC\_IN1

MIC input register

Address: 0x402E147C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MIC_IN_UPPER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MIC_IN_UPPER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_IN_UPPER	This is the upper 16-bits of the MIC field used for CCM decryption. Default Value: 0

## 1.1.132 BLE\_BLELL\_MIC\_OUT0

MIC output register

Address: 0x402E1480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MIC_OUT_LOWER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MIC_OUT_LOWER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_OUT_LOWER	This is the lower 16-bits of the MIC generated during CCM encryption. Default Value: 0

## 1.1.133 BLE\_BLELL\_MIC\_OUT1

MIC output register

Address: 0x402E1484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MIC_OUT_UPPER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MIC_OUT_UPPER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_OUT_UPPER	This is the lower 16-bits of the MIC generated during CCM encryption. Default Value: 0

## 1.1.134 BLE\_BLELL\_ENC\_PARAMS

Encryption Parameter register

Address: 0x402E1488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	DIRECTION	PAYLOAD_LENGTH [6:2]					DATA_PDU_HEADER [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DIRECTION	The directionBit shall be set to 1 for Data Channel PDUs sent by the master and set to 0 for Data Channel PDUs sent by the slave. Default Value: 0
6 : 2	PAYLOAD_LENGTH	Length of the input data. Default Value: 0
1 : 0	DATA_PDU_HEADER	LLID of the packet. Default Value: 0



## 1.1.135 BLE\_BLELL\_ENC\_CONFIG

Encryption Configuration

Address: 0x402E1490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					DEC_ENC	ECB_CCM	START_PRO OC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	DEC_ENC	Decryption/Encryption 0 - Encrypt 1 - Decrypt Default Value: 0
1	ECB_CCM	0 - CCM 1 - ECB Default Value: 0
0	START_PROC	1 Start the AES processing Default Value: 0

## 1.1.136 BLE\_BLELL\_ENC\_INTR\_EN

Encryption Interrupt enable

Address: 0x402E1498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CCM_PRO C_INTR_E N	ECB_PRO C_INTR_EN	AUTH_PAS S_INTR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CCM_PROC_INTR_EN	CCM processed interrupt enable 0 - Disable 1 - Enable Default Value: 0
1	ECB_PROC_INTR_EN	ECB processed interrupt enable 0 - Disable 1 - Enable Default Value: 0
0	AUTH_PASS_INTR_EN	Authentication interrupt enable 0 - Disable 1 - Enable Default Value: 0

## 1.1.137 BLE\_BLELL\_ENC\_INTR

Encryption Interrupt status and clear register

Address: 0x402E14A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W	RW1C	RW1C	RW1C
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				IN_DATA_C LEAR	CCM_PRO C_INTR	ECB_PRO C_INTR	AUTH_PAS S_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	IN_DATA_CLEAR	Clears the input data. Used for Zero padding of encryption for less than block sized data. Default Value: 0
2	CCM_PROC_INTR	CCM processed interrupt. Writing 1 to this register clears the interrupt Default Value: 0
1	ECB_PROC_INTR	ECB processed interrupt. Writing 1 to this register clears the interrupt. Default Value: 0
0	AUTH_PASS_INTR	Authentication interrupt. 0x1- indicates MIC matched 0x0 indicated MIC mismatched Writing 1 to this register clears the interrupt. Default Value: 0

## 1.1.138 BLE\_BLELL\_CONN\_TXMEM\_BASE\_ADDR

Connection TX memory base address

Address: 0x402E1600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_TX_MEM_BASE_ADDR	Data values written to Tx memory are written as 16-bit wide data. Default Value: 0

## 1.1.139 BLE\_BLELL\_CONN\_RXMEM\_BASE\_ADDR

Connection RX memory base address

Address: 0x402E1800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_RX_MEM_BASE_ADDR	Data values written to Rx memory are written as 16-bit wide data Default Value: 0

## 1.1.140 BLE\_BLELL\_PDU\_RESP\_TIMER

PDU response timer

Address: 0x402E1A04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PDU_RESP_TIME_VAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PDU_RESP_TIME_VAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_RESP_TIME_VAL	<p>This register is loaded with the count value to monitor the time to get a response for a PDU from peer device.</p> <p>Firmware starts the timer by issuing the command, RESP_TIMER_ON, after it has queued a PDU for transmission, that requires a response.</p> <p>If a response is received, firmware stops and clears the timer by issuing the command RESP_TIMER_OFF.</p> <p>If this timer expires, it results in hardware closing the connection and triggering a conn_closed interrupt.</p> <p>The discon_status field in the Connection status register is set with the appropriate reason.</p> <p>Units : Milliseconds.</p> <p>Resolution : 1.25 ms</p> <p>Default Value: 0</p>

## 1.1.141 BLE\_BLELL\_NEXT\_RESP\_TIMER\_EXP

Next response timeout instant

Address: 0x402E1A08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_RESPONSE_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_RESPONSE_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_RESPONSE_INSTANT	<p>This field defines the clock instant at which the next PDU response timeout event will occur on a connection.</p> <p>This is with reference to the 16-bit internal reference clock.</p> <p>Default Value: 0</p>

## 1.1.142 BLE\_BLELL\_NEXT\_SUP\_TO

Next supervision timeout instant

Address: 0x402E1A0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_TIMEOUT_INSTANT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_TIMEOUT_INSTANT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_TIMEOUT_INSTANT	This field defines the clock instant at which the next connection supervision timeout event will occur on a connection This is with reference to the 16-bit internal reference clock. Default Value: 0



## 1.1.143 BLE\_BLELL\_LLH\_FEATURE\_CONFIG

Feature enable

Address: 0x402E1A10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						SL_DSM_EN	QUICK_TRANSMIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SL_DSM_EN	Enable/Disable Slave Latency Period DSM. Default Value: 1
0	QUICK_TRANSMIT	Quick transmit feature in slave latency is enabled by setting this bit. When slave latency is enabled, this feature enables the slave to transmit in the immediate connection interval, in case required, instead of waiting till the end of slave latency Default Value: 0

## 1.1.144 BLE\_BLELL\_WIN\_MIN\_STEP\_SIZE

Window minimum step size

Address: 0x402E1A14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	STEPUP [7:4]				STEPDN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WINDOW_MIN_FW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WINDOW_MIN_FW	Minimum window interval value programmed by firmware. While the slave receive window is decremented, the windows_min_fw sets the lowest value of the window widen value to ensure packets are not missed. The unit is in microseconds. Default Value: 32
7 : 4	STEPUP	If packets are missed, the reference window is gradually increased by step up size, until it receives 2 consecutive good packets. The unit is in microseconds Default Value: 6
3 : 0	STEPDN	After receiving 2 consecutive good packets the reference window is gradually decremented by step down size until it reaches window minimum. The unit is in microseconds Default Value: 4

## 1.1.145 BLE\_BLELL\_SLV\_WIN\_ADJ

Slave window adjustment

Address: 0x402E1A18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SLV_WIN_ADJ [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					SLV_WIN_ADJ [10:8]		
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	SLV_WIN_ADJ	Window Adjust value. This value is added to the calculated slave window widening value to be used as final window widen value. Default Value: 16

## 1.1.146 BLE\_BLELL\_SL\_CONN\_INTERVAL

Slave Latency X Conn Interval Value

Address: 0x402E1A1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SL_CONN_INTERVAL_VAL [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SL_CONN_INTERVAL_VAL [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SL_CONN_INTERVAL_VAL	This field defines the (SL*CI) product for the ongoing connection. This value is used in calculation of next connection instant during slave latency. Default Value: 0

## 1.1.147 BLE\_BLELL\_LE\_PING\_TIMER\_ADDR

LE Ping connection timer address

Address: 0x402E1A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIMER_ADDR	The register used to configure the LE Au-thenticated payload Timeout (LE APTO) which is the Maximum amount of time specified between packets authenticated by a MIC. This value of ping timer is in the order of 10ms, valid range 0x1 ~ 0xFFFF Default Value: 0

## 1.1.148 BLE\_BLELL\_LE\_PING\_TIMER\_OFFSET

LE Ping connection timer offset

Address: 0x402E1A24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_OFFSET [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_OFFSET [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIMER_OFFSET	The value of ping timer nearly expired offset in the order of 10ms, valid range 0x0 ~ 0xFFFF. This is the time period after which the ping timer nearly expired interrupt is generated. Default Value: 0

## 1.1.149 BLE\_BLELL\_LE\_PING\_TIMER\_NEXT\_EXP

LE Ping timer next expiry instant

Address: 0x402E1A28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONN_PING_TIMER_NEXT_EXP [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONN_PING_TIMER_NEXT_EXP [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIMER_NEXT_EXP	The value of ping timer next expiry instant in the terms of native clock value (least 16 bit value of the 17 bit ping counter). This together with CONN_PING_TIMER_NEXT_EXP_WRAP will provide the correct status of ping timer duration. Default Value: 0

## 1.1.150 BLE\_BLELL\_LE\_PING\_TIMER\_WRAP\_COUNT

LE Ping Timer wrap count

Address: 0x402E1A2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONN_SEC_CURRENT_WRAP [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONN_SEC_CURRENT_WRAP [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_SEC_CURRENT_WRAP	This register holds the current position of the Ping timer. Default Value: 0



## 1.1.151 BLE\_BLELL\_TX\_EN\_EXT\_DELAY

Transmit enable extension delay

Address: 0x402E1E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TXEN_EXT_DELAY [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	TXEN_EXT_DELAY	Transmit enable extension delay. This is to extend the active state (high) of rif_tx_en signal after the last bit is sent out from LLH. The unit is in microsecond and the supported range is 00 31 us. Default Value: 5

## 1.1.152 BLE\_BLELL\_TX\_RX\_SYNTH\_DELAY

Transmit/Receive enable delay

Address: 0x402E1E04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RX_EN_DELAY [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TX_EN_DELAY [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	TX_EN_DELAY	<p>The delay used to assert <code>rif_tx_en</code> exactly <code>Tx_tRamp</code> micro-seconds ahead of the first bit of the <code>tx_data</code>, which can be used to turn on the Radio transmitter.</p> <p>The value to be programmed to the <code>Tx_en_delay [7:0]</code> = <code>tx_on_delay - Tx_tRamp</code>  <code>tx_on_delay[7:0] = TX_RX_ON_DELAY[15:8]</code>  <code>Tx_tRamp</code> = Radio transmitter ramp_up  Default Value: 0</p>
7 : 0	RX_EN_DELAY	<p>The delay used to assert <code>rif_rx_en</code>, <code>Rx_tRamp</code> micro-seconds, ahead of first bit of the expected <code>rx_data</code>, which can be used to turn on the Radio receiver.</p> <p>The value to be programmed to the <code>Rx_en_delay [7:0]</code> = <code>rx_on_delay - Rx_tRamp</code>  <code>rx_on_delay[7:0] = TX_RX_ON_DELAY[7:0]</code>  <code>Rx_tRamp</code> = Radio receiver rampup time  Default Value: 0</p>

## 2 BLE Radio (BLERD) Registers



This section discusses the BLERD registers. It lists all the registers in mapping tables, in address order.

### 2.1 Register Details

Register Name	Address
<a href="#">BLE_BLERD_CFG1</a>	0x402E0000
<a href="#">BLE_BLERD_CFG2</a>	0x402E0004
<a href="#">BLE_BLERD_MODEM</a>	0x402E0008
<a href="#">BLE_BLERD_FSM</a>	0x402E000C
<a href="#">BLE_BLERD_DBUS</a>	0x402E0010
<a href="#">BLE_BLERD_CFGCTRL</a>	0x402E0014
<a href="#">BLE_BLERD_RSSI</a>	0x402E0018
<a href="#">BLE_BLERD_RMAP</a>	0x402E0024
<a href="#">BLE_BLERD_KVCAL</a>	0x402E0028
<a href="#">BLE_BLERD_CFG_1_FCAL</a>	0x402E002C
<a href="#">BLE_BLERD_CFG_2_FCAL</a>	0x402E0030
<a href="#">BLE_BLERD_CFG_3_FCAL</a>	0x402E0034
<a href="#">BLE_BLERD_CFG_4_FCAL</a>	0x402E0038
<a href="#">BLE_BLERD_CFG_5_FCAL</a>	0x402E003C
<a href="#">BLE_BLERD_CFG_6_FCAL</a>	0x402E0040
<a href="#">BLE_BLERD_FCAL_TEST</a>	0x402E0044
<a href="#">BLE_BLERD_TEST</a>	0x402E0048
<a href="#">BLE_BLERD_FPD_TEST</a>	0x402E004C
<a href="#">BLE_BLERD_SY</a>	0x402E0050
<a href="#">BLE_BLERD_TEST2_SY</a>	0x402E0054
<a href="#">BLE_BLERD_TX</a>	0x402E0058
<a href="#">BLE_BLERD_RX</a>	0x402E005C
<a href="#">BLE_BLERD_DIAG1</a>	0x402E0060
<a href="#">BLE_BLERD_IM</a>	0x402E0064
<a href="#">BLE_BLERD_LDO_BYPASS</a>	0x402E0068
<a href="#">BLE_BLERD_LDO</a>	0x402E006C
<a href="#">BLE_BLERD_BB_BUMP1</a>	0x402E0070

Register Name	Address
BLE_BLERD_BB_BUMP2	0x402E0074
BLE_BLERD_BB_XO	0x402E0078
BLE_BLERD_BB_XO_CAPTRIM	0x402E007C
BLE_BLERD_SY_BUMP1	0x402E0080
BLE_BLERD_SY_BUMP2	0x402E0084
BLE_BLERD_TX_BUMP1	0x402E0088
BLE_BLERD_TX_BUMP2	0x402E008C
BLE_BLERD_RX_BUMP1	0x402E0090
BLE_BLERD_RX_BUMP2	0x402E0094
BLE_BLERD_ADC_BUMP1	0x402E0098
BLE_BLERD_ADC_BUMP2	0x402E009C
BLE_BLERD_BALUN	0x402E00A0
BLE_BLERD_CTR1	0x402E00A4
BLE_BLERD_AGC	0x402E00A8
BLE_BLERD_THRSHD1	0x402E00AC
BLE_BLERD_THRSHD2	0x402E00B0
BLE_BLERD_THRSHD3	0x402E00B4
BLE_BLERD_THRSHD4	0x402E00B8
BLE_BLERD_THRSHD5	0x402E00BC
BLE_BLERD_DC	0x402E00C0
BLE_BLERD_IQMIS	0x402E00C4
BLE_BLERD_DCCAL	0x402E00C8
BLE_BLERD_RCCAL	0x402E00CC
BLE_BLERD_DSM1	0x402E00D0
BLE_BLERD_DSM2	0x402E00D4
BLE_BLERD_DSM3	0x402E00D8
BLE_BLERD_DSM4	0x402E00DC
BLE_BLERD_DSM5	0x402E00E0
BLE_BLERD_DSM6	0x402E00E4
BLE_BLERD_MONI	0x402E00E8
BLE_BLERD_DBG_BB	0x402E00EC
BLE_BLERD_DBG_1	0x402E00F0
BLE_BLERD_DBG_2	0x402E00F4
BLE_BLERD_DBG_3	0x402E00F8
BLE_BLERD_READ_IQ_1	0x402E0100
BLE_BLERD_READ_IQ_2	0x402E0104
BLE_BLERD_READ_IQ_3	0x402E0108
BLE_BLERD_READ_IQ_4	0x402E010C

## 2.1.1 BLE\_BLERD\_CFG1

Generic configure register.

Address: 0x402E0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TX_PA_RAMP_MODE	ADC_IQ_INVERSE	EN_BR_CLK	CLKGATING_DISABLE	RF_PLL_DIRECT	AGC_DISABLE	TX_DATA_INVERSE	RX_DATA_INVERSE

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW		RW	RW	RW
HW Access	R			R		R	R	R
Name	LNA_GAIN [15:13]			CBPF_GAIN [12:11]		BURNIN_CLK_EN	ADC_DC_CAPTURE_EN	RADIO_STANDALONE

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	LNA_GAIN	LNA+TIA manually gain setting when AGC is disabled by asserting bit[2]. The gain obtained is a function of the LNA gm as well as the TIA feedback resistor. 101: VH, 100: H, 011: IH, 010: M, 001: L, 000: VL Default Value: 5
12 : 11	CBPF_GAIN	CBPF manually gain setting when AGC is disabled by asserting bit[2]. This gain is truly reflective of the voltage gain across the CBPF and is determined by the ratio of resistors 11: 15dB, 10: 12dB, 01: 3dB, 00: 0dB Default Value: 3
10	BURNIN_CLK_EN	burn in function mode 1: digital main clock from clk_core. 0: digital main clock from HardIP Default Value: 0
9	ADC_DC_CAPTURE_EN	1: ADC DC capture enable Default Value: 1

### 2.1.1 BLE\_BLERD\_CFG1 (continued)

8	RADIO_STANDALONE	1: radio standalone without link layer controller in SoC, Tx command from reg0x10[13] and RX command from reg0x10[12] Default Value: 0
7	TX_PA_RAMP_MODE	1: ramp to PA gain which given txpa_gain in 2dB steps, starting from min gain. 0: ramp to PA gain which given in txpa_gain in one short from min gain Default Value: 0
6	ADC_IQ_INVERSE	1: swap ADC I, Q path Default Value: 1
5	EN_BR_CLK	1: enable brclk output Default Value: 0
4	CLKGATING_DISABLE	1. disable the clock gating logic globally. Independent of any other conditions. None of the clocks can be gated when this bit is set. 0: clock gating logic is enabled, the logic in clk_gen will determine which clocks are to be gated. Default Value: 0
3	RF_PLL_DIRECT	program channel frequency as direct frequency mode. high active. When RF_PLL_DIRECT = 1, RF = reg0x10[11:0] Mhz. When RF_PLL_DIRECT = 0, RF = 2402 + 2*reg7[5:0] Mhz. Default Value: 0
2	AGC_DISABLE	1: disable the AGC, the LNA+TIA and CBPF gain are given based on bits [15:11] of reg0. Default Value: 0
1	TX_DATA_INVERSE	invert modulation transmit data, high active Default Value: 0
0	RX_DATA_INVERSE	Invert demodulation receiving data, high active Default Value: 0

## 2.1.2 BLE\_BLERD\_CFG2

Generic configure register.

Address: 0x402E0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DAC_REG_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW	RW		RW	
HW Access	R	R		R	R		R	
Name	ADC_DFT_EN	ADC_DFT_MODE [14:13]		DAC_DFT_EN	DAC_DFT_MODE [11:10]		DAC_REG_DATA [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	ADC_DFT_EN	1: ADC DFT enable Default Value: 0
14 : 13	ADC_DFT_MODE	Reserved - this bit is not available and should be set to 0. Default Value: 0
12	DAC_DFT_EN	1: DAC DFT mode enable Default Value: 0
11 : 10	DAC_DFT_MODE	DAC DFT mode definition 00: DAC input from dac_reg_data[9:0] 01: DAC input as 12Mhz increased value 10: DAC input as 1MHz Sine Wave 11: DAC input as 4MHz SIN wave Default Value: 0
9 : 0	DAC_REG_DATA	DAC input from this register when CFG2_DAC_DFT_EN =1 and dft_mode = 2'b00 Default Value: 512

## 2.1.3 BLE\_BLERD\_MODEM

modem configuration

Address: 0x402E0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	DC_PARAM [7:6]		RESET2_EN	RST_CNT2_SEL	WIDE_SPD [3:2]		NARROW_SPD [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CW_MODE	ADCDFT_SEL	READ_DC_OFFSET_SEL	LOAD_PREV_GAIN_EN	ADC_PWR_EST_EN	DC_SCALING_EN	ADC_FULL_SWING_DETECT_EN	IMREJ_BYPASS

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CW_MODE	1: modulation continue wave output Default Value: 0
14	ADCDFT_SEL	1: ADC DFT capture data after image filter 0: ADC DFT capture data before image filter Default Value: 0
13	READ_DC_OFFSET_SEL	1: read back of analog DC CAL result. 0: read back of DC capture in digital Default Value: 0
12	LOAD_PREV_GAIN_EN	1: load previous RX packet gain setting at first gain change step 0: not load previous RX packet gain. Default Value: 1
11	ADC_PWR_EST_EN	1: power estimation for ADC output is enabled. Default Value: 0



### 2.1.3 BLE\_BLERD\_MODEM (continued)

10	DC_SCALING_EN	1: DC scaling is enabled in the Demodulator. The Scaling happens when CBPF gain changes. Default Value: 0
9	ADC_FULL_SWING_DETECT_EN	1: select new AGC methodology with ADC full swing detection Default Value: 0
8	IMREJ_BYPASS	bypass image filter in demodulation Default Value: 0
7 : 6	DC_PARAM	demodulation frequency deviation selection 00: 320K, 01: 350K, 10: 400K, 11:430K Default Value: 1
5	RESET2_EN	demodulation soft reset enable, 0: disable, 1: enable soft reset Default Value: 1
4	RST_CNT2_SEL	soft reset condition selection, 0: 32bits all '0'/1', 1: 16bits all '0'/1' Default Value: 0
3 : 2	WIDE_SPD	demodulation alpha value for DC offset tracking in wide speed 00: dc value times 8 01: dc value times 10 10: dc value times 12 11: dc value times 14 Default Value: 2
1 : 0	NARROW_SPD	set alpha value for dC offset tracking speed in narrow mode 00: dc value times 1 01: dc value times 2 10: dc value times 3 11: dc value times 4 Default Value: 0

## 2.1.4 BLE\_BLERD\_FSM

RFCTRL state information

Address: 0x402E000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R			R	R	R	R	R
HW Access	W			W	W	W	W	W
Name	RX_STATE [7:5]			ISO_ENAB LE	FCAL_PAS S_DETECT	LFLDO_OK	LSLDO_OK	XO_AMP_D TECT

Bits	15	14	13	12	11	10	9	8
SW Access	R		R			R		
HW Access	W		W			W		
Name	STATE [15:14]		SY_STATE [13:11]			TX_STATE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	STATE	RFCTRL major state, 00: sleep mode, 11: idle mode, 01: TX mode, 01: RX mode Default Value: 3
13 : 11	SY_STATE	RFCTRL SYNTH state 000: SY off, 001: SY Regulator power up, 010: SY VCO pup up 011: SY LO path power up, 100: Frequency calibration, 101: PLL setting. 110: PLL locked Default Value: 0

## 2.1.4 BLE\_BLERD\_FSM (continued)

10 : 8	TX_STATE	RFCTRL TX state 000: TX Off 001: TX Regulator Powerup 010: TX Baseband Powerup 011: KV Calibration 100: TX PLL Settling 101: TX Ready Default Value: 0
7 : 5	RX_STATE	RFCTRL RX state 000: RX Off 001: RX Regulator Powerup 010: RX Baseband and IF Powerup 011: DC Calibration 100: RX Wait for PLL settling 101: RX ADC DC value capture 110: RX Receive ON Default Value: 0
4	ISO_ENABLE	monitor isolation cell enable signal 1: isolation cell enabled. Default Value: 1
3	FCAL_PASS_DETECT	TX balun power detector, 1: Frequency calibration has passed. 0: Frequency calibration has failed Default Value: 0
2	LFLDO_OK	1: LF LDO powered up Default Value: 0
1	LSLDO_OK	1: LS LDO powered up Default Value: 0
0	XO_AMP_DETECT	1: XO is oscillating reached 60% amplitude. 0: XO is no oscillating or not reached 60% amplitude. BLERD_BB_XO[1] determines fast or normal charge. XO within 50ppm needs 2 times of XO detection BLERD_BB_XO[1]    XO_amp_detect    XO stable 1                   320us           640us 0                   1120us          2.24ms Default Value: 0

## 2.1.5 BLE\_BLERD\_DBUS

RFCTRL mode transition control

Address: 0x402E0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RF_FREQ [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW			
HW Access	R	R	R	R	R			
Name	XTAL_ENA BLE	ISOLATE_N	DIRECT_T XEN	DIRECT_R XEN	RF_FREQ [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	XTAL_ENABLE	crystal enable. High active Default Value: 0
14	ISOLATE_N	force isolation cell enable of analog / digital boundary. low active Default Value: 1
13	DIRECT_TXEN	When cfg1_radio_standalone =1, dbus_direct_rxen replace dbus_rx_en Default Value: 0
12	DIRECT_RXEN	When cfg1_radio_standalone =1, dbus_direct_rxen replace dbus_rx_en Default Value: 0
11 : 0	RF_FREQ	When CFG1_RF_PLL_DIRECT=1, RF frequency is direct program from DBUS register [11:0] Default Value: 2450

## 2.1.6 BLE\_BLERD\_CFGCTRL

RFCTRL running configuration

Address: 0x402E0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW				
HW Access	R	R	R	R				
Name	DCCAL_M ODE	DCCAL_RE RUN	IGNORE_F RAC	DSM_MODE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None			RW	RW	RW	RW
HW Access	R	None			R	R	R	R
Name	TESTMOD E_EN	None [14:12]			FCAL_RER UN	KVCAL_RE RUN	RCCAL_M ODE	RCCAL_RE RUN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	TESTMODE_EN	1: enables the test mode feature of RFCTRL Default Value: 0
11	FCAL_RERUN	1: KVCAL will be force rerun when cfgctrl_testmode_en = 1 Default Value: 0
10	KVCAL_RERUN	1: FCAL will be force rerun when cfgctrl_testmode_en = 1 Default Value: 0
9	RCCAL_MODE	0: normal mode 1: slow mode, The timer for each setp in calibration is doubled with normal mode Default Value: 0
8	RCCAL_RERUN	1: RC-cal force to rerun when cfgctrl_testmode_en = 1 Default Value: 0
7	DCCAL_MODE	0: RX DC offset calibration in run normal mode 1: RX DC offset calibration is run in slow mode. Here each step in calibration is given double time compared to the normal mode Default Value: 0

## 2.1.6 BLE\_BLERD\_CFGCTRL (continued)

6	DCCAL_RERUN	1: DC CAL is forced to run when cfgctrl_testmode_en = 1 Default Value: 0
5	IGNORE_FRAC	0: Do not ignore fractional part in DSM (Frac-N PLL). 1: Ignore the fractional part in DSM (Int-N PLL). Default Value: 0
4 : 0	DSM_MODE	Cfgctrl_dsm_mode[4]: 1b0: Third order PLL is used in TX mode, this is not effective in RX mode 1b1: First order PLL is used in TX mode, this is not effective in RX mode  Cfgctrl_dsm_mode[3:2] The following bits determine the DSM mode in TX 00: Input dither but no initial condition for DSM 01: Input dither and initial condition to DSM. 10: No input dither and initial condition 11: No input dither but initial condition is given  Cfgctrl_dsm_mode[1:0] The following bits determine the DSM mode in RX 00: Input dither but no initial condition for DSM 01: Input dither and initial condition to DSM. 10: No input dither and initial condition 11: No input dither but initial condition is given Default Value: 24

## 2.1.7 BLE\_BLERD\_RSSI

RX envelope detector and RSSI value

Address: 0x402E0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	PREFILT [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None	POSTFILT [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	POSTFILT	RSSI value after the filter in digital, 0 represents -85dBm Default Value: 0
6 : 0	PREFILT	RSSI value before the filter in thd digital, 0 represents -85dBm Default Value: 0

## 2.1.8 BLE\_BLERD\_RMAP

BG LDO bypass mode

Address: 0x402E0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BB_BYPASS [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BB_BYPASS [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
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## 2.1.8 BLE\_BLERD\_RMAP (continued)

15 : 0	BB_BYPASS	<p>[0]:bypass lsldo ok signal if set this bit</p> <p>[1]:bypass lfldo ok signal if set this bit</p> <p>[2]:bypass xo amp detect if set this bit</p> <p>[3]:BG output is force external by enabling T-gate if set this bit</p> <p>[4]: bypass LF LDO and the line supply is directly given out as regulator output. This field should not be enable if line supply is moreh than 2.1V. This should not toggled in Scan Mode</p> <p>[5]: bypass LS LDO and the line supply is directly given out as regulator output. This field should not be enable if line supply is moreh than 2.1V. This should not toggled in Scan Mode</p> <p>[6]: bypass BBV2LDO and the line supply is directly given out as regulator output. This field should not be enable if line supply is moreh than 2.1V. This should not toggled in Scan Mode</p> <p>[7]:spare bit</p> <p>[8]:0: LF LDO power down controlled by m0s8blerd 1: powerdown LF LDO</p> <p>[9]:0: LS LDO power down controlled by m0s8blerd 1: power done LS LDO</p> <p>[10]:0: BG LDO power down controlled by m0s8blerd 1: power down BG LDO</p> <p>[11]:0: V2ILDO power down controlled by m0s8blerd 1: power done V2ILDO</p> <p>[15:12]:reserved for furture</p> <p>Default Value: 0</p>
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## 2.1.9 BLE\_BLERD\_KVCAL

KVCAL running configuration

Address: 0x402E0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	EXP_FREQ_DIFF [7:4]				RUN_DURATION [3:2]		DAC_STEP [1:0]	
Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				EXP_FREQ_DIFF [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 4	EXP_FREQ_DIFF	This expected difference in KVCAL configuration counts(100 counts for an idela modulation path gain) Default Value: 100
3 : 2	RUN_DURATION	This values tells by what value should the DAC be offset from the mid-code, when the KVCAL is running. 00 : 512 (1MHz deviation). 01: 376 (0.75 Mhz deviation). 10: 256 (0.5 Mhz deviation) 11 : 128 (0.25 Mhz deviation) Default Value: 0
1 : 0	DAC_STEP	This values tells by what value should the DAC be offset from the mid-code, when the KVCAL is running. 00 : 512 (1MHz deviation). 01: 376 (0.75 Mhz deviation). 10: 256 (0.5 Mhz deviation) 11 : 128 (0.25 Mhz deviation) Default Value: 0

## 2.1.10 BLE\_BLERD\_CFG\_1\_FCAL

FCAL running configure 5\_6

Address: 0x402E002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_FRAMES_7	COARSE_FRAMES_6 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_7 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_7	numbere of frames to run for the calibration 7th coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_6	numbere of frames to run for the calibration 6th coarse bit Default Value: 7

## 2.1.11 BLE\_BLERD\_CFG\_2\_FCAL

FCAL running configure 7\_2

Address: 0x402E0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_F RAMES_5	COARSE_FRAMES_4 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_5 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_5	numbere of frames to run for the calibration 5th coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_4	numbere of frames to run for the calibration 4th coarse bit Default Value: 7

## 2.1.12 BLE\_BLERD\_CFG\_3\_FCAL

FCAL running configure 3\_4

Address: 0x402E0034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_F RAMES_3	COARSE_FRAMES_2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_3 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_3	numbere of frames to run for the calibration 3rd coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_2	numbere of frames to run for the calibration 2nd coarse bit Default Value: 7

## 2.1.13 BLE\_BLERD\_CFG\_4\_FCAL

FCAL running configure 0\_1

Address: 0x402E0038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_FRAMES_1	COARSE_FRAMES_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_1 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_1	numbere of frames to run for the calibration 1st coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_0	numbere of frames to run for the calibration 0th coarse bit Default Value: 7

## 2.1.14 BLE\_BLERD\_CFG\_5\_FCAL

FCAL running framer fine

Address: 0x402E003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	CNT_SEL	FINE_FRAMES [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					CNT_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 7	CNT_SEL	select which count should be reflected in the FCAL_DBG_2 and FCAL_DBG_3 registers 4d1: FCAL 7th Coarse bit calibration 4d2: FCAL 6th Coarse bit calibration 4d3: FCAL 5th Coarse bit calibration 4d4: FCAL 4th Coarse bit calibration 4d5: FCAL 3rd Coarse bit calibration 4d6: FCAL 2nd Coarse bit calibration 4d7: FCAL 1st Coarse bit calibration 4d8: FCAL 0th Coarse bit calibration 4d9: FCAL 3rd Fine bit calibration 4d10: FCAL 2nd Fine bit calibration 4d11: FCAL 1st Fine bit calibration 4d12: FCAL 0th Fine bit calibration 4d13: VCO Open loop count 4d14: KVCAL Observed Count 4d15: KVCAL Gain Default: Gives zero output Default Value: 15
6 : 0	FINE_FRAMES	numbere of frames to run for all the calibration of all the Fine bits Default Value: 14

## 2.1.15 BLE\_BLERD\_CFG\_6\_FCAL

FCAL running VCO OL

Address: 0x402E0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FRAMES_VCO_OL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW		RW	RW	RW		
HW Access	None	R		R	R	R		
Name	None	DRIFT_CHECK [14:13]		DRIFT_CHECK_EN	VCO_OL_ENBL	FRAMES_VCO_OL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 13	DRIFT_CHECK	00: start drift check when the TX driver is powered up 01: start drift check measurement 100us after TX driver is power ed up 10: start drift check measurement 200us after the TX driver is powered up 11: start drift check measurement 300us after the TX drive is powered up Default Value: 0
12	DRIFT_CHECK_EN	enables the FCAL drift check, This needs to be set prior to the TX burst being programmed as it affects the timing sequence. Ensure that FB buffer has not been powered down such that the FCAL counter is left alive. This requires a cahgne to reg0xcc[5] to be set to 0 (disable FB buffer power save). This needs to be set piror to placing the part in TX mode Default Value: 0
11	VCO_OL_ENBL	1:enable vco openloop characterization Default Value: 0
10 : 0	FRAMES_VCO_OL	Number of frames to run in VCO openloop Characterization . If bit[12] fcaldrift_check_en is asserted, then this field indicates for how many frames the FCAL drift has to be measured Default Value: 512



## 2.1.16 BLE\_BLERD\_FCAL\_TEST

FCAL test mode configuration

Address: 0x402E0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COARSE [7:4]				FINE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	LOOP_POLARITY	CNT_POLARITY	MODE	COARSE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	LOOP_POLARITY	1: Inverts the polarity of the FCAL loop. In this mode the DCAP code is decreased if observed count is greater than target count. 0: This is normal FCAL loop, where DCAP code is increased if the observed count is greater than target_count Default Value: 0
13	CNT_POLARITY	1: Inverts the polarity of the FCAL counter output coming in to the RFCTRL Default Value: 0
12	MODE	force the coarse and fine bits of FCAL output enable, high active Default Value: 0
11 : 4	COARSE	force coarse bits output of the FCAL engine when test_mode is set Default Value: 0
3 : 0	FINE	force fine bits output of the FCAL engine when test_mode is set Default Value: 0

## 2.1.17 BLE\_BLERD\_TEST

RCCAL and procmon test configuration

Address: 0x402E0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	KVCAL_MODE	KVCAL_GAIN [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW				
HW Access	None	R	R	R				
Name	None	FRCCAL_POLARITY	FRCCAL_MODE	FRCCAL_CODE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	FRCCAL_POLARITY	1: invert RC CAL polarity. Default Value: 0
13	FRCCAL_MODE	1: RC-CAL code is forced to the given code Default Value: 0
12 : 8	FRCCAL_CODE	this code is forced as the RC_CAL code when test_frccal_mode = 1 Default Value: 0
7	KVCAL_MODE	1: KV-CAL code is forced to the given code Default Value: 0
6 : 0	KVCAL_GAIN	this code is forced as the KV_CAL code when when test_kvcal_mode = 1 Default Value: 0

## 2.1.18 BLE\_BLERD\_FPD\_TEST

LDOs test

Address: 0x402E004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW	RW	RW	None	RW
HW Access	R	None		R	R	R	None	R
Name	FAST_CHARGE	None [6:5]		BB_RCCAL_BLOCK	BB_XO_BUF_SY	BB_XO_BUF_ADC	None	BB_FPUP_XO_BUF_ALL

  

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [15:14]		FPUP_ALL	BALUN_CTUNE	BALUN_HFLDO	SY_LDOFFFB	SY_LDOLOPATH	SY_LDOVCO

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13	FPUP_ALL	1: This is used to force powerup the blocks controlled by this register. Fpd has higher precedence over force_powerup if cfgctrl_testmode_en = 1 Default Value: 0
12	BALUN_CTUNE	1: force powerdown Balun Ctune block if cfgctrl_testmode_en = 1 Default Value: 0
11	BALUN_HFLDO	1: Balun HF LDO is forced power down if cfgctrl_testmode_en = 1 Default Value: 0
10	SY_LDOFFFB	1: force power down SY LDO LOFFFB if cfgctrl_testmode_en = 1 Default Value: 0
9	SY_LDOLOPATH	1: force power down SY LDO LOPATH if cfgctrl_testmode_en = 1 Default Value: 0
8	SY_LDOVCO	1: force power down SY LDOVCO if cfgctrl_testmode_en = 1 Default Value: 0

## 2.1.18 BLE\_BLERD\_FPD\_TEST (continued)

7	FAST_CHARGE	1: force power the fast charge bit for LDO Lopath if cfgctrl_testmode_en = 1 Default Value: 0
4	BB_RCCAL_BLOCK	1: forcefully powers down the RC CAL block if cfgctrl_testmode_en = 1 Default Value: 0
3	BB_XO_BUF_SY	1: forcefully powers down xo buffer to synth if cfgctrl_testmode_en = 1 Default Value: 0
2	BB_XO_BUF_ADC	1: forcefully powers down xo buffer to ADC if cfgctrl_testmode_en = 1 Default Value: 0
0	BB_FPUP_XO_BUF_ALL	1: forcefully powers down all the buffers in XO if cfgctrl_testmode_en = 1 Default Value: 0

## 2.1.19 BLE\_BLERD\_SY

SY test configuration 1

Address: 0x402E0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	RW
HW Access	R	R	R	R	None	R	R	R
Name	TEST_FPD_FCAL	TEST_FPD_DIVN	TEST_FPD_DIV2_BUF	TEST_FPD_LOPATHDIVN	None	TEST_FPD_DIV2	TEST_FPD_VCO	TEST_FPD_IBIAS

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST_FPU_P_ALL	TEST_FPD_LOOP_FREEZE	TEST_FPD_OPENLOOP	TEST_FPD_FCAL_AMP	TEST_FPD_TX_POWERSAVE	TEST_FPD_DIV2_DRV	TEST_FPD_LOPATHTX	TEST_FPD_CPLPF

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	TEST_FPU_P_ALL	1: all the blocks in SY are forced power up if cfgctrl_testmode_en = 1 Default Value: 0
14	TEST_FPD_LOOP_FREEZE	1: loop freeze is forced low if cfgctrl_testmode_en = 1 Default Value: 0
13	TEST_FPD_OPENLOOP	The loop_freeze is forced low if this bit is asserted and cfgctrl_testmode_en = 1 Default Value: 0
12	TEST_FPD_FCAL_AMP	The fcal amp is forced powered down, if this bit is asserted and cfgctrl_testmode_en = 1 Default Value: 0
11	TEST_FPD_TX_POWER_SAVE	The fcal amp is forced powered down, if this bit is asserted and cfgctrl_testmode_en = 1 Default Value: 0
10	TEST_FPD_DIV2_DRV	the TX powersave bit si force to zero if this bit is asserted and and cfgctrl_testmode_en = 1 Default Value: 0

## 2.1.19 BLE\_BLERD\_SY (continued)

9	TEST_FPD_LOPATHTX	SY LOPATH TX buffer is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
8	TEST_FPD_CPLPF	SY CP and LPF are forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
7	TEST_FPD_FCAL	SY FCAL counter is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
6	TEST_FPD_DIVN	SY DIVN block is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
5	TEST_FPD_DIV2_BUF	SY LOPATH FCAL buffer is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
4	TEST_FPD_LOPATHDIVN	SY LOPATH DIVN buffer is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
2	TEST_FPD_DIV2	SY high speed divider block is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
1	TEST_FPD_VCO	SY VCO block is forced powered down, if this bit is set and RF_TST_EN = 1 Default Value: 0
0	TEST_FPD_IBIAS	SY IBIAS block is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0

## 2.1.20 BLE\_BLERD\_TEST2\_SY

SY test configuration 2

Address: 0x402E0054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW			
HW Access	R	R	R	None	R			
Name	FORCE_DS M_FRAC	FORCE_DS M_RUN	FPD_DSM_ RUN	None	ICP_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DSM_FRAC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	DSM_FRAC	fore bits for DSM fractional bits if test2_sy_force_dsm_frac=1 Default Value: 0
7	FORCE_DSM_FRAC	1: Force the MSB 8bit of the DSM fractional part with Reg[15-8]. The LSB bits should be 0. 0: DSM fractional bits will be driven by Timing Engine Default Value: 0
6	FORCE_DSM_RUN	DSM_run signal is asserted if this bit is set and rfcrtl_testmode_en = 1 Default Value: 0
5	FPD_DSM_RUN	DSM run signal is de-asserted if this bit si set and rfcrtl_testmode_en = 1 Default Value: 0
3 : 0	ICP_CODE	ICP code will be programmed with these bits. Default Value: 0

## 2.1.21 BLE\_BLERD\_TX

transmit test configuration

Address: 0x402E0058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST_FPD_KVM_PFD_EV	TEST_FPD_KVM_NFD_EV	TEST_FPD_FN_TXEN	TEST_FPD_PREDRIVER	TEST_FPD_DRIVER	TEST_FPD_LPF	TEST_FPD_DAC	TEST_FPD_IBIAS

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TEST_FPU_P_TX_ALL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TEST_FPU_P_TX_ALL	force powerup all the TX blocks if rfctrl_testmode_en = 1 Default Value: 0
7	TEST_FPD_KVM_PFDDEV	modulator will not enable positive 1Mhz frequency deviation mode, if this bit is set and rfctrl_testmdoe_en = 1 Default Value: 0
6	TEST_FPD_KVM_NFDEV	modulator will not enable negative 1Mhz frequency deviation mode, if this bit is set and rfctrl_testmdoe_en = 1 Default Value: 0
5	TEST_FPD_FN_TXEN	the modulator control signal f_n_txen is deasserted, if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
4	TEST_FPD_PREDRIVER	1: forced power down TX pre-drive if rfctrl_testmode_en = 1 Default Value: 0
3	TEST_FPD_DRIVER	1: forced power down TX driver if rfctrl_testmode_en = 1 Default Value: 0



### 2.1.21 BLE\_BLERD\_TX (continued)

2	TEST_FPD_LPF	1: forced power down TX LPF if rfctrl_testmode_en = 1 Default Value: 0
1	TEST_FPD_DAC	1: forced power down TX DAC if rfctrl_testmode_en = 1 Default Value: 0
0	TEST_FPD_IBIAS	1: forced power down TX ibias if rfctrl_testmode_en = 1 Default Value: 0

## 2.1.22 BLE\_BLERD\_RX

RX test configuration

Address: 0x402E005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST_FPD_MIXER_LO	TEST_FPD_TIA	TEST_FPD_BPF	TEST_FPD_ADC_QREFGEN	TEST_FPD_ADC_QCORE	TEST_FPD_ADC_IREFGEN	TEST_FPD_ADC_ICORE	TEST_FPD_IBIAS

  

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			TEST_FPU_P_RX_ALL	TEST_FPD_FN_RXEN	TEST_FPD_LNA_HIZ	TEST_FPD_LNA	TEST_FPD_MIXER_RF

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	TEST_FPU_P_RX_ALL	1:force powerup all RX blocks,if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
11	TEST_FPD_FN_RXEN	1:the demodulator control signal f_n_rxen is deasserted if this bit is set and rfctrl_testmode_en=1 Default Value: 0
10	TEST_FPD_LNA_HIZ	1:LNA HIZ signal is deasserted, if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
9	TEST_FPD_LNA	1: force power down RX LNA if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
8	TEST_FPD_MIXER_RF	1: force power down RX MIXER RF block if rfctrl_testmode_en = 1. Default Value: 0
7	TEST_FPD_MIXER_LO	1:force power down RX MIXER LO block if this bit is set and rfctrl_testmode_en = 1 Default Value: 0

## 2.1.22 BLE\_BLERD\_RX (continued)

6	TEST_FPD_TIA	1:force power down RX TIA if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
5	TEST_FPD_BPF	1:force power down RX BPF, if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
4	TEST_FPD_ADC_QREFG EN	1:force power donw RX ADC QREF generation lock,if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
3	TEST_FPD_ADC_QCOR E	1:force power down RX ADC Q Core block is force powerdown if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
2	TEST_FPD_ADC_IREFG EN	1:force power donw RX ADC IREF generation lock,if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
1	TEST_FPD_ADC_ICORE	1:force power down RX ADC I Core block is force powerdown if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
0	TEST_FPD_IBIAS	1:force power down RX IBIAS block if this bit is set and rfctrl_testmode_en = 1 Default Value: 0

## 2.1.23 BLE\_BLERD\_DIAG1

RF diagnostics configuration 1

Address: 0x402E0060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	SEL [7:5]			CODE [4:1]				DISABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits      Name      Description

## 2.1.23 BLE\_BLERD\_DIAG1 (continued)

9 : 5	SEL	<p>This needs to be decoded and given to HardIP</p> <p>5'd31 Injection_Monitor</p> <p>5'd30 SY_PDCPLPF</p> <p>5'd29 SY_DIVN_FCAL</p> <p>5'd28 Reserved</p> <p>5'd27 SY LO Path</p> <p>5'd26 SY IBIAS</p> <p>5'd25 SY LDO FFFB</p> <p>5'd24 Reserved</p> <p>5'd23 SY LDO Lopath</p> <p>5'd22 TX Driver</p> <p>5'd21 reserved</p> <p>5'd20 TX LPF</p> <p>5'd19 TX DAC</p> <p>5'd18 TX IBIAS</p> <p>5'd17 RX LNA</p> <p>5'd16 RX Mixer</p> <p>5'd15 RX TIA</p> <p>5'd14 RX CBPF1</p> <p>5'd13 RX CBPF2</p> <p>5'd12 RX ADC</p> <p>5'd11 RX IBIAS</p> <p>5'd10 BB XO</p> <p>5'd9 BB Refcore</p> <p>5'd8 BB RCCAL</p> <p>5'd7 BB LFLDO</p> <p>5'd6 BB BGAP</p> <p>5'd5 BB_V2I</p> <p>5'd4 BB_V2ILDO</p> <p>5'd3 BB_LSLDO</p> <p>5'd2 BB_TRANCHAR</p> <p>5'd1 Balun</p> <p>5'd0 HFLDO</p> <p>Default Value: 0</p>
4 : 1	CODE	<p>global diagnostic code, this is given to all the blocks. The block which has the diagnostics enabled will decode this code</p> <p>Default Value: 0</p>
0	DISABLE	<p>1: diagnostics fro all blocks are disabled</p> <p>0: diagnostics are enabled an global level. The diagnostics for each block is controlled by as corresponding block level diag_enable signal</p> <p>Default Value: 1</p>

## 2.1.24 BLE\_BLERD\_IM

inject monitor configuration

Address: 0x402E0064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW				RW
HW Access	R		R	R				R
Name	DIAG_INJ_CODE [7:6]		DIAG_INJ_DISABLE	DIAG_MONI_CODE [4:1]				DIAG_MON_DISABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW				RW	RW	
HW Access	R	R				R	R	
Name	DIAG_RESV	DIAG_BUMP [14:11]				DIAG_LOOPBACK	DIAG_INJ_CODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	DIAG_RESV	reserved for feature Default Value: 0
14 : 11	DIAG_BUMP	diag bump code im_diag_bump[3:2] 2'b00: Mon OTA ref. voltage is 0.9V 2'b01: Mon OTA ref. voltage is 1.0V 2'b10: Mon OTA ref. voltage is 1.1V 2'b11: Mon OTA ref. voltage is 0.8V im_diag_bump[1:0] 2'b00: Inj OTA ref. voltage is 0.9V 2'b01: Inj OTA ref. voltage is 1.0V 2'b10: Inj OTA ref. voltage is 1.1V 2'b11: Inj OTA ref. voltage is 0.8V Default Value: 0
10	DIAG_LOOPBACK	1: This will be used to monitor various outputs in the chip and inject them to on-chip ADC 0: no monitor to injection loopback Default Value: 0

## 2.1.24 BLE\_BLERD\_IM (continued)

9 : 6	DIAG_INJ_CODE	<p>injection code. This determines for which block is the injection enabled</p> <p>Code:    inj_p                  inj_n</p> <p>4h1:    vin_lpf                  unused</p> <p>4d 4    I TIA in_p                I TIA in_n</p> <p>4d 5    Q TIA in_p                Q TIA in_n</p> <p>4d 6    I TIA in_p                Q TIA in_n</p> <p>4d 7    Q TIA in_p                I TIA in_n</p> <p>4d 8    I ADC in_p                I ADC in_n</p> <p>4d 9    Q ADC in_p                Q ADC in_n</p> <p>4h0, 4d2, 4d10, 4d11, 4d12, 4d13, 4d14, 4d15 are unused</p> <p>Default Value: 0</p>
5	DIAG_INJ_DISABLE	<p>1:globally disable the injection</p> <p>Default Value: 1</p>
4 : 1	DIAG_MONI_CODE	<p>monitor code, this determine from lock the monitor is being driven</p> <p>Code    moni_p                  moni_n</p> <p>4d 1    dac_outp                  gnd</p> <p>4d 2    lpf_out                   gnd</p> <p>4d 4    I TIA out_p                I TIA out_n</p> <p>4d 5    Q TIA out_p                Q TIA out_n</p> <p>4d 6    I CBPF out_p               I CBPF out_n</p> <p>4d 7    Q CBPF out_p               Q CBPF out_n</p> <p>4d 8    I CBPF out_p               Q CBPF out_n</p> <p>4d 9    Q CBPF out_p               I CBPF out_n</p> <p>4d0, 4d10, 4d11, 4d12, 4d13, 4d14, 4d15: unused</p> <p>Default Value: 0</p>
0	DIAG_MON_DISABLE	<p>1:globally disable the monitor</p> <p>Default Value: 1</p>

## 2.1.25 BLE\_BLERD\_LDO\_BYPASS

LDOs bypass configuration

Address: 0x402E0068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW	RW	RW	RW
HW Access	R				R	R	R	R
Name	RESV_LDOBP [7:4]				HFLDO	SYL-DOFFFB	SYLDOLO-PATH	SYLDOV-CO

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RESV_LDOBP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 4	RESV_LDOBP	reserved for feature Default Value: 0
3	HFLDO	1: BB SY HF LDO is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0
2	SYLDOFFFB	1: Synth LDO_FFFB is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0
1	SYLDOLOPATH	1: Synth LDO_LOPATH is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0
0	SYLDOVCO	1: Synth LDO_VCO is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0



## 2.1.26 BLE\_BLERD\_LDO

bump bit for LDOs Atlantis

Address: 0x402E006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW		RW		
HW Access	R	R		R		R		
Name	BUMP_SY_LHV	BUMP_SY_LOPATH [6:5]		BUMP_SY_VCO [4:3]		BUMP_BALUM_HF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	REV_LDO [15:12]				BUMP_SY_FFFB [11:9]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	REV_LDO	received for feature Default Value: 0
11 : 9	BUMP_SY_FFFB	3d0: FF and FB LDO outputs are 1.800V 3d1: FF and FB LDO outputs are 1.846V 3d2: FF and FB LDO outputs are 1.894V 3d3: FF and FB LDO outputs are 1.946V 3d4: FF and FB LDO outputs are 2.000V 3d5: FF and FB LDO outputs are 1.649V 3d6: FF and FB LDO outputs are 1.701V 3d7: FF and FB LDO outputs are 1.756V Default Value: 0
8 : 7	BUMP_SY_LHV	2d0: HV LDO outputs are 1.894V 2d1: HV LDO outputs are 2.000V 2d2: HV LDO outputs are 1.800V 2d3: HV LDO outputs are 1.846V Default Value: 0

## 2.1.26 BLE\_BLERD\_LDO (continued)

6 : 5	BUMP_SY_LOPATH	2d0: LOPATH LDO outputs are 1.762V 2d1: LOPATH LDO outputs are 1.861V 2d2: LOPATH LDO outputs are 1.673V 2d3: LOPATH LDO outputs are 1.716V Default Value: 0
4 : 3	BUMP_SY_VCO	2d0: VCO LDO outputs are 1.413V 2d1: VCO LDO outputs are 1.494V 2d2: VCO LDO outputs are 1.329V 2d3: VCO LDO outputs are 1.371V Default Value: 0
2 : 0	BUMP_BALUM_HF	3d0: HF LDO output is 1.800V 3d1: HF LDO output is 1.846V 3d2: HF LDO output is 1.894V 3d3: HF LDO output is 1.946V Default Value: 0

## 2.1.27 BLE\_BLERD\_BB\_BUMP1

bump bit for LDOs BB, TXRX

Address: 0x402E0070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	LFLDO [7:5]			V2I_REG [4:2]			REFCORE_VDD [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None	RW		RW		
HW Access	R	R	None	R		R		
Name	FPD_REFO RCE	FORCE_BG STARTUP	None	REV_BBBUMP [12:11]		LSLDO [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	FPD_REFORCE	1: Force Power down for refcore Default Value: 0
14	FORCE_BGSTARTUP	1: force BG start u/p Default Value: 0
12 : 11	REV_BBBUMP	reserved for feature Default Value: 0
10 : 8	LSLDO	3d0: LS LDO output is 1.708V 3d1: LS LDO output is 1.747V 3d2: LS LDO output is 1.802V 3d3: LS LDO output is 1.849V 3d4: LS LDO output is 1.904V 3d5: LS LDO output is 1.552V 3d6: LS LDO output is 1.591V 3d7: LS LDO output is 1.650V Default Value: 0

## 2.1.27 BLE\_BLERD\_BB\_BUMP1 (continued)

7 : 5	LFLDO	<p>3d0: XO LDO output is 1.894V; BB LDO output is 1.800V  3d1: XO LDO output is 1.946V; BB LDO output is 1.846V  3d2: XO LDO output is 2.000V; BB LDO output is 1.894V  3d3: XO LDO output is 2.000V; BB LDO output is 1.946V  3d4: XO LDO output is 1.701V; BB LDO output is 1.649V  3d5: XO LDO output is 1.756V; BB LDO output is 1.649V  3d6: XO LDO output is 1.800V; BB LDO output is 1.701V  3d7: XO LDO output is 1.846V; BB LDO output is 1.756V  Default Value: 0</p>
4 : 2	V2I_REG	<p>Bit[4]  1: Error amp quiescent current is 5u  0: Error amp quiescent current is 10u</p> <p>Bit[3:2]  2d0: V2I LDO output is 1.8V  2d1: V2I LDO output is 1.85V  2d2: V2I LDO output is 1.9V  2d3: V2I LDO output is 1.75V  Default Value: 0</p>
1 : 0	REFCORE_VDD	<p>2d0: Bumps the I<sub>bias</sub> current of Refcore to 10u  2d1: Bumps the I<sub>bias</sub> current of Refcore to 9.1u  2d2: Bumps the I<sub>bias</sub> current of Refcore to 11.1u  2d3: Bumps the I<sub>bias</sub> current of Refcore to 12.5u  Default Value: 0</p>

## 2.1.28 BLE\_BLERD\_BB\_BUMP2

BB bump configuration

Address: 0x402E0074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	V2I [7:5]			V2I_RCAL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	SY_IBIAS [15:13]			VBG_TRIM [12:10]			V2I [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	SY_IBIAS	3'b1xx: RCAL current bumped 3'b0xx: BG current bumped. 2'bx: represent current bump 01: +12.5%, 00: 0%, 11: -12.5%, 10:-25% Default Value: 0
12 : 10	VBG_TRIM	3d0: Trims the Bandgap voltage by 0% 3d1: Trims the Bandgap voltage by 1.6% 3d2: Trims the Bandgap voltage by 3.2% 3d3: Trims the Bandgap voltage by 4.8% 3d4: Trims the Bandgap voltage by 6.4% 3d5: Trims the Bandgap voltage by -4.8% 3d6: Trims the Bandgap voltage by -3.2% 3d7: Trims the Bandgap voltage by -1.6% Default Value: 0

## 2.1.28 BLE\_BLERD\_BB\_BUMP2 (continued)

9 : 5	V2I	<p>Bit[9]</p> <p>1: Error amp quiescent current is 5u</p> <p>0: Error amp quiescent current is 10u</p> <p>Bit[8:5]</p> <p>4d0: Trims the BGR current by 0%</p> <p>4d1: Trims the BGR current by -2.5%</p> <p>4d2: Trims the BGR current by -5%</p> <p>4d3: Trims the BGR current by -7.5%</p> <p>4d4: Trims the BGR current by -10%</p> <p>4d5: Trims the BGR current by -12.5%</p> <p>4d6: Trims the BGR current by -15%</p> <p>4d7: Trims the BGR current by -17.5%</p> <p>4d8: Trims the BGR current by 20%</p> <p>4d9: Trims the BGR current by 17.5%</p> <p>4d10: Trims the BGR current by 15%</p> <p>4d11: Trims the BGR current by 12.5%</p> <p>4d12: Trims the BGR current by 10%</p> <p>4d13: Trims the BGR current by 7.5%</p> <p>4d14: Trims the BGR current by 5%</p> <p>4d15: Trims the BGR current by 2.5%</p> <p>Default Value: 0</p>
4 : 0	V2I_RCAL	<p>Bit[4]</p> <p>1: Error amp quiescent current is 5u</p> <p>0: Error amp quiescent current is 10u</p> <p>Bit[3:0]</p> <p>4d0: Trims the RCAL current by 0%</p> <p>4d1: Trims the RCAL current by -2.5%</p> <p>4d2: Trims the RCAL current by -5%</p> <p>4d3: Trims the RCAL current by -7.5%</p> <p>4d4: Trims the RCAL current by -10%</p> <p>Default Value: 0</p>

## 2.1.29 BLE\_BLERD\_BB\_XO

BB bump configuration 1

Address: 0x402E0078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	CTRL_VDDL_XO	CTRL_RC_FASTSTART_RES [6:5]		EN_AMPDET_FASTSTART	EN_AMPDET_CURMEAS	EN_CURMEAS	EN_RE_FASTSTART	DIS_XOCORE_SUPPLT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	rev_bb_xo	CTRL_RPREF [14:13]		CTRL_VDDL_XB [12:10]			CTRL_VDDL_XO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	rev_bb_xo	reserved for feature Default Value: 0
14 : 13	CTRL_RPREF	Controls the reference voltage fed as input to the regulators which generate vdd_xo and vdd_xb. 2d0 : 1.289V 2d0 : 1.227V 2d0 : 1.164V 2d0 : 1.382V Default Value: 0

## 2.1.29 BLE\_BLERD\_BB\_XO (continued)

12 : 10	CTRL_VDDL_XB	Controls the value of supply filter resistance in the inverter chain. This in turn controls the supply voltage at which the inverter chain runs. 3d0 : 1.028k 3d0 : 1.172k 3d0 : 1.367k 3d0 : 1.540k 3d0 : 1.889k 3d0 : 2.055k 3d0 : 0.503k 3d0 : 0.747k Default Value: 0
9 : 7	CTRL_VDDL_XO	Controls the value of supply filter resistance in the xo core. This in turn controls the supply voltage at which the core runs. 3d0 : 0.769k 3d0 : 0.877k 3d0 : 1.023k 3d0 : 1.152k 3d0 : 1.413k 3d0 : 1.537k 3d0 : 0.376k 3d0 : 0.559k Default Value: 0
6 : 5	CTRL_RC_FASTSTART_RES	Controls the time constant with which the surge current from rc_faststart block decays down to zero. 2d0 : 387us 2d1 : 309us 2d2 : 232us 2d3 : 464us Default Value: 0
4	EN_AMPDET_FASTSTART	This bit is used to force startup of the vtnbyr circuit in the biasgen_and_reg block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
3	EN_AMPDET_CURMEAS	This bit can be used to disable all the caps on both X1 node and X2 node. 1d0 : Caps Enabled 1d1 : Caps disabled. Even when all the caps are disabled, due to finite on/off ratio of the caps, the cap on both X1 and X2 node is still 3.69pF Default Value: 0
2	EN_CURMEAS	This bit is used to force startup of the positive feedback loop in the amplitude detect block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
1	EN_RE_FASTSTART	Enables/Disables the RC faststart block in the XO. When enabled, this block provides a surge current at xo startup to reduce the settling time of the XO. 1: RC Fast start in XO is enabled 0: RC Fast start in XO is disabled Default Value: 0
0	DIS_XOCORE_SUPFILT	Enables/Disables the supply filter of the XO core. 1: Disabled 0: Enabled Default Value: 0



## 2.1.30 BLE\_BLERD\_BB\_XO\_CAPTRIM

BB bump configuration 2

Address: 0x402E007C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	X2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	X1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	X1	Bits 15-8 together control cap on X1 node. Bits 14-8 : Fine Control Value of 14-8 : Cap Value 7d0 : 3.6900pF 7d1 : 3.7911pF 7d2 : 3.8922pF . . . 7d127 : 16.4280pF Bit 15 : Coarse control 1d0 : No additional cap turned on 1d1 : Additional cap of 8.1pF turned on Default Value: 45

## 2.1.30 BLE\_BLERD\_BB\_XO\_CAPTRIM (continued)

7 : 0	X2	<p>Bits 7-0 together control cap on X2 node.</p> <p>Bits 6-0 : Fine Control</p> <p>Value of 6-0 : Cap Value</p> <p>7d0 : 3.6900pF</p> <p>7d1 : 3.7911pF</p> <p>7d2 : 3.8922pF</p> <p>.</p> <p>.</p> <p>.</p> <p>7d127 : 16.4280pF</p> <p>Bit 7 : Coarse control</p> <p>1d0 : No additional cap turned on</p> <p>1d1 : Additional cap of 8.1pF turned on</p> <p>Default Value: 106</p>
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## 2.1.31 BLE\_BLERD\_SY\_BUMP1

SY bump bits configuration 1

Address: 0x402E0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW			
HW Access	R	R		R	R			
Name	LDOLFO RCE_STARTUP	IBIAS_LOPATH [6:5]		LOFB_POWERSAVE	VCO [3:0]			

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDCPLPF [15:12]				LOPATH [11:8]			

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	PDCPLPF	Bump for PD CP and LPF blocks.[2:0] is used to get range of -20%to +15% in 5% steps. ICP_BUMP[2:0] ICP 1 0 0 -20% 1 0 1 -15% 1 1 0 -10% 1 1 1 -05% 0 0 0 00% 0 0 1 05% 0 1 0 10% 0 1 1 15%. Default Value: 0

## 2.1.31 BLE\_BLERD\_SY\_BUMP1 (continued)

11 : 8	LOPATH	<p>Bump bits for LO path bulk bias. Goes to DIVN/FCAL/LOPATH for bumps. 2 bits for pBulk [3:2] and 2 bits for nBulk[1:0].</p> <table> <tr> <th>bump</th><th>pbulk</th><th></th></tr> <tr> <td>0 0</td><td></td><td>vddx-380mV</td></tr> <tr> <td>0 1</td><td></td><td>vddx-320mV</td></tr> <tr> <td>1 0</td><td></td><td>vddx-440mV</td></tr> <tr> <td>1 1</td><td></td><td>vddx</td></tr> </table> <p>Default Value: 5</p>	bump	pbulk		0 0		vddx-380mV	0 1		vddx-320mV	1 0		vddx-440mV	1 1		vddx
bump	pbulk																
0 0		vddx-380mV															
0 1		vddx-320mV															
1 0		vddx-440mV															
1 1		vddx															
7	LDOLO_FORCE_START UP	<p>1: force start-up of the VT/R circuit in VCOLOPATH LCO 0: no force start-up Default Value: 0</p>															
6 : 5	IBIAS_LOPATH	<p>bump bits for clkbias in lopath</p> <table> <tr> <th>bump</th><th>clk bias pM</th><th>clk bias nM</th></tr> <tr> <td>0 0</td><td>vddo-vgsp</td><td>vg sn</td></tr> <tr> <td>0 1</td><td>vddlo-vgsp-100m</td><td>vg sn+100m</td></tr> <tr> <td>1 0</td><td>vddlo-vgsp-200m</td><td>vg sn+200m</td></tr> <tr> <td>1 1</td><td>vddlo-vgsp-400m</td><td>vg sn+400m</td></tr> </table> <p>Default Value: 0</p>	bump	clk bias pM	clk bias nM	0 0	vddo-vgsp	vg sn	0 1	vddlo-vgsp-100m	vg sn+100m	1 0	vddlo-vgsp-200m	vg sn+200m	1 1	vddlo-vgsp-400m	vg sn+400m
bump	clk bias pM	clk bias nM															
0 0	vddo-vgsp	vg sn															
0 1	vddlo-vgsp-100m	vg sn+100m															
1 0	vddlo-vgsp-200m	vg sn+200m															
1 1	vddlo-vgsp-400m	vg sn+400m															
4	LOFB_POWERSAVE	<p>1: enable powersave for LOFB buffer 0: disable powersave for LOFB buffer Default Value: 0</p>															
3 : 0	VCO	<p>Bump bits for SY VCO block.</p> <p>Rt VCO (2 bits) - sy_bump1_vco [3:2] 00 ~ 50 Ohms 01 ~ 30 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms</p> <p>and Rb VCO (2 bits) - sy_bump1_vco[1:0] 00 ~ 58 Ohms 01 ~ 39 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms Default Value: 5</p>															

## 2.1.32 BLE\_BLERD\_SY\_BUMP2

SY bump bits configuration 2

Address: 0x402E0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	ICP_OFFSET [7:6]		ICP_XFACTOR [5:4]		ACAP_BIAS_SEL [3:2]		FCAL_BIAS_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	PDCP_OFFSET [15:14]		RST_DLY [13:12]		VMOD_PUL LDN	VCTRL_PU LLDN	PUP_MON	CLKNC_M ODE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	PDCP_OFFSET	Bump for the bias voltage of the 8x node. sel[1:0] R2 Vbp 00 38.5k 925mV (Default) 01 43.0k 925mV+108mV 10 31.9k 925mV-158mV 11 35.2k 925mV-080mV Default Value: 0
13 : 12	RST_DLY	Bumping the reset (up+down) delay. Code[1:0] delay 00 500ps 01 424ps 10 350ps 11 300ps Default Value: 0
11	VMOD_PULLDN	1: Pull down control for the modulating port Default Value: 0
10	VCTRL_PULLDN	1: Test mode to pull down for noise simulation Default Value: 0

## 2.1.32 BLE\_BLERD\_SY\_BUMP2 (continued)

9	PUP_MON	1: Test mode to monitor buffered 1x output on the injmon buffer Default Value: 0
8	CLKNC_MODE	Control the NC_clock_mux. 0: The NC clock is given from DIVN once openloop is made low. 1: The NC clock is always connected to Crystal clock Default Value: 0
7 : 6	ICP_OFFSET	Bump bits to set the offset pulse width in RX mode Code[1:0] delay 00 2.45n 01 1.75ns 10 1.3ns 11 25ps Default Value: 0
5 : 4	ICP_XFACTOR	sy_bump2_icp_xfactor[1]: enable power save for SY FB buffers in TXPOWERSAVE mode, high active sy_bump2_icp_xfactor[0]: HSDIV2 is put in self oscillation mode, this can be used to find out the process corner of the chip, high active Default Value: 0
3 : 2	ACAP_BIAS_SEL	ACAP bias voltage is selected based on these bits. Code[1:0] acapbias 00 630mV 01 700mV 10 560mV 11 595mV Default Value: 0
1 : 0	FCAL_BIAS_SEL	VCTRL bias voltage is selected based on these bits. Code[1:0] fcal_bias 00 Vddvco/2 01 Vddvco/2 + 5.6%(+100mV) 10 Vddvco/2 - 2.8%(-050mV) 11 Vddvco/2 - 5.6%(-100mV) Default Value: 0

## 2.1.33 BLE\_BLERD\_TX\_BUMP1

transmit bump configuration 1

Address: 0x402E0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	TX_LPF [7:6]		SY_RST_DLY_TX [5:4]		TX_DRIVER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW				RW	
HW Access	R		R				R	
Name	SY_DIVN_TXPOWERSAVE [15:14]		TX_VTXREF_PROG [13:10]				TX_LPF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	SY_DIVN_TXPOWERSAVE	Divn power save bits
		pup freeze txpowersave<1:0> PupBlocks
		0 0 X X NONE
		1 0 X X ALL
		1 1 0 0 ALL
		1 1 0 1 ALL-D2
		1 1 1 0 ALL-D2-D1
		1 1 1 1 ALL-D2-D1-Buf
		Default Value: 3

## 2.1.33 BLE\_BLERD\_TX\_BUMP1 (continued)

13 : 10	TX_VTXREF_PROG	<p>TX Modulation port varactor vtxref bias voltage bump settings</p> <p>0000 Sets vtxref value to 100mV</p> <p>0001 Sets vtxref value to 150mV</p> <p>0010 Sets vtxref value to 200mV</p> <p>0011 Sets vtxref value to 250mV</p> <p>0100 Sets vtxref value to 300mV</p> <p>0101 Sets vtxref value to 350mV</p> <p>0110 Sets vtxref value to 400mV</p> <p>0111 Sets vtxref value to 450mV</p> <p>1000 Sets vtxref value to 500mV</p> <p>1001 Sets vtxref value to 550mV</p> <p>1010 Sets vtxref value to 600mV</p> <p>Default Value: 4</p>
9 : 6	TX_LPF	<p>Bump bits for TX LPF op-amp reference voltage [3:2]</p> <p>00 Bumps the opamp ref voltage to 400mV</p> <p>01 Bumps the opamp ref voltage to 450mV</p> <p>10 Bumps the opamp ref voltage to 300mV</p> <p>11 Bumps the opamp ref voltage to 350mV</p> <p>Bump bits for TX LPF op-amp bias current [1:0]</p> <p>00 Bumps the opamp bias current to 10u</p> <p>01 Bumps the opamp bias current to 12.5u</p> <p>10 Bumps the opamp bias current to 8.3u</p> <p>11 Bumps the opamp bias current to 7.7u</p> <p>Default Value: 0</p>
5 : 4	SY_RST_DLY_TX	<p>Bumping the reset (up+down) delay.</p> <p>Code[1:0] delay</p> <p>00 500ps</p> <p>01 424ps</p> <p>10 350ps</p> <p>11 300ps</p> <p>Default Value: 3</p>
3 : 0	TX_DRIVER	<p>Driver bias current selection bump bit</p> <p>tx_bump1_tx_driver[3] Driver bias current</p> <p>tx_bump1_tx_driver[0] PTAT current selection</p> <p>Additional Class AB driver bias voltage bump related to Tx_bump2_drv_ab_vbias[3:0]</p> <p>Default Value: 0</p>



## 2.1.34 BLE\_BLERD\_TX\_BUMP2

transmit bump configuration 2

Address: 0x402E008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	SY_LDOBGREF_EN [7:6]		DRV_VCASCH [5:4]		DRV_AB_VBIAS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW				RW	
HW Access	R		R				R	
Name	SY_CP_TXPOWERSAVE [15:14]		DAC_RES [13:10]				SY_ICP_OFFSET_TX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	SY_CP_TXPOWERSAVE	Charge pump power save bits pup freeze txpowersave<1:0> PupBlocks 0 0 X X NONE 1 0 X X ALL 1 1 0 0 ALL 1 1 0 1 ALL-8x CP 1 1 1 0 ALL-8x-1x CP 1 1 1 1 ALL-buffer Default Value: 3

## 2.1.34 BLE\_BLERD\_TX\_BUMP2 (continued)

13 : 10	DAC_RES	<p>TX DAC load resistor bump settings</p> <p>0000 DAC output resistor bump by -20%</p> <p>0001 DAC output resistor bump by -17.5%</p> <p>0010 DAC output resistor bump by -15%</p> <p>0011 DAC output resistor bump by -12.5%</p> <p>0100 DAC output resistor bump by -10%</p> <p>0101 DAC output resistor bump by -7.5%</p> <p>0110 DAC output resistor bump by -5%</p> <p>0111 DAC output resistor bump by -2.5%</p> <p>1000 DAC output resistor bump by 0%</p> <p>1001 DAC output resistor bump by 2.5%</p> <p>1010 DAC output resistor bump by 5%</p> <p>1011 DAC output resistor bump by 7.5%</p> <p>1100 DAC output resistor bump by 10%</p> <p>1101 DAC output resistor bump by 12.5%</p> <p>1110 DAC output resistor bump by 15%</p> <p>1111 DAC output resistor bump by 17.5%</p> <p>Default Value: 8</p>
9 : 8	SY_ICP_OFFSET_TX	<p>Bump bits to set the offset pulse width in TX mode</p> <p>Code[1:0] xfactor</p> <p>00 : 2.45ns</p> <p>01 : 1.75ns</p> <p>10 : 1.3ns</p> <p>11 : 25ps</p> <p>Default Value: 3</p>
7 : 6	SY_LDOBGREF_EN	<p>Enables a bandgap (low temp coeff) for the</p> <p>00 None</p> <p>01 VCO Ido</p> <p>10 LOPATH Ido</p> <p>11 VCO+LOPATH Ido</p> <p>Default Value: 0</p>
5 : 4	DRV_VCASCH	<p>Programs the driver cascode gate bias voltage</p> <p>Tx_bump2_drv_vcasch[1:0] Driver cascode bias voltage</p> <p>00 Vdd_driver 0.3V</p> <p>01 Vdd_driver 0.2V</p> <p>10 Vdd_driver 0.1V</p> <p>11 Vdd_driver</p> <p>Default Value: 3</p>

## 2.1.34 BLE\_BLERD\_TX\_BUMP2 (continued)

3 : 0	DRV_AB_VBIAS	Bias voltage for the class-AB driver with tx_bump1_tx_driver[1:0]=00 Tx_bump2_drv_ab_vbias[3:0] Vbias_AB , mV
		0000 571.224
		0001 604.508
		0010 626.357
		0011 641.856
		0100 656.04
		0101 667.096
		0110 678.775
		0111 688.005
		1000 698.817
		1001 707.272
		1010 718.103
		1011 726.411
		1100 737.995
		1101 746.708
		1110 759.919
		1111 769.735
		Default Value: 8

## 2.1.35 BLE\_BLERD\_RX\_BUMP1

receiver bump configuration 1

Address: 0x402E0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	IF_OFFSET_CALDAC [7:6]		CBPF [5:3]			TIA [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	LNA [15:12]				MIXER [11:10]		MIXER_VBIAS_SW [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	LNA	<p>rx_bump1_lna[3] 1: enables the HG and LG LNA section's cascode biases to be alive independent of whether LNA is HG or LG mode. This enables fast transition from LG to HG in AGC events</p> <p>rx_bump1_lna[2] 1: forces pull down of inputs of LNA (post AC coupling) if LNA is powered up in Hi-Z mode to ensure good isolation during DC offset calibration of Receiver chain</p> <p>rx_bump1_lna[1] 1: Boost the LNA bias current of HP equivalent (1.5mA current penalty) if LNA gain is at 101 (66dB setting) and this bit is set. this boosts sensitivity by 2-3dB but the hit in the current consumption is only at 66dB gain setting. so average current consumption in field should not be impacted much but a 2dB boost in sensitivity is seen</p> <p>rx_bump1_lna[0] 1: Forces the TIA to have lower feedback resistor to avoid EVM degradation in the TIA due to complex filter distortion caused by I/Q cross talk if feedback resistors is high in the TIA Default Value: 12</p>

## 2.1.35 BLE\_BLERD\_RX\_BUMP1 (continued)

11 : 10	MIXER	<p>bump bits to control LNA gate bias voltage in RX mode</p> <p>01 0.5V</p> <p>00 0.4V</p> <p>11 0.3V</p> <p>10 0.2V</p> <p>Default Value: 2</p>
9 : 8	MIXER_VBIAS_SW	<p>Bump bits for Mixer VBIAS switch</p> <p>Mixer Bias Programmability</p> <p>01 TIA CM + 0.38V</p> <p>00 TIA CM + 0.3V</p> <p>11 TIA CM + 0.255V</p> <p>10 TIA CM + 0.17V</p> <p>Default Value: 2</p>
7 : 6	IF_OFFSET_CALDAC	<p>Bit Setting Offset DAC LSB</p> <p>00 132.4nA</p> <p>01 150.8nA</p> <p>10 118.0nA</p> <p>11 106.5nA</p> <p>Default Value: 0</p>
5 : 3	CBPF	<p>2'b0xx: CBPF CM ref voltage 850mV and 1V for 1st stage and 2nd stage resp. for irefbg 8.5uA.</p> <p>2'b1xx: CBPF CM ref voltage 850mV and 1V for 1st stage and 2nd stage resp. for irefbg 10uA.</p> <p>2'bx0: CBPF OTA1 CMFB tail current 17.27uA (Bias current 8.5uA).</p> <p>2'bx1: CBPF OTA1 CMFB tail current 21.58uA (Bias current 8.5uA).</p> <p>2'bx0x: CBPF OTA2 CMFB tail current 17.27uA (Bias current 8.5uA).</p> <p>2'bx1x: CBPF OTA2 CMFB tail current 21.58uA (Bias current 8.5uA).</p> <p>Default Value: 0</p>
2 : 0	TIA	<p>2'b0xx: TIA CM ref voltage 850mV for iref bias current 8.5uA.</p> <p>2'b1xx: TIA CM ref voltage 850mV for iref bias current 10uA.</p> <p>2'bx00: TIA OTA CMFB tail current 69uA (Bias current 8.5uA).</p> <p>2'bx01: TIA OTA CMFB tail current 78uA (Bias current 8.5uA).</p> <p>2'bx10: TIA OTA CMFB tail current 86uA (Bias current 8.5uA).</p> <p>2'bx11: TIA OTA CMFB tail current 95uA (Bias current 8.5uA).</p> <p>Default Value: 0</p>

## 2.1.36 BLE\_BLERD\_RX\_BUMP2

receiver bump configuration 2

Address: 0x402E0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IF_CM_IBIAS [7:6]		CBPF_IBIAS [5:4]		TIA_IBIAS [3:2]		LNA_IBIAS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	RW	RW	RW
HW Access	R		R	R	R	R	R	R
Name	REV_RX_BUMP2 [15:14]		SY_LOWKV MMODE	SY_LOWKV AMODE	SY_HILINE ARITYR2_ MODE	SY_R2HIG HMODE	COMPLEX_ DISABLE	CBPF_HIZ_ ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	REV_RX_BUMP2	reserved for feature Default Value: 0
13	SY_LOWKVMMODE	Enables a lower Kv/2 mode 0 10 MHz/V 1 5 MHz/V Default Value: 0
12	SY_LOWKVAMODE	Enables a lower Kv/2 mode 0 70 MHz/V 1 45 MHz/V Default Value: 0
11	SY_HILINEARITYR2_MODE	Switches the RX mode between settings used in TX vs a higher linearity setting. 0 Use same as TX 1 Use alternative bias for RX. Effective only in RX mode. This is don't care in TX mode Default Value: 1

## 2.1.36 BLE\_BLERD\_RX\_BUMP2 (continued)

10	SY_R2HIGHMODE	Enables a higher R2 mode for loop stabilization with low Kv and debug mode. 0 40 kohms 1 60 kohms Default Value: 0
9	COMPLEX_DISABLE	setting this bit to disables the complex operation for the band pass filter configuring it as two low pass filters Default Value: 0
8	CBPF_HIZ_ENABLE	Setting this bit to 1 configures the CBPF output as hi-Z enabling independent ADC testing with the injection system Default Value: 0
7 : 6	IF_CM_IBIAS	Bump bits for Common mode setting currents of the TIA and the CBPF amplifiers (Default is 11 for current saving). 01 IBias+15% 00 IBias+0% 11 IBias-15% (Default) 10 IBias-20% Default Value: 3
5 : 4	CBPF_IBIAS	Bump bits for BGR bias currents of Offset Calibration DAC (Default is 00) 01 IBias+15% 00 IBias_0% (Default) 11 IBias-15% 10 IBias-20% Default Value: 0
3 : 2	TIA_IBIAS	Bump bits for RCAL bias currents of the TIA and the CBPF amplifiers (Default is 11 for current saving). 01 IBias+15% 00 IBias+0% 11 IBias-15% (Default) 10 IBias-20% Default Value: 3
1 : 0	LNA_IBIAS	Bump bits for PTAT bias currents of LNA (Default is 00). Play with these to enable Low Power and Ultra Low Power modes in the LNA. 01 IBias+15% 00 IBias+0% (Default) 11 IBias-25% 10 IBias-50% Default Value: 2

## 2.1.37 BLE\_BLERD\_ADC\_BUMP1

ADC1 bump configuration

Address: 0x402E0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	IBG_CAL [7:6]		Q_REF [5:3]			I_REF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	RW		RW
HW Access	R		R	R	R	R		R
Name	BWCTRL [15:14]		OPAMP_BY PASS	LOWPOW- ER	LOOPDLY4 X_EN	LOOPDLY [10:9]		IBG_CAL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	BWCTRL	Reference generators bandwidth boost by injecting current in the output arm. Injection Current : 00 0 A 01 20 A 10 40 A 11 60 A Default Value: 0
13	OPAMP_BYPASS	Bypass op-amp and diode connect reference generator's servo loop 0 Op-amp enabled 1 Op-amp bypassed Default Value: 0
12	LOWPOWER	rCurrent reduction mode in the reference generator. 0 No bump 1 50% bump Default Value: 0



## 2.1.37 BLE\_BLERD\_ADC\_BUMP1 (continued)

11	LOOPDLY4X_EN	<p>Loop delay increment by 4x in SAR return path</p> <p>0 Delay determined by loopdly[1:0]</p> <p>1 4x the delay dictated by the said bit</p> <p>Default Value: 0</p>
10 : 9	LOOPDLY	<p>Loop delay control in SAR return path.</p> <p>00 Min delay</p> <p>11 Max delay</p> <p>Default Value: 0</p>
8 : 6	IBG_CAL	<p>Bump bits for the preamps bias current.</p> <p>X00 + 0 % ( I<sub>bias</sub> - 0 A)</p> <p>X01 +25 % ( I<sub>bias</sub> - 12.5 A)</p> <p>X10 - 50 % ( I<sub>bias</sub> - 5 A)</p> <p>X11 - 25 % ( I<sub>bias</sub> - 7.5 A)</p> <p>Default Value: 0</p>
5 : 3	Q_REF	<p>Bump bits for the channel-Q reference voltage. (2s complement interpretation) Every bit changes the reference voltage by 10mV.</p> <p>100 610 mV</p> <p>000 650 mV</p> <p>011 680 mV</p> <p>Default Value: 4</p>
2 : 0	I_REF	<p>Bump bits for the channel-I reference voltage. (2s complement interpretation) Every bit changes the reference voltage by 10mV. See the above table</p> <p>Default Value: 4</p>

## 2.1.38 BLE\_BLERD\_ADC\_BUMP2

ADC 2 bump configuration

Address: 0x402E009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SHORT_IN PUT	PREAMP_ GAINCTRL _N	PREAMP_S OURCECT RL_N	IBUMP	METADET_ EN	DUTCYCLE _25	CYCLE_B5 _DELAY	CYCLE_B2 _DELAY

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW	RW		
HW Access	R		R		R	R		
Name	REV_ADC_BUMP2 [15:14]		PREAMP_BWCTRL [13:12]		IQSWAP	RETURN_SKEW [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	REV_ADC_BUMP2	[1] -- not used [0] Enable clean Vdd for the cascodes & op-amp in refgen. The clean Vdd supplied through the diag. ( Diag code = 0101 for channel I and Diag code =1101 for channel Q). Default connection to the internal Vdd Default Value: 0
13 : 12	PREAMP_BWCTRL	Bandwidth bump bits for the preamp. Each bit connects a 5fF cap to the output nodes. No cap is connected by default Default Value: 0
11	IQSWAP	Swaps the I and Q channel Vbg/R for ref.gen 0 No swap 1 Enable swapping Default Value: 0
10 : 8	RETURN_SKEW	Delaying the sampling clock from the comparator wrt to the data. 000 Min delay 111 Max delay Default Value: 0

## 2.1.38 BLE\_BLERD\_ADC\_BUMP2 (continued)

7	SHORT_INPUT	Put the ADC in idle channel mode. Inputs are shorted to locally generated 1V signal. 0 Normal operation 1 Idle channel mode Default Value: 0
6	PREAMP_GAINCTRL_N	Enable preamps low/high gain modes over conversion cycle. 0 Functionality enabled 1 Functionality disabled Default Value: 0
5	PREAMP_SOURCECTRL_N	Disconnect source coupled node of the preamp during track phase. 0 Functionality enabled 1 Functionality disabled Default Value: 0
4	IBUMP	0: 6dB attenuation in CBPF gain only at lowest gain setting to improve the Max signal level the receiver can tolerate Note: in order to share the tub width with AGC disabled, this back off mode is effective only with AGC profile set to rev** mode. This is in reg0xa4[3] which needs to be set to '0' for rev** profile Default Value: 0
3	METADET_EN	Enable meta detection Default Value: 0
2	DUTCYCLE_25	Clock duty cycle control 0 50 % time for track phase & 50 % time for convert phase 1 25 % time for track phase & 75 % time for convert phase Default Value: 1
1	CYCLE_B5_DELAY	Enable redundant conversion cycle at b5 position. 0 Disabled 1 Enabled Default Value: 0
0	CYCLE_B2_DELAY	Enable redundant conversion cycle at b2 position. 0 Enabled 1 Disabled Default Value: 0

## 2.1.39 BLE\_BLERD\_BALUN

BALUN bump configuration

Address: 0x402E00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUMP_TX_CTUNE [7:4]				BUMP_RX_CTUNE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW		RW		
HW Access	R			R		R		
Name	REV_BALUN [15:13]			BUMP_RTUNE [12:11]		BUMP_VTUNE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	REV_BALUN	resereved for feature Default Value: 0
12 : 11	BUMP_RTUNE	resereved for feature Default Value: 0
10 : 8	BUMP_VTUNE	resereved for feature Default Value: 0

## 2.1.39 BLE\_BLERD\_BALUN (continued)

7 : 4	BUMP_TX_CTUNE	<div>Programmable bits to change tuning capacitance in the Balun primary side in TX operation</div> <div>Balun_bump_tx_ctune[3:0] Ctune, fF</div> <table><tr><td>0000</td><td>42.5</td></tr><tr><td>0001</td><td>48.8</td></tr><tr><td>0010</td><td>55.1</td></tr><tr><td>0011</td><td>61.4</td></tr><tr><td>0100</td><td>67.7</td></tr><tr><td>0101</td><td>74</td></tr><tr><td>0110</td><td>80.3</td></tr><tr><td>0111</td><td>86.6</td></tr><tr><td>1000</td><td>92.9</td></tr><tr><td>1001</td><td>99.2</td></tr><tr><td>1010</td><td>105.5</td></tr><tr><td>1011</td><td>111.8</td></tr><tr><td>1100</td><td>118.1</td></tr><tr><td>1101</td><td>124.4</td></tr><tr><td>1110</td><td>130.7</td></tr><tr><td>1111</td><td>137</td></tr></table> <div>Default Value: 0</div>	0000	42.5	0001	48.8	0010	55.1	0011	61.4	0100	67.7	0101	74	0110	80.3	0111	86.6	1000	92.9	1001	99.2	1010	105.5	1011	111.8	1100	118.1	1101	124.4	1110	130.7	1111	137
0000	42.5																																	
0001	48.8																																	
0010	55.1																																	
0011	61.4																																	
0100	67.7																																	
0101	74																																	
0110	80.3																																	
0111	86.6																																	
1000	92.9																																	
1001	99.2																																	
1010	105.5																																	
1011	111.8																																	
1100	118.1																																	
1101	124.4																																	
1110	130.7																																	
1111	137																																	
3 : 0	BUMP_RX_CTUNE	<div>Programmable bits to change tuning capacitance in the Balun primary side in RX operation</div> <div>Balun_bump_tx_ctune[3:0] Ctune, fF</div> <table><tr><td>0000</td><td>42.5</td></tr><tr><td>0001</td><td>48.8</td></tr><tr><td>0010</td><td>55.1</td></tr><tr><td>0011</td><td>61.4</td></tr><tr><td>0100</td><td>67.7</td></tr><tr><td>0101</td><td>74</td></tr><tr><td>0110</td><td>80.3</td></tr><tr><td>0111</td><td>86.6</td></tr><tr><td>1000</td><td>92.9</td></tr><tr><td>1001</td><td>99.2</td></tr><tr><td>1010</td><td>105.5</td></tr><tr><td>1011</td><td>111.8</td></tr><tr><td>1100</td><td>118.1</td></tr><tr><td>1101</td><td>124.4</td></tr><tr><td>1110</td><td>130.7</td></tr><tr><td>1111</td><td>137</td></tr></table> <div>Default Value: 3</div>	0000	42.5	0001	48.8	0010	55.1	0011	61.4	0100	67.7	0101	74	0110	80.3	0111	86.6	1000	92.9	1001	99.2	1010	105.5	1011	111.8	1100	118.1	1101	124.4	1110	130.7	1111	137
0000	42.5																																	
0001	48.8																																	
0010	55.1																																	
0011	61.4																																	
0100	67.7																																	
0101	74																																	
0110	80.3																																	
0111	86.6																																	
1000	92.9																																	
1001	99.2																																	
1010	105.5																																	
1011	111.8																																	
1100	118.1																																	
1101	124.4																																	
1110	130.7																																	
1111	137																																	

## 2.1.40 BLE\_BLERD\_CTR1

RFCTRL control timing 1

Address: 0x402E00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW		RW		RW
HW Access	R		R	R		R		R
Name	TX_MODSTART_TIME [7:6]		TX_PREDR V_TIME	TX_FREEZE_TIME [4:3]		PLL_SETTLING_TIME [2:1]		VCO_WAR MUP_TIME

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW		RW	RW
HW Access	R		R	R	R		R	R
Name	AGC_RST_DLY [15:14]		RX_ENV_FREEZE_EN	RX_DC_FREEZE_EN	DBG_SELECT [11:10]		ADC_FULL_SWING_MONI_EN	TX_DF2_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	AGC_RST_DLY	00: 0.25us delay; 01: 1.25us delay, 10: 2.25us delay, 11: 3.25us delay Default Value: 0
13	RX_ENV_FREEZE_EN	demodulation soft reset to frequency tracking enabled, high active Default Value: 1
12	RX_DC_FREEZE_EN	demodulation soft reset to DC cancellation enabled, high active Default Value: 1
11 : 10	DBG_SELECT	00: demod soft reset / AGC reset, 01: AGC FSM MSB and f_n_rxen 10: gain decrease and gain increase. 11: ADC full swing detection and ADC saturation detected signal Default Value: 0
9	ADC_FULL_SWING_MONI_EN	when ctr1_adc_full_swing_moni_en is set and ctr1_dbg_select is 2'b11. ADC full swing detection can be monitored in debug pin Default Value: 0

## 2.1.40 BLE\_BLERD\_CTR1 (continued)

8	TX_DF2_SEL	0: DF2 Max frequency deviation as 224KHz 1: DF2 Max frequency deviation as 242KHz Default Value: 1
7 : 6	TX_MODSTART_TIME	this controls the time between the PUP_TX_DRIVER going high and when f_n_txen is asserted. 00: 0us, 01: 1us, 10: 2us, 11, 3us Default Value: 3
5	TX_PREDRV_TIME	PA predrive pup time, 1:powered up after LDO, 0: powered up after KVCAL Default Value: 0
4 : 3	TX_FREEZE_TIME	tx freeze time 00: 30us, 01: 40us, 10: 50us, 11: 25us Default Value: 0
2 : 1	PLL_SETTLING_TIME	PLL setting time 00: 25us, 01: 30us, 10: 40us, 11:50us Default Value: 0
0	VCO_WARMUP_TIME	vco warm up time, 1: 10us, 0: 5us Default Value: 0

## 2.1.41 BLE\_BLERD\_AGC

AGC timing configuration

Address: 0x402E00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	PWR_MEAS_TIM [7:6]		GAIN_SAT_THRES [5:4]		GAIN_MAP PING_MODE	SAT_CHK_ TIM	CHECK_SA T_EN	RST_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	START_WAIT_TIM [15:13]				GAIN_STABLE_TIM [12:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	START_WAIT_TIM	start AGC waiting time when RFCTRL set AGC enable 1 represents 1us, base 1us Default Value: 1
12 : 8	GAIN_STABLE_TIM	gain stable time after gain assignment. 1 represents one 12Mhz clock Default Value: 5
7 : 6	PWR_MEAS_TIM	AGC power measurement time 11: 1us, 10: 0.75us, 01: 0.5us, 00:0.25us Default Value: 3
5 : 4	GAIN_SAT_THRES	ADC saturated detection threshold for doing a fast transition 00: 0dBm; 01: 1dBm; 10: 2dBm, 11: 3dBm Default Value: 3
3	GAIN_MAPPING_MODE	0: Atlantis TC rev** gain mapping 1: Atlantis TC revA gain mapping Default Value: 1



## 2.1.41 BLE\_BLERD\_AGC (continued)

2	SAT_CHK_TIM	ADC saturated detection timing 0: 3 12MHz clock; 1: 3 12MHz clock; Default Value: 1
1	CHECK_SAT_EN	1: quick check saturated ADC 0: measure ADC power at fixed period Default Value: 1
0	RST_EN	1: AGC soft reset enable Default Value: 1

## 2.1.42 BLE\_BLERD\_THRSHD1

AGC step threshold 1

Address: 0x402E00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC60_66 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC66_60 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC66_60	threshold gain change from 60dB to 48dB Default Value: 60
5 : 0	AGC60_66	threshold gain change from 66dB to 60dB Default Value: 44

## 2.1.43 BLE\_BLERD\_THRSHD2

AGC step threshold 2

Address: 0x402E00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC48_60 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC60_48 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC60_48	threshold gain change from 48dB to 60dB Default Value: 59
5 : 0	AGC48_60	threshold gain change from 60dB to 48dB Default Value: 42

## 2.1.44 BLE\_BLERD\_THRSHD3

AGC step threshold 3

Address: 0x402E00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC36_48 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC48_36 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC48_36	threshold gain change from 366dB to 48dB Default Value: 59
5 : 0	AGC36_48	threshold gain change from 48dB to 36dB Default Value: 44

## 2.1.45 BLE\_BLERD\_THRSHD4

AGC step threshold 4

Address: 0x402E00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC18_36 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC36_18 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC36_18	threshold gain change from 18dB to 36dB Default Value: 60
5 : 0	AGC18_36	threshold gain change from 36dB to 18dB Default Value: 43

## 2.1.46 BLE\_BLERD\_THRSHD5

AGC step threshold 5

Address: 0x402E00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC0_18 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC18_0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC18_0	threshold for gain change from 0dB to 18dB Default Value: 62
5 : 0	AGC0_18	threshold for gain change from 18dB to 0dB Default Value: 38

## 2.1.47 BLE\_BLERD\_DC

ADC I/Q DC compensate value

Address: 0x402E00C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP_Q_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP_I_CODE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	COMP_I_CODE	this code is removed from the ADC Q output. This field can be programmed to remove systematic DC offset Default Value: 0
7 : 0	COMP_Q_CODE	this code is removed from the ADC I output. This field can be programmed to remove systematic DC offset Default Value: 0

## 2.1.48 BLE\_BLERD\_IQMIS

IQ mismatch correction value

Address: 0x402E00C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IQCOMP_QVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IQCOMP_IVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	IQCOMP_IVAL	Q-component of the IQ mismatch correction Default Value: 0
7 : 0	IQCOMP_QVAL	I-component of the IQ mismatch correction Default Value: 0



## 2.1.49 BLE\_BLERD\_DCCAL

DC CAL and setting

Address: 0x402E00C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	TEST_QBITS [7:6]		TEST_IBITS [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	TEST_I_PO LARITY	TEST_Q_P OLARITY	TEST_MOD E	TEST_QBITS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	TEST_I_POLARITY	1: inverts the polarity of DCCAL I code Default Value: 0
13	TEST_Q_POLARITY	1: inverts the polarity of DCCAL Q code Default Value: 0
12	TEST_MODE	enable the DCCAL test mode Default Value: 0
11 : 6	TEST_QBITS	this value is driven to DCCAL Qcode if the DCCA: test mode enabled Default Value: 0
5 : 0	TEST_IBITS	this value is driven to DCCAL Icode if the DCCA: test mode enabled Default Value: 0

## 2.1.50 BLE\_BLERD\_RCCAL

TX LPF and TIA/CBPF RC code

Address: 0x402E00CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	CODE_TX [7:5]			CODE_RX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	None	RW	
HW Access	R		R	R	R	None	R	
Name	AGC_GAIN_INC_TIMES_THRES [15:14]		SOFTTRST_EN_TODIFF	SOFTTRST_EN_TOSTR	SOFTTRST_POWER_DIFF	None	CODE_TX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	AGC_GAIN_INC_TIMES_THRES	AGC gain increase requirement wait times: 00: response for 1st gain increase request 01: response for 2nd gain increase request 10: response for 3rd gain increase request 11: response for 4th gain increase request Default Value: 0
13	SOFTTRST_EN_TODIFF	soft reset is enable to diffdet block Default Value: 0
12	SOFTTRST_EN_TOSTR	soft reset is enabled to STR block Default Value: 1
11	SOFTTRST_POWER_DIFF	soft reset power change detection, 1: 12dB, 0:6dB Default Value: 1
9 : 5	CODE_TX	force RC code for TX LPF under test mode Default Value: 16

## 2.1.50 BLE\_BLERD\_RCCAL (continued)

4 : 0	CODE_RX	force RC code for TIA/CBPF under test mode Default Value: 16
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## 2.1.51 BLE\_BLERD\_DSM1

DSM freeze code 1

Address: 0x402E00D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE2 [7:4]				INDX_CODE3 [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE0 [15:12]				INDX_CODE1 [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE0	index at which DSM code should be freezed when fection value = 0 Default Value: 13
11 : 8	INDX_CODE1	index at which DSM code should be freezed when fection value = 1/24 Default Value: 9
7 : 4	INDX_CODE2	index at which DSM code should be freezed when fection value = 2/24 Default Value: 6
3 : 0	INDX_CODE3	index at which DSM code should be freezed when fection value = 3/24 Default Value: 4

## 2.1.52 BLE\_BLERD\_DSM2

DSM freeze code 2

Address: 0x402E00D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE6 [7:4]				INDX_CODE7 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE4 [15:12]				INDX_CODE5 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE4	index at which DSM code should be freezed when fection value = 4/24 Default Value: 5
11 : 8	INDX_CODE5	index at which DSM code should be freezed when fection value = 5/24 Default Value: 4
7 : 4	INDX_CODE6	index at which DSM code should be freezed when fection value = 6/24 Default Value: 12
3 : 0	INDX_CODE7	index at which DSM code should be freezed when fection value = 7/24 Default Value: 1

## 2.1.53 BLE\_BLERD\_DSM3

DSM freeze code 3

Address: 0x402E00D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE10 [7:4]				INDX_CODE11 [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE8 [15:12]				INDX_CODE9 [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE8	index at which DSM code should be freezed when fection value = 8/24 Default Value: 10
11 : 8	INDX_CODE9	index at which DSM code should be freezed when fection value = 9/24 Default Value: 10
7 : 4	INDX_CODE10	index at which DSM code should be freezed when fection value = 10/24 Default Value: 10
3 : 0	INDX_CODE11	index at which DSM code should be freezed when fection value = 11/24 Default Value: 5

## 2.1.54 BLE\_BLERD\_DSM4

DSM freeze code 4

Address: 0x402E00DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE14 [7:4]				INDX_CODE15 [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE12 [15:12]				INDX_CODE13 [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE12	index at which DSM code should be freezed when fection value = 12/24 Default Value: 8
11 : 8	INDX_CODE13	index at which DSM code should be freezed when fection value = 13/24 Default Value: 9
7 : 4	INDX_CODE14	index at which DSM code should be freezed when fection value = 14/24 Default Value: 1
3 : 0	INDX_CODE15	index at which DSM code should be freezed when fection value = 15/24 Default Value: 1

## 2.1.55 BLE\_BLERD\_DSM5

DSM freeze code 5

Address: 0x402E00E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE18 [7:4]				INDX_CODE19 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE16 [15:12]				INDX_CODE17 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE16	index at which DSM code should be freezed when fection value = 16/24 Default Value: 9
11 : 8	INDX_CODE17	index at which DSM code should be freezed when fection value = 17/24 Default Value: 13
7 : 4	INDX_CODE18	index at which DSM code should be freezed when fection value = 18/24 Default Value: 3
3 : 0	INDX_CODE19	index at which DSM code should be freezed when fection value = 19/24 Default Value: 7



## 2.1.56 BLE\_BLERD\_DSM6

DSM freeze code 6

Address: 0x402E00E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE22 [7:4]				INDX_CODE23 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE20 [15:12]				INDX_CODE21 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE20	index at which DSM code should be freezed when fection value = 20/24 Default Value: 7
11 : 8	INDX_CODE21	index at which DSM code should be freezed when fection value = 21/24 Default Value: 8
7 : 4	INDX_CODE22	index at which DSM code should be freezed when fection value = 22/24 Default Value: 8
3 : 0	INDX_CODE23	index at which DSM code should be freezed when fection value = 23/24 Default Value: 12

## 2.1.57 BLE\_BLERD\_MONI

agc gain and pup signal monitor

Address: 0x402E00E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PUP_SIG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R			R		R		
HW Access	W			W		W		
Name	LNA_CODE [15:13]			CBPF_CODE [12:11]		PUP_SIG [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	LNA_CODE	Ina gain code read back Default Value: 5
12 : 11	CBPF_CODE	cbpf gain code read back Default Value: 3
10 : 0	PUP_SIG	block pup up signals monitor. 10: iso_eanble 9: balum LDO power up, high active 8: SY bias power up, high active 7: SY VCO pup up, high active 6: TX bias pup up, high active 5: TX DAC pup up, high active 4: TX LPF pup up, high active 3: TX driver pup up, high active 2: RX LNA pup up, high active 1: RX CBPF pup up, high active 0: RX ADC ICORE pup, high active Default Value: 1024

## 2.1.58 BLE\_BLERD\_DBG\_BB

RX offcal and RC cal code

Address: 0x402E00EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RX_OFFSET_Q_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RX_OFFSET_I_CODE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	RX_OFFSET_I_CODE	when modem_read_dc_offset_sel = 1, RX DCCAL I path can be read through this field. When modem_read_dc_offset_sel = 0, RC DC offset capture I code can be read through this field rx offsetcal Q code can be read through this field if modem_read_dc_offset_sel = 0 Default Value: 0
7 : 0	RX_OFFSET_Q_CODE	when modem_read_dc_offset_sel = 1, RX DCCAL Q path can be read through this field. When modem_read_dc_offset_sel = 0, RC DC offset capture Q code can be read through this field rx offsetcal Q code can be read through this field if modem_read_dc_offset_sel = 0 Default Value: 0

## 2.1.59 BLE\_BLERD\_DBG\_1

FCAL coarse / fine code is reflected in this field

Address: 0x402E00F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	FCAL_COARSE_CODE [7:4]				FCAL_FINE_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	R			
HW Access	None	W	W	W	W			
Name	None	DCCAL_DONE	KVCAL_DONE	FCAL_DONE	FCAL_COARSE_CODE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	DCCAL_DONE	1: indicates RX DC calibration is done for current packet Default Value: 0
13	KVCAL_DONE	1: indicates TX KV calibration is done for current packet Default Value: 0
12	FCAL_DONE	1: indicates when frequency calibration is done Default Value: 0
11 : 4	FCAL_COARSE_CODE	The FCAL coars code is reflected in this field Default Value: 128
3 : 0	FCAL_FINE_CODE	The FCAL fine code is reflected in this field Default Value: 8

## 2.1.60 BLE\_BLERD\_DBG\_2

FCAL countere value ate the end of 7th bit (MSB)

Address: 0x402E00F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FCAL_CNT_LSB [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	FCAL_CNT_LSB [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	FCAL_CNT_LSB	the dbg_fcal_cnt_sel value, the 16 LSB bits of the corresponding debug counter is pouplated in this register [6:0] is kvcal_gain when select kvcal_gain Default Value: 0

## 2.1.61 BLE\_BLERD\_DBG\_3

VCO OL count read out (MSB)

Address: 0x402E00F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				FCAL_CNT_MSB [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R					None	
HW Access	W	W					None	
Name	RD_RCCAL_DONE	RD_RCCAL_CODE [14:10]					None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	RD_RCCAL_DONE	RCCAL done indicator Default Value: 0
14 : 10	RD_RCCAL_CODE	RCCAL code read out through register Default Value: 0
3 : 0	FCAL_CNT_MSB	the dbg_fcsl_cnt_sel value, the 4 MSB bits of the corresponding debug counter is populated in this register Default Value: 0

## 2.1.62 BLE\_BLERD\_READ\_IQ\_1

I Path ADC Data

Address: 0x402E0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_1 [31:24]							

Bits	Name	Description
31 : 0	ADC_1	read out I path ADC data, first 16bits of I and Qcombination of 63bits Default Value: 0

## 2.1.63 BLE\_BLERD\_READ\_IQ\_2

I Path ADC Data

Address: 0x402E0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_2 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_2 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_2 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_2 [31:24]							

Bits	Name	Description
31 : 0	ADC_2	read out I path ADC data, second 16bits of I and Qcombination of 63bits Default Value: 0



## 2.1.64 BLE\_BLERD\_READ\_IQ\_3

I Path ADC Data

Address: 0x402E0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_3 [31:24]							

Bits	Name	Description
31 : 0	ADC_3	read out I path ADC data, third 16bits of I and Qcombination of 63bits Default Value: 0

## 2.1.65 BLE\_BLERD\_READ\_IQ\_4

I Path ADC Data

Address: 0x402E010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_4 [31:24]							

Bits	Name	Description
31 : 0	ADC_4	read out I path ADC data, fourth 15bits of I and Qcombination of 63bits Default Value: 0

## 3 BLE Sub System (BLESS) Registers



This section discusses the BLESS registers. It lists all the registers in mapping tables, in address order.

### 3.1 Register Details

Register Name	Address
<a href="#">BLE_BLESS_WCO_CONFIG</a>	0x402EF000
<a href="#">BLE_BLESS_WCO_STATUS</a>	Address = 0x402EF004
<a href="#">BLE_BLESS_RF_CONFIG</a>	Address = 0x402EF060
<a href="#">BLE_BLESS_XTAL_CLK_DIV_CONFIG</a>	Address = 0x402EF064
<a href="#">BLE_BLESS_LL_DSM_INTR_STAT</a>	Address = 0x402EF068
<a href="#">BLE_BLESS_LL_DSM_CTRL</a>	Address = 0x402EF06C
<a href="#">BLE_BLESS_LL_CLK_EN</a>	Address = 0x402EF070
<a href="#">BLE_BLESS_LF_CLK_CTRL</a>	Address = 0x402EF074
<a href="#">BLE_BLESS_WCO_TRIM</a>	Address = 0x402EFF00

### 3.1.1 BLE\_BLESS\_WCO\_CONFIG

WCO Configuration Register

Address: 0x402EF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EXT_INPUT_EN	LPM_AUTO	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENBUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for WCO oscillator Default Value: 0
23 : 16	ENBUS	Test Mode Control bits enbus[7] - N/A enbus[6] - 1=enable both primary Beta Multipliers enbus[5] - N/A enbus[4] - 1=enable digital oscillator detect enbus[3] - Load Resistor Control enbus[2] - Load Resistor Control enbus[1] - Load Resistor Control enbus[0] - Load Resistor Control Default Value: 71
2	EXT_INPUT_EN	Disables the load resistor and allows external clock input for pad_xin Default Value: 0
1	LPM_AUTO	Reserved - This bit is not functional and should be set to 0. Default Value: 1

### 3.1.1 BLE\_BLESS\_WCO\_CONFIG (continued)

0	LPM_EN	Force block into Low Power Mode: 0: Do not force low power mode (LPM) on 1: Force low power mode (LPM) on Default Value: 0
---	--------	---

### 3.1.2 BLE\_BLESS\_WCO\_STATUS

WCO Status Register

Address: 0x402EF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT_BLNK_A

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	OUT_BLNK_A	Indicates that WCO clock has transitioned- This bit is intended for Test Mode Only and is not a reliable indicator. Default Value: 0

### 3.1.3 BLE\_BLESS\_RF\_CONFIG

Radio configuration register

Address: 0x402EF060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None			RW
HW Access	R				None			R
Name	DDFT_MUX_CFG1 [7:4]				None [3:1]			RF_ENAB LE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None		RW			
HW Access	R	R	None		R			
Name	BPKTCTL_ FW_DRIVE	BPKTCTL_ FW	None [13:12]		DDFT_MUX_CFG2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BPKTCTL_FW_DRIVE	Enabled FW drives BLERD bpkctl for radio standalone testing Default Value: 0
14	BPKTCTL_FW	FW drives BLERD bpkctl if this register bit 15 enabled Default Value: 0
11 : 8	DDFT_MUX_CFG2	dbg_mux_pin2 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_2_rd 4'h1 rxdata (RD output) 4'b2 ll_decode_rx_data (llh_cy_asic output) 4'h3 dbus_tx_en (llh_cy_asic output) 4'h4 fw_clk_en (pwr_ctrl_top output) 4'h5 interrupt_ll_n (llh_cy_asic output) 4'h6 ll_st_sm (llh is in SM ) 4'h7 ll_st_dsm (llh is in DSM) 4'he clk_gate_en_xtal (RD eco xtal clock gater enable) 4'hf bb_xo_amp_detect_dft_mux (RD output) Default Value: 0

### 3.1.3 BLE\_BLESS\_RF\_CONFIG (continued)

7 : 4	DDFT_MUX_CFG1	dbg_mux_pin1 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_1_rd (RD output) 4'h1 rxclk (RD output) 4'h2 bpktctl_to_rd (RD input) 4'h3 dbus_rx_en (llh_cy_asic output) 4'h4 hw_clk_en (pwr_ctrl_top) 4'h5 clk_switch_to_sysclk (pwr_ctrl_top) 4'h6 ll_clk_en_sync (LL global clock enable from BLESS reg synced) 4'h7 dsm_entry_stat (llh_cy_asic output) 4'h8 ll_dsm_xo_on (LL in DSM, RD XO enabled) 4'h9 ll_dsm_xo_off (LL in DSM, RD XO disabled) 4'hf delayed_bg_en (m0s8bless_misc_dpssp_top output vs LS to s8blerf) Default Value: 0
0	RF_ENABLE	Enables the RF oscillator band gap. 1: band gap is enabled 0: band gap is disabled Default Value: 0



### 3.1.4 BLE\_BLESS\_XTAL\_CLK\_DIV\_CONFIG

Crystal clock divider configuration register

Address: 0x402EF064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				LLCLK_DIV [3:2]		SYSCLK_DIV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 2	LLCLK_DIV	Link Layer clock pre-divider value. The 24 MHz crystal clock is divided to generate the Link Layer clock. 0: NO_DIV: LLCLK= XTALCLK/1 1: DIV_BY_2: LLCLK= XTALCLK/2 2: DIV_BY_4: LLCLK= XTALCLK/4 3: DIV_BY_8: LLCLK= XTALCLK/8 Default Value: 0
1 : 0	SYSCLK_DIV	System clock pre-divider value. The 24 MHz crystal clock is divided to generate the system clock. 0: NO_DIV: SYSCLK= XTALCLK/1 1: DIV_BY_2: SYSCLK= XTALCLK/2 2: DIV_BY_4: SYSCLK= XTALCLK/4 3: DIV_BY_8: SYSCLK= XTALCLK/8 Default Value: 0

### 3.1.5 BLE\_BLESS\_LL\_DSM\_INTR\_STAT

Link Layer interrupt status register

Address: 0x402EF068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						DSM_EXIT ED_INTR	DSM_ENTE RED_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							XTAL_ON_I NTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	XTAL_ON_INTR	enabled crystal stable signal rising edge interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0
1	DSM_EXITED_INTR	On a firmware request to LL to exit from Deep Sleep Mode, working on LF clock, LL transitions from Deep Sleep Mode and asserts this interrupt when the Deep Sleep clock gater is turned ON. The interrupt can be cleared by writing one into this location. Default Value: 0
0	DSM_ENTERED_INTR	On a firmware request to LL to enter into state machine, working on LF clock, LL transitions into Deep Sleep Mode and asserts this interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0

### 3.1.6 BLE\_BLESS\_LL\_DSM\_CTRL

Link Layer state machine control register

Address: 0x402EF06C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	RW1C
Name	None [7:4]				XTAL_ON_INTR_MASK	DSM_EXITED_INTR_MASK	DSM_ENTERED_INTR_MASK	DSM_EXIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	XTAL_ON_INTR_MASK	Masks the Crystal Stable Interrupt, when disabled. Default Value: 1
2	DSM_EXITED_INTR_MASK	Masks the DSM Exited Interrupt, when disabled. Default Value: 1
1	DSM_ENTERED_INTR_MASK	Masks the DSM Entered Interrupt, when disabled. Default Value: 1
0	DSM_EXIT	When the Link Layer is in Deep Sleep Mode, firmware can set this bit to wake the Link Layer. Default Value: 0

### 3.1.7 BLE\_BLESS\_LL\_CLK\_EN

Link Layer primary clock enable

Address: 0x402EF070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CY_CORR EL_EN	CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CY_CORREL_EN	Set this bit 1 to enable Cypress Correlator logic to bypass MT logic Default Value: 1
0	CLK_EN	Set this bit 1 to enable the clock to Link Layer. Default Value: 0

### 3.1.8 BLE\_BLESS\_LF\_CLK\_CTRL

BLESS LF clock control

Address: 0x402EF074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DISABLE_L F_CLK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DISABLE_LF_CLK	When set to 1, gates the LF clock input to the Link Layer. This is done for extended DSM mode where the DSM state machine needs to be forzen to prevent a default auto exit. Default Value: 0

### 3.1.9 BLE\_BLESS\_WCO\_TRIM

WCO Trim Register

Address: 0x402EFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [7:6]		LPM_GM [5:4]		None	XGM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LPM_GM	GM setting for LPM (bandwidth = DC/ms) Default Value: 1
2 : 0	XGM	Amplifier GM setting 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 1

## 4 BLE Sub System Version 2 Registers



This section discusses the BLESS Version 2 registers. It lists all the registers in mapping tables, in address order.

### 4.1 Register Details

Register Name	Address
BLE_BLESS_WCO_CONFIG	0x402EF000
BLE_BLESS_WCO_STATUS	0x402EF004
BLE_BLESS_BIST_MODE_EN	0x402EF00C
BLE_BLESS_BIST_CMD	0x402EF010
BLE_BLESS_BIST_DATA	0x402EF014
BLE_BLESS_BIST_MASK	0x402EF018
BLE_BLESS_BIST_CTL	0x402EF01C
BLE_BLESS_BIST_STEP0_CTL	0x402EF020
BLE_BLESS_BIST_STEP1_CTL	0x402EF024
BLE_BLESS_BIST_STEP2_CTL	0x402EF028
BLE_BLESS_BIST_STEP3_CTL	0x402EF02C
BLE_BLESS_BIST_STEP4_CTL	0x402EF030
BLE_BLESS_BIST_STEP5_CTL	0x402EF034
BLE_BLESS_BIST_STEP6_CTL	0x402EF038
BLE_BLESS_BIST_STEP7_CTL	0x402EF03C
BLE_BLESS_BIST_ADDR_START	0x402EF040
BLE_BLESS_BIST_POL_MASK	0x402EF044
BLE_BLESS_BIST_STATUS	0x402EF048
BLE_BLESS_BIST_DATA_ACT	0x402EF04C
BLE_BLESS_BIST_DATA_EXP	0x402EF050
BLE_BLESS_BIST_ADDR	0x402EF054
BLE_BLESS_RF_CONFIG	0x402EF060
BLE_BLESS_XTAL_CLK_DIV_CONFIG	0x402EF064
BLE_BLESS_LL_DSM_INTR_STAT	0x402EF068
BLE_BLESS_LL_DSM_CTRL	0x402EF06C
BLE_BLESS_LL_CLK_EN	0x402EF070
BLE_BLESS_LF_CLK_CTRL	0x402EF074

Register Name	Address
BLE_BLESS_WCO_TRIM	0x402EFF00



## 4.1.1 BLE\_BLESS\_WCO\_CONFIG

WCO Configuration Register

Address: 0x402EF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EXT_INPUT_EN	LPM_AUTO	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENBUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for WCO oscillator Default Value: 0
23 : 16	ENBUS	Test Mode Control bits enbus[7] - N/A enbus[6] - 1=enable both primary Beta Multipliers enbus[5] - N/A enbus[4] - 1=enable digital oscillator detect enbus[3] - Load Resistor Control enbus[2] - Load Resistor Control enbus[1] - Load Resistor Control enbus[0] - Load Resistor Control Default Value: 71
2	EXT_INPUT_EN	Disables the load resistor and allows external clock input for pad_xin Default Value: 0

#### 4.1.1 BLE\_BLESS\_WCO\_CONFIG (continued)

1	LPM_AUTO	<p>Automatically control low power mode (only relevant when LPM_EN=0):</p> <p>0: Do not enter low power mode (LPM) in DeepSleep</p> <p>1: Enter low power mode (LPM) in DeepSleep</p> <p>This bit is not functional and should be set to 0,</p> <p>While entering System DeepSleep Mode, do the following before executing WFI</p> <p>IOW BLESS.WCO_TRIM.XGM = 3b010</p> <p>IOW BLESS.WCO_TRIM.LPM_GM = 2b10</p> <p>IOW BLESS.WCO_CONFIG.LPM_EN = 1b1</p> <p>While existing from System DeepSleep Mode, do the following before executing ISR</p> <p>IOW BLESS.WCO_CONFIG.LPM_EN = 1b0</p> <p>IOW BLESS.WCO_TRIM.XGM = 3b001</p> <p>IOW BLESS.WCO_TRIM.LPM_GM = 2b01</p> <p>Default Value: 1</p>
0	LPM_EN	<p>Force block into Low Power Mode:</p> <p>0: Do not force low power mode (LPM) on</p> <p>1: Force low power mode (LPM) on</p> <p>Default Value: 0</p>

## 4.1.2 BLE\_BLESS\_WCO\_STATUS

WCO Status Register

Address: 0x402EF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT_BLNK_A

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	OUT_BLNK_A	Indicates that WCO clock has transitioned- This bit is intended for Test Mode Only and is not a reliable indicator. Default Value: 0

### 4.1.3 BLE\_BLESS\_BIST\_MODE\_EN

Memory BIST mode enable

Address: 0x402EF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MEM_BIST_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MEM_BIST_MODE	enables memory BIST mode 1'b0 : Memories are in functional mode and receive 24MHz Xtal clock 1'b1 : Memories are in BIST mode and receive system clock Default Value: 0

## 4.1.4 BLE\_BLESS\_BIST\_CMD

Bist command register

Address: 0x402EF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW1C
Name	None [7:1]							SRAM_GO

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SRAM_GO	1': Start SRAM BIST. Hardware set this field to '0' when BIST is completed. Default Value: 0

## 4.1.5 BLE\_BLESS\_BIST\_DATA

BIST data register

Address: 0x402EF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data that is written into a SRAM during a W0 substep (~BIST_DATA.DATA is written into a SRAM during a W1 substep). Default Value: 0

## 4.1.6 BLE\_BLESS\_BIST\_MASK

BIST mask register

Address: 0x402EF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MASK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MASK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MASK [31:24]							

Bits	Name	Description
31 : 0	MASK	Bit mask, which effectively reduces the data bits on which the BIST is performed. A '1' indicates that the corresponding data bit is partakes in BIST. Default Value: 4294967295

## 4.1.7 BLE\_BLESS\_BIST\_CTL

BIST control register

Address: 0x402EF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SRAMS_ENABLED [5:0]					
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [23:22]		ADDR_START_ENABLED	ROW_FIRST	None	STEPS [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	ADDR_START_ENABLED	0': Row and column addresses start with their maximum/minimum values. '1': Row and column addresses start with their values as specified by BIST_ADDR_START. Default Value: 0
20	ROW_FIRST	Specifies how the SRAM addresses are generated: '0': Column address is incremented/decremented till it reaches its maximum/minimum value. Once it reach its maximum/minimum value, it is set to its minimum/maximum value and only then is the row address incremented/decremented. '1': Row address is incremented/decremented till it reaches its maximum/minimum value. Once it reach its maximum/minimum value, it is set to its minimum/maximum value and only then is the column address incremented/decremented. Default Value: 0



#### 4.1.7 BLE\_BLESS\_BIST\_CTL (continued)

18 : 16	STEPS	<p>Amount of steps. The steps are further detailed by the BIST_STEPi_CTL registers. Multiple steps are used in sequence to implement a specific BIST algorithm:</p> <ul style="list-style-type: none"> <li>- MATS (4N, 3 steps: up/down W0; up/down R0_W1; up/down R1)</li> <li>- MATS+ (5N, 3 steps: up/down W0; up R0_W1; down R1_W0)</li> <li>- Marching 1/0 (14N, 6 steps: up/down W0; up R0_W1_R1; down R1_W0_R0; up/down W1; up R1_W0_R0; down R0_W1_R1)</li> <li>- MATS++ (6N, 3 steps: up/down W0; up R0_W1; down R1_W0_R0)</li> <li>- MARCH C (10N, 6 steps: up/down W0; up R0_W1; up R1_W0; up/down R0; down R1_W0_W1_W0; down R0_W1_W0)</li> <li>- MARCH A (15N, 5 steps: up/down W0; up R0_W1_W0_W1; up R1_W0_W1; down R1_W0_W1_W0; down R0_W1_W0)</li> <li>- MARCH Y (8N, 4 steps: up/down W0; up R0_W1_R1; down R1_W0_R0; up/down R0)</li> <li>- MARCH B (17N, 5 steps: up/down W0; up R0_W1_R1_W0_R0_W1; up R1_W0_W1; down R1_W0_W1_W0; down R0_W1_W0)</li> <li>- MARCH LR (14N, 6 steps: up/down W0; up R0_W1; up R1_W0_R0_W1; down R1_W0; down R0_W1_R1_W0; up/down R0)</li> </ul> <p>Default Value: 0</p>
5 : 0	SRAMS_ENABLED	<p>Hot-one mask for the SRAMs for which the BIST is performed. Default Value: 0</p> <p><b>0x1: ADV_TX_SRAM_MASK:</b> ADV TX FIFO memory</p> <p><b>0x2: ADV_RX_SRAM_MASK:</b> ADV RX FIFO memory</p> <p><b>0x4: CONN_RX_SRAM_MASK:</b> CONN RX FIFO0 and CONN RX FIFO1 memories</p> <p><b>0x8: CONN_TX_SRAM_MASK:</b> CONN TX FIFO0 and CONN TX FIFO1 memories</p> <p><b>0x10: DUT_SRAM_MASK:</b> DUP FIFO memory</p> <p><b>0x20: WLF_SRAM_MASK:</b> WLF FIFO memory</p> <p><b>0x40: ENC_SRAM_MASK:</b> ENC FIFO memory</p>

## 4.1.8 BLE\_BLESS\_BIST\_STEP0\_CTL

BIST step 0 control register

Address: 0x402EF020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	<p>Specifies direction in which SRAM BIST steps through addresses</p> <p>'0': BIST steps through the SRAM from the maximum row and column addresses (as specified by a design time configuration parameter when ADDR_START_ENABLED is '0' and as specified by BIST_ADDR_START when ADDR_START_ENABLED is '1') to the minimum row and column addresses.</p> <p>'1': BIST steps through the SRAM from the minimum row and column addresses ("0" when ADDR_START_ENABLED is '0' and as specified by BIST_ADDR_START when ADDR_START_ENABLED is '1') to the maximum row and column addresses.</p> <p>Default Value: 0</p>

### 4.1.8 BLE\_BLESS\_BIST\_STEP0\_CTL (continued)

3 : 0	OPCODE	<p>Specifies what sequence of SRAM BIST steps (R0, R1, W0, W1) is performed (not used for SROM BIST):</p> <p>"0": W0. Write SRAM with BIST_DATA.DATA.</p> <p>"1": W1. Write SRAM with ~BIST_DATA.DATA.</p> <p>"2": R0. Read SRAM and compare output to BIST_DATA.DATA.</p> <p>"3": R1. Read SRAM and compare output to ~BIST_DATA.DATA.</p> <p>"4": W0, R0. Write SRAM with BIST_DATA.DATA, followed by read SRAM and compare output to BIST_DATA.DATA (all to the same address).</p> <p>"5": R0, W1.</p> <p>"6": R1, W0.</p> <p>"7": R0, W1, R1.</p> <p>"8": R1, W0, R0.</p> <p>"9": R0, W1, W0.</p> <p>"10": R1, W0, W1.</p> <p>"11": R0, W1, W0, W1.</p> <p>"12": R1, W0, W1, W0.</p> <p>"13": R0, W1, R1, W0.</p> <p>"14": R1, W0, R0, W1.</p> <p>"15": R0, W1, R1, W0, R0, W1.</p> <p>Default Value: 0</p>
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## 4.1.9 BLE\_BLESS\_BIST\_STEP1\_CTL

BIST step 1 control register

Address: 0x402EF024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

## 4.1.10 BLE\_BLESS\_BIST\_STEP2\_CTL

BIST step 2 control register

Address: 0x402EF028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

## 4.1.11 BLE\_BLESS\_BIST\_STEP3\_CTL

BIST step 3 control register

Address: 0x402EF02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

## 4.1.12 BLE\_BLESS\_BIST\_STEP4\_CTL

BIST step 4 control register

Address: 0x402EF030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

### 4.1.13 BLE\_BLESS\_BIST\_STEP5\_CTL

BIST step 5 control register

Address: 0x402EF034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0



## 4.1.14 BLE\_BLESS\_BIST\_STEP6\_CTL

BIST step 6 control register

Address: 0x402EF038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

## 4.1.15 BLE\_BLESS\_BIST\_STEP7\_CTL

BIST step 7 control register

Address: 0x402EF03C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

## 4.1.16 BLE\_BLESS\_BIST\_ADDR\_START

BIST address start register

Address: 0x402EF040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COL_ADDR_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COL_ADDR_START [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ROW_ADDR_START [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				ROW_ADDR_START [27:24]			

Bits	Name	Description
27 : 16	ROW_ADDR_START	Row start address. Useful to apply BIST to a part of an SRAM. The value of this field should be in a legal range (a value outside of the legal range has an undefined result, and may lock up the BIST state machine). This legal range is dependent on the number of rows of the SRAM the BIST is applied to (as specified by BIST_CTL.SRAMS_ENABLED). E.g. for a SRAM with m columns, the legal range is [0, m-1]. Default Value: 0
11 : 0	COL_ADDR_START	Column start address. Useful to apply BIST to a part of an SRAM. The value of this field should be in a legal range (a value outside of the legal range has an undefined result, and may lock up the BIST state machine). This legal range is dependent on the number of columns of the SRAM the BIST is applied to (as specified by BIST_CTL.SRAMS_ENABLED). E.g. for a SRAM with n columns, the legal range is [0, n-1]. Default Value: 0

## 4.1.17 BLE\_BLESS\_BIST\_POL\_MASK

BIST address polarity mask register

Address: 0x402EF044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COL_POLARITY_MASK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ROW_POLARITY_MASK [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	ROW_POLARITY_MASK	See description above. Default Value: 0
7 : 0	COL_POLARITY_MASK	Used to change the polarity of a step from R0 into R1 and vice versa or from W0 into W1 and vice versa. Given a row address ROW_ADDR and a column address COL_ADDR, the polarity is changed when the following expression is '1': $\wedge \{ (COL\_ADDR[7:0] \& COL\_POLARITY\_MASK), (ROW\_ADDR[7:0] \& ROW\_POLARITY\_MASK) \}$ Default Value: 0

## 4.1.18 BLE\_BLESS\_BIST\_STATUS

BIST status register

Address: 0x402EF048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					W		
Name	None [7:3]					SUB_STEP [2:0]		
Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					W		
Name	None [15:11]					STEP [10:8]		
Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:20]					SRAM [19:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							W1S
Name	None [31:25]							FAIL

Bits	Name	Description
24	FAIL	0': BIST passed. '1': BIST failed (SRAM match error or ROM MISR check error). BIST error information is found in SRAM, STEP, SUB_STEP fields and BIST_DATA_ACT, BIST_DATA_EXP and BIST_ADDR registers. Default Value: 0
19 : 16	SRAM	SRAM identifier. Default Value: Undefined  <b>0x0: ADV_TX_SRAM:</b> ADV TX FIFO memory  <b>0x1: ADV_RX_SRAM:</b> ADV RX FIFO memory  <b>0x2: CONN_RX_SRAM:</b> CONN RX FIFO memory  <b>0x3: CONN_TX_SRAM:</b> CONN TX FIFO memory  <b>0x4: DUT_SRAM:</b> DUP FIFO memory

#### 4.1.18 BLE\_BLESS\_BIST\_STATUS (continued)

		<b>0x5: WLF_SRAM:</b> WLF FIFO memory
		<b>0x6: ENC_SRAM:</b> ENC FIFO memory
10 : 8	STEP	BIST step (step i uses BIST_STEPi_CTL). Default Value: Undefined
2 : 0	SUB_STEP	BIST substep (either R0, R1, W0, or W1). Default Value: Undefined

## 4.1.19 BLE\_BLESS\_BIST\_DATA\_ACT

BIST data expected register

Address: 0x402EF04C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	For SRAM BIST, this field is the SRAM output data that caused a BIST failure. For ROM BIST, this field is the calculated Multiple Input Shift Register (MISR). Default Value: Undefined

## 4.1.20 BLE\_BLESS\_BIST\_DATA\_EXP

BIST data actual register

Address: 0x402EF050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	For SRAM BIST. This field is the expected data from SRAM. This value is BIST_DATA.DATA for a R0 substep and ~BIST_DATA.DATA for a R1 substep. Default Value: Undefined



## 4.1.21 BLE\_BLESS\_BIST\_ADDR

BIST address register

Address: 0x402EF054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COL_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				COL_ADDR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ROW_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				ROW_ADDR [27:24]			

Bits	Name	Description
27 : 16	ROW_ADDR	Current row address. Default Value: Undefined
11 : 0	COL_ADDR	Current column address. Default Value: Undefined

## 4.1.22 BLE\_BLESS\_RF\_CONFIG

Radio configuration register

Address: 0x402EF060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None			RW
HW Access	R				None			R
Name	DDFT_MUX_CFG1 [7:4]				None [3:1]			RF_ENAB LE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None		RW			
HW Access	R	R	None		R			
Name	BPKTCTL_ FW_DRIVE	BPKTCTL_ FW	None [13:12]		DDFT_MUX_CFG2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BPKTCTL_FW_DRIVE	Enabled FW drives BLERD bpkctl for radio standalone testing Default Value: 0
14	BPKTCTL_FW	FW drives BLERD bpkctl if this register bit 15 enabled Default Value: 0
11 : 8	DDFT_MUX_CFG2	dbg_mux_pin2 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_2_rd 4'h1 rxdata (RD output) 4'b2 ll_decode_rx_data (llh_cy_asic output) 4'h3 dbus_tx_en (llh_cy_asic output) 4'h4 fw_clk_en (pwr_ctrl_top output) 4'h5 interrupt_ll_n (llh_cy_asic output) 4'h6 ll_st_sm (llh is in SM ) 4'h7 ll_st_dsm (llh is in DSM) 4'he clk_gate_en_xtal (RD eco xtal clock gater enable) 4'hf bb_xo_amp_detect_dft_mux (RD output) Default Value: 0

#### 4.1.22 BLE\_BLESS\_RF\_CONFIG (continued)

7 : 4	DDFT_MUX_CFG1	dbg_mux_pin1 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_1_rd (RD output) 4'h1 rxclk (RD output) 4'h2 bpktctl_to_rd (RD input) 4'h3 dbus_rx_en (llh_cy_asic output) 4'h4 hw_clk_en (pwr_ctrl_top) 4'h5 clk_switch_to_sysclk (pwr_ctrl_top) 4'h6 ll_clk_en_sync (LL global clock enable from BLESS reg synced) 4'h7 dsm_entry_stat (llh_cy_asic output) 4'h8 ll_dsm_xo_on (LL in DSM, RD XO enabled) 4'h9 ll_dsm_xo_off (LL in DSM, RD XO disabled) 4'hf delayed_bg_en (m0s8bless_misc_dpssp_top output vs LS to s8blerf) Default Value: 0
0	RF_ENABLE	Enables the RF oscillator band gap. 1: band gap is enabled 0: band gap is disabled Default Value: 0

## 4.1.23 BLE\_BLESS\_XTAL\_CLK\_DIV\_CONFIG

Crystal clock divider configuration register

Address: 0x402EF064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				LLCLK_DIV [3:2]		SYSCLK_DIV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 2	LLCLK_DIV	Link Layer clock pre-divider value. The 24 MHz crystal clock is divided to generate the Link Layer clock. 0: NO_DIV: LLCLK= XTALCLK/1 1: DIV_BY_2: LLCLK= XTALCLK/2 2: DIV_BY_4: LLCLK= XTALCLK/4 3: DIV_BY_8: LLCLK= XTALCLK/8 Default Value: 0
1 : 0	SYSCLK_DIV	System clock pre-divider value. The 24 MHz crystal clock is divided to generate the system clock. 0: NO_DIV: SYSCLK= XTALCLK/1 1: DIV_BY_2: SYSCLK= XTALCLK/2 2: DIV_BY_4: SYSCLK= XTALCLK/4 3: DIV_BY_8: SYSCLK= XTALCLK/8 Default Value: 0

## 4.1.24 BLE\_BLESS\_LL\_DSM\_INTR\_STAT

Link Layer interrupt status register

Address: 0x402EF068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						DSM_EXIT ED_INTR	DSM_ENTE RED_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							XTAL_ON_I NTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	XTAL_ON_INTR	enabled crystal stable signal rising edge interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0
1	DSM_EXITED_INTR	On a firmware request to LL to exit from Deep Sleep Mode, working on LF clock, LL transitions from Deep Sleep Mode and asserts this interrupt when the Deep Sleep clock gater is turned ON. The interrupt can be cleared by writing one into this location. Default Value: 0
0	DSM_ENTERED_INTR	On a firmware request to LL to enter into state machine, working on LF clock, LL transitions into Deep Sleep Mode and asserts this interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0

## 4.1.25 BLE\_BLESS\_LL\_DSM\_CTRL

Link Layer state machine control register

Address: 0x402EF06C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	RW1C
Name	None [7:4]				XTAL_ON_INTR_MASK	DSM_EXITED_INTR_MASK	DSM_ENTERED_INTR_MASK	DSM_EXIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	XTAL_ON_INTR_MASK	Masks the Crystal Stable Interrupt, when disabled. Default Value: 1
2	DSM_EXITED_INTR_MASK	Masks the DSM Exited Interrupt, when disabled. Default Value: 1
1	DSM_ENTERED_INTR_MASK	Masks the DSM Entered Interrupt, when disabled. Default Value: 1
0	DSM_EXIT	When the Link Layer is in Deep Sleep Mode, firmware can set this bit to wake the Link Layer. Default Value: 0

## 4.1.26 BLE\_BLESS\_LL\_CLK\_EN

Link Layer primary clock enable

Address: 0x402EF070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CY_CORR EL_EN	CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CY_CORREL_EN	Set this bit 1 to enable Cypress Correlator logic to bypass MT logic Default Value: 1
0	CLK_EN	Set this bit 1 to enable the clock to Link Layer. Default Value: 0

## 4.1.27 BLE\_BLESS\_LF\_CLK\_CTRL

BLESS LF clock control and BLESS revision ID indicator

Address: 0x402EF074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DISABLE_L F_CLK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R			None				
HW Access	R			None				
Name	M0S8BLESS_REV_ID [31:29]			None [28:24]				

Bits	Name	Description
31 : 29	M0S8BLESS_REV_ID	Indicates the m0s8bless IP revision. Default Value: 1
0	DISABLE_LF_CLK	When set to 1, gates the LF clock input to the Link Layer. This is done for extended DSM mode where the DSM state machine needs to be forzen to prevent a default auto exit. Default Value: 0



## 4.1.28 BLE\_BLESS\_WCO\_TRIM

WCO Trim Register

Address: 0x402EFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [7:6]		LPM_GM [5:4]		None	XGM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LPM_GM	GM setting for LPM (bandwidth = DC/ms) Default Value: 1
2 : 0	XGM	Amplifier GM setting 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 1

## 5 Cortex M0 (CM0) Registers



This section discusses the CM0 registers. It lists all the registers in mapping tables, in address order.

### 5.1 Register Details

Register Name	Address
CM0_DWT_PID4	0xE0001FD0
CM0_DWT_PID0	0xE0001FE0
CM0_DWT_PID1	0xE0001FE4
CM0_DWT_PID2	0xE0001FE8
CM0_DWT_PID3	0xE0001FEC
CM0_DWT_CID0	0xE0001FF0
CM0_DWT_CID1	0xE0001FF4
CM0_DWT_CID2	0xE0001FF8
CM0_DWT_CID3	0xE0001FFC
CM0_BP_PID4	0xE0002FD0
CM0_BP_PID0	0xE0002FE0
CM0_BP_PID1	0xE0002FE4
CM0_BP_PID2	0xE0002FE8
CM0_BP_PID3	0xE0002FEC
CM0_BP_CID0	0xE0002FF0
CM0_BP_CID1	0xE0002FF4
CM0_BP_CID2	0xE0002FF8
CM0_BP_CID3	0xE0002FFC
CM0_SYST_CSR	0xE000E010
CM0_SYST_RVR	0xE000E014
CM0_SYST_CVR	0xE000E018
CM0_SYST_CALIB	0xE000E01C
CM0_ISER	0xE000E100
CM0_ICER	0xE000E180
CM0_ISPR	0xE000E200
CM0_ICPR	0xE000E280

Register Name	Address
CM0_IPR0	0xE000E400
CM0_IPR1	0xE000E404
CM0_IPR2	0xE000E408
CM0_IPR3	0xE000E40C
CM0_IPR4	0xE000E410
CM0_IPR5	0xE000E414
CM0_IPR6	0xE000E418
CM0_IPR7	0xE000E41C
CM0_CPUID	0xE000ED00
CM0_ICSR	0xE000ED04
CM0_AIRCR	0xE000ED0C
CM0_SCR	0xE000ED10
CM0_CCR	0xE000ED14
CM0_SHPR2	0xE000ED1C
CM0_SHPR3	0xE000ED20
CM0_SHCSR	0xE000ED24
CM0_SCS_PID4	0xE000EFD0
CM0_SCS_PID0	0xE000EFE0
CM0_SCS_PID1	0xE000EFE4
CM0_SCS_PID2	0xE000EFE8
CM0_SCS_PID3	0xE000EFEC
CM0_SCS_CID0	0xE000EFF0
CM0_SCS_CID1	0xE000EFF4
CM0_SCS_CID2	0xE000EFF8
CM0_SCS_CID3	0xE000EFFC
CM0_ROM_SCS	0xE00FF000
CM0_ROM_DWT	0xE00FF004
CM0_ROM_BPU	0xE00FF008
CM0_ROM_END	0xE00FF00C
CM0_ROM_CSMT	0xE00FF0CC
CM0_ROM_PID4	0xE00FFFD0
CM0_ROM_PID0	0xE00FFFE0
CM0_ROM_PID1	0xE00FFFE4
CM0_ROM_PID2	0xE00FFFE8
CM0_ROM_PID3	0xE00FF FEC
CM0_ROM_CID0	0xE00FFFF0
CM0_ROM_CID1	0xE00FFFF4
CM0_ROM_CID2	0xE00FFFF8
CM0_ROM_CID3	0xE00FFFFC

## 5.1.1 CM0\_DWT\_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0001FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

## 5.1.2 CM0\_DWT\_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0001FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 10

### 5.1.3 CM0\_DWT\_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0001FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

## 5.1.4 CM0\_DWT\_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0001FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

## 5.1.5 CM0\_DWT\_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0001FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0



## 5.1.6 CM0\_DWT\_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0001FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

## 5.1.7 CM0\_DWT\_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0001FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

## 5.1.8 CM0\_DWT\_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0001FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

## 5.1.9 CM0\_DWT\_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0001FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

## 5.1.10 CM0\_BP\_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0002FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

## 5.1.11 CM0\_BP\_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0002FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 11

## 5.1.12 CM0\_BP\_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0002FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

## 5.1.13 CM0\_BP\_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0002FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11



## 5.1.14 CM0\_BP\_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0002FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

## 5.1.15 CM0\_BP\_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0002FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

## 5.1.16 CM0\_BP\_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0002FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

## 5.1.17 CM0\_BP\_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0002FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

## 5.1.18 CM0\_BP\_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0002FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

## 5.1.19 CM0\_SYST\_CSR

SysTick Control &amp; Status

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CLK-SOURCE	TICKINT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							COUNT-FLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	COUNTFLAG	<p>Indicates whether the counter has counted to "0" since the last read of this register:  '0': counter has not counted to "0".  '1': counter has counted to "0".</p> <p>COUNTFLAG is set to '1' by a count transition from "1" to "0".  COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register.  Default Value: 0</p>

## 5.1.19 CM0\_SYST\_CSR (continued)

2	CLKSOURCE	<p>Indicates the SysTick counter clock source:</p> <p>'0': SysTick uses the low frequency clock "clk_lf". For this mode to function, "clk_lf" should be less than half the frequency of "clk_sys". Note that "clk_lf" is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 KHz and as high as 60 kHz).</p> <p>'1': SysTick uses the system/processor clock "clk_sys".</p> <p>In PRoC BLE (and later products), SysTick counter functionality on the low frequency clock is provided. in SF, TSG6M products, this functionality is not provided. For these products, this field should be set to '1', such that SysTick uses the system clock "clk_sys".</p> <p>Default Value: 0</p>
1	TICKINT	<p>Indicates whether counting to "0" causes the status of the SysTick exception to change to pending:</p> <p>'0': count to "0" does not affect the SysTick exception status.</p> <p>'1': count to "0" changes the SysTick exception status to pending.</p> <p>Changing the value of the counter to "0" by writing zero to the SYST_CVR register to "0" never changes the status of the SysTick exception.</p> <p>Default Value: 0</p>
0	ENABLE	<p>Indicates the enabled status of the SysTick counter:</p> <p>'0': counter is disabled.</p> <p>'1': counter is operating.</p> <p>Default Value: 0</p>

## 5.1.20 CM0\_SYST\_RVR

SysTick Reload Value

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELOAD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELOAD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RELOAD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X



## 5.1.21 CM0\_SYST\_CVR

SysTick Current Value

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CURRENT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CURRENT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CURRENT [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

## 5.1.22 CM0\_SYST\_CALIB

SysTick Calibration Value

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TENMS [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TENMS [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TENMS [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	None	RW	None					
Name	NOREF	SKEW	None [29:24]					

Bits	Name	Description
31	NOREF	<p>Indicates whether a implementation defined reference clock is provided:  '0': the reference clock is provided.  '1': the reference clock is not provided.  When this bit is '1', the SYST_CSR.CLKSOURCE is forced to '1' and cannot be cleared to '0'.</p> <p>In PRoC BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '0'. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '1'.  Default Value: 0</p>
30	SKEW	<p>Indicates whether the 10ms calibration value is exact:  '0': 10ms calibration value is exact.  '1': 10ms calibration value is inexact, because of the clock frequency.</p> <p>In PRoC BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '0'.  Default Value: X</p>

## 5.1.22 CM0\_SYST\_CALIB (continued)

23 : 0      TENMS

Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is "0", the calibration value is not known.

In PRoC BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is 0x00:0000.  
Default Value: X

## 5.1.23 CM0\_ISER

Interrupt Set-Enable Register

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETENA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETENA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETENA [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETENA [31:24]							

Bits	Name	Description
31 : 0	SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

## 5.1.24 CM0\_ICER

Interrupt Clear Enable Register

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRENA [31:24]							

Bits	Name	Description
31 : 0	CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

## 5.1.25 CM0\_ISPR

Interrupt Set-Pending Register

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETPEND [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETPEND [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETPEND [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETPEND [31:24]							

Bits	Name	Description
31 : 0	SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

## 5.1.26 CM0\_ICPR

Interrupt Clear-Pending Register

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

## 5.1.27 CM0\_IPR0

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0



## 5.1.28 CM0\_IPR1

Interrupt Priority Registers

Address: 0xE000E404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

  

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

  

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

## 5.1.29 CM0\_IPR2

Interrupt Priority Registers

Address: 0xE000E408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					
Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					
Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					
Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

## 5.1.30 CM0\_IPR3

Interrupt Priority Registers

Address: 0xE000E40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					
Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					
Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					
Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

## 5.1.31 CM0\_IPR4

Interrupt Priority Registers

Address: 0xE000E410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

  

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

  

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

## 5.1.32 CM0\_IPR5

Interrupt Priority Registers

Address: 0xE000E414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					
Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					
Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					
Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

## 5.1.33 CM0\_IPR6

Interrupt Priority Registers

Address: 0xE000E418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

  

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

  

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

## 5.1.34 CM0\_IPR7

Interrupt Priority Registers

Address: 0xE000E41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

## 5.1.35 CM0\_CPUID

CPUID Register

Address: 0xE00ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	None				None			
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	None				None			
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	IMPLEMENTER	Implementer code for ARM. Default Value: 65
23 : 20	VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rn timer revision status, Product revision status on page xii. Default Value: 0
19 : 16	CONSTANT	Indicates the architecture, ARMv6-M Default Value: 12
15 : 4	PARTNO	Indicates part number, Cortex-M0 Default Value: 3104
3 : 0	REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rn timer revision status, see Product revision status on page xii. For release r0p0. Default Value: 0



## 5.1.36 CM0\_ICSR

Interrupt Control State Register

Address: 0xE000ED04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	VECTPENDING [15:12]				None [11:9]			VECTACTIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	ISRPRE-EMPT	ISRPENDING	None	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	NMIPEND-SET	None [30:29]		PENDSV-SET	PENDSV-CLR	PENDST-SETb	PENDST-CLR	None

Bits	Name	Description
31	NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
27	PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
25	PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0

### 5.1.36 CM0\_ICSR (continued)

23	ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0
22	ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

## 5.1.37 CM0\_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					SYSRESE- TREQ	VECTCL- RACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	None	None						
Name	ENDIAN- NESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VECTKEY [31:24]							

Bits	Name	Description
31 : 16	VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UNPREDICTABLE. Readback value is UNKNOWN. Default Value: X
15	ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default Value: 0
2	SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information. Default Value: 0
1	VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. Default Value: 0

## 5.1.38 CM0\_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			SEVON- PEND	None	SLEEP- DEEP	SLEEPON- EXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information. Default Value: 0
2	SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default Value: 0
1	SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information. Default Value: 0

## 5.1.39 CM0\_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None				None	None		
Name	None [7:4]				UNALIGN_ TRP	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None						None	None
Name	None [15:10]						STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

## 5.1.40 CM0\_SHPR2

System Handler Priority Register 2

Address: 0xE000ED1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_11	Priority of system handler 11, SVCall Default Value: 0

## 5.1.41 CM0\_SHPR3

System Handler Priority Register 3

Address: 0xE000ED20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_14 [23:22]		None [21:16]					
Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	PRI_14	Priority of system handler 14, PendSV Default Value: 0

## 5.1.42 CM0\_SHCSR

System Handler Control and State Register

Address: 0xE000ED24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	SVCALL- PENDEDED	None [14:8]						
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SVCALLPENDEDED	<p>0 SVCAll is not pending.  1 SVCAll is pending.  This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.)  Default Value: 0</p>



## 5.1.43 CM0\_SCS\_PID4

System Control Space ROM Table Peripheral ID #4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

## 5.1.44 CM0\_SCS\_PID0

System Control Space ROM Table Peripheral ID #0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 8

## 5.1.45 CM0\_SCS\_PID1

System Control Space ROM Table Peripheral ID #1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

## 5.1.46 CM0\_SCS\_PID2

System Control Space ROM Table Peripheral ID #2

Address: 0xE00EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

## 5.1.47 CM0\_SCS\_PID3

System Control Space ROM Table Peripheral ID #3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

## 5.1.48 CM0\_SCS\_CID0

System Control Space ROM Table Component ID #0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

## 5.1.49 CM0\_SCS\_CID1

System Control Space ROM Table Component ID #1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

## 5.1.50 CM0\_SCS\_CID2

System Control Space ROM Table Component ID #2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5



## 5.1.51 CM0\_SCS\_CID3

System Control Space ROM Table Component ID #3

Address: 0xE000E0FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

## 5.1.52 CM0\_ROM\_SCS

CM0 CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 4293980163

## 5.1.53 CM0\_ROM\_DWT

CM0 CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 4293926915

## 5.1.54 CM0\_ROM\_BPU

CM0 CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table Default Value: 4293931011

## 5.1.55 CM0\_ROM\_END

CM0 CoreSight ROM Table End Marker

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	End marker in peripheral list Default Value: 0

## 5.1.56 CM0\_ROM\_CSMT

CM0 CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

## 5.1.57 CM0\_ROM\_PID4

CM0 CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

## 5.1.58 CM0\_ROM\_PID0

CM0 CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 113



## 5.1.59 CM0\_ROM\_PID1

CM0 CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 180

## 5.1.60 CM0\_ROM\_PID2

CM0 CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

## 5.1.61 CM0\_ROM\_PID3

CM0 CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

## 5.1.62 CM0\_ROM\_CID0

CM0 CoreSight ROM Table Component ID #0

Address: 0xE00FFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

## 5.1.63 CM0\_ROM\_CID1

CM0 CoreSight ROM Table Component ID #1

Address: 0xE00FFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 16

## 5.1.64 CM0\_ROM\_CID2

CM0 CoreSight ROM Table Component ID #2

Address: 0xE00FFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

## 5.1.65 CM0\_ROM\_CID3

CM0 CoreSight ROM Table Component ID #3

Address: 0xE00FFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

## 6 Timer, Counter, PWM Counter (CNT) Registers



This section discusses the CNT registers. It lists all the registers in mapping tables, in address order.

### 6.1 Register Details

Register Name	Address
<a href="#">TCPWM_CNT0_CTRL</a>	0x40200100
<a href="#">TCPWM_CNT0_STATUS</a>	0x40200104
<a href="#">TCPWM_CNT0_COUNTER</a>	0x40200108
<a href="#">TCPWM_CNT0_CC</a>	0x4020010C
<a href="#">TCPWM_CNT0_CC_BUFF</a>	0x40200110
<a href="#">TCPWM_CNT0_PERIOD</a>	0x40200114
<a href="#">TCPWM_CNT0_PERIOD_BUFF</a>	0x40200118
<a href="#">TCPWM_CNT0_TR_CTRL0</a>	0x40200120
<a href="#">TCPWM_CNT0_TR_CTRL1</a>	0x40200124
<a href="#">TCPWM_CNT0_TR_CTRL2</a>	0x40200128
<a href="#">TCPWM_CNT0_INTR</a>	0x40200130
<a href="#">TCPWM_CNT0_INTR_SET</a>	0x40200134
<a href="#">TCPWM_CNT0_INTR_MASK</a>	0x40200138
<a href="#">TCPWM_CNT0_INTR_MASKED</a>	0x4020013C
<a href="#">TCPWM_CNT1_CTRL</a>	0x40200140
<a href="#">TCPWM_CNT1_STATUS</a>	0x40200144
<a href="#">TCPWM_CNT1_COUNTER</a>	0x40200148
<a href="#">TCPWM_CNT1_CC</a>	0x4020014C
<a href="#">TCPWM_CNT1_CC_BUFF</a>	0x40200150
<a href="#">TCPWM_CNT1_PERIOD</a>	0x40200154
<a href="#">TCPWM_CNT1_PERIOD_BUFF</a>	0x40200158
<a href="#">TCPWM_CNT1_TR_CTRL0</a>	0x40200160
<a href="#">TCPWM_CNT1_TR_CTRL1</a>	0x40200164
<a href="#">TCPWM_CNT1_TR_CTRL2</a>	0x40200168
<a href="#">TCPWM_CNT1_INTR</a>	0x40200170
<a href="#">TCPWM_CNT1_INTR_SET</a>	0x40200174



Register Name	Address
TCPWM_CNT1_INTR_MASK	0x40200178
TCPWM_CNT1_INTR_MASKED	0x4020017C
TCPWM_CNT2_CTRL	0x40200180
TCPWM_CNT2_STATUS	0x40200184
TCPWM_CNT2_COUNTER	0x40200188
TCPWM_CNT2_CC	0x4020018C
TCPWM_CNT2_CC_BUFF	0x40200190
TCPWM_CNT2_PERIOD	0x40200194
TCPWM_CNT2_PERIOD_BUFF	0x40200198
TCPWM_CNT2_TR_CTRL0	0x402001A0
TCPWM_CNT2_TR_CTRL1	0x402001A4
TCPWM_CNT2_TR_CTRL2	0x402001A8
TCPWM_CNT2_INTR	0x402001B0
TCPWM_CNT2_INTR_SET	0x402001B4
TCPWM_CNT2_INTR_MASK	0x402001B8
TCPWM_CNT2_INTR_MASKED	0x402001BC
TCPWM_CNT3_CTRL	0x402001C0
TCPWM_CNT3_STATUS	0x402001C4
TCPWM_CNT3_COUNTER	0x402001C8
TCPWM_CNT3_CC	0x402001CC
TCPWM_CNT3_CC_BUFF	0x402001D0
TCPWM_CNT3_PERIOD	0x402001D4
TCPWM_CNT3_PERIOD_BUFF	0x402001D8
TCPWM_CNT3_TR_CTRL0	0x402001E0
TCPWM_CNT3_TR_CTRL1	0x402001E4
TCPWM_CNT3_TR_CTRL2	0x402001E8
TCPWM_CNT3_INTR	0x402001F0
TCPWM_CNT3_INTR_SET	0x402001F4
TCPWM_CNT3_INTR_MASK	0x402001F8
TCPWM_CNT3_INTR_MASKED	0x402001FC

## 6.1.1 TCPWM\_CNT0\_CTRL

Counter control register

Address: 0x40200100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STO P_ON_KILL	PWM_SYN C_KILL	AUTO_REL OAD_PERI OD	AUTO_REL OAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0  <b>0x0: TIMER:</b> Timer mode  <b>0x2: CAPTURE:</b> Capture mode  <b>0x3: QUAD:</b> Quadrature encoding mode  <b>0x4: PWM:</b> Pulse width modulation (PWM) mode  <b>0x5: PWM_DT:</b> PWM with deadtime insertion mode  <b>0x6: PWM_PR:</b> Pseudo random pulse width modulation

## 6.1.1 TCPWM\_CNT0\_CTRL (continued)

21 : 20	QUADRATURE_MODE	<p>In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1].</p> <p>Default Value: 0</p> <p><b>0x0: X1:</b> X1 encoding (QUAD mode)</p> <p><b>0x1: X2:</b> X2 encoding (QUAD mode)</p> <p><b>0x1: INV_OUT:</b> When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes)</p> <p><b>0x2: X4:</b> X4 encoding (QUAD mode)</p> <p><b>0x2: INV_COMPL_OUT:</b> When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)</p>
18	ONE_SHOT	<p>When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated.</p> <p>Default Value: 0</p>
17 : 16	UP_DOWN_MODE	<p>Determines counter direction.</p> <p>Default Value: 0</p> <p><b>0x0: COUNT_UP:</b> Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD.</p> <p><b>0x1: COUNT_DOWN:</b> Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x2: COUNT_UPDN1:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x3: COUNT_UPDN2:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).</p>
15 : 8	GENERIC	<p>Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock.</p> <p>Default Value: 0</p> <p><b>0x0: DIVBY1:</b> Divide by 1 (other-than-PWM_DT mode)</p> <p><b>0x1: DIVBY2:</b> Divide by 2 (other-than-PWM_DT mode)</p> <p><b>0x2: DIVBY4:</b> Divide by 4 (other-than-PWM_DT mode)</p>

### 6.1.1 TCPWM\_CNT0\_CTRL (continued)

		<p><b>0x3: DIVBY8:</b> Divide by 8 (other-than-PWM_DT mode)</p> <p><b>0x4: DIVBY16:</b> Divide by 16 (other-than-PWM_DT mode)</p> <p><b>0x5: DIVBY32:</b> Divide by 32 (other-than-PWM_DT mode)</p> <p><b>0x6: DIVBY64:</b> Divide by 64 (other-than-PWM_DT mode)</p> <p><b>0x7: DIVBY128:</b> Divide by 128 (other-than-PWM_DT mode)</p>
3	PWM_STOP_ON_KILL	<p>Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter.</p> <p>This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0</p>
2	PWM_SYNC_KILL	<p>Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET.</p> <p>This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0</p>
1	AUTO_RELOAD_PERIOD	<p>Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0</p>
0	AUTO_RELOAD_CC	<p>Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0': never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0</p>

## 6.1.2 TCPWM\_CNT0\_STATUS

Counter status register

Address: 0x40200104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

## 6.1.3 TCPWM\_CNT0\_COUNTER

Counter count register

Address: 0x40200108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

## 6.1.4 TCPWM\_CNT0\_CC

Counter compare/capture register

Address: 0x4020010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

## 6.1.5 TCPWM\_CNT0\_CC\_BUFF

Counter buffered compare/capture register

Address: 0x40200110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535



## 6.1.6 TCPWM\_CNT0\_PERIOD

Counter period register

Address: 0x40200114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

## 6.1.7 TCPWM\_CNT0\_PERIOD\_BUFF

Counter buffered period register

Address: 0x40200118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

## 6.1.8 TCPWM\_CNT0\_TR\_CTRL0

Counter trigger control register 0

Address: 0x40200120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

### 6.1.8 TCPWM\_CNT0\_TR\_CTRL0 (continued)

3 : 0	CAPTURE_SEL	<p>Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts.</p> <p>Default Value: 0</p>
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## 6.1.9 TCPWM\_CNT0\_TR\_CTRL1

Counter trigger control register 1

Address: 0x40200124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	<p>A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
7 : 6	STOP_EDGE	<p>A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p>

## 6.1.9 TCPWM\_CNT0\_TR\_CTRL1 (continued)

		<p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
5 : 4	RELOAD_EDGE	<p>A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
3 : 2	COUNT_EDGE	<p>A counter event will increase or decrease the counter by '1'. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
1 : 0	CAPTURE_EDGE	<p>A capture event will copy the counter value into the CC register. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>

## 6.1.10 TCPWM\_CNT0\_TR\_CTRL2

Counter trigger control register 2

Address: 0x40200128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	<p>Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>
3 : 2	OVERFLOW_MODE	<p>Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p>

## 6.1.10 TCPWM\_CNT0\_TR\_CTRL2 (continued)

		<b>0x1: CLEAR:</b> Set to '0'
		<b>0x2: INVERT:</b> Invert
		<b>0x3: NO_CHANGE:</b> No Change
1 : 0	CC_MATCH_MODE	<p>Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation.</p> <p>To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register.</p> <p>Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>



## 6.1.11 TCPWM\_CNT0\_INTR

Interrupt request register.

Address: 0x40200130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

## 6.1.12 TCPWM\_CNT0\_INTR\_SET

Interrupt set request register.

Address: 0x40200134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 6.1.13 TCPWM\_CNT0\_INTR\_MASK

Interrupt mask register.

Address: 0x40200138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 6.1.14 TCPWM\_CNT0\_INTR\_MASKED

Interrupt masked request register

Address: 0x4020013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

## 6.1.15 TCPWM\_CNT1\_CTRL

Counter control register

Address: 0x40200140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STO P_ON_KILL	PWM_SYN C_KILL	AUTO_REL OAD_PERI OD	AUTO_REL OAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0  <b>0x0: TIMER:</b> Timer mode  <b>0x2: CAPTURE:</b> Capture mode  <b>0x3: QUAD:</b> Quadrature encoding mode  <b>0x4: PWM:</b> Pulse width modulation (PWM) mode  <b>0x5: PWM_DT:</b> PWM with deadtime insertion mode  <b>0x6: PWM_PR:</b> Pseudo random pulse width modulation

## 6.1.15 TCPWM\_CNT1\_CTRL (continued)

21 : 20	QUADRATURE_MODE	<p>In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0</p> <p><b>0x0: X1:</b> X1 encoding (QUAD mode)</p> <p><b>0x1: X2:</b> X2 encoding (QUAD mode)</p> <p><b>0x1: INV_OUT:</b> When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes)</p> <p><b>0x2: X4:</b> X4 encoding (QUAD mode)</p> <p><b>0x2: INV_COMPL_OUT:</b> When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)</p>
18	ONE_SHOT	<p>When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0</p>
17 : 16	UP_DOWN_MODE	<p>Determines counter direction. Default Value: 0</p> <p><b>0x0: COUNT_UP:</b> Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD.</p> <p><b>0x1: COUNT_DOWN:</b> Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x2: COUNT_UPDN1:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x3: COUNT_UPDN2:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).</p>
15 : 8	GENERIC	<p>Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0</p> <p><b>0x0: DIVBY1:</b> Divide by 1 (other-than-PWM_DT mode)</p> <p><b>0x1: DIVBY2:</b> Divide by 2 (other-than-PWM_DT mode)</p> <p><b>0x2: DIVBY4:</b> Divide by 4 (other-than-PWM_DT mode)</p>

## 6.1.15 TCPWM\_CNT1\_CTRL (continued)

		<p><b>0x3: DIVBY8:</b> Divide by 8 (other-than-PWM_DT mode)</p> <p><b>0x4: DIVBY16:</b> Divide by 16 (other-than-PWM_DT mode)</p> <p><b>0x5: DIVBY32:</b> Divide by 32 (other-than-PWM_DT mode)</p> <p><b>0x6: DIVBY64:</b> Divide by 64 (other-than-PWM_DT mode)</p> <p><b>0x7: DIVBY128:</b> Divide by 128 (other-than-PWM_DT mode)</p>
3	PWM_STOP_ON_KILL	<p>Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter.</p> <p>This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0</p>
2	PWM_SYNC_KILL	<p>Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET.</p> <p>This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0</p>
1	AUTO_RELOAD_PERIOD	<p>Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0</p>
0	AUTO_RELOAD_CC	<p>Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0': never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0</p>

## 6.1.16 TCPWM\_CNT1\_STATUS

Counter status register

Address: 0x40200144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0



## 6.1.17 TCPWM\_CNT1\_COUNTER

Counter count register

Address: 0x40200148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

## 6.1.18 TCPWM\_CNT1\_CC

Counter compare/capture register

Address: 0x4020014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

## 6.1.19 TCPWM\_CNT1\_CC\_BUFF

Counter buffered compare/capture register

Address: 0x40200150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

## 6.1.20 TCPWM\_CNT1\_PERIOD

Counter period register

Address: 0x40200154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

## 6.1.21 TCPWM\_CNT1\_PERIOD\_BUFF

Counter buffered period register

Address: 0x40200158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

## 6.1.22 TCPWM\_CNT1\_TR\_CTRL0

Counter trigger control register 0

Address: 0x40200160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

### 6.1.22 TCPWM\_CNT1\_TR\_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0
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## 6.1.23 TCPWM\_CNT1\_TR\_CTRL1

Counter trigger control register 1

Address: 0x40200164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	<p>A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
7 : 6	STOP_EDGE	<p>A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p>



## 6.1.23 TCPWM\_CNT1\_TR\_CTRL1 (continued)

		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3
		<b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.
		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3
		<b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.
		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3
		<b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.
		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.

## 6.1.24 TCPWM\_CNT1\_TR\_CTRL2

Counter trigger control register 2

Address: 0x40200168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	<p>Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>
3 : 2	OVERFLOW_MODE	<p>Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p>

## 6.1.24 TCPWM\_CNT1\_TR\_CTRL2 (continued)

		<b>0x1: CLEAR:</b> Set to '0'
		<b>0x2: INVERT:</b> Invert
		<b>0x3: NO_CHANGE:</b> No Change
1 : 0	CC_MATCH_MODE	<p>Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation.</p> <p>To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register.</p> <p>Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>

## 6.1.25 TCPWM\_CNT1\_INTR

Interrupt request register.

Address: 0x40200170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

## 6.1.26 TCPWM\_CNT1\_INTR\_SET

Interrupt set request register.

Address: 0x40200174

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 6.1.27 TCPWM\_CNT1\_INTR\_MASK

Interrupt mask register.

Address: 0x40200178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 6.1.28 TCPWM\_CNT1\_INTR\_MASKED

Interrupt masked request register

Address: 0x4020017C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

## 6.1.29 TCPWM\_CNT2\_CTRL

Counter control register

Address: 0x40200180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STO P_ON_KILL	PWM_SYN C_KILL	AUTO_REL OAD_PERI OD	AUTO_REL OAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0  <b>0x0: TIMER:</b> Timer mode  <b>0x2: CAPTURE:</b> Capture mode  <b>0x3: QUAD:</b> Quadrature encoding mode  <b>0x4: PWM:</b> Pulse width modulation (PWM) mode  <b>0x5: PWM_DT:</b> PWM with deadtime insertion mode  <b>0x6: PWM_PR:</b> Pseudo random pulse width modulation



## 6.1.29 TCPWM\_CNT2\_CTRL (continued)

21 : 20	QUADRATURE_MODE	<p>In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0</p> <p><b>0x0: X1:</b> X1 encoding (QUAD mode)</p> <p><b>0x1: X2:</b> X2 encoding (QUAD mode)</p> <p><b>0x1: INV_OUT:</b> When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes)</p> <p><b>0x2: X4:</b> X4 encoding (QUAD mode)</p> <p><b>0x2: INV_COMPL_OUT:</b> When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)</p>
18	ONE_SHOT	<p>When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0</p>
17 : 16	UP_DOWN_MODE	<p>Determines counter direction. Default Value: 0</p> <p><b>0x0: COUNT_UP:</b> Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD.</p> <p><b>0x1: COUNT_DOWN:</b> Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x2: COUNT_UPDN1:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x3: COUNT_UPDN2:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).</p>
15 : 8	GENERIC	<p>Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0</p> <p><b>0x0: DIVBY1:</b> Divide by 1 (other-than-PWM_DT mode)</p> <p><b>0x1: DIVBY2:</b> Divide by 2 (other-than-PWM_DT mode)</p> <p><b>0x2: DIVBY4:</b> Divide by 4 (other-than-PWM_DT mode)</p>

## 6.1.29 TCPWM\_CNT2\_CTRL (continued)

		<p><b>0x3: DIVBY8:</b> Divide by 8 (other-than-PWM_DT mode)</p> <p><b>0x4: DIVBY16:</b> Divide by 16 (other-than-PWM_DT mode)</p> <p><b>0x5: DIVBY32:</b> Divide by 32 (other-than-PWM_DT mode)</p> <p><b>0x6: DIVBY64:</b> Divide by 64 (other-than-PWM_DT mode)</p> <p><b>0x7: DIVBY128:</b> Divide by 128 (other-than-PWM_DT mode)</p>
3	PWM_STOP_ON_KILL	<p>Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter.</p> <p>This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0</p>
2	PWM_SYNC_KILL	<p>Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET.</p> <p>This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0</p>
1	AUTO_RELOAD_PERIOD	<p>Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0</p>
0	AUTO_RELOAD_CC	<p>Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0': never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0</p>

## 6.1.30 TCPWM\_CNT2\_STATUS

Counter status register

Address: 0x40200184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

## 6.1.31 TCPWM\_CNT2\_COUNTER

Counter count register

Address: 0x40200188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

## 6.1.32 TCPWM\_CNT2\_CC

Counter compare/capture register

Address: 0x4020018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

## 6.1.33 TCPWM\_CNT2\_CC\_BUFF

Counter buffered compare/capture register

Address: 0x40200190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

## 6.1.34 TCPWM\_CNT2\_PERIOD

Counter period register

Address: 0x40200194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

## 6.1.35 TCPWM\_CNT2\_PERIOD\_BUFF

Counter buffered period register

Address: 0x40200198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535



## 6.1.36 TCPWM\_CNT2\_TR\_CTRL0

Counter trigger control register 0

Address: 0x402001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

### 6.1.36 TCPWM\_CNT2\_TR\_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0
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## 6.1.37 TCPWM\_CNT2\_TR\_CTRL1

Counter trigger control register 1

Address: 0x402001A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	<p>A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
7 : 6	STOP_EDGE	<p>A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p>

## 6.1.37 TCPWM\_CNT2\_TR\_CTRL1 (continued)

		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3
		<b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.
		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3
		<b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.
		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3
		<b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.
		<b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.
		<b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.
		<b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.

## 6.1.38 TCPWM\_CNT2\_TR\_CTRL2

Counter trigger control register 2

Address: 0x402001A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	<p>Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>
3 : 2	OVERFLOW_MODE	<p>Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p>

### 6.1.38 TCPWM\_CNT2\_TR\_CTRL2 (continued)

		<b>0x1: CLEAR:</b> Set to '0'
		<b>0x2: INVERT:</b> Invert
		<b>0x3: NO_CHANGE:</b> No Change
1 : 0	CC_MATCH_MODE	<p>Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation.</p> <p>To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register.</p> <p>Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>

## 6.1.39 TCPWM\_CNT2\_INTR

Interrupt request register.

Address: 0x402001B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

## 6.1.40 TCPWM\_CNT2\_INTR\_SET

Interrupt set request register.

Address: 0x402001B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0



## 6.1.41 TCPWM\_CNT2\_INTR\_MASK

Interrupt mask register.

Address: 0x402001B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 6.1.42 TCPWM\_CNT2\_INTR\_MASKED

Interrupt masked request register

Address: 0x402001BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

## 6.1.43 TCPWM\_CNT3\_CTRL

Counter control register

Address: 0x402001C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STO P_ON_KILL	PWM_SYN C_KILL	AUTO_REL OAD_PERI OD	AUTO_REL OAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0  <b>0x0: TIMER:</b> Timer mode  <b>0x2: CAPTURE:</b> Capture mode  <b>0x3: QUAD:</b> Quadrature encoding mode  <b>0x4: PWM:</b> Pulse width modulation (PWM) mode  <b>0x5: PWM_DT:</b> PWM with deadtime insertion mode  <b>0x6: PWM_PR:</b> Pseudo random pulse width modulation

## 6.1.43 TCPWM\_CNT3\_CTRL (continued)

21 : 20	QUADRATURE_MODE	<p>In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0</p> <p><b>0x0: X1:</b> X1 encoding (QUAD mode)</p> <p><b>0x1: X2:</b> X2 encoding (QUAD mode)</p> <p><b>0x1: INV_OUT:</b> When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes)</p> <p><b>0x2: X4:</b> X4 encoding (QUAD mode)</p> <p><b>0x2: INV_COMPL_OUT:</b> When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)</p>
18	ONE_SHOT	<p>When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0</p>
17 : 16	UP_DOWN_MODE	<p>Determines counter direction. Default Value: 0</p> <p><b>0x0: COUNT_UP:</b> Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD.</p> <p><b>0x1: COUNT_DOWN:</b> Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x2: COUNT_UPDN1:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".</p> <p><b>0x3: COUNT_UPDN2:</b> Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).</p>
15 : 8	GENERIC	<p>Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0</p> <p><b>0x0: DIVBY1:</b> Divide by 1 (other-than-PWM_DT mode)</p> <p><b>0x1: DIVBY2:</b> Divide by 2 (other-than-PWM_DT mode)</p> <p><b>0x2: DIVBY4:</b> Divide by 4 (other-than-PWM_DT mode)</p>

## 6.1.43 TCPWM\_CNT3\_CTRL (continued)

		<p><b>0x3: DIVBY8:</b> Divide by 8 (other-than-PWM_DT mode)</p> <p><b>0x4: DIVBY16:</b> Divide by 16 (other-than-PWM_DT mode)</p> <p><b>0x5: DIVBY32:</b> Divide by 32 (other-than-PWM_DT mode)</p> <p><b>0x6: DIVBY64:</b> Divide by 64 (other-than-PWM_DT mode)</p> <p><b>0x7: DIVBY128:</b> Divide by 128 (other-than-PWM_DT mode)</p>
3	PWM_STOP_ON_KILL	<p>Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter.</p> <p>This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0</p>
2	PWM_SYNC_KILL	<p>Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET.</p> <p>This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0</p>
1	AUTO_RELOAD_PERIOD	<p>Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0</p>
0	AUTO_RELOAD_CC	<p>Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0': never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0</p>

## 6.1.44 TCPWM\_CNT3\_STATUS

Counter status register

Address: 0x402001C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

## 6.1.45 TCPWM\_CNT3\_COUNTER

Counter count register

Address: 0x402001C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

## 6.1.46 TCPWM\_CNT3\_CC

Counter compare/capture register

Address: 0x402001CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535



## 6.1.47 TCPWM\_CNT3\_CC\_BUFF

Counter buffered compare/capture register

Address: 0x402001D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

## 6.1.48 TCPWM\_CNT3\_PERIOD

Counter period register

Address: 0x402001D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

## 6.1.49 TCPWM\_CNT3\_PERIOD\_BUFF

Counter buffered period register

Address: 0x402001D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

## 6.1.50 TCPWM\_CNT3\_TR\_CTRL0

Counter trigger control register 0

Address: 0x402001E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

### 6.1.50 TCPWM\_CNT3\_TR\_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0
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## 6.1.51 TCPWM\_CNT3\_TR\_CTRL1

Counter trigger control register 1

Address: 0x402001E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	<p>A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
7 : 6	STOP_EDGE	<p>A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p>

## 6.1.51 TCPWM\_CNT3\_TR\_CTRL1 (continued)

		<p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
5 : 4	RELOAD_EDGE	<p>A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
3 : 2	COUNT_EDGE	<p>A counter event will increase or decrease the counter by '1'. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>
1 : 0	CAPTURE_EDGE	<p>A capture event will copy the counter value into the CC register. Default Value: 3</p> <p><b>0x0: RISING_EDGE:</b> Rising edge. Any rising edge generates an event.</p> <p><b>0x1: FALLING_EDGE:</b> Falling edge. Any falling edge generates an event.</p> <p><b>0x2: BOTH_EDGES:</b> Rising AND falling edge. Any odd amount of edges generates an event.</p> <p><b>0x3: NO_EDGE_DET:</b> No edge detection, use trigger as is.</p>

## 6.1.52 TCPWM\_CNT3\_TR\_CTRL2

Counter trigger control register 2

Address: 0x402001E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	<p>Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>
3 : 2	OVERFLOW_MODE	<p>Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p>



## 6.1.52 TCPWM\_CNT3\_TR\_CTRL2 (continued)

		<b>0x1: CLEAR:</b> Set to '0'
		<b>0x2: INVERT:</b> Invert
		<b>0x3: NO_CHANGE:</b> No Change
1 : 0	CC_MATCH_MODE	<p>Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation.</p> <p>To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register.</p> <p>Default Value: 3</p> <p><b>0x0: SET:</b> Set to '1'</p> <p><b>0x1: CLEAR:</b> Set to '0'</p> <p><b>0x2: INVERT:</b> Invert</p> <p><b>0x3: NO_CHANGE:</b> No Change</p>

## 6.1.53 TCPWM\_CNT3\_INTR

Interrupt request register.

Address: 0x402001F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

## 6.1.54 TCPWM\_CNT3\_INTR\_SET

Interrupt set request register.

Address: 0x402001F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 6.1.55 TCPWM\_CNT3\_INTR\_MASK

Interrupt mask register.

Address: 0x402001F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 6.1.56 TCPWM\_CNT3\_INTR\_MASKED

Interrupt masked request register

Address: 0x402001FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

# 7 System Resource Sub System Registers



This section discusses the CORE registers. It lists all the registers in mapping tables, in address order.

## 7.1 Register Details

Register Name	Address
PWR_CONTROL	0x400B0000
PWR_INTR	0x400B0004
PWR_INTR_MASK	0x400B0008
PWR_KEY_DELAY	0x400B000C
PWR_BG_CONFIG	0x400B0014
PWR_VMON_CONFIG	0x400B0018
PWR_DDFT_SELECT	0x400B0020
PWR_DFT_KEY	0x400B0024
PWR_BOD_KEY	0x400B0028
PWR_STOP	0x400B002C
CLK_SELECT	0x400B0100
CLK_ILO_CONFIG	0x400B0104
CLK_IMO_CONFIG	0x400B0108
CLK_IMO_SPREAD	0x400B010C
CLK_DFT_SELECT	0x400B0110
WDT_CTRLOW	0x400B0200
WDT_CTRHIGH	0x400B0204
WDT_MATCH	0x400B0208
WDT_CONFIG	0x400B020C
WDT_CONTROL	0x400B0210
RES_CAUSE	0x400B0300
PWR_BG_TRIM3	0x400BFF18
PWR_BG_TRIM4	0x400BFF1C
PWR_BG_TRIM5	0x400BFF20
CLK_ILO_TRIM	0x400BFF24
CLK_IMO_TRIM1	0x400BFF28
CLK_IMO_TRIM2	0x400BFF2C

Register Name	Address
CLK_IMO_TRIM4	0x400BFF34
PWR_RSVD_TRIM	0x400BFF38

## 7.1.1 PWR\_CONTROL

Power Mode Control

Address: 0x400B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		RW	RW	RW			
Name	None [7:6]		LPM_READ Y	DEBUG_SE SSION	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None						
HW Access	R	None						
Name	EXT_VCCD	None [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW1S	RW	None	RW1S	RW
HW Access	R	None	R	R	A	None	RW0C	R
Name	HIBER- NATE	None	LFCLK_SH ORT	HIBERNAT E_DISABLE	FIMO_DISA BLE	None	HVMON_R ELOAD	HVMON_E NABLE

Bits	Name	Description
31	HIBERNATE	<p>Selects between HIBERNATE/DEEPSLEEP modes when Cortex-M0 enters low power mode (SleepDeep). Note: this bit is ignored when HIBERNATE_DISABLE=1. Default Value: 1</p> <p><b>0x0: DEEP_SLEEP:</b> Enter DeepSleep mode when CPU asserts SLEEPDEEP signal</p> <p><b>0x1: HIBERNATE:</b> Enter Hibernate mode when CPU asserts SLEEPDEEP signal</p>
29	LFCLK_SHORT	<p>Short Vccfclk and Vccdsp power rails in DeepSleep power mode. This mode selection affects the accuracy specifications of the ILO oscillator due to supply noise. See Data Sheet for more details.</p> <p>0: Do not short power domains 1: Short power domains Default Value: 0</p>



### 7.1.1 PWR\_CONTROL (continued)

28	HIBERNATE_DISABLE	<p>0: Normal operation, HIBERNATE works as described  1: HIBERNATE bit is ignored, Hibernate mode is permanently disabled (part will go to DeepSleep instead).  Note: This bit is a write-once bit until the next reset.  Default Value: 0</p>
27	FIMO_DISABLE	<p>This bit is asserted during the boot process  0: Forces IMO to operate at 12MHz, ignore its frequency and trim settings and operate independent on its external references.  1: Turns IMO into normal operational mode  Default Value: 0</p>
25	HVMON_RELOAD	<p>Firmware writes 1 to reload HV State in hibernate shadow copy. Hardware clears this bit after reload was successful. Wait at least 9 cycles after writing/recalling NVL before reloading the HVMON.  Default Value: 0</p>
24	HVMON_ENABLE	<p>0: HV State Monitoring is disabled  1: HV State Monitoring is automatically enable by sleep controller  Default Value: 1</p>
23	EXT_VCCD	<p>Should be set by firmware if Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (PBOD) unless both Vddd and Vccd pins are supplied externally.  Default Value: 0</p>
5	LPM_READY	<p>Indicates whether the low power mode regulators are ready to enter DEEPSLEEP or HIBERNATE mode.  0: If DEEPSLEEP or HIBERNATE mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode.  1: Normal operation. DEEPSLEEP and HIBERNATE work as described.  Default Value: 0</p>
4	DEBUG_SESSION	<p>Indicates whether a debug session is active (CDBGPWUPREQ signal is 1)  Default Value: 0</p> <p><b>0x0: NO_SESSION:</b>  No debug session active</p> <p><b>0x1: SESSION_ACTIVE:</b>  Debug session is active</p>
3 : 0	POWER_MODE	<p>Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon.  Default Value: 0</p> <p><b>0x0: RESET:</b>  RESET state</p> <p><b>0x1: ACTIVE:</b>  ACTIVE state</p> <p><b>0x2: SLEEP:</b>  SLEEP state</p> <p><b>0x3: DEEP_SLEEP:</b>  DEEP_SLEEP state</p> <p><b>0x4: HIBERNATE:</b>  HIBERNATE state</p>

## 7.1.2 PWR\_INTR

Power System Interrupt Register

Address: 0x400B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	None
HW Access	None						A	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	Indicates an Low Voltage Detect interrupt Default Value: 0

## 7.1.3 PWR\_INTR\_MASK

Power System Interrupt Mask Register

Address: 0x400B0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	1: Propagate interrupt to CPU Default Value: 0

## 7.1.4 PWR\_KEY\_DELAY

Power System Key Register

Address: 0x400B000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: 780

## 7.1.5 PWR\_BG\_CONFIG

Bandgap Trim and Configuration

Address: 0x400B0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW				RW
HW Access	R		R	R				R
Name	BG_DFT_ICORE_SEL [7:6]		BG_DFT_CORE_SEL	BG_DFT_VREF_SEL [4:1]				BG_DFT_EN

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							BG_DFT_VCORE_SEL

  

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					VREF_EN [18:16]		

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18 : 16	VREF_EN	Reference voltage enable. Each bit enables a reference voltage used by a peripheral: vref[0] = 1 enables SRSS.VREF[0] to 1.024V vref[1] = 1 enables SRSS.VREF[1] to 1.024V vref[2] = 1 enables SRSS.VREF[2] to 1.2V  These references require 40us to settle after enabling them and 30us to settle after waking from DeepSleep. Default Value: 0
8	BG_DFT_VCORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects a BG core voltage to output on mux2out 0=vout 1=vgnd Default Value: 0

### 7.1.5 PWR\_BG\_CONFIG (continued)

7 : 6	BG_DFT_ICORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects a BG core current to output on mux1out 0=iptat (current) 1=ictat (current) 2=inl_cross_over detect (voltage) 3=iref9p6u_dft (dedicated output for DFT) Also selects a current for iref_dft (when BG_DFT_VREF_SEL=13) 0=iref2p4u[1] 1=iptat2p4u[7] 2=iref_imo (9.6uA current output from IMO IBG) 3=iref3u_dft (dedicated output for DFT) Default Value: 0
5	BG_DFT_CORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects which BG core signal to output on adft_bg_core 0=BG core voltage selected by BG_DFT_VCORE_SEL (mux2out) 1=BG core current selected by BG_DFT_ICORE_SEL (mux1out) Default Value: 0
4 : 1	BG_DFT_VREF_SEL	ADFT mux select for Reference System characterization (engineering only). Select a voltage reference to output on adft_bg_ref 0=vgnd 1=vref_fast[0] 2=vref_fast[1] 3=vref_fast[2] 4=vref_fast[3] 5=vref_fast[4] 6=vref_fast[5] 7=vref_fast[6] 8=vref_fast[7] 9=vref[0] 10=vref[1] 11=vref[2] 12=vcctat 13=iref_dft (see BG_DFT_ICORE_SEL) 14=imo_iref (current) 15=inl_imoref (voltage) Default Value: 0
0	BG_DFT_EN	Enables DFT capability for Bandgap. (engineering only) Default Value: 0

## 7.1.6 PWR\_VMON\_CONFIG

Voltage Monitoring Trim and Configuration

Address: 0x400B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	VMON_DDFT_SEL [7:5]			LVD_SEL [4:1]				LVD_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						VMON_ADFT_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	VMON_ADFT_SEL	ADFT mux select for HVPOR, PBOD, and LVD circuits (engineering only). Selects a signal to output on adft_vmon 0: Hi-Z 1: Comparator Input of pbod Monitor 2: Comparator Input of hvpbod Monitor 3: Comparator Input of lvi Monitor Default Value: 0
7 : 5	VMON_DDFT_SEL	DDFT mux select for HVPOR, PBOD, and LVD circuits (engineering only). Selects a signal to output on adft_vmon 0: 0 1: pbod_out 2: Pulse Strecher output of pbod Monitor 3: hvpbod_out 4: Pulse Strecher output of hvpbod Monitor 5: lvi_out 6: Pulse Strecher output of lvi Monitor 7: 0 Default Value: 0

## 7.1.6 PWR\_VMON\_CONFIG (continued)

4 : 1	LVD_SEL	<p>Threshold selection for Low Voltage Detect circuit. Disable the LVD (LVD_EN=0) before changing the threshold. Threshold variation is +/- 2.5% from these typical voltage choices:</p> <p>0: 1.7500 V  1: 1.8000 V  2: 1.9000 V  3: 2.0000 V  4: 2.1000 V  5: 2.2000 V  6: 2.3000 V  7: 2.4000 V  8: 2.5000 V  9: 2.6000 V  10: 2.7000 V  11: 2.8000 V  12: 2.9000 V  13: 3.0000 V  14: 3.2000 V  15: 4.5000 V  Default Value: 0</p>
0	LVD_EN	<p>Enable Low Voltage Detect circuit.  Default Value: 0</p>



## 7.1.7 PWR\_DDFT\_SELECT

Digital DFT Select

Address: 0x400B0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DDFT2_SEL [7:4]				DDFT1_SEL [3:0]			

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	DDFT2_SEL	Signal select for ddft2 output: 0: act_power_en_a 1: power_up_raw 2: act_power_good_a 3: fastrefs_valid 4: vmon 5: bootref_outen 6: bootref_refsw 7: active_inrush_dis 8: awake 9: hypor_reset_n 10: lpcomp_dis 11: wakeup_a 12: vmon_valid 13: block_rst_awake 14: slpholdreq_n 15: io_disable_delayed Default Value: 0

### 7.1.7 PWR\_DDFT\_SELECT (continued)

3 : 0	DDFT1_SEL	Signal select for ddft1 output: 0: wakeup_a 1: ipor_reset 2: hbod_reset_raw_n 3: lpcomp_dis 4: power_up_delayed 5: awake 6: hvmon_out_of_sync 7: pbod_reset 8: hvbod_reset 9: lpm_ready 10: io_disable_req_lv (excluding por_force_in_hv) 11: bootref_en Default Value: 0
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## 7.1.8 PWR\_DFT\_KEY

DFT Safety Override

Address: 0x400B0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	KEY16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	KEY16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			VMON_PD	IO_DISABLE_BYPASS	DFT_MODE	BODS_OFF	HBOD_OFF_AWAKE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	VMON_PD	Disables the VMON block, which includes PBOD, HVBOD, and LVD circuits. Set BODS_OFF=1 in a previous write cycle to prevent an unintended reset. Default Value: 0
19	IO_DISABLE_BYPASS	Bypasses the IO disable logic for testing the delay-line that is part of the glitch-free IO reset circuitry. Internally, prevents the outputs from getting disabled (io_disable_req_hv=0) and blocks resets (io_disable_ack_hv=0). The delay-line continues to function and can be routed to DDFT for testing. Default Value: 0
18	DFT_MODE	Enable DfT modes other than the above. Currently gates power_up comparator for characterization. Default Value: 0
17	BODS_OFF	Forces all outputs of BOD detectors to be ignored, effectively disabling all brown-out detection. Can be used in conjunction with DDFT to test the detectors without triggering reset. Default Value: 0
16	HBOD_OFF_AWAKE	Forces the output of the HBOD to be blocked (ignored) while in Active or Sleep mode (i.e. when under the umbrella of PBOD). Default Value: 0

### 7.1.8 PWR\_DFT\_KEY (continued)

15 : 0	KEY16	<p>This field must be set to 0xE4C5 for any of the other fields in this register to have effect and for scan_mode to be allowed. When this field has any other value, all other fields in this register are ignored and assumed to be 0 by the hardware, and scan_mode is ignored inside the power generation system. It is assumed that this register will always be set to 0xE4C5 before entering scan.</p> <p>Default Value: 0</p>
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## 7.1.9 PWR\_BOD\_KEY

BOD Detection Key

Address: 0x400B0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	KEY16 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	KEY16 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	KEY16	<p>To detect brown-outs firmware should do this on boot:</p> <ol style="list-style-type: none"> <li>1. Set key= KEY16</li> <li>2. Set KEY16= 0x3A71</li> <li>3. If key==0x3A71 this was a brown-out event.</li> </ol> <p>Default Value: X</p>

## 7.1.10 PWR\_STOP

STOP Mode Register

Address: 0x400B002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [23:18]						FREEZE	POLARITY
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	STOP	None [30:24]						

Bits	Name	Description
31	STOP	Firmware sets this bit to enter STOP mode. Both UNLOCK and FREEZE must have been set correctly in a previous write operation. Otherwise, writes to this bit will affect the freeze override but will not actually set the STOP bit. The system will enter STOP mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Default Value: 0
17	FREEZE	Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. Two identical write cycles are required to freeze the IO explicitly. The first cycle instructs DEEPSLEEP and HIBERNATE peripherals whether they can override upcoming freeze command(s). UNLOCK setting does not affect this. If firmware writes FREEZE=1 and STOP=0, peripherals can override the freeze and remain functional according to their configuration. If firmware writes FREEZE=1 and STOP=1, peripherals cannot override the next freeze command. The second write cycle freezes the IO if UNLOCK is set and the peripheral does not override the freeze. While FREEZE=1, peripherals will automatically freeze according to the override directive when entering DEEPSLEEP or HIBERNATE, regardless of the UNLOCK setting. Default Value: 0
16	POLARITY	0: WAKEUP=0 will wakeup the part from STOP 1: WAKEUP=1 will wakeup the part from STOP Default Value: 0

### 7.1.10 PWR\_STOP (continued)

15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or STOP fields to operate. Any other value in this register will cause FREEZE/STOP to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a STOP/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from STOP using XRES will reset this register. Default Value: 0

## 7.1.11 CLK\_SELECT

Clock Select Register

Address: 0x400B0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PLL_SEL [7:6]		DBL_SEL [5:3]			DIRECT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW			RW
HW Access	A		R		R			R
Name	WDT_LOCK [15:14]		DPLLREF_SEL [13:12]		DPLLIN_SEL [11:9]			PLL_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW			RW	RW	
HW Access	None		R			R	R	
Name	None [23:22]		SYSCLK_DIV [21:19]			HALF_EN	HFCLK_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 19	SYSCLK_DIV	<p>SYSCLK Pre-Scaler Value. Default Value: 0</p> <p><b>0x0: NO_DIV:</b> SYSCLK= HFCLK/1</p> <p><b>0x1: DIV_BY_2:</b> SYSCLK= HFCLK/2</p> <p><b>0x2: DIV_BY_4:</b> SYSCLK= HFCLK/4</p> <p><b>0x3: DIV_BY_8:</b> SYSCLK= HFCLK/8</p> <p><b>0x4: DIV_BY_16:</b> SYSCLK= HFCLK/16</p> <p><b>0x5: DIV_BY_32:</b> SYSCLK= HFCLK/32</p> <p><b>0x6: DIV_BY_64:</b> SYSCLK= HFCLK/64</p>



## 7.1.11 CLK\_SELECT (continued)

		<b>0x7: DIV_BY_128:</b> SYSCLK= HFCLK/128
18	HALF_EN	<p>This bit impact products using CPUSSv1 only. It has no effect on products using CPUSSv2. FLASH Wait-state selection. This must be set to 1 when clk_sys is set to a frequency greater than 24MHz.</p> <p>0: Access FLASH using 0 wait-states. Only use this setting when HFCLK is &lt;=24MHz.  1: Access FLASH using 1 wait-state. Safe to use this setting for any clock frequency.  Default Value: 0</p>
17 : 16	HFCLK_SEL	<p>Selects the source for HFCLK.  Default Value: 0</p> <p><b>0x0: DIRECT_SEL:</b>  Source selected by DIRECT_SEL</p> <p><b>0x1: DBL:</b>  Output of DBL (Doublor) - Selects output of EXCO PLL1 if supported.  Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior.  Note: this is called DBL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products.</p> <p><b>0x2: PLL:</b>  Output of PLL - Selects output of EXCO PLL0 if supported.  Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior.  Note: this is called PLL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products.</p>
15 : 14	WDT_LOCK	<p>Prohibits writing to WDT_* registers and CLK_ILO register when not equal 0. Requires at least two different writes to unlock.  Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all WATCHDOG registers at the same time.  Default Value: 0</p> <p><b>0x0: NO_CHG:</b>  No effect</p> <p><b>0x1: CLR0:</b>  Clears bit 0</p> <p><b>0x2: CLR1:</b>  Clears bit 1</p> <p><b>0x3: SET01:</b>  Sets both bits 0 and 1</p>
13 : 12	DPLLREF_SEL	<p>Selects a source for the reference (tracking) input of DPLL:</p> <p>0: DSI_OUT[0]  1: DSI_OUT[1]  2: DSI_OUT[2]  3: DSI_OUT[3]  Default Value: 0</p> <p><b>0x0: DSI0:</b>  DSI_OUT[0]</p> <p><b>0x1: DSI1:</b>  DSI_OUT[1]</p> <p><b>0x2: DSI2:</b>  DSI_OUT[2]</p>

## 7.1.11 CLK\_SELECT (continued)

11 : 9	DPLLIN_SEL	<p><b>0x3: DSI3:</b> DSI_OUT[3]</p> <p>Selects a source for the input of DPLL. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0</p> <p><b>0x0: IMO:</b> IMO - Internal R/C Oscillator</p> <p><b>0x1: EXTCLK:</b> EXTCLK - External Clock Pin</p> <p><b>0x2: ECO:</b> ECO - External-Crystal Oscillator (Crystal external, Oscillator internal)</p> <p><b>0x4: DSI0:</b> DSI_OUT[0]</p> <p><b>0x5: DSI1:</b> DSI_OUT[1]</p> <p><b>0x6: DSI2:</b> DSI_OUT[2]</p> <p><b>0x7: DSI3:</b> DSI_OUT[3]</p>
8 : 6	PLL_SEL	<p>Selects a source the input of EXCO PLL0, if supported. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note: this is called PLL_SEL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products. Default Value: 0</p> <p><b>0x0: IMO:</b> IMO - Internal R/C Oscillator</p> <p><b>0x1: EXTCLK:</b> EXTCLK - External Clock Pin</p> <p><b>0x2: ECO:</b> ECO - External-Crystal Oscillator (Crystal external, Oscillator internal)</p> <p><b>0x3: DPLL:</b> DPLL - DPLL Output</p> <p><b>0x4: DSI0:</b> DSI_OUT[0]</p> <p><b>0x5: DSI1:</b> DSI_OUT[1]</p> <p><b>0x6: DSI2:</b> DSI_OUT[2]</p> <p><b>0x7: DSI3:</b> DSI_OUT[3]</p>

### 7.1.11 CLK\_SELECT (continued)

5 : 3	DBL_SEL	<p>Selects a source the input of EXCO PLL1, if supported. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note: this is called DBL_SEL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products. Default Value: 0</p> <p><b>0x0: IMO:</b> IMO - Internal R/C Oscillator</p> <p><b>0x1: EXTCLK:</b> EXTCLK - External Clock Pin</p> <p><b>0x2: ECO:</b> ECO - External-Crystal Oscillator (Crystal external, Oscillator internal)</p> <p><b>0x4: DSI0:</b> DSI_OUT[0]</p> <p><b>0x5: DSI1:</b> DSI_OUT[1]</p> <p><b>0x6: DSI2:</b> DSI_OUT[2]</p> <p><b>0x7: DSI3:</b> DSI_OUT[3]</p>
2 : 0	DIRECT_SEL	<p>Selects a source for HFCLK (when HFCLK_SEL=0) and DSI_IN[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note that using DSI_OUT[3:0] as HFCLK source will also result in undefined behavior. These values are available strictly to provide a clock in DSI_IN[0]. Default Value: 0</p> <p><b>0x0: IMO:</b> IMO - Internal R/C Oscillator</p> <p><b>0x1: EXTCLK:</b> EXTCLK - External Clock Pin</p> <p><b>0x2: ECO:</b> ECO - External-Crystal Oscillator (Crystal external, Oscillator internal)</p> <p><b>0x4: DSI0:</b> DSI_OUT[0]</p> <p><b>0x5: DSI1:</b> DSI_OUT[1]</p> <p><b>0x6: DSI2:</b> DSI_OUT[2]</p> <p><b>0x7: DSI3:</b> DSI_OUT[3]</p>

## 7.1.12 CLK\_ILO\_CONFIG

ILO Configuration

Address: 0x400B0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SATBIAS	TURBO	PD_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator Default Value: 0
2	SATBIAS	PFET bias. Leave this bit at the default setting for normal operation. Engineering only. Default Value: 1  <b>0x0: SATURATED:</b> Enable saturated PFET bias  <b>0x1: SUBTHRESHOLD:</b> Enable subthreshold PFET bias
1	TURBO	Turbo mode for faster startup from coma power down. Leave this bit at the default setting for normal operation. Engineering only. 0: turbo disabled 1: turbo enabled Default Value: 1
0	PD_MODE	Power down mode. Note: this bit must always be set to 0 and never changed. Behavior is undefined when set to 1. Default Value: 0

## 7.1.12 CLK\_ILO\_CONFIG (continued)

**0x0: SLEEP:**

Sleep (faster startup - enables pulsegen block)

**0x1: COMA:**

Coma (slower startup)

## 7.1.13 CLK\_IMO\_CONFIG

IMO Configuration

Address: 0x400B0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	EN_FASTBIAS	FLASHPUMP_SEL	None [21:16]					
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW			RW
HW Access	R	R	R	R	R			R
Name	ENABLE	EN_CLK2X	EN_CLK36	TEST_USB_MODE	PUMP_SEL [27:25]			TEST_FAS_TBIAS

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO but not disconnect it from the power rail. This bit can also be used during IDDQ testing. Default Value: 1
30	EN_CLK2X	Enables main oscillator doubler circuit that can be used for TSS Charge Pumps. This circuit is not available to generate any digital clocks. Default Value: 0
29 and PUMP_SEL3	EN_CLK36	Enables 36MHz secondary oscillator that can be used for Pump or Flash Pump. Note: Since there are two consumers of the 36MHz clock, care should be taken when clearing this bit. The correct procedure for clearing this bit is: 1. Disable interrupts 2. Check if both FLASHPUMP_SEL Default Value: 0

### 7.1.13 CLK\_IMO\_CONFIG (continued)

28	TEST_USB_MODE	<p>Forces IMO into USB mode. Engineering only.</p> <p>1: Software can write FSOFFSET, OFFSET, and GAIN settings for characterization. Hardware updates to these registers are not blocked, so disable USB peripheral updates if they are not desired.</p> <p>0: Normal operation. IMO operates in either USB or non-USB mode, depending on the USB peripheral setting.</p> <p>Default Value: 0</p>
27 : 25	PUMP_SEL	<p>Selects operating source for Pump clock. This clock is not guaranteed to be glitch free when changing IMO parameters or clock divider settings.</p> <p>5-7: reserved, do not use</p> <p>Default Value: 0</p> <p><b>0x0: GND:</b> No clock, connect to gnd</p> <p><b>0x1: IMO:</b> Use main IMO output</p> <p><b>0x2: DBL:</b> Use doubler output</p> <p><b>0x3: CLK36:</b> Use 36MHz oscillator. Note: always set EN_CLK36 when selecting this value for PUMP_SEL. Flash program/erase operations will set EN_CLK36=0 when PUMP_SEL!=CLK36. This selection is ONLY valid for PRoC.</p> <p><b>0x4: FF1:</b> Use divided clock FF1</p>
24	TEST_FASTBIAS	<p>Forces the IMO into FIMO mode (engineering only). Only works when EN_FASTBIAS=1.</p> <p>Default Value: 0</p>
23	EN_FASTBIAS	<p>Forces the FIMO's fast bias circuits to remain powered (engineering only). This bit must be cleared by BootROM after FIMO is no longer required.</p> <p>Default Value: 1</p>
22	FLASHPUMP_SEL	<p>Selects operating source for SPCIF Timer/Flash Pump clock.</p> <p>Default Value: 0</p> <p><b>0x0: GND:</b> No clock, connect to gnd</p> <p><b>0x1: CLK36:</b> Use 36MHz oscillator</p>

## 7.1.14 CLK\_IMO\_SPREAD

IMO Spread Spectrum Configuration

Address: 0x400B010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			SS_VALUE [4:0]				
Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			SS_MAX [12:8]				
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	SS_MODE [31:30]		SS_RANGE [29:28]		None [27:24]			

Bits	Name	Description
31 : 30	SS_MODE	<p>Spread Spectrum Mode. Default Value: 0</p> <p><b>0x0: OFF:</b> Off, do not change SS_VALUE</p> <p><b>0x1: TRIANGLE:</b> Modulate using triangle wave (see SS_MAX)</p> <p><b>0x2: LFSR:</b> Modulate using pseudo random sequence (using LFSR)</p> <p><b>0x3: DSI:</b> Take value directly from DSI (synchronized by divided clock FF1)</p>
29 : 28	SS_RANGE	<p>Spread spectrum range (downspread when SS_VALUE=16). 3: reserved, do not use Default Value: 0</p> <p><b>0x0: M1:</b> 0 .. -1%</p>



## 7.1.14 CLK\_IMO\_SPREAD (continued)

		<b>0x1: M2:</b> 0 .. -2%
		<b>0x2: M4:</b> 0 .. -4%
12 : 8	SS_MAX	Maximum counter value for spread spectrum. Counter will count from 0..SS_MAX..0 and keep repeating this indefinitely. Only works when SS_MODE=1. Default Value: 0
4 : 0	SS_VALUE	Current offset value for spread spectrum modulation. IMO supports values 0..16. Step size is determined by SS_RANGE. Value is encoded in proper thermometric format for IMO in hardware. Value can be modified in firmware only when SS_MODE=0. Default Value: 0

## 7.1.15 CLK\_DFT\_SELECT

Clock DFT Mode Selection Register

Address: 0x400B0110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		DFT_DIV1 [5:4]		DFT_SEL1 [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [15:14]		DFT_DIV2 [13:12]		DFT_SEL2 [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 12	DFT_DIV2	DFT Output Divide Down. Default Value: 0  <b>0x0: NO_DIV:</b> Direct Output  <b>0x1: DIV_BY_2:</b> Divide by 2  <b>0x2: DIV_BY_4:</b> Divide by 4  <b>0x3: DIV_BY_8:</b> Divide by 8
11 : 8	DFT_SEL2	Select signal for DFT output #2. Default Value: 0  <b>0x0: NC:</b> Disabled - output is not connected  <b>0x1: ILO:</b> ILO output

## 7.1.15 CLK\_DFT\_SELECT (continued)

		<b>0x2: WCO:</b> WCO output
		<b>0x3: IMO:</b> IMO primary output
		<b>0x4: ECO:</b> ECO output
		<b>0x5: PLL:</b> PLL output
		<b>0x6: DPLL_OUT:</b> DPLL output
		<b>0x7: DPLL_REF:</b> DPLL reference input
		<b>0x8: DBL:</b> DBL output
		<b>0x9: IMO2X:</b> IMO 2x Clock Output
		<b>0xa: IMO36:</b> IMO 36MHz Clock Output
		<b>0xb: HFCLK:</b> HFCLK
		<b>0xc: LFCLK:</b> LFCLK
		<b>0xd: SYSCLK:</b> SYSCLK
		<b>0xe: EXTCLK:</b> EXTCLK
		<b>0xf: HALFSYSCLK:</b> 0 - removed
5 : 4	DFT_DIV1	DFT Output Divide Down. Default Value: 0
		<b>0x0: NO_DIV:</b> Direct Output
		<b>0x1: DIV_BY_2:</b> Divide by 2
		<b>0x2: DIV_BY_4:</b> Divide by 4
		<b>0x3: DIV_BY_8:</b> Divide by 8
3 : 0	DFT_SEL1	Select signal for DFT output #1. Default Value: 0
		<b>0x0: NC:</b> Disabled - output is not connected
		<b>0x1: ILO:</b> ILO output

### 7.1.15 CLK\_DFT\_SELECT (continued)

**0x2: WCO:**

WCO output

**0x3: IMO:**

IMO primary output

**0x4: ECO:**

ECO output

**0x5: PLL:**

PLL output

**0x6: DPLL\_OUT:**

DPLL output

**0x7: DPLL\_REF:**

DPLL reference input

**0x8: DBL:**

DBL output

**0x9: IMO2X:**

IMO 2x Clock Output

**0xa: IMO36:**

IMO 36MHz Clock Output

**0xb: HFCLK:**

HFCLK

**0xc: LFCLK:**

LFCLK

**0xd: SYSCLK:**

SYSCLK

**0xe: EXTCLK:**

EXTCLK

**0xf: HALFSYSCLK:**

0 - removed

## 7.1.16 WDT\_CTRLLOW

Watchdog Counters 0/1

Address: 0x400B0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTRL0 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTRL0 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTRL1 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTRL1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTRL1	Current value of WDT Counter 1 Default Value: 0
15 : 0	WDT_CTRL0	Current value of WDT Counter 0 Default Value: 0

## 7.1.17 WDT\_CTRHIGH

Watchdog Counter 2

Address: 0x400B0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of WDT Counter 2 Default Value: 0

## 7.1.18 WDT\_MATCH

Watchdog counter match values

Address: 0x400B0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for Watchdog Counter 1 Default Value: 0
15 : 0	WDT_MATCH0	Match value for Watchdog Counter 0 Default Value: 0

## 7.1.19 WDT\_CONFIG

Watchdog Counters Configuration

Address: 0x400B020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CAS CADE0_1	WDT_CLEA R0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CAS CADE1_2	WDT_CLEA R1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_MOD E2

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	LFCLK_SEL [31:30]		None	WDT_BITS2 [28:24]				

Bits	Name	Description
31 : 30	LFCLK_SEL	Select source for LFCLK: 0: ILO - Internal R/C Oscillator 1: WCO - Internal Crystal Oscillator 2-3: Reserved - do not use Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. To safely change LFCLK_SEL wait for WDT_CTLLOW/WDT_CTLHIGH to change then change the setting immediately. Default Value: 0
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert when bit0 of WDT_CTL2 toggles (one int every tick) .. 31: Assert when bit31 of WDT_CTL2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0



## 7.1.19 WDT\_CONFIG (continued)

		<p><b>0x0: NOTHING:</b> Free running counter with no interrupt requests</p> <p><b>0x1: INT:</b> Free running counter with interrupt request when a specified bit in CTR2 toggles (see WDT_BITS2)</p>
11	WDT_CASCADE1_2	<p>Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_MATCH1. It is allowed to cascade all three WDT counters.</p> <p>0: Independent counters 1: Cascaded counters Default Value: 0</p>
10	WDT_CLEAR1	<p>Clear Watchdog Counter when WDT_CTR1=WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1).</p> <p>0: Free running counter 1: Clear on match Default Value: 0</p>
9 : 8	WDT_MODE1	<p>Watchdog Counter Action on Match (WDT_CTR1=WDT_MATCH1). Default Value: 0</p> <p><b>0x0: NOTHING:</b> Do nothing</p> <p><b>0x1: INT:</b> Assert WDT_INTx</p> <p><b>0x2: RESET:</b> Assert WDT Reset</p> <p><b>0x3: INT_THEN_RESET:</b> Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt</p>
3	WDT_CASCADE0_1	<p>Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_MATCH0.</p> <p>0: Independent counters 1: Cascaded counters Default Value: 0</p>
2	WDT_CLEAR0	<p>Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1).</p> <p>0: Free running counter 1: Clear on match Default Value: 0</p>
1 : 0	WDT_MODE0	<p>Watchdog Counter Action on Match (WDT_CTR0=WDT_MATCH0). Default Value: 0</p> <p><b>0x0: NOTHING:</b> Do nothing</p> <p><b>0x1: INT:</b> Assert WDT_INTx</p> <p><b>0x2: RESET:</b> Assert WDT Reset</p> <p><b>0x3: INT_THEN_RESET:</b> Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt</p>

## 7.1.20 WDT\_CONTROL

Watchdog Counters Control

Address: 0x400B0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [7:4]				WDT_RESET0	WDT_INT0	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [15:12]				WDT_RESET1	WDT_INT1	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [23:20]				WDT_RESET2	WDT_INT2	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000_0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
18	WDT_INT2	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to 3 LFCLK cycles. After changing WDT_ENABLE2, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0

## 7.1.20 WDT\_CONTROL (continued)

16	WDT_ENABLE2	<p>Enable Counter 2</p> <p>0: Counter is disabled (not clocked)</p> <p>1: Counter is enabled (counting up)</p> <p>Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period.</p> <p>Default Value: 0</p>
11	WDT_RESET1	<p>Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT.</p> <p>Default Value: 0</p>
10	WDT_INT1	<p>WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt.</p> <p>Default Value: 0</p>
9	WDT_ENABLED1	<p>Indicates actual state of counter. May lag WDT_ENABLE1 by up to 3 LFCLK cycles. After changing WDT_ENABLE1, do not enter DEEPSLEEP mode until this field acknowledges the change.</p> <p>Default Value: 0</p>
8	WDT_ENABLE1	<p>Enable Counter 1</p> <p>0: Counter is disabled (not clocked)</p> <p>1: Counter is enabled (counting up)</p> <p>Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period.</p> <p>Default Value: 0</p>
3	WDT_RESET0	<p>Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT.</p> <p>Default Value: 0</p>
2	WDT_INT0	<p>WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt.</p> <p>Default Value: 0</p>
1	WDT_ENABLED0	<p>Indicates actual state of counter. May lag WDT_ENABLE0 by up to 3 LFCLK cycles. After changing WDT_ENABLE0, do not enter DEEPSLEEP mode until this field acknowledges the change.</p> <p>Default Value: 0</p>
0	WDT_ENABLE0	<p>Enable Counter 0</p> <p>0: Counter is disabled (not clocked)</p> <p>1: Counter is enabled (counting up)</p> <p>Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period.</p> <p>Default Value: 0</p>

## 7.1.21 RES\_CAUSE

Reset Cause Observation Register

Address: 0x400B0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	RESET_XRES	RESET_PBOD	RESET_HVBOD	RESET_SOFT	RESET_PROT_FAULT	RESET_LOCKUP	RESET_DSOD	RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RESET_XRES	This field is deprecated and will always read 0. Default Value: 0
6	RESET_PBOD	This field is deprecated and will always read 0. Default Value: 0
5	RESET_HVBOD	This field is deprecated and will always read 0. Default Value: 0
4	RESET_SOFT	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0
3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default Value: 0
2	RESET_LOCKUP	This field is deprecated and will always read 0. Cortex-M0 LOCKUP is no longer a reset source. Default Value: 0
1	RESET_DSOD	This field is deprecated and will always read 0. Default Value: 0

### 7.1.21 RES\_CAUSE (continued)

0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default Value: 0
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## 7.1.22 PWR\_BG\_TRIM3

Bandgap Trim Register

Address: 0x400BFF18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW				RW		
HW Access	None	R				R		
Name	None	INL_CROSS_IMO [6:3]				INL_TRIM_IMO [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 3	INL_CROSS_IMO	IMO Irefgen INL cross-over point control for centering curve at 30C. Default Value: 11
2 : 0	INL_TRIM_IMO	IMO Irefgen nonlinear current trim for curvature correction. Default Value: 7

## 7.1.23 PWR\_BG\_TRIM4

Bandgap Trim Register

Address: 0x400BFF1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: 32

## 7.1.24 PWR\_BG\_TRIM5

Bandgap Trim Register

Address: 0x400BFF20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: 32



## 7.1.25 CLK\_ILO\_TRIM

ILO Trim Register

Address: 0x400BFF24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COARSE_TRIM [7:4]				TRIM [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COARSE_TRIM	<p>Adjusts the bias in the event of high current after fab. Leave these bits at the default setting for normal operation.:</p> <p>Bias trim:</p> <p>bit3=0: Normal Mode</p> <p>bit3=1:Low Current Mode</p> <p>Resistor Trim (Short R to gnd):</p> <p>bit2=0: Normal Mode</p> <p>bit2=1: Short R/4</p> <p>bit1=0: Unshort R/2</p> <p>bit1=1: Normal Mode (Short R/2)</p> <p>bit0=0: Unshort R/4</p> <p>bit0=1: Normal Mode (Short 3R/4)</p> <p>Default Value: 3</p>
3 : 0	TRIM	<p>Trim bits to control frequency</p> <p>0: Minimum frequency</p> <p>15: Maximum frequency</p> <p>Default Value: 8</p>

## 7.1.26 CLK\_IMO\_TRIM1

IMO Trim Register

Address: 0x400BFF28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	OFFSET [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. Default Value: 128

## 7.1.27 CLK\_IMO\_TRIM2

IMO Trim Register

Address: 0x400BFF2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		FREQ [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	FREQ	<p>Frequency to be selected (default 24MHz). Frequencies can be selected from 3..48MHz. When changing this field appropriate values for IMO_CLK_TRIM1, PWR_BG_TRIM4 and PWR_BG_TRIM5 must be selected from trim tables determined at manufacturing time and stored in SFLASH. This process is documented in the SAS under "Clocks - Selecting IMO Frequency". For encoding of this field a lookup table is required, where the frequency increases in 1MHz steps in the regions listed below. Unspecified values have undefined behavior. A complete lookup table is in BROS 001-59652 Sec 4.2.2.</p> <p>[3-12] =&gt; [3MHz-12MHz]  [14-25] =&gt; [13MHz-24MHz]  [27-35] =&gt; [25MHz-33MHz]  [37-43] =&gt; [34MHz-40MHz]  [46-53] =&gt; [41MHz-48MHz]  Default Value: 25</p>

## 7.1.28 CLK\_IMO\_TRIM4

IMO Trim Register

Address: 0x400BFF34

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	RW			R				
Name	FSOFFSET [7:5]			GAIN [4:0]				

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 5	FSOFFSET	Full-speed USB offset. Updated by hardware during USB osclock mode. Can be updated by software when TEST_USB_MODE=1. Otherwise writes are ignored. Engineering only. Default Value: 0
4 : 0	GAIN	Gain for IMO. Typically stored in SFLASH and copied here on boot. Only used during USB mode, either during USB operation or when CLK_IMO_CONFIG.TEST_USB_MODE=1. When not in USB mode, this register is not used and the actual IMO gain is forced to a setting of 0. Default Value: 0

## 7.1.29 PWR\_RSVD\_TRIM

Reserved, unused registers

Address: 0x400BFF38

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				RSVD_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	RSVD_TRIM	Reserved, unused registers. Default Value: 0

## 8 CPU Sub System (CPUSS) Registers



This section discusses the CPUSS registers. It lists all the registers in mapping tables, in address order.

### 8.1 Register Details

Register Name	Address
<a href="#">CPUSS_CONFIG</a>	0x40100000
<a href="#">CPUSS_SYSREQ</a>	0x40100004
<a href="#">CPUSS_SYSARG</a>	0x40100008
<a href="#">CPUSS_INT_SEL</a>	0x40100020
<a href="#">CPUSS_INT_MODE</a>	0x40100024
<a href="#">CPUSS_NMI_MODE</a>	0x40100028
<a href="#">CPUSS_FLASH_CTL</a>	0x40100030
<a href="#">CPUSS_ROM_CTL</a>	0x40100034

## 8.1.1 CPUSS\_CONFIG

Configuration register

Address: 0x40100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							VECT_IN_RAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VECT_IN_RAM	<p>0': Vector Table is located at 0x0000:0000 in flash</p> <p>'1': Vector Table is located at 0x2000:0000 in SRAM</p> <p>Note that vectors for RESET and FAULT are always fetched from ROM. Value in flash/RAM is ignored for these vectors.</p> <p>Default Value: 0</p>

## 8.1.2 CPUSS\_SYSREQ

SYSCALL control register

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	R	RW	RW	None		
HW Access	R	A	RW	A	R	None		
Name	SYSCALL_REQ	HMASTER_0	ROM_ACCESS_EN	PRIVILEGED	DIS_RESET_VECT_REL	None [26:24]		

Bits	Name	Description
31	SYSCALL_REQ	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request. Default Value: 0
30	HMASTER_0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. HW sets this field when the SYSREQ register is written to and SYSCALL_REQ is '0' (the last time it is set is when SW sets SYSCALL_REQ from '0' to '1'). Default Value: 0
29	ROM_ACCESS_EN	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only. Default Value: 1



### 8.1.2 CPUSS\_SYSREQ (continued)

28	PRIVILEGED	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Cypress proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions. Default Value: 1
27	DIS_RESET_VECT_REL	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Flash DfT routines may set this bit to '1' to enable uninhibited read-back of programmed data in the first flash page. Default Value: 0
15 : 0	SYSCALL_COMMAND	Opcode of the system call being requested. Default Value: 0

### 8.1.3 CPUSS\_SYSARG

SYSARG control register

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [31:24]							

Bits	Name	Description
31 : 0	SYSCALL_ARG	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default Value: 0

## 8.1.4 CPUSS\_INT\_SEL

Interrupt multiplexer select register

Address: 0x40100020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	Reserved							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	Reserved							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	Reserved							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	Reserved							

Bits	Name	Description
31 : 0	Reserved	Reserved

## 8.1.5 CPUSS\_INT\_MODE

Reserved register

Address: 0x40100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	Reserved							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	Reserved							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	Reserved							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	Reserved							

Bits	Name	Description
31 : 0	Reserved	Reserved

## 8.1.6 CPUSS\_NMI\_MODE

Reserved register

Address: 0x40100028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							None
HW Access	None							None
Name	None [7:1]							Reserved

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	Reserved	Reserved

## 8.1.7 CPUSS\_FLASH\_CTL

FLASH control register

Address: 0x40100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			PREF_EN	None [3:2]		FLASH_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW1C
Name	None [15:9]							FLASH_INV ALIDATE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLASH_INVALIDATE	1': Invalidates the content of the flash controller's buffers. Default Value: 0
4	PREF_EN	Prefetch enable: '0': disabled. This is a desirable setting when FLASH_WS is "0" or when predictable execution behavior is required. '1': enabled. Default Value: 0
1 : 0	FLASH_WS	Amount of ROM wait states: "0": 0 wait states (fast flash: [0, 24] MHz system frequency, slow flash: [0, 16] MHz system frequency) "1": 1 wait state (fast flash: [24, 48] MHz system frequency, slow flash: [16, 32] MHz system frequency) "2": 2 wait states (slow flash: [32, 48] MHz system frequency) "3": undefined Default Value: 0

## 8.1.8 CPUSS\_ROM\_CTL

ROM control register

Address: 0x40100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ROM_WS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ROM_WS	<p>Amount of ROM wait states:</p> <p>'0': 0 wait states. Use this setting for newer, faster ROM design. Use this setting for older, slower ROM design and frequencies in the range [0, 24] MHz.</p> <p>'1': 1 wait state. Use this setting for older, slower ROM design and frequencies in the range &lt;24, 48] MHz.</p> <p>CPUSSv2 supports two types of ROM memory: an older, slower design (operating at up to 24 MHz) and a newer, faster design (operating at up to 48 MHz). The older design requires 1 wait state for frequencies above 24 MHz. The newer design never requires wait states. All chips after Street Fighter will use the newer design. As a result, all chips after Street Fighter can always use 0 wait states.</p> <p>Default Value: 0</p>

## 9 DMA Controller Registers



This section discusses the DMA Controller registers. It lists all the registers in mapping tables, in address order.

### 9.1 Register Details

Register Name	Address
DMAC_CTL	0x40101000
DMAC_STATUS	0x40101010
DMAC_STATUS_SRC_ADDR	0x40101014
DMAC_STATUS_DST_ADDR	0x40101018
DMAC_STATUS_CH_ACT	0x4010101C
DMAC_CH_CTL0	0x40101080
DMAC_CH_CTL1	0x40101084
DMAC_CH_CTL2	0x40101088
DMAC_CH_CTL3	0x4010108C
DMAC_CH_CTL4	0x40101090
DMAC_CH_CTL5	0x40101094
DMAC_CH_CTL6	0x40101098
DMAC_CH_CTL7	0x4010109C
DMAC_INTR	0x401017F0
DMAC_INTR_SET	0x401017F4
DMAC_INTR_MASK	0x401017F8
DMAC_INTR_MASKED	0x401017FC



## 9.1.1 DMAC\_CTL

Control register

Address: 0x40101000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	<p>0': IP is disabled. Non-retainable MMIO registers and logic functionality are reset (retainable MMIO registers are NOT reset):</p> <ul style="list-style-type: none"> <li>- INTR register is set to "0".</li> <li>- DW/DMA functionality is aborted.</li> <li>- DW/DMA controller input/pending triggers are de-activated.</li> <li>- DW/DMA controller output triggers are de-activated.</li> </ul> <p>Disabling the IP has the same effect as an active "rst_sys_act_n" reset in DeepSleep power mode. To prevent a loss of active (pending) DW/DMA triggers when disabling the IP or when transitioning from Active to DeepSleep power mode, the STATUS.ACTIVE and STATUS_CH_ACTIVE.CH fields can be used.</p> <p>Note that most MMIO registers are retainable, and a transition from DeepSleep to Active/Sleep power modes makes the DW/DMA controller operational, and ready to react to DW/DMA input triggers that are activated after the transition. Triggers are Active/Sleep functionality.</p> <p>'1': IP is enabled.</p> <p>Default Value: 0</p>

## 9.1.2 DMAC\_STATUS

Status register

Address: 0x40101010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					CH_ADDR [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R		None	R		
HW Access	W	W	W		None	W		
Name	ACTIVE	PING_PONG	PRIO [29:28]		None	STATE [26:24]		

Bits	Name	Description
31	ACTIVE	Specifies if there is a currently active (pending) channel in the data transfer engine: 0: no currently active channel. 1: currently active channel. Default Value: 0
30	PING_PONG	Specifies whether the PING descriptor (0) or PONG descriptor (1) of the channel is currently in use. Default Value: Undefined
29 : 28	PRIO	Specifies the priority of the currently active channel. Default Value: Undefined
26 : 24	STATE	State of the data transfer engine. 0: DEFAULT state. 1: Loading descriptor (SRC, DST, CONTROL and STATUS words). 2: Loading data element from source location. 3: Storing data element to destination location. 4: Storing descriptor (STATUS word). 5: Wait for trigger de-activation. 6: Storing descriptor with error response (STATUS word). Default Value: 0

### 9.1.2 DMAC\_STATUS (continued)

18 : 16	CH_ADDR	Specifies the channel number of the currently active channel. E.g. if we have 32 channels, the channel number address with CH_ADDR_WIDTH is $\text{LOG}_2(32) = 5$ , and this field is a 5-bit field. If channel 7 is active, STATUS.ACTIVE is '1' and STATUS.CH_ADDR is "7". Default Value: Undefined
15 : 0	DATA_NR	Specifies the index of the currently active data transfer. This value increases from "0" to CONTROL.DATA_NR. Default Value: Undefined

### 9.1.3 DMAC\_STATUS\_SRC\_ADDR

Source address status register

Address: 0x40101014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of source location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

## 9.1.4 DMAC\_STATUS\_DST\_ADDR

Destination address register

Address: 0x40101018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of destination location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

## 9.1.5 DMAC\_STATUS\_CH\_ACT

Channel activation status register

Address: 0x4010101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Channel activation status. Bit i is associated to channel i, with i = 0, , CH_NR-1.  Software reads this field to get information on all actively pending channels (either in pending or in the data transfer engine). Default Value: 0

## 9.1.6 DMAC\_CH\_CTL0

Channel control register

Address: 0x40101080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.6 DMAC\_CH\_CTL0 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index <i>i</i>, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>



## 9.1.7 DMAC\_CH\_CTL1

Channel control register

Address: 0x40101084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.7 DMAC\_CH\_CTL1 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>

## 9.1.8 DMAC\_CH\_CTL2

Channel control register

Address: 0x40101088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.8 DMAC\_CH\_CTL2 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>

## 9.1.9 DMAC\_CH\_CTL3

Channel control register

Address: 0x4010108C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.9 DMAC\_CH\_CTL3 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index <i>i</i>, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>

## 9.1.10 DMAC\_CH\_CTL4

Channel control register

Address: 0x40101090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.10 DMAC\_CH\_CTL4 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>



## 9.1.11 DMAC\_CH\_CTL5

Channel control register

Address: 0x40101094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.11 DMAC\_CH\_CTL5 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>

## 9.1.12 DMAC\_CH\_CTL6

Channel control register

Address: 0x40101098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.12 DMAC\_CH\_CTL6 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>

## 9.1.13 DMAC\_CH\_CTL7

Channel control register

Address: 0x4010109C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	<p>0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled.</p> <p>Software sets this field to 1 to enable a specific channel.</p> <p>Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0</p>

### 9.1.13 DMAC\_CH\_CTL7 (continued)

30	PING_PONG	<p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Software sets this field to the desired descriptor structure.</p> <p>Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1.</p> <p>Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller.</p> <p>Default Value: 0</p>
29 : 28	PRI0	<p>Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index <i>i</i>, is considered the highest priority activated channel.</p> <p>Default Value: 0</p>

## 9.1.14 DMAC\_INTR

Interrupt register

Address: 0x401017F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CH [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

## 9.1.15 DMAC\_INTR\_SET

Interrupt set register

Address: 0x401017F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	CH [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0



## 9.1.16 DMAC\_INTR\_MASK

Interrupt mask register

Address: 0x401017F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CH [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Mask for corresponding field in INTR register. Default Value: 0

## 9.1.17 DMAC\_INTR\_MASKED

Interrupt masked register

Address: 0x401017FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Logical and of corresponding request and mask fields. Default Value: 0

# 10 DMA Descriptor Registers



This section discusses the DMA Descriptor registers. It lists all the registers in mapping tables, in address order.

## 10.1 Register Details

Register Name	Address
DMAC_DESCR0_PING_SRC	0x40101800
DMAC_DESCR0_PING_DST	0x40101804
DMAC_DESCR0_PING_CTL	0x40101808
DMAC_DESCR0_PING_STATUS	0x4010180C
DMAC_DESCR0_PONG_SRC	0x40101810
DMAC_DESCR0_PONG_DST	0x40101814
DMAC_DESCR0_PONG_CTL	0x40101818
DMAC_DESCR0_PONG_STATUS	0x4010181C
DMAC_DESCR1_PING_SRC	0x40101820
DMAC_DESCR1_PING_DST	0x40101824
DMAC_DESCR1_PING_CTL	0x40101828
DMAC_DESCR1_PING_STATUS	0x4010182C
DMAC_DESCR1_PONG_SRC	0x40101830
DMAC_DESCR1_PONG_DST	0x40101834
DMAC_DESCR1_PONG_CTL	0x40101838
DMAC_DESCR1_PONG_STATUS	0x4010183C
DMAC_DESCR2_PING_SRC	0x40101840
DMAC_DESCR2_PING_DST	0x40101844
DMAC_DESCR2_PING_CTL	0x40101848
DMAC_DESCR2_PING_STATUS	0x4010184C
DMAC_DESCR2_PONG_SRC	0x40101850
DMAC_DESCR2_PONG_DST	0x40101854
DMAC_DESCR2_PONG_CTL	0x40101858
DMAC_DESCR2_PONG_STATUS	0x4010185C
DMAC_DESCR3_PING_SRC	0x40101860
DMAC_DESCR3_PING_DST	0x40101864
DMAC_DESCR3_PING_CTL	0x40101868

Register Name	Address
DMAC_DESCR3_PING_STATUS	0x4010186C
DMAC_DESCR3_PONG_SRC	0x40101870
DMAC_DESCR3_PONG_DST	0x40101874
DMAC_DESCR3_PONG_CTL	0x40101878
DMAC_DESCR3_PONG_STATUS	0x4010187C
DMAC_DESCR4_PING_SRC	0x40101880
DMAC_DESCR4_PING_DST	0x40101884
DMAC_DESCR4_PING_CTL	0x40101888
DMAC_DESCR4_PING_STATUS	0x4010188C
DMAC_DESCR4_PONG_SRC	0x40101890
DMAC_DESCR4_PONG_DST	0x40101894
DMAC_DESCR4_PONG_CTL	0x40101898
DMAC_DESCR4_PONG_STATUS	0x4010189C
DMAC_DESCR5_PING_SRC	0x401018A0
DMAC_DESCR5_PING_DST	0x401018A4
DMAC_DESCR5_PING_CTL	0x401018A8
DMAC_DESCR5_PING_STATUS	0x401018AC
DMAC_DESCR5_PONG_SRC	0x401018B0
DMAC_DESCR5_PONG_DST	0x401018B4
DMAC_DESCR5_PONG_CTL	0x401018B8
DMAC_DESCR5_PONG_STATUS	0x401018BC
DMAC_DESCR6_PING_SRC	0x401018C0
DMAC_DESCR6_PING_DST	0x401018C4
DMAC_DESCR6_PING_CTL	0x401018C8
DMAC_DESCR6_PING_STATUS	0x401018CC
DMAC_DESCR6_PONG_SRC	0x401018D0
DMAC_DESCR6_PONG_DST	0x401018D4
DMAC_DESCR6_PONG_CTL	0x401018D8
DMAC_DESCR6_PONG_STATUS	0x401018DC
DMAC_DESCR7_PING_SRC	0x401018E0
DMAC_DESCR7_PING_DST	0x401018E4
DMAC_DESCR7_PING_CTL	0x401018E8
DMAC_DESCR7_PING_STATUS	0x401018EC
DMAC_DESCR7_PONG_SRC	0x401018F0
DMAC_DESCR7_PONG_DST	0x401018F4
DMAC_DESCR7_PONG_CTL	0x401018F8
DMAC_DESCR7_PONG_STATUS	0x401018FC

## 10.1.1 DMAC\_DESCR0\_PING\_SRC

Ping source address

Address: 0x40101800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.2 DMAC\_DESCR0\_PING\_DST

Ping destination address

Address: 0x40101804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

### 10.1.3 DMAC\_DESCR0\_PING\_CTL

Ping control word

Address: 0x40101808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

**Bits**      **Name**      **Description**

### 10.1.3 DMAC\_DESCR0\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHI_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHI_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>



### 10.1.3 DMAC\_DESCR0\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>

### 10.1.3 DMAC\_DESCR0\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>

## 10.1.4 DMAC\_DESCR0\_PING\_STATUS

Ping status word

Address: 0x4010180C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1).</p> <p>1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized.</p> <p>Default Value: Undefined</p>

## 10.1.4 DMAC\_DESCR0\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP-PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined

## 10.1.5 DMAC\_DESCR0\_PONG\_SRC

Pong source address

Address: 0x40101810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

## 10.1.6 DMAC\_DESCR0\_PONG\_DST

Pong destination address

Address: 0x40101814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

## 10.1.7 DMAC\_DESCR0\_PONG\_CTL

Pong control word

Address: 0x40101818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

### 10.1.7 DMAC\_DESCR0\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined



## 10.1.8 DMAC\_DESCR0\_PONG\_STATUS

Pong status word

Address: 0x4010181C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

## 10.1.9 DMAC\_DESCR1\_PING\_SRC

Ping source address

Address: 0x40101820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.10 DMAC\_DESCR1\_PING\_DST

Ping destination address

Address: 0x40101824

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.11 DMAC\_DESCR1\_PING\_CTL

Ping control word

Address: 0x40101828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
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### 10.1.11 DMAC\_DESCR1\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>

### 10.1.11 DMAC\_DESCR1\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>

### 10.1.11 DMAC\_DESCR1\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>

## 10.1.12 DMAC\_DESCR1\_PING\_STATUS

Ping status word

Address: 0x4010182C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1).</p> <p>1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized.</p> <p>Default Value: Undefined</p>



## 10.1.12 DMAC\_DESCR1\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP\_PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined

### 10.1.13 DMAC\_DESCR1\_PONG\_SRC

Pong source address

Address: 0x40101830

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

## 10.1.14 DMAC\_DESCR1\_PONG\_DST

Pong destination address

Address: 0x40101834

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

## 10.1.15 DMAC\_DESCR1\_PONG\_CTL

Pong control word

Address: 0x40101838

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

### 10.1.15 DMAC\_DESCR1\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

## 10.1.16 DMAC\_DESCR1\_PONG\_STATUS

Pong status word

Address: 0x4010183C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

## 10.1.17 DMAC\_DESCR2\_PING\_SRC

Ping source address

Address: 0x40101840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.18 DMAC\_DESCR2\_PING\_DST

Ping destination address

Address: 0x40101844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined



## 10.1.19 DMAC\_DESCR2\_PING\_CTL

Ping control word

Address: 0x40101848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
------	------	-------------

### 10.1.19 DMAC\_DESCR2\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>

### 10.1.19 DMAC\_DESCR2\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>

### 10.1.19 DMAC\_DESCR2\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>

## 10.1.20 DMAC\_DESCR2\_PING\_STATUS

Ping status word

Address: 0x4010184C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined</p>

## 10.1.20 DMAC\_DESCR2\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP-PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined

## 10.1.21 DMAC\_DESCR2\_PONG\_SRC

Pong source address

Address: 0x40101850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

## 10.1.22 DMAC\_DESCR2\_PONG\_DST

Pong destination address

Address: 0x40101854

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined



## 10.1.23 DMAC\_DESCR2\_PONG\_CTL

Pong control word

Address: 0x40101858

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

### 10.1.23 DMAC\_DESCR2\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

## 10.1.24 DMAC\_DESCR2\_PONG\_STATUS

Pong status word

Address: 0x4010185C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

## 10.1.25 DMAC\_DESCR3\_PING\_SRC

Ping source address

Address: 0x40101860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.26 DMAC\_DESCR3\_PING\_DST

Ping destination address

Address: 0x40101864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.27 DMAC\_DESCR3\_PING\_CTL

Ping control word

Address: 0x40101868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
------	------	-------------

## 10.1.27 DMAC\_DESCR3\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>

## 10.1.27 DMAC\_DESCR3\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>



### 10.1.27 DMAC\_DESCR3\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>

## 10.1.28 DMAC\_DESCR3\_PING\_STATUS

Ping status word

Address: 0x4010186C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1).</p> <p>1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized.</p> <p>Default Value: Undefined</p>

## 10.1.28 DMAC\_DESCR3\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP-PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined

## 10.1.29 DMAC\_DESCR3\_PONG\_SRC

Pong source address

Address: 0x40101870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

### 10.1.30 DMAC\_DESCR3\_PONG\_DST

Pong destination address

Address: 0x40101874

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

### 10.1.31 DMAC\_DESCR3\_PONG\_CTL

Pong control word

Address: 0x40101878

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

### 10.1.31 DMAC\_DESCR3\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

## 10.1.32 DMAC\_DESCR3\_PONG\_STATUS

Pong status word

Address: 0x4010187C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined



### 10.1.33 DMAC\_DESCR4\_PING\_SRC

Ping source address

Address: 0x40101880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

### 10.1.34 DMAC\_DESCR4\_PING\_DST

Ping destination address

Address: 0x40101884

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.35 DMAC\_DESCR4\_PING\_CTL

Ping control word

Address: 0x40101888

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
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### 10.1.35 DMAC\_DESCR4\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>

### 10.1.35 DMAC\_DESCR4\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>

### 10.1.35 DMAC\_DESCR4\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>

## 10.1.36 DMAC\_DESCR4\_PING\_STATUS

Ping status word

Address: 0x4010188C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1).</p> <p>1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized.</p> <p>Default Value: Undefined</p>

### 10.1.36 DMAC\_DESCR4\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP-PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined



## 10.1.37 DMAC\_DESCR4\_PONG\_SRC

Pong source address

Address: 0x40101890

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

## 10.1.38 DMAC\_DESCR4\_PONG\_DST

Pong destination address

Address: 0x40101894

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

## 10.1.39 DMAC\_DESCR4\_PONG\_CTL

Pong control word

Address: 0x40101898

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

### 10.1.39 DMAC\_DESCR4\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

## 10.1.40 DMAC\_DESCR4\_PONG\_STATUS

Pong status word

Address: 0x4010189C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

## 10.1.41 DMAC\_DESCR5\_PING\_SRC

Ping source address

Address: 0x401018A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.42 DMAC\_DESCR5\_PING\_DST

Ping destination address

Address: 0x401018A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.43 DMAC\_DESCR5\_PING\_CTL

Ping control word

Address: 0x401018A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
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### 10.1.43 DMAC\_DESCR5\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>

### 10.1.43 DMAC\_DESCR5\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>

### 10.1.43 DMAC\_DESCR5\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>

## 10.1.44 DMAC\_DESCR5\_PING\_STATUS

Ping status word

Address: 0x401018AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1).</p> <p>1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized.</p> <p>Default Value: Undefined</p>

## 10.1.44 DMAC\_DESCR5\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP\_PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined

## 10.1.45 DMAC\_DESCR5\_PONG\_SRC

Pong source address

Address: 0x401018B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

## 10.1.46 DMAC\_DESCR5\_PONG\_DST

Pong destination address

Address: 0x401018B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

## 10.1.47 DMAC\_DESCR5\_PONG\_CTL

Pong control word

Address: 0x401018B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined



#### 10.1.47 DMAC\_DESCR5\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

## 10.1.48 DMAC\_DESCR5\_PONG\_STATUS

Pong status word

Address: 0x401018BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

## 10.1.49 DMAC\_DESCR6\_PING\_SRC

Ping source address

Address: 0x401018C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.50 DMAC\_DESCR6\_PING\_DST

Ping destination address

Address: 0x401018C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.51 DMAC\_DESCR6\_PING\_CTL

Ping control word

Address: 0x401018C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
------	------	-------------

### 10.1.51 DMAC\_DESCR6\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>

### 10.1.51 DMAC\_DESCR6\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>

### 10.1.51 DMAC\_DESCR6\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>



## 10.1.52 DMAC\_DESCR6\_PING\_STATUS

Ping status word

Address: 0x401018CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1).</p> <p>1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized.</p> <p>Default Value: Undefined</p>

## 10.1.52 DMAC\_DESCR6\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP-PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined

## 10.1.53 DMAC\_DESCR6\_PONG\_SRC

Pong source address

Address: 0x401018D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

## 10.1.54 DMAC\_DESCR6\_PONG\_DST

Pong destination address

Address: 0x401018D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

## 10.1.55 DMAC\_DESCR6\_PONG\_CTL

Pong control word

Address: 0x401018D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

### 10.1.55 DMAC\_DESCR6\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

## 10.1.56 DMAC\_DESCR6\_PONG\_STATUS

Pong status word

Address: 0x401018DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

## 10.1.57 DMAC\_DESCR7\_PING\_SRC

Ping source address

Address: 0x401018E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined



## 10.1.58 DMAC\_DESCR7\_PING\_DST

Ping destination address

Address: 0x401018E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

## 10.1.59 DMAC\_DESCR7\_PING\_CTL

Ping control word

Address: 0x401018E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

**Bits**      **Name**      **Description**

### 10.1.59 DMAC\_DESCR7\_PING\_CTL (continued)

31 : 30	OPCODE	<p>Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1):</p> <p>0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1).</p> <p>1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed.</p> <p>2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHI_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer).</p> <p>After completion of the opcode (and waiting for de-activation, the channel's output trigger is activated).</p> <p>Default Value: Undefined</p>
29	FLIPPING	<p>1: On completion of the current descriptor structure, the current descriptor identifier CHI_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures.</p> <p>Default Value: Undefined</p>
28	PREEMPTABLE	<p>1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled.</p> <p>Default Value: Undefined</p>
27	SET_CAUSE	<p>1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]).</p> <p>Default Value: Undefined</p>
26	INV_DESCR	<p>1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0.</p> <p>Default Value: Undefined</p>

### 10.1.59 DMAC\_DESCR7\_PING\_CTL (continued)

25 : 24	WAIT_FOR_DEACT	<p>Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance.</p> <p>0: Do not wait for de-activation (for pulse sensitive triggers).</p> <p>1: Wait for up to 4 cycles.</p> <p>2: Wait for up to 8 cycles.</p> <p>3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent.</p> <p>Default Value: Undefined</p>
23	SRC_ADDR_INCR	<p>Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0: No increment, typically used for receive (RX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
22	SRC_TRANSFER_SIZE	<p>Specifies the bus transfer size to the source location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element.</p> <p>Default Value: Undefined</p>
21	DST_ADDR_INCR	<p>Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not.</p> <p>0 : No increment, typically used for transmit (TX) FIFO structures.</p> <p>1: Increment, typically used for memory structures.</p> <p>Default Value: Undefined</p>
20	DST_TRANSFER_SIZE	<p>Specifies the bus transfer size to the destination location:</p> <p>0: As specified by DATA_SIZE.</p> <p>1: Word (32 bits).</p> <p>Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element.</p> <p>Default Value: Undefined</p>

### 10.1.59 DMAC\_DESCR7\_PING\_CTL (continued)

17 : 16	DATA_SIZE	<p>Specifies the data element size:</p> <p>0: Byte (8 bits).</p> <p>1: Halfword (16 bits).</p> <p>2: Word (32 bits).</p> <p>DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings:</p> <ul style="list-style-type: none"> <li>- DATA is 8 bit, SRC is 8 bit, DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit</li> <li>- DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit</li> <li>- DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0)</li> <li>- DATA is 32 bit, SRC is 32 bit, DST is 32 bit</li> </ul> <p>Default Value: Undefined</p>
15 : 0	DATA_NR	<p>Number of data elements that are transferred by a single descriptor.</p> <p>In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure.</p> <p>In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements.</p> <p>Default Value: Undefined</p>

## 10.1.60 DMAC\_DESCR7\_PING\_STATUS

Ping status word

Address: 0x401018EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	<p>0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1).</p> <p>1: Valid.</p> <p>Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1.</p> <p>Software sets this field to 1 when a descriptor is initialized.</p> <p>Default Value: Undefined</p>

## 10.1.60 DMAC\_DESCR7\_PING\_STATUS (continued)

18 : 16 RESPONSE

Response code (the first two codes NO\_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior).

0/NO\_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO\_ERROR during descriptor initialization.

1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET\_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV\_DESCR is 1. CHi\_CTL.ENABLED is NOT affected. CHi\_CTL.PING\_PONG is updated if CONTROL.FLIP-PING is 1.

2/SRC\_BUS\_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

3/DST\_BUS\_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

4/SRC\_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

5/DST\_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi\_CTL.ENABLED is set to 0.

CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

6/INVALID\_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi\_CTL.ENABLED is set to 0. CHi\_CTL.PING\_PONG is not updated (it identifies the descriptor that caused the error).

Default Value: Undefined

15 : 0 CURR\_DATA\_NR

Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA\_NR. HW sets this field:

- When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING\_CTL.INV\_DESCR is '0' and the field is set to PING\_CTL.DATA\_NR when PING\_CTL.INV\_DESCR is '1'.

- When a descriptor is not done (RESPONSE is NO\_ERROR), the field reflects the progress of a data transfer.

- In case of erroneous behavior (RESPONSE is neither DONE or NO\_ERROR), the field is not updated, but keeps its value to ease debugging.

HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0.

This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR\_DATA\_NR is modified during data transfer and provides an offset wrt. the base addresses.

Default Value: Undefined

## 10.1.61 DMAC\_DESCR7\_PONG\_SRC

Pong source address

Address: 0x401018F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined



## 10.1.62 DMAC\_DESCR7\_PONG\_DST

Pong destination address

Address: 0x401018F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

## 10.1.63 DMAC\_DESCR7\_PONG\_CTL

Pong control word

Address: 0x401018F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	
Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPTABLE	SET_CAUSE	INV_DESCRIPTOR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCRIPTOR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

### 10.1.63 DMAC\_DESCR7\_PONG\_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

## 10.1.64 DMAC\_DESCR7\_PONG\_STATUS

Pong status word

Address: 0x401018FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

# 11 CapSense Sigma Delta (CSD) Registers



This section discusses the CSD registers. It lists all the registers in mapping tables, in address order.

## 11.1 Register Details

Register Name	Address
<a href="#">CSD_ID</a>	0x40280000
<a href="#">CSD_INTR</a>	0x40280014
<a href="#">CSD_INTR_SET</a>	0x40280018
<a href="#">CSD_PWM</a>	0x4028001C

## 11.1.1 CSD\_ID

ID & Revision Number

Address: 0x40280000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of CSD peripheral is 0xE0E1 Default Value: 57569

## 11.1.2 CSD\_INTR

CSD Interrupt Request Register

Address: 0x40280014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	The CSD IRQ bit is set. Firmware must clear this bit as part of the interrupt handler. Default Value: 0

### 11.1.3 CSD\_INTR\_SET

CSD Interrupt set register

Address: 0x40280018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	Only for debug/test purpose this field can be set to '1' to set corresponding bit in interrupt request register INTR. Default Value: 0



## 11.1.4 CSD\_PWM

CSD PWM Register

Address: 0x4028001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		PWM_SEL [5:4]		PWM_COUNT [3:0]			

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	PWM_SEL	<p>The mode of the PWM modulator</p> <p>Default Value: 0</p> <p><b>0x0: OFF:</b></p> <p>The PWM modulator is OFF and it has no effect on sensor clock generated by PRS/divide-by-2</p> <p><b>0x2: FIXED_HIGH:</b></p> <p>The PWM modulator changes the low phase of sensor clock to a fixed length (used during negative charge transfer mode).</p> <p><b>0x3: FIXED_LOW:</b></p> <p>The PWM modulator changes the high phase of sensor clock to a fixed length (used during positive charge transfer mode).</p>
3 : 0	PWM_COUNT	<p>Pulse width modulation can be used to change the length of sensor clock pulse (low time/high time) when using PRS/Divide-by-2 as source of sensor clock. The length of the sensor clock pulse low/high time is multiples of clk_csd2 cycles.</p> <p>Default Value: 0</p>

# 12 GPIO Registers



This section discusses the GPIO registers. It lists all the registers in mapping tables, in address order.

---

## 12.1 Register Details

Register Name	Address
<a href="#">GPIO_INTR_CAUSE</a>	0x40041000

## 12.1.1 GPIO\_INTR\_CAUSE

Interrupt port cause register

Address: 0x40041000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	PORT_INT [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a shared/combined interrupt line "gpio_interrupt". The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line "gpio_interrupt". Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt. Default Value: 0

# 13 GPIO Port Registers



This section discusses the GPIO Port registers. It lists all the registers in mapping tables, in address order.

## 13.1 Register Details

Register Name	Address
<a href="#">GPIO_PRT0_DR</a>	0x40040000
<a href="#">GPIO_PRT0_PS</a>	0x40040004
<a href="#">GPIO_PRT0_PC</a>	0x40040008
<a href="#">GPIO_PRT0_INTR_CFG</a>	0x4004000C
<a href="#">GPIO_PRT0_INTR</a>	0x40040010
<a href="#">GPIO_PRT0_PC2</a>	0x40040018
<a href="#">GPIO_PRT0_DR_SET</a>	0x40040040
<a href="#">GPIO_PRT0_DR_CLR</a>	0x40040044
<a href="#">GPIO_PRT0_DR_INV</a>	0x40040048
<a href="#">GPIO_PRT1_DR</a>	0x40040100
<a href="#">GPIO_PRT1_PS</a>	0x40040104
<a href="#">GPIO_PRT1_PC</a>	0x40040108
<a href="#">GPIO_PRT1_INTR_CFG</a>	0x4004010C
<a href="#">GPIO_PRT1_INTR</a>	0x40040110
<a href="#">GPIO_PRT1_PC2</a>	0x40040118
<a href="#">GPIO_PRT1_DR_SET</a>	0x40040140
<a href="#">GPIO_PRT1_DR_CLR</a>	0x40040144
<a href="#">GPIO_PRT1_DR_INV</a>	0x40040148
<a href="#">GPIO_PRT2_DR</a>	0x40040200
<a href="#">GPIO_PRT2_PS</a>	0x40040204
<a href="#">GPIO_PRT2_PC</a>	0x40040208
<a href="#">GPIO_PRT2_INTR_CFG</a>	0x4004020C
<a href="#">GPIO_PRT2_INTR</a>	0x40040210
<a href="#">GPIO_PRT2_PC2</a>	0x40040218
<a href="#">GPIO_PRT2_DR_SET</a>	0x40040240
<a href="#">GPIO_PRT2_DR_CLR</a>	0x40040244
<a href="#">GPIO_PRT2_DR_INV</a>	0x40040248

Register Name	Address
GPIO_PRT3_DR	0x40040300
GPIO_PRT3_PS	0x40040304
GPIO_PRT3_PC	0x40040308
GPIO_PRT3_INTR_CFG	0x4004030C
GPIO_PRT3_INTR	0x40040310
GPIO_PRT3_PC2	0x40040318
GPIO_PRT3_DR_SET	0x40040340
GPIO_PRT3_DR_CLR	0x40040344
GPIO_PRT3_DR_INV	0x40040348
GPIO_PRT4_DR	0x40040400
GPIO_PRT4_PS	0x40040404
GPIO_PRT4_PC	0x40040408
GPIO_PRT4_INTR_CFG	0x4004040C
GPIO_PRT4_INTR	0x40040410
GPIO_PRT4_PC2	0x40040418
GPIO_PRT4_DR_SET	0x40040440
GPIO_PRT4_DR_CLR	0x40040444
GPIO_PRT4_DR_INV	0x40040448
GPIO_PRT5_DR	0x40040500
GPIO_PRT5_PS	0x40040504
GPIO_PRT5_PC	0x40040508
GPIO_PRT5_INTR_CFG	0x4004050C
GPIO_PRT5_INTR	0x40040510
GPIO_PRT5_PC2	0x40040518
GPIO_PRT5_DR_SET	0x40040540
GPIO_PRT5_DR_CLR	0x40040544
GPIO_PRT5_DR_INV	0x40040548
GPIO_PRT6_DR	0x40040600
GPIO_PRT6_PS	0x40040604
GPIO_PRT6_PC	0x40040608
GPIO_PRT6_INTR_CFG	0x4004060C
GPIO_PRT6_INTR	0x40040610
GPIO_PRT6_PC2	0x40040618
GPIO_PRT6_DR_SET	0x40040640
GPIO_PRT6_DR_CLR	0x40040644
GPIO_PRT6_DR_INV	0x40040648

## 13.1.1 GPIO\_PRT0\_DR

Port output data register

Address: 0x40040000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

## 13.1.2 GPIO\_PRT0\_PS

Port IO pad state register

Address: 0x40040004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

### 13.1.2 GPIO\_PRT0\_PS (continued)

0	DATA0	<p>IO pad 0 state:</p> <p>1: Logic high, if the pin voltage is above the input buffer threshold, logic high.</p> <p>0: Logic low, if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> <p>Default Value: 0</p>
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### 13.1.3 GPIO\_PRT0\_PC

Port configuration register

Address: 0x40040008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

  

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

  

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None			RW		RW
HW Access	R		None			R		R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]			PORT_SLOW		PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	<p>This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell.</p> <p>For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell):</p> <p>"0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1"/"3": vcchib.</p> <p>For GPIO_OVTV2 and SIOv2 IO cells:</p> <p>"0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1": vcchib.</p> <p>"2": OVT.</p> <p>"3": Reference (possibly from reference generator cell).</p> <p>For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available).</p> <p>Default Value: 0</p>
25	PORT_SLOW	<p>This field controls the output edge rate of all pins on the port:</p> <p>'0': fast.</p> <p>'1': slow.</p> <p>Default Value: 0</p>

### 13.1.3 GPIO\_PRT0\_PC (continued)

		<p><b>0x0: PORT_SLEW_CTL_0:</b>  HS mode (100pf &lt; Cb &lt; 400pF, 1.71&lt;5.5, Vext&gt;3.0)  FS mode (10pf&lt;400pf,1.71&lt;5.5) (20-160ns)</p> <p><b>0x1: PORT_SLEW_CTL_1:</b>  HS mode (Cb&lt;100pf,1.71&lt;5.5,Vext&gt;2.8,F=1.7MHz) (10-80ns)  FS+ Mode (Vext&gt;2.8,1.71&lt;5.5) (20-120ns)</p> <p><b>0x2: PORT_SLEW_CTL_2:</b>  HS mode (100pf&lt;400pf, 1.71&lt;5.5,Vext&lt;3.3) (20-160ns)</p> <p><b>0x3: PORT_SLEW_CTL_3:</b>  HS mode (Cb&lt;100pf,1.71&lt;5.5,Vext&lt;=2.8,F=1.7MHz) (10-80ns)  FS+ mode (Vext&lt;=2.8,1.71&lt;5.5) (20-120ns)</p>
24	PORT_VTRIP_SEL	<p>The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair).</p> <p>0: input buffer functions as a CMOS input buffer.  1: input buffer functions as a LVTTL input buffer.  Default Value: 0</p>
23 : 21	DM7	<p>The GPIO drive mode for IO pad 7.  Default Value: 0</p>
20 : 18	DM6	<p>The GPIO drive mode for IO pad 6.  Default Value: 0</p>
17 : 15	DM5	<p>The GPIO drive mode for IO pad 5.  Default Value: 0</p>
14 : 12	DM4	<p>The GPIO drive mode for IO pad 4.  Default Value: 0</p>
11 : 9	DM3	<p>The GPIO drive mode for IO pad 3.  Default Value: 0</p>
8 : 6	DM2	<p>The GPIO drive mode for IO pad 2.  Default Value: 0</p>
5 : 3	DM1	<p>The GPIO drive mode for IO pad 1.  Default Value: 0</p>
2 : 0	DM0	<p>The GPIO drive mode for IO pad 0.  Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus.  Default Value: 0</p> <p><b>0x0: OFF:</b>  Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.</p> <p><b>0x1: INPUT:</b>  Mode 1: Output buffer off (high Z). Input buffer on.</p> <p><b>0x2: 0_PU:</b>  Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.</p> <p><b>0x3: PD_1:</b>  Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.</p> <p><b>0x4: 0_Z:</b>  Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.</p>

### 13.1.3 GPIO\_PRT0\_PC (continued)

**0x5: Z\_1:**

Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

**0x6: 0\_1:**

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

**0x7: PD\_PU:**

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

## 13.1.4 GPIO\_PRT0\_INTR\_CFG

Port interrupt configuration register

Address: 0x4004000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0  <b>0x0: DISABLE:</b> Disabled  <b>0x1: RISING:</b> Rising edge  <b>0x2: FALLING:</b> Falling edge  <b>0x3: BOTH:</b> Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

### 13.1.4 GPIO\_PRT0\_INTR\_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

**0x0: DISABLE:**

Disabled

**0x1: RISING:**

Rising edge

**0x2: FALLING:**

Falling edge

**0x3: BOTH:**

Both rising and falling edges

## 13.1.5 GPIO\_PRT0\_INTR

Port interrupt status register

Address: 0x40040010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

  

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

### 13.1.5 GPIO\_PRT0\_INTR (continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

## 13.1.6 GPIO\_PRT0\_PC2

Port configuration register 2

Address: 0x40040018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0



### 13.1.6 GPIO\_PRT0\_PC2 (continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0
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## 13.1.7 GPIO\_PRT0\_DR\_SET

Port output data set register

Address: 0x40040040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

## 13.1.8 GPIO\_PRT0\_DR\_CLR

Port output data clear register

Address: 0x40040044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

## 13.1.9 GPIO\_PRT0\_DR\_INV

Port output data invert register

Address: 0x40040048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

## 13.1.10 GPIO\_PRT1\_DR

Port output data register

Address: 0x40040100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

## 13.1.11 GPIO\_PRT1\_PS

Port IO pad state register

Address: 0x40040104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

### 13.1.11 GPIO\_PRT1\_PS (continued)

0	DATA0	<p>IO pad 0 state:</p> <p>1: Logic high, if the pin voltage is above the input buffer threshold, logic high.</p> <p>0: Logic low, if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> <p>Default Value: 0</p>
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## 13.1.12 GPIO\_PRT1\_PC

Port configuration register

Address: 0x40040108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	<p>This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell.</p> <p>For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell):</p> <p>"0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1"/"3": vcchib.</p> <p>For GPIO_OVTV2 and SIOv2 IO cells:</p> <p>"0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1": vcchib.</p> <p>"2": OVT.</p> <p>"3": Reference (possibly from reference generator cell).</p> <p>For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available).</p> <p>Default Value: 0</p>
25	PORT_SLOW	<p>This field controls the output edge rate of all pins on the port:</p> <p>'0': fast.</p> <p>'1': slow.</p> <p>Default Value: 0</p>



### 13.1.12 GPIO\_PRT1\_PC (continued)

		<p><b>0x0: PORT_SLEW_CTL_0:</b> HS mode (100pf &lt; Cb &lt; 400pF, 1.71&lt;5.5, Vext&gt;3.0) FS mode (10pf&lt;400pf,1.71&lt;5.5) (20-160ns)</p> <p><b>0x1: PORT_SLEW_CTL_1:</b> HS mode (Cb&lt;100pf,1.71&lt;5.5,Vext&gt;2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext&gt;2.8,1.71&lt;5.5) (20-120ns)</p> <p><b>0x2: PORT_SLEW_CTL_2:</b> HS mode (100pf&lt;400pf, 1.71&lt;5.5,Vext&lt;3.3) (20-160ns)</p> <p><b>0x3: PORT_SLEW_CTL_3:</b> HS mode (Cb&lt;100pf,1.71&lt;5.5,Vext&lt;=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext&lt;=2.8,1.71&lt;5.5) (20-120ns)</p>
24	PORT_VTRIP_SEL	<p>The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair).</p> <p>0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0</p>
23 : 21	DM7	<p>The GPIO drive mode for IO pad 7. Default Value: 0</p>
20 : 18	DM6	<p>The GPIO drive mode for IO pad 6. Default Value: 0</p>
17 : 15	DM5	<p>The GPIO drive mode for IO pad 5. Default Value: 0</p>
14 : 12	DM4	<p>The GPIO drive mode for IO pad 4. Default Value: 0</p>
11 : 9	DM3	<p>The GPIO drive mode for IO pad 3. Default Value: 0</p>
8 : 6	DM2	<p>The GPIO drive mode for IO pad 2. Default Value: 0</p>
5 : 3	DM1	<p>The GPIO drive mode for IO pad 1. Default Value: 0</p>
2 : 0	DM0	<p>The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0</p> <p><b>0x0: OFF:</b> Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.</p> <p><b>0x1: INPUT:</b> Mode 1: Output buffer off (high Z). Input buffer on.</p> <p><b>0x2: 0_PU:</b> Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.</p> <p><b>0x3: PD_1:</b> Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.</p> <p><b>0x4: 0_Z:</b> Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.</p>

### 13.1.12 GPIO\_PRT1\_PC (continued)

**0x5: Z\_1:**

Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

**0x6: 0\_1:**

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

**0x7: PD\_PU:**

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

### 13.1.13 GPIO\_PRT1\_INTR\_CFG

Port interrupt configuration register

Address: 0x4004010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			RW
HW Access	None				R			R
Name	None [23:21]				FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0  <b>0x0: DISABLE:</b> Disabled  <b>0x1: RISING:</b> Rising edge  <b>0x2: FALLING:</b> Falling edge  <b>0x3: BOTH:</b> Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

### 13.1.13 GPIO\_PRT1\_INTR\_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

**0x0: DISABLE:**

Disabled

**0x1: RISING:**

Rising edge

**0x2: FALLING:**

Falling edge

**0x3: BOTH:**

Both rising and falling edges

## 13.1.14 GPIO\_PRT1\_INTR

Port interrupt status register

Address: 0x40040110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

  

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

### 13.1.14 GPIO\_PRT1\_INTR (continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

## 13.1.15 GPIO\_PRT1\_PC2

Port configuration register 2

Address: 0x40040118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

### 13.1.15 GPIO\_PRT1\_PC2 (continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0
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## 13.1.16 GPIO\_PRT1\_DR\_SET

Port output data set register

Address: 0x40040140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

## 13.1.17 GPIO\_PRT1\_DR\_CLR

Port output data clear register

Address: 0x40040144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

## 13.1.18 GPIO\_PRT1\_DR\_INV

Port output data invert register

Address: 0x40040148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

## 13.1.19 GPIO\_PRT2\_DR

Port output data register

Address: 0x40040200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

## 13.1.20 GPIO\_PRT2\_PS

Port IO pad state register

Address: 0x40040204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

### 13.1.20 GPIO\_PRT2\_PS (continued)

0	DATA0	<p>IO pad 0 state:</p> <p>1: Logic high, if the pin voltage is above the input buffer threshold, logic high.</p> <p>0: Logic low, if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> <p>Default Value: 0</p>
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## 13.1.21 GPIO\_PRT2\_PC

Port configuration register

Address: 0x40040208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

  

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

  

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	<p>This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell.</p> <p>For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell):</p> <p>"0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1"/"3": vcchib.</p> <p>For GPIO_OVTV2 and SIOv2 IO cells:</p> <p>"0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1": vcchib.</p> <p>"2": OVT.</p> <p>"3": Reference (possibly from reference generator cell).</p> <p>For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available).</p> <p>Default Value: 0</p>
25	PORT_SLOW	<p>This field controls the output edge rate of all pins on the port:</p> <p>'0': fast.</p> <p>'1': slow.</p> <p>Default Value: 0</p>

### 13.1.21 GPIO\_PRT2\_PC (continued)

		<p><b>0x0: PORT_SLEW_CTL_0:</b> HS mode (100pf &lt; Cb &lt; 400pF, 1.71&lt;5.5, Vext&gt;3.0) FS mode (10pf&lt;400pf,1.71&lt;5.5) (20-160ns)</p> <p><b>0x1: PORT_SLEW_CTL_1:</b> HS mode (Cb&lt;100pf,1.71&lt;5.5,Vext&gt;2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext&gt;2.8,1.71&lt;5.5) (20-120ns)</p> <p><b>0x2: PORT_SLEW_CTL_2:</b> HS mode (100pf&lt;400pf, 1.71&lt;5.5,Vext&lt;3.3) (20-160ns)</p> <p><b>0x3: PORT_SLEW_CTL_3:</b> HS mode (Cb&lt;100pf,1.71&lt;5.5,Vext&lt;=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext&lt;=2.8,1.71&lt;5.5) (20-120ns)</p>
24	PORT_VTRIP_SEL	<p>The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair).</p> <p>0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0</p>
23 : 21	DM7	<p>The GPIO drive mode for IO pad 7. Default Value: 0</p>
20 : 18	DM6	<p>The GPIO drive mode for IO pad 6. Default Value: 0</p>
17 : 15	DM5	<p>The GPIO drive mode for IO pad 5. Default Value: 0</p>
14 : 12	DM4	<p>The GPIO drive mode for IO pad 4. Default Value: 0</p>
11 : 9	DM3	<p>The GPIO drive mode for IO pad 3. Default Value: 0</p>
8 : 6	DM2	<p>The GPIO drive mode for IO pad 2. Default Value: 0</p>
5 : 3	DM1	<p>The GPIO drive mode for IO pad 1. Default Value: 0</p>
2 : 0	DM0	<p>The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0</p> <p><b>0x0: OFF:</b> Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.</p> <p><b>0x1: INPUT:</b> Mode 1: Output buffer off (high Z). Input buffer on.</p> <p><b>0x2: 0_PU:</b> Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.</p> <p><b>0x3: PD_1:</b> Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.</p> <p><b>0x4: 0_Z:</b> Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.</p>



### 13.1.21 GPIO\_PRT2\_PC (continued)

**0x5: Z\_1:**

Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

**0x6: 0\_1:**

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

**0x7: PD\_PU:**

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

## 13.1.22 GPIO\_PRT2\_INTR\_CFG

Port interrupt configuration register

Address: 0x4004020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

  

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0  <b>0x0: DISABLE:</b> Disabled  <b>0x1: RISING:</b> Rising edge  <b>0x2: FALLING:</b> Falling edge  <b>0x3: BOTH:</b> Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

### 13.1.22 GPIO\_PRT2\_INTR\_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0
<b>0x0: DISABLE:</b> Disabled		
<b>0x1: RISING:</b> Rising edge		
<b>0x2: FALLING:</b> Falling edge		
<b>0x3: BOTH:</b> Both rising and falling edges		

## 13.1.23 GPIO\_PRT2\_INTR

Port interrupt status register

Address: 0x40040210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

  

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

### 13.1.23 GPIO\_PRT2\_INTR (continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

## 13.1.24 GPIO\_PRT2\_PC2

Port configuration register 2

Address: 0x40040218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

### 13.1.24 GPIO\_PRT2\_PC2 (continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0
---	----------	---

## 13.1.25 GPIO\_PRT2\_DR\_SET

Port output data set register

Address: 0x40040240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0



## 13.1.26 GPIO\_PRT2\_DR\_CLR

Port output data clear register

Address: 0x40040244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

## 13.1.27 GPIO\_PRT2\_DR\_INV

Port output data invert register

Address: 0x40040248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

## 13.1.28 GPIO\_PRT3\_DR

Port output data register

Address: 0x40040300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

## 13.1.29 GPIO\_PRT3\_PS

Port IO pad state register

Address: 0x40040304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

### 13.1.29 GPIO\_PRT3\_PS (continued)

0	DATA0	<p>IO pad 0 state:</p> <p>1: Logic high, if the pin voltage is above the input buffer threshold, logic high.</p> <p>0: Logic low, if the pin voltage is below that threshold, logic low.</p> <p>If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin.</p> <p>Default Value: 0</p>
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### 13.1.30 GPIO\_PRT3\_PC

Port configuration register

Address: 0x40040308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None			RW		RW
HW Access	R		None			R		R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]			PORT_SLOW		PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	<p>This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell.</p> <p>For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell):</p> <p>"0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1"/"3": vcchib.</p> <p>For GPIO_OVTV2 and SIOv2 IO cells:</p> <p>"0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1": vcchib.</p> <p>"2": OVT.</p> <p>"3": Reference (possibly from reference generator cell).</p> <p>For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available).</p> <p>Default Value: 0</p>
25	PORT_SLOW	<p>This field controls the output edge rate of all pins on the port:</p> <p>'0': fast.</p> <p>'1': slow.</p> <p>Default Value: 0</p>

### 13.1.30 GPIO\_PRT3\_PC (continued)

		<b>0x0: PORT_SLEW_CTL_0:</b> HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns)
		<b>0x1: PORT_SLEW_CTL_1:</b> HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns)
		<b>0x2: PORT_SLEW_CTL_2:</b> HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns)
		<b>0x3: PORT_SLEW_CTL_3:</b> HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0
		<b>0x0: OFF:</b> Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.
		<b>0x1: INPUT:</b> Mode 1: Output buffer off (high Z). Input buffer on.
		<b>0x2: 0_PU:</b> Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.
		<b>0x3: PD_1:</b> Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.
		<b>0x4: 0_Z:</b> Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.

### 13.1.30 GPIO\_PRT3\_PC (continued)

**0x5: Z\_1:**

Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

**0x6: 0\_1:**

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

**0x7: PD\_PU:**

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.



### 13.1.31 GPIO\_PRT3\_INTR\_CFG

Port interrupt configuration register

Address: 0x4004030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0  <b>0x0: DISABLE:</b> Disabled  <b>0x1: RISING:</b> Rising edge  <b>0x2: FALLING:</b> Falling edge  <b>0x3: BOTH:</b> Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

### 13.1.31 GPIO\_PRT3\_INTR\_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

**0x0: DISABLE:**

Disabled

**0x1: RISING:**

Rising edge

**0x2: FALLING:**

Falling edge

**0x3: BOTH:**

Both rising and falling edges

## 13.1.32 GPIO\_PRT3\_INTR

Port interrupt status register

Address: 0x40040310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

  

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

### 13.1.32 GPIO\_PRT3\_INTR (continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

### 13.1.33 GPIO\_PRT3\_PC2

Port configuration register 2

Address: 0x40040318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

### 13.1.33 GPIO\_PRT3\_PC2 (continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0
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### 13.1.34 GPIO\_PRT3\_DR\_SET

Port output data set register

Address: 0x40040340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

### 13.1.35 GPIO\_PRT3\_DR\_CLR

Port output data clear register

Address: 0x40040344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0



### 13.1.36 GPIO\_PRT3\_DR\_INV

Port output data invert register

Address: 0x40040348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

## 13.1.37 GPIO\_PRT4\_DR

Port output data register

Address: 0x40040400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

## 13.1.38 GPIO\_PRT4\_PS

Port IO pad state register

Address: 0x40040404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

## 13.1.39 GPIO\_PRT4\_PC

Port configuration register

Address: 0x40040408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM1 [5:3]			DM0 [2:0]		
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	<p>This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell.</p> <p>For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell):</p> <p>"0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1"/"3": vcchib.</p> <p>For GPIO_OVTV2 and SIOv2 IO cells:</p> <p>"0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1": vcchib.</p> <p>"2": OVT.</p> <p>"3": Reference (possibly from reference generator cell).</p> <p>For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available).</p> <p>Default Value: 0</p>
25	PORT_SLOW	<p>This field controls the output edge rate of all pins on the port:</p> <p>'0': fast.</p> <p>'1': slow.</p> <p>Default Value: 0</p>

### 13.1.39 GPIO\_PRT4\_PC (continued)

		<p><b>0x0: PORT_SLEW_CTL_0:</b>  HS mode (100pf &lt; Cb &lt; 400pF, 1.71&lt;5.5, Vext&gt;3.0)  FS mode (10pf&lt;400pf, 1.71&lt;5.5) (20-160ns)</p> <p><b>0x1: PORT_SLEW_CTL_1:</b>  HS mode (Cb&lt;100pf, 1.71&lt;5.5, Vext&gt;2.8, F=1.7MHz) (10-80ns)  FS+ Mode (Vext&gt;2.8, 1.71&lt;5.5) (20-120ns)</p> <p><b>0x2: PORT_SLEW_CTL_2:</b>  HS mode (100pf&lt;400pf, 1.71&lt;5.5, Vext&lt;3.3) (20-160ns)</p> <p><b>0x3: PORT_SLEW_CTL_3:</b>  HS mode (Cb&lt;100pf, 1.71&lt;5.5, Vext&lt;=2.8, F=1.7MHz) (10-80ns)  FS+ mode (Vext&lt;=2.8, 1.71&lt;5.5) (20-120ns)</p>
24	PORT_VTRIP_SEL	<p>The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair).</p> <p>0: input buffer functions as a CMOS input buffer.  1: input buffer functions as a LVTTL input buffer.  Default Value: 0</p>
5 : 3	DM1	<p>The GPIO drive mode for IO pad 1.  Default Value: 0</p>
2 : 0	DM0	<p>The GPIO drive mode for IO pad 0.  Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus.  Default Value: 0</p> <p><b>0x0: OFF:</b>  Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.</p> <p><b>0x1: INPUT:</b>  Mode 1: Output buffer off (high Z). Input buffer on.</p> <p><b>0x2: 0_PU:</b>  Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.</p> <p><b>0x3: PD_1:</b>  Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.</p> <p><b>0x4: 0_Z:</b>  Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.</p> <p><b>0x5: Z_1:</b>  Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.</p> <p><b>0x6: 0_1:</b>  Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.</p> <p><b>0x7: PD_PU:</b>  Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.</p>

## 13.1.40 GPIO\_PRT4\_INTR\_CFG

Port interrupt configuration register

Address: 0x4004040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:21]				FLT_SEL [20:18]		FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0  <b>0x0: DISABLE:</b> Disabled  <b>0x1: RISING:</b> Rising edge  <b>0x2: FALLING:</b> Falling edge  <b>0x3: BOTH:</b> Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

### 13.1.40 GPIO\_PRT4\_INTR\_CFG (continued)

**0x0: DISABLE:**

Disabled

**0x1: RISING:**

Rising edge

**0x2: FALLING:**

Falling edge

**0x3: BOTH:**

Both rising and falling edges

## 13.1.41 GPIO\_PRT4\_INTR

Port interrupt status register

Address: 0x40040410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0



## 13.1.42 GPIO\_PRT4\_PC2

Port configuration register 2

Address: 0x40040418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

### 13.1.43 GPIO\_PRT4\_DR\_SET

Port output data set register

Address: 0x40040440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

## 13.1.44 GPIO\_PRT4\_DR\_CLR

Port output data clear register

Address: 0x40040444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

## 13.1.45 GPIO\_PRT4\_DR\_INV

Port output data invert register

Address: 0x40040448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

## 13.1.46 GPIO\_PRT5\_DR

Port output data register

Address: 0x40040500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

## 13.1.47 GPIO\_PRT5\_PS

Port IO pad state register

Address: 0x40040504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

## 13.1.48 GPIO\_PRT5\_PC

Port configuration register

Address: 0x40040508

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW	None	RW	RW
HW Access	R		R		R	None	R	R
Name	PORT_IB_MODE_SEL [31:30]		PORT_SLEW_CTL [29:28]		PORT_HYST_TRIM	None	PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	<p>This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell.</p> <p>For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell):</p> <p>"0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1"/"3": vcchib.</p> <p>For GPIO_OVTV2 and SIOv2 IO cells:</p> <p>"0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1": vcchib.</p> <p>"2": OVT.</p> <p>"3": Reference (possibly from reference generator cell).</p> <p>For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available).</p> <p>Default Value: 0</p>
29 : 28	PORT_SLEW_CTL	<p>Slew control. Only used in the O_Z drive mode (mode 4: strong pull down, open drain): This field is intended for I2C functionality.</p> <p>Default Value: 0</p>

### 13.1.48 GPIO\_PRT5\_PC (continued)

		<p><b>0x0: PORT_SLEW_CTL_0:</b>  HS mode (100pf &lt; Cb &lt; 400pF, 1.71&lt;5.5, Vext&gt;3.0)  FS mode (10pf&lt;400pf, 1.71&lt;5.5) (20-160ns)</p> <p><b>0x1: PORT_SLEW_CTL_1:</b>  HS mode (Cb&lt;100pf, 1.71&lt;5.5, Vext&gt;2.8, F=1.7MHz) (10-80ns)  FS+ Mode (Vext&gt;2.8, 1.71&lt;5.5) (20-120ns)</p> <p><b>0x2: PORT_SLEW_CTL_2:</b>  HS mode (100pf&lt;400pf, 1.71&lt;5.5, Vext&lt;3.3) (20-160ns)</p> <p><b>0x3: PORT_SLEW_CTL_3:</b>  HS mode (Cb&lt;100pf, 1.71&lt;5.5, Vext&lt;=2.8, F=1.7MHz) (10-80ns)  FS+ mode (Vext&lt;=2.8, 1.71&lt;5.5) (20-120ns)</p>
27	PORT_HYST_TRIM	<p>This field is used to improve the hysteresis (to 10% of vddio) of the selectable trip point input buffer. The voltage reference comes from the VREFGEN block and is only available when using the VREFGEN block:</p> <p>'0': &lt;= 2.2 V input signaling Voltage.  '1': &gt; 2.2 V input signaling Voltage.  Default Value: 0</p>
25	PORT_SLOW	<p>This field controls the output edge rate of all pins on the port:</p> <p>'0': fast.  '1': slow.  Default Value: 0</p>
24	PORT_VTRIP_SEL	<p>The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair).</p> <p>0: input buffer functions as a CMOS input buffer.  1: input buffer functions as a LVTTTL input buffer.  Default Value: 0</p>
5 : 3	DM1	<p>The GPIO drive mode for IO pad 1.  Default Value: 0</p>
2 : 0	DM0	<p>The GPIO drive mode for IO pad 0.  Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus.  Default Value: 0</p> <p><b>0x0: OFF:</b>  Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.</p> <p><b>0x1: INPUT:</b>  Mode 1: Output buffer off (high Z). Input buffer on.</p> <p><b>0x2: 0_PU:</b>  Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.</p> <p><b>0x3: PD_1:</b>  Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.</p> <p><b>0x4: 0_Z:</b>  Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.</p> <p><b>0x5: Z_1:</b>  Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.</p> <p><b>0x6: 0_1:</b>  Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.</p>



### 13.1.48 GPIO\_PRT5\_PC (continued)

**0x7: PD\_PU:**

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

## 13.1.49 GPIO\_PRT5\_INTR\_CFG

Port interrupt configuration register

Address: 0x4004050C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:21]				FLT_SEL [20:18]		FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0  <b>0x0: DISABLE:</b> Disabled  <b>0x1: RISING:</b> Rising edge  <b>0x2: FALLING:</b> Falling edge  <b>0x3: BOTH:</b> Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

### 13.1.49 GPIO\_PRT5\_INTR\_CFG (continued)

**0x0: DISABLE:**

Disabled

**0x1: RISING:**

Rising edge

**0x2: FALLING:**

Falling edge

**0x3: BOTH:**

Both rising and falling edges

## 13.1.50 GPIO\_PRT5\_INTR

Port interrupt status register

Address: 0x40040510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglinted interrupt pending (selected by FLT_SELECT). Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

## 13.1.51 GPIO\_PRT5\_PC2

Port configuration register 2

Address: 0x40040518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

## 13.1.52 GPIO\_PRT5\_DR\_SET

Port output data set register

Address: 0x40040540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

### 13.1.53 GPIO\_PRT5\_DR\_CLR

Port output data clear register

Address: 0x40040544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

## 13.1.54 GPIO\_PRT5\_DR\_INV

Port output data invert register

Address: 0x40040548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0



## 13.1.55 GPIO\_PRT6\_DR

Port output data register

Address: 0x40040600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

## 13.1.56 GPIO\_PRT6\_PS

Port IO pad state register

Address: 0x40040604

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

## 13.1.57 GPIO\_PRT6\_PC

Port configuration register

Address: 0x40040608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	<p>This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell.</p> <p>For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell):</p> <p>"0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1"/"3": vcchib.</p> <p>For GPIO_OVTV2 and SIOv2 IO cells:</p> <p>"0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTTL input buffer (PORT_VTRIP_SEL is '1')</p> <p>"1": vcchib.</p> <p>"2": OVT.</p> <p>"3": Reference (possibly from reference generator cell).</p> <p>For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available).</p> <p>Default Value: 0</p>
25	PORT_SLOW	<p>This field controls the output edge rate of all pins on the port:</p> <p>'0': fast.</p> <p>'1': slow.</p> <p>Default Value: 0</p>

### 13.1.57 GPIO\_PRT6\_PC (continued)

		<p><b>0x0: PORT_SLEW_CTL_0:</b>  HS mode (100pf &lt; Cb &lt; 400pF, 1.71&lt;5.5, Vext&gt;3.0)  FS mode (10pf&lt;400pf, 1.71&lt;5.5) (20-160ns)</p> <p><b>0x1: PORT_SLEW_CTL_1:</b>  HS mode (Cb&lt;100pf, 1.71&lt;5.5, Vext&gt;2.8, F=1.7MHz) (10-80ns)  FS+ Mode (Vext&gt;2.8, 1.71&lt;5.5) (20-120ns)</p> <p><b>0x2: PORT_SLEW_CTL_2:</b>  HS mode (100pf&lt;400pf, 1.71&lt;5.5, Vext&lt;3.3) (20-160ns)</p> <p><b>0x3: PORT_SLEW_CTL_3:</b>  HS mode (Cb&lt;100pf, 1.71&lt;5.5, Vext&lt;=2.8, F=1.7MHz) (10-80ns)  FS+ mode (Vext&lt;=2.8, 1.71&lt;5.5) (20-120ns)</p>
24	PORT_VTRIP_SEL	<p>The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair).</p> <p>0: input buffer functions as a CMOS input buffer.  1: input buffer functions as a LVTTTL input buffer.  Default Value: 0</p>
5 : 3	DM1	<p>The GPIO drive mode for IO pad 1.  Default Value: 0</p>
2 : 0	DM0	<p>The GPIO drive mode for IO pad 0.  Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus.  Default Value: 0</p> <p><b>0x0: OFF:</b>  Mode 0 (analog mode): Output buffer off (high Z). Input buffer off.</p> <p><b>0x1: INPUT:</b>  Mode 1: Output buffer off (high Z). Input buffer on.</p> <p><b>0x2: 0_PU:</b>  Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on.</p> <p><b>0x3: PD_1:</b>  Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on.</p> <p><b>0x4: 0_Z:</b>  Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.</p> <p><b>0x5: Z_1:</b>  Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.</p> <p><b>0x6: 0_1:</b>  Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.</p> <p><b>0x7: PD_PU:</b>  Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.</p>

## 13.1.58 GPIO\_PRT6\_INTR\_CFG

Port interrupt configuration register

Address: 0x4004060C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:21]				FLT_SEL [20:18]		FLT_EDGE_SEL [17:16]	

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0  <b>0x0: DISABLE:</b> Disabled  <b>0x1: RISING:</b> Rising edge  <b>0x2: FALLING:</b> Falling edge  <b>0x3: BOTH:</b> Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

### 13.1.58 GPIO\_PRT6\_INTR\_CFG (continued)

**0x0: DISABLE:**

Disabled

**0x1: RISING:**

Rising edge

**0x2: FALLING:**

Falling edge

**0x3: BOTH:**

Both rising and falling edges

## 13.1.59 GPIO\_PRT6\_INTR

Port interrupt status register

Address: 0x40040610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglinted interrupt pending (selected by FLT_SELECT). Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

## 13.1.60 GPIO\_PRT6\_PC2

Port configuration register 2

Address: 0x40040618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0



## 13.1.61 GPIO\_PRT6\_DR\_SET

Port output data set register

Address: 0x40040640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

## 13.1.62 GPIO\_PRT6\_DR\_CLR

Port output data clear register

Address: 0x40040644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

### 13.1.63 GPIO\_PRT6\_DR\_INV

Port output data invert register

Address: 0x40040648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

# 14 High Speed IO Matrix (HSIOM) Registers



This section discusses the HSIOM registers. It lists all the registers in mapping tables, in address order.

## 14.1 Register Details

Register Name	Address
<a href="#">HSIOM_AMUX_SPLIT_CTL0</a>	0x40022100
<a href="#">HSIOM_AMUX_SPLIT_CTL1</a>	0x40022104
<a href="#">HSIOM_AMUX_SPLIT_CTL2</a>	0x40022108

## 14.1.1 HSIOM\_AMUX\_SPLIT\_CTL0

AMUX splitter cell control

Address: 0x40022100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

### 14.1.1 HSIOM\_AMUX\_SPLIT\_CTL0 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUS switch: '0': switch open. '1': switch closed. Default Value: 0
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## 14.1.2 HSIOM\_AMUX\_SPLIT\_CTL1

AMUX splitter cell control

Address: 0x40022104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

### 14.1.2 HSIOM\_AMUX\_SPLIT\_CTL1 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUS switch: '0': switch open. '1': switch closed. Default Value: 0
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### 14.1.3 HSIOM\_AMUX\_SPLIT\_CTL2

AMUX splitter cell control

Address: 0x40022108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

### 14.1.3 HSIOM\_AMUX\_SPLIT\_CTL2 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUS switch: '0': switch open. '1': switch closed. Default Value: 0
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# 15 HSIOM Port Registers



This section discusses the HSIOM Port registers. It lists all the registers in mapping tables, in address order.

## 15.1 Register Details

Register Name	Address
HSIOM_PORT_SEL0	0x40020000
HSIOM_PORT_SEL1	0x40020100
HSIOM_PORT_SEL2	0x40020200
HSIOM_PORT_SEL3	0x40020300
HSIOM_PORT_SEL4	0x40020400
HSIOM_PORT_SEL5	0x40020500
HSIOM_PORT_SEL6	0x40020600

## 15.1.1 HSIOM\_PORT\_SEL0

Port selection register

Address: 0x40020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

## 15.1.1 HSIOM\_PORT\_SELO (continued)

### 0x0: GPIO:

SW controlled GPIO.

### 0x1: Reserved

### 0x2: Reserved

### 0x3: Reserved

### 0x4: CSD\_SENSE:

CSD sense connection (analog mode)

### 0x5: CSD\_SHIELD:

CSD shield connection (analog mode)

### 0x6: AMUXA:

AMUXBUS A connection.

### 0x7: AMUXB:

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD\_CONTROL, "oe\_n" is connected to "!csd\_charge" signal (and IO pad is also still connected to AMUXBUS B).

### 0x8: ACT\_0:

Chip specific Active source 0 connection.

### 0x9: ACT\_1:

Chip specific Active source 1 connection.

### 0xa: ACT\_2:

Chip specific Active source 2 connection.

### 0xb: ACT\_3:

Chip specific Active source 3 connection.

### 0xc: LCD\_COM:

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

### 0xc: DS\_0:

Chip specific DeepSleep source 0 connection.

### 0xd: LCD\_SEG:

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

### 0xd: DS\_1:

Chip specific DeepSleep source 1 connection.

### 0xe: DS\_2:

Chip specific DeepSleep source 2 connection.

### 0xf: DS\_3:

Chip specific DeepSleep source 3 connection.

## 15.1.2 HSIOM\_PORT\_SEL1

Port selection register

Address: 0x40020100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

## 15.1.2 HSIOM\_PORT\_SEL1 (continued)

### 0x0: GPIO:

SW controlled GPIO.

### 0x1: Reserved

### 0x2: Reserved

### 0x3: Reserved

### 0x4: CSD\_SENSE:

CSD sense connection (analog mode)

### 0x5: CSD\_SHIELD:

CSD shield connection (analog mode)

### 0x6: AMUXA:

AMUXBUS A connection.

### 0x7: AMUXB:

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD\_CONTROL, "oe\_n" is connected to "!csd\_charge" signal (and IO pad is also still connected to AMUXBUS B).

### 0x8: ACT\_0:

Chip specific Active source 0 connection.

### 0x9: ACT\_1:

Chip specific Active source 1 connection.

### 0xa: ACT\_2:

Chip specific Active source 2 connection.

### 0xb: ACT\_3:

Chip specific Active source 3 connection.

### 0xc: LCD\_COM:

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

### 0xc: DS\_0:

Chip specific DeepSleep source 0 connection.

### 0xd: LCD\_SEG:

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

### 0xd: DS\_1:

Chip specific DeepSleep source 1 connection.

### 0xe: DS\_2:

Chip specific DeepSleep source 2 connection.

### 0xf: DS\_3:

Chip specific DeepSleep source 3 connection.

## 15.1.3 HSIOM\_PORT\_SEL2

Port selection register

Address: 0x40020200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0



### 15.1.3 HSIOM\_PORT\_SEL2 (continued)

**0x0: GPIO:**

SW controlled GPIO.

**0x1: Reserved**

**0x2: Reserved**

**0x3: Reserved**

**0x4: CSD\_SENSE:**

CSD sense connection (analog mode)

**0x5: CSD\_SHIELD:**

CSD shield connection (analog mode)

**0x6: AMUXA:**

AMUXBUS A connection.

**0x7: AMUXB:**

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD\_CONTROL, "oe\_n" is connected to "!csd\_charge" signal (and IO pad is also still connected to AMUXBUS B).

**0x8: ACT\_0:**

Chip specific Active source 0 connection.

**0x9: ACT\_1:**

Chip specific Active source 1 connection.

**0xa: ACT\_2:**

Chip specific Active source 2 connection.

**0xb: ACT\_3:**

Chip specific Active source 3 connection.

**0xc: LCD\_COM:**

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xc: DS\_0:**

Chip specific DeepSleep source 0 connection.

**0xd: LCD\_SEG:**

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xd: DS\_1:**

Chip specific DeepSleep source 1 connection.

**0xe: DS\_2:**

Chip specific DeepSleep source 2 connection.

**0xf: DS\_3:**

Chip specific DeepSleep source 3 connection.

## 15.1.4 HSIOM\_PORT\_SEL3

Port selection register

Address: 0x40020300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

## 15.1.4 HSIOM\_PORT\_SEL3 (continued)

### 0x0: GPIO:

SW controlled GPIO.

### 0x1: Reserved

### 0x2: Reserved

### 0x3: Reserved

### 0x4: CSD\_SENSE:

CSD sense connection (analog mode)

### 0x5: CSD\_SHIELD:

CSD shield connection (analog mode)

### 0x6: AMUXA:

AMUXBUS A connection.

### 0x7: AMUXB:

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD\_CONTROL, "oe\_n" is connected to "!csd\_charge" signal (and IO pad is also still connected to AMUXBUS B).

### 0x8: ACT\_0:

Chip specific Active source 0 connection.

### 0x9: ACT\_1:

Chip specific Active source 1 connection.

### 0xa: ACT\_2:

Chip specific Active source 2 connection.

### 0xb: ACT\_3:

Chip specific Active source 3 connection.

### 0xc: LCD\_COM:

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

### 0xc: DS\_0:

Chip specific DeepSleep source 0 connection.

### 0xd: LCD\_SEG:

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

### 0xd: DS\_1:

Chip specific DeepSleep source 1 connection.

### 0xe: DS\_2:

Chip specific DeepSleep source 2 connection.

### 0xf: DS\_3:

Chip specific DeepSleep source 3 connection.

## 15.1.5 HSIOM\_PORT\_SEL4

Port selection register

Address: 0x40020400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0
		<b>0x0: GPIO:</b> SW controlled GPIO.
		<b>0x1: Reserved</b>
		<b>0x2: Reserved</b>
		<b>0x3: Reserved</b>
		<b>0x4: CSD_SENSE:</b> CSD sense connection (analog mode)
		<b>0x5: CSD_SHIELD:</b> CSD shield connection (analog mode)
		<b>0x6: AMUXA:</b> AMUXBUS A connection.

## 15.1.5 HSIOM\_PORT\_SEL4 (continued)

**0x7: AMUXB:**

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD\_CONTROL, "oe\_n" is connected to "!csd\_charge" signal (and IO pad is also still connected to AMUXBUS B).

**0x8: ACT\_0:**

Chip specific Active source 0 connection.

**0x9: ACT\_1:**

Chip specific Active source 1 connection.

**0xa: ACT\_2:**

Chip specific Active source 2 connection.

**0xb: ACT\_3:**

Chip specific Active source 3 connection.

**0xc: LCD\_COM:**

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xc: DS\_0:**

Chip specific DeepSleep source 0 connection.

**0xd: LCD\_SEG:**

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xd: DS\_1:**

Chip specific DeepSleep source 1 connection.

**0xe: DS\_2:**

Chip specific DeepSleep source 2 connection.

**0xf: DS\_3:**

Chip specific DeepSleep source 3 connection.

## 15.1.6 HSIOM\_PORT\_SEL5

Port selection register

Address: 0x40020500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0
	<b>0x0: GPIO:</b>	SW controlled GPIO.
	<b>0x1: Reserved</b>	
	<b>0x2: Reserved</b>	
	<b>0x3: Reserved</b>	
	<b>0x4: CSD_SENSE:</b>	CSD sense connection (analog mode)
	<b>0x5: CSD_SHIELD:</b>	CSD shield connection (analog mode)
	<b>0x6: AMUXA:</b>	AMUXBUS A connection.

## 15.1.6 HSIOM\_PORT\_SEL5 (continued)

**0x7: AMUXB:**

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD\_CONTROL, "oe\_n" is connected to "!csd\_charge" signal (and IO pad is also still connected to AMUXBUS B).

**0x8: ACT\_0:**

Chip specific Active source 0 connection.

**0x9: ACT\_1:**

Chip specific Active source 1 connection.

**0xa: ACT\_2:**

Chip specific Active source 2 connection.

**0xb: ACT\_3:**

Chip specific Active source 3 connection.

**0xc: LCD\_COM:**

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xc: DS\_0:**

Chip specific DeepSleep source 0 connection.

**0xd: LCD\_SEG:**

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xd: DS\_1:**

Chip specific DeepSleep source 1 connection.

**0xe: DS\_2:**

Chip specific DeepSleep source 2 connection.

**0xf: DS\_3:**

Chip specific DeepSleep source 3 connection.

## 15.1.7 HSIOM\_PORT\_SEL6

Port selection register

Address: 0x40020600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0
	<b>0x0: GPIO:</b>	SW controlled GPIO.
	<b>0x1: Reserved</b>	
	<b>0x2: Reserved</b>	
	<b>0x3: Reserved</b>	
	<b>0x4: CSD_SENSE:</b>	CSD sense connection (analog mode)
	<b>0x5: CSD_SHIELD:</b>	CSD shield connection (analog mode)
	<b>0x6: AMUXA:</b>	AMUXBUS A connection.



## 15.1.7 HSIOM\_PORT\_SEL6 (continued)

**0x7: AMUXB:**

AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD\_CONTROL, "oe\_n" is connected to "!csd\_charge" signal (and IO pad is also still connected to AMUXBUS B).

**0x8: ACT\_0:**

Chip specific Active source 0 connection.

**0x9: ACT\_1:**

Chip specific Active source 1 connection.

**0xa: ACT\_2:**

Chip specific Active source 2 connection.

**0xb: ACT\_3:**

Chip specific Active source 3 connection.

**0xc: LCD\_COM:**

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xc: DS\_0:**

Chip specific DeepSleep source 0 connection.

**0xd: LCD\_SEG:**

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

**0xd: DS\_1:**

Chip specific DeepSleep source 1 connection.

**0xe: DS\_2:**

Chip specific DeepSleep source 2 connection.

**0xf: DS\_3:**

Chip specific DeepSleep source 3 connection.

# 16 LCD Registers



This section discusses the LCD registers. It lists all the registers in mapping tables, in address order.

## 16.1 Register Details

Register Name	Address
LCD_ID	0x402A0000
LCD_DIVIDER	0x402A0004
LCD_CONTROL	0x402A0008
LCD_DATA00	0x402A0100
LCD_DATA01	0x402A0104
LCD_DATA02	0x402A0108
LCD_DATA03	0x402A010C
LCD_DATA04	0x402A0110
LCD_DATA05	0x402A0114
LCD_DATA06	0x402A0118
LCD_DATA07	0x402A011C

## 16.1.1 LCD\_ID

ID & Revision

Address: 0x402A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LCD controller peripheral is 0xF0F0 Default Value: 61680

## 16.1.2 LCD\_DIVIDER

LCD Divider Register

Address: 0x402A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

## 16.1.3 LCD\_CONTROL

LCD Configuration Register

Address: 0x402A0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW	RW	RW	RW	RW
HW Access	None	R		R	R	R	R	R
Name	None	BIAS [6:5]		OP_MODE	TYPE	LCD_MODE	HS_EN	LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LS_EN_STAT	<p>LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0.</p> <p>The following procedure should be followed to disable the LS generator:</p> <ol style="list-style-type: none"> <li>1. If LS_EN=0 we are done. Exit the procedure.</li> <li>2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet.</li> <li>3. Set LS_EN=0.</li> <li>4. Wait until LS_EN_STAT=0.</li> </ol> <p>Default Value: 0</p>

### 16.1.3 LCD\_CONTROL (continued)

11 : 8	COM_NUM	<p>The number of COM connections minus 2. So:</p> <p>0: 2 COM's</p> <p>1: 3 COM's</p> <p>...</p> <p>13: 15 COM's</p> <p>14: 16 COM's</p> <p>15: undefined</p> <p>Default Value: 0</p>
6 : 5	BIAS	<p>PWM bias selection</p> <p>Default Value: 0</p> <p><b>0x0: HALF:</b> 1/2 Bias</p> <p><b>0x1: THIRD:</b> 1/3 Bias</p> <p><b>0x2: FOURTH:</b> 1/4 Bias (not supported by LS generator)</p> <p><b>0x3: FIFTH:</b> 1/5 Bias (not supported by LS generator)</p>
4	OP_MODE	<p>Driving mode configuration</p> <p>Default Value: 0</p> <p><b>0x0: PWM:</b> PWM Mode</p> <p><b>0x1: CORRELATION:</b> Digital Correlation Mode</p>
3	TYPE	<p>LCD driving waveform type configuration.</p> <p>Default Value: 0</p> <p><b>0x0: TYPE_A:</b> Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform.</p> <p><b>0x1: TYPE_B:</b> Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).</p>
2	LCD_MODE	<p>HS/LS Mode selection</p> <p>Default Value: 0</p> <p><b>0x0: LS:</b> Select Low Speed (32kHz) Generator (Works in Active, Sleep and DeepSleep power modes).</p> <p><b>0x1: HS:</b> Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).</p>
1	HS_EN	<p>High speed (HS) generator enable</p> <p>1: enable</p> <p>0: disable</p> <p>Default Value: 0</p>
0	LS_EN	<p>Low speed (LS) generator enable</p> <p>1: enable</p> <p>0: disable</p> <p>Default Value: 0</p>

## 16.1.4 LCD\_DATA00

LCD Pin Data Registers

Address: 0x402A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

## 16.1.5 LCD\_DATA01

LCD Pin Data Registers

Address: 0x402A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0



## 16.1.6 LCD\_DATA02

LCD Pin Data Registers

Address: 0x402A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

## 16.1.7 LCD\_DATA03

LCD Pin Data Registers

Address: 0x402A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

## 16.1.8 LCD\_DATA04

LCD Pin Data Registers

Address: 0x402A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

## 16.1.9 LCD\_DATA05

LCD Pin Data Registers

Address: 0x402A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

## 16.1.10 LCD\_DATA06

LCD Pin Data Registers

Address: 0x402A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

## 16.1.11 LCD\_DATA07

LCD Pin Data Registers

Address: 0x402A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

# 17 Peripheral Interconnect (PERI) Registers



This section discusses the PERI registers. It lists all the registers in mapping tables, in address order.

## 17.1 Register Details

Register Name	Address
<a href="#">PERI_DIV_CMD</a>	0x40010000
<a href="#">PERI_PCLK_CTL0</a>	0x40010100
<a href="#">PERI_PCLK_CTL1</a>	0x40010104
<a href="#">PERI_PCLK_CTL2</a>	0x40010108
<a href="#">PERI_PCLK_CTL3</a>	0x4001010C
<a href="#">PERI_PCLK_CTL4</a>	0x40010110
<a href="#">PERI_PCLK_CTL5</a>	0x40010114
<a href="#">PERI_PCLK_CTL6</a>	0x40010118
<a href="#">PERI_PCLK_CTL7</a>	0x4001011C
<a href="#">PERI_PCLK_CTL8</a>	0x40010120
<a href="#">PERI_PCLK_CTL9</a>	0x40010124
<a href="#">PERI_PCLK_CTL10</a>	0x40010128
<a href="#">PERI_PCLK_CTL11</a>	0x4001012C
<a href="#">PERI_PCLK_CTL12</a>	0x40010130
<a href="#">PERI_PCLK_CTL13</a>	0x40010134
<a href="#">PERI_PCLK_CTL14</a>	0x40010138
<a href="#">PERI_PCLK_CTL15</a>	0x4001013C
<a href="#">PERI_DIV_16_CTL0</a>	0x40010300
<a href="#">PERI_DIV_16_CTL1</a>	0x40010304
<a href="#">PERI_DIV_16_CTL2</a>	0x40010308
<a href="#">PERI_DIV_16_CTL3</a>	0x4001030C
<a href="#">PERI_DIV_16_CTL4</a>	0x40010310
<a href="#">PERI_DIV_16_CTL5</a>	0x40010314
<a href="#">PERI_DIV_16_CTL6</a>	0x40010318
<a href="#">PERI_DIV_16_CTL7</a>	0x4001031C
<a href="#">PERI_DIV_16_CTL8</a>	0x40010320

Register Name	Address
PERI_DIV_16_CTL9	0x40010324
PERI_DIV_16_5_CTL0	0x40010400
PERI_DIV_16_5_CTL1	0x40010404



## 17.1.1 PERI\_DIV\_CMD

Divider command register

Address: 0x40010000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	ENABLE	DISABLE	None [29:24]					

Bits	Name	Description
------	------	-------------

## 17.1.1 PERI\_DIV\_CMD (continued)

31	ENABLE	<p>Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps:</p> <p>0: Disable the divider using the DIV_CMD.DISABLE field.  1: Configure the divider's DIV_XXX_CTL register.  2: Enable the divider using the DIV_CMD_ENABLE field.</p> <p>The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_hf" (typical usage) or to ANY enabled divider.</p> <p>The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider.</p> <p>The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_hf"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_hf" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process.  Default Value: 0</p>
30	DISABLE	<p>Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'.</p> <p>The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled.</p> <p>The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately.  Default Value: 0</p>
15 : 14	PA_SEL_TYPE	<p>Specifies the divider type of the divider to which phase alignment is performed for the clock enable command:</p> <p>0: 8.0 (integer) clock dividers.  1: 16.0 (integer) clock dividers.  2: 16.5 (fractional) clock dividers.  3: 24.5 (fractional) clock dividers.  Default Value: 3</p>
13 : 8	PA_SEL_DIV	<p>(PA_SEL_TYPE, PA_SEL_DIV) pecifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times.</p> <p>If PA_SEL_DIV is "63" and "PA_SEL_TYPE" is "3", "clk_hf" is used as reference.  Default Value: 63</p>
7 : 6	SEL_TYPE	<p>Specifies the divider type of the divider on which the command is performed:</p> <p>0: 8.0 (integer) clock dividers.  1: 16.0 (integer) clock dividers.  2: 16.5 (fractional) clock dividers.  3: 24.5 (fractional) clock dividers.  Default Value: 3</p>
5 : 0	SEL_DIV	<p>(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed.</p> <p>If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock signal(s) are generated.  Default Value: 63</p>

## 17.1.2 PERI\_PCLK\_CTL0

Programmable clock control register

Address: 0x40010100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.3 PERI\_PCLK\_CTL1

Programmable clock control register

Address: 0x40010104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.4 PERI\_PCLK\_CTL2

Programmable clock control register

Address: 0x40010108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.5 PERI\_PCLK\_CTL3

Programmable clock control register

Address: 0x4001010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.6 PERI\_PCLK\_CTL4

Programmable clock control register

Address: 0x40010110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.7 PERI\_PCLK\_CTL5

Programmable clock control register

Address: 0x40010114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15



## 17.1.8 PERI\_PCLK\_CTL6

Programmable clock control register

Address: 0x40010118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.9 PERI\_PCLK\_CTL7

Programmable clock control register

Address: 0x4001011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.10 PERI\_PCLK\_CTL8

Programmable clock control register

Address: 0x40010120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.11 PERI\_PCLK\_CTL9

Programmable clock control register

Address: 0x40010124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.12 PERI\_PCLK\_CTL10

Programmable clock control register

Address: 0x40010128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.13 PERI\_PCLK\_CTL11

Programmable clock control register

Address: 0x4001012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.14 PERI\_PCLK\_CTL12

Programmable clock control register

Address: 0x40010130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.15 PERI\_PCLK\_CTL13

Programmable clock control register

Address: 0x40010134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15



## 17.1.16 PERI\_PCLK\_CTL14

Programmable clock control register

Address: 0x40010138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.17 PERI\_PCLK\_CTL15

Programmable clock control register

Address: 0x4001013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE.  If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated.  When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

## 17.1.18 PERI\_DIV\_16\_CTL0

Divider control register (for 16.0 divider)

Address: 0x40010300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.19 PERI\_DIV\_16\_CTL1

Divider control register (for 16.0 divider)

Address: 0x40010304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.20 PERI\_DIV\_16\_CTL2

Divider control register (for 16.0 divider)

Address: 0x40010308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.21 PERI\_DIV\_16\_CTL3

Divider control register (for 16.0 divider)

Address: 0x4001030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.22 PERI\_DIV\_16\_CTL4

Divider control register (for 16.0 divider)

Address: 0x40010310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.23 PERI\_DIV\_16\_CTL5

Divider control register (for 16.0 divider)

Address: 0x40010314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>



## 17.1.24 PERI\_DIV\_16\_CTL6

Divider control register (for 16.0 divider)

Address: 0x40010318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.25 PERI\_DIV\_16\_CTL7

Divider control register (for 16.0 divider)

Address: 0x4001031C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.26 PERI\_DIV\_16\_CTL8

Divider control register (for 16.0 divider)

Address: 0x40010320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.27 PERI\_DIV\_16\_CTL9

Divider control register (for 16.0 divider)

Address: 0x40010324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division.</p> <p>For the generation of a divided clock, the integer division range is restricted to [2, 65,536].</p> <p>For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.28 PERI\_DIV\_16\_5\_CTL0

Divider control register (for 16.5 divider)

Address: 0x40010400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/ 32] in 1/32 increments.</p> <p>For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32].</p> <p>For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536].</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
7 : 3	FRAC5_DIV	<p>Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.28 PERI\_DIV\_16\_5\_CTL0 (continued)

0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.</p> <p>Default Value: 0</p>
---	----	---

## 17.1.29 PERI\_DIV\_16\_5\_CTL1

Divider control register (for 16.5 divider)

Address: 0x40010404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	<p>Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/ 32] in 1/32 increments.</p> <p>For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32].</p> <p>For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536].</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>
7 : 3	FRAC5_DIV	<p>Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods.</p> <p>Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0</p>

## 17.1.29 PERI\_DIV\_16\_5\_CTL1 (continued)

0	EN	<p>Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command.</p> <p>Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode.</p> <p>Default Value: 0</p>
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# 18 ROM Table Registers



This section discusses the ROM Table registers. It lists all the registers in mapping tables, in address order.

## 18.1 Register Details

Register Name	Address
ROMTABLE_ADDR	0xF0000000
ROMTABLE_DID	0xF0000FCC
ROMTABLE_PID4	0xF0000FD0
ROMTABLE_PID5	0xF0000FD4
ROMTABLE_PID6	0xF0000FD8
ROMTABLE_PID7	0xF0000FDC
ROMTABLE_PID0	0xF0000FE0
ROMTABLE_PID1	0xF0000FE4
ROMTABLE_PID2	0xF0000FE8
ROMTABLE_PID3	0xF0000FEC
ROMTABLE_CID0	0xF0000FF0
ROMTABLE_CID1	0xF0000FF4
ROMTABLE_CID2	0xF0000FF8
ROMTABLE_CID3	0xF0000FFC

## 18.1.1 ROMTABLE\_ADDR

Link to Cortex M0 ROM Table.

Address: 0xF0000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FORMAT_3 2BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 983295
1	FORMAT_32BIT	ROM Table format: '0': 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

## 18.1.2 ROMTABLE\_DID

Device Type Identifier register.

Address: 0xF0000FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 1

## 18.1.3 ROMTABLE\_PID4

Peripheral Identification Register 4.

Address: 0xF0000FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2 <sup>COUNT</sup> * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

## 18.1.4 ROMTABLE\_PID5

Peripheral Identification Register 5.

Address: 0xF0000FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

## 18.1.5 ROMTABLE\_PID6

Peripheral Identification Register 6.

Address: 0xF0000FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

## 18.1.6 ROMTABLE\_PID7

Peripheral Identification Register 7.

Address: 0xF0000FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

## 18.1.7 ROMTABLE\_PID0

Peripheral Identification Register 0.

Address: 0xF0000FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined



## 18.1.8 ROMTABLE\_PID1

Peripheral Identification Register 1.

Address: 0xF0000FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

## 18.1.9 ROMTABLE\_PID2

Peripheral Identification Register 2.

Address: 0xF0000FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVersion number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined

## 18.1.10 ROMTABLE\_PID3

Peripheral Identification Register 3.

Address: 0xF0000FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REvision number (chip specific). For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of componenet IP reuse. Default Value: 0

## 18.1.11 ROMTABLE\_CID0

Component Identification Register 0.

Address: 0xF0000FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 13

## 18.1.12 ROMTABLE\_CID1

Component Identification Register 1.

Address: 0xF0000FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 16

## 18.1.13 ROMTABLE\_CID2

Component Identification Register 2.

Address: 0xF0000FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 5

## 18.1.14 ROMTABLE\_CID3

Component Identification Register 3.

Address: 0xF0000FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 177

# 19 SAR Registers



This section discusses the SAR registers. It lists all the registers in mapping tables, in address order.

## 19.1 Register Details

Register Name	Address
SAR_CTRL	0x403A0000
SAR_SAMPLE_CTRL	0x403A0004
SAR_SAMPLE_TIME01	0x403A0010
SAR_SAMPLE_TIME23	0x403A0014
SAR_RANGE_THRES	0x403A0018
SAR_RANGE_COND	0x403A001C
SAR_CHAN_EN	0x403A0020
SAR_START_CTRL	0x403A0024
SAR_DFT_CTRL	0x403A0030
SAR_CHAN_CONFIG0	0x403A0080
SAR_CHAN_CONFIG1	0x403A0084
SAR_CHAN_CONFIG2	0x403A0088
SAR_CHAN_CONFIG3	0x403A008C
SAR_CHAN_CONFIG4	0x403A0090
SAR_CHAN_CONFIG5	0x403A0094
SAR_CHAN_CONFIG6	0x403A0098
SAR_CHAN_CONFIG7	0x403A009C
SAR_CHAN_CONFIG8	0x403A00A0
SAR_CHAN_CONFIG9	0x403A00A4
SAR_CHAN_CONFIG10	0x403A00A8
SAR_CHAN_CONFIG11	0x403A00AC
SAR_CHAN_CONFIG12	0x403A00B0
SAR_CHAN_CONFIG13	0x403A00B4
SAR_CHAN_CONFIG14	0x403A00B8
SAR_CHAN_CONFIG15	0x403A00BC
SAR_CHAN_WORK0	0x403A0100



Register Name	Address
SAR_CHAN_WORK1	0x403A0104
SAR_CHAN_WORK2	0x403A0108
SAR_CHAN_WORK3	0x403A010C
SAR_CHAN_WORK4	0x403A0110
SAR_CHAN_WORK5	0x403A0114
SAR_CHAN_WORK6	0x403A0118
SAR_CHAN_WORK7	0x403A011C
SAR_CHAN_WORK8	0x403A0120
SAR_CHAN_WORK9	0x403A0124
SAR_CHAN_WORK10	0x403A0128
SAR_CHAN_WORK11	0x403A012C
SAR_CHAN_WORK12	0x403A0130
SAR_CHAN_WORK13	0x403A0134
SAR_CHAN_WORK14	0x403A0138
SAR_CHAN_WORK15	0x403A013C
SAR_CHAN_RESULT0	0x403A0180
SAR_CHAN_RESULT1	0x403A0184
SAR_CHAN_RESULT2	0x403A0188
SAR_CHAN_RESULT3	0x403A018C
SAR_CHAN_RESULT4	0x403A0190
SAR_CHAN_RESULT5	0x403A0194
SAR_CHAN_RESULT6	0x403A0198
SAR_CHAN_RESULT7	0x403A019C
SAR_CHAN_RESULT8	0x403A01A0
SAR_CHAN_RESULT9	0x403A01A4
SAR_CHAN_RESULT10	0x403A01A8
SAR_CHAN_RESULT11	0x403A01AC
SAR_CHAN_RESULT12	0x403A01B0
SAR_CHAN_RESULT13	0x403A01B4
SAR_CHAN_RESULT14	0x403A01B8
SAR_CHAN_RESULT15	0x403A01BC
SAR_CHAN_WORK_VALID	0x403A0200
SAR_CHAN_RESULT_VALID	0x403A0204
SAR_STATUS	0x403A0208
SAR_AVG_STAT	0x403A020C
SAR_INTR	0x403A0210
SAR_INTR_SET	0x403A0214
SAR_INTR_MASK	0x403A0218
SAR_INTR_MASKED	0x403A021C
SAR_SATURATE_INTR	0x403A0220

Register Name	Address
SAR_SATURATE_INTR_SET	0x403A0224
SAR_SATURATE_INTR_MASK	0x403A0228
SAR_SATURATE_INTR_MASKED	0x403A022C
SAR_RANGE_INTR	0x403A0230
SAR_RANGE_INTR_SET	0x403A0234
SAR_RANGE_INTR_MASK	0x403A0238
SAR_RANGE_INTR_MASKED	0x403A023C
SAR_INTR_CAUSE	0x403A0240
SAR_INJ_CHAN_CONFIG	0x403A0280
SAR_INJ_RESULT	0x403A0290
SAR_MUX_SWITCH0	0x403A0300
SAR_MUX_SWITCH_CLEAR0	0x403A0304
SAR_MUX_SWITCH1	0x403A0308
SAR_MUX_SWITCH_CLEAR1	0x403A030C
SAR_MUX_SWITCH_HW_CTRL	0x403A0340
SAR_MUX_SWITCH_STATUS	0x403A0348
SAR_PUMP_CTRL	0x403A0380
SAR_ANA_TRIM	0x403A0F00
SAR_WOUNDING	0x403A0F04

## 19.1.1 SAR\_CTRL

Analog control register.

Address: 0x403A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	VREF_BYP_CAP_EN	VREF_SEL [6:4]			None [3:0]			

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	PWR_CTRL_VREF [15:14]		SAR_HW_CTRL_NEG_VREF	None	NEG_SEL [11:9]			None

  

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [23:21]			BOOSTPU_MP_EN	SPARE [19:16]			

  

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	None	RW	None	RW	
HW Access	R	R	None	None	R	None	R	
Name	ENABLED	SWITCH_DISABLE	Reserved	Reserved	DEEPSLEEP_ON	None	ICONT_LV [25:24]	

Bits	Name	Description
31	ENABLED	Before enabling always make sure the SAR is idle (STATUS.BUSY==0) - 0: SAR IP disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgating) on write. - 1: SAR IP enabled. Default Value: 0
30	SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware to set the switches to route the signal to be converted through the SARMUX Default Value: 0
29	Reserved	Reserved
28	Reserved	Reserved

### 19.1.1 SAR\_CTRL (continued)

27	DEEPSLEEP_ON	<p>- 0: SARMUX IP disabled off during DeepSleep power mode  - 1: SARMUX IP remains enabled during DeepSleep power mode (if ENABLED=1)  Default Value: 0</p>
25 : 24	ICONT_LV	<p>SARADC low power mode.  Default Value: 0</p> <p><b>0x0: NORMAL_PWR:</b>  normal power (default), max clk_sar is 18MHz.</p> <p><b>0x1: HALF_PWR:</b>  1/2 power mode, max clk_sar is 9MHz.</p> <p><b>0x2: MORE_PWR:</b>  1.333 power mode, max clk_sar is 18MHz.</p> <p><b>0x3: QUARTER_PWR:</b>  1/4 power mode, max clk_sar is 4.5MHz.</p>
20	BOOSTPUMP_EN	<p>SARADC internal pump: 0=disabled: pump output is VDDA, 1=enabled: pump output is boosted.  Default Value: 0</p>
19 : 16	SPARE	<p>Spare controls, not yet designated, for late changes done with an ECO  Default Value: 0</p>
15 : 14	PWR_CTRL_VREF	<p>VREF buffer low power mode.  Default Value: 0</p> <p><b>0x0: NORMAL_PWR:</b>  normal power (default), bypass cap, max clk_sar is 18MHz.</p> <p><b>0x1: HALF_PWR:</b>  deprecated</p> <p><b>0x2: THIRD_PWR:</b>  Invalid for PRoC BLE otherwise 2X power, no bypass cap, max clk_sar is 1.8MHz</p> <p><b>0x3: QUARTER_PWR:</b>  deprecated</p>
13	SAR_HW_CTRL_NEGVREF	<p>Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch.  Default Value: 0</p>
11 : 9	NEG_SEL	<p>SARADC internal NEG selection for Single ended conversion  Default Value: 0</p> <p><b>0x0: VSSA_KELVIN:</b>  NEG input of SARADC is connected to "vssa_kelvin", gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high.</p> <p><b>0x1: ART_VSSA:</b>  NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC</p> <p><b>0x2: P1:</b>  NEG input of SARADC is connected to P1 pin of SARMUX</p> <p><b>0x3: P3:</b>  NEG input of SARADC is connected to P3 pin of SARMUX</p> <p><b>0x4: P5:</b>  NEG input of SARADC is connected to P5 pin of SARMUX</p> <p><b>0x5: P7:</b>  NEG input of SARADC is connected to P7 pin of SARMUX</p>

## 19.1.1 SAR\_CTRL (continued)

		<b>0x6: ACORE:</b> NEG input of SARADC is connected to an ACORE in AROUTE
		<b>0x7: VREF:</b> NEG input of SARADC is shorted with VREF input of SARADC.
7	VREF_BYP_CAP_EN	VREF bypass cap enable for when VREF buffer is on Default Value: 0
6 : 4	VREF_SEL	SARADC internal VREF selection. Default Value: 0
		<b>0x0: VREF0:</b> VREF0 from PRB (VREF buffer on)
		<b>0x1: VREF1:</b> VREF1 from PRB (VREF buffer on)
		<b>0x2: VREF2:</b> VREF2 from PRB (VREF buffer on)
		<b>0x3: VREF_AROUTE:</b> VREF from AROUTE (VREF buffer on)
		<b>0x4: VBGR:</b> 1.024V from BandGap (VREF buffer on)
		<b>0x5: VREF_EXT:</b> External precision Vref direct from a pin (low impedance path).
		<b>0x6: VDDA_DIV_2:</b> Vdda/2 (VREF buffer on)
		<b>0x7: VDDA:</b> Vdda.

## 19.1.2 SAR\_SAMPLE\_CTRL

Sample control register.

Address: 0x403A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	AVG_SHIFT	AVG_CNT [6:4]			DIFFERENTIAL_SIGNED	SINGLE_ENDED_SIGNED	LEFT_ALIGN	SUB_RESOLUTION

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None				None	None	None	RW
HW Access	None				None	None	None	R
Name	None [23:20]				Reserved	Reserved	Reserved	CONTINUOUS

  

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
19	Reserved	Reserved
18	Reserved	Reserved
17	Reserved	Reserved
16	CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. Default Value: 0
7	AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in the sample resolution. For averaging the sample resolution is the highest resolution allowed by rounding. Default Value: 0

## 19.1.2 SAR\_SAMPLE\_CTRL (continued)

6 : 4	AVG_CNT	<p>Averaging Count for channels that have over sampling enabled (AVG_EN). A channel will be sampled back to back <math>(1 \leq \text{AVG\_CNT} + 1) = [2..256]</math> times before the result is stored and the next enabled channel is sampled (1st order accumulate and dump filter).</p> <p>If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that it fits in 16 bits, so right shift is done by <math>\max(0, \text{AVG\_CNT} - 3)</math>.</p> <p>Default Value: 0</p>
3	DIFFERENTIAL_SIGNED	<p>Output data from a differential conversion as a signed value</p> <p>Default Value: 1</p> <p><b>0x0: UNSIGNED:</b> result data is unsigned (zero extended if needed)</p> <p><b>0x1: SIGNED:</b> Default: result data is signed (sign extended if needed)</p>
2	SINGLE_ENDED_SIGNED	<p>Output data from a single ended conversion as a signed value</p> <p>Default Value: 0</p> <p><b>0x0: UNSIGNED:</b> Default: result data is unsigned (zero extended if needed)</p> <p><b>0x1: SIGNED:</b> result data is signed (sign extended if needed)</p>
1	LEFT_ALIGN	<p>Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential.</p> <p>Default Value: 0</p>
0	SUB_RESOLUTION	<p>Conversion resolution for channels that have sub-resolution enabled (RESOLUTION=1) (otherwise resolution is 12-bit).</p> <p>Default Value: 0</p> <p><b>0x0: 8B:</b> 8-bit.</p> <p><b>0x1: 10B:</b> 10-bit.</p>

## 19.1.3 SAR\_SAMPLE\_TIME01

Sample time specification ST0 and ST1

Address: 0x403A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME0 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME0 [9:8]	
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME1 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME1	Sample time1 Default Value: 4
9 : 0	SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is half a clock less than specified here. The minimum sample time is 194ns, which is 3.5 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 4



## 19.1.4 SAR\_SAMPLE\_TIME23

Sample time specification ST2 and ST3

Address: 0x403A0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME2 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME2 [9:8]	
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME3 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME3	Sample time3 Default Value: 4
9 : 0	SAMPLE_TIME2	Sample time2 Default Value: 4

## 19.1.5 SAR\_RANGE\_THRES

Global range detect threshold register.

Address: 0x403A0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	RANGE_HIGH	High threshold for range detect. Default Value: 0
15 : 0	RANGE_LOW	Low threshold for range detect. Default Value: 0

## 19.1.6 SAR\_RANGE\_COND

Global range detect mode register.

Address: 0x403A001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	RANGE_COND	<p>Range condition select. Default Value: 0</p> <p><b>0x0: BELOW:</b> result &lt; RANGE_LOW</p> <p><b>0x1: INSIDE:</b> RANGE_LOW &lt;= result &lt; RANGE_HIGH</p> <p><b>0x2: ABOVE:</b> RANGE_HIGH &lt;= result</p> <p><b>0x3: OUTSIDE:</b> result &lt; RANGE_LOW    RANGE_HIGH &lt;= result</p>

## 19.1.7 SAR\_CHAN\_EN

Enable bits for the channels

Address: 0x403A0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_EN [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_EN [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_EN	<p>Channel enable.</p> <ul style="list-style-type: none"> <li>- 0: the corresponding channel is disabled.</li> <li>- 1: the corresponding channel is enabled, it will be included in the next scan.</li> </ul> <p>Default Value: 0</p>

## 19.1.8 SAR\_START\_CTRL

Start control register (firmware trigger).

Address: 0x403A0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							FW_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default Value: 0

## 19.1.9 SAR\_DFT\_CTRL

DFT control register.

Address: 0x403A0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						HIZ	DLY_INC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			RW			
HW Access	None	R			R			
Name	None	DFT_OUTC [22:20]			DFT_INC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW	RW			
HW Access	R	None	R	R	R			
Name	ADFT_OVE RRIDE	None	DCEN	EN_CSEL_ DFT	SEL_CSEL_DFT [27:24]			

Bits	Name	Description
31	ADFT_OVERRIDE	During deepsleep/ hibernate mode keep SARMUX active, i.e. do not open all switches (disconnect), to be used for ADFT Default Value: 0
29	DCEN	Delay Control Enable for latch. - 0: doubles the latch enable time. - 1: normal latch enable time (default). Default Value: 0
28	EN_CSEL_DFT	Mux select signal for DAC control Default Value: 0
27 : 24	SEL_CSEL_DFT	Usage 1: DFT bits for DAC array Usage 2: For [0]=1 (when dcen=0): Delay timing for latch enable increased by 20% [1]=1: comparator preamp power level increased by 25% Default Value: 0
22 : 20	DFT_OUTC	DFT control for preamp outputs Default Value: 0

### 19.1.9 SAR\_DFT\_CTRL (continued)

19 : 16	DFT_INC	DFT control for preamp inputs Default Value: 0
1	HIZ	DFT control for getting higher input impedance, must be 1 (0 is deprecated) Default Value: 1
0	DLY_INC	DFT control: Control for delay circuits on sampling phase, =1 doubles the non-overlap delay Default Value: 0

## 19.1.10 SAR\_CHAN\_CONFIG0

Channel configuration register.

Address: 0x403A0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.



### 19.1.10 SAR\_CHAN\_CONFIG0 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.11 SAR\_CHAN\_CONFIG1

Channel configuration register.

Address: 0x403A0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.11 SAR\_CHAN\_CONFIG1 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.12 SAR\_CHAN\_CONFIG2

Channel configuration register.

Address: 0x403A0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.12 SAR\_CHAN\_CONFIG2 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.13 SAR\_CHAN\_CONFIG3

Channel configuration register.

Address: 0x403A008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.13 SAR\_CHAN\_CONFIG3 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.14 SAR\_CHAN\_CONFIG4

Channel configuration register.

Address: 0x403A0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.



### 19.1.14 SAR\_CHAN\_CONFIG4 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.15 SAR\_CHAN\_CONFIG5

Channel configuration register.

Address: 0x403A0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.15 SAR\_CHAN\_CONFIG5 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.16 SAR\_CHAN\_CONFIG6

Channel configuration register.

Address: 0x403A0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.16 SAR\_CHAN\_CONFIG6 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.17 SAR\_CHAN\_CONFIG7

Channel configuration register.

Address: 0x403A009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0
<b>0x0: MAXRES:</b>		
The maximum resolution is used for this channel (maximum resolution depends on rounding).		
<b>0x1: SUBRES:</b>		
The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.		

### 19.1.17 SAR\_CHAN\_CONFIG7 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.18 SAR\_CHAN\_CONFIG8

Channel configuration register.

Address: 0x403A00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.



### 19.1.18 SAR\_CHAN\_CONFIG8 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.19 SAR\_CHAN\_CONFIG9

Channel configuration register.

Address: 0x403A00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.19 SAR\_CHAN\_CONFIG9 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.20 SAR\_CHAN\_CONFIG10

Channel configuration register.

Address: 0x403A00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.20 SAR\_CHAN\_CONFIG10 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.21 SAR\_CHAN\_CONFIG11

Channel configuration register.

Address: 0x403A00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.21 SAR\_CHAN\_CONFIG11 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.22 SAR\_CHAN\_CONFIG12

Channel configuration register.

Address: 0x403A00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0
<b>0x0: MAXRES:</b>		
The maximum resolution is used for this channel (maximum resolution depends on rounding).		
<b>0x1: SUBRES:</b>		
The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.		



## 19.1.22 SAR\_CHAN\_CONFIG12 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.23 SAR\_CHAN\_CONFIG13

Channel configuration register.

Address: 0x403A00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0
<b>0x0: MAXRES:</b>		
The maximum resolution is used for this channel (maximum resolution depends on rounding).		
<b>0x1: SUBRES:</b>		
The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.		

### 19.1.23 SAR\_CHAN\_CONFIG13 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.24 SAR\_CHAN\_CONFIG14

Channel configuration register.

Address: 0x403A00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.24 SAR\_CHAN\_CONFIG14 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.25 SAR\_CHAN\_CONFIG15

Channel configuration register.

Address: 0x403A00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLUTION	DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	None						
HW Access	None	None						
Name	Reserved	None [30:24]						

Bits	Name	Description
31	Reserved	Reserved
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by rounding) is used for this channel. Default Value: 0  <b>0x0: MAXRES:</b> The maximum resolution is used for this channel (maximum resolution depends on rounding).  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

### 19.1.25 SAR\_CHAN\_CONFIG15 (continued)

8	DIFFERENTIAL_EN	<p>Differential enable for this channel.</p> <ul style="list-style-type: none"> <li>- 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register.</li> <li>- 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored).</li> </ul> <p>Default Value: 0</p>
6 : 4	PORT_ADDR	<p>Address of the port that contains the pin to be sampled by this channel.</p> <p>Default Value: 0</p> <p><b>0x0: SARMUX:</b> SARMUX pins.</p> <p><b>0x1: CTB0:</b> CTB0</p> <p><b>0x2: CTB1:</b> CTB1</p> <p><b>0x3: CTB2:</b> CTB2</p> <p><b>0x4: CTB3:</b> CTB3</p> <p><b>0x5: AROUTE_VIRT2:</b> AROUTE virtual port2 (VPORT2)</p> <p><b>0x6: AROUTE_VIRT1:</b> AROUTE virtual port1 (VPORT1)</p> <p><b>0x7: SARMUX_VIRT:</b> SARMUX virtual port (VPORT0)</p>
2 : 0	PIN_ADDR	<p>Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus.</p> <p>Default Value: 0</p>

## 19.1.26 SAR\_CHAN\_WORK0

Channel working data register

Address: 0x403A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined



## 19.1.27 SAR\_CHAN\_WORK1

Channel working data register

Address: 0x403A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.28 SAR\_CHAN\_WORK2

Channel working data register

Address: 0x403A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.29 SAR\_CHAN\_WORK3

Channel working data register

Address: 0x403A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.30 SAR\_CHAN\_WORK4

Channel working data register

Address: 0x403A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.31 SAR\_CHAN\_WORK5

Channel working data register

Address: 0x403A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.32 SAR\_CHAN\_WORK6

Channel working data register

Address: 0x403A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

### 19.1.33 SAR\_CHAN\_WORK7

Channel working data register

Address: 0x403A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.34 SAR\_CHAN\_WORK8

Channel working data register

Address: 0x403A0120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined



## 19.1.35 SAR\_CHAN\_WORK9

Channel working data register

Address: 0x403A0124

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.36 SAR\_CHAN\_WORK10

Channel working data register

Address: 0x403A0128

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.37 SAR\_CHAN\_WORK11

Channel working data register

Address: 0x403A012C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.38 SAR\_CHAN\_WORK12

Channel working data register

Address: 0x403A0130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.39 SAR\_CHAN\_WORK13

Channel working data register

Address: 0x403A0134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.40 SAR\_CHAN\_WORK14

Channel working data register

Address: 0x403A0138

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.41 SAR\_CHAN\_WORK15

Channel working data register

Address: 0x403A013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

## 19.1.42 SAR\_CHAN\_RESULT0

Channel result data register

Address: 0x403A0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined



## 19.1.43 SAR\_CHAN\_RESULT1

Channel result data register

Address: 0x403A0184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.44 SAR\_CHAN\_RESULT2

Channel result data register

Address: 0x403A0188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.45 SAR\_CHAN\_RESULT3

Channel result data register

Address: 0x403A018C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.46 SAR\_CHAN\_RESULT4

Channel result data register

Address: 0x403A0190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.47 SAR\_CHAN\_RESULT5

Channel result data register

Address: 0x403A0194

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.48 SAR\_CHAN\_RESULT6

Channel result data register

Address: 0x403A0198

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.49 SAR\_CHAN\_RESULT7

Channel result data register

Address: 0x403A019C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.50 SAR\_CHAN\_RESULT8

Channel result data register

Address: 0x403A01A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined



## 19.1.51 SAR\_CHAN\_RESULT9

Channel result data register

Address: 0x403A01A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.52 SAR\_CHAN\_RESULT10

Channel result data register

Address: 0x403A01A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.53 SAR\_CHAN\_RESULT11

Channel result data register

Address: 0x403A01AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.54 SAR\_CHAN\_RESULT12

Channel result data register

Address: 0x403A01B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.55 SAR\_CHAN\_RESULT13

Channel result data register

Address: 0x403A01B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.56 SAR\_CHAN\_RESULT14

Channel result data register

Address: 0x403A01B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.57 SAR\_CHAN\_RESULT15

Channel result data register

Address: 0x403A01BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

## 19.1.58 SAR\_CHAN\_WORK\_VALID

Channel working data register valid bits

Address: 0x403A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_WORK_VALID	If set the corresponding WORK data is valid, i.e. was already sampled during the current scan. Default Value: 0



## 19.1.59 SAR\_CHAN\_RESULT\_VALID

Channel result data register valid bits

Address: 0x403A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_RESULT_VALID	If set the corresponding RESULT data is valid, i.e. was sampled during the last scan. Default Value: 0

## 19.1.60 SAR\_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x403A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	BUSY	SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SW_VREF_NEG	the current switch status, including sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default Value: 0
4 : 0	CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default Value: 0

## 19.1.61 SAR\_AVG\_STAT

Current averaging status (for debug)

Address: 0x403A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

## 19.1.62 SAR\_INTR

Interrupt request register.

Address: 0x403A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
Name	INJ_COLLISION_INTR	INJ_RANGE_INTR	INJ_SATURATE_INTR	INJ_EOC_INTR	Reserved	FW_COLLISION_INTR	OVERFLOW_INTR	EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit. Default Value: 0
6	INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0
5	INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0
4	INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit. Default Value: 0

### 19.1.62 SAR\_INTR (continued)

3	Reserved	Reserved
2	FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
1	OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. Default Value: 0
0	EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

## 19.1.63 SAR\_INTR\_SET

Interrupt set request register

Address: 0x403A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	A	A	A	A	None	A	A	A
Name	INJ_COLLISION_SET	INJ_RANGE_SET	INJ_SATURATE_SET	INJ_EOC_SET	Reserved	FW_COLLISION_SET	OVERFLOW_SET	EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	Reserved	Reserved
2	FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 19.1.64 SAR\_INTR\_MASK (continued)

## 19.1.64 SAR\_INTR\_MASK

Interrupt mask register.

Address: 0x403A0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	RW
HW Access	R	R	R	R	None	R	R	R
Name	INJ_COLLISION_MASK	INJ_RANGE_MASK	INJ_SATURATE_MASK	INJ_EOC_MASK	Reserved	FW_COLLISION_MASK	OVERFLOW_MASK	EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	Reserved	Reserved
2	FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

0	EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
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## 19.1.65 SAR\_INTR\_MASKED (continued)

## 19.1.65 SAR\_INTR\_MASKED

Interrupt masked request register

Address: 0x403A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None	R	R	R
HW Access	W	W	W	W	None	W	W	W
Name	INJ_COLLISION_MASKED	INJ_RANGE_MASKED	INJ_SATURATE_MASKED	INJ_EOC_MASKED	Reserved	FW_COLLISION_MASKED	OVERFLOW_MASKED	EOS_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	INJ_SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	Reserved	Reserved
2	FW_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

0	EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
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### 19.1.66 SAR\_SATURATE\_INTR (continued)

### 19.1.66 SAR\_SATURATE\_INTR

Saturate interrupt request register.

Address: 0x403A0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

## 19.1.67 SAR\_SATURATE\_INTR\_SET

Saturate interrupt set request register

Address: 0x403A0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 19.1.68 SAR\_SATURATE\_INTR\_MASK

Saturate interrupt mask register.

Address: 0x403A0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 19.1.69 SAR\_SATURATE\_INTR\_MASKED

Saturate interrupt masked request register

Address: 0x403A022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

## 19.1.70 SAR\_RANGE\_INTR

Range detect interrupt request register.

Address: 0x403A0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

## 19.1.71 SAR\_RANGE\_INTR\_SET

Range detect interrupt set request register

Address: 0x403A0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0



## 19.1.72 SAR\_RANGE\_INTR\_MASK

Range detect interrupt mask register.

Address: 0x403A0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 19.1.73 SAR\_RANGE\_INTR\_MASKED

Range interrupt masked request register

Address: 0x403A023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

## 19.1.74 SAR\_INTR\_CAUSE

Interrupt cause register

Address: 0x403A0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None	R	R	R
HW Access	W	W	W	W	None	W	W	W
Name	INJ_COLLISION_MASKED_MIR	INJ_RANGE_MASKED_MIR	INJ_SATURATE_MASKED_MIR	INJ_EOC_MASKED_MIR	Reserved	FW_COLLISION_MASKED_MIR	OVERFLOW_MASKED_MIR	EOS_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	RANGE_MASKED_RED	SATURATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SATURATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	INJ_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
6	INJ_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
5	INJ_SATURATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
4	INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
3	Reserved	Reserved

2	FW_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	OVERFLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

### 19.1.75 SAR\_INJ\_CHAN\_CONFIG (continued)

### 19.1.75 SAR\_INJ\_CHAN\_CONFIG

Injection channel configuration register.

Address: 0x403A0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	INJ_PORT_ADDR [6:4]			None	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None	INJ_AVG_EN	INJ_RESOLUTION	INJ_DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	INJ_START_EN	INJ_TAILGATING	None [29:24]					

Bits	Name	Description
31	INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default Value: 0
30	INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0

10	INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	INJ_RESOLUTION	Resolution for this channel. Default Value: 0  <b>0x0: 12B:</b> 12-bit resolution is used for this channel.  <b>0x1: SUBRES:</b> The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0  <b>0x0: SARMUX:</b> SARMUX pins.  <b>0x1: CTB0:</b> CTB0  <b>0x2: CTB1:</b> CTB1  <b>0x3: CTB2:</b> CTB2  <b>0x4: CTB3:</b> CTB3  <b>0x6: AROUTE_VIRT:</b> AROUTE virtual port  <b>0x7: SARMUX_VIRT:</b> SARMUX virtual port
2 : 0	INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default Value: 0

## 19.1.76 SAR\_INJ\_RESULT (continued)

## 19.1.76 SAR\_INJ\_RESULT

Injection channel result register

Address: 0x403A0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	INJ_EOC_INTR_MIR	INJ_RANGE_INTR_MIR	INJ_SATURATE_INTR_MIR	INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
30	INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
29	INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
28	INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
15 : 0	INJ_RESULT	SAR conversion result of the channel. Default Value: Undefined

## 19.1.77 SAR\_MUX\_SWITCH0

SARMUX Firmware switch controls

Address: 0x403A0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

  

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUS_B_VMINUS	MUX_FW_AMUXBUS_A_VMINUS	MUX_FW_AMUXBUS_B_VPLUS	MUX_FW_AMUXBUS_A_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

  

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with '1' to set bit. Default Value: 0
28	MUX_FW_P6_COREIO2	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with '1' to set bit. Default Value: 0
27	MUX_FW_P5_COREIO1	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with '1' to set bit. Default Value: 0
26	MUX_FW_P4_COREIO0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with '1' to set bit. Default Value: 0
25	MUX_FW_SARBUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0



24	MUX_FW_SARBUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	MUX_FW_AMUXBUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	MUX_FW_AMUXBUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit. Default Value: 0
16	MUX_FW_VSSA_VMINUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0
15	MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit. Default Value: 0
14	MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit. Default Value: 0
13	MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit. Default Value: 0
12	MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit. Default Value: 0
11	MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit. Default Value: 0
10	MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit. Default Value: 0
9	MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit. Default Value: 0
8	MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit. Default Value: 0

### 19.1.77 SAR\_MUX\_SWITCH0 (continued)

7	MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit. Default Value: 0
6	MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit. Default Value: 0
5	MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit. Default Value: 0
4	MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit. Default Value: 0
3	MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit. Default Value: 0

## 19.1.78 SAR\_MUX\_SWITCH\_CLEAR0 (continued)

## 19.1.78 SAR\_MUX\_SWITCH\_CLEAR0

SARMUX Firmware switch control clear

Address: 0x403A0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
<b>HW Access</b>	A	A	A	A	A	A	A	A
<b>Name</b>	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
<b>SW Access</b>	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
<b>HW Access</b>	A	A	A	A	A	A	A	A
<b>Name</b>	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
<b>SW Access</b>	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
<b>HW Access</b>	A	A	A	A	A	A	A	A
<b>Name</b>	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUS_B_VMINUS	MUX_FW_AMUXBUS_A_VMINUS	MUX_FW_AMUXBUS_B_VPLUS	MUX_FW_AMUXBUS_A_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
<b>SW Access</b>	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
<b>HW Access</b>	None		A	A	A	A	A	A
<b>Name</b>	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
28	MUX_FW_P6_COREIO2	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
27	MUX_FW_P5_COREIO1	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
26	MUX_FW_P4_COREIO0	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

25	MUX_FW_SARBUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUXBUSB_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUXBUSB_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

### 19.1.78 SAR\_MUX\_SWITCH\_CLEAR0 (continued)

2	MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

## 19.1.79 SAR\_MUX\_SWITCH1 (continued)

## 19.1.79 SAR\_MUX\_SWITCH1

SARMUX Firmware switch controls

Address: 0x403A0308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				RW1C	RW1C	RW1C	RW1C
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Firmware control: 0=open, 1=close switch between adft1 signal and sarbus1 signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Firmware control: 0=open, 1=close switch between adft0 signal and sarbus0 signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P5_DFT_INM	Firmware control: 0=open, 1=close switch between P5 pin and dft_inm signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P4_DFT_INP	Firmware control: 0=open, 1=close switch between P4 pin and dft_inp signal. Write with '1' to set bit. Default Value: 0

## 19.1.80 SAR\_MUX\_SWITCH\_CLEAR1

SARMUX Firmware switch control clear

Address: 0x403A030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
1	MUX_FW_P5_DFT_INM	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
0	MUX_FW_P4_DFT_INP	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0

## 19.1.81 SAR\_MUX\_SWITCH\_HW\_CTRL

SARMUX switch hardware control

Address: 0x403A0340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX_HW_CTRL_P7	MUX_HW_CTRL_P6	MUX_HW_CTRL_P5	MUX_HW_CTRL_P4	MUX_HW_CTRL_P3	MUX_HW_CTRL_P2	MUX_HW_CTRL_P1	MUX_HW_CTRL_P0

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX_HW_CTRL_SARBUS1	MUX_HW_CTRL_SARBUS0	None [21:20]		MUX_HW_CTRL_AMUXBUSB	MUX_HW_CTRL_AMUXBUSA	MUX_HW_CTRL_TEMP	MUX_HW_CTRL_VSSA

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_HW_CTRL_SARBUS1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus1 switches. Default Value: 0
22	MUX_HW_CTRL_SARBUS0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus0 switches. Default Value: 0
19	MUX_HW_CTRL_AMUXBUSB	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusb switches. Default Value: 0
18	MUX_HW_CTRL_AMUXBUSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusa switches. Default Value: 0
17	MUX_HW_CTRL_TEMP	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for temp switch. Default Value: 0



16	MUX_HW_CTRL_VSSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for vssa switch. Default Value: 0
7	MUX_HW_CTRL_P7	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P7 switches. Default Value: 0
6	MUX_HW_CTRL_P6	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P6 switches. Default Value: 0
5	MUX_HW_CTRL_P5	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P5 switches. Default Value: 0
4	MUX_HW_CTRL_P4	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P4 switches. Default Value: 0
3	MUX_HW_CTRL_P3	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P3 switches. Default Value: 0
2	MUX_HW_CTRL_P2	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P2 switches. Default Value: 0
1	MUX_HW_CTRL_P1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P1 switches. Default Value: 0
0	MUX_HW_CTRL_P0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P0 switches. Default Value: 0

## 19.1.82 SAR\_MUX\_SWITCH\_STATUS (continued)

## 19.1.82 SAR\_MUX\_SWITCH\_STATUS

SARMUX switch status

Address: 0x403A0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

  

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

  

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUS_B_VMINUS	MUX_FW_AMUXBUS_A_VMINUS	MUX_FW_AMUXBUS_B_VPLUS	MUX_FW_AMUXBUS_A_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

  

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

21	MUX_FW_AMUXBUSB_V MINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUXBUSA_V MINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUSB_V PLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUXBUSA_V PLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMINU S	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

### 19.1.83 SAR\_PUMP\_CTRL (continued)

### 19.1.83 SAR\_PUMP\_CTRL

Switch pump control

Address: 0x403A0380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted. Default Value: 0
0	CLOCK_SEL	Clock select: 0=external clock, 1=internal clock (deprecated). Default Value: 0

## 19.1.84 SAR\_ANA\_TRIM

Analog trim register.

Address: 0x403A0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [7:4]				TRIMUNIT	CAP_TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	TRIMUNIT	Attenuation cap trimming Default Value: 0
2 : 0	CAP_TRIM	Attenuation cap trimming Default Value: 0

## 19.1.85 SAR\_WOUNDING

SAR wounding register

Address: 0x403A0F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	
HW Access	None						R	
Name	None [7:2]						WOUND_RESOLUTION [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	WOUND_RESOLUTION	<p>Maximum SAR resolution allowed Default Value: 0</p> <p><b>0x0: 12BIT:</b> unwounded: up to full 12-bit SAR resolution allowed</p> <p><b>0x1: 10BIT:</b> wounded: max resolution upto 10-bit SAR resolution allowed</p> <p><b>0x2: 8BIT:</b> wounded: only 8-bit SAR resolution allowed</p> <p><b>0x3: 8BIT_TOO:</b> wounded: only 8-bit SAR resolution allowed</p>



## 20 SCB Registers



This section discusses the SCB registers. It lists all the registers in mapping tables, in address order.

### 20.1 Register Details

Register Name	Address
SCB0_CTRL	0x40240000
SCB0_STATUS	0x40240004
SCB0_SPI_CTRL	0x40240020
SCB0_SPI_STATUS	0x40240024
SCB0_UART_CTRL	0x40240040
SCB0_UART_TX_CTRL	0x40240044
SCB0_UART_RX_CTRL	0x40240048
SCB0_UART_RX_STATUS	0x4024004C
SCB0_UART_FLOW_CTRL	0x40240050
SCB0_I2C_CTRL	0x40240060
SCB0_I2C_STATUS	0x40240064
SCB0_I2C_M_CMD	0x40240068
SCB0_I2C_S_CMD	0x4024006C
SCB0_I2C_CFG	0x40240070
SCB0_TX_CTRL	0x40240200
SCB0_TX_FIFO_CTRL	0x40240204
SCB0_TX_FIFO_STATUS	0x40240208
SCB0_TX_FIFO_WR	0x40240240
SCB0_RX_CTRL	0x40240300
SCB0_RX_FIFO_CTRL	0x40240304
SCB0_RX_FIFO_STATUS	0x40240308
SCB0_RX_MATCH	0x40240310
SCB0_RX_FIFO_RD	0x40240340
SCB0_RX_FIFO_RD_SILENT	0x40240344
SCB0_EZ_DATA0	0x40240400
SCB0_EZ_DATA1	0x40240404
SCB0_EZ_DATA2	0x40240408



Register Name	Address
SCB0_EZ_DATA3	0x4024040C
SCB0_EZ_DATA4	0x40240410
SCB0_EZ_DATA5	0x40240414
SCB0_EZ_DATA6	0x40240418
SCB0_EZ_DATA7	0x4024041C
SCB0_EZ_DATA8	0x40240420
SCB0_EZ_DATA9	0x40240424
SCB0_EZ_DATA10	0x40240428
SCB0_EZ_DATA11	0x4024042C
SCB0_EZ_DATA12	0x40240430
SCB0_EZ_DATA13	0x40240434
SCB0_EZ_DATA14	0x40240438
SCB0_EZ_DATA15	0x4024043C
SCB0_EZ_DATA16	0x40240440
SCB0_EZ_DATA17	0x40240444
SCB0_EZ_DATA18	0x40240448
SCB0_EZ_DATA19	0x4024044C
SCB0_EZ_DATA20	0x40240450
SCB0_EZ_DATA21	0x40240454
SCB0_EZ_DATA22	0x40240458
SCB0_EZ_DATA23	0x4024045C
SCB0_EZ_DATA24	0x40240460
SCB0_EZ_DATA25	0x40240464
SCB0_EZ_DATA26	0x40240468
SCB0_EZ_DATA27	0x4024046C
SCB0_EZ_DATA28	0x40240470
SCB0_EZ_DATA29	0x40240474
SCB0_EZ_DATA30	0x40240478
SCB0_EZ_DATA31	0x4024047C
SCB0_INTR_CAUSE	0x40240E00
SCB0_INTR_I2C_EC	0x40240E80
SCB0_INTR_I2C_EC_MASK	0x40240E88
SCB0_INTR_I2C_EC_MASKED	0x40240E8C
SCB0_INTR_SPI_EC	0x40240EC0
SCB0_INTR_SPI_EC_MASK	0x40240EC8
SCB0_INTR_SPI_EC_MASKED	0x40240ECC
SCB0_INTR_M	0x40240F00
SCB0_INTR_M_SET	0x40240F04
SCB0_INTR_M_MASK	0x40240F08
SCB0_INTR_M_MASKED	0x40240F0C
SCB0_INTR_S	0x40240F40
SCB0_INTR_S_SET	0x40240F44

Register Name	Address
SCB0_INTR_S_MASK	0x40240F48
SCB0_INTR_S_MASKED	0x40240F4C
SCB0_INTR_TX	0x40240F80
SCB0_INTR_TX_SET	0x40240F84
SCB0_INTR_TX_MASK	0x40240F88
SCB0_INTR_TX_MASKED	0x40240F8C
SCB0_INTR_RX	0x40240FC0
SCB0_INTR_RX_SET	0x40240FC4
SCB0_INTR_RX_MASK	0x40240FC8
SCB0_INTR_RX_MASKED	0x40240FCC
SCB1_CTRL	0x40250000
SCB1_STATUS	0x40250004
SCB1_SPI_CTRL	0x40250020
SCB1_SPI_STATUS	0x40250024
SCB1_UART_CTRL	0x40250040
SCB1_UART_TX_CTRL	0x40250044
SCB1_UART_RX_CTRL	0x40250048
SCB1_UART_RX_STATUS	0x4025004C
SCB1_UART_FLOW_CTRL	0x40250050
SCB1_I2C_CTRL	0x40250060
SCB1_I2C_STATUS	0x40250064
SCB1_I2C_M_CMD	0x40250068
SCB1_I2C_S_CMD	0x4025006C
SCB1_I2C_CFG	0x40250070
SCB1_TX_CTRL	0x40250200
SCB1_TX_FIFO_CTRL	0x40250204
SCB1_TX_FIFO_STATUS	0x40250208
SCB1_TX_FIFO_WR	0x40250240
SCB1_RX_CTRL	0x40250300
SCB1_RX_FIFO_CTRL	0x40250304
SCB1_RX_FIFO_STATUS	0x40250308
SCB1_RX_MATCH	0x40250310
SCB1_RX_FIFO_RD	0x40250340
SCB1_RX_FIFO_RD_SILENT	0x40250344
SCB1_EZ_DATA0	0x40250400
SCB1_EZ_DATA1	0x40250404
SCB1_EZ_DATA2	0x40250408
SCB1_EZ_DATA3	0x4025040C
SCB1_EZ_DATA4	0x40250410
SCB1_EZ_DATA5	0x40250414
SCB1_EZ_DATA6	0x40250418
SCB1_EZ_DATA7	0x4025041C

Register Name	Address
SCB1_EZ_DATA8	0x40250420
SCB1_EZ_DATA9	0x40250424
SCB1_EZ_DATA10	0x40250428
SCB1_EZ_DATA11	0x4025042C
SCB1_EZ_DATA12	0x40250430
SCB1_EZ_DATA13	0x40250434
SCB1_EZ_DATA14	0x40250438
SCB1_EZ_DATA15	0x4025043C
SCB1_EZ_DATA16	0x40250440
SCB1_EZ_DATA17	0x40250444
SCB1_EZ_DATA18	0x40250448
SCB1_EZ_DATA19	0x4025044C
SCB1_EZ_DATA20	0x40250450
SCB1_EZ_DATA21	0x40250454
SCB1_EZ_DATA22	0x40250458
SCB1_EZ_DATA23	0x4025045C
SCB1_EZ_DATA24	0x40250460
SCB1_EZ_DATA25	0x40250464
SCB1_EZ_DATA26	0x40250468
SCB1_EZ_DATA27	0x4025046C
SCB1_EZ_DATA28	0x40250470
SCB1_EZ_DATA29	0x40250474
SCB1_EZ_DATA30	0x40250478
SCB1_EZ_DATA31	0x4025047C
SCB1_INTR_CAUSE	0x40250E00
SCB1_INTR_I2C_EC	0x40250E80
SCB1_INTR_I2C_EC_MASK	0x40250E88
SCB1_INTR_I2C_EC_MASKED	0x40250E8C
SCB1_INTR_SPI_EC	0x40250EC0
SCB1_INTR_SPI_EC_MASK	0x40250EC8
SCB1_INTR_SPI_EC_MASKED	0x40250ECC
SCB1_INTR_M	0x40250F00
SCB1_INTR_M_SET	0x40250F04
SCB1_INTR_M_MASK	0x40250F08
SCB1_INTR_M_MASKED	0x40250F0C
SCB1_INTR_S	0x40250F40
SCB1_INTR_S_SET	0x40250F44
SCB1_INTR_S_MASK	0x40250F48
SCB1_INTR_S_MASKED	0x40250F4C
SCB1_INTR_TX	0x40250F80
SCB1_INTR_TX_SET	0x40250F84
SCB1_INTR_TX_MASK	0x40250F88

Register Name	Address
SCB1_INTR_TX_MASKED	0x40250F8C
SCB1_INTR_RX	0x40250FC0
SCB1_INTR_RX_SET	0x40250FC4
SCB1_INTR_RX_MASK	0x40250FC8
SCB1_INTR_RX_MASKED	0x40250FCC

## 20.1.1 SCB0\_CTRL

Generic control register.

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OPERATION_MODE	EC_AM_MODE
Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	<p>IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows:</p> <ul style="list-style-type: none"> <li>- Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable.</li> <li>- Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality.</li> <li>- Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information.</li> <li>- Program CTRL to enable IP, select the specific operation mode and oversampling factor.</li> </ul> <p>When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0</p>
25 : 24	MODE	<p>Mode of operation (3: Reserved) Default Value: 3</p> <p><b>0x0: I2C:</b> Inter-Integrated Circuits (I2C) mode.</p>

## 20.1.1 SCB0\_CTRL (continued)

### 0x1: SPI:

Serial Peripheral Interface (SPI) mode.

### 0x2: UART:

Universal Asynchronous Receiver/Transmitter (UART) mode.

17	BLOCK	<p>Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not ('BLOCK is 0'). If BLOCK is 0 and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX.</p> <p>Default Value: 0</p>
16	ADDR_ACCEPT	<p>Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0').</p> <p>In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers.</p> <p>In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO.</p> <p>Default Value: 0</p>
11	BYTE_MODE	<p>Determines the number of bits per FIFO data element:</p> <p>'0': 16-bit FIFO data elements.</p> <p>'1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7].</p> <p>Default Value: 0</p>
10	EZ_MODE	<p>Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first.</p> <p>In UART mode this field should be '0'.</p> <p>Default Value: 0</p>
9	EC_OP_MODE	<p>Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate).</p> <p>In UART mode this field should be '0'.</p> <p>Default Value: 0</p>

### 20.1.1 SCB0\_CTRL (continued)

8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported.
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In UART mode this field should be '0'.  
Default Value: 0

## 20.1.1 SCB0\_CTRL (continued)

3 : 0 OVS

Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period.

In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi\_clk\_out" to SPI MISO input "spi\_miso\_in" round trip delay is introducing significant delays (multiple "spi\_clk\_out" cycles), it may be necessary to increase OVS and/or to set SPI\_CTRL.LATE\_MISO\_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX\_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI\_CTRL.LATE\_MISO\_SAMPLE):

- MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps.
- MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps.
- MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps.
- MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps.

The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:

- 0: 16 times oversampling.
  - IP clock frequency of 16\*115.2 KHz for 115.2 Kbps.
  - IP clock frequency of 16\*57.6 KHz for 57.6 Kbps.
  - IP clock frequency of 16\*38.4 KHz for 38.4 Kbps.
  - IP clock frequency of 16\*19.2 KHz for 19.2 Kbps.
  - IP clock frequency of 16\*9.6 KHz for 9.6 Kbps.
  - IP clock frequency of 16\*2.4 KHz for 2.4 Kbps.
  - IP clock frequency of 16\*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX\_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency):

- 0: 16 times oversampling.
  - IP clock frequency of 16\*115.2 KHz for 115.2 Kbps.
  - IP clock frequency of 16\*57.6 KHz for 57.6 Kbps.
  - IP clock frequency of 16\*38.4 KHz for 38.4 Kbps.
  - IP clock frequency of 16\*19.2 KHz for 19.2 Kbps.
  - IP clock frequency of 16\*9.6 KHz for 9.6 Kbps.
  - IP clock frequency of 16\*2.4 KHz for 2.4 Kbps.
  - IP clock frequency of 16\*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

Low power mode, OVS field values (with the required IP clock frequency):

- 0: 16 times oversampling.
  - IP clock frequency of 16\*115.2 KHz for 115.2 Kbps.
- 1: 32 times oversampling.
  - IP clock frequency of 32\*57.6 KHz for 57.6 Kbps.
- 2: 48 times oversampling.
  - IP clock frequency of 48\*38.4 KHz for 38.4 Kbps.
- 3: 96 times oversampling.
  - IP clock frequency of 96\*19.2 KHz for 19.2 Kbps.
- 4: 192 times oversampling.
  - IP clock frequency of 192\*9.6 KHz for 9.6 Kbps.
- 5: 768 times oversampling.
  - IP clock frequency of 768\*2.4 KHz for 2.4 Kbps.
- 6: 1536 times oversampling.
  - IP clock frequency of 1536\*1.2 KHz for 1.2 Kbps.
- all other values are not used in low power mode.

Default Value: 15



## 20.1.2 SCB0\_STATUS

Generic status register.

Address: 0x40240004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

## 20.1.3 SCB0\_SPI\_CTRL

SPI control register.

Address: 0x40240020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_P RECEDE	CONTINUOUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POL ARITY3	SSEL_POL ARITY2	SSEL_POL ARITY1	SSEL_POL ARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

### 20.1.3 SCB0\_SPI\_CTRL (continued)

#### 0x0: SPI\_MOTOROLA:

SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.

#### 0x1: SPI\_TI:

SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated.

#### 0x2: SPI\_NS:

SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.

16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

### 20.1.3 SCB0\_SPI\_CTRL (continued)

4	LATE_MISO_SAMPLE	<p>Changes the SCLK edge on which MISO is captured. Only used in master mode.</p> <p>When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK).</p> <p>When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.</p> <p>Default Value: 0</p>
3	CPOL	<p>Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured:</p> <ul style="list-style-type: none"> <li>- CPOL is 0: SCLK is 0 when not transmitting data.</li> <li>- CPOL is 1: SCLK is 1 when not transmitting data.</li> </ul> <p>Default Value: 0</p>
2	CPHA	<p>Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured:</p> <ul style="list-style-type: none"> <li>- Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.</li> <li>- Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK.</li> <li>- Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK.</li> <li>- Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.</li> </ul> <p>Default Value: 0</p>
1	SELECT_PRECEDE	<p>Only used in SPI Texas Instruments' submode.</p> <p>When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit.</p> <p>When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit.</p> <p>Default Value: 0</p>
0	CONTINUOUS	<p>Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field.</p> <p>When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are sent out without slave deselection.</p> <p>When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are sent out with slave deselection.</p> <p>Default Value: 0</p>

## 20.1.4 SCB0\_SPI\_STATUS

SPI status register.

Address: 0x40240024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

## 20.1.5 SCB0\_UART\_CTRL

UART control register.

Address: 0x40240040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK
Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	<p>Submode of UART operation (3: Reserved) Default Value: 3</p> <p><b>0x0: UART_STD:</b> Standard UART submode.</p> <p><b>0x1: UART_SMARTCARD:</b> SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side.</p> <p><b>0x2: UART_IRDA:</b> Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.</p>
16	LOOPBACK	<p>Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in".</p> <p>This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0</p>

## 20.1.6 SCB0\_UART\_TX\_CTRL

UART transmitter control register.

Address: 0x40240044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

## 20.1.7 SCB0\_UART\_RX\_CTRL

UART receiver control register.

Address: 0x40240048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

  

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

  

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	<p>Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value.</p> <p>Default Value: 10</p>



## 20.1.7 SCB0\_UART\_RX\_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERR OR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERR OR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

## 20.1.7 SCB0\_UART\_RX\_CTRL (continued)

2 : 0	STOP_BITS	<p>Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value.</p> <p>Default Value: 2</p>
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## 20.1.8 SCB0\_UART\_RX\_STATUS

UART receiver status register.

Address: 0x4024004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

## 20.1.9 SCB0\_UART\_FLOW\_CTRL

UART flow control register

Address: 0x40240050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	<p>Enable use of CTS input signal "uart_cts_in" by the UART transmitter:</p> <p>'0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register.</p> <p>'1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register.</p> <p>If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY).</p> <p>Default Value: 0</p>
24	CTS_POLARITY	<p>Polarity of the CTS input signal "uart_cts_in":</p> <p>'0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive.</p> <p>'1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive.</p> <p>Default Value: 0</p>

## 20.1.9 SCB0\_UART\_FLOW\_CTRL (continued)

16	RTS_POLARITY	<p>Polarity of the RTS output signal "uart_rts_out":</p> <p>'0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive.</p> <p>'1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive.</p> <p>During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity.</p> <p>Default Value: 0</p>
3 : 0	TRIGGER_LEVEL	<p>Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes).</p> <p>Default Value: 0</p>

## 20.1.10 SCB0\_I2C\_CTRL

I2C control register.

Address: 0x40240060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

## 20.1.10 SCB0\_I2C\_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	<p>For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when:</p> <ul style="list-style-type: none"> <li>- EC_AM is '0', EC_OP is '0' and non EZ mode.</li> </ul> <p>Functionality is as follows:</p> <ul style="list-style-type: none"> <li>- 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full.</li> <li>- 0: clock stretching is performed (till the receiver FIFO is no longer full).</li> </ul> <p>For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode):</p> <ul style="list-style-type: none"> <li>- EC_AM is '1' and EC_OP is '0'.</li> <li>- EC_AM is '1' and general call address match.</li> <li>- EC_AM is '1' and non EZ mode.</li> </ul> <p>Functionality is as follows:</p> <ul style="list-style-type: none"> <li>- 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode).</li> <li>- 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled.</li> </ul> <p>Default Value: 1</p>
13	S_READY_DATA_ACK	<p>When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.</p> <p>Default Value: 1</p>
12	S_READY_ADDR_ACK	<p>When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.</p> <p>Default Value: 1</p>
11	S_GENERAL_IGNORE	<p>When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure.</p> <p>Default Value: 1</p>
9	M_NOT_READY_DATA_NACK	<p>When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full).</p> <p>Default Value: 1</p>
8	M_READY_DATA_ACK	<p>When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full.</p> <p>Default Value: 1</p>
7 : 4	LOW_PHASE_OVS	<p>Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering.</p> <p>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be <math>\geq 8</math> IP clock cycles and <math>\leq 16</math> IP clock cycles. Without input signal median filtering, the IF low time should be <math>\geq 7</math> IP clock cycles and <math>\leq 16</math> IP clock cycles.</p> <p>Default Value: 8</p>

### 20.1.10 SCB0\_I2C\_CTRL (continued)

3 : 0	HIGH_PHASE_OVS	<p>Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering.</p> <p>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be <math>\geq 6</math> IP clock cycles and <math>\leq 16</math> IP clock cycles. Without input signal median filtering, the IF high time should be <math>\geq 5</math> IP clock cycles and <math>\leq 16</math> IP clock cycles.</p> <p>Default Value: 8</p>
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## 20.1.11 SCB0\_I2C\_STATUS

I2C status register.

Address: 0x40240064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/ idle or transmitting START, REPEATED START, STOP or an address, this field is '0'. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0'. Default Value: 0

## 20.1.11 SCB0\_I2C\_STATUS (continued)

1	I2C_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	<p>I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period).</p> <p>For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions).</p> <p>For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0</p>

## 20.1.12 SCB0\_I2C\_M\_CMD

I2C master command register.

Address: 0x40240068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0'). A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

### 20.1.12 SCB0\_I2C\_M\_CMD (continued)

0	M_START	<p>When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0</p>
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## 20.1.13 SCB0\_I2C\_S\_CMD

I2C slave command register.

Address: 0x4024006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

## 20.1.14 SCB0\_I2C\_CFG

I2C configuration register.

Address: 0x40240070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILTER_SEL	None [3:2]		SDA_IN_FILTER_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILTER_SEL	None [11:10]		SCL_IN_FILTER_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILTER2_TRIM [21:20]		SDA_OUT_FILTER1_TRIM [19:18]		SDA_OUT_FILTER0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILTER_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILTER_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILTER2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
19 : 18	SDA_OUT_FILTER1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
17 : 16	SDA_OUT_FILTER0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2

### 20.1.14 SCB0\_I2C\_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1': 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1': 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 3

## 20.1.15 SCB0\_TX\_CTRL

Transmitter control register.

Address: 0x40240200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7



## 20.1.16 SCB0\_TX\_FIFO\_CTRL

Transmitter FIFO control register.

Address: 0x40240204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

## 20.1.17 SCB0\_TX\_FIFO\_STATUS

Transmitter FIFO status register.

Address: 0x40240208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				
Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						
Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

## 20.1.18 SCB0\_TX\_FIFO\_WR

Transmitter FIFO write register.

Address: 0x40240240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	<p>Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used.</p> <p>A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0</p>

## 20.1.19 SCB0\_RX\_CTRL

Receiver control register.

Address: 0x40240300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

## 20.1.20 SCB0\_RX\_FIFO\_CTRL

Receiver FIFO control register.

Address: 0x40240304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

## 20.1.21 SCB0\_RX\_FIFO\_STATUS

Receiver FIFO status register.

Address: 0x40240308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

## 20.1.22 SCB0\_RX\_MATCH

Slave address and mask register.

Address: 0x40240310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address.  In UART multi-processor mode, all 8 bits are used.  In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

## 20.1.23 SCB0\_RX\_FIFO\_RD

Receiver FIFO read register.

Address: 0x40240340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	<p>Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used.</p> <p>This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register.</p> <p>A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined</p>



## 20.1.24 SCB0\_RX\_FIFO\_RD\_SILENT

Receiver FIFO read register.

Address: 0x40240344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	<p>Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used.</p> <p>A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'.</p> <p>Default Value: Undefined</p>

## 20.1.25 SCB0\_EZ\_DATA0

Memory buffer registers.

Address: 0x40240400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.26 SCB0\_EZ\_DATA1

Memory buffer registers.

Address: 0x40240404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.27 SCB0\_EZ\_DATA2

Memory buffer registers.

Address: 0x40240408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.28 SCB0\_EZ\_DATA3

Memory buffer registers.

Address: 0x4024040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.29 SCB0\_EZ\_DATA4

Memory buffer registers.

Address: 0x40240410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.30 SCB0\_EZ\_DATA5

Memory buffer registers.

Address: 0x40240414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.31 SCB0\_EZ\_DATA6

Memory buffer registers.

Address: 0x40240418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.32 SCB0\_EZ\_DATA7

Memory buffer registers.

Address: 0x4024041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.33 SCB0\_EZ\_DATA8

Memory buffer registers.

Address: 0x40240420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.34 SCB0\_EZ\_DATA9

Memory buffer registers.

Address: 0x40240424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.35 SCB0\_EZ\_DATA10

Memory buffer registers.

Address: 0x40240428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.36 SCB0\_EZ\_DATA11

Memory buffer registers.

Address: 0x4024042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.37 SCB0\_EZ\_DATA12

Memory buffer registers.

Address: 0x40240430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.38 SCB0\_EZ\_DATA13

Memory buffer registers.

Address: 0x40240434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.39 SCB0\_EZ\_DATA14

Memory buffer registers.

Address: 0x40240438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.40 SCB0\_EZ\_DATA15

Memory buffer registers.

Address: 0x4024043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.41 SCB0\_EZ\_DATA16

Memory buffer registers.

Address: 0x40240440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.42 SCB0\_EZ\_DATA17

Memory buffer registers.

Address: 0x40240444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.43 SCB0\_EZ\_DATA18

Memory buffer registers.

Address: 0x40240448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.44 SCB0\_EZ\_DATA19

Memory buffer registers.

Address: 0x4024044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.45 SCB0\_EZ\_DATA20

Memory buffer registers.

Address: 0x40240450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.46 SCB0\_EZ\_DATA21

Memory buffer registers.

Address: 0x40240454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.47 SCB0\_EZ\_DATA22

Memory buffer registers.

Address: 0x40240458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.48 SCB0\_EZ\_DATA23

Memory buffer registers.

Address: 0x4024045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.49 SCB0\_EZ\_DATA24

Memory buffer registers.

Address: 0x40240460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.50 SCB0\_EZ\_DATA25

Memory buffer registers.

Address: 0x40240464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.51 SCB0\_EZ\_DATA26

Memory buffer registers.

Address: 0x40240468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.52 SCB0\_EZ\_DATA27

Memory buffer registers.

Address: 0x4024046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.53 SCB0\_EZ\_DATA28

Memory buffer registers.

Address: 0x40240470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.54 SCB0\_EZ\_DATA29

Memory buffer registers.

Address: 0x40240474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.55 SCB0\_EZ\_DATA30

Memory buffer registers.

Address: 0x40240478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.56 SCB0\_EZ\_DATA31

Memory buffer registers.

Address: 0x4024047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.57 SCB0\_INTR\_CAUSE

Active clocked interrupt signal register

Address: 0x40240E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

## 20.1.58 SCB0\_INTR\_I2C\_EC

Externally clocked I2C interrupt request register

Address: 0x40240E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	<p>STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from.</p> <p>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0</p>
2	EZ_WRITE_STOP	<p>STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event.</p> <p>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0</p>
1	EZ_STOP	<p>STOP detection. Activated on the end of a every transfer (I2C STOP).</p> <p>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0</p>

### 20.1.58 SCB0\_INTR\_I2C\_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match).  Only used when EC_AM is '1'. Default Value: 0
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## 20.1.59 SCB0\_INTR\_I2C\_EC\_MASK

Externally clocked I2C interrupt mask register

Address: 0x40240E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.60 SCB0\_INTR\_I2C\_EC\_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40240E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.61 SCB0\_INTR\_SPI\_EC

Externally clocked SPI interrupt request register

Address: 0x40240EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	<p>STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from.</p> <p>Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0</p>
2	EZ_WRITE_STOP	<p>STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event.</p> <p>Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0</p>
1	EZ_STOP	<p>STOP detection. Activated on the end of a every transfer (SPI deselection).</p> <p>Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0</p>

### 20.1.61 SCB0\_INTR\_SPI\_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'.  Only used when EC_AM is '1'. Default Value: 0
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## 20.1.62 SCB0\_INTR\_SPI\_EC\_MASK

Externally clocked SPI interrupt mask register

Address: 0x40240EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.63 SCB0\_INTR\_SPI\_EC\_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40240ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.64 SCB0\_INTR\_M

Master interrupt request register.

Address: 0x40240F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

### 20.1.64 SCB0\_INTR\_M (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0
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## 20.1.65 SCB0\_INTR\_M\_SET

Master interrupt set request register

Address: 0x40240F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.66 SCB0\_INTR\_M\_MASK

Master interrupt mask register.

Address: 0x40240F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.67 SCB0\_INTR\_M\_MASKED

Master interrupt masked request register

Address: 0x40240F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.68 SCB0\_INTR\_S

Slave interrupt request register.

Address: 0x40240F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

  

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0



## 20.1.68 SCB0\_INTR\_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected.  In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.  The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.  In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd.  In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

## 20.1.69 SCB0\_INTR\_S\_SET

Slave interrupt set request register.

Address: 0x40240F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.69 SCB0\_INTR\_S\_SET (continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.70 SCB0\_INTR\_S\_MASK

Slave interrupt mask register.

Address: 0x40240F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

### 20.1.70 SCB0\_INTR\_S\_MASK (continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.71 SCB0\_INTR\_S\_MASKED

Slave interrupt masked request register

Address: 0x40240F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

### 20.1.71 SCB0\_INTR\_S\_MASKED (continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.72 SCB0\_INTR\_TX

Transmitter interrupt request register.

Address: 0x40240F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

  

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0



## 20.1.72 SCB0\_INTR\_TX (continued)

6	UNDERFLOW	<p>Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'.</p> <p>Only used in FIFO mode. Default Value: 0</p>
5	OVERFLOW	<p>Attempt to write to a full TX FIFO.</p> <p>Only used in FIFO mode. Default Value: 0</p>
4	EMPTY	<p>TX FIFO is empty; i.e. it has 0 entries.</p> <p>Only used in FIFO mode. Default Value: 0</p>
1	NOT_FULL	<p>TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR.</p> <p>Only used in FIFO mode. Default Value: 0</p>
0	TRIGGER	<p>Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.</p> <p>Only used in FIFO mode. Default Value: 0</p>

## 20.1.73 SCB0\_INTR\_TX\_SET

Transmitter interrupt set request register

Address: 0x40240F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

**20.1.73 SCB0\_INTR\_TX\_SET** (continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.74 SCB0\_INTR\_TX\_MASK

Transmitter interrupt mask register.

Address: 0x40240F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

**20.1.74 SCB0\_INTR\_TX\_MASK** (continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.75 SCB0\_INTR\_TX\_MASKED

Transmitter interrupt masked request register

Address: 0x40240F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

**20.1.75 SCB0\_INTR\_TX\_MASKED** (continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.76 SCB0\_INTR\_RX

Receiver interrupt request register.

Address: 0x40240FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0



## 20.1.76 SCB0\_INTR\_RX (continued)

9	PARITY_ERROR	<p>Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO.</p> <p>Default Value: 0</p>
8	FRAME_ERROR	<p>Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error:</p> <p>Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received.</p> <p>Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received.</p> <p>A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames.</p> <p>Default Value: 0</p>
7	BLOCKED	<p>AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'.</p> <p>Default Value: 0</p>
6	UNDERFLOW	<p>Attempt to read from an empty RX FIFO.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
5	OVERFLOW	<p>Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
3	FULL	<p>RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET:</p> <p>BYTE_MODE is '0': # entries == FF_DATA_NR/2.</p> <p>BYTE_MODE is '1': # entries == FF_DATA_NR.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
2	NOT_EMPTY	<p>RX FIFO is not empty.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
0	TRIGGER	<p>More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>

## 20.1.77 SCB0\_INTR\_RX\_SET

Receiver interrupt set request register.

Address: 0x40240FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

**20.1.77 SCB0\_INTR\_RX\_SET** (continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.78 SCB0\_INTR\_RX\_MASK

Receiver interrupt mask register.

Address: 0x40240FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

**20.1.78 SCB0\_INTR\_RX\_MASK** (continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.79 SCB0\_INTR\_RX\_MASKED

Receiver interrupt masked request register

Address: 0x40240FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

**20.1.79 SCB0\_INTR\_RX\_MASKED** (continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.80 SCB1\_CTRL

Generic control register.

Address: 0x40250000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OPERATION_MODE	EC_AM_MODE
Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT
Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	<p>IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows:</p> <ul style="list-style-type: none"> <li>- Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable.</li> <li>- Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality.</li> <li>- Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information.</li> <li>- Program CTRL to enable IP, select the specific operation mode and oversampling factor.</li> </ul> <p>When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0</p>
25 : 24	MODE	<p>Mode of operation (3: Reserved) Default Value: 3</p> <p><b>0x0: I2C:</b> Inter-Integrated Circuits (I2C) mode.</p>



## 20.1.80 SCB1\_CTRL (continued)

### 0x1: SPI:

Serial Peripheral Interface (SPI) mode.

### 0x2: UART:

Universal Asynchronous Receiver/Transmitter (UART) mode.

17	BLOCK	<p>Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not ('BLOCK is 0'). IF BLOCK is 0 and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX.</p> <p>Default Value: 0</p>
16	ADDR_ACCEPT	<p>Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0').</p> <p>In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers.</p> <p>In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO.</p> <p>Default Value: 0</p>
11	BYTE_MODE	<p>Determines the number of bits per FIFO data element:</p> <p>'0': 16-bit FIFO data elements.</p> <p>'1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7].</p> <p>Default Value: 0</p>
10	EZ_MODE	<p>Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first.</p> <p>In UART mode this field should be '0'.</p> <p>Default Value: 0</p>
9	EC_OP_MODE	<p>Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate).</p> <p>In UART mode this field should be '0'.</p> <p>Default Value: 0</p>

## 20.1.80 SCB1\_CTRL (continued)

8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported.
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In UART mode this field should be '0'.

Default Value: 0

## 20.1.80 SCB1\_CTRL (continued)

3 : 0 OVS

Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period.

In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi\_clk\_out" to SPI MISO input "spi\_miso\_in" round trip delay is introducing significant delays (multiple "spi\_clk\_out" cycles), it may be necessary to increase OVS and/or to set SPI\_CTRL.LATE\_MISO\_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX\_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI\_CTRL.LATE\_MISO\_SAMPLE):

- MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps.
- MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps.
- MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps.
- MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps.

The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account.

In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15].

In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value:

- 0: 16 times oversampling.
  - IP clock frequency of 16\*115.2 KHz for 115.2 Kbps.
  - IP clock frequency of 16\*57.6 KHz for 57.6 Kbps.
  - IP clock frequency of 16\*38.4 KHz for 38.4 Kbps.
  - IP clock frequency of 16\*19.2 KHz for 19.2 Kbps.
  - IP clock frequency of 16\*9.6 KHz for 9.6 Kbps.
  - IP clock frequency of 16\*2.4 KHz for 2.4 Kbps.
  - IP clock frequency of 16\*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX\_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency):

- 0: 16 times oversampling.
  - IP clock frequency of 16\*115.2 KHz for 115.2 Kbps.
  - IP clock frequency of 16\*57.6 KHz for 57.6 Kbps.
  - IP clock frequency of 16\*38.4 KHz for 38.4 Kbps.
  - IP clock frequency of 16\*19.2 KHz for 19.2 Kbps.
  - IP clock frequency of 16\*9.6 KHz for 9.6 Kbps.
  - IP clock frequency of 16\*2.4 KHz for 2.4 Kbps.
  - IP clock frequency of 16\*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

Low power mode, OVS field values (with the required IP clock frequency):

- 0: 16 times oversampling.
  - IP clock frequency of 16\*115.2 KHz for 115.2 Kbps.
- 1: 32 times oversampling.
  - IP clock frequency of 32\*57.6 KHz for 57.6 Kbps.
- 2: 48 times oversampling.
  - IP clock frequency of 48\*38.4 KHz for 38.4 Kbps.
- 3: 96 times oversampling.
  - IP clock frequency of 96\*19.2 KHz for 19.2 Kbps.
- 4: 192 times oversampling.
  - IP clock frequency of 192\*9.6 KHz for 9.6 Kbps.
- 5: 768 times oversampling.
  - IP clock frequency of 768\*2.4 KHz for 2.4 Kbps.
- 6: 1536 times oversampling.
  - IP clock frequency of 1536\*1.2 KHz for 1.2 Kbps.
- all other values are not used in low power mode.

Default Value: 15

## 20.1.81 SCB1\_STATUS

Generic status register.

Address: 0x40250004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

## 20.1.82 SCB1\_SPI\_CTRL

SPI control register.

Address: 0x40250020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_P RECEDE	CONTINUOUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POL ARITY3	SSEL_POL ARITY2	SSEL_POL ARITY1	SSEL_POL ARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

## 20.1.82 SCB1\_SPI\_CTRL (continued)

### 0x0: SPI\_MOTOROLA:

SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.

### 0x1: SPI\_TI:

SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated.

### 0x2: SPI\_NS:

SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.

16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

## 20.1.82 SCB1\_SPI\_CTRL (continued)

4	LATE_MISO_SAMPLE	<p>Changes the SCLK edge on which MISO is captured. Only used in master mode.</p> <p>When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK).</p> <p>When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.</p> <p>Default Value: 0</p>
3	CPOL	<p>Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured:</p> <ul style="list-style-type: none"> <li>- CPOL is 0: SCLK is 0 when not transmitting data.</li> <li>- CPOL is 1: SCLK is 1 when not transmitting data.</li> </ul> <p>Default Value: 0</p>
2	CPHA	<p>Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured:</p> <ul style="list-style-type: none"> <li>- Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.</li> <li>- Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK.</li> <li>- Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK.</li> <li>- Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK.</li> </ul> <p>Default Value: 0</p>
1	SELECT_PRECEDE	<p>Only used in SPI Texas Instruments' submode.</p> <p>When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit.</p> <p>When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit.</p> <p>Default Value: 0</p>
0	CONTINUOUS	<p>Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field.</p> <p>When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are sent out without slave deselection.</p> <p>When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are sent out with slave deselection.</p> <p>Default Value: 0</p>

## 20.1.83 SCB1\_SPI\_STATUS

SPI status register.

Address: 0x40250024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined



## 20.1.84 SCB1\_UART\_CTRL

UART control register.

Address: 0x40250040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK
Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	<p>Submode of UART operation (3: Reserved) Default Value: 3</p> <p><b>0x0: UART_STD:</b> Standard UART submode.</p> <p><b>0x1: UART_SMARTCARD:</b> SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side.</p> <p><b>0x2: UART_IRDA:</b> Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.</p>
16	LOOPBACK	<p>Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in".</p> <p>This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0</p>

## 20.1.85 SCB1\_UART\_TX\_CTRL

UART transmitter control register.

Address: 0x40250044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

## 20.1.86 SCB1\_UART\_RX\_CTRL

UART receiver control register.

Address: 0x40250048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	<p>Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of <math>10+1 = 11</math> bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value.</p> <p>Default Value: 10</p>

## 20.1.86 SCB1\_UART\_RX\_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERR OR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERR OR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

## 20.1.86 SCB1\_UART\_RX\_CTRL (continued)

2 : 0	STOP_BITS	<p>Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value.</p> <p>Default Value: 2</p>
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## 20.1.87 SCB1\_UART\_RX\_STATUS

UART receiver status register.

Address: 0x4025004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

## 20.1.88 SCB1\_UART\_FLOW\_CTRL

UART flow control register

Address: 0x40250050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	<p>Enable use of CTS input signal "uart_cts_in" by the UART transmitter:</p> <p>'0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register.</p> <p>'1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register.</p> <p>If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY).</p> <p>Default Value: 0</p>
24	CTS_POLARITY	<p>Polarity of the CTS input signal "uart_cts_in":</p> <p>'0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive.</p> <p>'1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive.</p> <p>Default Value: 0</p>

## 20.1.88 SCB1\_UART\_FLOW\_CTRL (continued)

16	RTS_POLARITY	<p>Polarity of the RTS output signal "uart_rts_out":</p> <p>'0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive.</p> <p>'1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive.</p> <p>During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity.</p> <p>Default Value: 0</p>
3 : 0	TRIGGER_LEVEL	<p>Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes).</p> <p>Default Value: 0</p>



## 20.1.89 SCB1\_I2C\_CTRL

I2C control register.

Address: 0x40250060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

## 20.1.89 SCB1\_I2C\_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	<p>For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when:</p> <ul style="list-style-type: none"> <li>- EC_AM is '0', EC_OP is '0' and non EZ mode.</li> </ul> <p>Functionality is as follows:</p> <ul style="list-style-type: none"> <li>- 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full.</li> <li>- 0: clock stretching is performed (till the receiver FIFO is no longer full).</li> </ul> <p>For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode):</p> <ul style="list-style-type: none"> <li>- EC_AM is '1' and EC_OP is '0'.</li> <li>- EC_AM is '1' and general call address match.</li> <li>- EC_AM is '1' and non EZ mode.</li> </ul> <p>Functionality is as follows:</p> <ul style="list-style-type: none"> <li>- 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode).</li> <li>- 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled.</li> </ul> <p>Default Value: 1</p>
13	S_READY_DATA_ACK	<p>When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.</p> <p>Default Value: 1</p>
12	S_READY_ADDR_ACK	<p>When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'.</p> <p>Default Value: 1</p>
11	S_GENERAL_IGNORE	<p>When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure.</p> <p>Default Value: 1</p>
9	M_NOT_READY_DATA_NACK	<p>When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full).</p> <p>Default Value: 1</p>
8	M_READY_DATA_ACK	<p>When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full.</p> <p>Default Value: 1</p>
7 : 4	LOW_PHASE_OVS	<p>Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering.</p> <p>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be <math>\geq 8</math> IP clock cycles and <math>\leq 16</math> IP clock cycles. Without input signal median filtering, the IF low time should be <math>\geq 7</math> IP clock cycles and <math>\leq 16</math> IP clock cycles.</p> <p>Default Value: 8</p>

## 20.1.89 SCB1\_I2C\_CTRL (continued)

3 : 0	HIGH_PHASE_OVS	<p>Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering.</p> <p>The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be <math>\geq 6</math> IP clock cycles and <math>\leq 16</math> IP clock cycles. Without input signal median filtering, the IF high time should be <math>\geq 5</math> IP clock cycles and <math>\leq 16</math> IP clock cycles.</p> <p>Default Value: 8</p>
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## 20.1.90 SCB1\_I2C\_STATUS

I2C status register.

Address: 0x40250064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/ idle or transmitting START, REPEATED START, STOP or an address, this field is '0'. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0'. Default Value: 0

## 20.1.90 SCB1\_I2C\_STATUS (continued)

1	I2C_EC_BUSY	<p>Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable.</p> <p>Default Value: Undefined</p>
0	BUS_BUSY	<p>I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period).</p> <p>For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions).</p> <p>For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions).</p> <p>Default Value: 0</p>

## 20.1.91 SCB1\_I2C\_M\_CMD

I2C master command register.

Address: 0x40250068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0'). A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

### 20.1.91 SCB1\_I2C\_M\_CMD (continued)

0	M_START	<p>When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0</p>
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## 20.1.92 SCB1\_I2C\_S\_CMD

I2C slave command register.

Address: 0x4025006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0



## 20.1.93 SCB1\_I2C\_CFG

I2C configuration register.

Address: 0x40250070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILTER_SEL	None [3:2]		SDA_IN_FILTER_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILTER_SEL	None [11:10]		SCL_IN_FILTER_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILTER2_TRIM [21:20]		SDA_OUT_FILTER1_TRIM [19:18]		SDA_OUT_FILTER0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILTER_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILTER_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILTER2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
19 : 18	SDA_OUT_FILTER1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
17 : 16	SDA_OUT_FILTER0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2

### 20.1.93 SCB1\_I2C\_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1': 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1': 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 3

## 20.1.94 SCB1\_TX\_CTRL

Transmitter control register.

Address: 0x40250200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

## 20.1.95 SCB1\_TX\_FIFO\_CTRL

Transmitter FIFO control register.

Address: 0x40250204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

## 20.1.96 SCB1\_TX\_FIFO\_STATUS

Transmitter FIFO status register.

Address: 0x40250208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				
Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						
Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

## 20.1.97 SCB1\_TX\_FIFO\_WR

Transmitter FIFO write register.

Address: 0x40250240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	<p>Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used.</p> <p>A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0</p>

## 20.1.98 SCB1\_RX\_CTRL

Receiver control register.

Address: 0x40250300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

## 20.1.99 SCB1\_RX\_FIFO\_CTRL

Receiver FIFO control register.

Address: 0x40250304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0



## 20.1.100 SCB1\_RX\_FIFO\_STATUS

Receiver FIFO status register.

Address: 0x40250308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

## 20.1.101 SCB1\_RX\_MATCH

Slave address and mask register.

Address: 0x40250310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address.  In UART multi-processor mode, all 8 bits are used.  In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

## 20.1.102 SCB1\_RX\_FIFO\_RD

Receiver FIFO read register.

Address: 0x40250340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	<p>Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used.</p> <p>This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register.</p> <p>A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined</p>

## 20.1.103 SCB1\_RX\_FIFO\_RD\_SILENT

Receiver FIFO read register.

Address: 0x40250344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	<p>Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used.</p> <p>A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'.</p> <p>Default Value: Undefined</p>

## 20.1.104 SCB1\_EZ\_DATA0

Memory buffer registers.

Address: 0x40250400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.105 SCB1\_EZ\_DATA1

Memory buffer registers.

Address: 0x40250404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.106 SCB1\_EZ\_DATA2

Memory buffer registers.

Address: 0x40250408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.107 SCB1\_EZ\_DATA3

Memory buffer registers.

Address: 0x4025040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.108 SCB1\_EZ\_DATA4

Memory buffer registers.

Address: 0x40250410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.109 SCB1\_EZ\_DATA5

Memory buffer registers.

Address: 0x40250414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.110 SCB1\_EZ\_DATA6

Memory buffer registers.

Address: 0x40250418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.111 SCB1\_EZ\_DATA7

Memory buffer registers.

Address: 0x4025041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.112 SCB1\_EZ\_DATA8

Memory buffer registers.

Address: 0x40250420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.113 SCB1\_EZ\_DATA9

Memory buffer registers.

Address: 0x40250424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.114 SCB1\_EZ\_DATA10

Memory buffer registers.

Address: 0x40250428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.115 SCB1\_EZ\_DATA11

Memory buffer registers.

Address: 0x4025042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.116 SCB1\_EZ\_DATA12

Memory buffer registers.

Address: 0x40250430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.117 SCB1\_EZ\_DATA13

Memory buffer registers.

Address: 0x40250434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.118 SCB1\_EZ\_DATA14

Memory buffer registers.

Address: 0x40250438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.119 SCB1\_EZ\_DATA15

Memory buffer registers.

Address: 0x4025043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.120 SCB1\_EZ\_DATA16

Memory buffer registers.

Address: 0x40250440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.121 SCB1\_EZ\_DATA17

Memory buffer registers.

Address: 0x40250444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.122 SCB1\_EZ\_DATA18

Memory buffer registers.

Address: 0x40250448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.123 SCB1\_EZ\_DATA19

Memory buffer registers.

Address: 0x4025044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.124 SCB1\_EZ\_DATA20

Memory buffer registers.

Address: 0x40250450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.125 SCB1\_EZ\_DATA21

Memory buffer registers.

Address: 0x40250454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.126 SCB1\_EZ\_DATA22

Memory buffer registers.

Address: 0x40250458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.127 SCB1\_EZ\_DATA23

Memory buffer registers.

Address: 0x4025045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.128 SCB1\_EZ\_DATA24

Memory buffer registers.

Address: 0x40250460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.129 SCB1\_EZ\_DATA25

Memory buffer registers.

Address: 0x40250464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.130 SCB1\_EZ\_DATA26

Memory buffer registers.

Address: 0x40250468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.131 SCB1\_EZ\_DATA27

Memory buffer registers.

Address: 0x4025046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined



## 20.1.132 SCB1\_EZ\_DATA28

Memory buffer registers.

Address: 0x40250470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.133 SCB1\_EZ\_DATA29

Memory buffer registers.

Address: 0x40250474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.134 SCB1\_EZ\_DATA30

Memory buffer registers.

Address: 0x40250478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.135 SCB1\_EZ\_DATA31

Memory buffer registers.

Address: 0x4025047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

## 20.1.136 SCB1\_INTR\_CAUSE

Active clocked interrupt signal register

Address: 0x40250E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

## 20.1.137 SCB1\_INTR\_I2C\_EC

Externally clocked I2C interrupt request register

Address: 0x40250E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	<p>STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from.</p> <p>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0</p>
2	EZ_WRITE_STOP	<p>STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event.</p> <p>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0</p>
1	EZ_STOP	<p>STOP detection. Activated on the end of a every transfer (I2C STOP).</p> <p>Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0</p>

**20.1.137 SCB1\_INTR\_I2C\_EC** (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match).  Only used when EC_AM is '1'. Default Value: 0
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## 20.1.138 SCB1\_INTR\_I2C\_EC\_MASK

Externally clocked I2C interrupt mask register

Address: 0x40250E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0



## 20.1.139 SCB1\_INTR\_I2C\_EC\_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40250E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.140 SCB1\_INTR\_SPI\_EC

Externally clocked SPI interrupt request register

Address: 0x40250EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	<p>STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from.</p> <p>Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0</p>
2	EZ_WRITE_STOP	<p>STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event.</p> <p>Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0</p>
1	EZ_STOP	<p>STOP detection. Activated on the end of a every transfer (SPI deselection).</p> <p>Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0</p>

**20.1.140 SCB1\_INTR\_SPI\_EC** (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'.  Only used when EC_AM is '1'. Default Value: 0
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## 20.1.141 SCB1\_INTR\_SPI\_EC\_MASK

Externally clocked SPI interrupt mask register

Address: 0x40250EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.142 SCB1\_INTR\_SPI\_EC\_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40250ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.143 SCB1\_INTR\_M

Master interrupt request register.

Address: 0x40250F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

**20.1.143 SCB1\_INTR\_M** (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0
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## 20.1.144 SCB1\_INTR\_M\_SET

Master interrupt set request register

Address: 0x40250F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0



## 20.1.145 SCB1\_INTR\_M\_MASK

Master interrupt mask register.

Address: 0x40250F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

## 20.1.146 SCB1\_INTR\_M\_MASKED

Master interrupt masked request register

Address: 0x40250F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.147 SCB1\_INTR\_S

Slave interrupt request register.

Address: 0x40250F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

## 20.1.147 SCB1\_INTR\_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected.  In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.  The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address.  In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd.  In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

## 20.1.148 SCB1\_INTR\_S\_SET

Slave interrupt set request register.

Address: 0x40250F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

### 20.1.148 SCB1\_INTR\_S\_SET (continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.149 SCB1\_INTR\_S\_MASK

Slave interrupt mask register.

Address: 0x40250F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

### 20.1.149 SCB1\_INTR\_S\_MASK (continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0



## 20.1.150 SCB1\_INTR\_S\_MASKED

Slave interrupt masked request register

Address: 0x40250F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

**20.1.150 SCB1\_INTR\_S\_MASKED** (continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.151 SCB1\_INTR\_TX

Transmitter interrupt request register.

Address: 0x40250F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

  

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

## 20.1.151 SCB1\_INTR\_TX (continued)

6	UNDERFLOW	<p>Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'.</p> <p>Only used in FIFO mode. Default Value: 0</p>
5	OVERFLOW	<p>Attempt to write to a full TX FIFO.</p> <p>Only used in FIFO mode. Default Value: 0</p>
4	EMPTY	<p>TX FIFO is empty; i.e. it has 0 entries.</p> <p>Only used in FIFO mode. Default Value: 0</p>
1	NOT_FULL	<p>TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR.</p> <p>Only used in FIFO mode. Default Value: 0</p>
0	TRIGGER	<p>Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.</p> <p>Only used in FIFO mode. Default Value: 0</p>

## 20.1.152 SCB1\_INTR\_TX\_SET

Transmitter interrupt set request register

Address: 0x40250F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

**20.1.152 SCB1\_INTR\_TX\_SET** (continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.153 SCB1\_INTR\_TX\_MASK

Transmitter interrupt mask register.

Address: 0x40250F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

**20.1.153 SCB1\_INTR\_TX\_MASK** (continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0



## 20.1.154 SCB1\_INTR\_TX\_MASKED

Transmitter interrupt masked request register

Address: 0x40250F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

**20.1.154 SCB1\_INTR\_TX\_MASKED** (continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

## 20.1.155 SCB1\_INTR\_RX

Receiver interrupt request register.

Address: 0x40250FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

## 20.1.155 SCB1\_INTR\_RX (continued)

9	PARITY_ERROR	<p>Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO.</p> <p>Default Value: 0</p>
8	FRAME_ERROR	<p>Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error:</p> <p>Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received.</p> <p>Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received.</p> <p>A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames.</p> <p>Default Value: 0</p>
7	BLOCKED	<p>AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'.</p> <p>Default Value: 0</p>
6	UNDERFLOW	<p>Attempt to read from an empty RX FIFO.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
5	OVERFLOW	<p>Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
3	FULL	<p>RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET:</p> <p>BYTE_MODE is '0': # entries == FF_DATA_NR/2.</p> <p>BYTE_MODE is '1': # entries == FF_DATA_NR.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
2	NOT_EMPTY	<p>RX FIFO is not empty.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>
0	TRIGGER	<p>More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL.</p> <p>Only used in FIFO mode.</p> <p>Default Value: 0</p>

## 20.1.156 SCB1\_INTR\_RX\_SET

Receiver interrupt set request register.

Address: 0x40250FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

**20.1.156 SCB1\_INTR\_RX\_SET** (continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

## 20.1.157 SCB1\_INTR\_RX\_MASK

Receiver interrupt mask register.

Address: 0x40250FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

**20.1.157 SCB1\_INTR\_RX\_MASK** (continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0



## 20.1.158 SCB1\_INTR\_RX\_MASKED

Receiver interrupt masked request register

Address: 0x40250FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

**20.1.158 SCB1\_INTR\_RX\_MASKED** (continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

# 21 Supervisory Flash (128 KB) Registers



This section discusses the Supervisory Flash (SFLASH) registers for 128 KB devices. It lists all the registers in mapping tables, in address order.

## 21.1 Register Details

Register Name	Address
<a href="#">SFLASH_PROT_ROW0</a>	0x0FFFF000
<a href="#">SFLASH_PROT_ROW1</a>	0x0FFFF001
<a href="#">SFLASH_PROT_ROW2</a>	0x0FFFF002
<a href="#">SFLASH_PROT_ROW3</a>	0x0FFFF003
<a href="#">SFLASH_PROT_ROW4</a>	0x0FFFF004
<a href="#">SFLASH_PROT_ROW5</a>	0x0FFFF005
<a href="#">SFLASH_PROT_ROW6</a>	0x0FFFF006
<a href="#">SFLASH_PROT_ROW7</a>	0x0FFFF007
<a href="#">SFLASH_PROT_ROW8</a>	0x0FFFF008
<a href="#">SFLASH_PROT_ROW9</a>	0x0FFFF009
<a href="#">SFLASH_PROT_ROW10</a>	0x0FFFF00A
<a href="#">SFLASH_PROT_ROW11</a>	0x0FFFF00B
<a href="#">SFLASH_PROT_ROW12</a>	0x0FFFF00C
<a href="#">SFLASH_PROT_ROW13</a>	0x0FFFF00D
<a href="#">SFLASH_PROT_ROW14</a>	0x0FFFF00E
<a href="#">SFLASH_PROT_ROW15</a>	0x0FFFF00F
<a href="#">SFLASH_PROT_ROW16</a>	0x0FFFF010
<a href="#">SFLASH_PROT_ROW17</a>	0x0FFFF011
<a href="#">SFLASH_PROT_ROW18</a>	0x0FFFF012
<a href="#">SFLASH_PROT_ROW19</a>	0x0FFFF013
<a href="#">SFLASH_PROT_ROW20</a>	0x0FFFF014
<a href="#">SFLASH_PROT_ROW21</a>	0x0FFFF015
<a href="#">SFLASH_PROT_ROW22</a>	0x0FFFF016
<a href="#">SFLASH_PROT_ROW23</a>	0x0FFFF017
<a href="#">SFLASH_PROT_ROW24</a>	0x0FFFF018
<a href="#">SFLASH_PROT_ROW25</a>	0x0FFFF019
<a href="#">SFLASH_PROT_ROW26</a>	0x0FFFF01A

Register Name	Address
SFLASH_PROT_ROW27	0x0FFF01B
SFLASH_PROT_ROW28	0x0FFF01C
SFLASH_PROT_ROW29	0x0FFF01D
SFLASH_PROT_ROW30	0x0FFF01E
SFLASH_PROT_ROW31	0x0FFF01F
SFLASH_PROT_ROW32	0x0FFF020
SFLASH_PROT_ROW33	0x0FFF021
SFLASH_PROT_ROW34	0x0FFF022
SFLASH_PROT_ROW35	0x0FFF023
SFLASH_PROT_ROW36	0x0FFF024
SFLASH_PROT_ROW37	0x0FFF025
SFLASH_PROT_ROW38	0x0FFF026
SFLASH_PROT_ROW39	0x0FFF027
SFLASH_PROT_ROW40	0x0FFF028
SFLASH_PROT_ROW41	0x0FFF029
SFLASH_PROT_ROW42	0x0FFF02A
SFLASH_PROT_ROW43	0x0FFF02B
SFLASH_PROT_ROW44	0x0FFF02C
SFLASH_PROT_ROW45	0x0FFF02D
SFLASH_PROT_ROW46	0x0FFF02E
SFLASH_PROT_ROW47	0x0FFF02F
SFLASH_PROT_ROW48	0x0FFF030
SFLASH_PROT_ROW49	0x0FFF031
SFLASH_PROT_ROW50	0x0FFF032
SFLASH_PROT_ROW51	0x0FFF033
SFLASH_PROT_ROW52	0x0FFF034
SFLASH_PROT_ROW53	0x0FFF035
SFLASH_PROT_ROW54	0x0FFF036
SFLASH_PROT_ROW55	0x0FFF037
SFLASH_PROT_ROW56	0x0FFF038
SFLASH_PROT_ROW57	0x0FFF039
SFLASH_PROT_ROW58	0x0FFF03A
SFLASH_PROT_ROW59	0x0FFF03B
SFLASH_PROT_ROW60	0x0FFF03C
SFLASH_PROT_ROW61	0x0FFF03D
SFLASH_PROT_ROW62	0x0FFF03E
SFLASH_PROT_ROW63	0x0FFF03F
SFLASH_PROT_PROTECTION	0x0FFF07F
SFLASH_AV_PAIRS_8B0	0x0FFF080
SFLASH_AV_PAIRS_8B1	0x0FFF081
SFLASH_AV_PAIRS_8B2	0x0FFF082
SFLASH_AV_PAIRS_8B3	0x0FFF083

Register Name	Address
SFLASH_AV_PAIRS_8B4	0x0FFF084
SFLASH_AV_PAIRS_8B5	0x0FFF085
SFLASH_AV_PAIRS_8B6	0x0FFF086
SFLASH_AV_PAIRS_8B7	0x0FFF087
SFLASH_AV_PAIRS_8B8	0x0FFF088
SFLASH_AV_PAIRS_8B9	0x0FFF089
SFLASH_AV_PAIRS_8B10	0x0FFF08A
SFLASH_AV_PAIRS_8B11	0x0FFF08B
SFLASH_AV_PAIRS_8B12	0x0FFF08C
SFLASH_AV_PAIRS_8B13	0x0FFF08D
SFLASH_AV_PAIRS_8B14	0x0FFF08E
SFLASH_AV_PAIRS_8B15	0x0FFF08F
SFLASH_AV_PAIRS_8B16	0x0FFF090
SFLASH_AV_PAIRS_8B17	0x0FFF091
SFLASH_AV_PAIRS_8B18	0x0FFF092
SFLASH_AV_PAIRS_8B19	0x0FFF093
SFLASH_AV_PAIRS_8B20	0x0FFF094
SFLASH_AV_PAIRS_8B21	0x0FFF095
SFLASH_AV_PAIRS_8B22	0x0FFF096
SFLASH_AV_PAIRS_8B23	0x0FFF097
SFLASH_AV_PAIRS_8B24	0x0FFF098
SFLASH_AV_PAIRS_8B25	0x0FFF099
SFLASH_AV_PAIRS_8B26	0x0FFF09A
SFLASH_AV_PAIRS_8B27	0x0FFF09B
SFLASH_AV_PAIRS_8B28	0x0FFF09C
SFLASH_AV_PAIRS_8B29	0x0FFF09D
SFLASH_AV_PAIRS_8B30	0x0FFF09E
SFLASH_AV_PAIRS_8B31	0x0FFF09F
SFLASH_AV_PAIRS_8B32	0x0FFF0A0
SFLASH_AV_PAIRS_8B33	0x0FFF0A1
SFLASH_AV_PAIRS_8B34	0x0FFF0A2
SFLASH_AV_PAIRS_8B35	0x0FFF0A3
SFLASH_AV_PAIRS_8B36	0x0FFF0A4
SFLASH_AV_PAIRS_8B37	0x0FFF0A5
SFLASH_AV_PAIRS_8B38	0x0FFF0A6
SFLASH_AV_PAIRS_8B39	0x0FFF0A7
SFLASH_AV_PAIRS_8B40	0x0FFF0A8
SFLASH_AV_PAIRS_8B41	0x0FFF0A9
SFLASH_AV_PAIRS_8B42	0x0FFF0AA
SFLASH_AV_PAIRS_8B43	0x0FFF0AB
SFLASH_AV_PAIRS_8B44	0x0FFF0AC
SFLASH_AV_PAIRS_8B45	0x0FFF0AD

Register Name	Address
SFLASH_AV_PAIRS_8B46	0x0FFF0AE
SFLASH_AV_PAIRS_8B47	0x0FFF0AF
SFLASH_AV_PAIRS_8B48	0x0FFF0B0
SFLASH_AV_PAIRS_8B49	0x0FFF0B1
SFLASH_AV_PAIRS_8B50	0x0FFF0B2
SFLASH_AV_PAIRS_8B51	0x0FFF0B3
SFLASH_AV_PAIRS_8B52	0x0FFF0B4
SFLASH_AV_PAIRS_8B53	0x0FFF0B5
SFLASH_AV_PAIRS_8B54	0x0FFF0B6
SFLASH_AV_PAIRS_8B55	0x0FFF0B7
SFLASH_AV_PAIRS_8B56	0x0FFF0B8
SFLASH_AV_PAIRS_8B57	0x0FFF0B9
SFLASH_AV_PAIRS_8B58	0x0FFF0BA
SFLASH_AV_PAIRS_8B59	0x0FFF0BB
SFLASH_AV_PAIRS_8B60	0x0FFF0BC
SFLASH_AV_PAIRS_8B61	0x0FFF0BD
SFLASH_AV_PAIRS_8B62	0x0FFF0BE
SFLASH_AV_PAIRS_8B63	0x0FFF0BF
SFLASH_AV_PAIRS_8B64	0x0FFF0C0
SFLASH_AV_PAIRS_8B65	0x0FFF0C1
SFLASH_AV_PAIRS_8B66	0x0FFF0C2
SFLASH_AV_PAIRS_8B67	0x0FFF0C3
SFLASH_AV_PAIRS_8B68	0x0FFF0C4
SFLASH_AV_PAIRS_8B69	0x0FFF0C5
SFLASH_AV_PAIRS_8B70	0x0FFF0C6
SFLASH_AV_PAIRS_8B71	0x0FFF0C7
SFLASH_AV_PAIRS_8B72	0x0FFF0C8
SFLASH_AV_PAIRS_8B73	0x0FFF0C9
SFLASH_AV_PAIRS_8B74	0x0FFF0CA
SFLASH_AV_PAIRS_8B75	0x0FFF0CB
SFLASH_AV_PAIRS_8B76	0x0FFF0CC
SFLASH_AV_PAIRS_8B77	0x0FFF0CD
SFLASH_AV_PAIRS_8B78	0x0FFF0CE
SFLASH_AV_PAIRS_8B79	0x0FFF0CF
SFLASH_AV_PAIRS_8B80	0x0FFF0D0
SFLASH_AV_PAIRS_8B81	0x0FFF0D1
SFLASH_AV_PAIRS_8B82	0x0FFF0D2
SFLASH_AV_PAIRS_8B83	0x0FFF0D3
SFLASH_AV_PAIRS_8B84	0x0FFF0D4
SFLASH_AV_PAIRS_8B85	0x0FFF0D5
SFLASH_AV_PAIRS_8B86	0x0FFF0D6
SFLASH_AV_PAIRS_8B87	0x0FFF0D7

Register Name	Address
SFLASH_AV_PAIRS_8B88	0x0FFF0D8
SFLASH_BLESS_BB_BUMP2	0x0FFF0D8
SFLASH_AV_PAIRS_8B89	0x0FFF0D9
SFLASH_AV_PAIRS_8B90	0x0FFF0DA
SFLASH_BLESS_BB_XO	0x0FFF0DA
SFLASH_AV_PAIRS_8B91	0x0FFF0DB
SFLASH_AV_PAIRS_8B92	0x0FFF0DC
SFLASH_BLESS_SY_BUMP1	0x0FFF0DC
SFLASH_AV_PAIRS_8B93	0x0FFF0DD
SFLASH_AV_PAIRS_8B94	0x0FFF0DE
SFLASH_BLESS_LDO	0x0FFF0DE
SFLASH_AV_PAIRS_8B95	0x0FFF0DF
SFLASH_AV_PAIRS_8B96	0x0FFF0E0
SFLASH_AV_PAIRS_8B97	0x0FFF0E1
SFLASH_AV_PAIRS_8B98	0x0FFF0E2
SFLASH_AV_PAIRS_8B99	0x0FFF0E3
SFLASH_AV_PAIRS_8B100	0x0FFF0E4
SFLASH_AV_PAIRS_8B101	0x0FFF0E5
SFLASH_AV_PAIRS_8B102	0x0FFF0E6
SFLASH_AV_PAIRS_8B103	0x0FFF0E7
SFLASH_AV_PAIRS_8B104	0x0FFF0E8
SFLASH_AV_PAIRS_8B105	0x0FFF0E9
SFLASH_AV_PAIRS_8B106	0x0FFF0EA
SFLASH_AV_PAIRS_8B107	0x0FFF0EB
SFLASH_AV_PAIRS_8B108	0x0FFF0EC
SFLASH_AV_PAIRS_8B109	0x0FFF0ED
SFLASH_AV_PAIRS_8B110	0x0FFF0EE
SFLASH_AV_PAIRS_8B111	0x0FFF0EF
SFLASH_AV_PAIRS_8B112	0x0FFF0F0
SFLASH_AV_PAIRS_8B113	0x0FFF0F1
SFLASH_AV_PAIRS_8B114	0x0FFF0F2
SFLASH_AV_PAIRS_8B115	0x0FFF0F3
SFLASH_AV_PAIRS_8B116	0x0FFF0F4
SFLASH_AV_PAIRS_8B117	0x0FFF0F5
SFLASH_AV_PAIRS_8B118	0x0FFF0F6
SFLASH_AV_PAIRS_8B119	0x0FFF0F7
SFLASH_AV_PAIRS_8B120	0x0FFF0F8
SFLASH_AV_PAIRS_8B121	0x0FFF0F9
SFLASH_AV_PAIRS_8B122	0x0FFF0FA
SFLASH_AV_PAIRS_8B123	0x0FFF0FB
SFLASH_AV_PAIRS_8B124	0x0FFF0FC
SFLASH_AV_PAIRS_8B125	0x0FFF0FD

Register Name	Address
SFLASH_AV_PAIRS_8B126	0x0FFF0FE
SFLASH_AV_PAIRS_8B127	0x0FFF0FF
SFLASH_AV_PAIRS_32B0	0x0FFF100
SFLASH_AV_PAIRS_32B1	0x0FFF104
SFLASH_AV_PAIRS_32B2	0x0FFF108
SFLASH_AV_PAIRS_32B3	0x0FFF10C
SFLASH_AV_PAIRS_32B4	0x0FFF110
SFLASH_AV_PAIRS_32B5	0x0FFF114
SFLASH_AV_PAIRS_32B6	0x0FFF118
SFLASH_AV_PAIRS_32B7	0x0FFF11C
SFLASH_AV_PAIRS_32B8	0x0FFF120
SFLASH_AV_PAIRS_32B9	0x0FFF124
SFLASH_AV_PAIRS_32B10	0x0FFF128
SFLASH_AV_PAIRS_32B11	0x0FFF12C
SFLASH_AV_PAIRS_32B12	0x0FFF130
SFLASH_AV_PAIRS_32B13	0x0FFF134
SFLASH_AV_PAIRS_32B14	0x0FFF138
SFLASH_AV_PAIRS_32B15	0x0FFF13C
SFLASH_CPUSS_WOUNDING	0x0FFF140
SFLASH_SILICON_ID	0x0FFF144
SFLASH_CPUSS_PRIV_RAM	0x0FFF148
SFLASH_CPUSS_PRIV_ROM_BROM	0x0FFF14A
SFLASH_CPUSS_PRIV_FLASH	0x0FFF14C
SFLASH_CPUSS_PRIV_ROM_SROM	0x0FFF14E
SFLASH_HIB_KEY_DELAY	0x0FFF150
SFLASH_DPSLP_KEY_DELAY	0x0FFF152
SFLASH_SWD_CONFIG	0x0FFF154
SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0	0x0FFF155
SFLASH_SWD_LISTEN	0x0FFF158
SFLASH_FLASH_START	0x0FFF15C
SFLASH_CSD_TRIM1_HVIDAC	0x0FFF160
SFLASH_CSD_TRIM2_HVIDAC	0x0FFF161
SFLASH_CSD_TRIM1_CSD	0x0FFF162
SFLASH_CSD_TRIM2_CSD	0x0FFF163
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFF164
SFLASH_SAR_TEMP_OFFSET	0x0FFF166
SFLASH_SKIP_CHECKSUM	0x0FFF169
SFLASH_PROT_VIRGINKEY0	0x0FFF170
SFLASH_PROT_VIRGINKEY1	0x0FFF171
SFLASH_PROT_VIRGINKEY2	0x0FFF172
SFLASH_PROT_VIRGINKEY3	0x0FFF173
SFLASH_PROT_VIRGINKEY4	0x0FFF174



Register Name	Address
SFLASH_PROT_VIRGINKEY5	0x0FFF175
SFLASH_PROT_VIRGINKEY6	0x0FFF176
SFLASH_PROT_VIRGINKEY7	0x0FFF177
SFLASH_DIE_LOT0	0x0FFF178
SFLASH_DIE_LOT1	0x0FFF179
SFLASH_DIE_LOT2	0x0FFF17A
SFLASH_DIE_WAFER	0x0FFF17B
SFLASH_DIE_X	0x0FFF17C
SFLASH_DIE_Y	0x0FFF17D
SFLASH_DIE_SORT	0x0FFF17E
SFLASH_DIE_MINOR	0x0FFF17F
SFLASH_PE_TE_DATA0	0x0FFF180
SFLASH_PE_TE_DATA1	0x0FFF181
SFLASH_PE_TE_DATA2	0x0FFF182
SFLASH_PE_TE_DATA3	0x0FFF183
SFLASH_PE_TE_DATA4	0x0FFF184
SFLASH_PE_TE_DATA5	0x0FFF185
SFLASH_PE_TE_DATA6	0x0FFF186
SFLASH_PE_TE_DATA7	0x0FFF187
SFLASH_PE_TE_DATA8	0x0FFF188
SFLASH_PE_TE_DATA9	0x0FFF189
SFLASH_PE_TE_DATA10	0x0FFF18A
SFLASH_PE_TE_DATA11	0x0FFF18B
SFLASH_PE_TE_DATA12	0x0FFF18C
SFLASH_PE_TE_DATA13	0x0FFF18D
SFLASH_PE_TE_DATA14	0x0FFF18E
SFLASH_PE_TE_DATA15	0x0FFF18F
SFLASH_PE_TE_DATA16	0x0FFF190
SFLASH_PE_TE_DATA17	0x0FFF191
SFLASH_PE_TE_DATA18	0x0FFF192
SFLASH_PE_TE_DATA19	0x0FFF193
SFLASH_PE_TE_DATA20	0x0FFF194
SFLASH_PE_TE_DATA21	0x0FFF195
SFLASH_PE_TE_DATA22	0x0FFF196
SFLASH_PE_TE_DATA23	0x0FFF197
SFLASH_PE_TE_DATA24	0x0FFF198
SFLASH_PE_TE_DATA25	0x0FFF199
SFLASH_PE_TE_DATA26	0x0FFF19A
SFLASH_PE_TE_DATA27	0x0FFF19B
SFLASH_PE_TE_DATA28	0x0FFF19C
SFLASH_PE_TE_DATA29	0x0FFF19D
SFLASH_PE_TE_DATA30	0x0FFF19E

Register Name	Address
SFLASH_PE_TE_DATA31	0x0FFF19F
SFLASH_PP	0x0FFF1A0
SFLASH_E	0x0FFF1A4
SFLASH_P	0x0FFF1A8
SFLASH_EA_E	0x0FFF1AC
SFLASH_EA_P	0x0FFF1B0
SFLASH_ES_E	0x0FFF1B4
SFLASH_ES_P_EO	0x0FFF1B8
SFLASH_E_VCTAT	0x0FFF1BC
SFLASH_P_VCTAT	0x0FFF1BD
SFLASH_IMO_MAXF0	0x0FFF1C0
SFLASH_IMO_ABS0	0x0FFF1C1
SFLASH_IMO_TMPCO0	0x0FFF1C2
SFLASH_IMO_MAXF1	0x0FFF1C3
SFLASH_IMO_ABS1	0x0FFF1C4
SFLASH_IMO_TMPCO1	0x0FFF1C5
SFLASH_IMO_MAXF2	0x0FFF1C6
SFLASH_IMO_ABS2	0x0FFF1C7
SFLASH_IMO_TMPCO2	0x0FFF1C8
SFLASH_IMO_MAXF3	0x0FFF1C9
SFLASH_IMO_ABS3	0x0FFF1CA
SFLASH_IMO_TMPCO3	0x0FFF1CB
SFLASH_IMO_ABS4	0x0FFF1CC
SFLASH_IMO_TMPCO4	0x0FFF1CD
SFLASH_IMO_TRIM0	0x0FFF1D0
SFLASH_IMO_TRIM1	0x0FFF1D1
SFLASH_IMO_TRIM2	0x0FFF1D2
SFLASH_IMO_TRIM3	0x0FFF1D3
SFLASH_IMO_TRIM4	0x0FFF1D4
SFLASH_IMO_TRIM5	0x0FFF1D5
SFLASH_IMO_TRIM6	0x0FFF1D6
SFLASH_IMO_TRIM7	0x0FFF1D7
SFLASH_IMO_TRIM8	0x0FFF1D8
SFLASH_IMO_TRIM9	0x0FFF1D9
SFLASH_IMO_TRIM10	0x0FFF1DA
SFLASH_IMO_TRIM11	0x0FFF1DB
SFLASH_IMO_TRIM12	0x0FFF1DC
SFLASH_IMO_TRIM13	0x0FFF1DD
SFLASH_IMO_TRIM14	0x0FFF1DE
SFLASH_IMO_TRIM15	0x0FFF1DF
SFLASH_IMO_TRIM16	0x0FFF1E0
SFLASH_IMO_TRIM17	0x0FFF1E1

Register Name	Address
SFLASH_IMO_TRIM18	0x0FFF1E2
SFLASH_IMO_TRIM19	0x0FFF1E3
SFLASH_IMO_TRIM20	0x0FFF1E4
SFLASH_IMO_TRIM21	0x0FFF1E5
SFLASH_IMO_TRIM22	0x0FFF1E6
SFLASH_IMO_TRIM23	0x0FFF1E7
SFLASH_IMO_TRIM24	0x0FFF1E8
SFLASH_IMO_TRIM25	0x0FFF1E9
SFLASH_IMO_TRIM26	0x0FFF1EA
SFLASH_IMO_TRIM27	0x0FFF1EB
SFLASH_IMO_TRIM28	0x0FFF1EC
SFLASH_IMO_TRIM29	0x0FFF1ED
SFLASH_IMO_TRIM30	0x0FFF1EE
SFLASH_IMO_TRIM31	0x0FFF1EF
SFLASH_IMO_TRIM32	0x0FFF1F0
SFLASH_IMO_TRIM33	0x0FFF1F1
SFLASH_IMO_TRIM34	0x0FFF1F2
SFLASH_IMO_TRIM35	0x0FFF1F3
SFLASH_IMO_TRIM36	0x0FFF1F4
SFLASH_IMO_TRIM37	0x0FFF1F5
SFLASH_IMO_TRIM38	0x0FFF1F6
SFLASH_IMO_TRIM39	0x0FFF1F7
SFLASH_IMO_TRIM40	0x0FFF1F8
SFLASH_IMO_TRIM41	0x0FFF1F9
SFLASH_IMO_TRIM42	0x0FFF1FA
SFLASH_IMO_TRIM43	0x0FFF1FB
SFLASH_IMO_TRIM44	0x0FFF1FC
SFLASH_IMO_TRIM45	0x0FFF1FD
SFLASH_CHECKSUM	0x0FFF1FE
SFLASH_MACRO_0_FREE_SFLASH0	0x0FFF200
SFLASH_MACRO_0_FREE_SFLASH1	0x0FFF201
SFLASH_MACRO_0_FREE_SFLASH2	0x0FFF202
SFLASH_MACRO_0_FREE_SFLASH3	0x0FFF203
SFLASH_MACRO_0_FREE_SFLASH4	0x0FFF204
SFLASH_MACRO_0_FREE_SFLASH5	0x0FFF205
SFLASH_MACRO_0_FREE_SFLASH6	0x0FFF206
SFLASH_MACRO_0_FREE_SFLASH7	0x0FFF207
SFLASH_MACRO_0_FREE_SFLASH8	0x0FFF208
SFLASH_MACRO_0_FREE_SFLASH9	0x0FFF209
SFLASH_MACRO_0_FREE_SFLASH10	0x0FFF20A
SFLASH_MACRO_0_FREE_SFLASH11	0x0FFF20B
SFLASH_MACRO_0_FREE_SFLASH12	0x0FFF20C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH13	0x0FFF20D
SFLASH_MACRO_0_FREE_SFLASH14	0x0FFF20E
SFLASH_MACRO_0_FREE_SFLASH15	0x0FFF20F
SFLASH_MACRO_0_FREE_SFLASH16	0x0FFF210
SFLASH_MACRO_0_FREE_SFLASH17	0x0FFF211
SFLASH_MACRO_0_FREE_SFLASH18	0x0FFF212
SFLASH_MACRO_0_FREE_SFLASH19	0x0FFF213
SFLASH_MACRO_0_FREE_SFLASH20	0x0FFF214
SFLASH_MACRO_0_FREE_SFLASH21	0x0FFF215
SFLASH_MACRO_0_FREE_SFLASH22	0x0FFF216
SFLASH_MACRO_0_FREE_SFLASH23	0x0FFF217
SFLASH_MACRO_0_FREE_SFLASH24	0x0FFF218
SFLASH_MACRO_0_FREE_SFLASH25	0x0FFF219
SFLASH_MACRO_0_FREE_SFLASH26	0x0FFF21A
SFLASH_MACRO_0_FREE_SFLASH27	0x0FFF21B
SFLASH_MACRO_0_FREE_SFLASH28	0x0FFF21C
SFLASH_MACRO_0_FREE_SFLASH29	0x0FFF21D
SFLASH_MACRO_0_FREE_SFLASH30	0x0FFF21E
SFLASH_MACRO_0_FREE_SFLASH31	0x0FFF21F
SFLASH_MACRO_0_FREE_SFLASH32	0x0FFF220
SFLASH_MACRO_0_FREE_SFLASH33	0x0FFF221
SFLASH_MACRO_0_FREE_SFLASH34	0x0FFF222
SFLASH_MACRO_0_FREE_SFLASH35	0x0FFF223
SFLASH_MACRO_0_FREE_SFLASH36	0x0FFF224
SFLASH_MACRO_0_FREE_SFLASH37	0x0FFF225
SFLASH_MACRO_0_FREE_SFLASH38	0x0FFF226
SFLASH_MACRO_0_FREE_SFLASH39	0x0FFF227
SFLASH_MACRO_0_FREE_SFLASH40	0x0FFF228
SFLASH_MACRO_0_FREE_SFLASH41	0x0FFF229
SFLASH_MACRO_0_FREE_SFLASH42	0x0FFF22A
SFLASH_MACRO_0_FREE_SFLASH43	0x0FFF22B
SFLASH_MACRO_0_FREE_SFLASH44	0x0FFF22C
SFLASH_MACRO_0_FREE_SFLASH45	0x0FFF22D
SFLASH_MACRO_0_FREE_SFLASH46	0x0FFF22E
SFLASH_MACRO_0_FREE_SFLASH47	0x0FFF22F
SFLASH_MACRO_0_FREE_SFLASH48	0x0FFF230
SFLASH_MACRO_0_FREE_SFLASH49	0x0FFF231
SFLASH_MACRO_0_FREE_SFLASH50	0x0FFF232
SFLASH_MACRO_0_FREE_SFLASH51	0x0FFF233
SFLASH_MACRO_0_FREE_SFLASH52	0x0FFF234
SFLASH_MACRO_0_FREE_SFLASH53	0x0FFF235
SFLASH_MACRO_0_FREE_SFLASH54	0x0FFF236

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH55	0x0FFF237
SFLASH_MACRO_0_FREE_SFLASH56	0x0FFF238
SFLASH_MACRO_0_FREE_SFLASH57	0x0FFF239
SFLASH_MACRO_0_FREE_SFLASH58	0x0FFF23A
SFLASH_MACRO_0_FREE_SFLASH59	0x0FFF23B
SFLASH_MACRO_0_FREE_SFLASH60	0x0FFF23C
SFLASH_MACRO_0_FREE_SFLASH61	0x0FFF23D
SFLASH_MACRO_0_FREE_SFLASH62	0x0FFF23E
SFLASH_MACRO_0_FREE_SFLASH63	0x0FFF23F
SFLASH_MACRO_0_FREE_SFLASH64	0x0FFF240
SFLASH_MACRO_0_FREE_SFLASH65	0x0FFF241
SFLASH_MACRO_0_FREE_SFLASH66	0x0FFF242
SFLASH_MACRO_0_FREE_SFLASH67	0x0FFF243
SFLASH_MACRO_0_FREE_SFLASH68	0x0FFF244
SFLASH_MACRO_0_FREE_SFLASH69	0x0FFF245
SFLASH_MACRO_0_FREE_SFLASH70	0x0FFF246
SFLASH_MACRO_0_FREE_SFLASH71	0x0FFF247
SFLASH_MACRO_0_FREE_SFLASH72	0x0FFF248
SFLASH_MACRO_0_FREE_SFLASH73	0x0FFF249
SFLASH_MACRO_0_FREE_SFLASH74	0x0FFF24A
SFLASH_MACRO_0_FREE_SFLASH75	0x0FFF24B
SFLASH_MACRO_0_FREE_SFLASH76	0x0FFF24C
SFLASH_MACRO_0_FREE_SFLASH77	0x0FFF24D
SFLASH_MACRO_0_FREE_SFLASH78	0x0FFF24E
SFLASH_MACRO_0_FREE_SFLASH79	0x0FFF24F
SFLASH_MACRO_0_FREE_SFLASH80	0x0FFF250
SFLASH_MACRO_0_FREE_SFLASH81	0x0FFF251
SFLASH_MACRO_0_FREE_SFLASH82	0x0FFF252
SFLASH_MACRO_0_FREE_SFLASH83	0x0FFF253
SFLASH_MACRO_0_FREE_SFLASH84	0x0FFF254
SFLASH_MACRO_0_FREE_SFLASH85	0x0FFF255
SFLASH_MACRO_0_FREE_SFLASH86	0x0FFF256
SFLASH_MACRO_0_FREE_SFLASH87	0x0FFF257
SFLASH_MACRO_0_FREE_SFLASH88	0x0FFF258
SFLASH_MACRO_0_FREE_SFLASH89	0x0FFF259
SFLASH_MACRO_0_FREE_SFLASH90	0x0FFF25A
SFLASH_MACRO_0_FREE_SFLASH91	0x0FFF25B
SFLASH_MACRO_0_FREE_SFLASH92	0x0FFF25C
SFLASH_MACRO_0_FREE_SFLASH93	0x0FFF25D
SFLASH_MACRO_0_FREE_SFLASH94	0x0FFF25E
SFLASH_MACRO_0_FREE_SFLASH95	0x0FFF25F
SFLASH_MACRO_0_FREE_SFLASH96	0x0FFF260

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH97	0x0FFF261
SFLASH_MACRO_0_FREE_SFLASH98	0x0FFF262
SFLASH_MACRO_0_FREE_SFLASH99	0x0FFF263
SFLASH_MACRO_0_FREE_SFLASH100	0x0FFF264
SFLASH_MACRO_0_FREE_SFLASH101	0x0FFF265
SFLASH_MACRO_0_FREE_SFLASH102	0x0FFF266
SFLASH_MACRO_0_FREE_SFLASH103	0x0FFF267
SFLASH_MACRO_0_FREE_SFLASH104	0x0FFF268
SFLASH_MACRO_0_FREE_SFLASH105	0x0FFF269
SFLASH_MACRO_0_FREE_SFLASH106	0x0FFF26A
SFLASH_MACRO_0_FREE_SFLASH107	0x0FFF26B
SFLASH_MACRO_0_FREE_SFLASH108	0x0FFF26C
SFLASH_MACRO_0_FREE_SFLASH109	0x0FFF26D
SFLASH_MACRO_0_FREE_SFLASH110	0x0FFF26E
SFLASH_MACRO_0_FREE_SFLASH111	0x0FFF26F
SFLASH_MACRO_0_FREE_SFLASH112	0x0FFF270
SFLASH_MACRO_0_FREE_SFLASH113	0x0FFF271
SFLASH_MACRO_0_FREE_SFLASH114	0x0FFF272
SFLASH_MACRO_0_FREE_SFLASH115	0x0FFF273
SFLASH_MACRO_0_FREE_SFLASH116	0x0FFF274
SFLASH_MACRO_0_FREE_SFLASH117	0x0FFF275
SFLASH_MACRO_0_FREE_SFLASH118	0x0FFF276
SFLASH_MACRO_0_FREE_SFLASH119	0x0FFF277
SFLASH_MACRO_0_FREE_SFLASH120	0x0FFF278
SFLASH_MACRO_0_FREE_SFLASH121	0x0FFF279
SFLASH_MACRO_0_FREE_SFLASH122	0x0FFF27A
SFLASH_MACRO_0_FREE_SFLASH123	0x0FFF27B
SFLASH_MACRO_0_FREE_SFLASH124	0x0FFF27C
SFLASH_MACRO_0_FREE_SFLASH125	0x0FFF27D
SFLASH_MACRO_0_FREE_SFLASH126	0x0FFF27E
SFLASH_MACRO_0_FREE_SFLASH127	0x0FFF27F
SFLASH_MACRO_0_FREE_SFLASH128	0x0FFF280
SFLASH_MACRO_0_FREE_SFLASH129	0x0FFF281
SFLASH_MACRO_0_FREE_SFLASH130	0x0FFF282
SFLASH_MACRO_0_FREE_SFLASH131	0x0FFF283
SFLASH_MACRO_0_FREE_SFLASH132	0x0FFF284
SFLASH_MACRO_0_FREE_SFLASH133	0x0FFF285
SFLASH_MACRO_0_FREE_SFLASH134	0x0FFF286
SFLASH_MACRO_0_FREE_SFLASH135	0x0FFF287
SFLASH_MACRO_0_FREE_SFLASH136	0x0FFF288
SFLASH_MACRO_0_FREE_SFLASH137	0x0FFF289
SFLASH_MACRO_0_FREE_SFLASH138	0x0FFF28A

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH139	0x0FFF28B
SFLASH_MACRO_0_FREE_SFLASH140	0x0FFF28C
SFLASH_MACRO_0_FREE_SFLASH141	0x0FFF28D
SFLASH_MACRO_0_FREE_SFLASH142	0x0FFF28E
SFLASH_MACRO_0_FREE_SFLASH143	0x0FFF28F
SFLASH_MACRO_0_FREE_SFLASH144	0x0FFF290
SFLASH_MACRO_0_FREE_SFLASH145	0x0FFF291
SFLASH_MACRO_0_FREE_SFLASH146	0x0FFF292
SFLASH_MACRO_0_FREE_SFLASH147	0x0FFF293
SFLASH_MACRO_0_FREE_SFLASH148	0x0FFF294
SFLASH_MACRO_0_FREE_SFLASH149	0x0FFF295
SFLASH_MACRO_0_FREE_SFLASH150	0x0FFF296
SFLASH_MACRO_0_FREE_SFLASH151	0x0FFF297
SFLASH_MACRO_0_FREE_SFLASH152	0x0FFF298
SFLASH_MACRO_0_FREE_SFLASH153	0x0FFF299
SFLASH_MACRO_0_FREE_SFLASH154	0x0FFF29A
SFLASH_MACRO_0_FREE_SFLASH155	0x0FFF29B
SFLASH_MACRO_0_FREE_SFLASH156	0x0FFF29C
SFLASH_MACRO_0_FREE_SFLASH157	0x0FFF29D
SFLASH_MACRO_0_FREE_SFLASH158	0x0FFF29E
SFLASH_MACRO_0_FREE_SFLASH159	0x0FFF29F
SFLASH_MACRO_0_FREE_SFLASH160	0x0FFF2A0
SFLASH_MACRO_0_FREE_SFLASH161	0x0FFF2A1
SFLASH_MACRO_0_FREE_SFLASH162	0x0FFF2A2
SFLASH_MACRO_0_FREE_SFLASH163	0x0FFF2A3
SFLASH_MACRO_0_FREE_SFLASH164	0x0FFF2A4
SFLASH_MACRO_0_FREE_SFLASH165	0x0FFF2A5
SFLASH_MACRO_0_FREE_SFLASH166	0x0FFF2A6
SFLASH_MACRO_0_FREE_SFLASH167	0x0FFF2A7
SFLASH_MACRO_0_FREE_SFLASH168	0x0FFF2A8
SFLASH_MACRO_0_FREE_SFLASH169	0x0FFF2A9
SFLASH_MACRO_0_FREE_SFLASH170	0x0FFF2AA
SFLASH_MACRO_0_FREE_SFLASH171	0x0FFF2AB
SFLASH_MACRO_0_FREE_SFLASH172	0x0FFF2AC
SFLASH_MACRO_0_FREE_SFLASH173	0x0FFF2AD
SFLASH_MACRO_0_FREE_SFLASH174	0x0FFF2AE
SFLASH_MACRO_0_FREE_SFLASH175	0x0FFF2AF
SFLASH_MACRO_0_FREE_SFLASH176	0x0FFF2B0
SFLASH_MACRO_0_FREE_SFLASH177	0x0FFF2B1
SFLASH_MACRO_0_FREE_SFLASH178	0x0FFF2B2
SFLASH_MACRO_0_FREE_SFLASH179	0x0FFF2B3
SFLASH_MACRO_0_FREE_SFLASH180	0x0FFF2B4

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH181	0x0FFF2B5
SFLASH_MACRO_0_FREE_SFLASH182	0x0FFF2B6
SFLASH_MACRO_0_FREE_SFLASH183	0x0FFF2B7
SFLASH_MACRO_0_FREE_SFLASH184	0x0FFF2B8
SFLASH_MACRO_0_FREE_SFLASH185	0x0FFF2B9
SFLASH_MACRO_0_FREE_SFLASH186	0x0FFF2BA
SFLASH_MACRO_0_FREE_SFLASH187	0x0FFF2BB
SFLASH_MACRO_0_FREE_SFLASH188	0x0FFF2BC
SFLASH_MACRO_0_FREE_SFLASH189	0x0FFF2BD
SFLASH_MACRO_0_FREE_SFLASH190	0x0FFF2BE
SFLASH_MACRO_0_FREE_SFLASH191	0x0FFF2BF
SFLASH_MACRO_0_FREE_SFLASH192	0x0FFF2C0
SFLASH_MACRO_0_FREE_SFLASH193	0x0FFF2C1
SFLASH_MACRO_0_FREE_SFLASH194	0x0FFF2C2
SFLASH_MACRO_0_FREE_SFLASH195	0x0FFF2C3
SFLASH_MACRO_0_FREE_SFLASH196	0x0FFF2C4
SFLASH_MACRO_0_FREE_SFLASH197	0x0FFF2C5
SFLASH_MACRO_0_FREE_SFLASH198	0x0FFF2C6
SFLASH_MACRO_0_FREE_SFLASH199	0x0FFF2C7
SFLASH_MACRO_0_FREE_SFLASH200	0x0FFF2C8
SFLASH_MACRO_0_FREE_SFLASH201	0x0FFF2C9
SFLASH_MACRO_0_FREE_SFLASH202	0x0FFF2CA
SFLASH_MACRO_0_FREE_SFLASH203	0x0FFF2CB
SFLASH_MACRO_0_FREE_SFLASH204	0x0FFF2CC
SFLASH_MACRO_0_FREE_SFLASH205	0x0FFF2CD
SFLASH_MACRO_0_FREE_SFLASH206	0x0FFF2CE
SFLASH_MACRO_0_FREE_SFLASH207	0x0FFF2CF
SFLASH_MACRO_0_FREE_SFLASH208	0x0FFF2D0
SFLASH_MACRO_0_FREE_SFLASH209	0x0FFF2D1
SFLASH_MACRO_0_FREE_SFLASH210	0x0FFF2D2
SFLASH_MACRO_0_FREE_SFLASH211	0x0FFF2D3
SFLASH_MACRO_0_FREE_SFLASH212	0x0FFF2D4
SFLASH_MACRO_0_FREE_SFLASH213	0x0FFF2D5
SFLASH_MACRO_0_FREE_SFLASH214	0x0FFF2D6
SFLASH_MACRO_0_FREE_SFLASH215	0x0FFF2D7
SFLASH_MACRO_0_FREE_SFLASH216	0x0FFF2D8
SFLASH_MACRO_0_FREE_SFLASH217	0x0FFF2D9
SFLASH_MACRO_0_FREE_SFLASH218	0x0FFF2DA
SFLASH_MACRO_0_FREE_SFLASH219	0x0FFF2DB
SFLASH_MACRO_0_FREE_SFLASH220	0x0FFF2DC
SFLASH_MACRO_0_FREE_SFLASH221	0x0FFF2DD
SFLASH_MACRO_0_FREE_SFLASH222	0x0FFF2DE



Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH223	0x0FFF2DF
SFLASH_MACRO_0_FREE_SFLASH224	0x0FFF2E0
SFLASH_MACRO_0_FREE_SFLASH225	0x0FFF2E1
SFLASH_MACRO_0_FREE_SFLASH226	0x0FFF2E2
SFLASH_MACRO_0_FREE_SFLASH227	0x0FFF2E3
SFLASH_MACRO_0_FREE_SFLASH228	0x0FFF2E4
SFLASH_MACRO_0_FREE_SFLASH229	0x0FFF2E5
SFLASH_MACRO_0_FREE_SFLASH230	0x0FFF2E6
SFLASH_MACRO_0_FREE_SFLASH231	0x0FFF2E7
SFLASH_MACRO_0_FREE_SFLASH232	0x0FFF2E8
SFLASH_MACRO_0_FREE_SFLASH233	0x0FFF2E9
SFLASH_MACRO_0_FREE_SFLASH234	0x0FFF2EA
SFLASH_MACRO_0_FREE_SFLASH235	0x0FFF2EB
SFLASH_MACRO_0_FREE_SFLASH236	0x0FFF2EC
SFLASH_MACRO_0_FREE_SFLASH237	0x0FFF2ED
SFLASH_MACRO_0_FREE_SFLASH238	0x0FFF2EE
SFLASH_MACRO_0_FREE_SFLASH239	0x0FFF2EF
SFLASH_MACRO_0_FREE_SFLASH240	0x0FFF2F0
SFLASH_MACRO_0_FREE_SFLASH241	0x0FFF2F1
SFLASH_MACRO_0_FREE_SFLASH242	0x0FFF2F2
SFLASH_MACRO_0_FREE_SFLASH243	0x0FFF2F3
SFLASH_MACRO_0_FREE_SFLASH244	0x0FFF2F4
SFLASH_MACRO_0_FREE_SFLASH245	0x0FFF2F5
SFLASH_MACRO_0_FREE_SFLASH246	0x0FFF2F6
SFLASH_MACRO_0_FREE_SFLASH247	0x0FFF2F7
SFLASH_MACRO_0_FREE_SFLASH248	0x0FFF2F8
SFLASH_MACRO_0_FREE_SFLASH249	0x0FFF2F9
SFLASH_MACRO_0_FREE_SFLASH250	0x0FFF2FA
SFLASH_MACRO_0_FREE_SFLASH251	0x0FFF2FB
SFLASH_MACRO_0_FREE_SFLASH252	0x0FFF2FC
SFLASH_MACRO_0_FREE_SFLASH253	0x0FFF2FD
SFLASH_MACRO_0_FREE_SFLASH254	0x0FFF2FE
SFLASH_MACRO_0_FREE_SFLASH255	0x0FFF2FF
SFLASH_MACRO_0_FREE_SFLASH256	0x0FFF300
SFLASH_MACRO_0_FREE_SFLASH257	0x0FFF301
SFLASH_MACRO_0_FREE_SFLASH258	0x0FFF302
SFLASH_MACRO_0_FREE_SFLASH259	0x0FFF303
SFLASH_MACRO_0_FREE_SFLASH260	0x0FFF304
SFLASH_MACRO_0_FREE_SFLASH261	0x0FFF305
SFLASH_MACRO_0_FREE_SFLASH262	0x0FFF306
SFLASH_MACRO_0_FREE_SFLASH263	0x0FFF307
SFLASH_MACRO_0_FREE_SFLASH264	0x0FFF308

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH265	0x0FFF309
SFLASH_MACRO_0_FREE_SFLASH266	0x0FFF30A
SFLASH_MACRO_0_FREE_SFLASH267	0x0FFF30B
SFLASH_MACRO_0_FREE_SFLASH268	0x0FFF30C
SFLASH_MACRO_0_FREE_SFLASH269	0x0FFF30D
SFLASH_MACRO_0_FREE_SFLASH270	0x0FFF30E
SFLASH_MACRO_0_FREE_SFLASH271	0x0FFF30F
SFLASH_MACRO_0_FREE_SFLASH272	0x0FFF310
SFLASH_MACRO_0_FREE_SFLASH273	0x0FFF311
SFLASH_MACRO_0_FREE_SFLASH274	0x0FFF312
SFLASH_MACRO_0_FREE_SFLASH275	0x0FFF313
SFLASH_MACRO_0_FREE_SFLASH276	0x0FFF314
SFLASH_MACRO_0_FREE_SFLASH277	0x0FFF315
SFLASH_MACRO_0_FREE_SFLASH278	0x0FFF316
SFLASH_MACRO_0_FREE_SFLASH279	0x0FFF317
SFLASH_MACRO_0_FREE_SFLASH280	0x0FFF318
SFLASH_MACRO_0_FREE_SFLASH281	0x0FFF319
SFLASH_MACRO_0_FREE_SFLASH282	0x0FFF31A
SFLASH_MACRO_0_FREE_SFLASH283	0x0FFF31B
SFLASH_MACRO_0_FREE_SFLASH284	0x0FFF31C
SFLASH_MACRO_0_FREE_SFLASH285	0x0FFF31D
SFLASH_MACRO_0_FREE_SFLASH286	0x0FFF31E
SFLASH_MACRO_0_FREE_SFLASH287	0x0FFF31F
SFLASH_MACRO_0_FREE_SFLASH288	0x0FFF320
SFLASH_MACRO_0_FREE_SFLASH289	0x0FFF321
SFLASH_MACRO_0_FREE_SFLASH290	0x0FFF322
SFLASH_MACRO_0_FREE_SFLASH291	0x0FFF323
SFLASH_MACRO_0_FREE_SFLASH292	0x0FFF324
SFLASH_MACRO_0_FREE_SFLASH293	0x0FFF325
SFLASH_MACRO_0_FREE_SFLASH294	0x0FFF326
SFLASH_MACRO_0_FREE_SFLASH295	0x0FFF327
SFLASH_MACRO_0_FREE_SFLASH296	0x0FFF328
SFLASH_MACRO_0_FREE_SFLASH297	0x0FFF329
SFLASH_MACRO_0_FREE_SFLASH298	0x0FFF32A
SFLASH_MACRO_0_FREE_SFLASH299	0x0FFF32B
SFLASH_MACRO_0_FREE_SFLASH300	0x0FFF32C
SFLASH_MACRO_0_FREE_SFLASH301	0x0FFF32D
SFLASH_MACRO_0_FREE_SFLASH302	0x0FFF32E
SFLASH_MACRO_0_FREE_SFLASH303	0x0FFF32F
SFLASH_MACRO_0_FREE_SFLASH304	0x0FFF330
SFLASH_MACRO_0_FREE_SFLASH305	0x0FFF331
SFLASH_MACRO_0_FREE_SFLASH306	0x0FFF332

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH307	0x0FFF333
SFLASH_MACRO_0_FREE_SFLASH308	0x0FFF334
SFLASH_MACRO_0_FREE_SFLASH309	0x0FFF335
SFLASH_MACRO_0_FREE_SFLASH310	0x0FFF336
SFLASH_MACRO_0_FREE_SFLASH311	0x0FFF337
SFLASH_MACRO_0_FREE_SFLASH312	0x0FFF338
SFLASH_MACRO_0_FREE_SFLASH313	0x0FFF339
SFLASH_MACRO_0_FREE_SFLASH314	0x0FFF33A
SFLASH_MACRO_0_FREE_SFLASH315	0x0FFF33B
SFLASH_MACRO_0_FREE_SFLASH316	0x0FFF33C
SFLASH_MACRO_0_FREE_SFLASH317	0x0FFF33D
SFLASH_MACRO_0_FREE_SFLASH318	0x0FFF33E
SFLASH_MACRO_0_FREE_SFLASH319	0x0FFF33F
SFLASH_MACRO_0_FREE_SFLASH320	0x0FFF340
SFLASH_MACRO_0_FREE_SFLASH321	0x0FFF341
SFLASH_MACRO_0_FREE_SFLASH322	0x0FFF342
SFLASH_MACRO_0_FREE_SFLASH323	0x0FFF343
SFLASH_MACRO_0_FREE_SFLASH324	0x0FFF344
SFLASH_MACRO_0_FREE_SFLASH325	0x0FFF345
SFLASH_MACRO_0_FREE_SFLASH326	0x0FFF346
SFLASH_MACRO_0_FREE_SFLASH327	0x0FFF347
SFLASH_MACRO_0_FREE_SFLASH328	0x0FFF348
SFLASH_MACRO_0_FREE_SFLASH329	0x0FFF349
SFLASH_MACRO_0_FREE_SFLASH330	0x0FFF34A
SFLASH_MACRO_0_FREE_SFLASH331	0x0FFF34B
SFLASH_MACRO_0_FREE_SFLASH332	0x0FFF34C
SFLASH_MACRO_0_FREE_SFLASH333	0x0FFF34D
SFLASH_MACRO_0_FREE_SFLASH334	0x0FFF34E
SFLASH_MACRO_0_FREE_SFLASH335	0x0FFF34F
SFLASH_MACRO_0_FREE_SFLASH336	0x0FFF350
SFLASH_MACRO_0_FREE_SFLASH337	0x0FFF351
SFLASH_MACRO_0_FREE_SFLASH338	0x0FFF352
SFLASH_MACRO_0_FREE_SFLASH339	0x0FFF353
SFLASH_MACRO_0_FREE_SFLASH340	0x0FFF354
SFLASH_MACRO_0_FREE_SFLASH341	0x0FFF355
SFLASH_MACRO_0_FREE_SFLASH342	0x0FFF356
SFLASH_MACRO_0_FREE_SFLASH343	0x0FFF357
SFLASH_MACRO_0_FREE_SFLASH344	0x0FFF358
SFLASH_MACRO_0_FREE_SFLASH345	0x0FFF359
SFLASH_MACRO_0_FREE_SFLASH346	0x0FFF35A
SFLASH_MACRO_0_FREE_SFLASH347	0x0FFF35B
SFLASH_MACRO_0_FREE_SFLASH348	0x0FFF35C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH349	0x0FFF35D
SFLASH_MACRO_0_FREE_SFLASH350	0x0FFF35E
SFLASH_MACRO_0_FREE_SFLASH351	0x0FFF35F
SFLASH_MACRO_0_FREE_SFLASH352	0x0FFF360
SFLASH_MACRO_0_FREE_SFLASH353	0x0FFF361
SFLASH_MACRO_0_FREE_SFLASH354	0x0FFF362
SFLASH_MACRO_0_FREE_SFLASH355	0x0FFF363
SFLASH_MACRO_0_FREE_SFLASH356	0x0FFF364
SFLASH_MACRO_0_FREE_SFLASH357	0x0FFF365
SFLASH_MACRO_0_FREE_SFLASH358	0x0FFF366
SFLASH_MACRO_0_FREE_SFLASH359	0x0FFF367
SFLASH_MACRO_0_FREE_SFLASH360	0x0FFF368
SFLASH_MACRO_0_FREE_SFLASH361	0x0FFF369
SFLASH_MACRO_0_FREE_SFLASH362	0x0FFF36A
SFLASH_MACRO_0_FREE_SFLASH363	0x0FFF36B
SFLASH_MACRO_0_FREE_SFLASH364	0x0FFF36C
SFLASH_MACRO_0_FREE_SFLASH365	0x0FFF36D
SFLASH_MACRO_0_FREE_SFLASH366	0x0FFF36E
SFLASH_MACRO_0_FREE_SFLASH367	0x0FFF36F
SFLASH_MACRO_0_FREE_SFLASH368	0x0FFF370
SFLASH_MACRO_0_FREE_SFLASH369	0x0FFF371
SFLASH_MACRO_0_FREE_SFLASH370	0x0FFF372
SFLASH_MACRO_0_FREE_SFLASH371	0x0FFF373
SFLASH_MACRO_0_FREE_SFLASH372	0x0FFF374
SFLASH_MACRO_0_FREE_SFLASH373	0x0FFF375
SFLASH_MACRO_0_FREE_SFLASH374	0x0FFF376
SFLASH_MACRO_0_FREE_SFLASH375	0x0FFF377
SFLASH_MACRO_0_FREE_SFLASH376	0x0FFF378
SFLASH_MACRO_0_FREE_SFLASH377	0x0FFF379
SFLASH_MACRO_0_FREE_SFLASH378	0x0FFF37A
SFLASH_MACRO_0_FREE_SFLASH379	0x0FFF37B
SFLASH_MACRO_0_FREE_SFLASH380	0x0FFF37C
SFLASH_MACRO_0_FREE_SFLASH381	0x0FFF37D
SFLASH_MACRO_0_FREE_SFLASH382	0x0FFF37E
SFLASH_MACRO_0_FREE_SFLASH383	0x0FFF37F
SFLASH_MACRO_0_FREE_SFLASH384	0x0FFF380
SFLASH_MACRO_0_FREE_SFLASH385	0x0FFF381
SFLASH_MACRO_0_FREE_SFLASH386	0x0FFF382
SFLASH_MACRO_0_FREE_SFLASH387	0x0FFF383
SFLASH_MACRO_0_FREE_SFLASH388	0x0FFF384
SFLASH_MACRO_0_FREE_SFLASH389	0x0FFF385
SFLASH_MACRO_0_FREE_SFLASH390	0x0FFF386

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH391	0x0FFF387
SFLASH_MACRO_0_FREE_SFLASH392	0x0FFF388
SFLASH_MACRO_0_FREE_SFLASH393	0x0FFF389
SFLASH_MACRO_0_FREE_SFLASH394	0x0FFF38A
SFLASH_MACRO_0_FREE_SFLASH395	0x0FFF38B
SFLASH_MACRO_0_FREE_SFLASH396	0x0FFF38C
SFLASH_MACRO_0_FREE_SFLASH397	0x0FFF38D
SFLASH_MACRO_0_FREE_SFLASH398	0x0FFF38E
SFLASH_MACRO_0_FREE_SFLASH399	0x0FFF38F
SFLASH_MACRO_0_FREE_SFLASH400	0x0FFF390
SFLASH_MACRO_0_FREE_SFLASH401	0x0FFF391
SFLASH_MACRO_0_FREE_SFLASH402	0x0FFF392
SFLASH_MACRO_0_FREE_SFLASH403	0x0FFF393
SFLASH_MACRO_0_FREE_SFLASH404	0x0FFF394
SFLASH_MACRO_0_FREE_SFLASH405	0x0FFF395
SFLASH_MACRO_0_FREE_SFLASH406	0x0FFF396
SFLASH_MACRO_0_FREE_SFLASH407	0x0FFF397
SFLASH_MACRO_0_FREE_SFLASH408	0x0FFF398
SFLASH_MACRO_0_FREE_SFLASH409	0x0FFF399
SFLASH_MACRO_0_FREE_SFLASH410	0x0FFF39A
SFLASH_MACRO_0_FREE_SFLASH411	0x0FFF39B
SFLASH_MACRO_0_FREE_SFLASH412	0x0FFF39C
SFLASH_MACRO_0_FREE_SFLASH413	0x0FFF39D
SFLASH_MACRO_0_FREE_SFLASH414	0x0FFF39E
SFLASH_MACRO_0_FREE_SFLASH415	0x0FFF39F
SFLASH_MACRO_0_FREE_SFLASH416	0x0FFF3A0
SFLASH_MACRO_0_FREE_SFLASH417	0x0FFF3A1
SFLASH_MACRO_0_FREE_SFLASH418	0x0FFF3A2
SFLASH_MACRO_0_FREE_SFLASH419	0x0FFF3A3
SFLASH_MACRO_0_FREE_SFLASH420	0x0FFF3A4
SFLASH_MACRO_0_FREE_SFLASH421	0x0FFF3A5
SFLASH_MACRO_0_FREE_SFLASH422	0x0FFF3A6
SFLASH_MACRO_0_FREE_SFLASH423	0x0FFF3A7
SFLASH_MACRO_0_FREE_SFLASH424	0x0FFF3A8
SFLASH_MACRO_0_FREE_SFLASH425	0x0FFF3A9
SFLASH_MACRO_0_FREE_SFLASH426	0x0FFF3AA
SFLASH_MACRO_0_FREE_SFLASH427	0x0FFF3AB
SFLASH_MACRO_0_FREE_SFLASH428	0x0FFF3AC
SFLASH_MACRO_0_FREE_SFLASH429	0x0FFF3AD
SFLASH_MACRO_0_FREE_SFLASH430	0x0FFF3AE
SFLASH_MACRO_0_FREE_SFLASH431	0x0FFF3AF
SFLASH_MACRO_0_FREE_SFLASH432	0x0FFF3B0

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH433	0x0FFF3B1
SFLASH_MACRO_0_FREE_SFLASH434	0x0FFF3B2
SFLASH_MACRO_0_FREE_SFLASH435	0x0FFF3B3
SFLASH_MACRO_0_FREE_SFLASH436	0x0FFF3B4
SFLASH_MACRO_0_FREE_SFLASH437	0x0FFF3B5
SFLASH_MACRO_0_FREE_SFLASH438	0x0FFF3B6
SFLASH_MACRO_0_FREE_SFLASH439	0x0FFF3B7
SFLASH_MACRO_0_FREE_SFLASH440	0x0FFF3B8
SFLASH_MACRO_0_FREE_SFLASH441	0x0FFF3B9
SFLASH_MACRO_0_FREE_SFLASH442	0x0FFF3BA
SFLASH_MACRO_0_FREE_SFLASH443	0x0FFF3BB
SFLASH_MACRO_0_FREE_SFLASH444	0x0FFF3BC
SFLASH_MACRO_0_FREE_SFLASH445	0x0FFF3BD
SFLASH_MACRO_0_FREE_SFLASH446	0x0FFF3BE
SFLASH_MACRO_0_FREE_SFLASH447	0x0FFF3BF
SFLASH_MACRO_0_FREE_SFLASH448	0x0FFF3C0
SFLASH_MACRO_0_FREE_SFLASH449	0x0FFF3C1
SFLASH_MACRO_0_FREE_SFLASH450	0x0FFF3C2
SFLASH_MACRO_0_FREE_SFLASH451	0x0FFF3C3
SFLASH_MACRO_0_FREE_SFLASH452	0x0FFF3C4
SFLASH_MACRO_0_FREE_SFLASH453	0x0FFF3C5
SFLASH_MACRO_0_FREE_SFLASH454	0x0FFF3C6
SFLASH_MACRO_0_FREE_SFLASH455	0x0FFF3C7
SFLASH_MACRO_0_FREE_SFLASH456	0x0FFF3C8
SFLASH_MACRO_0_FREE_SFLASH457	0x0FFF3C9
SFLASH_MACRO_0_FREE_SFLASH458	0x0FFF3CA
SFLASH_MACRO_0_FREE_SFLASH459	0x0FFF3CB
SFLASH_MACRO_0_FREE_SFLASH460	0x0FFF3CC
SFLASH_MACRO_0_FREE_SFLASH461	0x0FFF3CD
SFLASH_MACRO_0_FREE_SFLASH462	0x0FFF3CE
SFLASH_MACRO_0_FREE_SFLASH463	0x0FFF3CF
SFLASH_MACRO_0_FREE_SFLASH464	0x0FFF3D0
SFLASH_MACRO_0_FREE_SFLASH465	0x0FFF3D1
SFLASH_MACRO_0_FREE_SFLASH466	0x0FFF3D2
SFLASH_MACRO_0_FREE_SFLASH467	0x0FFF3D3
SFLASH_MACRO_0_FREE_SFLASH468	0x0FFF3D4
SFLASH_MACRO_0_FREE_SFLASH469	0x0FFF3D5
SFLASH_MACRO_0_FREE_SFLASH470	0x0FFF3D6
SFLASH_MACRO_0_FREE_SFLASH471	0x0FFF3D7
SFLASH_MACRO_0_FREE_SFLASH472	0x0FFF3D8
SFLASH_MACRO_0_FREE_SFLASH473	0x0FFF3D9
SFLASH_MACRO_0_FREE_SFLASH474	0x0FFF3DA

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH475	0x0FFF3DB
SFLASH_MACRO_0_FREE_SFLASH476	0x0FFF3DC
SFLASH_MACRO_0_FREE_SFLASH477	0x0FFF3DD
SFLASH_MACRO_0_FREE_SFLASH478	0x0FFF3DE
SFLASH_MACRO_0_FREE_SFLASH479	0x0FFF3DF
SFLASH_MACRO_0_FREE_SFLASH480	0x0FFF3E0
SFLASH_MACRO_0_FREE_SFLASH481	0x0FFF3E1
SFLASH_MACRO_0_FREE_SFLASH482	0x0FFF3E2
SFLASH_MACRO_0_FREE_SFLASH483	0x0FFF3E3
SFLASH_MACRO_0_FREE_SFLASH484	0x0FFF3E4
SFLASH_MACRO_0_FREE_SFLASH485	0x0FFF3E5
SFLASH_MACRO_0_FREE_SFLASH486	0x0FFF3E6
SFLASH_MACRO_0_FREE_SFLASH487	0x0FFF3E7
SFLASH_MACRO_0_FREE_SFLASH488	0x0FFF3E8
SFLASH_MACRO_0_FREE_SFLASH489	0x0FFF3E9
SFLASH_MACRO_0_FREE_SFLASH490	0x0FFF3EA
SFLASH_MACRO_0_FREE_SFLASH491	0x0FFF3EB
SFLASH_MACRO_0_FREE_SFLASH492	0x0FFF3EC
SFLASH_MACRO_0_FREE_SFLASH493	0x0FFF3ED
SFLASH_MACRO_0_FREE_SFLASH494	0x0FFF3EE
SFLASH_MACRO_0_FREE_SFLASH495	0x0FFF3EF
SFLASH_MACRO_0_FREE_SFLASH496	0x0FFF3F0
SFLASH_MACRO_0_FREE_SFLASH497	0x0FFF3F1
SFLASH_MACRO_0_FREE_SFLASH498	0x0FFF3F2
SFLASH_MACRO_0_FREE_SFLASH499	0x0FFF3F3
SFLASH_MACRO_0_FREE_SFLASH500	0x0FFF3F4
SFLASH_MACRO_0_FREE_SFLASH501	0x0FFF3F5
SFLASH_MACRO_0_FREE_SFLASH502	0x0FFF3F6
SFLASH_MACRO_0_FREE_SFLASH503	0x0FFF3F7
SFLASH_MACRO_0_FREE_SFLASH504	0x0FFF3F8
SFLASH_MACRO_0_FREE_SFLASH505	0x0FFF3F9
SFLASH_MACRO_0_FREE_SFLASH506	0x0FFF3FA
SFLASH_MACRO_0_FREE_SFLASH507	0x0FFF3FB
SFLASH_MACRO_0_FREE_SFLASH508	0x0FFF3FC
SFLASH_MACRO_0_FREE_SFLASH509	0x0FFF3FD
SFLASH_MACRO_0_FREE_SFLASH510	0x0FFF3FE
SFLASH_MACRO_0_FREE_SFLASH511	0x0FFF3FF
SFLASH_ALT_PROT_ROW0	0x0FFF400
SFLASH_ALT_PROT_ROW1	0x0FFF401
SFLASH_ALT_PROT_ROW2	0x0FFF402
SFLASH_ALT_PROT_ROW3	0x0FFF403
SFLASH_ALT_PROT_ROW4	0x0FFF404

Register Name	Address
SFLASH_ALT_PROT_ROW5	0x0FFF405
SFLASH_ALT_PROT_ROW6	0x0FFF406
SFLASH_ALT_PROT_ROW7	0x0FFF407
SFLASH_ALT_PROT_ROW8	0x0FFF408
SFLASH_ALT_PROT_ROW9	0x0FFF409
SFLASH_ALT_PROT_ROW10	0x0FFF40A
SFLASH_ALT_PROT_ROW11	0x0FFF40B
SFLASH_ALT_PROT_ROW12	0x0FFF40C
SFLASH_ALT_PROT_ROW13	0x0FFF40D
SFLASH_ALT_PROT_ROW14	0x0FFF40E
SFLASH_ALT_PROT_ROW15	0x0FFF40F
SFLASH_ALT_PROT_ROW16	0x0FFF410
SFLASH_ALT_PROT_ROW17	0x0FFF411
SFLASH_ALT_PROT_ROW18	0x0FFF412
SFLASH_ALT_PROT_ROW19	0x0FFF413
SFLASH_ALT_PROT_ROW20	0x0FFF414
SFLASH_ALT_PROT_ROW21	0x0FFF415
SFLASH_ALT_PROT_ROW22	0x0FFF416
SFLASH_ALT_PROT_ROW23	0x0FFF417
SFLASH_ALT_PROT_ROW24	0x0FFF418
SFLASH_ALT_PROT_ROW25	0x0FFF419
SFLASH_ALT_PROT_ROW26	0x0FFF41A
SFLASH_ALT_PROT_ROW27	0x0FFF41B
SFLASH_ALT_PROT_ROW28	0x0FFF41C
SFLASH_ALT_PROT_ROW29	0x0FFF41D
SFLASH_ALT_PROT_ROW30	0x0FFF41E
SFLASH_ALT_PROT_ROW31	0x0FFF41F
SFLASH_ALT_PROT_ROW32	0x0FFF420
SFLASH_ALT_PROT_ROW33	0x0FFF421
SFLASH_ALT_PROT_ROW34	0x0FFF422
SFLASH_ALT_PROT_ROW35	0x0FFF423
SFLASH_ALT_PROT_ROW36	0x0FFF424
SFLASH_ALT_PROT_ROW37	0x0FFF425
SFLASH_ALT_PROT_ROW38	0x0FFF426
SFLASH_ALT_PROT_ROW39	0x0FFF427
SFLASH_ALT_PROT_ROW40	0x0FFF428
SFLASH_ALT_PROT_ROW41	0x0FFF429
SFLASH_ALT_PROT_ROW42	0x0FFF42A
SFLASH_ALT_PROT_ROW43	0x0FFF42B
SFLASH_ALT_PROT_ROW44	0x0FFF42C
SFLASH_ALT_PROT_ROW45	0x0FFF42D
SFLASH_ALT_PROT_ROW46	0x0FFF42E



Register Name	Address
SFLASH_ALT_PROT_ROW47	0x0FFF42F
SFLASH_ALT_PROT_ROW48	0x0FFF430
SFLASH_ALT_PROT_ROW49	0x0FFF431
SFLASH_ALT_PROT_ROW50	0x0FFF432
SFLASH_ALT_PROT_ROW51	0x0FFF433
SFLASH_ALT_PROT_ROW52	0x0FFF434
SFLASH_ALT_PROT_ROW53	0x0FFF435
SFLASH_ALT_PROT_ROW54	0x0FFF436
SFLASH_ALT_PROT_ROW55	0x0FFF437
SFLASH_ALT_PROT_ROW56	0x0FFF438
SFLASH_ALT_PROT_ROW57	0x0FFF439
SFLASH_ALT_PROT_ROW58	0x0FFF43A
SFLASH_ALT_PROT_ROW59	0x0FFF43B
SFLASH_ALT_PROT_ROW60	0x0FFF43C
SFLASH_ALT_PROT_ROW61	0x0FFF43D
SFLASH_ALT_PROT_ROW62	0x0FFF43E
SFLASH_ALT_PROT_ROW63	0x0FFF43F
SFLASH_ALT_PROT_ROW64	0x0FFF440
SFLASH_ALT_PROT_ROW65	0x0FFF441
SFLASH_ALT_PROT_ROW66	0x0FFF442
SFLASH_ALT_PROT_ROW67	0x0FFF443
SFLASH_ALT_PROT_ROW68	0x0FFF444
SFLASH_ALT_PROT_ROW69	0x0FFF445
SFLASH_ALT_PROT_ROW70	0x0FFF446
SFLASH_ALT_PROT_ROW71	0x0FFF447
SFLASH_ALT_PROT_ROW72	0x0FFF448
SFLASH_ALT_PROT_ROW73	0x0FFF449
SFLASH_ALT_PROT_ROW74	0x0FFF44A
SFLASH_ALT_PROT_ROW75	0x0FFF44B
SFLASH_ALT_PROT_ROW76	0x0FFF44C
SFLASH_ALT_PROT_ROW77	0x0FFF44D
SFLASH_ALT_PROT_ROW78	0x0FFF44E
SFLASH_ALT_PROT_ROW79	0x0FFF44F
SFLASH_ALT_PROT_ROW80	0x0FFF450
SFLASH_ALT_PROT_ROW81	0x0FFF451
SFLASH_ALT_PROT_ROW82	0x0FFF452
SFLASH_ALT_PROT_ROW83	0x0FFF453
SFLASH_ALT_PROT_ROW84	0x0FFF454
SFLASH_ALT_PROT_ROW85	0x0FFF455
SFLASH_ALT_PROT_ROW86	0x0FFF456
SFLASH_ALT_PROT_ROW87	0x0FFF457
SFLASH_ALT_PROT_ROW88	0x0FFF458

Register Name	Address
SFLASH_ALT_PROT_ROW89	0x0FFF459
SFLASH_ALT_PROT_ROW90	0x0FFF45A
SFLASH_ALT_PROT_ROW91	0x0FFF45B
SFLASH_ALT_PROT_ROW92	0x0FFF45C
SFLASH_ALT_PROT_ROW93	0x0FFF45D
SFLASH_ALT_PROT_ROW94	0x0FFF45E
SFLASH_ALT_PROT_ROW95	0x0FFF45F
SFLASH_ALT_PROT_ROW96	0x0FFF460
SFLASH_ALT_PROT_ROW97	0x0FFF461
SFLASH_ALT_PROT_ROW98	0x0FFF462
SFLASH_ALT_PROT_ROW99	0x0FFF463
SFLASH_ALT_PROT_ROW100	0x0FFF464
SFLASH_ALT_PROT_ROW101	0x0FFF465
SFLASH_ALT_PROT_ROW102	0x0FFF466
SFLASH_ALT_PROT_ROW103	0x0FFF467
SFLASH_ALT_PROT_ROW104	0x0FFF468
SFLASH_ALT_PROT_ROW105	0x0FFF469
SFLASH_ALT_PROT_ROW106	0x0FFF46A
SFLASH_ALT_PROT_ROW107	0x0FFF46B
SFLASH_ALT_PROT_ROW108	0x0FFF46C
SFLASH_ALT_PROT_ROW109	0x0FFF46D
SFLASH_ALT_PROT_ROW110	0x0FFF46E
SFLASH_ALT_PROT_ROW111	0x0FFF46F
SFLASH_ALT_PROT_ROW112	0x0FFF470
SFLASH_ALT_PROT_ROW113	0x0FFF471
SFLASH_ALT_PROT_ROW114	0x0FFF472
SFLASH_ALT_PROT_ROW115	0x0FFF473
SFLASH_ALT_PROT_ROW116	0x0FFF474
SFLASH_ALT_PROT_ROW117	0x0FFF475
SFLASH_ALT_PROT_ROW118	0x0FFF476
SFLASH_ALT_PROT_ROW119	0x0FFF477
SFLASH_ALT_PROT_ROW120	0x0FFF478
SFLASH_ALT_PROT_ROW121	0x0FFF479
SFLASH_ALT_PROT_ROW122	0x0FFF47A
SFLASH_ALT_PROT_ROW123	0x0FFF47B
SFLASH_ALT_PROT_ROW124	0x0FFF47C
SFLASH_ALT_PROT_ROW125	0x0FFF47D
SFLASH_ALT_PROT_ROW126	0x0FFF47E
SFLASH_ALT_PROT_ROW127	0x0FFF47F
SFLASH_ALT_PROT_ROW128	0x0FFF480
SFLASH_ALT_PROT_ROW129	0x0FFF481
SFLASH_ALT_PROT_ROW130	0x0FFF482

Register Name	Address
SFLASH_ALT_PROT_ROW131	0x0FFF483
SFLASH_ALT_PROT_ROW132	0x0FFF484
SFLASH_ALT_PROT_ROW133	0x0FFF485
SFLASH_ALT_PROT_ROW134	0x0FFF486
SFLASH_ALT_PROT_ROW135	0x0FFF487
SFLASH_ALT_PROT_ROW136	0x0FFF488
SFLASH_ALT_PROT_ROW137	0x0FFF489
SFLASH_ALT_PROT_ROW138	0x0FFF48A
SFLASH_ALT_PROT_ROW139	0x0FFF48B
SFLASH_ALT_PROT_ROW140	0x0FFF48C
SFLASH_ALT_PROT_ROW141	0x0FFF48D
SFLASH_ALT_PROT_ROW142	0x0FFF48E
SFLASH_ALT_PROT_ROW143	0x0FFF48F
SFLASH_ALT_PROT_ROW144	0x0FFF490
SFLASH_ALT_PROT_ROW145	0x0FFF491
SFLASH_ALT_PROT_ROW146	0x0FFF492
SFLASH_ALT_PROT_ROW147	0x0FFF493
SFLASH_ALT_PROT_ROW148	0x0FFF494
SFLASH_ALT_PROT_ROW149	0x0FFF495
SFLASH_ALT_PROT_ROW150	0x0FFF496
SFLASH_ALT_PROT_ROW151	0x0FFF497
SFLASH_ALT_PROT_ROW152	0x0FFF498
SFLASH_ALT_PROT_ROW153	0x0FFF499
SFLASH_ALT_PROT_ROW154	0x0FFF49A
SFLASH_ALT_PROT_ROW155	0x0FFF49B
SFLASH_ALT_PROT_ROW156	0x0FFF49C
SFLASH_ALT_PROT_ROW157	0x0FFF49D
SFLASH_ALT_PROT_ROW158	0x0FFF49E
SFLASH_ALT_PROT_ROW159	0x0FFF49F
SFLASH_ALT_PROT_ROW160	0x0FFF4A0
SFLASH_ALT_PROT_ROW161	0x0FFF4A1
SFLASH_ALT_PROT_ROW162	0x0FFF4A2
SFLASH_ALT_PROT_ROW163	0x0FFF4A3
SFLASH_ALT_PROT_ROW164	0x0FFF4A4
SFLASH_ALT_PROT_ROW165	0x0FFF4A5
SFLASH_ALT_PROT_ROW166	0x0FFF4A6
SFLASH_ALT_PROT_ROW167	0x0FFF4A7
SFLASH_ALT_PROT_ROW168	0x0FFF4A8
SFLASH_ALT_PROT_ROW169	0x0FFF4A9
SFLASH_ALT_PROT_ROW170	0x0FFF4AA
SFLASH_ALT_PROT_ROW171	0x0FFF4AB
SFLASH_ALT_PROT_ROW172	0x0FFF4AC

Register Name	Address
SFLASH_ALT_PROT_ROW173	0x0FFF4AD
SFLASH_ALT_PROT_ROW174	0x0FFF4AE
SFLASH_ALT_PROT_ROW175	0x0FFF4AF
SFLASH_ALT_PROT_ROW176	0x0FFF4B0
SFLASH_ALT_PROT_ROW177	0x0FFF4B1
SFLASH_ALT_PROT_ROW178	0x0FFF4B2
SFLASH_ALT_PROT_ROW179	0x0FFF4B3
SFLASH_ALT_PROT_ROW180	0x0FFF4B4
SFLASH_ALT_PROT_ROW181	0x0FFF4B5
SFLASH_ALT_PROT_ROW182	0x0FFF4B6
SFLASH_ALT_PROT_ROW183	0x0FFF4B7
SFLASH_ALT_PROT_ROW184	0x0FFF4B8
SFLASH_ALT_PROT_ROW185	0x0FFF4B9
SFLASH_ALT_PROT_ROW186	0x0FFF4BA
SFLASH_ALT_PROT_ROW187	0x0FFF4BB
SFLASH_ALT_PROT_ROW188	0x0FFF4BC
SFLASH_ALT_PROT_ROW189	0x0FFF4BD
SFLASH_ALT_PROT_ROW190	0x0FFF4BE
SFLASH_ALT_PROT_ROW191	0x0FFF4BF
SFLASH_ALT_PROT_ROW192	0x0FFF4C0
SFLASH_ALT_PROT_ROW193	0x0FFF4C1
SFLASH_ALT_PROT_ROW194	0x0FFF4C2
SFLASH_ALT_PROT_ROW195	0x0FFF4C3
SFLASH_ALT_PROT_ROW196	0x0FFF4C4
SFLASH_ALT_PROT_ROW197	0x0FFF4C5
SFLASH_ALT_PROT_ROW198	0x0FFF4C6
SFLASH_ALT_PROT_ROW199	0x0FFF4C7
SFLASH_ALT_PROT_ROW200	0x0FFF4C8
SFLASH_ALT_PROT_ROW201	0x0FFF4C9
SFLASH_ALT_PROT_ROW202	0x0FFF4CA
SFLASH_ALT_PROT_ROW203	0x0FFF4CB
SFLASH_ALT_PROT_ROW204	0x0FFF4CC
SFLASH_ALT_PROT_ROW205	0x0FFF4CD
SFLASH_ALT_PROT_ROW206	0x0FFF4CE
SFLASH_ALT_PROT_ROW207	0x0FFF4CF
SFLASH_ALT_PROT_ROW208	0x0FFF4D0
SFLASH_ALT_PROT_ROW209	0x0FFF4D1
SFLASH_ALT_PROT_ROW210	0x0FFF4D2
SFLASH_ALT_PROT_ROW211	0x0FFF4D3
SFLASH_ALT_PROT_ROW212	0x0FFF4D4
SFLASH_ALT_PROT_ROW213	0x0FFF4D5
SFLASH_ALT_PROT_ROW214	0x0FFF4D6

Register Name	Address
SFLASH_ALT_PROT_ROW215	0x0FFF4D7
SFLASH_ALT_PROT_ROW216	0x0FFF4D8
SFLASH_ALT_PROT_ROW217	0x0FFF4D9
SFLASH_ALT_PROT_ROW218	0x0FFF4DA
SFLASH_ALT_PROT_ROW219	0x0FFF4DB
SFLASH_ALT_PROT_ROW220	0x0FFF4DC
SFLASH_ALT_PROT_ROW221	0x0FFF4DD
SFLASH_ALT_PROT_ROW222	0x0FFF4DE
SFLASH_ALT_PROT_ROW223	0x0FFF4DF
SFLASH_ALT_PROT_ROW224	0x0FFF4E0
SFLASH_ALT_PROT_ROW225	0x0FFF4E1
SFLASH_ALT_PROT_ROW226	0x0FFF4E2
SFLASH_ALT_PROT_ROW227	0x0FFF4E3
SFLASH_ALT_PROT_ROW228	0x0FFF4E4
SFLASH_ALT_PROT_ROW229	0x0FFF4E5
SFLASH_ALT_PROT_ROW230	0x0FFF4E6
SFLASH_ALT_PROT_ROW231	0x0FFF4E7
SFLASH_ALT_PROT_ROW232	0x0FFF4E8
SFLASH_ALT_PROT_ROW233	0x0FFF4E9
SFLASH_ALT_PROT_ROW234	0x0FFF4EA
SFLASH_ALT_PROT_ROW235	0x0FFF4EB
SFLASH_ALT_PROT_ROW236	0x0FFF4EC
SFLASH_ALT_PROT_ROW237	0x0FFF4ED
SFLASH_ALT_PROT_ROW238	0x0FFF4EE
SFLASH_ALT_PROT_ROW239	0x0FFF4EF
SFLASH_ALT_PROT_ROW240	0x0FFF4F0
SFLASH_ALT_PROT_ROW241	0x0FFF4F1
SFLASH_ALT_PROT_ROW242	0x0FFF4F2
SFLASH_ALT_PROT_ROW243	0x0FFF4F3
SFLASH_ALT_PROT_ROW244	0x0FFF4F4
SFLASH_ALT_PROT_ROW245	0x0FFF4F5
SFLASH_ALT_PROT_ROW246	0x0FFF4F6
SFLASH_ALT_PROT_ROW247	0x0FFF4F7
SFLASH_ALT_PROT_ROW248	0x0FFF4F8
SFLASH_ALT_PROT_ROW249	0x0FFF4F9
SFLASH_ALT_PROT_ROW250	0x0FFF4FA
SFLASH_ALT_PROT_ROW251	0x0FFF4FB
SFLASH_ALT_PROT_ROW252	0x0FFF4FC
SFLASH_ALT_PROT_ROW253	0x0FFF4FD
SFLASH_ALT_PROT_ROW254	0x0FFF4FE
SFLASH_ALT_PROT_ROW255	0x0FFF4FF
SFLASH_ALT_PP	0x0FFF5A0

Register Name	Address
SFLASH_ALT_E	0x0FFF5A4
SFLASH_ALT_P	0x0FFF5A8
SFLASH_ALT_EA_E	0x0FFF5AC
SFLASH_ALT_EA_P	0x0FFF5B0
SFLASH_ALT_ES_E	0x0FFF5B4
SFLASH_ALT_ES_P_EO	0x0FFF5B8
SFLASH_ALT_E_VCTAT	0x0FFF5BC
SFLASH_ALT_P_VCTAT	0x0FFF5BD

## 21.1.1 SFLASH\_PROT\_ROW0

Per Page Write Protection

Address: 0x0FFF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.2 SFLASH\_PROT\_ROW1

Per Page Write Protection

Address: 0x0FFF001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.3 SFLASH\_PROT\_ROW2

Per Page Write Protection

Address: 0x0FFF002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.4 SFLASH\_PROT\_ROW3

Per Page Write Protection

Address: 0x0FFF003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.5 SFLASH\_PROT\_ROW4

Per Page Write Protection

Address: 0x0FFF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.6 SFLASH\_PROT\_ROW5

Per Page Write Protection

Address: 0x0FFF005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.7 SFLASH\_PROT\_ROW6

Per Page Write Protection

Address: 0x0FFF006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.8 SFLASH\_PROT\_ROW7

Per Page Write Protection

Address: 0x0FFF007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.9 SFLASH\_PROT\_ROW8

Per Page Write Protection

Address: 0x0FFF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.10 SFLASH\_PROT\_ROW9

Per Page Write Protection

Address: 0x0FFF009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.11 SFLASH\_PROT\_ROW10

Per Page Write Protection

Address: 0x0FFF00A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.12 SFLASH\_PROT\_ROW11

Per Page Write Protection

Address: 0x0FFF00B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.13 SFLASH\_PROT\_ROW12

Per Page Write Protection

Address: 0x0FFF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.14 SFLASH\_PROT\_ROW13

Per Page Write Protection

Address: 0x0FFF00D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.15 SFLASH\_PROT\_ROW14

Per Page Write Protection

Address: 0x0FFF00E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.16 SFLASH\_PROT\_ROW15

Per Page Write Protection

Address: 0x0FFF00F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.17 SFLASH\_PROT\_ROW16

Per Page Write Protection

Address: 0x0FFF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.18 SFLASH\_PROT\_ROW17

Per Page Write Protection

Address: 0x0FFF011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.19 SFLASH\_PROT\_ROW18

Per Page Write Protection

Address: 0x0FFF012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.20 SFLASH\_PROT\_ROW19

Per Page Write Protection

Address: 0x0FFF013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.21 SFLASH\_PROT\_ROW20

Per Page Write Protection

Address: 0x0FFF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.22 SFLASH\_PROT\_ROW21

Per Page Write Protection

Address: 0x0FFF015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.23 SFLASH\_PROT\_ROW22

Per Page Write Protection

Address: 0x0FFF016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.24 SFLASH\_PROT\_ROW23

Per Page Write Protection

Address: 0x0FFFF017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.25 SFLASH\_PROT\_ROW24

Per Page Write Protection

Address: 0x0FFF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.26 SFLASH\_PROT\_ROW25

Per Page Write Protection

Address: 0x0FFF019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.27 SFLASH\_PROT\_ROW26

Per Page Write Protection

Address: 0x0FFF01A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.28 SFLASH\_PROT\_ROW27

Per Page Write Protection

Address: 0x0FFF01B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.29 SFLASH\_PROT\_ROW28

Per Page Write Protection

Address: 0x0FFF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.30 SFLASH\_PROT\_ROW29

Per Page Write Protection

Address: 0x0FFF01D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.31 SFLASH\_PROT\_ROW30

Per Page Write Protection

Address: 0x0FFF01E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.32 SFLASH\_PROT\_ROW31

Per Page Write Protection

Address: 0x0FFFF01F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.33 SFLASH\_PROT\_ROW32

Per Page Write Protection

Address: 0x0FFF020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.34 SFLASH\_PROT\_ROW33

Per Page Write Protection

Address: 0x0FFF021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.35 SFLASH\_PROT\_ROW34

Per Page Write Protection

Address: 0x0FFF022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.36 SFLASH\_PROT\_ROW35

Per Page Write Protection

Address: 0x0FFF023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.37 SFLASH\_PROT\_ROW36

Per Page Write Protection

Address: 0x0FFF024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.38 SFLASH\_PROT\_ROW37

Per Page Write Protection

Address: 0x0FFF025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.39 SFLASH\_PROT\_ROW38

Per Page Write Protection

Address: 0x0FFF026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.40 SFLASH\_PROT\_ROW39

Per Page Write Protection

Address: 0x0FFF027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.41 SFLASH\_PROT\_ROW40

Per Page Write Protection

Address: 0x0FFF028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.42 SFLASH\_PROT\_ROW41

Per Page Write Protection

Address: 0x0FFF029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.43 SFLASH\_PROT\_ROW42

Per Page Write Protection

Address: 0x0FFF02A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.44 SFLASH\_PROT\_ROW43

Per Page Write Protection

Address: 0x0FFF02B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.45 SFLASH\_PROT\_ROW44

Per Page Write Protection

Address: 0x0FFF02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.46 SFLASH\_PROT\_ROW45

Per Page Write Protection

Address: 0x0FFF02D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.47 SFLASH\_PROT\_ROW46

Per Page Write Protection

Address: 0x0FFF02E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.48 SFLASH\_PROT\_ROW47

Per Page Write Protection

Address: 0x0FFF02F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.49 SFLASH\_PROT\_ROW48

Per Page Write Protection

Address: 0x0FFF030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.50 SFLASH\_PROT\_ROW49

Per Page Write Protection

Address: 0x0FFF031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.51 SFLASH\_PROT\_ROW50

Per Page Write Protection

Address: 0x0FFF032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.52 SFLASH\_PROT\_ROW51

Per Page Write Protection

Address: 0x0FFF033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.53 SFLASH\_PROT\_ROW52

Per Page Write Protection

Address: 0x0FFF034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.54 SFLASH\_PROT\_ROW53

Per Page Write Protection

Address: 0x0FFF035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.55 SFLASH\_PROT\_ROW54

Per Page Write Protection

Address: 0x0FFF036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.56 SFLASH\_PROT\_ROW55

Per Page Write Protection

Address: 0x0FFF037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.57 SFLASH\_PROT\_ROW56

Per Page Write Protection

Address: 0x0FFF038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.58 SFLASH\_PROT\_ROW57

Per Page Write Protection

Address: 0x0FFF039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.59 SFLASH\_PROT\_ROW58

Per Page Write Protection

Address: 0x0FFF03A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.60 SFLASH\_PROT\_ROW59

Per Page Write Protection

Address: 0x0FFF03B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.61 SFLASH\_PROT\_ROW60

Per Page Write Protection

Address: 0x0FFF03C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.62 SFLASH\_PROT\_ROW61

Per Page Write Protection

Address: 0x0FFF03D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.63 SFLASH\_PROT\_ROW62

Per Page Write Protection

Address: 0x0FFF03E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.64 SFLASH\_PROT\_ROW63

Per Page Write Protection

Address: 0x0FFF03F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.65 SFLASH\_PROT\_PROTECTION

Protection Level

Address: 0x0FFF07F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						None	
Name	None [7:2]						PROT_LEVEL [1:0]	

Bits	Name	Description
1 : 0	PROT_LEVEL	<p>Current Protection Mode - note that encoding is different from CPUSS_PROTECTION !! Default Value: X</p> <p><b>0x0: OPEN:</b> System is in OPEN mode</p> <p><b>0x1: VIRGIN:</b> System is in VIRGIN mode</p> <p><b>0x2: PROTECTED:</b> System is in PROTECTED mode</p> <p><b>0x3: KILL:</b> System is in KILL mode</p>

## 21.1.66 SFLASH\_AV\_PAIRS\_8B0

8b Addr/Value pair Section

Address: 0x0FFF080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.67 SFLASH\_AV\_PAIRS\_8B1

8b Addr/Value pair Section

Address: 0x0FFF081

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.68 SFLASH\_AV\_PAIRS\_8B2

8b Addr/Value pair Section

Address: 0x0FFF082

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.69 SFLASH\_AV\_PAIRS\_8B3

8b Addr/Value pair Section

Address: 0x0FFF083

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.70 SFLASH\_AV\_PAIRS\_8B4

8b Addr/Value pair Section

Address: 0x0FFF084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.71 SFLASH\_AV\_PAIRS\_8B5

8b Addr/Value pair Section

Address: 0x0FFF085

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.72 SFLASH\_AV\_PAIRS\_8B6

8b Addr/Value pair Section

Address: 0x0FFF086

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.73 SFLASH\_AV\_PAIRS\_8B7

8b Addr/Value pair Section

Address: 0x0FFF087

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.74 SFLASH\_AV\_PAIRS\_8B8

8b Addr/Value pair Section

Address: 0x0FFF088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.75 SFLASH\_AV\_PAIRS\_8B9

8b Addr/Value pair Section

Address: 0x0FFF089

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.76 SFLASH\_AV\_PAIRS\_8B10

8b Addr/Value pair Section

Address: 0x0FFF08A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.77 SFLASH\_AV\_PAIRS\_8B11

8b Addr/Value pair Section

Address: 0x0FFF08B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.78 SFLASH\_AV\_PAIRS\_8B12

8b Addr/Value pair Section

Address: 0x0FFF08C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.79 SFLASH\_AV\_PAIRS\_8B13

8b Addr/Value pair Section

Address: 0x0FFF08D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.80 SFLASH\_AV\_PAIRS\_8B14

8b Addr/Value pair Section

Address: 0x0FFF08E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.81 SFLASH\_AV\_PAIRS\_8B15

8b Addr/Value pair Section

Address: 0x0FFFF08F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.82 SFLASH\_AV\_PAIRS\_8B16

8b Addr/Value pair Section

Address: 0x0FFF090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.83 SFLASH\_AV\_PAIRS\_8B17

8b Addr/Value pair Section

Address: 0x0FFF091

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.84 SFLASH\_AV\_PAIRS\_8B18

8b Addr/Value pair Section

Address: 0x0FFF092

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.85 SFLASH\_AV\_PAIRS\_8B19

8b Addr/Value pair Section

Address: 0x0FFF093

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.86 SFLASH\_AV\_PAIRS\_8B20

8b Addr/Value pair Section

Address: 0x0FFF094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.87 SFLASH\_AV\_PAIRS\_8B21

8b Addr/Value pair Section

Address: 0x0FFF095

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.88 SFLASH\_AV\_PAIRS\_8B22

8b Addr/Value pair Section

Address: 0x0FFF096

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.89 SFLASH\_AV\_PAIRS\_8B23

8b Addr/Value pair Section

Address: 0x0FFF097

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.90 SFLASH\_AV\_PAIRS\_8B24

8b Addr/Value pair Section

Address: 0x0FFF098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.91 SFLASH\_AV\_PAIRS\_8B25

8b Addr/Value pair Section

Address: 0x0FFF099

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.92 SFLASH\_AV\_PAIRS\_8B26

8b Addr/Value pair Section

Address: 0x0FFF09A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.93 SFLASH\_AV\_PAIRS\_8B27

8b Addr/Value pair Section

Address: 0x0FFF09B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.94 SFLASH\_AV\_PAIRS\_8B28

8b Addr/Value pair Section

Address: 0x0FFF09C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.95 SFLASH\_AV\_PAIRS\_8B29

8b Addr/Value pair Section

Address: 0x0FFF09D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.96 SFLASH\_AV\_PAIRS\_8B30

8b Addr/Value pair Section

Address: 0x0FFF09E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.97 SFLASH\_AV\_PAIRS\_8B31

8b Addr/Value pair Section

Address: 0x0FFFF09F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.98 SFLASH\_AV\_PAIRS\_8B32

8b Addr/Value pair Section

Address: 0x0FFF0A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.99 SFLASH\_AV\_PAIRS\_8B33

8b Addr/Value pair Section

Address: 0x0FFF0A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.100 SFLASH\_AV\_PAIRS\_8B34

8b Addr/Value pair Section

Address: 0x0FFF0A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.101 SFLASH\_AV\_PAIRS\_8B35

8b Addr/Value pair Section

Address: 0x0FFF0A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.102 SFLASH\_AV\_PAIRS\_8B36

8b Addr/Value pair Section

Address: 0x0FFF0A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.103 SFLASH\_AV\_PAIRS\_8B37

8b Addr/Value pair Section

Address: 0x0FFF0A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.104 SFLASH\_AV\_PAIRS\_8B38

8b Addr/Value pair Section

Address: 0x0FFF0A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.105 SFLASH\_AV\_PAIRS\_8B39

8b Addr/Value pair Section

Address: 0x0FFF0A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.106 SFLASH\_AV\_PAIRS\_8B40

8b Addr/Value pair Section

Address: 0x0FFF0A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.107 SFLASH\_AV\_PAIRS\_8B41

8b Addr/Value pair Section

Address: 0x0FFF0A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.108 SFLASH\_AV\_PAIRS\_8B42

8b Addr/Value pair Section

Address: 0x0FFFF0AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.109 SFLASH\_AV\_PAIRS\_8B43

8b Addr/Value pair Section

Address: 0x0FFFF0AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.110 SFLASH\_AV\_PAIRS\_8B44

8b Addr/Value pair Section

Address: 0x0FFFF0AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.111 SFLASH\_AV\_PAIRS\_8B45

8b Addr/Value pair Section

Address: 0x0FFFF0AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.112 SFLASH\_AV\_PAIRS\_8B46

8b Addr/Value pair Section

Address: 0x0FFFF0AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.113 SFLASH\_AV\_PAIRS\_8B47

8b Addr/Value pair Section

Address: 0x0FFF0AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.114 SFLASH\_AV\_PAIRS\_8B48

8b Addr/Value pair Section

Address: 0x0FFF0B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.115 SFLASH\_AV\_PAIRS\_8B49

8b Addr/Value pair Section

Address: 0x0FFF0B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.116 SFLASH\_AV\_PAIRS\_8B50

8b Addr/Value pair Section

Address: 0x0FFF0B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.117 SFLASH\_AV\_PAIRS\_8B51

8b Addr/Value pair Section

Address: 0x0FFF0B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.118 SFLASH\_AV\_PAIRS\_8B52

8b Addr/Value pair Section

Address: 0x0FFF0B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.119 SFLASH\_AV\_PAIRS\_8B53

8b Addr/Value pair Section

Address: 0x0FFF0B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.120 SFLASH\_AV\_PAIRS\_8B54

8b Addr/Value pair Section

Address: 0x0FFF0B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.121 SFLASH\_AV\_PAIRS\_8B55

8b Addr/Value pair Section

Address: 0x0FFF0B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.122 SFLASH\_AV\_PAIRS\_8B56

8b Addr/Value pair Section

Address: 0x0FFF0B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.123 SFLASH\_AV\_PAIRS\_8B57

8b Addr/Value pair Section

Address: 0x0FFF0B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.124 SFLASH\_AV\_PAIRS\_8B58

8b Addr/Value pair Section

Address: 0x0FFF0BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.125 SFLASH\_AV\_PAIRS\_8B59

8b Addr/Value pair Section

Address: 0x0FFF0BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.126 SFLASH\_AV\_PAIRS\_8B60

8b Addr/Value pair Section

Address: 0x0FFFF0BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.127 SFLASH\_AV\_PAIRS\_8B61

8b Addr/Value pair Section

Address: 0x0FFFF0BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.128 SFLASH\_AV\_PAIRS\_8B62

8b Addr/Value pair Section

Address: 0x0FFFF0BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.129 SFLASH\_AV\_PAIRS\_8B63

8b Addr/Value pair Section

Address: 0x0FFF0BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.130 SFLASH\_AV\_PAIRS\_8B64

8b Addr/Value pair Section

Address: 0x0FFF0C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.131 SFLASH\_AV\_PAIRS\_8B65

8b Addr/Value pair Section

Address: 0x0FFFF0C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.132 SFLASH\_AV\_PAIRS\_8B66

8b Addr/Value pair Section

Address: 0x0FFF0C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.133 SFLASH\_AV\_PAIRS\_8B67

8b Addr/Value pair Section

Address: 0x0FFF0C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.134 SFLASH\_AV\_PAIRS\_8B68

8b Addr/Value pair Section

Address: 0x0FFF0C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.135 SFLASH\_AV\_PAIRS\_8B69

8b Addr/Value pair Section

Address: 0x0FFF0C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.136 SFLASH\_AV\_PAIRS\_8B70

8b Addr/Value pair Section

Address: 0x0FFF0C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.137 SFLASH\_AV\_PAIRS\_8B71

8b Addr/Value pair Section

Address: 0x0FFF0C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.138 SFLASH\_AV\_PAIRS\_8B72

8b Addr/Value pair Section

Address: 0x0FFF0C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.139 SFLASH\_AV\_PAIRS\_8B73

8b Addr/Value pair Section

Address: 0x0FFF0C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.140 SFLASH\_AV\_PAIRS\_8B74

8b Addr/Value pair Section

Address: 0x0FFFF0CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.141 SFLASH\_AV\_PAIRS\_8B75

8b Addr/Value pair Section

Address: 0x0FFFF0CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.142 SFLASH\_AV\_PAIRS\_8B76

8b Addr/Value pair Section

Address: 0x0FFFF0CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.143 SFLASH\_AV\_PAIRS\_8B77

8b Addr/Value pair Section

Address: 0x0FFFF0CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.144 SFLASH\_AV\_PAIRS\_8B78

8b Addr/Value pair Section

Address: 0x0FFFF0CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.145 SFLASH\_AV\_PAIRS\_8B79

8b Addr/Value pair Section

Address: 0x0FFFF0CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.146 SFLASH\_AV\_PAIRS\_8B80

8b Addr/Value pair Section

Address: 0x0FFFF0D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.147 SFLASH\_AV\_PAIRS\_8B81

8b Addr/Value pair Section

Address: 0x0FFF0D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.148 SFLASH\_AV\_PAIRS\_8B82

8b Addr/Value pair Section

Address: 0x0FFF0D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.149 SFLASH\_AV\_PAIRS\_8B83

8b Addr/Value pair Section

Address: 0x0FFFF0D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.150 SFLASH\_AV\_PAIRS\_8B84

8b Addr/Value pair Section

Address: 0x0FFF0D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.151 SFLASH\_AV\_PAIRS\_8B85

8b Addr/Value pair Section

Address: 0x0FFF0D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.152 SFLASH\_AV\_PAIRS\_8B86

8b Addr/Value pair Section

Address: 0x0FFFF0D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.153 SFLASH\_AV\_PAIRS\_8B87

8b Addr/Value pair Section

Address: 0x0FFF0D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.154 SFLASH\_AV\_PAIRS\_8B88

8b Addr/Value pair Section

Address: 0x0FFFF0D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.155 SFLASH\_BLESS\_BB\_BUMP2

BLESS Bump bit for LDO BB, TXRX

Address: 0x0FFF0D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	V2I [7:5]			V2I_RCAL [4:0]				

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	SY_IBIAS [15:13]			VBG_TRIM [12:10]			V2I [9:8]	

Bits	Name	Description
15 : 13	SY_IBIAS	3'b1xx: RCAL current bumped 3'b0xx: BG current bumped. 2'bx: represent current bump 01: +12.5%, 00: 0%, 11: -12.5%, 10:-25% Default Value: 0
12 : 10	VBG_TRIM	3d0: Trims the Bandgap voltage by 0% 3d1: Trims the Bandgap voltage by 1.6% 3d2: Trims the Bandgap voltage by 3.2% 3d3: Trims the Bandgap voltage by 4.8% 3d4: Trims the Bandgap voltage by 6.4% 3d5: Trims the Bandgap voltage by -4.8% 3d6: Trims the Bandgap voltage by -3.2% 3d7: Trims the Bandgap voltage by -1.6% Default Value: 0

## 21.1.155 SFLASH\_BLESS\_BB\_BUMP2 (continued)

9 : 5	V2I	Bit[9] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u  Bit[8:5] 4d0: Trims the BGR current by 0% 4d1: Trims the BGR current by -2.5% 4d2: Trims the BGR current by -5% 4d3: Trims the BGR current by -7.5% 4d4: Trims the BGR current by -10% 4d5: Trims the BGR current by -12.5% 4d6: Trims the BGR current by -15% 4d7: Trims the BGR current by -17.5% 4d8: Trims the BGR current by 20% 4d9: Trims the BGR current by 17.5% 4d10: Trims the BGR current by 15% 4d11: Trims the BGR current by 12.5% 4d12: Trims the BGR current by 10% 4d13: Trims the BGR current by 7.5% 4d14: Trims the BGR current by 5% 4d15: Trims the BGR current by 2.5% Default Value: 0
4 : 0	V2I_RCAL	Bit[4] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u  Bit[3:0] 4d0: Trims the RCAL current by 0% 4d1: Trims the RCAL current by -2.5% 4d2: Trims the RCAL current by -5% 4d3: Trims the RCAL current by -7.5% 4d4: Trims the RCAL current by -10% Default Value: 0

## 21.1.156 SFLASH\_AV\_PAIRS\_8B89

8b Addr/Value pair Section

Address: 0x0FFF0D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.157 SFLASH\_AV\_PAIRS\_8B90

8b Addr/Value pair Section

Address: 0x0FFFF0DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.158 SFLASH\_BLESS\_BB\_XO

BLESS bump configuration 1

Address: 0x0FFFF0DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	CTRL_VDDL_XO	CTRL_RC_FASTSTART_RES [6:5]		EN_AMPDET_FASTSTART	EN_AMPDET_CURMEAS	EN_CURMEAS	EN_RE_FASTSTART	DIS_XOCORE_SUPPLIANT

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	rev_bb_xo	CTRL_RPREF [14:13]		CTRL_VDDL_XB [12:10]			CTRL_VDDL_XO [9:8]	

Bits	Name	Description
15	rev_bb_xo	reserved for feature Default Value: 0
14 : 13	CTRL_RPREF	Controls the reference voltage fed as input to the regulators which generate vdd_xo and vdd_xb. 2d0 : 1.289V 2d0 : 1.227V 2d0 : 1.164V 2d0 : 1.382V Default Value: 0
12 : 10	CTRL_VDDL_XB	Controls the value of supply filter resistance in the inverter chain. This in turn controls the supply voltage at which the inverter chain runs. 3d0 : 1.028k 3d0 : 1.172k 3d0 : 1.367k 3d0 : 1.540k 3d0 : 1.889k 3d0 : 2.055k 3d0 : 0.503k 3d0 : 0.747k Default Value: 0
9 : 7	CTRL_VDDL_XO	Controls the value of supply filter resistance in the xo core. This in turn controls the supply voltage at which the core runs. 3d0 : 0.769k 3d0 : 0.877k 3d0 : 1.023k 3d0 : 1.152k 3d0 : 1.413k 3d0 : 1.537k 3d0 : 0.376k 3d0 : 0.559k Default Value: 0

### 21.1.158 SFLASH\_BLESS\_BB\_XO (continued)

6 : 5	CTRL_RC_FASTSTART_RES	Controls the time constant with which the surge current from rc_faststart block decays down to zero. 2d0 : 387us 2d1 : 309us 2d2 : 232us 2d3 : 464us Default Value: 0
4	EN_AMPDET_FASTSTART	This bit is used to force startup of the vtnbyr circuit in the biasgen_and_reg block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
3	EN_AMPDET_CURMEAS	This bit can be used to disable all the caps on both X1 node and X2 node. 1d0 : Caps Enabled 1d1 : Caps disabled. Even when all the caps are disabled, due to finite on/off ratio of the caps, the cap on both X1 and X2 node is still 3.69pF Default Value: 0
2	EN_CURMEAS	This bit is used to force startup of the positive feedback loop in the amplitude detect block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
1	EN_RE_FASTSTART	Enables/Disables the RC faststart block in the XO. When enabled, this block provides a surge current at xo startup to reduce the settling time of the XO. 1: RC Fast start in XO is enabled 0: RC Fast start in XO is disabled Default Value: 0
0	DIS_XOCORE_SUPFILT	Enables/Disables the supply filter of the XO core. 1: Disabled 0: Enabled Default Value: 0

## 21.1.159 SFLASH\_AV\_PAIRS\_8B91

8b Addr/Value pair Section

Address: 0x0FFFF0DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.160 SFLASH\_AV\_PAIRS\_8B92

8b Addr/Value pair Section

Address: 0x0FFFF0DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.161 SFLASH\_BLESS\_SY\_BUMP1

BLESS SY bump bits configuration 1

Address: 0x0FFFF0DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW			
HW Access	R	R		R	R			
Name	LDOLO_FORCE_STARTUP	IBIAS_LOPATH [6:5]		LOFB_POWER_SAVE	VCO [3:0]			

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDCPLPF [15:12]				LOPATH [11:8]			

Bits	Name	Description																		
15 : 12	PDCPLPF	<p>Bump for PD CP and LPF blocks.[2:0] is used to get range of -20%to +15% in 5% steps.</p> <table><tr><th>ICP_BUMP[2:0]</th><th>ICP</th></tr><tr><td>1 0 0</td><td>-20%</td></tr><tr><td>1 0 1</td><td>-15%</td></tr><tr><td>1 1 0</td><td>-10%</td></tr><tr><td>1 1 1</td><td>-05%</td></tr><tr><td>0 0 0</td><td>00%</td></tr><tr><td>0 0 1</td><td>05%</td></tr><tr><td>0 1 0</td><td>10%</td></tr><tr><td>0 1 1</td><td>15%.</td></tr></table> <p>Default Value: 0</p>	ICP_BUMP[2:0]	ICP	1 0 0	-20%	1 0 1	-15%	1 1 0	-10%	1 1 1	-05%	0 0 0	00%	0 0 1	05%	0 1 0	10%	0 1 1	15%.
ICP_BUMP[2:0]	ICP																			
1 0 0	-20%																			
1 0 1	-15%																			
1 1 0	-10%																			
1 1 1	-05%																			
0 0 0	00%																			
0 0 1	05%																			
0 1 0	10%																			
0 1 1	15%.																			
11 : 8	LOPATH	<p>Bump bits for LO path bulk bias. Goes to DIVN/FCAL/LOPATH for bumps. 2 bits for pBulk [3:2] and 2 bits for nBulk[1:0].</p> <table><tr><th>bump</th><th>pbulk</th></tr><tr><td>0 0</td><td>vddx-380mV</td></tr><tr><td>0 1</td><td>vddx-320mV</td></tr><tr><td>1 0</td><td>vddx-440mV</td></tr><tr><td>1 1</td><td>vddx</td></tr></table> <p>Default Value: 5</p>	bump	pbulk	0 0	vddx-380mV	0 1	vddx-320mV	1 0	vddx-440mV	1 1	vddx								
bump	pbulk																			
0 0	vddx-380mV																			
0 1	vddx-320mV																			
1 0	vddx-440mV																			
1 1	vddx																			
7	LDOLO_FORCE_STARTUP	<p>1: force start-up of the VT/R circuit in VCOLOPATH LCO</p> <p>0: no force start-up</p> <p>Default Value: 0</p>																		
6 : 5	IBIAS_LOPATH	<p>bump bits for clkbias in lopath</p> <table><tr><th>bump</th><th>clk bias pM</th><th>clk bias nM</th></tr><tr><td>0 0</td><td>vddo-vgsp</td><td>vgasn</td></tr><tr><td>0 1</td><td>vddlo-vgsp-100m</td><td>vgasn+100m</td></tr><tr><td>1 0</td><td>vddlo-vgsp-200m</td><td>vgasn+200m</td></tr><tr><td>1 1</td><td>vddlo-vgsp-400m</td><td>vgasn+400m</td></tr></table> <p>Default Value: 0</p>	bump	clk bias pM	clk bias nM	0 0	vddo-vgsp	vgasn	0 1	vddlo-vgsp-100m	vgasn+100m	1 0	vddlo-vgsp-200m	vgasn+200m	1 1	vddlo-vgsp-400m	vgasn+400m			
bump	clk bias pM	clk bias nM																		
0 0	vddo-vgsp	vgasn																		
0 1	vddlo-vgsp-100m	vgasn+100m																		
1 0	vddlo-vgsp-200m	vgasn+200m																		
1 1	vddlo-vgsp-400m	vgasn+400m																		

### 21.1.161 SFLASH\_BLESS\_SY\_BUMP1 (continued)

4	LOFB_POWERSAVE	1: enable powersave for LOFB buffer 0: disable powersave for LOFB buffer Default Value: 0
3 : 0	VCO	Bump bits for SY VCO block. Rt VCO (2 bits) - sy_bump1_vco [3:2] 00 ~ 50 Ohms 01 ~ 30 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms and Rb VCO (2 bits) - sy_bump1_vco[1:0] 00 ~ 58 Ohms 01 ~ 39 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms Default Value: 5

## 21.1.162 SFLASH\_AV\_PAIRS\_8B93

8b Addr/Value pair Section

Address: 0x0FFFF0DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.163 SFLASH\_AV\_PAIRS\_8B94

8b Addr/Value pair Section

Address: 0x0FFFF0DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.164 SFLASH\_BLESS\_LDO

BLESS bump bit for LDO

Address: 0x0FFFF0DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW		RW		
HW Access	R	R		R		R		
Name	BUMP_SY_LHV	BUMP_SY_LOPATH [6:5]		BUMP_SY_VCO [4:3]		BUMP_BALUM_HF [2:0]		

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			RW
HW Access	R				R			R
Name	REV_LDO [15:12]				BUMP_SY_FFFB [11:9]			BUMP_SY_LHV

Bits	Name	Description
15 : 12	REV_LDO	received for feature Default Value: 0
11 : 9	BUMP_SY_FFFB	3d0: FF and FB LDO outputs are 1.800V 3d1: FF and FB LDO outputs are 1.846V 3d2: FF and FB LDO outputs are 1.894V 3d3: FF and FB LDO outputs are 1.946V 3d4: FF and FB LDO outputs are 2.000V 3d5: FF and FB LDO outputs are 1.649V 3d6: FF and FB LDO outputs are 1.701V 3d7: FF and FB LDO outputs are 1.756V Default Value: 0
8 : 7	BUMP_SY_LHV	2d0: HV LDO outputs are 1.894V 2d1: HV LDO outputs are 2.000V 2d2: HV LDO outputs are 1.800V 2d3: HV LDO outputs are 1.846V Default Value: 0
6 : 5	BUMP_SY_LOPATH	2d0: LOPATH LDO outputs are 1.762V 2d1: LOPATH LDO outputs are 1.861V 2d2: LOPATH LDO outputs are 1.673V 2d3: LOPATH LDO outputs are 1.716V Default Value: 0
4 : 3	BUMP_SY_VCO	2d0: VCO LDO outputs are 1.413V 2d1: VCO LDO outputs are 1.494V 2d2: VCO LDO outputs are 1.329V 2d3: VCO LDO outputs are 1.371V Default Value: 0

### 21.1.164 SFLASH\_BLESS\_LDO (continued)

2 : 0	BUMP_BALUM_HF	3d0: HF LDO output is 1.800V 3d1: HF LDO output is 1.846V 3d2: HF LDO output is 1.894V 3d3: HF LDO output is 1.946V Default Value: 0
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## 21.1.165 SFLASH\_AV\_PAIRS\_8B95

8b Addr/Value pair Section

Address: 0x0FFFF0DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.166 SFLASH\_AV\_PAIRS\_8B96

8b Addr/Value pair Section

Address: 0x0FFF0E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.167 SFLASH\_AV\_PAIRS\_8B97

8b Addr/Value pair Section

Address: 0x0FFF0E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.168 SFLASH\_AV\_PAIRS\_8B98

8b Addr/Value pair Section

Address: 0x0FFF0E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.169 SFLASH\_AV\_PAIRS\_8B99

8b Addr/Value pair Section

Address: 0x0FFF0E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.170 SFLASH\_AV\_PAIRS\_8B100

8b Addr/Value pair Section

Address: 0x0FFF0E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.171 SFLASH\_AV\_PAIRS\_8B101

8b Addr/Value pair Section

Address: 0x0FFF0E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.172 SFLASH\_AV\_PAIRS\_8B102

8b Addr/Value pair Section

Address: 0x0FFF0E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.173 SFLASH\_AV\_PAIRS\_8B103

8b Addr/Value pair Section

Address: 0x0FFF0E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.174 SFLASH\_AV\_PAIRS\_8B104

8b Addr/Value pair Section

Address: 0x0FFF0E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.175 SFLASH\_AV\_PAIRS\_8B105

8b Addr/Value pair Section

Address: 0x0FFF0E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.176 SFLASH\_AV\_PAIRS\_8B106

8b Addr/Value pair Section

Address: 0x0FFFF0EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.177 SFLASH\_AV\_PAIRS\_8B107

8b Addr/Value pair Section

Address: 0x0FFFF0EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.178 SFLASH\_AV\_PAIRS\_8B108

8b Addr/Value pair Section

Address: 0x0FFFF0EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.179 SFLASH\_AV\_PAIRS\_8B109

8b Addr/Value pair Section

Address: 0x0FFFF0ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.180 SFLASH\_AV\_PAIRS\_8B110

8b Addr/Value pair Section

Address: 0x0FFFF0EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.181 SFLASH\_AV\_PAIRS\_8B111

8b Addr/Value pair Section

Address: 0x0FFF0EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.182 SFLASH\_AV\_PAIRS\_8B112

8b Addr/Value pair Section

Address: 0x0FFF0F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.183 SFLASH\_AV\_PAIRS\_8B113

8b Addr/Value pair Section

Address: 0x0FFF0F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.184 SFLASH\_AV\_PAIRS\_8B114

8b Addr/Value pair Section

Address: 0x0FFF0F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.185 SFLASH\_AV\_PAIRS\_8B115

8b Addr/Value pair Section

Address: 0x0FFF0F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.186 SFLASH\_AV\_PAIRS\_8B116

8b Addr/Value pair Section

Address: 0x0FFF0F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.187 SFLASH\_AV\_PAIRS\_8B117

8b Addr/Value pair Section

Address: 0x0FFF0F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.188 SFLASH\_AV\_PAIRS\_8B118

8b Addr/Value pair Section

Address: 0x0FFF0F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.189 SFLASH\_AV\_PAIRS\_8B119

8b Addr/Value pair Section

Address: 0x0FFF0F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.190 SFLASH\_AV\_PAIRS\_8B120

8b Addr/Value pair Section

Address: 0x0FFF0F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 21.1.191 SFLASH\_AV\_PAIRS\_8B121

8b Addr/Value pair Section

Address: 0x0FFF0F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.192 SFLASH\_AV\_PAIRS\_8B122

8b Addr/Value pair Section

Address: 0x0FFF0FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.193 SFLASH\_AV\_PAIRS\_8B123

8b Addr/Value pair Section

Address: 0x0FFF0FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.194 SFLASH\_AV\_PAIRS\_8B124

8b Addr/Value pair Section

Address: 0x0FFFF0FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.195 SFLASH\_AV\_PAIRS\_8B125

8b Addr/Value pair Section

Address: 0x0FFFF0FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.196 SFLASH\_AV\_PAIRS\_8B126

8b Addr/Value pair Section

Address: 0x0FFF0FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.197 SFLASH\_AV\_PAIRS\_8B127

8b Addr/Value pair Section

Address: 0x0FFFF0FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 21.1.198 SFLASH\_AV\_PAIRS\_32B0

32b Addr/Value pair Section

Address: 0x0FFF100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X



## 21.1.199 SFLASH\_AV\_PAIRS\_32B1

32b Addr/Value pair Section

Address: 0x0FFF104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.200 SFLASH\_AV\_PAIRS\_32B2

32b Addr/Value pair Section

Address: 0x0FFF108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.201 SFLASH\_AV\_PAIRS\_32B3

32b Addr/Value pair Section

Address: 0x0FFFF10C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.202 SFLASH\_AV\_PAIRS\_32B4

32b Addr/Value pair Section

Address: 0x0FFFF110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.203 SFLASH\_AV\_PAIRS\_32B5

32b Addr/Value pair Section

Address: 0x0FFF114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.204 SFLASH\_AV\_PAIRS\_32B6

32b Addr/Value pair Section

Address: 0x0FFF118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.205 SFLASH\_AV\_PAIRS\_32B7

32b Addr/Value pair Section

Address: 0x0FFFF11C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.206 SFLASH\_AV\_PAIRS\_32B8

32b Addr/Value pair Section

Address: 0x0FFF120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X



## 21.1.207 SFLASH\_AV\_PAIRS\_32B9

32b Addr/Value pair Section

Address: 0x0FFF124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.208 SFLASH\_AV\_PAIRS\_32B10

32b Addr/Value pair Section

Address: 0x0FFF128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.209 SFLASH\_AV\_PAIRS\_32B11

32b Addr/Value pair Section

Address: 0x0FFFF12C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.210 SFLASH\_AV\_PAIRS\_32B12

32b Addr/Value pair Section

Address: 0x0FFF130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.211 SFLASH\_AV\_PAIRS\_32B13

32b Addr/Value pair Section

Address: 0x0FFF134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.212 SFLASH\_AV\_PAIRS\_32B14

32b Addr/Value pair Section

Address: 0x0FFF138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.213 SFLASH\_AV\_PAIRS\_32B15

32b Addr/Value pair Section

Address: 0x0FFFF13C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 21.1.214 SFLASH\_CPUSW\_WOUNDING

CPUSW Wounding Register

Address: 0x0FFF140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Data to use for register Default Value: X



## 21.1.215 SFLASH\_SILICON\_ID

Silicon ID

Address: 0x0FFFF144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

## 21.1.216 SFLASH\_CPUSS\_PRIV\_RAM

RAM Privileged Limit

Address: 0x0FFF148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RAM_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RAM_PROT_LIMIT

Bits	Name	Description
8 : 0	RAM_PROT_LIMIT	<p>Indicates the limit where the privileged area of SRAM starts in increments of 256 Bytes.</p> <p>"0": Entire SRAM is Privileged.</p> <p>"1": First 256 Bytes are User accessible.</p> <p>Any number larger than the size of the SRAM indicates that the entire SRAM is user mode accessible.</p> <p>Default Value: 0</p>

## 21.1.217 SFLASH\_CPUSS\_PRIV\_ROM\_BROM

Boot ROM Privileged Limit

Address: 0x0FFF14A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BROM_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 0	BROM_PROT_LIMIT	<p>Indicates the limit where the privileged area of the Boot ROM partition starts in increments of 256 Bytes.</p> <p>"0": Entire Boot ROM is Privileged.</p> <p>"1": First 256 Bytes are User accessible.</p> <p>...</p> <p>BROM_PROT_LIMIT &gt;= "Boot ROM partition capacity": Entire Boot ROM partition is user mode accessible.</p> <p>Default Value: 0</p>

## 21.1.218 SFLASH\_CPUSS\_PRIV\_FLASH

Flash Privileged Limit

Address: 0x0FFFF14C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLASH_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					FLASH_PROT_LIMIT [10:8]		

Bits	Name	Description
10 : 0	FLASH_PROT_LIMIT	<p>Indicates the limit where the privileged area of flash starts in increments of 256 Bytes.</p> <p>"0": Entire flash is Privileged.</p> <p>"1": First 256 Bytes are User accessible.</p> <p>Any number larger than the size of the flash indicates that the entire flash is user mode accessible. Note that SuperVisory rows are always User accessible.</p> <p>If FLASH_PROT_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using SYSREQ.</p> <p>Default Value: 0</p>

## 21.1.219 SFLASH\_CPUSS\_PRIV\_ROM\_SROM

System ROM Privileged Limit

Address: 0x0FFFF14E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SROM_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SROM_PROT_LIMIT [9:8]	

Bits	Name	Description
9 : 0	SROM_PROT_LIMIT	<p>Indicates the limit where the privileged area of System ROM partition starts in increments of 256 Bytes. The limit is wrt. the start of the ROM memory (start of the Boot ROM partition).</p> <p>SROM_PROT_LIMIT * 256 Byte &lt;= "Boot ROM partition capacity": Entire System ROM is Privileged.</p> <p>SROM_PROT_LIMIT * 256 Byte &gt; "Boot ROM partition capacity": First SROM_PROT_LIMIT * 256 - "Boot ROM partition capacity" Bytes are User accessible.</p> <p>...</p> <p>SROM_PROT_LIMIT &gt;= "ROM capacity": Entire System ROM is user mode accessible.</p> <p>Default Value: 0</p>

## 21.1.220 SFLASH\_HIB\_KEY\_DELAY

Hibernate wakeup value for PWR\_KEY\_DELAY

Address: 0x0FFF150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

## 21.1.221 SFLASH\_DPSLP\_KEY\_DELAY

DeepSleep wakeup value for PWR\_KEY\_DELAY

Address: 0x0FFF152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

## 21.1.222 SFLASH\_SWD\_CONFIG

SWD pinout selector (not present in TSG4/TSG5-M)

Address: 0x0FFF154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							None
Name	None [7:1]							SWD_SELECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X



## 21.1.223 SFLASH\_INITIAL\_SPCIF\_TRIM\_M1\_DAC0

FLASH IDAC trim used during boot

Address: 0x0FFF155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	SLOPE [7:5]			IDAC [4:0]				

Bits	Name	Description
7 : 5	SLOPE	See SPCIF_TRIM1 Default Value: 0
4 : 0	IDAC	See SPCIF_TRIM1 Default Value: 0

## 21.1.224 SFLASH\_SWD\_LISTEN

Listen Window Length

Address: 0x0FFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

## 21.1.225 SFLASH\_FLASH\_START

Flash Image Start Address

Address: 0x0FFFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ADDRESS [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ADDRESS [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	ADDRESS [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

## 21.1.226 SFLASH\_CSD\_TRIM1\_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

## 21.1.227 SFLASH\_CSD\_TRIM2\_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFF161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

## 21.1.228 SFLASH\_CSD\_TRIM1\_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFF162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

## 21.1.229 SFLASH\_CSD\_TRIM2\_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFF163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

## 21.1.230 SFLASH\_SAR\_TEMP\_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFF164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X



## 21.1.231 SFLASH\_SAR\_TEMP\_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFF166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

## 21.1.232 SFLASH\_SKIP\_CHECKSUM

Checksum Skip Option Register

Address: 0x0FFF169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SKIP [7:0]							

Bits	Name	Description
7 : 0	SKIP	0: Perform checksum check (see CHECKSUM field below) 1: Skip checksum check >1: Undefined - do not use Default Value: X

## 21.1.233 SFLASH\_PROT\_VIRGINKEY0

Virgin Protection Mode Key

Address: 0x0FFF170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 21.1.234 SFLASH\_PROT\_VIRGINKEY1

Virgin Protection Mode Key

Address: 0x0FFF171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 21.1.235 SFLASH\_PROT\_VIRGINKEY2

Virgin Protection Mode Key

Address: 0x0FFF172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 21.1.236 SFLASH\_PROT\_VIRGINKEY3

Virgin Protection Mode Key

Address: 0x0FFF173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 21.1.237 SFLASH\_PROT\_VIRGINKEY4

Virgin Protection Mode Key

Address: 0x0FFF174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 21.1.238 SFLASH\_PROT\_VIRGINKEY5

Virgin Protection Mode Key

Address: 0x0FFF175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X



## 21.1.239 SFLASH\_PROT\_VIRGINKEY6

Virgin Protection Mode Key

Address: 0x0FFF176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 21.1.240 SFLASH\_PROT\_VIRGINKEY7

Virgin Protection Mode Key

Address: 0x0FFF177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 21.1.241 SFLASH\_DIE\_LOT0

Lot Number (3 bytes)

Address: 0x0FFF178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

## 21.1.242 SFLASH\_DIE\_LOT1

Lot Number (3 bytes)

Address: 0x0FFF179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

## 21.1.243 SFLASH\_DIE\_LOT2

Lot Number (3 bytes)

Address: 0x0FFF17A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

## 21.1.244 SFLASH\_DIE\_WAFER

Wafer Number

Address: 0x0FFF17B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	WAFER [7:0]							

Bits	Name	Description
7 : 0	WAFER	Wafer Number Default Value: X

## 21.1.245 SFLASH\_DIE\_X

X Position on Wafer, CRI Pass/Fail Bin

Address: 0x0FFF17C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	X [7:0]							

Bits	Name	Description
7 : 0	X	X Position Default Value: X

## 21.1.246 SFLASH\_DIE\_Y

Y Position on Wafer, CHI Pass/Fail Bin

Address: 0x0FFF17D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	Y [7:0]							

Bits	Name	Description
7 : 0	Y	Y Position Default Value: X



## 21.1.247 SFLASH\_DIE\_SORT

Sort1/2/3 Pass/Fail Bin

Address: 0x0FFF17E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		None	None	None	None	None	None
Name	None [7:6]		ENG_PASS	CHI_PASS	CRI_PASS	S3_PASS	S2_PASS	S1_PASS

Bits	Name	Description
5	ENG_PASS	ENG Pass Bin Default Value: X
4	CHI_PASS	CHI Pass Bin (1) or 0 (Fail Bin) Default Value: X
3	CRI_PASS	CRI Pass Bin (1) or 0 (Fail Bin) Default Value: X
2	S3_PASS	SORT3 Pass Bin (1) or 0 (Fail Bin) Default Value: X
1	S2_PASS	SORT2 Pass Bin (1) or 0 (Fail Bin) Default Value: X
0	S1_PASS	SORT1 Pass Bin (1) or 0 (Fail Bin) Default Value: X

## 21.1.248 SFLASH\_DIE\_MINOR

Minor Revision Number

Address: 0x0FFFF17F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Minor revision number Default Value: X

## 21.1.249 SFLASH\_PE\_TE\_DATA0

PE/TE Data

Address: 0x0FFF180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.250 SFLASH\_PE\_TE\_DATA1

PE/TE Data

Address: 0x0FFF181

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.251 SFLASH\_PE\_TE\_DATA2

PE/TE Data

Address: 0x0FFF182

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.252 SFLASH\_PE\_TE\_DATA3

PE/TE Data

Address: 0x0FFF183

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.253 SFLASH\_PE\_TE\_DATA4

PE/TE Data

Address: 0x0FFF184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.254 SFLASH\_PE\_TE\_DATA5

PE/TE Data

Address: 0x0FFF185

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 21.1.255 SFLASH\_PE\_TE\_DATA6

PE/TE Data

Address: 0x0FFF186

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.256 SFLASH\_PE\_TE\_DATA7

PE/TE Data

Address: 0x0FFF187

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.257 SFLASH\_PE\_TE\_DATA8

PE/TE Data

Address: 0x0FFF188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.258 SFLASH\_PE\_TE\_DATA9

PE/TE Data

Address: 0x0FFF189

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.259 SFLASH\_PE\_TE\_DATA10

PE/TE Data

Address: 0x0FFF18A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.260 SFLASH\_PE\_TE\_DATA11

PE/TE Data

Address: 0x0FFF18B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.261 SFLASH\_PE\_TE\_DATA12

PE/TE Data

Address: 0x0FFF18C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.262 SFLASH\_PE\_TE\_DATA13

PE/TE Data

Address: 0x0FFF18D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 21.1.263 SFLASH\_PE\_TE\_DATA14

PE/TE Data

Address: 0x0FFF18E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.264 SFLASH\_PE\_TE\_DATA15

PE/TE Data

Address: 0x0FFF18F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.265 SFLASH\_PE\_TE\_DATA16

PE/TE Data

Address: 0x0FFF190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.266 SFLASH\_PE\_TE\_DATA17

PE/TE Data

Address: 0x0FFF191

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.267 SFLASH\_PE\_TE\_DATA18

PE/TE Data

Address: 0x0FFF192

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.268 SFLASH\_PE\_TE\_DATA19

PE/TE Data

Address: 0x0FFF193

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.269 SFLASH\_PE\_TE\_DATA20

PE/TE Data

Address: 0x0FFF194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.270 SFLASH\_PE\_TE\_DATA21

PE/TE Data

Address: 0x0FFF195

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 21.1.271 SFLASH\_PE\_TE\_DATA22

PE/TE Data

Address: 0x0FFF196

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.272 SFLASH\_PE\_TE\_DATA23

PE/TE Data

Address: 0x0FFF197

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.273 SFLASH\_PE\_TE\_DATA24

PE/TE Data

Address: 0x0FFF198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.274 SFLASH\_PE\_TE\_DATA25

PE/TE Data

Address: 0x0FFF199

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.275 SFLASH\_PE\_TE\_DATA26

PE/TE Data

Address: 0x0FFF19A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.276 SFLASH\_PE\_TE\_DATA27

PE/TE Data

Address: 0x0FFF19B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.277 SFLASH\_PE\_TE\_DATA28

PE/TE Data

Address: 0x0FFF19C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.278 SFLASH\_PE\_TE\_DATA29

PE/TE Data

Address: 0x0FFF19D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 21.1.279 SFLASH\_PE\_TE\_DATA30

PE/TE Data

Address: 0x0FFF19E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.280 SFLASH\_PE\_TE\_DATA31

PE/TE Data

Address: 0x0FFF19F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 21.1.281 SFLASH\_PP

Preprogram Settings

Address: 0x0FFF1A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.282 SFLASH\_E

Erase Settings

Address: 0x0FFF1A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.283 SFLASH\_P

Program Settings

Address: 0x0FFF1A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.284 SFLASH\_EA\_E

Erase All - Erase Settings

Address: 0x0FFFF1AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.285 SFLASH\_EA\_P

Erase All - Program Settings

Address: 0x0FFFF1B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.286 SFLASH\_ES\_E

Erase Sector - Erase Settings

Address: 0x0FFF1B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X



## 21.1.287 SFLASH\_ES\_P\_EO

Erase Sector - Program EO Settings

Address: 0x0FFF1B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.288 SFLASH\_E\_VCTAT

Bandgap Trim Register

Address: 0x0FFFF1BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_EN ABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

## 21.1.289 SFLASH\_P\_VCTAT

Bandgap Trim Register

Address: 0x0FFFF1BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

## 21.1.290 SFLASH\_IMO\_MAXF0

Max frequency for trim pair

Address: 0x0FFFF1C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

## 21.1.291 SFLASH\_IMO\_ABS0

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

## 21.1.292 SFLASH\_IMO\_TMPCO0

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 21.1.293 SFLASH\_IMO\_MAXF1

Max frequency for trim pair

Address: 0x0FFFF1C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

## 21.1.294 SFLASH\_IMO\_ABS1

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFF1C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X



## 21.1.295 SFLASH\_IMO\_TMPCO1

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 21.1.296 SFLASH\_IMO\_MAXF2

Max frequency for trim pair

Address: 0x0FFFF1C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

## 21.1.297 SFLASH\_IMO\_ABS2

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFF1C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

## 21.1.298 SFLASH\_IMO\_TMPCO2

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 21.1.299 SFLASH\_IMO\_MAXF3

Max frequency for trim pair

Address: 0x0FFFF1C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

## 21.1.300 SFLASH\_IMO\_ABS3

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

## 21.1.301 SFLASH\_IMO\_TMPCO3

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 21.1.302 SFLASH\_IMO\_ABS4

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X



## 21.1.303 SFLASH\_IMO\_TMPCO4

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 21.1.304 SFLASH\_IMO\_TRIM0

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.305 SFLASH\_IMO\_TRIM1

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.306 SFLASH\_IMO\_TRIM2

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.307 SFLASH\_IMO\_TRIM3

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.308 SFLASH\_IMO\_TRIM4

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.309 SFLASH\_IMO\_TRIM5

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.310 SFLASH\_IMO\_TRIM6

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 21.1.311 SFLASH\_IMO\_TRIM7

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.312 SFLASH\_IMO\_TRIM8

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.313 SFLASH\_IMO\_TRIM9

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.314 SFLASH\_IMO\_TRIM10

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.315 SFLASH\_IMO\_TRIM11

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.316 SFLASH\_IMO\_TRIM12

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.317 SFLASH\_IMO\_TRIM13

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.318 SFLASH\_IMO\_TRIM14

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 21.1.319 SFLASH\_IMO\_TRIM15

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.320 SFLASH\_IMO\_TRIM16

IMO Trim Register (SRSSv2)

Address: 0x0FFF1E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.321 SFLASH\_IMO\_TRIM17

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.322 SFLASH\_IMO\_TRIM18

IMO Trim Register (SRSSv2)

Address: 0x0FFF1E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.323 SFLASH\_IMO\_TRIM19

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.324 SFLASH\_IMO\_TRIM20

IMO Trim Register (SRSSv2)

Address: 0x0FFF1E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.325 SFLASH\_IMO\_TRIM21

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.326 SFLASH\_IMO\_TRIM22

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 21.1.327 SFLASH\_IMO\_TRIM23

IMO Trim Register (SRSSv2)

Address: 0x0FFF1E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.328 SFLASH\_IMO\_TRIM24

IMO Trim Register (SRSSv2)

Address: 0x0FFF1E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.329 SFLASH\_IMO\_TRIM25

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.330 SFLASH\_IMO\_TRIM26

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.331 SFLASH\_IMO\_TRIM27

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.332 SFLASH\_IMO\_TRIM28

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.333 SFLASH\_IMO\_TRIM29

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.334 SFLASH\_IMO\_TRIM30

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 21.1.335 SFLASH\_IMO\_TRIM31

IMO Trim Register (SRSSv2)

Address: 0x0FFF1EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.336 SFLASH\_IMO\_TRIM32

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.337 SFLASH\_IMO\_TRIM33

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.338 SFLASH\_IMO\_TRIM34

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.339 SFLASH\_IMO\_TRIM35

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.340 SFLASH\_IMO\_TRIM36

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.341 SFLASH\_IMO\_TRIM37

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.342 SFLASH\_IMO\_TRIM38

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 21.1.343 SFLASH\_IMO\_TRIM39

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.344 SFLASH\_IMO\_TRIM40

IMO Trim Register (SRSSv2)

Address: 0x0FFF1F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.345 SFLASH\_IMO\_TRIM41

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.346 SFLASH\_IMO\_TRIM42

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.347 SFLASH\_IMO\_TRIM43

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.348 SFLASH\_IMO\_TRIM44

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.349 SFLASH\_IMO\_TRIM45

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 21.1.350 SFLASH\_CHECKSUM

Boot Checksum

Address: 0x0FFFF1FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CHECKSUM [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CHECKSUM [15:8]							

Bits	Name	Description
15 : 0	CHECKSUM	Checksum of fixed data checked during boot. This checksum covers all of rows 1,2,3 of macro 0 + row 3 of macro 1 (except this checksum, and row 3 of macro 1 only if it exists). Default Value: X



## 21.1.351 SFLASH\_MACRO\_0\_FREE\_SFLASH0

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.352 SFLASH\_MACRO\_0\_FREE\_SFLASH1

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF201

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.353 SFLASH\_MACRO\_0\_FREE\_SFLASH2

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF202

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.354 SFLASH\_MACRO\_0\_FREE\_SFLASH3

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF203

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.355 SFLASH\_MACRO\_0\_FREE\_SFLASH4

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.356 SFLASH\_MACRO\_0\_FREE\_SFLASH5

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF205

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.357 SFLASH\_MACRO\_0\_FREE\_SFLASH6

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF206

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.358 SFLASH\_MACRO\_0\_FREE\_SFLASH7

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF207

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.359 SFLASH\_MACRO\_0\_FREE\_SFLASH8

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.360 SFLASH\_MACRO\_0\_FREE\_SFLASH9

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF209

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.361 SFLASH\_MACRO\_0\_FREE\_SFLASH10

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF20A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.362 SFLASH\_MACRO\_0\_FREE\_SFLASH11

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF20B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.363 SFLASH\_MACRO\_0\_FREE\_SFLASH12

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF20C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.364 SFLASH\_MACRO\_0\_FREE\_SFLASH13

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF20D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.365 SFLASH\_MACRO\_0\_FREE\_SFLASH14

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF20E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.366 SFLASH\_MACRO\_0\_FREE\_SFLASH15

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF20F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.367 SFLASH\_MACRO\_0\_FREE\_SFLASH16

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.368 SFLASH\_MACRO\_0\_FREE\_SFLASH17

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF211

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.369 SFLASH\_MACRO\_0\_FREE\_SFLASH18

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF212

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.370 SFLASH\_MACRO\_0\_FREE\_SFLASH19

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF213

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.371 SFLASH\_MACRO\_0\_FREE\_SFLASH20

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.372 SFLASH\_MACRO\_0\_FREE\_SFLASH21

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF215

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.373 SFLASH\_MACRO\_0\_FREE\_SFLASH22

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF216

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.374 SFLASH\_MACRO\_0\_FREE\_SFLASH23

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF217

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.375 SFLASH\_MACRO\_0\_FREE\_SFLASH24

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.376 SFLASH\_MACRO\_0\_FREE\_SFLASH25

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF219

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.377 SFLASH\_MACRO\_0\_FREE\_SFLASH26

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF21A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.378 SFLASH\_MACRO\_0\_FREE\_SFLASH27

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF21B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.379 SFLASH\_MACRO\_0\_FREE\_SFLASH28

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.380 SFLASH\_MACRO\_0\_FREE\_SFLASH29

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.381 SFLASH\_MACRO\_0\_FREE\_SFLASH30

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF21E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.382 SFLASH\_MACRO\_0\_FREE\_SFLASH31

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF21F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.383 SFLASH\_MACRO\_0\_FREE\_SFLASH32

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.384 SFLASH\_MACRO\_0\_FREE\_SFLASH33

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF221

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.385 SFLASH\_MACRO\_0\_FREE\_SFLASH34

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF222

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.386 SFLASH\_MACRO\_0\_FREE\_SFLASH35

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF223

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.387 SFLASH\_MACRO\_0\_FREE\_SFLASH36

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.388 SFLASH\_MACRO\_0\_FREE\_SFLASH37

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF225

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.389 SFLASH\_MACRO\_0\_FREE\_SFLASH38

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF226

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.390 SFLASH\_MACRO\_0\_FREE\_SFLASH39

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF227

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.391 SFLASH\_MACRO\_0\_FREE\_SFLASH40

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.392 SFLASH\_MACRO\_0\_FREE\_SFLASH41

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF229

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.393 SFLASH\_MACRO\_0\_FREE\_SFLASH42

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF22A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.394 SFLASH\_MACRO\_0\_FREE\_SFLASH43

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF22B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.395 SFLASH\_MACRO\_0\_FREE\_SFLASH44

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF22C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.396 SFLASH\_MACRO\_0\_FREE\_SFLASH45

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF22D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.397 SFLASH\_MACRO\_0\_FREE\_SFLASH46

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF22E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.398 SFLASH\_MACRO\_0\_FREE\_SFLASH47

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF22F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.399 SFLASH\_MACRO\_0\_FREE\_SFLASH48

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.400 SFLASH\_MACRO\_0\_FREE\_SFLASH49

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF231

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.401 SFLASH\_MACRO\_0\_FREE\_SFLASH50

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF232

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.402 SFLASH\_MACRO\_0\_FREE\_SFLASH51

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF233

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.403 SFLASH\_MACRO\_0\_FREE\_SFLASH52

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.404 SFLASH\_MACRO\_0\_FREE\_SFLASH53

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF235

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.405 SFLASH\_MACRO\_0\_FREE\_SFLASH54

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF236

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.406 SFLASH\_MACRO\_0\_FREE\_SFLASH55

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF237

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.407 SFLASH\_MACRO\_0\_FREE\_SFLASH56

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.408 SFLASH\_MACRO\_0\_FREE\_SFLASH57

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF239

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.409 SFLASH\_MACRO\_0\_FREE\_SFLASH58

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF23A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.410 SFLASH\_MACRO\_0\_FREE\_SFLASH59

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF23B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.411 SFLASH\_MACRO\_0\_FREE\_SFLASH60

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF23C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.412 SFLASH\_MACRO\_0\_FREE\_SFLASH61

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF23D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.413 SFLASH\_MACRO\_0\_FREE\_SFLASH62

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF23E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.414 SFLASH\_MACRO\_0\_FREE\_SFLASH63

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF23F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.415 SFLASH\_MACRO\_0\_FREE\_SFLASH64

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.416 SFLASH\_MACRO\_0\_FREE\_SFLASH65

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF241

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.417 SFLASH\_MACRO\_0\_FREE\_SFLASH66

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF242

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.418 SFLASH\_MACRO\_0\_FREE\_SFLASH67

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF243

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.419 SFLASH\_MACRO\_0\_FREE\_SFLASH68

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.420 SFLASH\_MACRO\_0\_FREE\_SFLASH69

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF245

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.421 SFLASH\_MACRO\_0\_FREE\_SFLASH70

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF246

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.422 SFLASH\_MACRO\_0\_FREE\_SFLASH71

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF247

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.423 SFLASH\_MACRO\_0\_FREE\_SFLASH72

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.424 SFLASH\_MACRO\_0\_FREE\_SFLASH73

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF249

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.425 SFLASH\_MACRO\_0\_FREE\_SFLASH74

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF24A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.426 SFLASH\_MACRO\_0\_FREE\_SFLASH75

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF24B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.427 SFLASH\_MACRO\_0\_FREE\_SFLASH76

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF24C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.428 SFLASH\_MACRO\_0\_FREE\_SFLASH77

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF24D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.429 SFLASH\_MACRO\_0\_FREE\_SFLASH78

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF24E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.430 SFLASH\_MACRO\_0\_FREE\_SFLASH79

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF24F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.431 SFLASH\_MACRO\_0\_FREE\_SFLASH80

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.432 SFLASH\_MACRO\_0\_FREE\_SFLASH81

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF251

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.433 SFLASH\_MACRO\_0\_FREE\_SFLASH82

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.434 SFLASH\_MACRO\_0\_FREE\_SFLASH83

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF253

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.435 SFLASH\_MACRO\_0\_FREE\_SFLASH84

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.436 SFLASH\_MACRO\_0\_FREE\_SFLASH85

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF255

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.437 SFLASH\_MACRO\_0\_FREE\_SFLASH86

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF256

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.438 SFLASH\_MACRO\_0\_FREE\_SFLASH87

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF257

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.439 SFLASH\_MACRO\_0\_FREE\_SFLASH88

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.440 SFLASH\_MACRO\_0\_FREE\_SFLASH89

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF259

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.441 SFLASH\_MACRO\_0\_FREE\_SFLASH90

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF25A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.442 SFLASH\_MACRO\_0\_FREE\_SFLASH91

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF25B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.443 SFLASH\_MACRO\_0\_FREE\_SFLASH92

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF25C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.444 SFLASH\_MACRO\_0\_FREE\_SFLASH93

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF25D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.445 SFLASH\_MACRO\_0\_FREE\_SFLASH94

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF25E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.446 SFLASH\_MACRO\_0\_FREE\_SFLASH95

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF25F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.447 SFLASH\_MACRO\_0\_FREE\_SFLASH96

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.448 SFLASH\_MACRO\_0\_FREE\_SFLASH97

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF261

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.449 SFLASH\_MACRO\_0\_FREE\_SFLASH98

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.450 SFLASH\_MACRO\_0\_FREE\_SFLASH99

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF263

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.451 SFLASH\_MACRO\_0\_FREE\_SFLASH100

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.452 SFLASH\_MACRO\_0\_FREE\_SFLASH101

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF265

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.453 SFLASH\_MACRO\_0\_FREE\_SFLASH102

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.454 SFLASH\_MACRO\_0\_FREE\_SFLASH103

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF267

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.455 SFLASH\_MACRO\_0\_FREE\_SFLASH104

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.456 SFLASH\_MACRO\_0\_FREE\_SFLASH105

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF269

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.457 SFLASH\_MACRO\_0\_FREE\_SFLASH106

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF26A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.458 SFLASH\_MACRO\_0\_FREE\_SFLASH107

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF26B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.459 SFLASH\_MACRO\_0\_FREE\_SFLASH108

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF26C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.460 SFLASH\_MACRO\_0\_FREE\_SFLASH109

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF26D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.461 SFLASH\_MACRO\_0\_FREE\_SFLASH110

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF26E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.462 SFLASH\_MACRO\_0\_FREE\_SFLASH111

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF26F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.463 SFLASH\_MACRO\_0\_FREE\_SFLASH112

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.464 SFLASH\_MACRO\_0\_FREE\_SFLASH113

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF271

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.465 SFLASH\_MACRO\_0\_FREE\_SFLASH114

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF272

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.466 SFLASH\_MACRO\_0\_FREE\_SFLASH115

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF273

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.467 SFLASH\_MACRO\_0\_FREE\_SFLASH116

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.468 SFLASH\_MACRO\_0\_FREE\_SFLASH117

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF275

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.469 SFLASH\_MACRO\_0\_FREE\_SFLASH118

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF276

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.470 SFLASH\_MACRO\_0\_FREE\_SFLASH119

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF277

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.471 SFLASH\_MACRO\_0\_FREE\_SFLASH120

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.472 SFLASH\_MACRO\_0\_FREE\_SFLASH121

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF279

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.473 SFLASH\_MACRO\_0\_FREE\_SFLASH122

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF27A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.474 SFLASH\_MACRO\_0\_FREE\_SFLASH123

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF27B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.475 SFLASH\_MACRO\_0\_FREE\_SFLASH124

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF27C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.476 SFLASH\_MACRO\_0\_FREE\_SFLASH125

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF27D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.477 SFLASH\_MACRO\_0\_FREE\_SFLASH126

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF27E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.478 SFLASH\_MACRO\_0\_FREE\_SFLASH127

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF27F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.479 SFLASH\_MACRO\_0\_FREE\_SFLASH128

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.480 SFLASH\_MACRO\_0\_FREE\_SFLASH129

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF281

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.481 SFLASH\_MACRO\_0\_FREE\_SFLASH130

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF282

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.482 SFLASH\_MACRO\_0\_FREE\_SFLASH131

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF283

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.483 SFLASH\_MACRO\_0\_FREE\_SFLASH132

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.484 SFLASH\_MACRO\_0\_FREE\_SFLASH133

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF285

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.485 SFLASH\_MACRO\_0\_FREE\_SFLASH134

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF286

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.486 SFLASH\_MACRO\_0\_FREE\_SFLASH135

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF287

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.487 SFLASH\_MACRO\_0\_FREE\_SFLASH136

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.488 SFLASH\_MACRO\_0\_FREE\_SFLASH137

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF289

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.489 SFLASH\_MACRO\_0\_FREE\_SFLASH138

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF28A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.490 SFLASH\_MACRO\_0\_FREE\_SFLASH139

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF28B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.491 SFLASH\_MACRO\_0\_FREE\_SFLASH140

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF28C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.492 SFLASH\_MACRO\_0\_FREE\_SFLASH141

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF28D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.493 SFLASH\_MACRO\_0\_FREE\_SFLASH142

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF28E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.494 SFLASH\_MACRO\_0\_FREE\_SFLASH143

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF28F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.495 SFLASH\_MACRO\_0\_FREE\_SFLASH144

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.496 SFLASH\_MACRO\_0\_FREE\_SFLASH145

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF291

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.497 SFLASH\_MACRO\_0\_FREE\_SFLASH146

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF292

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.498 SFLASH\_MACRO\_0\_FREE\_SFLASH147

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF293

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.499 SFLASH\_MACRO\_0\_FREE\_SFLASH148

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.500 SFLASH\_MACRO\_0\_FREE\_SFLASH149

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF295

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.501 SFLASH\_MACRO\_0\_FREE\_SFLASH150

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF296

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.502 SFLASH\_MACRO\_0\_FREE\_SFLASH151

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF297

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.503 SFLASH\_MACRO\_0\_FREE\_SFLASH152

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.504 SFLASH\_MACRO\_0\_FREE\_SFLASH153

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF299

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.505 SFLASH\_MACRO\_0\_FREE\_SFLASH154

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF29A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.506 SFLASH\_MACRO\_0\_FREE\_SFLASH155

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF29B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.507 SFLASH\_MACRO\_0\_FREE\_SFLASH156

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF29C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.508 SFLASH\_MACRO\_0\_FREE\_SFLASH157

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF29D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.509 SFLASH\_MACRO\_0\_FREE\_SFLASH158

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF29E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.510 SFLASH\_MACRO\_0\_FREE\_SFLASH159

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF29F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.511 SFLASH\_MACRO\_0\_FREE\_SFLASH160

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.512 SFLASH\_MACRO\_0\_FREE\_SFLASH161

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.513 SFLASH\_MACRO\_0\_FREE\_SFLASH162

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.514 SFLASH\_MACRO\_0\_FREE\_SFLASH163

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.515 SFLASH\_MACRO\_0\_FREE\_SFLASH164

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.516 SFLASH\_MACRO\_0\_FREE\_SFLASH165

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.517 SFLASH\_MACRO\_0\_FREE\_SFLASH166

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.518 SFLASH\_MACRO\_0\_FREE\_SFLASH167

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.519 SFLASH\_MACRO\_0\_FREE\_SFLASH168

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.520 SFLASH\_MACRO\_0\_FREE\_SFLASH169

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.521 SFLASH\_MACRO\_0\_FREE\_SFLASH170

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.522 SFLASH\_MACRO\_0\_FREE\_SFLASH171

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.523 SFLASH\_MACRO\_0\_FREE\_SFLASH172

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.524 SFLASH\_MACRO\_0\_FREE\_SFLASH173

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.525 SFLASH\_MACRO\_0\_FREE\_SFLASH174

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.526 SFLASH\_MACRO\_0\_FREE\_SFLASH175

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.527 SFLASH\_MACRO\_0\_FREE\_SFLASH176

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.528 SFLASH\_MACRO\_0\_FREE\_SFLASH177

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.529 SFLASH\_MACRO\_0\_FREE\_SFLASH178

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.530 SFLASH\_MACRO\_0\_FREE\_SFLASH179

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.531 SFLASH\_MACRO\_0\_FREE\_SFLASH180

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.532 SFLASH\_MACRO\_0\_FREE\_SFLASH181

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.533 SFLASH\_MACRO\_0\_FREE\_SFLASH182

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.534 SFLASH\_MACRO\_0\_FREE\_SFLASH183

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.535 SFLASH\_MACRO\_0\_FREE\_SFLASH184

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.536 SFLASH\_MACRO\_0\_FREE\_SFLASH185

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.537 SFLASH\_MACRO\_0\_FREE\_SFLASH186

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.538 SFLASH\_MACRO\_0\_FREE\_SFLASH187

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.539 SFLASH\_MACRO\_0\_FREE\_SFLASH188

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.540 SFLASH\_MACRO\_0\_FREE\_SFLASH189

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.541 SFLASH\_MACRO\_0\_FREE\_SFLASH190

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.542 SFLASH\_MACRO\_0\_FREE\_SFLASH191

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.543 SFLASH\_MACRO\_0\_FREE\_SFLASH192

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.544 SFLASH\_MACRO\_0\_FREE\_SFLASH193

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.545 SFLASH\_MACRO\_0\_FREE\_SFLASH194

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.546 SFLASH\_MACRO\_0\_FREE\_SFLASH195

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.547 SFLASH\_MACRO\_0\_FREE\_SFLASH196

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.548 SFLASH\_MACRO\_0\_FREE\_SFLASH197

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.549 SFLASH\_MACRO\_0\_FREE\_SFLASH198

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.550 SFLASH\_MACRO\_0\_FREE\_SFLASH199

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.551 SFLASH\_MACRO\_0\_FREE\_SFLASH200

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.552 SFLASH\_MACRO\_0\_FREE\_SFLASH201

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.553 SFLASH\_MACRO\_0\_FREE\_SFLASH202

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.554 SFLASH\_MACRO\_0\_FREE\_SFLASH203

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.555 SFLASH\_MACRO\_0\_FREE\_SFLASH204

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.556 SFLASH\_MACRO\_0\_FREE\_SFLASH205

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.557 SFLASH\_MACRO\_0\_FREE\_SFLASH206

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.558 SFLASH\_MACRO\_0\_FREE\_SFLASH207

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.559 SFLASH\_MACRO\_0\_FREE\_SFLASH208

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.560 SFLASH\_MACRO\_0\_FREE\_SFLASH209

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.561 SFLASH\_MACRO\_0\_FREE\_SFLASH210

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.562 SFLASH\_MACRO\_0\_FREE\_SFLASH211

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.563 SFLASH\_MACRO\_0\_FREE\_SFLASH212

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.564 SFLASH\_MACRO\_0\_FREE\_SFLASH213

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.565 SFLASH\_MACRO\_0\_FREE\_SFLASH214

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.566 SFLASH\_MACRO\_0\_FREE\_SFLASH215

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.567 SFLASH\_MACRO\_0\_FREE\_SFLASH216

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.568 SFLASH\_MACRO\_0\_FREE\_SFLASH217

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.569 SFLASH\_MACRO\_0\_FREE\_SFLASH218

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.570 SFLASH\_MACRO\_0\_FREE\_SFLASH219

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.571 SFLASH\_MACRO\_0\_FREE\_SFLASH220

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.572 SFLASH\_MACRO\_0\_FREE\_SFLASH221

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.573 SFLASH\_MACRO\_0\_FREE\_SFLASH222

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.574 SFLASH\_MACRO\_0\_FREE\_SFLASH223

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.575 SFLASH\_MACRO\_0\_FREE\_SFLASH224

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.576 SFLASH\_MACRO\_0\_FREE\_SFLASH225

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.577 SFLASH\_MACRO\_0\_FREE\_SFLASH226

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.578 SFLASH\_MACRO\_0\_FREE\_SFLASH227

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.579 SFLASH\_MACRO\_0\_FREE\_SFLASH228

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.580 SFLASH\_MACRO\_0\_FREE\_SFLASH229

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.581 SFLASH\_MACRO\_0\_FREE\_SFLASH230

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.582 SFLASH\_MACRO\_0\_FREE\_SFLASH231

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.583 SFLASH\_MACRO\_0\_FREE\_SFLASH232

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.584 SFLASH\_MACRO\_0\_FREE\_SFLASH233

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.585 SFLASH\_MACRO\_0\_FREE\_SFLASH234

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.586 SFLASH\_MACRO\_0\_FREE\_SFLASH235

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.587 SFLASH\_MACRO\_0\_FREE\_SFLASH236

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.588 SFLASH\_MACRO\_0\_FREE\_SFLASH237

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.589 SFLASH\_MACRO\_0\_FREE\_SFLASH238

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.590 SFLASH\_MACRO\_0\_FREE\_SFLASH239

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.591 SFLASH\_MACRO\_0\_FREE\_SFLASH240

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.592 SFLASH\_MACRO\_0\_FREE\_SFLASH241

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.593 SFLASH\_MACRO\_0\_FREE\_SFLASH242

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.594 SFLASH\_MACRO\_0\_FREE\_SFLASH243

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.595 SFLASH\_MACRO\_0\_FREE\_SFLASH244

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.596 SFLASH\_MACRO\_0\_FREE\_SFLASH245

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.597 SFLASH\_MACRO\_0\_FREE\_SFLASH246

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.598 SFLASH\_MACRO\_0\_FREE\_SFLASH247

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.599 SFLASH\_MACRO\_0\_FREE\_SFLASH248

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.600 SFLASH\_MACRO\_0\_FREE\_SFLASH249

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.601 SFLASH\_MACRO\_0\_FREE\_SFLASH250

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.602 SFLASH\_MACRO\_0\_FREE\_SFLASH251

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF2FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.603 SFLASH\_MACRO\_0\_FREE\_SFLASH252

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.604 SFLASH\_MACRO\_0\_FREE\_SFLASH253

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.605 SFLASH\_MACRO\_0\_FREE\_SFLASH254

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.606 SFLASH\_MACRO\_0\_FREE\_SFLASH255

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.607 SFLASH\_MACRO\_0\_FREE\_SFLASH256

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.608 SFLASH\_MACRO\_0\_FREE\_SFLASH257

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.609 SFLASH\_MACRO\_0\_FREE\_SFLASH258

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.610 SFLASH\_MACRO\_0\_FREE\_SFLASH259

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.611 SFLASH\_MACRO\_0\_FREE\_SFLASH260

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.612 SFLASH\_MACRO\_0\_FREE\_SFLASH261

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.613 SFLASH\_MACRO\_0\_FREE\_SFLASH262

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.614 SFLASH\_MACRO\_0\_FREE\_SFLASH263

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.615 SFLASH\_MACRO\_0\_FREE\_SFLASH264

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.616 SFLASH\_MACRO\_0\_FREE\_SFLASH265

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.617 SFLASH\_MACRO\_0\_FREE\_SFLASH266

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF30A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.618 SFLASH\_MACRO\_0\_FREE\_SFLASH267

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF30B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.619 SFLASH\_MACRO\_0\_FREE\_SFLASH268

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF30C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.620 SFLASH\_MACRO\_0\_FREE\_SFLASH269

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF30D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.621 SFLASH\_MACRO\_0\_FREE\_SFLASH270

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF30E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.622 SFLASH\_MACRO\_0\_FREE\_SFLASH271

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF30F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.623 SFLASH\_MACRO\_0\_FREE\_SFLASH272

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.624 SFLASH\_MACRO\_0\_FREE\_SFLASH273

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.625 SFLASH\_MACRO\_0\_FREE\_SFLASH274

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.626 SFLASH\_MACRO\_0\_FREE\_SFLASH275

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.627 SFLASH\_MACRO\_0\_FREE\_SFLASH276

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.628 SFLASH\_MACRO\_0\_FREE\_SFLASH277

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.629 SFLASH\_MACRO\_0\_FREE\_SFLASH278

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.630 SFLASH\_MACRO\_0\_FREE\_SFLASH279

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.631 SFLASH\_MACRO\_0\_FREE\_SFLASH280

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.632 SFLASH\_MACRO\_0\_FREE\_SFLASH281

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.633 SFLASH\_MACRO\_0\_FREE\_SFLASH282

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF31A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.634 SFLASH\_MACRO\_0\_FREE\_SFLASH283

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF31B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.635 SFLASH\_MACRO\_0\_FREE\_SFLASH284

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF31C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.636 SFLASH\_MACRO\_0\_FREE\_SFLASH285

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF31D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.637 SFLASH\_MACRO\_0\_FREE\_SFLASH286

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF31E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.638 SFLASH\_MACRO\_0\_FREE\_SFLASH287

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF31F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.639 SFLASH\_MACRO\_0\_FREE\_SFLASH288

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.640 SFLASH\_MACRO\_0\_FREE\_SFLASH289

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF321

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.641 SFLASH\_MACRO\_0\_FREE\_SFLASH290

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF322

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.642 SFLASH\_MACRO\_0\_FREE\_SFLASH291

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF323

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.643 SFLASH\_MACRO\_0\_FREE\_SFLASH292

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.644 SFLASH\_MACRO\_0\_FREE\_SFLASH293

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF325

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.645 SFLASH\_MACRO\_0\_FREE\_SFLASH294

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF326

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.646 SFLASH\_MACRO\_0\_FREE\_SFLASH295

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF327

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.647 SFLASH\_MACRO\_0\_FREE\_SFLASH296

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.648 SFLASH\_MACRO\_0\_FREE\_SFLASH297

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF329

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.649 SFLASH\_MACRO\_0\_FREE\_SFLASH298

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF32A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.650 SFLASH\_MACRO\_0\_FREE\_SFLASH299

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF32B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.651 SFLASH\_MACRO\_0\_FREE\_SFLASH300

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF32C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.652 SFLASH\_MACRO\_0\_FREE\_SFLASH301

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF32D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.653 SFLASH\_MACRO\_0\_FREE\_SFLASH302

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF32E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.654 SFLASH\_MACRO\_0\_FREE\_SFLASH303

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF32F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.655 SFLASH\_MACRO\_0\_FREE\_SFLASH304

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.656 SFLASH\_MACRO\_0\_FREE\_SFLASH305

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF331

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.657 SFLASH\_MACRO\_0\_FREE\_SFLASH306

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF332

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.658 SFLASH\_MACRO\_0\_FREE\_SFLASH307

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF333

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.659 SFLASH\_MACRO\_0\_FREE\_SFLASH308

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.660 SFLASH\_MACRO\_0\_FREE\_SFLASH309

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF335

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.661 SFLASH\_MACRO\_0\_FREE\_SFLASH310

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF336

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.662 SFLASH\_MACRO\_0\_FREE\_SFLASH311

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF337

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.663 SFLASH\_MACRO\_0\_FREE\_SFLASH312

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.664 SFLASH\_MACRO\_0\_FREE\_SFLASH313

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF339

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.665 SFLASH\_MACRO\_0\_FREE\_SFLASH314

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF33A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.666 SFLASH\_MACRO\_0\_FREE\_SFLASH315

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF33B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.667 SFLASH\_MACRO\_0\_FREE\_SFLASH316

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF33C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.668 SFLASH\_MACRO\_0\_FREE\_SFLASH317

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF33D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.669 SFLASH\_MACRO\_0\_FREE\_SFLASH318

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF33E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.670 SFLASH\_MACRO\_0\_FREE\_SFLASH319

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF33F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.671 SFLASH\_MACRO\_0\_FREE\_SFLASH320

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.672 SFLASH\_MACRO\_0\_FREE\_SFLASH321

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.673 SFLASH\_MACRO\_0\_FREE\_SFLASH322

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.674 SFLASH\_MACRO\_0\_FREE\_SFLASH323

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.675 SFLASH\_MACRO\_0\_FREE\_SFLASH324

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.676 SFLASH\_MACRO\_0\_FREE\_SFLASH325

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.677 SFLASH\_MACRO\_0\_FREE\_SFLASH326

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.678 SFLASH\_MACRO\_0\_FREE\_SFLASH327

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.679 SFLASH\_MACRO\_0\_FREE\_SFLASH328

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.680 SFLASH\_MACRO\_0\_FREE\_SFLASH329

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.681 SFLASH\_MACRO\_0\_FREE\_SFLASH330

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF34A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.682 SFLASH\_MACRO\_0\_FREE\_SFLASH331

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF34B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.683 SFLASH\_MACRO\_0\_FREE\_SFLASH332

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF34C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.684 SFLASH\_MACRO\_0\_FREE\_SFLASH333

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF34D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.685 SFLASH\_MACRO\_0\_FREE\_SFLASH334

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF34E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.686 SFLASH\_MACRO\_0\_FREE\_SFLASH335

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF34F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.687 SFLASH\_MACRO\_0\_FREE\_SFLASH336

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.688 SFLASH\_MACRO\_0\_FREE\_SFLASH337

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.689 SFLASH\_MACRO\_0\_FREE\_SFLASH338

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.690 SFLASH\_MACRO\_0\_FREE\_SFLASH339

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.691 SFLASH\_MACRO\_0\_FREE\_SFLASH340

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.692 SFLASH\_MACRO\_0\_FREE\_SFLASH341

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.693 SFLASH\_MACRO\_0\_FREE\_SFLASH342

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.694 SFLASH\_MACRO\_0\_FREE\_SFLASH343

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.695 SFLASH\_MACRO\_0\_FREE\_SFLASH344

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.696 SFLASH\_MACRO\_0\_FREE\_SFLASH345

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.697 SFLASH\_MACRO\_0\_FREE\_SFLASH346

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF35A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.698 SFLASH\_MACRO\_0\_FREE\_SFLASH347

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF35B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.699 SFLASH\_MACRO\_0\_FREE\_SFLASH348

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF35C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.700 SFLASH\_MACRO\_0\_FREE\_SFLASH349

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF35D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.701 SFLASH\_MACRO\_0\_FREE\_SFLASH350

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF35E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.702 SFLASH\_MACRO\_0\_FREE\_SFLASH351

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF35F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.703 SFLASH\_MACRO\_0\_FREE\_SFLASH352

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.704 SFLASH\_MACRO\_0\_FREE\_SFLASH353

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.705 SFLASH\_MACRO\_0\_FREE\_SFLASH354

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.706 SFLASH\_MACRO\_0\_FREE\_SFLASH355

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.707 SFLASH\_MACRO\_0\_FREE\_SFLASH356

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.708 SFLASH\_MACRO\_0\_FREE\_SFLASH357

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.709 SFLASH\_MACRO\_0\_FREE\_SFLASH358

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.710 SFLASH\_MACRO\_0\_FREE\_SFLASH359

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.711 SFLASH\_MACRO\_0\_FREE\_SFLASH360

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.712 SFLASH\_MACRO\_0\_FREE\_SFLASH361

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.713 SFLASH\_MACRO\_0\_FREE\_SFLASH362

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF36A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.714 SFLASH\_MACRO\_0\_FREE\_SFLASH363

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF36B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.715 SFLASH\_MACRO\_0\_FREE\_SFLASH364

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF36C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.716 SFLASH\_MACRO\_0\_FREE\_SFLASH365

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF36D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.717 SFLASH\_MACRO\_0\_FREE\_SFLASH366

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF36E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.718 SFLASH\_MACRO\_0\_FREE\_SFLASH367

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF36F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.719 SFLASH\_MACRO\_0\_FREE\_SFLASH368

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.720 SFLASH\_MACRO\_0\_FREE\_SFLASH369

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.721 SFLASH\_MACRO\_0\_FREE\_SFLASH370

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.722 SFLASH\_MACRO\_0\_FREE\_SFLASH371

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.723 SFLASH\_MACRO\_0\_FREE\_SFLASH372

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.724 SFLASH\_MACRO\_0\_FREE\_SFLASH373

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.725 SFLASH\_MACRO\_0\_FREE\_SFLASH374

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.726 SFLASH\_MACRO\_0\_FREE\_SFLASH375

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.727 SFLASH\_MACRO\_0\_FREE\_SFLASH376

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.728 SFLASH\_MACRO\_0\_FREE\_SFLASH377

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.729 SFLASH\_MACRO\_0\_FREE\_SFLASH378

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF37A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.730 SFLASH\_MACRO\_0\_FREE\_SFLASH379

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF37B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.731 SFLASH\_MACRO\_0\_FREE\_SFLASH380

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF37C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.732 SFLASH\_MACRO\_0\_FREE\_SFLASH381

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF37D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.733 SFLASH\_MACRO\_0\_FREE\_SFLASH382

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF37E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.734 SFLASH\_MACRO\_0\_FREE\_SFLASH383

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF37F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.735 SFLASH\_MACRO\_0\_FREE\_SFLASH384

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.736 SFLASH\_MACRO\_0\_FREE\_SFLASH385

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF381

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.737 SFLASH\_MACRO\_0\_FREE\_SFLASH386

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF382

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.738 SFLASH\_MACRO\_0\_FREE\_SFLASH387

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF383

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.739 SFLASH\_MACRO\_0\_FREE\_SFLASH388

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF384

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.740 SFLASH\_MACRO\_0\_FREE\_SFLASH389

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF385

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.741 SFLASH\_MACRO\_0\_FREE\_SFLASH390

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF386

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.742 SFLASH\_MACRO\_0\_FREE\_SFLASH391

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF387

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.743 SFLASH\_MACRO\_0\_FREE\_SFLASH392

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF388

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.744 SFLASH\_MACRO\_0\_FREE\_SFLASH393

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF389

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.745 SFLASH\_MACRO\_0\_FREE\_SFLASH394

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF38A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.746 SFLASH\_MACRO\_0\_FREE\_SFLASH395

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF38B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.747 SFLASH\_MACRO\_0\_FREE\_SFLASH396

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF38C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.748 SFLASH\_MACRO\_0\_FREE\_SFLASH397

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF38D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.749 SFLASH\_MACRO\_0\_FREE\_SFLASH398

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF38E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.750 SFLASH\_MACRO\_0\_FREE\_SFLASH399

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF38F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.751 SFLASH\_MACRO\_0\_FREE\_SFLASH400

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF390

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.752 SFLASH\_MACRO\_0\_FREE\_SFLASH401

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF391

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.753 SFLASH\_MACRO\_0\_FREE\_SFLASH402

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF392

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.754 SFLASH\_MACRO\_0\_FREE\_SFLASH403

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF393

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.755 SFLASH\_MACRO\_0\_FREE\_SFLASH404

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF394

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.756 SFLASH\_MACRO\_0\_FREE\_SFLASH405

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF395

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.757 SFLASH\_MACRO\_0\_FREE\_SFLASH406

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF396

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.758 SFLASH\_MACRO\_0\_FREE\_SFLASH407

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF397

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.759 SFLASH\_MACRO\_0\_FREE\_SFLASH408

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF398

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.760 SFLASH\_MACRO\_0\_FREE\_SFLASH409

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF399

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.761 SFLASH\_MACRO\_0\_FREE\_SFLASH410

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF39A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.762 SFLASH\_MACRO\_0\_FREE\_SFLASH411

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF39B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.763 SFLASH\_MACRO\_0\_FREE\_SFLASH412

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF39C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.764 SFLASH\_MACRO\_0\_FREE\_SFLASH413

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF39D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.765 SFLASH\_MACRO\_0\_FREE\_SFLASH414

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF39E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.766 SFLASH\_MACRO\_0\_FREE\_SFLASH415

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF39F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.767 SFLASH\_MACRO\_0\_FREE\_SFLASH416

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.768 SFLASH\_MACRO\_0\_FREE\_SFLASH417

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.769 SFLASH\_MACRO\_0\_FREE\_SFLASH418

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.770 SFLASH\_MACRO\_0\_FREE\_SFLASH419

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.771 SFLASH\_MACRO\_0\_FREE\_SFLASH420

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.772 SFLASH\_MACRO\_0\_FREE\_SFLASH421

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.773 SFLASH\_MACRO\_0\_FREE\_SFLASH422

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.774 SFLASH\_MACRO\_0\_FREE\_SFLASH423

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.775 SFLASH\_MACRO\_0\_FREE\_SFLASH424

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.776 SFLASH\_MACRO\_0\_FREE\_SFLASH425

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.777 SFLASH\_MACRO\_0\_FREE\_SFLASH426

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.778 SFLASH\_MACRO\_0\_FREE\_SFLASH427

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.779 SFLASH\_MACRO\_0\_FREE\_SFLASH428

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.780 SFLASH\_MACRO\_0\_FREE\_SFLASH429

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.781 SFLASH\_MACRO\_0\_FREE\_SFLASH430

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.782 SFLASH\_MACRO\_0\_FREE\_SFLASH431

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.783 SFLASH\_MACRO\_0\_FREE\_SFLASH432

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.784 SFLASH\_MACRO\_0\_FREE\_SFLASH433

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.785 SFLASH\_MACRO\_0\_FREE\_SFLASH434

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.786 SFLASH\_MACRO\_0\_FREE\_SFLASH435

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.787 SFLASH\_MACRO\_0\_FREE\_SFLASH436

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.788 SFLASH\_MACRO\_0\_FREE\_SFLASH437

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.789 SFLASH\_MACRO\_0\_FREE\_SFLASH438

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.790 SFLASH\_MACRO\_0\_FREE\_SFLASH439

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.791 SFLASH\_MACRO\_0\_FREE\_SFLASH440

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.792 SFLASH\_MACRO\_0\_FREE\_SFLASH441

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.793 SFLASH\_MACRO\_0\_FREE\_SFLASH442

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.794 SFLASH\_MACRO\_0\_FREE\_SFLASH443

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.795 SFLASH\_MACRO\_0\_FREE\_SFLASH444

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.796 SFLASH\_MACRO\_0\_FREE\_SFLASH445

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.797 SFLASH\_MACRO\_0\_FREE\_SFLASH446

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.798 SFLASH\_MACRO\_0\_FREE\_SFLASH447

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.799 SFLASH\_MACRO\_0\_FREE\_SFLASH448

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.800 SFLASH\_MACRO\_0\_FREE\_SFLASH449

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.801 SFLASH\_MACRO\_0\_FREE\_SFLASH450

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.802 SFLASH\_MACRO\_0\_FREE\_SFLASH451

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.803 SFLASH\_MACRO\_0\_FREE\_SFLASH452

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.804 SFLASH\_MACRO\_0\_FREE\_SFLASH453

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.805 SFLASH\_MACRO\_0\_FREE\_SFLASH454

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.806 SFLASH\_MACRO\_0\_FREE\_SFLASH455

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.807 SFLASH\_MACRO\_0\_FREE\_SFLASH456

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.808 SFLASH\_MACRO\_0\_FREE\_SFLASH457

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.809 SFLASH\_MACRO\_0\_FREE\_SFLASH458

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.810 SFLASH\_MACRO\_0\_FREE\_SFLASH459

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.811 SFLASH\_MACRO\_0\_FREE\_SFLASH460

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.812 SFLASH\_MACRO\_0\_FREE\_SFLASH461

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.813 SFLASH\_MACRO\_0\_FREE\_SFLASH462

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.814 SFLASH\_MACRO\_0\_FREE\_SFLASH463

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.815 SFLASH\_MACRO\_0\_FREE\_SFLASH464

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.816 SFLASH\_MACRO\_0\_FREE\_SFLASH465

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.817 SFLASH\_MACRO\_0\_FREE\_SFLASH466

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.818 SFLASH\_MACRO\_0\_FREE\_SFLASH467

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.819 SFLASH\_MACRO\_0\_FREE\_SFLASH468

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.820 SFLASH\_MACRO\_0\_FREE\_SFLASH469

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.821 SFLASH\_MACRO\_0\_FREE\_SFLASH470

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.822 SFLASH\_MACRO\_0\_FREE\_SFLASH471

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.823 SFLASH\_MACRO\_0\_FREE\_SFLASH472

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.824 SFLASH\_MACRO\_0\_FREE\_SFLASH473

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.825 SFLASH\_MACRO\_0\_FREE\_SFLASH474

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.826 SFLASH\_MACRO\_0\_FREE\_SFLASH475

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.827 SFLASH\_MACRO\_0\_FREE\_SFLASH476

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.828 SFLASH\_MACRO\_0\_FREE\_SFLASH477

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.829 SFLASH\_MACRO\_0\_FREE\_SFLASH478

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.830 SFLASH\_MACRO\_0\_FREE\_SFLASH479

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.831 SFLASH\_MACRO\_0\_FREE\_SFLASH480

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.832 SFLASH\_MACRO\_0\_FREE\_SFLASH481

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.833 SFLASH\_MACRO\_0\_FREE\_SFLASH482

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.834 SFLASH\_MACRO\_0\_FREE\_SFLASH483

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.835 SFLASH\_MACRO\_0\_FREE\_SFLASH484

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.836 SFLASH\_MACRO\_0\_FREE\_SFLASH485

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.837 SFLASH\_MACRO\_0\_FREE\_SFLASH486

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.838 SFLASH\_MACRO\_0\_FREE\_SFLASH487

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.839 SFLASH\_MACRO\_0\_FREE\_SFLASH488

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.840 SFLASH\_MACRO\_0\_FREE\_SFLASH489

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.841 SFLASH\_MACRO\_0\_FREE\_SFLASH490

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.842 SFLASH\_MACRO\_0\_FREE\_SFLASH491

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.843 SFLASH\_MACRO\_0\_FREE\_SFLASH492

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.844 SFLASH\_MACRO\_0\_FREE\_SFLASH493

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.845 SFLASH\_MACRO\_0\_FREE\_SFLASH494

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.846 SFLASH\_MACRO\_0\_FREE\_SFLASH495

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.847 SFLASH\_MACRO\_0\_FREE\_SFLASH496

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.848 SFLASH\_MACRO\_0\_FREE\_SFLASH497

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.849 SFLASH\_MACRO\_0\_FREE\_SFLASH498

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.850 SFLASH\_MACRO\_0\_FREE\_SFLASH499

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.851 SFLASH\_MACRO\_0\_FREE\_SFLASH500

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.852 SFLASH\_MACRO\_0\_FREE\_SFLASH501

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.853 SFLASH\_MACRO\_0\_FREE\_SFLASH502

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.854 SFLASH\_MACRO\_0\_FREE\_SFLASH503

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.855 SFLASH\_MACRO\_0\_FREE\_SFLASH504

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.856 SFLASH\_MACRO\_0\_FREE\_SFLASH505

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.857 SFLASH\_MACRO\_0\_FREE\_SFLASH506

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.858 SFLASH\_MACRO\_0\_FREE\_SFLASH507

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.859 SFLASH\_MACRO\_0\_FREE\_SFLASH508

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.860 SFLASH\_MACRO\_0\_FREE\_SFLASH509

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.861 SFLASH\_MACRO\_0\_FREE\_SFLASH510

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 21.1.862 SFLASH\_MACRO\_0\_FREE\_SFLASH511

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF3FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 21.1.863 SFLASH\_ALT\_PROT\_ROW0

Per Page Write Protection

Address: 0x0FFF400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.864 SFLASH\_ALT\_PROT\_ROW1

Per Page Write Protection

Address: 0x0FFF401

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.865 SFLASH\_ALT\_PROT\_ROW2

Per Page Write Protection

Address: 0x0FFF402

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.866 SFLASH\_ALT\_PROT\_ROW3

Per Page Write Protection

Address: 0x0FFF403

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.867 SFLASH\_ALT\_PROT\_ROW4

Per Page Write Protection

Address: 0x0FFF404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.868 SFLASH\_ALT\_PROT\_ROW5

Per Page Write Protection

Address: 0x0FFF405

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.869 SFLASH\_ALT\_PROT\_ROW6

Per Page Write Protection

Address: 0x0FFF406

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.870 SFLASH\_ALT\_PROT\_ROW7

Per Page Write Protection

Address: 0x0FFF407

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.871 SFLASH\_ALT\_PROT\_ROW8

Per Page Write Protection

Address: 0x0FFF408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.872 SFLASH\_ALT\_PROT\_ROW9

Per Page Write Protection

Address: 0x0FFF409

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.873 SFLASH\_ALT\_PROT\_ROW10

Per Page Write Protection

Address: 0x0FFF40A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.874 SFLASH\_ALT\_PROT\_ROW11

Per Page Write Protection

Address: 0x0FFF40B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.875 SFLASH\_ALT\_PROT\_ROW12

Per Page Write Protection

Address: 0x0FFF40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.876 SFLASH\_ALT\_PROT\_ROW13

Per Page Write Protection

Address: 0x0FFF40D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.877 SFLASH\_ALT\_PROT\_ROW14

Per Page Write Protection

Address: 0x0FFF40E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.878 SFLASH\_ALT\_PROT\_ROW15

Per Page Write Protection

Address: 0x0FFFF40F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.879 SFLASH\_ALT\_PROT\_ROW16

Per Page Write Protection

Address: 0x0FFF410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.880 SFLASH\_ALT\_PROT\_ROW17

Per Page Write Protection

Address: 0x0FFFF411

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.881 SFLASH\_ALT\_PROT\_ROW18

Per Page Write Protection

Address: 0x0FFF412

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.882 SFLASH\_ALT\_PROT\_ROW19

Per Page Write Protection

Address: 0x0FFF413

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.883 SFLASH\_ALT\_PROT\_ROW20

Per Page Write Protection

Address: 0x0FFFF414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.884 SFLASH\_ALT\_PROT\_ROW21

Per Page Write Protection

Address: 0x0FFF415

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.885 SFLASH\_ALT\_PROT\_ROW22

Per Page Write Protection

Address: 0x0FFF416

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.886 SFLASH\_ALT\_PROT\_ROW23

Per Page Write Protection

Address: 0x0FFFF417

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.887 SFLASH\_ALT\_PROT\_ROW24

Per Page Write Protection

Address: 0x0FFF418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.888 SFLASH\_ALT\_PROT\_ROW25

Per Page Write Protection

Address: 0x0FFF419

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.889 SFLASH\_ALT\_PROT\_ROW26

Per Page Write Protection

Address: 0x0FFF41A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.890 SFLASH\_ALT\_PROT\_ROW27

Per Page Write Protection

Address: 0x0FFF41B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.891 SFLASH\_ALT\_PROT\_ROW28

Per Page Write Protection

Address: 0x0FFF41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.892 SFLASH\_ALT\_PROT\_ROW29

Per Page Write Protection

Address: 0x0FFFF41D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.893 SFLASH\_ALT\_PROT\_ROW30

Per Page Write Protection

Address: 0x0FFFF41E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.894 SFLASH\_ALT\_PROT\_ROW31

Per Page Write Protection

Address: 0x0FFFF41F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.895 SFLASH\_ALT\_PROT\_ROW32

Per Page Write Protection

Address: 0x0FFF420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.896 SFLASH\_ALT\_PROT\_ROW33

Per Page Write Protection

Address: 0x0FFF421

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.897 SFLASH\_ALT\_PROT\_ROW34

Per Page Write Protection

Address: 0x0FFF422

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.898 SFLASH\_ALT\_PROT\_ROW35

Per Page Write Protection

Address: 0x0FFF423

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.899 SFLASH\_ALT\_PROT\_ROW36

Per Page Write Protection

Address: 0x0FFF424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.900 SFLASH\_ALT\_PROT\_ROW37

Per Page Write Protection

Address: 0x0FFF425

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.901 SFLASH\_ALT\_PROT\_ROW38

Per Page Write Protection

Address: 0x0FFF426

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.902 SFLASH\_ALT\_PROT\_ROW39

Per Page Write Protection

Address: 0x0FFF427

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.903 SFLASH\_ALT\_PROT\_ROW40

Per Page Write Protection

Address: 0x0FFF428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.904 SFLASH\_ALT\_PROT\_ROW41

Per Page Write Protection

Address: 0x0FFF429

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.905 SFLASH\_ALT\_PROT\_ROW42

Per Page Write Protection

Address: 0x0FFF42A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.906 SFLASH\_ALT\_PROT\_ROW43

Per Page Write Protection

Address: 0x0FFF42B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.907 SFLASH\_ALT\_PROT\_ROW44

Per Page Write Protection

Address: 0x0FFF42C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.908 SFLASH\_ALT\_PROT\_ROW45

Per Page Write Protection

Address: 0x0FFF42D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.909 SFLASH\_ALT\_PROT\_ROW46

Per Page Write Protection

Address: 0x0FFF42E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.910 SFLASH\_ALT\_PROT\_ROW47

Per Page Write Protection

Address: 0x0FFF42F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.911 SFLASH\_ALT\_PROT\_ROW48

Per Page Write Protection

Address: 0x0FFFF430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.912 SFLASH\_ALT\_PROT\_ROW49

Per Page Write Protection

Address: 0x0FFF431

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.913 SFLASH\_ALT\_PROT\_ROW50

Per Page Write Protection

Address: 0x0FFF432

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.914 SFLASH\_ALT\_PROT\_ROW51

Per Page Write Protection

Address: 0x0FFF433

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.915 SFLASH\_ALT\_PROT\_ROW52

Per Page Write Protection

Address: 0x0FFF434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.916 SFLASH\_ALT\_PROT\_ROW53

Per Page Write Protection

Address: 0x0FFF435

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.917 SFLASH\_ALT\_PROT\_ROW54

Per Page Write Protection

Address: 0x0FFF436

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.918 SFLASH\_ALT\_PROT\_ROW55

Per Page Write Protection

Address: 0x0FFF437

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.919 SFLASH\_ALT\_PROT\_ROW56

Per Page Write Protection

Address: 0x0FFF438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.920 SFLASH\_ALT\_PROT\_ROW57

Per Page Write Protection

Address: 0x0FFF439

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.921 SFLASH\_ALT\_PROT\_ROW58

Per Page Write Protection

Address: 0x0FFF43A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.922 SFLASH\_ALT\_PROT\_ROW59

Per Page Write Protection

Address: 0x0FFF43B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.923 SFLASH\_ALT\_PROT\_ROW60

Per Page Write Protection

Address: 0x0FFF43C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.924 SFLASH\_ALT\_PROT\_ROW61

Per Page Write Protection

Address: 0x0FFF43D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.925 SFLASH\_ALT\_PROT\_ROW62

Per Page Write Protection

Address: 0x0FFFF43E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.926 SFLASH\_ALT\_PROT\_ROW63

Per Page Write Protection

Address: 0x0FFFF43F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.927 SFLASH\_ALT\_PROT\_ROW64

Per Page Write Protection

Address: 0x0FFF440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.928 SFLASH\_ALT\_PROT\_ROW65

Per Page Write Protection

Address: 0x0FFF441

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.929 SFLASH\_ALT\_PROT\_ROW66

Per Page Write Protection

Address: 0x0FFF442

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.930 SFLASH\_ALT\_PROT\_ROW67

Per Page Write Protection

Address: 0x0FFF443

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.931 SFLASH\_ALT\_PROT\_ROW68

Per Page Write Protection

Address: 0x0FFF444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.932 SFLASH\_ALT\_PROT\_ROW69

Per Page Write Protection

Address: 0x0FFF445

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.933 SFLASH\_ALT\_PROT\_ROW70

Per Page Write Protection

Address: 0x0FFF446

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.934 SFLASH\_ALT\_PROT\_ROW71

Per Page Write Protection

Address: 0x0FFF447

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.935 SFLASH\_ALT\_PROT\_ROW72

Per Page Write Protection

Address: 0x0FFF448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.936 SFLASH\_ALT\_PROT\_ROW73

Per Page Write Protection

Address: 0x0FFF449

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.937 SFLASH\_ALT\_PROT\_ROW74

Per Page Write Protection

Address: 0x0FFF44A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.938 SFLASH\_ALT\_PROT\_ROW75

Per Page Write Protection

Address: 0x0FFF44B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.939 SFLASH\_ALT\_PROT\_ROW76

Per Page Write Protection

Address: 0x0FFF44C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.940 SFLASH\_ALT\_PROT\_ROW77

Per Page Write Protection

Address: 0x0FFF44D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.941 SFLASH\_ALT\_PROT\_ROW78

Per Page Write Protection

Address: 0x0FFF44E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.942 SFLASH\_ALT\_PROT\_ROW79

Per Page Write Protection

Address: 0x0FFFF44F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.943 SFLASH\_ALT\_PROT\_ROW80

Per Page Write Protection

Address: 0x0FFF450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.944 SFLASH\_ALT\_PROT\_ROW81

Per Page Write Protection

Address: 0x0FFF451

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.945 SFLASH\_ALT\_PROT\_ROW82

Per Page Write Protection

Address: 0x0FFF452

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.946 SFLASH\_ALT\_PROT\_ROW83

Per Page Write Protection

Address: 0x0FFF453

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.947 SFLASH\_ALT\_PROT\_ROW84

Per Page Write Protection

Address: 0x0FFF454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.948 SFLASH\_ALT\_PROT\_ROW85

Per Page Write Protection

Address: 0x0FFF455

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.949 SFLASH\_ALT\_PROT\_ROW86

Per Page Write Protection

Address: 0x0FFF456

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.950 SFLASH\_ALT\_PROT\_ROW87

Per Page Write Protection

Address: 0x0FFF457

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.951 SFLASH\_ALT\_PROT\_ROW88

Per Page Write Protection

Address: 0x0FFF458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.952 SFLASH\_ALT\_PROT\_ROW89

Per Page Write Protection

Address: 0x0FFF459

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.953 SFLASH\_ALT\_PROT\_ROW90

Per Page Write Protection

Address: 0x0FFF45A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.954 SFLASH\_ALT\_PROT\_ROW91

Per Page Write Protection

Address: 0x0FFF45B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.955 SFLASH\_ALT\_PROT\_ROW92

Per Page Write Protection

Address: 0x0FFF45C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.956 SFLASH\_ALT\_PROT\_ROW93

Per Page Write Protection

Address: 0x0FFF45D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.957 SFLASH\_ALT\_PROT\_ROW94

Per Page Write Protection

Address: 0x0FFF45E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.958 SFLASH\_ALT\_PROT\_ROW95

Per Page Write Protection

Address: 0x0FFF45F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.959 SFLASH\_ALT\_PROT\_ROW96

Per Page Write Protection

Address: 0x0FFF460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.960 SFLASH\_ALT\_PROT\_ROW97

Per Page Write Protection

Address: 0x0FFF461

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.961 SFLASH\_ALT\_PROT\_ROW98

Per Page Write Protection

Address: 0x0FFF462

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.962 SFLASH\_ALT\_PROT\_ROW99

Per Page Write Protection

Address: 0x0FFF463

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.963 SFLASH\_ALT\_PROT\_ROW100

Per Page Write Protection

Address: 0x0FFF464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.964 SFLASH\_ALT\_PROT\_ROW101

Per Page Write Protection

Address: 0x0FFF465

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.965 SFLASH\_ALT\_PROT\_ROW102

Per Page Write Protection

Address: 0x0FFF466

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.966 SFLASH\_ALT\_PROT\_ROW103

Per Page Write Protection

Address: 0x0FFF467

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.967 SFLASH\_ALT\_PROT\_ROW104

Per Page Write Protection

Address: 0x0FFF468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.968 SFLASH\_ALT\_PROT\_ROW105

Per Page Write Protection

Address: 0x0FFF469

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.969 SFLASH\_ALT\_PROT\_ROW106

Per Page Write Protection

Address: 0x0FFF46A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.970 SFLASH\_ALT\_PROT\_ROW107

Per Page Write Protection

Address: 0x0FFF46B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.971 SFLASH\_ALT\_PROT\_ROW108

Per Page Write Protection

Address: 0x0FFF46C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.972 SFLASH\_ALT\_PROT\_ROW109

Per Page Write Protection

Address: 0x0FFF46D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.973 SFLASH\_ALT\_PROT\_ROW110

Per Page Write Protection

Address: 0x0FFF46E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.974 SFLASH\_ALT\_PROT\_ROW111

Per Page Write Protection

Address: 0x0FFF46F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.975 SFLASH\_ALT\_PROT\_ROW112

Per Page Write Protection

Address: 0x0FFF470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.976 SFLASH\_ALT\_PROT\_ROW113

Per Page Write Protection

Address: 0x0FFF471

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.977 SFLASH\_ALT\_PROT\_ROW114

Per Page Write Protection

Address: 0x0FFF472

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.978 SFLASH\_ALT\_PROT\_ROW115

Per Page Write Protection

Address: 0x0FFF473

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.979 SFLASH\_ALT\_PROT\_ROW116

Per Page Write Protection

Address: 0x0FFF474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.980 SFLASH\_ALT\_PROT\_ROW117

Per Page Write Protection

Address: 0x0FFF475

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.981 SFLASH\_ALT\_PROT\_ROW118

Per Page Write Protection

Address: 0x0FFF476

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.982 SFLASH\_ALT\_PROT\_ROW119

Per Page Write Protection

Address: 0x0FFF477

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.983 SFLASH\_ALT\_PROT\_ROW120

Per Page Write Protection

Address: 0x0FFF478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.984 SFLASH\_ALT\_PROT\_ROW121

Per Page Write Protection

Address: 0x0FFF479

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.985 SFLASH\_ALT\_PROT\_ROW122

Per Page Write Protection

Address: 0x0FFF47A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.986 SFLASH\_ALT\_PROT\_ROW123

Per Page Write Protection

Address: 0x0FFF47B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.987 SFLASH\_ALT\_PROT\_ROW124

Per Page Write Protection

Address: 0x0FFF47C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.988 SFLASH\_ALT\_PROT\_ROW125

Per Page Write Protection

Address: 0x0FFF47D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.989 SFLASH\_ALT\_PROT\_ROW126

Per Page Write Protection

Address: 0x0FFF47E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.990 SFLASH\_ALT\_PROT\_ROW127

Per Page Write Protection

Address: 0x0FFFF47F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.991 SFLASH\_ALT\_PROT\_ROW128

Per Page Write Protection

Address: 0x0FFF480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.992 SFLASH\_ALT\_PROT\_ROW129

Per Page Write Protection

Address: 0x0FFF481

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.993 SFLASH\_ALT\_PROT\_ROW130

Per Page Write Protection

Address: 0x0FFF482

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.994 SFLASH\_ALT\_PROT\_ROW131

Per Page Write Protection

Address: 0x0FFF483

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.995 SFLASH\_ALT\_PROT\_ROW132

Per Page Write Protection

Address: 0x0FFF484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.996 SFLASH\_ALT\_PROT\_ROW133

Per Page Write Protection

Address: 0x0FFF485

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.997 SFLASH\_ALT\_PROT\_ROW134

Per Page Write Protection

Address: 0x0FFF486

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.998 SFLASH\_ALT\_PROT\_ROW135

Per Page Write Protection

Address: 0x0FFF487

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.999 SFLASH\_ALT\_PROT\_ROW136

Per Page Write Protection

Address: 0x0FFF488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1000SFLASH\_ALT\_PROT\_ROW137

Per Page Write Protection

Address: 0x0FFF489

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1001SFLASH\_ALT\_PROT\_ROW138

Per Page Write Protection

Address: 0x0FFF48A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1002SFLASH\_ALT\_PROT\_ROW139

Per Page Write Protection

Address: 0x0FFF48B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1003SFLASH\_ALT\_PROT\_ROW140

Per Page Write Protection

Address: 0x0FFF48C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1004SFLASH\_ALT\_PROT\_ROW141

Per Page Write Protection

Address: 0x0FFF48D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1005SFLASH\_ALT\_PROT\_ROW142

Per Page Write Protection

Address: 0x0FFF48E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1006SFLASH\_ALT\_PROT\_ROW143

Per Page Write Protection

Address: 0x0FFF48F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1007SFLASH\_ALT\_PROT\_ROW144

Per Page Write Protection

Address: 0x0FFF490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1008SFLASH\_ALT\_PROT\_ROW145

Per Page Write Protection

Address: 0x0FFF491

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1009SFLASH\_ALT\_PROT\_ROW146

Per Page Write Protection

Address: 0x0FFF492

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1010SFLASH\_ALT\_PROT\_ROW147

Per Page Write Protection

Address: 0x0FFF493

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1011SFLASH\_ALT\_PROT\_ROW148

Per Page Write Protection

Address: 0x0FFF494

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1012SFLASH\_ALT\_PROT\_ROW149

Per Page Write Protection

Address: 0x0FFF495

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1013SFLASH\_ALT\_PROT\_ROW150

Per Page Write Protection

Address: 0x0FFF496

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1014SFLASH\_ALT\_PROT\_ROW151

Per Page Write Protection

Address: 0x0FFF497

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1015SFLASH\_ALT\_PROT\_ROW152

Per Page Write Protection

Address: 0x0FFF498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1016SFLASH\_ALT\_PROT\_ROW153

Per Page Write Protection

Address: 0x0FFF499

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1017SFLASH\_ALT\_PROT\_ROW154

Per Page Write Protection

Address: 0x0FFF49A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1018SFLASH\_ALT\_PROT\_ROW155

Per Page Write Protection

Address: 0x0FFF49B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1019SFLASH\_ALT\_PROT\_ROW156

Per Page Write Protection

Address: 0x0FFF49C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1020SFLASH\_ALT\_PROT\_ROW157

Per Page Write Protection

Address: 0x0FFF49D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1021SFLASH\_ALT\_PROT\_ROW158

Per Page Write Protection

Address: 0x0FFF49E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1022SFLASH\_ALT\_PROT\_ROW159

Per Page Write Protection

Address: 0x0FFF49F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1023SFLASH\_ALT\_PROT\_ROW160

Per Page Write Protection

Address: 0x0FFF4A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1024SFLASH\_ALT\_PROT\_ROW161

Per Page Write Protection

Address: 0x0FFF4A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1025SFLASH\_ALT\_PROT\_ROW162

Per Page Write Protection

Address: 0x0FFF4A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1026SFLASH\_ALT\_PROT\_ROW163

Per Page Write Protection

Address: 0x0FFF4A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1027SFLASH\_ALT\_PROT\_ROW164

Per Page Write Protection

Address: 0x0FFF4A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1028SFLASH\_ALT\_PROT\_ROW165

Per Page Write Protection

Address: 0x0FFF4A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1029SFLASH\_ALT\_PROT\_ROW166

Per Page Write Protection

Address: 0x0FFF4A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1030SFLASH\_ALT\_PROT\_ROW167

Per Page Write Protection

Address: 0x0FFF4A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1031SFLASH\_ALT\_PROT\_ROW168

Per Page Write Protection

Address: 0x0FFF4A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1032SFLASH\_ALT\_PROT\_ROW169

Per Page Write Protection

Address: 0x0FFF4A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1033SFLASH\_ALT\_PROT\_ROW170

Per Page Write Protection

Address: 0x0FFFF4AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1034SFLASH\_ALT\_PROT\_ROW171

Per Page Write Protection

Address: 0x0FFFF4AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1035SFLASH\_ALT\_PROT\_ROW172

Per Page Write Protection

Address: 0x0FFFF4AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1036SFLASH\_ALT\_PROT\_ROW173

Per Page Write Protection

Address: 0x0FFFF4AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1037SFLASH\_ALT\_PROT\_ROW174

Per Page Write Protection

Address: 0x0FFFF4AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1038SFLASH\_ALT\_PROT\_ROW175

Per Page Write Protection

Address: 0x0FFF4AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1039SFLASH\_ALT\_PROT\_ROW176

Per Page Write Protection

Address: 0x0FFF4B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1040SFLASH\_ALT\_PROT\_ROW177

Per Page Write Protection

Address: 0x0FFF4B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1041SFLASH\_ALT\_PROT\_ROW178

Per Page Write Protection

Address: 0x0FFF4B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1042SFLASH\_ALT\_PROT\_ROW179

Per Page Write Protection

Address: 0x0FFF4B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1043SFLASH\_ALT\_PROT\_ROW180

Per Page Write Protection

Address: 0x0FFF4B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1044SFLASH\_ALT\_PROT\_ROW181

Per Page Write Protection

Address: 0x0FFF4B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1045SFLASH\_ALT\_PROT\_ROW182

Per Page Write Protection

Address: 0x0FFF4B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1046SFLASH\_ALT\_PROT\_ROW183

Per Page Write Protection

Address: 0x0FFF4B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1047SFLASH\_ALT\_PROT\_ROW184

Per Page Write Protection

Address: 0x0FFF4B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1048SFLASH\_ALT\_PROT\_ROW185

Per Page Write Protection

Address: 0x0FFF4B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1049SFLASH\_ALT\_PROT\_ROW186

Per Page Write Protection

Address: 0x0FFFF4BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1050SFLASH\_ALT\_PROT\_ROW187

Per Page Write Protection

Address: 0x0FFFF4BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1051SFLASH\_ALT\_PROT\_ROW188

Per Page Write Protection

Address: 0x0FFFF4BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1052SFLASH\_ALT\_PROT\_ROW189

Per Page Write Protection

Address: 0x0FFFF4BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1053SFLASH\_ALT\_PROT\_ROW190

Per Page Write Protection

Address: 0x0FFFF4BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1054SFLASH\_ALT\_PROT\_ROW191

Per Page Write Protection

Address: 0x0FFF4BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1055SFLASH\_ALT\_PROT\_ROW192

Per Page Write Protection

Address: 0x0FFFF4C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1056SFLASH\_ALT\_PROT\_ROW193

Per Page Write Protection

Address: 0x0FFFF4C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1057SFLASH\_ALT\_PROT\_ROW194

Per Page Write Protection

Address: 0x0FFF4C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1058SFLASH\_ALT\_PROT\_ROW195

Per Page Write Protection

Address: 0x0FFF4C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1059SFLASH\_ALT\_PROT\_ROW196

Per Page Write Protection

Address: 0x0FFFF4C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1060SFLASH\_ALT\_PROT\_ROW197

Per Page Write Protection

Address: 0x0FFF4C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1061SFLASH\_ALT\_PROT\_ROW198

Per Page Write Protection

Address: 0x0FFF4C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1062SFLASH\_ALT\_PROT\_ROW199

Per Page Write Protection

Address: 0x0FFFF4C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1063SFLASH\_ALT\_PROT\_ROW200

Per Page Write Protection

Address: 0x0FFF4C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1064SFLASH\_ALT\_PROT\_ROW201

Per Page Write Protection

Address: 0x0FFFF4C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1065SFLASH\_ALT\_PROT\_ROW202

Per Page Write Protection

Address: 0x0FFFF4CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1066SFLASH\_ALT\_PROT\_ROW203

Per Page Write Protection

Address: 0x0FFFF4CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1067SFLASH\_ALT\_PROT\_ROW204

Per Page Write Protection

Address: 0x0FFFF4CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1068SFLASH\_ALT\_PROT\_ROW205

Per Page Write Protection

Address: 0x0FFFF4CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1069SFLASH\_ALT\_PROT\_ROW206

Per Page Write Protection

Address: 0x0FFFF4CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1070SFLASH\_ALT\_PROT\_ROW207

Per Page Write Protection

Address: 0x0FFFF4CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1071SFLASH\_ALT\_PROT\_ROW208

Per Page Write Protection

Address: 0x0FFF4D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1072SFLASH\_ALT\_PROT\_ROW209

Per Page Write Protection

Address: 0x0FFFF4D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1073SFLASH\_ALT\_PROT\_ROW210

Per Page Write Protection

Address: 0x0FFFF4D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1074SFLASH\_ALT\_PROT\_ROW211

Per Page Write Protection

Address: 0x0FFF4D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1075SFLASH\_ALT\_PROT\_ROW212

Per Page Write Protection

Address: 0x0FFF4D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1076SFLASH\_ALT\_PROT\_ROW213

Per Page Write Protection

Address: 0x0FFF4D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1077SFLASH\_ALT\_PROT\_ROW214

Per Page Write Protection

Address: 0x0FFF4D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1078SFLASH\_ALT\_PROT\_ROW215

Per Page Write Protection

Address: 0x0FFF4D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1079SFLASH\_ALT\_PROT\_ROW216

Per Page Write Protection

Address: 0x0FFFF4D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1080SFLASH\_ALT\_PROT\_ROW217

Per Page Write Protection

Address: 0x0FFF4D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1081SFLASH\_ALT\_PROT\_ROW218

Per Page Write Protection

Address: 0x0FFFF4DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1082SFLASH\_ALT\_PROT\_ROW219

Per Page Write Protection

Address: 0x0FFFF4DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1083SFLASH\_ALT\_PROT\_ROW220

Per Page Write Protection

Address: 0x0FFFF4DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1084SFLASH\_ALT\_PROT\_ROW221

Per Page Write Protection

Address: 0x0FFFF4DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1085SFLASH\_ALT\_PROT\_ROW222

Per Page Write Protection

Address: 0x0FFFF4DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1086SFLASH\_ALT\_PROT\_ROW223

Per Page Write Protection

Address: 0x0FFFF4DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1087SFLASH\_ALT\_PROT\_ROW224

Per Page Write Protection

Address: 0x0FFF4E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1088SFLASH\_ALT\_PROT\_ROW225

Per Page Write Protection

Address: 0x0FFF4E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1089SFLASH\_ALT\_PROT\_ROW226

Per Page Write Protection

Address: 0x0FFF4E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1090SFLASH\_ALT\_PROT\_ROW227

Per Page Write Protection

Address: 0x0FFF4E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1091SFLASH\_ALT\_PROT\_ROW228

Per Page Write Protection

Address: 0x0FFF4E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1092SFLASH\_ALT\_PROT\_ROW229

Per Page Write Protection

Address: 0x0FFF4E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1093SFLASH\_ALT\_PROT\_ROW230

Per Page Write Protection

Address: 0x0FFF4E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1094SFLASH\_ALT\_PROT\_ROW231

Per Page Write Protection

Address: 0x0FFF4E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1095SFLASH\_ALT\_PROT\_ROW232

Per Page Write Protection

Address: 0x0FFF4E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1096SFLASH\_ALT\_PROT\_ROW233

Per Page Write Protection

Address: 0x0FFF4E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1097SFLASH\_ALT\_PROT\_ROW234

Per Page Write Protection

Address: 0x0FFFF4EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1098SFLASH\_ALT\_PROT\_ROW235

Per Page Write Protection

Address: 0x0FFFF4EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1099SFLASH\_ALT\_PROT\_ROW236

Per Page Write Protection

Address: 0x0FFFF4EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1100SFLASH\_ALT\_PROT\_ROW237

Per Page Write Protection

Address: 0x0FFFF4ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1101SFLASH\_ALT\_PROT\_ROW238

Per Page Write Protection

Address: 0x0FFFF4EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1102SFLASH\_ALT\_PROT\_ROW239

Per Page Write Protection

Address: 0x0FFF4EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1103SFLASH\_ALT\_PROT\_ROW240

Per Page Write Protection

Address: 0x0FFF4F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1104SFLASH\_ALT\_PROT\_ROW241

Per Page Write Protection

Address: 0x0FFF4F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1105SFLASH\_ALT\_PROT\_ROW242

Per Page Write Protection

Address: 0x0FFF4F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1106SFLASH\_ALT\_PROT\_ROW243

Per Page Write Protection

Address: 0x0FFF4F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1107SFLASH\_ALT\_PROT\_ROW244

Per Page Write Protection

Address: 0x0FFFF4F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1108SFLASH\_ALT\_PROT\_ROW245

Per Page Write Protection

Address: 0x0FFF4F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1109SFLASH\_ALT\_PROT\_ROW246

Per Page Write Protection

Address: 0x0FFF4F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1110SFLASH\_ALT\_PROT\_ROW247

Per Page Write Protection

Address: 0x0FFF4F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1111 SFLASH\_ALT\_PROT\_ROW248

Per Page Write Protection

Address: 0x0FFF4F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1112SFLASH\_ALT\_PROT\_ROW249

Per Page Write Protection

Address: 0x0FFF4F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1113SFLASH\_ALT\_PROT\_ROW250

Per Page Write Protection

Address: 0x0FFFF4FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1114SFLASH\_ALT\_PROT\_ROW251

Per Page Write Protection

Address: 0x0FFFF4FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1115SFLASH\_ALT\_PROT\_ROW252

Per Page Write Protection

Address: 0x0FFFF4FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1116SFLASH\_ALT\_PROT\_ROW253

Per Page Write Protection

Address: 0x0FFFF4FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1117SFLASH\_ALT\_PROT\_ROW254

Per Page Write Protection

Address: 0x0FFFF4FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 21.1.1118SFLASH\_ALT\_PROT\_ROW255

Per Page Write Protection

Address: 0x0FFFF4FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 21.1.1119SFLASH\_ALT\_PP

Preprogram Settings

Address: 0x0FFF5A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.1120SFLASH\_ALT\_E

Erase Settings

Address: 0x0FFF5A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.1121SFLASH\_ALT\_P

Program Settings

Address: 0x0FFF5A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.1122SFLASH\_ALT\_EA\_E

Erase All - Erase Settings

Address: 0x0FFFF5AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.1123SFLASH\_ALT\_EA\_P

Erase All - Program Settings

Address: 0x0FFF5B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.1124SFLASH\_ALT\_ES\_E

Erase Sector - Erase Settings

Address: 0x0FFF5B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.1125SFLASH\_ALT\_ES\_P\_EO

Erase Sector - Program EO Settings

Address: 0x0FFF5B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_specif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 21.1.1126SFLASH\_ALT\_E\_VCTAT

Bandgap Trim Register

Address: 0x0FFFF5BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X



## 21.1.1127SFLASH\_ALT\_P\_VCTAT

Bandgap Trim Register

Address: 0x0FFFF5BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

## 22 Supervisory Flash (256 KB) Registers



This section discusses the Supervisory Flash (SFLASH) registers for 256 KB devices. It lists all the registers in mapping tables, in address order.

### 22.1 Register Details

Register Name	Address
<a href="#">SFLASH_PROT_ROW0</a>	0x0FFFF000
<a href="#">SFLASH_PROT_ROW1</a>	0x0FFFF001
<a href="#">SFLASH_PROT_ROW2</a>	0x0FFFF002
<a href="#">SFLASH_PROT_ROW3</a>	0x0FFFF003
<a href="#">SFLASH_PROT_ROW4</a>	0x0FFFF004
<a href="#">SFLASH_PROT_ROW5</a>	0x0FFFF005
<a href="#">SFLASH_PROT_ROW6</a>	0x0FFFF006
<a href="#">SFLASH_PROT_ROW7</a>	0x0FFFF007
<a href="#">SFLASH_PROT_ROW8</a>	0x0FFFF008
<a href="#">SFLASH_PROT_ROW9</a>	0x0FFFF009
<a href="#">SFLASH_PROT_ROW10</a>	0x0FFFF00A
<a href="#">SFLASH_PROT_ROW11</a>	0x0FFFF00B
<a href="#">SFLASH_PROT_ROW12</a>	0x0FFFF00C
<a href="#">SFLASH_PROT_ROW13</a>	0x0FFFF00D
<a href="#">SFLASH_PROT_ROW14</a>	0x0FFFF00E
<a href="#">SFLASH_PROT_ROW15</a>	0x0FFFF00F
<a href="#">SFLASH_PROT_ROW16</a>	0x0FFFF010
<a href="#">SFLASH_PROT_ROW17</a>	0x0FFFF011
<a href="#">SFLASH_PROT_ROW18</a>	0x0FFFF012
<a href="#">SFLASH_PROT_ROW19</a>	0x0FFFF013
<a href="#">SFLASH_PROT_ROW20</a>	0x0FFFF014
<a href="#">SFLASH_PROT_ROW21</a>	0x0FFFF015
<a href="#">SFLASH_PROT_ROW22</a>	0x0FFFF016
<a href="#">SFLASH_PROT_ROW23</a>	0x0FFFF017
<a href="#">SFLASH_PROT_ROW24</a>	0x0FFFF018
<a href="#">SFLASH_PROT_ROW25</a>	0x0FFFF019
<a href="#">SFLASH_PROT_ROW26</a>	0x0FFFF01A

Register Name	Address
SFLASH_PROT_ROW27	0x0FFF01B
SFLASH_PROT_ROW28	0x0FFF01C
SFLASH_PROT_ROW29	0x0FFF01D
SFLASH_PROT_ROW30	0x0FFF01E
SFLASH_PROT_ROW31	0x0FFF01F
SFLASH_PROT_ROW32	0x0FFF020
SFLASH_PROT_ROW33	0x0FFF021
SFLASH_PROT_ROW34	0x0FFF022
SFLASH_PROT_ROW35	0x0FFF023
SFLASH_PROT_ROW36	0x0FFF024
SFLASH_PROT_ROW37	0x0FFF025
SFLASH_PROT_ROW38	0x0FFF026
SFLASH_PROT_ROW39	0x0FFF027
SFLASH_PROT_ROW40	0x0FFF028
SFLASH_PROT_ROW41	0x0FFF029
SFLASH_PROT_ROW42	0x0FFF02A
SFLASH_PROT_ROW43	0x0FFF02B
SFLASH_PROT_ROW44	0x0FFF02C
SFLASH_PROT_ROW45	0x0FFF02D
SFLASH_PROT_ROW46	0x0FFF02E
SFLASH_PROT_ROW47	0x0FFF02F
SFLASH_PROT_ROW48	0x0FFF030
SFLASH_PROT_ROW49	0x0FFF031
SFLASH_PROT_ROW50	0x0FFF032
SFLASH_PROT_ROW51	0x0FFF033
SFLASH_PROT_ROW52	0x0FFF034
SFLASH_PROT_ROW53	0x0FFF035
SFLASH_PROT_ROW54	0x0FFF036
SFLASH_PROT_ROW55	0x0FFF037
SFLASH_PROT_ROW56	0x0FFF038
SFLASH_PROT_ROW57	0x0FFF039
SFLASH_PROT_ROW58	0x0FFF03A
SFLASH_PROT_ROW59	0x0FFF03B
SFLASH_PROT_ROW60	0x0FFF03C
SFLASH_PROT_ROW61	0x0FFF03D
SFLASH_PROT_ROW62	0x0FFF03E
SFLASH_PROT_ROW63	0x0FFF03F
SFLASH_PROT_PROTECTION	0x0FFF0FF
SFLASH_AV_PAIRS_8B0	0x0FFF100
SFLASH_AV_PAIRS_8B1	0x0FFF101
SFLASH_AV_PAIRS_8B2	0x0FFF102
SFLASH_AV_PAIRS_8B3	0x0FFF103

Register Name	Address
SFLASH_AV_PAIRS_8B4	0x0FFF104
SFLASH_AV_PAIRS_8B5	0x0FFF105
SFLASH_AV_PAIRS_8B6	0x0FFF106
SFLASH_AV_PAIRS_8B7	0x0FFF107
SFLASH_AV_PAIRS_8B8	0x0FFF108
SFLASH_AV_PAIRS_8B9	0x0FFF109
SFLASH_AV_PAIRS_8B10	0x0FFF10A
SFLASH_AV_PAIRS_8B11	0x0FFF10B
SFLASH_AV_PAIRS_8B12	0x0FFF10C
SFLASH_AV_PAIRS_8B13	0x0FFF10D
SFLASH_AV_PAIRS_8B14	0x0FFF10E
SFLASH_AV_PAIRS_8B15	0x0FFF10F
SFLASH_AV_PAIRS_8B16	0x0FFF110
SFLASH_AV_PAIRS_8B17	0x0FFF111
SFLASH_AV_PAIRS_8B18	0x0FFF112
SFLASH_AV_PAIRS_8B19	0x0FFF113
SFLASH_AV_PAIRS_8B20	0x0FFF114
SFLASH_AV_PAIRS_8B21	0x0FFF115
SFLASH_AV_PAIRS_8B22	0x0FFF116
SFLASH_AV_PAIRS_8B23	0x0FFF117
SFLASH_AV_PAIRS_8B24	0x0FFF118
SFLASH_AV_PAIRS_8B25	0x0FFF119
SFLASH_AV_PAIRS_8B26	0x0FFF11A
SFLASH_AV_PAIRS_8B27	0x0FFF11B
SFLASH_AV_PAIRS_8B28	0x0FFF11C
SFLASH_AV_PAIRS_8B29	0x0FFF11D
SFLASH_AV_PAIRS_8B30	0x0FFF11E
SFLASH_AV_PAIRS_8B31	0x0FFF11F
SFLASH_AV_PAIRS_8B32	0x0FFF120
SFLASH_AV_PAIRS_8B33	0x0FFF121
SFLASH_AV_PAIRS_8B34	0x0FFF122
SFLASH_AV_PAIRS_8B35	0x0FFF123
SFLASH_AV_PAIRS_8B36	0x0FFF124
SFLASH_AV_PAIRS_8B37	0x0FFF125
SFLASH_AV_PAIRS_8B38	0x0FFF126
SFLASH_AV_PAIRS_8B39	0x0FFF127
SFLASH_AV_PAIRS_8B40	0x0FFF128
SFLASH_AV_PAIRS_8B41	0x0FFF129
SFLASH_AV_PAIRS_8B42	0x0FFF12A
SFLASH_AV_PAIRS_8B43	0x0FFF12B
SFLASH_AV_PAIRS_8B44	0x0FFF12C
SFLASH_AV_PAIRS_8B45	0x0FFF12D

Register Name	Address
SFLASH_AV_PAIRS_8B46	0x0FFF12E
SFLASH_AV_PAIRS_8B47	0x0FFF12F
SFLASH_AV_PAIRS_8B48	0x0FFF130
SFLASH_AV_PAIRS_8B49	0x0FFF131
SFLASH_AV_PAIRS_8B50	0x0FFF132
SFLASH_AV_PAIRS_8B51	0x0FFF133
SFLASH_AV_PAIRS_8B52	0x0FFF134
SFLASH_AV_PAIRS_8B53	0x0FFF135
SFLASH_AV_PAIRS_8B54	0x0FFF136
SFLASH_AV_PAIRS_8B55	0x0FFF137
SFLASH_AV_PAIRS_8B56	0x0FFF138
SFLASH_AV_PAIRS_8B57	0x0FFF139
SFLASH_AV_PAIRS_8B58	0x0FFF13A
SFLASH_AV_PAIRS_8B59	0x0FFF13B
SFLASH_AV_PAIRS_8B60	0x0FFF13C
SFLASH_AV_PAIRS_8B61	0x0FFF13D
SFLASH_AV_PAIRS_8B62	0x0FFF13E
SFLASH_AV_PAIRS_8B63	0x0FFF13F
SFLASH_AV_PAIRS_8B64	0x0FFF140
SFLASH_AV_PAIRS_8B65	0x0FFF141
SFLASH_AV_PAIRS_8B66	0x0FFF142
SFLASH_AV_PAIRS_8B67	0x0FFF143
SFLASH_AV_PAIRS_8B68	0x0FFF144
SFLASH_AV_PAIRS_8B69	0x0FFF145
SFLASH_AV_PAIRS_8B70	0x0FFF146
SFLASH_AV_PAIRS_8B71	0x0FFF147
SFLASH_AV_PAIRS_8B72	0x0FFF148
SFLASH_AV_PAIRS_8B73	0x0FFF149
SFLASH_AV_PAIRS_8B74	0x0FFF14A
SFLASH_AV_PAIRS_8B75	0x0FFF14B
SFLASH_AV_PAIRS_8B76	0x0FFF14C
SFLASH_AV_PAIRS_8B77	0x0FFF14D
SFLASH_AV_PAIRS_8B78	0x0FFF14E
SFLASH_AV_PAIRS_8B79	0x0FFF14F
SFLASH_AV_PAIRS_8B80	0x0FFF150
SFLASH_AV_PAIRS_8B81	0x0FFF151
SFLASH_AV_PAIRS_8B82	0x0FFF152
SFLASH_AV_PAIRS_8B83	0x0FFF153
SFLASH_AV_PAIRS_8B84	0x0FFF154
SFLASH_AV_PAIRS_8B85	0x0FFF155
SFLASH_AV_PAIRS_8B86	0x0FFF156
SFLASH_AV_PAIRS_8B87	0x0FFF157

Register Name	Address
SFLASH_BLESS_BB_BUMP2	0x0FFF158
SFLASH_AV_PAIRS_8B88	0x0FFF158
SFLASH_AV_PAIRS_8B89	0x0FFF159
SFLASH_BLESS_BB_XO	0x0FFF15A
SFLASH_AV_PAIRS_8B90	0x0FFF15A
SFLASH_AV_PAIRS_8B91	0x0FFF15B
SFLASH_BLESS_SY_BUMP1	0x0FFF15C
SFLASH_AV_PAIRS_8B92	0x0FFF15C
SFLASH_AV_PAIRS_8B93	0x0FFF15D
SFLASH_BLESS_LDO	0x0FFF15E
SFLASH_AV_PAIRS_8B94	0x0FFF15E
SFLASH_AV_PAIRS_8B95	0x0FFF15F
SFLASH_AV_PAIRS_8B96	0x0FFF160
SFLASH_AV_PAIRS_8B97	0x0FFF161
SFLASH_AV_PAIRS_8B98	0x0FFF162
SFLASH_AV_PAIRS_8B99	0x0FFF163
SFLASH_AV_PAIRS_8B100	0x0FFF164
SFLASH_AV_PAIRS_8B101	0x0FFF165
SFLASH_AV_PAIRS_8B102	0x0FFF166
SFLASH_AV_PAIRS_8B103	0x0FFF167
SFLASH_AV_PAIRS_8B104	0x0FFF168
SFLASH_AV_PAIRS_8B105	0x0FFF169
SFLASH_AV_PAIRS_8B106	0x0FFF16A
SFLASH_AV_PAIRS_8B107	0x0FFF16B
SFLASH_AV_PAIRS_8B108	0x0FFF16C
SFLASH_AV_PAIRS_8B109	0x0FFF16D
SFLASH_AV_PAIRS_8B110	0x0FFF16E
SFLASH_AV_PAIRS_8B111	0x0FFF16F
SFLASH_AV_PAIRS_8B112	0x0FFF170
SFLASH_AV_PAIRS_8B113	0x0FFF171
SFLASH_AV_PAIRS_8B114	0x0FFF172
SFLASH_AV_PAIRS_8B115	0x0FFF173
SFLASH_AV_PAIRS_8B116	0x0FFF174
SFLASH_AV_PAIRS_8B117	0x0FFF175
SFLASH_AV_PAIRS_8B118	0x0FFF176
SFLASH_AV_PAIRS_8B119	0x0FFF177
SFLASH_AV_PAIRS_8B120	0x0FFF178
SFLASH_AV_PAIRS_8B121	0x0FFF179
SFLASH_AV_PAIRS_8B122	0x0FFF17A
SFLASH_AV_PAIRS_8B123	0x0FFF17B
SFLASH_AV_PAIRS_8B124	0x0FFF17C
SFLASH_AV_PAIRS_8B125	0x0FFF17D

Register Name	Address
SFLASH_AV_PAIRS_8B126	0x0FFF17E
SFLASH_AV_PAIRS_8B127	0x0FFF17F
SFLASH_AV_PAIRS_32B0	0x0FFF200
SFLASH_AV_PAIRS_32B1	0x0FFF204
SFLASH_AV_PAIRS_32B2	0x0FFF208
SFLASH_AV_PAIRS_32B3	0x0FFF20C
SFLASH_AV_PAIRS_32B4	0x0FFF210
SFLASH_AV_PAIRS_32B5	0x0FFF214
SFLASH_AV_PAIRS_32B6	0x0FFF218
SFLASH_AV_PAIRS_32B7	0x0FFF21C
SFLASH_AV_PAIRS_32B8	0x0FFF220
SFLASH_AV_PAIRS_32B9	0x0FFF224
SFLASH_AV_PAIRS_32B10	0x0FFF228
SFLASH_AV_PAIRS_32B11	0x0FFF22C
SFLASH_AV_PAIRS_32B12	0x0FFF230
SFLASH_AV_PAIRS_32B13	0x0FFF234
SFLASH_AV_PAIRS_32B14	0x0FFF238
SFLASH_AV_PAIRS_32B15	0x0FFF23C
SFLASH_CPUS_WOUNDING	0x0FFF240
SFLASH_SILICON_ID	0x0FFF244
SFLASH_CPUS_PRIV_RAM	0x0FFF248
SFLASH_CPUS_PRIV_ROM_BROM	0x0FFF24A
SFLASH_CPUS_PRIV_FLASH	0x0FFF24C
SFLASH_CPUS_PRIV_ROM_SROM	0x0FFF24E
SFLASH_HIB_KEY_DELAY	0x0FFF250
SFLASH_DPSLP_KEY_DELAY	0x0FFF252
SFLASH_SWD_CONFIG	0x0FFF254
SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0	0x0FFF255
SFLASH_SWD_LISTEN	0x0FFF258
SFLASH_FLASH_START	0x0FFF25C
SFLASH_CSD_TRIM1_HVIDAC	0x0FFF260
SFLASH_CSD_TRIM2_HVIDAC	0x0FFF261
SFLASH_CSD_TRIM1_CSD	0x0FFF262
SFLASH_CSD_TRIM2_CSD	0x0FFF263
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFF264
SFLASH_SAR_TEMP_OFFSET	0x0FFF266
SFLASH_SKIP_CHECKSUM	0x0FFF269
SFLASH_PROT_VIRGINKEY0	0x0FFF270
SFLASH_PROT_VIRGINKEY1	0x0FFF271
SFLASH_PROT_VIRGINKEY2	0x0FFF272
SFLASH_PROT_VIRGINKEY3	0x0FFF273
SFLASH_PROT_VIRGINKEY4	0x0FFF274

Register Name	Address
SFLASH_PROT_VIRGINKEY5	0x0FFF275
SFLASH_PROT_VIRGINKEY6	0x0FFF276
SFLASH_PROT_VIRGINKEY7	0x0FFF277
SFLASH_DIE_LOT0	0x0FFF278
SFLASH_DIE_LOT1	0x0FFF279
SFLASH_DIE_LOT2	0x0FFF27A
SFLASH_DIE_WAFER	0x0FFF27B
SFLASH_DIE_X	0x0FFF27C
SFLASH_DIE_Y	0x0FFF27D
SFLASH_DIE_SORT	0x0FFF27E
SFLASH_DIE_MINOR	0x0FFF27F
SFLASH_PE_TE_DATA0	0x0FFF300
SFLASH_PE_TE_DATA1	0x0FFF301
SFLASH_PE_TE_DATA2	0x0FFF302
SFLASH_PE_TE_DATA3	0x0FFF303
SFLASH_PE_TE_DATA4	0x0FFF304
SFLASH_PE_TE_DATA5	0x0FFF305
SFLASH_PE_TE_DATA6	0x0FFF306
SFLASH_PE_TE_DATA7	0x0FFF307
SFLASH_PE_TE_DATA8	0x0FFF308
SFLASH_PE_TE_DATA9	0x0FFF309
SFLASH_PE_TE_DATA10	0x0FFF30A
SFLASH_PE_TE_DATA11	0x0FFF30B
SFLASH_PE_TE_DATA12	0x0FFF30C
SFLASH_PE_TE_DATA13	0x0FFF30D
SFLASH_PE_TE_DATA14	0x0FFF30E
SFLASH_PE_TE_DATA15	0x0FFF30F
SFLASH_PE_TE_DATA16	0x0FFF310
SFLASH_PE_TE_DATA17	0x0FFF311
SFLASH_PE_TE_DATA18	0x0FFF312
SFLASH_PE_TE_DATA19	0x0FFF313
SFLASH_PE_TE_DATA20	0x0FFF314
SFLASH_PE_TE_DATA21	0x0FFF315
SFLASH_PE_TE_DATA22	0x0FFF316
SFLASH_PE_TE_DATA23	0x0FFF317
SFLASH_PE_TE_DATA24	0x0FFF318
SFLASH_PE_TE_DATA25	0x0FFF319
SFLASH_PE_TE_DATA26	0x0FFF31A
SFLASH_PE_TE_DATA27	0x0FFF31B
SFLASH_PE_TE_DATA28	0x0FFF31C
SFLASH_PE_TE_DATA29	0x0FFF31D
SFLASH_PE_TE_DATA30	0x0FFF31E



Register Name	Address
SFLASH_PE_TE_DATA31	0x0FFF31F
SFLASH_PP	0x0FFF320
SFLASH_E	0x0FFF324
SFLASH_P	0x0FFF328
SFLASH_EA_E	0x0FFF32C
SFLASH_EA_P	0x0FFF330
SFLASH_ES_E	0x0FFF334
SFLASH_ES_P_EO	0x0FFF338
SFLASH_E_VCTAT	0x0FFF33C
SFLASH_P_VCTAT	0x0FFF33D
SFLASH_IMO_MAXF0	0x0FFF340
SFLASH_IMO_ABS0	0x0FFF341
SFLASH_IMO_TMPCO0	0x0FFF342
SFLASH_IMO_MAXF1	0x0FFF343
SFLASH_IMO_ABS1	0x0FFF344
SFLASH_IMO_TMPCO1	0x0FFF345
SFLASH_IMO_MAXF2	0x0FFF346
SFLASH_IMO_ABS2	0x0FFF347
SFLASH_IMO_TMPCO2	0x0FFF348
SFLASH_IMO_MAXF3	0x0FFF349
SFLASH_IMO_ABS3	0x0FFF34A
SFLASH_IMO_TMPCO3	0x0FFF34B
SFLASH_IMO_ABS4	0x0FFF34C
SFLASH_IMO_TMPCO4	0x0FFF34D
SFLASH_IMO_TRIM0	0x0FFF350
SFLASH_IMO_TRIM1	0x0FFF351
SFLASH_IMO_TRIM2	0x0FFF352
SFLASH_IMO_TRIM3	0x0FFF353
SFLASH_IMO_TRIM4	0x0FFF354
SFLASH_IMO_TRIM5	0x0FFF355
SFLASH_IMO_TRIM6	0x0FFF356
SFLASH_IMO_TRIM7	0x0FFF357
SFLASH_IMO_TRIM8	0x0FFF358
SFLASH_IMO_TRIM9	0x0FFF359
SFLASH_IMO_TRIM10	0x0FFF35A
SFLASH_IMO_TRIM11	0x0FFF35B
SFLASH_IMO_TRIM12	0x0FFF35C
SFLASH_IMO_TRIM13	0x0FFF35D
SFLASH_IMO_TRIM14	0x0FFF35E
SFLASH_IMO_TRIM15	0x0FFF35F
SFLASH_IMO_TRIM16	0x0FFF360
SFLASH_IMO_TRIM17	0x0FFF361

Register Name	Address
SFLASH_IMO_TRIM18	0x0FFF362
SFLASH_IMO_TRIM19	0x0FFF363
SFLASH_IMO_TRIM20	0x0FFF364
SFLASH_IMO_TRIM21	0x0FFF365
SFLASH_IMO_TRIM22	0x0FFF366
SFLASH_IMO_TRIM23	0x0FFF367
SFLASH_IMO_TRIM24	0x0FFF368
SFLASH_IMO_TRIM25	0x0FFF369
SFLASH_IMO_TRIM26	0x0FFF36A
SFLASH_IMO_TRIM27	0x0FFF36B
SFLASH_IMO_TRIM28	0x0FFF36C
SFLASH_IMO_TRIM29	0x0FFF36D
SFLASH_IMO_TRIM30	0x0FFF36E
SFLASH_IMO_TRIM31	0x0FFF36F
SFLASH_IMO_TRIM32	0x0FFF370
SFLASH_IMO_TRIM33	0x0FFF371
SFLASH_IMO_TRIM34	0x0FFF372
SFLASH_IMO_TRIM35	0x0FFF373
SFLASH_IMO_TRIM36	0x0FFF374
SFLASH_IMO_TRIM37	0x0FFF375
SFLASH_IMO_TRIM38	0x0FFF376
SFLASH_IMO_TRIM39	0x0FFF377
SFLASH_IMO_TRIM40	0x0FFF378
SFLASH_IMO_TRIM41	0x0FFF379
SFLASH_IMO_TRIM42	0x0FFF37A
SFLASH_IMO_TRIM43	0x0FFF37B
SFLASH_IMO_TRIM44	0x0FFF37C
SFLASH_IMO_TRIM45	0x0FFF37D
SFLASH_CHECKSUM	0x0FFF3FE
SFLASH_MACRO_0_FREE_SFLASH0	0x0FFF400
SFLASH_MACRO_0_FREE_SFLASH1	0x0FFF401
SFLASH_MACRO_0_FREE_SFLASH2	0x0FFF402
SFLASH_MACRO_0_FREE_SFLASH3	0x0FFF403
SFLASH_MACRO_0_FREE_SFLASH4	0x0FFF404
SFLASH_MACRO_0_FREE_SFLASH5	0x0FFF405
SFLASH_MACRO_0_FREE_SFLASH6	0x0FFF406
SFLASH_MACRO_0_FREE_SFLASH7	0x0FFF407
SFLASH_MACRO_0_FREE_SFLASH8	0x0FFF408
SFLASH_MACRO_0_FREE_SFLASH9	0x0FFF409
SFLASH_MACRO_0_FREE_SFLASH10	0x0FFF40A
SFLASH_MACRO_0_FREE_SFLASH11	0x0FFF40B
SFLASH_MACRO_0_FREE_SFLASH12	0x0FFF40C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH13	0x0FFF40D
SFLASH_MACRO_0_FREE_SFLASH14	0x0FFF40E
SFLASH_MACRO_0_FREE_SFLASH15	0x0FFF40F
SFLASH_MACRO_0_FREE_SFLASH16	0x0FFF410
SFLASH_MACRO_0_FREE_SFLASH17	0x0FFF411
SFLASH_MACRO_0_FREE_SFLASH18	0x0FFF412
SFLASH_MACRO_0_FREE_SFLASH19	0x0FFF413
SFLASH_MACRO_0_FREE_SFLASH20	0x0FFF414
SFLASH_MACRO_0_FREE_SFLASH21	0x0FFF415
SFLASH_MACRO_0_FREE_SFLASH22	0x0FFF416
SFLASH_MACRO_0_FREE_SFLASH23	0x0FFF417
SFLASH_MACRO_0_FREE_SFLASH24	0x0FFF418
SFLASH_MACRO_0_FREE_SFLASH25	0x0FFF419
SFLASH_MACRO_0_FREE_SFLASH26	0x0FFF41A
SFLASH_MACRO_0_FREE_SFLASH27	0x0FFF41B
SFLASH_MACRO_0_FREE_SFLASH28	0x0FFF41C
SFLASH_MACRO_0_FREE_SFLASH29	0x0FFF41D
SFLASH_MACRO_0_FREE_SFLASH30	0x0FFF41E
SFLASH_MACRO_0_FREE_SFLASH31	0x0FFF41F
SFLASH_MACRO_0_FREE_SFLASH32	0x0FFF420
SFLASH_MACRO_0_FREE_SFLASH33	0x0FFF421
SFLASH_MACRO_0_FREE_SFLASH34	0x0FFF422
SFLASH_MACRO_0_FREE_SFLASH35	0x0FFF423
SFLASH_MACRO_0_FREE_SFLASH36	0x0FFF424
SFLASH_MACRO_0_FREE_SFLASH37	0x0FFF425
SFLASH_MACRO_0_FREE_SFLASH38	0x0FFF426
SFLASH_MACRO_0_FREE_SFLASH39	0x0FFF427
SFLASH_MACRO_0_FREE_SFLASH40	0x0FFF428
SFLASH_MACRO_0_FREE_SFLASH41	0x0FFF429
SFLASH_MACRO_0_FREE_SFLASH42	0x0FFF42A
SFLASH_MACRO_0_FREE_SFLASH43	0x0FFF42B
SFLASH_MACRO_0_FREE_SFLASH44	0x0FFF42C
SFLASH_MACRO_0_FREE_SFLASH45	0x0FFF42D
SFLASH_MACRO_0_FREE_SFLASH46	0x0FFF42E
SFLASH_MACRO_0_FREE_SFLASH47	0x0FFF42F
SFLASH_MACRO_0_FREE_SFLASH48	0x0FFF430
SFLASH_MACRO_0_FREE_SFLASH49	0x0FFF431
SFLASH_MACRO_0_FREE_SFLASH50	0x0FFF432
SFLASH_MACRO_0_FREE_SFLASH51	0x0FFF433
SFLASH_MACRO_0_FREE_SFLASH52	0x0FFF434
SFLASH_MACRO_0_FREE_SFLASH53	0x0FFF435
SFLASH_MACRO_0_FREE_SFLASH54	0x0FFF436

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH55	0x0FFF437
SFLASH_MACRO_0_FREE_SFLASH56	0x0FFF438
SFLASH_MACRO_0_FREE_SFLASH57	0x0FFF439
SFLASH_MACRO_0_FREE_SFLASH58	0x0FFF43A
SFLASH_MACRO_0_FREE_SFLASH59	0x0FFF43B
SFLASH_MACRO_0_FREE_SFLASH60	0x0FFF43C
SFLASH_MACRO_0_FREE_SFLASH61	0x0FFF43D
SFLASH_MACRO_0_FREE_SFLASH62	0x0FFF43E
SFLASH_MACRO_0_FREE_SFLASH63	0x0FFF43F
SFLASH_MACRO_0_FREE_SFLASH64	0x0FFF440
SFLASH_MACRO_0_FREE_SFLASH65	0x0FFF441
SFLASH_MACRO_0_FREE_SFLASH66	0x0FFF442
SFLASH_MACRO_0_FREE_SFLASH67	0x0FFF443
SFLASH_MACRO_0_FREE_SFLASH68	0x0FFF444
SFLASH_MACRO_0_FREE_SFLASH69	0x0FFF445
SFLASH_MACRO_0_FREE_SFLASH70	0x0FFF446
SFLASH_MACRO_0_FREE_SFLASH71	0x0FFF447
SFLASH_MACRO_0_FREE_SFLASH72	0x0FFF448
SFLASH_MACRO_0_FREE_SFLASH73	0x0FFF449
SFLASH_MACRO_0_FREE_SFLASH74	0x0FFF44A
SFLASH_MACRO_0_FREE_SFLASH75	0x0FFF44B
SFLASH_MACRO_0_FREE_SFLASH76	0x0FFF44C
SFLASH_MACRO_0_FREE_SFLASH77	0x0FFF44D
SFLASH_MACRO_0_FREE_SFLASH78	0x0FFF44E
SFLASH_MACRO_0_FREE_SFLASH79	0x0FFF44F
SFLASH_MACRO_0_FREE_SFLASH80	0x0FFF450
SFLASH_MACRO_0_FREE_SFLASH81	0x0FFF451
SFLASH_MACRO_0_FREE_SFLASH82	0x0FFF452
SFLASH_MACRO_0_FREE_SFLASH83	0x0FFF453
SFLASH_MACRO_0_FREE_SFLASH84	0x0FFF454
SFLASH_MACRO_0_FREE_SFLASH85	0x0FFF455
SFLASH_MACRO_0_FREE_SFLASH86	0x0FFF456
SFLASH_MACRO_0_FREE_SFLASH87	0x0FFF457
SFLASH_MACRO_0_FREE_SFLASH88	0x0FFF458
SFLASH_MACRO_0_FREE_SFLASH89	0x0FFF459
SFLASH_MACRO_0_FREE_SFLASH90	0x0FFF45A
SFLASH_MACRO_0_FREE_SFLASH91	0x0FFF45B
SFLASH_MACRO_0_FREE_SFLASH92	0x0FFF45C
SFLASH_MACRO_0_FREE_SFLASH93	0x0FFF45D
SFLASH_MACRO_0_FREE_SFLASH94	0x0FFF45E
SFLASH_MACRO_0_FREE_SFLASH95	0x0FFF45F
SFLASH_MACRO_0_FREE_SFLASH96	0x0FFF460

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH97	0x0FFF461
SFLASH_MACRO_0_FREE_SFLASH98	0x0FFF462
SFLASH_MACRO_0_FREE_SFLASH99	0x0FFF463
SFLASH_MACRO_0_FREE_SFLASH100	0x0FFF464
SFLASH_MACRO_0_FREE_SFLASH101	0x0FFF465
SFLASH_MACRO_0_FREE_SFLASH102	0x0FFF466
SFLASH_MACRO_0_FREE_SFLASH103	0x0FFF467
SFLASH_MACRO_0_FREE_SFLASH104	0x0FFF468
SFLASH_MACRO_0_FREE_SFLASH105	0x0FFF469
SFLASH_MACRO_0_FREE_SFLASH106	0x0FFF46A
SFLASH_MACRO_0_FREE_SFLASH107	0x0FFF46B
SFLASH_MACRO_0_FREE_SFLASH108	0x0FFF46C
SFLASH_MACRO_0_FREE_SFLASH109	0x0FFF46D
SFLASH_MACRO_0_FREE_SFLASH110	0x0FFF46E
SFLASH_MACRO_0_FREE_SFLASH111	0x0FFF46F
SFLASH_MACRO_0_FREE_SFLASH112	0x0FFF470
SFLASH_MACRO_0_FREE_SFLASH113	0x0FFF471
SFLASH_MACRO_0_FREE_SFLASH114	0x0FFF472
SFLASH_MACRO_0_FREE_SFLASH115	0x0FFF473
SFLASH_MACRO_0_FREE_SFLASH116	0x0FFF474
SFLASH_MACRO_0_FREE_SFLASH117	0x0FFF475
SFLASH_MACRO_0_FREE_SFLASH118	0x0FFF476
SFLASH_MACRO_0_FREE_SFLASH119	0x0FFF477
SFLASH_MACRO_0_FREE_SFLASH120	0x0FFF478
SFLASH_MACRO_0_FREE_SFLASH121	0x0FFF479
SFLASH_MACRO_0_FREE_SFLASH122	0x0FFF47A
SFLASH_MACRO_0_FREE_SFLASH123	0x0FFF47B
SFLASH_MACRO_0_FREE_SFLASH124	0x0FFF47C
SFLASH_MACRO_0_FREE_SFLASH125	0x0FFF47D
SFLASH_MACRO_0_FREE_SFLASH126	0x0FFF47E
SFLASH_MACRO_0_FREE_SFLASH127	0x0FFF47F
SFLASH_MACRO_0_FREE_SFLASH128	0x0FFF480
SFLASH_MACRO_0_FREE_SFLASH129	0x0FFF481
SFLASH_MACRO_0_FREE_SFLASH130	0x0FFF482
SFLASH_MACRO_0_FREE_SFLASH131	0x0FFF483
SFLASH_MACRO_0_FREE_SFLASH132	0x0FFF484
SFLASH_MACRO_0_FREE_SFLASH133	0x0FFF485
SFLASH_MACRO_0_FREE_SFLASH134	0x0FFF486
SFLASH_MACRO_0_FREE_SFLASH135	0x0FFF487
SFLASH_MACRO_0_FREE_SFLASH136	0x0FFF488
SFLASH_MACRO_0_FREE_SFLASH137	0x0FFF489
SFLASH_MACRO_0_FREE_SFLASH138	0x0FFF48A

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH139	0x0FFF48B
SFLASH_MACRO_0_FREE_SFLASH140	0x0FFF48C
SFLASH_MACRO_0_FREE_SFLASH141	0x0FFF48D
SFLASH_MACRO_0_FREE_SFLASH142	0x0FFF48E
SFLASH_MACRO_0_FREE_SFLASH143	0x0FFF48F
SFLASH_MACRO_0_FREE_SFLASH144	0x0FFF490
SFLASH_MACRO_0_FREE_SFLASH145	0x0FFF491
SFLASH_MACRO_0_FREE_SFLASH146	0x0FFF492
SFLASH_MACRO_0_FREE_SFLASH147	0x0FFF493
SFLASH_MACRO_0_FREE_SFLASH148	0x0FFF494
SFLASH_MACRO_0_FREE_SFLASH149	0x0FFF495
SFLASH_MACRO_0_FREE_SFLASH150	0x0FFF496
SFLASH_MACRO_0_FREE_SFLASH151	0x0FFF497
SFLASH_MACRO_0_FREE_SFLASH152	0x0FFF498
SFLASH_MACRO_0_FREE_SFLASH153	0x0FFF499
SFLASH_MACRO_0_FREE_SFLASH154	0x0FFF49A
SFLASH_MACRO_0_FREE_SFLASH155	0x0FFF49B
SFLASH_MACRO_0_FREE_SFLASH156	0x0FFF49C
SFLASH_MACRO_0_FREE_SFLASH157	0x0FFF49D
SFLASH_MACRO_0_FREE_SFLASH158	0x0FFF49E
SFLASH_MACRO_0_FREE_SFLASH159	0x0FFF49F
SFLASH_MACRO_0_FREE_SFLASH160	0x0FFF4A0
SFLASH_MACRO_0_FREE_SFLASH161	0x0FFF4A1
SFLASH_MACRO_0_FREE_SFLASH162	0x0FFF4A2
SFLASH_MACRO_0_FREE_SFLASH163	0x0FFF4A3
SFLASH_MACRO_0_FREE_SFLASH164	0x0FFF4A4
SFLASH_MACRO_0_FREE_SFLASH165	0x0FFF4A5
SFLASH_MACRO_0_FREE_SFLASH166	0x0FFF4A6
SFLASH_MACRO_0_FREE_SFLASH167	0x0FFF4A7
SFLASH_MACRO_0_FREE_SFLASH168	0x0FFF4A8
SFLASH_MACRO_0_FREE_SFLASH169	0x0FFF4A9
SFLASH_MACRO_0_FREE_SFLASH170	0x0FFF4AA
SFLASH_MACRO_0_FREE_SFLASH171	0x0FFF4AB
SFLASH_MACRO_0_FREE_SFLASH172	0x0FFF4AC
SFLASH_MACRO_0_FREE_SFLASH173	0x0FFF4AD
SFLASH_MACRO_0_FREE_SFLASH174	0x0FFF4AE
SFLASH_MACRO_0_FREE_SFLASH175	0x0FFF4AF
SFLASH_MACRO_0_FREE_SFLASH176	0x0FFF4B0
SFLASH_MACRO_0_FREE_SFLASH177	0x0FFF4B1
SFLASH_MACRO_0_FREE_SFLASH178	0x0FFF4B2
SFLASH_MACRO_0_FREE_SFLASH179	0x0FFF4B3
SFLASH_MACRO_0_FREE_SFLASH180	0x0FFF4B4

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH181	0x0FFF4B5
SFLASH_MACRO_0_FREE_SFLASH182	0x0FFF4B6
SFLASH_MACRO_0_FREE_SFLASH183	0x0FFF4B7
SFLASH_MACRO_0_FREE_SFLASH184	0x0FFF4B8
SFLASH_MACRO_0_FREE_SFLASH185	0x0FFF4B9
SFLASH_MACRO_0_FREE_SFLASH186	0x0FFF4BA
SFLASH_MACRO_0_FREE_SFLASH187	0x0FFF4BB
SFLASH_MACRO_0_FREE_SFLASH188	0x0FFF4BC
SFLASH_MACRO_0_FREE_SFLASH189	0x0FFF4BD
SFLASH_MACRO_0_FREE_SFLASH190	0x0FFF4BE
SFLASH_MACRO_0_FREE_SFLASH191	0x0FFF4BF
SFLASH_MACRO_0_FREE_SFLASH192	0x0FFF4C0
SFLASH_MACRO_0_FREE_SFLASH193	0x0FFF4C1
SFLASH_MACRO_0_FREE_SFLASH194	0x0FFF4C2
SFLASH_MACRO_0_FREE_SFLASH195	0x0FFF4C3
SFLASH_MACRO_0_FREE_SFLASH196	0x0FFF4C4
SFLASH_MACRO_0_FREE_SFLASH197	0x0FFF4C5
SFLASH_MACRO_0_FREE_SFLASH198	0x0FFF4C6
SFLASH_MACRO_0_FREE_SFLASH199	0x0FFF4C7
SFLASH_MACRO_0_FREE_SFLASH200	0x0FFF4C8
SFLASH_MACRO_0_FREE_SFLASH201	0x0FFF4C9
SFLASH_MACRO_0_FREE_SFLASH202	0x0FFF4CA
SFLASH_MACRO_0_FREE_SFLASH203	0x0FFF4CB
SFLASH_MACRO_0_FREE_SFLASH204	0x0FFF4CC
SFLASH_MACRO_0_FREE_SFLASH205	0x0FFF4CD
SFLASH_MACRO_0_FREE_SFLASH206	0x0FFF4CE
SFLASH_MACRO_0_FREE_SFLASH207	0x0FFF4CF
SFLASH_MACRO_0_FREE_SFLASH208	0x0FFF4D0
SFLASH_MACRO_0_FREE_SFLASH209	0x0FFF4D1
SFLASH_MACRO_0_FREE_SFLASH210	0x0FFF4D2
SFLASH_MACRO_0_FREE_SFLASH211	0x0FFF4D3
SFLASH_MACRO_0_FREE_SFLASH212	0x0FFF4D4
SFLASH_MACRO_0_FREE_SFLASH213	0x0FFF4D5
SFLASH_MACRO_0_FREE_SFLASH214	0x0FFF4D6
SFLASH_MACRO_0_FREE_SFLASH215	0x0FFF4D7
SFLASH_MACRO_0_FREE_SFLASH216	0x0FFF4D8
SFLASH_MACRO_0_FREE_SFLASH217	0x0FFF4D9
SFLASH_MACRO_0_FREE_SFLASH218	0x0FFF4DA
SFLASH_MACRO_0_FREE_SFLASH219	0x0FFF4DB
SFLASH_MACRO_0_FREE_SFLASH220	0x0FFF4DC
SFLASH_MACRO_0_FREE_SFLASH221	0x0FFF4DD
SFLASH_MACRO_0_FREE_SFLASH222	0x0FFF4DE

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH223	0x0FFF4DF
SFLASH_MACRO_0_FREE_SFLASH224	0x0FFF4E0
SFLASH_MACRO_0_FREE_SFLASH225	0x0FFF4E1
SFLASH_MACRO_0_FREE_SFLASH226	0x0FFF4E2
SFLASH_MACRO_0_FREE_SFLASH227	0x0FFF4E3
SFLASH_MACRO_0_FREE_SFLASH228	0x0FFF4E4
SFLASH_MACRO_0_FREE_SFLASH229	0x0FFF4E5
SFLASH_MACRO_0_FREE_SFLASH230	0x0FFF4E6
SFLASH_MACRO_0_FREE_SFLASH231	0x0FFF4E7
SFLASH_MACRO_0_FREE_SFLASH232	0x0FFF4E8
SFLASH_MACRO_0_FREE_SFLASH233	0x0FFF4E9
SFLASH_MACRO_0_FREE_SFLASH234	0x0FFF4EA
SFLASH_MACRO_0_FREE_SFLASH235	0x0FFF4EB
SFLASH_MACRO_0_FREE_SFLASH236	0x0FFF4EC
SFLASH_MACRO_0_FREE_SFLASH237	0x0FFF4ED
SFLASH_MACRO_0_FREE_SFLASH238	0x0FFF4EE
SFLASH_MACRO_0_FREE_SFLASH239	0x0FFF4EF
SFLASH_MACRO_0_FREE_SFLASH240	0x0FFF4F0
SFLASH_MACRO_0_FREE_SFLASH241	0x0FFF4F1
SFLASH_MACRO_0_FREE_SFLASH242	0x0FFF4F2
SFLASH_MACRO_0_FREE_SFLASH243	0x0FFF4F3
SFLASH_MACRO_0_FREE_SFLASH244	0x0FFF4F4
SFLASH_MACRO_0_FREE_SFLASH245	0x0FFF4F5
SFLASH_MACRO_0_FREE_SFLASH246	0x0FFF4F6
SFLASH_MACRO_0_FREE_SFLASH247	0x0FFF4F7
SFLASH_MACRO_0_FREE_SFLASH248	0x0FFF4F8
SFLASH_MACRO_0_FREE_SFLASH249	0x0FFF4F9
SFLASH_MACRO_0_FREE_SFLASH250	0x0FFF4FA
SFLASH_MACRO_0_FREE_SFLASH251	0x0FFF4FB
SFLASH_MACRO_0_FREE_SFLASH252	0x0FFF4FC
SFLASH_MACRO_0_FREE_SFLASH253	0x0FFF4FD
SFLASH_MACRO_0_FREE_SFLASH254	0x0FFF4FE
SFLASH_MACRO_0_FREE_SFLASH255	0x0FFF4FF
SFLASH_MACRO_0_FREE_SFLASH256	0x0FFF500
SFLASH_MACRO_0_FREE_SFLASH257	0x0FFF501
SFLASH_MACRO_0_FREE_SFLASH258	0x0FFF502
SFLASH_MACRO_0_FREE_SFLASH259	0x0FFF503
SFLASH_MACRO_0_FREE_SFLASH260	0x0FFF504
SFLASH_MACRO_0_FREE_SFLASH261	0x0FFF505
SFLASH_MACRO_0_FREE_SFLASH262	0x0FFF506
SFLASH_MACRO_0_FREE_SFLASH263	0x0FFF507
SFLASH_MACRO_0_FREE_SFLASH264	0x0FFF508



Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH265	0x0FFF509
SFLASH_MACRO_0_FREE_SFLASH266	0x0FFF50A
SFLASH_MACRO_0_FREE_SFLASH267	0x0FFF50B
SFLASH_MACRO_0_FREE_SFLASH268	0x0FFF50C
SFLASH_MACRO_0_FREE_SFLASH269	0x0FFF50D
SFLASH_MACRO_0_FREE_SFLASH270	0x0FFF50E
SFLASH_MACRO_0_FREE_SFLASH271	0x0FFF50F
SFLASH_MACRO_0_FREE_SFLASH272	0x0FFF510
SFLASH_MACRO_0_FREE_SFLASH273	0x0FFF511
SFLASH_MACRO_0_FREE_SFLASH274	0x0FFF512
SFLASH_MACRO_0_FREE_SFLASH275	0x0FFF513
SFLASH_MACRO_0_FREE_SFLASH276	0x0FFF514
SFLASH_MACRO_0_FREE_SFLASH277	0x0FFF515
SFLASH_MACRO_0_FREE_SFLASH278	0x0FFF516
SFLASH_MACRO_0_FREE_SFLASH279	0x0FFF517
SFLASH_MACRO_0_FREE_SFLASH280	0x0FFF518
SFLASH_MACRO_0_FREE_SFLASH281	0x0FFF519
SFLASH_MACRO_0_FREE_SFLASH282	0x0FFF51A
SFLASH_MACRO_0_FREE_SFLASH283	0x0FFF51B
SFLASH_MACRO_0_FREE_SFLASH284	0x0FFF51C
SFLASH_MACRO_0_FREE_SFLASH285	0x0FFF51D
SFLASH_MACRO_0_FREE_SFLASH286	0x0FFF51E
SFLASH_MACRO_0_FREE_SFLASH287	0x0FFF51F
SFLASH_MACRO_0_FREE_SFLASH288	0x0FFF520
SFLASH_MACRO_0_FREE_SFLASH289	0x0FFF521
SFLASH_MACRO_0_FREE_SFLASH290	0x0FFF522
SFLASH_MACRO_0_FREE_SFLASH291	0x0FFF523
SFLASH_MACRO_0_FREE_SFLASH292	0x0FFF524
SFLASH_MACRO_0_FREE_SFLASH293	0x0FFF525
SFLASH_MACRO_0_FREE_SFLASH294	0x0FFF526
SFLASH_MACRO_0_FREE_SFLASH295	0x0FFF527
SFLASH_MACRO_0_FREE_SFLASH296	0x0FFF528
SFLASH_MACRO_0_FREE_SFLASH297	0x0FFF529
SFLASH_MACRO_0_FREE_SFLASH298	0x0FFF52A
SFLASH_MACRO_0_FREE_SFLASH299	0x0FFF52B
SFLASH_MACRO_0_FREE_SFLASH300	0x0FFF52C
SFLASH_MACRO_0_FREE_SFLASH301	0x0FFF52D
SFLASH_MACRO_0_FREE_SFLASH302	0x0FFF52E
SFLASH_MACRO_0_FREE_SFLASH303	0x0FFF52F
SFLASH_MACRO_0_FREE_SFLASH304	0x0FFF530
SFLASH_MACRO_0_FREE_SFLASH305	0x0FFF531
SFLASH_MACRO_0_FREE_SFLASH306	0x0FFF532

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH307	0x0FFF533
SFLASH_MACRO_0_FREE_SFLASH308	0x0FFF534
SFLASH_MACRO_0_FREE_SFLASH309	0x0FFF535
SFLASH_MACRO_0_FREE_SFLASH310	0x0FFF536
SFLASH_MACRO_0_FREE_SFLASH311	0x0FFF537
SFLASH_MACRO_0_FREE_SFLASH312	0x0FFF538
SFLASH_MACRO_0_FREE_SFLASH313	0x0FFF539
SFLASH_MACRO_0_FREE_SFLASH314	0x0FFF53A
SFLASH_MACRO_0_FREE_SFLASH315	0x0FFF53B
SFLASH_MACRO_0_FREE_SFLASH316	0x0FFF53C
SFLASH_MACRO_0_FREE_SFLASH317	0x0FFF53D
SFLASH_MACRO_0_FREE_SFLASH318	0x0FFF53E
SFLASH_MACRO_0_FREE_SFLASH319	0x0FFF53F
SFLASH_MACRO_0_FREE_SFLASH320	0x0FFF540
SFLASH_MACRO_0_FREE_SFLASH321	0x0FFF541
SFLASH_MACRO_0_FREE_SFLASH322	0x0FFF542
SFLASH_MACRO_0_FREE_SFLASH323	0x0FFF543
SFLASH_MACRO_0_FREE_SFLASH324	0x0FFF544
SFLASH_MACRO_0_FREE_SFLASH325	0x0FFF545
SFLASH_MACRO_0_FREE_SFLASH326	0x0FFF546
SFLASH_MACRO_0_FREE_SFLASH327	0x0FFF547
SFLASH_MACRO_0_FREE_SFLASH328	0x0FFF548
SFLASH_MACRO_0_FREE_SFLASH329	0x0FFF549
SFLASH_MACRO_0_FREE_SFLASH330	0x0FFF54A
SFLASH_MACRO_0_FREE_SFLASH331	0x0FFF54B
SFLASH_MACRO_0_FREE_SFLASH332	0x0FFF54C
SFLASH_MACRO_0_FREE_SFLASH333	0x0FFF54D
SFLASH_MACRO_0_FREE_SFLASH334	0x0FFF54E
SFLASH_MACRO_0_FREE_SFLASH335	0x0FFF54F
SFLASH_MACRO_0_FREE_SFLASH336	0x0FFF550
SFLASH_MACRO_0_FREE_SFLASH337	0x0FFF551
SFLASH_MACRO_0_FREE_SFLASH338	0x0FFF552
SFLASH_MACRO_0_FREE_SFLASH339	0x0FFF553
SFLASH_MACRO_0_FREE_SFLASH340	0x0FFF554
SFLASH_MACRO_0_FREE_SFLASH341	0x0FFF555
SFLASH_MACRO_0_FREE_SFLASH342	0x0FFF556
SFLASH_MACRO_0_FREE_SFLASH343	0x0FFF557
SFLASH_MACRO_0_FREE_SFLASH344	0x0FFF558
SFLASH_MACRO_0_FREE_SFLASH345	0x0FFF559
SFLASH_MACRO_0_FREE_SFLASH346	0x0FFF55A
SFLASH_MACRO_0_FREE_SFLASH347	0x0FFF55B
SFLASH_MACRO_0_FREE_SFLASH348	0x0FFF55C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH349	0x0FFF55D
SFLASH_MACRO_0_FREE_SFLASH350	0x0FFF55E
SFLASH_MACRO_0_FREE_SFLASH351	0x0FFF55F
SFLASH_MACRO_0_FREE_SFLASH352	0x0FFF560
SFLASH_MACRO_0_FREE_SFLASH353	0x0FFF561
SFLASH_MACRO_0_FREE_SFLASH354	0x0FFF562
SFLASH_MACRO_0_FREE_SFLASH355	0x0FFF563
SFLASH_MACRO_0_FREE_SFLASH356	0x0FFF564
SFLASH_MACRO_0_FREE_SFLASH357	0x0FFF565
SFLASH_MACRO_0_FREE_SFLASH358	0x0FFF566
SFLASH_MACRO_0_FREE_SFLASH359	0x0FFF567
SFLASH_MACRO_0_FREE_SFLASH360	0x0FFF568
SFLASH_MACRO_0_FREE_SFLASH361	0x0FFF569
SFLASH_MACRO_0_FREE_SFLASH362	0x0FFF56A
SFLASH_MACRO_0_FREE_SFLASH363	0x0FFF56B
SFLASH_MACRO_0_FREE_SFLASH364	0x0FFF56C
SFLASH_MACRO_0_FREE_SFLASH365	0x0FFF56D
SFLASH_MACRO_0_FREE_SFLASH366	0x0FFF56E
SFLASH_MACRO_0_FREE_SFLASH367	0x0FFF56F
SFLASH_MACRO_0_FREE_SFLASH368	0x0FFF570
SFLASH_MACRO_0_FREE_SFLASH369	0x0FFF571
SFLASH_MACRO_0_FREE_SFLASH370	0x0FFF572
SFLASH_MACRO_0_FREE_SFLASH371	0x0FFF573
SFLASH_MACRO_0_FREE_SFLASH372	0x0FFF574
SFLASH_MACRO_0_FREE_SFLASH373	0x0FFF575
SFLASH_MACRO_0_FREE_SFLASH374	0x0FFF576
SFLASH_MACRO_0_FREE_SFLASH375	0x0FFF577
SFLASH_MACRO_0_FREE_SFLASH376	0x0FFF578
SFLASH_MACRO_0_FREE_SFLASH377	0x0FFF579
SFLASH_MACRO_0_FREE_SFLASH378	0x0FFF57A
SFLASH_MACRO_0_FREE_SFLASH379	0x0FFF57B
SFLASH_MACRO_0_FREE_SFLASH380	0x0FFF57C
SFLASH_MACRO_0_FREE_SFLASH381	0x0FFF57D
SFLASH_MACRO_0_FREE_SFLASH382	0x0FFF57E
SFLASH_MACRO_0_FREE_SFLASH383	0x0FFF57F
SFLASH_MACRO_0_FREE_SFLASH384	0x0FFF580
SFLASH_MACRO_0_FREE_SFLASH385	0x0FFF581
SFLASH_MACRO_0_FREE_SFLASH386	0x0FFF582
SFLASH_MACRO_0_FREE_SFLASH387	0x0FFF583
SFLASH_MACRO_0_FREE_SFLASH388	0x0FFF584
SFLASH_MACRO_0_FREE_SFLASH389	0x0FFF585
SFLASH_MACRO_0_FREE_SFLASH390	0x0FFF586

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH391	0x0FFF587
SFLASH_MACRO_0_FREE_SFLASH392	0x0FFF588
SFLASH_MACRO_0_FREE_SFLASH393	0x0FFF589
SFLASH_MACRO_0_FREE_SFLASH394	0x0FFF58A
SFLASH_MACRO_0_FREE_SFLASH395	0x0FFF58B
SFLASH_MACRO_0_FREE_SFLASH396	0x0FFF58C
SFLASH_MACRO_0_FREE_SFLASH397	0x0FFF58D
SFLASH_MACRO_0_FREE_SFLASH398	0x0FFF58E
SFLASH_MACRO_0_FREE_SFLASH399	0x0FFF58F
SFLASH_MACRO_0_FREE_SFLASH400	0x0FFF590
SFLASH_MACRO_0_FREE_SFLASH401	0x0FFF591
SFLASH_MACRO_0_FREE_SFLASH402	0x0FFF592
SFLASH_MACRO_0_FREE_SFLASH403	0x0FFF593
SFLASH_MACRO_0_FREE_SFLASH404	0x0FFF594
SFLASH_MACRO_0_FREE_SFLASH405	0x0FFF595
SFLASH_MACRO_0_FREE_SFLASH406	0x0FFF596
SFLASH_MACRO_0_FREE_SFLASH407	0x0FFF597
SFLASH_MACRO_0_FREE_SFLASH408	0x0FFF598
SFLASH_MACRO_0_FREE_SFLASH409	0x0FFF599
SFLASH_MACRO_0_FREE_SFLASH410	0x0FFF59A
SFLASH_MACRO_0_FREE_SFLASH411	0x0FFF59B
SFLASH_MACRO_0_FREE_SFLASH412	0x0FFF59C
SFLASH_MACRO_0_FREE_SFLASH413	0x0FFF59D
SFLASH_MACRO_0_FREE_SFLASH414	0x0FFF59E
SFLASH_MACRO_0_FREE_SFLASH415	0x0FFF59F
SFLASH_MACRO_0_FREE_SFLASH416	0x0FFF5A0
SFLASH_MACRO_0_FREE_SFLASH417	0x0FFF5A1
SFLASH_MACRO_0_FREE_SFLASH418	0x0FFF5A2
SFLASH_MACRO_0_FREE_SFLASH419	0x0FFF5A3
SFLASH_MACRO_0_FREE_SFLASH420	0x0FFF5A4
SFLASH_MACRO_0_FREE_SFLASH421	0x0FFF5A5
SFLASH_MACRO_0_FREE_SFLASH422	0x0FFF5A6
SFLASH_MACRO_0_FREE_SFLASH423	0x0FFF5A7
SFLASH_MACRO_0_FREE_SFLASH424	0x0FFF5A8
SFLASH_MACRO_0_FREE_SFLASH425	0x0FFF5A9
SFLASH_MACRO_0_FREE_SFLASH426	0x0FFF5AA
SFLASH_MACRO_0_FREE_SFLASH427	0x0FFF5AB
SFLASH_MACRO_0_FREE_SFLASH428	0x0FFF5AC
SFLASH_MACRO_0_FREE_SFLASH429	0x0FFF5AD
SFLASH_MACRO_0_FREE_SFLASH430	0x0FFF5AE
SFLASH_MACRO_0_FREE_SFLASH431	0x0FFF5AF
SFLASH_MACRO_0_FREE_SFLASH432	0x0FFF5B0

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH433	0x0FFF5B1
SFLASH_MACRO_0_FREE_SFLASH434	0x0FFF5B2
SFLASH_MACRO_0_FREE_SFLASH435	0x0FFF5B3
SFLASH_MACRO_0_FREE_SFLASH436	0x0FFF5B4
SFLASH_MACRO_0_FREE_SFLASH437	0x0FFF5B5
SFLASH_MACRO_0_FREE_SFLASH438	0x0FFF5B6
SFLASH_MACRO_0_FREE_SFLASH439	0x0FFF5B7
SFLASH_MACRO_0_FREE_SFLASH440	0x0FFF5B8
SFLASH_MACRO_0_FREE_SFLASH441	0x0FFF5B9
SFLASH_MACRO_0_FREE_SFLASH442	0x0FFF5BA
SFLASH_MACRO_0_FREE_SFLASH443	0x0FFF5BB
SFLASH_MACRO_0_FREE_SFLASH444	0x0FFF5BC
SFLASH_MACRO_0_FREE_SFLASH445	0x0FFF5BD
SFLASH_MACRO_0_FREE_SFLASH446	0x0FFF5BE
SFLASH_MACRO_0_FREE_SFLASH447	0x0FFF5BF
SFLASH_MACRO_0_FREE_SFLASH448	0x0FFF5C0
SFLASH_MACRO_0_FREE_SFLASH449	0x0FFF5C1
SFLASH_MACRO_0_FREE_SFLASH450	0x0FFF5C2
SFLASH_MACRO_0_FREE_SFLASH451	0x0FFF5C3
SFLASH_MACRO_0_FREE_SFLASH452	0x0FFF5C4
SFLASH_MACRO_0_FREE_SFLASH453	0x0FFF5C5
SFLASH_MACRO_0_FREE_SFLASH454	0x0FFF5C6
SFLASH_MACRO_0_FREE_SFLASH455	0x0FFF5C7
SFLASH_MACRO_0_FREE_SFLASH456	0x0FFF5C8
SFLASH_MACRO_0_FREE_SFLASH457	0x0FFF5C9
SFLASH_MACRO_0_FREE_SFLASH458	0x0FFF5CA
SFLASH_MACRO_0_FREE_SFLASH459	0x0FFF5CB
SFLASH_MACRO_0_FREE_SFLASH460	0x0FFF5CC
SFLASH_MACRO_0_FREE_SFLASH461	0x0FFF5CD
SFLASH_MACRO_0_FREE_SFLASH462	0x0FFF5CE
SFLASH_MACRO_0_FREE_SFLASH463	0x0FFF5CF
SFLASH_MACRO_0_FREE_SFLASH464	0x0FFF5D0
SFLASH_MACRO_0_FREE_SFLASH465	0x0FFF5D1
SFLASH_MACRO_0_FREE_SFLASH466	0x0FFF5D2
SFLASH_MACRO_0_FREE_SFLASH467	0x0FFF5D3
SFLASH_MACRO_0_FREE_SFLASH468	0x0FFF5D4
SFLASH_MACRO_0_FREE_SFLASH469	0x0FFF5D5
SFLASH_MACRO_0_FREE_SFLASH470	0x0FFF5D6
SFLASH_MACRO_0_FREE_SFLASH471	0x0FFF5D7
SFLASH_MACRO_0_FREE_SFLASH472	0x0FFF5D8
SFLASH_MACRO_0_FREE_SFLASH473	0x0FFF5D9
SFLASH_MACRO_0_FREE_SFLASH474	0x0FFF5DA

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH475	0x0FFF5DB
SFLASH_MACRO_0_FREE_SFLASH476	0x0FFF5DC
SFLASH_MACRO_0_FREE_SFLASH477	0x0FFF5DD
SFLASH_MACRO_0_FREE_SFLASH478	0x0FFF5DE
SFLASH_MACRO_0_FREE_SFLASH479	0x0FFF5DF
SFLASH_MACRO_0_FREE_SFLASH480	0x0FFF5E0
SFLASH_MACRO_0_FREE_SFLASH481	0x0FFF5E1
SFLASH_MACRO_0_FREE_SFLASH482	0x0FFF5E2
SFLASH_MACRO_0_FREE_SFLASH483	0x0FFF5E3
SFLASH_MACRO_0_FREE_SFLASH484	0x0FFF5E4
SFLASH_MACRO_0_FREE_SFLASH485	0x0FFF5E5
SFLASH_MACRO_0_FREE_SFLASH486	0x0FFF5E6
SFLASH_MACRO_0_FREE_SFLASH487	0x0FFF5E7
SFLASH_MACRO_0_FREE_SFLASH488	0x0FFF5E8
SFLASH_MACRO_0_FREE_SFLASH489	0x0FFF5E9
SFLASH_MACRO_0_FREE_SFLASH490	0x0FFF5EA
SFLASH_MACRO_0_FREE_SFLASH491	0x0FFF5EB
SFLASH_MACRO_0_FREE_SFLASH492	0x0FFF5EC
SFLASH_MACRO_0_FREE_SFLASH493	0x0FFF5ED
SFLASH_MACRO_0_FREE_SFLASH494	0x0FFF5EE
SFLASH_MACRO_0_FREE_SFLASH495	0x0FFF5EF
SFLASH_MACRO_0_FREE_SFLASH496	0x0FFF5F0
SFLASH_MACRO_0_FREE_SFLASH497	0x0FFF5F1
SFLASH_MACRO_0_FREE_SFLASH498	0x0FFF5F2
SFLASH_MACRO_0_FREE_SFLASH499	0x0FFF5F3
SFLASH_MACRO_0_FREE_SFLASH500	0x0FFF5F4
SFLASH_MACRO_0_FREE_SFLASH501	0x0FFF5F5
SFLASH_MACRO_0_FREE_SFLASH502	0x0FFF5F6
SFLASH_MACRO_0_FREE_SFLASH503	0x0FFF5F7
SFLASH_MACRO_0_FREE_SFLASH504	0x0FFF5F8
SFLASH_MACRO_0_FREE_SFLASH505	0x0FFF5F9
SFLASH_MACRO_0_FREE_SFLASH506	0x0FFF5FA
SFLASH_MACRO_0_FREE_SFLASH507	0x0FFF5FB
SFLASH_MACRO_0_FREE_SFLASH508	0x0FFF5FC
SFLASH_MACRO_0_FREE_SFLASH509	0x0FFF5FD
SFLASH_MACRO_0_FREE_SFLASH510	0x0FFF5FE
SFLASH_MACRO_0_FREE_SFLASH511	0x0FFF5FF
SFLASH_MACRO_0_FREE_SFLASH512	0x0FFF600
SFLASH_MACRO_0_FREE_SFLASH513	0x0FFF601
SFLASH_MACRO_0_FREE_SFLASH514	0x0FFF602
SFLASH_MACRO_0_FREE_SFLASH515	0x0FFF603
SFLASH_MACRO_0_FREE_SFLASH516	0x0FFF604

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH517	0x0FFF605
SFLASH_MACRO_0_FREE_SFLASH518	0x0FFF606
SFLASH_MACRO_0_FREE_SFLASH519	0x0FFF607
SFLASH_MACRO_0_FREE_SFLASH520	0x0FFF608
SFLASH_MACRO_0_FREE_SFLASH521	0x0FFF609
SFLASH_MACRO_0_FREE_SFLASH522	0x0FFF60A
SFLASH_MACRO_0_FREE_SFLASH523	0x0FFF60B
SFLASH_MACRO_0_FREE_SFLASH524	0x0FFF60C
SFLASH_MACRO_0_FREE_SFLASH525	0x0FFF60D
SFLASH_MACRO_0_FREE_SFLASH526	0x0FFF60E
SFLASH_MACRO_0_FREE_SFLASH527	0x0FFF60F
SFLASH_MACRO_0_FREE_SFLASH528	0x0FFF610
SFLASH_MACRO_0_FREE_SFLASH529	0x0FFF611
SFLASH_MACRO_0_FREE_SFLASH530	0x0FFF612
SFLASH_MACRO_0_FREE_SFLASH531	0x0FFF613
SFLASH_MACRO_0_FREE_SFLASH532	0x0FFF614
SFLASH_MACRO_0_FREE_SFLASH533	0x0FFF615
SFLASH_MACRO_0_FREE_SFLASH534	0x0FFF616
SFLASH_MACRO_0_FREE_SFLASH535	0x0FFF617
SFLASH_MACRO_0_FREE_SFLASH536	0x0FFF618
SFLASH_MACRO_0_FREE_SFLASH537	0x0FFF619
SFLASH_MACRO_0_FREE_SFLASH538	0x0FFF61A
SFLASH_MACRO_0_FREE_SFLASH539	0x0FFF61B
SFLASH_MACRO_0_FREE_SFLASH540	0x0FFF61C
SFLASH_MACRO_0_FREE_SFLASH541	0x0FFF61D
SFLASH_MACRO_0_FREE_SFLASH542	0x0FFF61E
SFLASH_MACRO_0_FREE_SFLASH543	0x0FFF61F
SFLASH_MACRO_0_FREE_SFLASH544	0x0FFF620
SFLASH_MACRO_0_FREE_SFLASH545	0x0FFF621
SFLASH_MACRO_0_FREE_SFLASH546	0x0FFF622
SFLASH_MACRO_0_FREE_SFLASH547	0x0FFF623
SFLASH_MACRO_0_FREE_SFLASH548	0x0FFF624
SFLASH_MACRO_0_FREE_SFLASH549	0x0FFF625
SFLASH_MACRO_0_FREE_SFLASH550	0x0FFF626
SFLASH_MACRO_0_FREE_SFLASH551	0x0FFF627
SFLASH_MACRO_0_FREE_SFLASH552	0x0FFF628
SFLASH_MACRO_0_FREE_SFLASH553	0x0FFF629
SFLASH_MACRO_0_FREE_SFLASH554	0x0FFF62A
SFLASH_MACRO_0_FREE_SFLASH555	0x0FFF62B
SFLASH_MACRO_0_FREE_SFLASH556	0x0FFF62C
SFLASH_MACRO_0_FREE_SFLASH557	0x0FFF62D
SFLASH_MACRO_0_FREE_SFLASH558	0x0FFF62E

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH559	0x0FFF62F
SFLASH_MACRO_0_FREE_SFLASH560	0x0FFF630
SFLASH_MACRO_0_FREE_SFLASH561	0x0FFF631
SFLASH_MACRO_0_FREE_SFLASH562	0x0FFF632
SFLASH_MACRO_0_FREE_SFLASH563	0x0FFF633
SFLASH_MACRO_0_FREE_SFLASH564	0x0FFF634
SFLASH_MACRO_0_FREE_SFLASH565	0x0FFF635
SFLASH_MACRO_0_FREE_SFLASH566	0x0FFF636
SFLASH_MACRO_0_FREE_SFLASH567	0x0FFF637
SFLASH_MACRO_0_FREE_SFLASH568	0x0FFF638
SFLASH_MACRO_0_FREE_SFLASH569	0x0FFF639
SFLASH_MACRO_0_FREE_SFLASH570	0x0FFF63A
SFLASH_MACRO_0_FREE_SFLASH571	0x0FFF63B
SFLASH_MACRO_0_FREE_SFLASH572	0x0FFF63C
SFLASH_MACRO_0_FREE_SFLASH573	0x0FFF63D
SFLASH_MACRO_0_FREE_SFLASH574	0x0FFF63E
SFLASH_MACRO_0_FREE_SFLASH575	0x0FFF63F
SFLASH_MACRO_0_FREE_SFLASH576	0x0FFF640
SFLASH_MACRO_0_FREE_SFLASH577	0x0FFF641
SFLASH_MACRO_0_FREE_SFLASH578	0x0FFF642
SFLASH_MACRO_0_FREE_SFLASH579	0x0FFF643
SFLASH_MACRO_0_FREE_SFLASH580	0x0FFF644
SFLASH_MACRO_0_FREE_SFLASH581	0x0FFF645
SFLASH_MACRO_0_FREE_SFLASH582	0x0FFF646
SFLASH_MACRO_0_FREE_SFLASH583	0x0FFF647
SFLASH_MACRO_0_FREE_SFLASH584	0x0FFF648
SFLASH_MACRO_0_FREE_SFLASH585	0x0FFF649
SFLASH_MACRO_0_FREE_SFLASH586	0x0FFF64A
SFLASH_MACRO_0_FREE_SFLASH587	0x0FFF64B
SFLASH_MACRO_0_FREE_SFLASH588	0x0FFF64C
SFLASH_MACRO_0_FREE_SFLASH589	0x0FFF64D
SFLASH_MACRO_0_FREE_SFLASH590	0x0FFF64E
SFLASH_MACRO_0_FREE_SFLASH591	0x0FFF64F
SFLASH_MACRO_0_FREE_SFLASH592	0x0FFF650
SFLASH_MACRO_0_FREE_SFLASH593	0x0FFF651
SFLASH_MACRO_0_FREE_SFLASH594	0x0FFF652
SFLASH_MACRO_0_FREE_SFLASH595	0x0FFF653
SFLASH_MACRO_0_FREE_SFLASH596	0x0FFF654
SFLASH_MACRO_0_FREE_SFLASH597	0x0FFF655
SFLASH_MACRO_0_FREE_SFLASH598	0x0FFF656
SFLASH_MACRO_0_FREE_SFLASH599	0x0FFF657
SFLASH_MACRO_0_FREE_SFLASH600	0x0FFF658



Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH601	0x0FFF659
SFLASH_MACRO_0_FREE_SFLASH602	0x0FFF65A
SFLASH_MACRO_0_FREE_SFLASH603	0x0FFF65B
SFLASH_MACRO_0_FREE_SFLASH604	0x0FFF65C
SFLASH_MACRO_0_FREE_SFLASH605	0x0FFF65D
SFLASH_MACRO_0_FREE_SFLASH606	0x0FFF65E
SFLASH_MACRO_0_FREE_SFLASH607	0x0FFF65F
SFLASH_MACRO_0_FREE_SFLASH608	0x0FFF660
SFLASH_MACRO_0_FREE_SFLASH609	0x0FFF661
SFLASH_MACRO_0_FREE_SFLASH610	0x0FFF662
SFLASH_MACRO_0_FREE_SFLASH611	0x0FFF663
SFLASH_MACRO_0_FREE_SFLASH612	0x0FFF664
SFLASH_MACRO_0_FREE_SFLASH613	0x0FFF665
SFLASH_MACRO_0_FREE_SFLASH614	0x0FFF666
SFLASH_MACRO_0_FREE_SFLASH615	0x0FFF667
SFLASH_MACRO_0_FREE_SFLASH616	0x0FFF668
SFLASH_MACRO_0_FREE_SFLASH617	0x0FFF669
SFLASH_MACRO_0_FREE_SFLASH618	0x0FFF66A
SFLASH_MACRO_0_FREE_SFLASH619	0x0FFF66B
SFLASH_MACRO_0_FREE_SFLASH620	0x0FFF66C
SFLASH_MACRO_0_FREE_SFLASH621	0x0FFF66D
SFLASH_MACRO_0_FREE_SFLASH622	0x0FFF66E
SFLASH_MACRO_0_FREE_SFLASH623	0x0FFF66F
SFLASH_MACRO_0_FREE_SFLASH624	0x0FFF670
SFLASH_MACRO_0_FREE_SFLASH625	0x0FFF671
SFLASH_MACRO_0_FREE_SFLASH626	0x0FFF672
SFLASH_MACRO_0_FREE_SFLASH627	0x0FFF673
SFLASH_MACRO_0_FREE_SFLASH628	0x0FFF674
SFLASH_MACRO_0_FREE_SFLASH629	0x0FFF675
SFLASH_MACRO_0_FREE_SFLASH630	0x0FFF676
SFLASH_MACRO_0_FREE_SFLASH631	0x0FFF677
SFLASH_MACRO_0_FREE_SFLASH632	0x0FFF678
SFLASH_MACRO_0_FREE_SFLASH633	0x0FFF679
SFLASH_MACRO_0_FREE_SFLASH634	0x0FFF67A
SFLASH_MACRO_0_FREE_SFLASH635	0x0FFF67B
SFLASH_MACRO_0_FREE_SFLASH636	0x0FFF67C
SFLASH_MACRO_0_FREE_SFLASH637	0x0FFF67D
SFLASH_MACRO_0_FREE_SFLASH638	0x0FFF67E
SFLASH_MACRO_0_FREE_SFLASH639	0x0FFF67F
SFLASH_MACRO_0_FREE_SFLASH640	0x0FFF680
SFLASH_MACRO_0_FREE_SFLASH641	0x0FFF681
SFLASH_MACRO_0_FREE_SFLASH642	0x0FFF682

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH643	0x0FFF683
SFLASH_MACRO_0_FREE_SFLASH644	0x0FFF684
SFLASH_MACRO_0_FREE_SFLASH645	0x0FFF685
SFLASH_MACRO_0_FREE_SFLASH646	0x0FFF686
SFLASH_MACRO_0_FREE_SFLASH647	0x0FFF687
SFLASH_MACRO_0_FREE_SFLASH648	0x0FFF688
SFLASH_MACRO_0_FREE_SFLASH649	0x0FFF689
SFLASH_MACRO_0_FREE_SFLASH650	0x0FFF68A
SFLASH_MACRO_0_FREE_SFLASH651	0x0FFF68B
SFLASH_MACRO_0_FREE_SFLASH652	0x0FFF68C
SFLASH_MACRO_0_FREE_SFLASH653	0x0FFF68D
SFLASH_MACRO_0_FREE_SFLASH654	0x0FFF68E
SFLASH_MACRO_0_FREE_SFLASH655	0x0FFF68F
SFLASH_MACRO_0_FREE_SFLASH656	0x0FFF690
SFLASH_MACRO_0_FREE_SFLASH657	0x0FFF691
SFLASH_MACRO_0_FREE_SFLASH658	0x0FFF692
SFLASH_MACRO_0_FREE_SFLASH659	0x0FFF693
SFLASH_MACRO_0_FREE_SFLASH660	0x0FFF694
SFLASH_MACRO_0_FREE_SFLASH661	0x0FFF695
SFLASH_MACRO_0_FREE_SFLASH662	0x0FFF696
SFLASH_MACRO_0_FREE_SFLASH663	0x0FFF697
SFLASH_MACRO_0_FREE_SFLASH664	0x0FFF698
SFLASH_MACRO_0_FREE_SFLASH665	0x0FFF699
SFLASH_MACRO_0_FREE_SFLASH666	0x0FFF69A
SFLASH_MACRO_0_FREE_SFLASH667	0x0FFF69B
SFLASH_MACRO_0_FREE_SFLASH668	0x0FFF69C
SFLASH_MACRO_0_FREE_SFLASH669	0x0FFF69D
SFLASH_MACRO_0_FREE_SFLASH670	0x0FFF69E
SFLASH_MACRO_0_FREE_SFLASH671	0x0FFF69F
SFLASH_MACRO_0_FREE_SFLASH672	0x0FFF6A0
SFLASH_MACRO_0_FREE_SFLASH673	0x0FFF6A1
SFLASH_MACRO_0_FREE_SFLASH674	0x0FFF6A2
SFLASH_MACRO_0_FREE_SFLASH675	0x0FFF6A3
SFLASH_MACRO_0_FREE_SFLASH676	0x0FFF6A4
SFLASH_MACRO_0_FREE_SFLASH677	0x0FFF6A5
SFLASH_MACRO_0_FREE_SFLASH678	0x0FFF6A6
SFLASH_MACRO_0_FREE_SFLASH679	0x0FFF6A7
SFLASH_MACRO_0_FREE_SFLASH680	0x0FFF6A8
SFLASH_MACRO_0_FREE_SFLASH681	0x0FFF6A9
SFLASH_MACRO_0_FREE_SFLASH682	0x0FFF6AA
SFLASH_MACRO_0_FREE_SFLASH683	0x0FFF6AB
SFLASH_MACRO_0_FREE_SFLASH684	0x0FFF6AC

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH685	0x0FFF6AD
SFLASH_MACRO_0_FREE_SFLASH686	0x0FFF6AE
SFLASH_MACRO_0_FREE_SFLASH687	0x0FFF6AF
SFLASH_MACRO_0_FREE_SFLASH688	0x0FFF6B0
SFLASH_MACRO_0_FREE_SFLASH689	0x0FFF6B1
SFLASH_MACRO_0_FREE_SFLASH690	0x0FFF6B2
SFLASH_MACRO_0_FREE_SFLASH691	0x0FFF6B3
SFLASH_MACRO_0_FREE_SFLASH692	0x0FFF6B4
SFLASH_MACRO_0_FREE_SFLASH693	0x0FFF6B5
SFLASH_MACRO_0_FREE_SFLASH694	0x0FFF6B6
SFLASH_MACRO_0_FREE_SFLASH695	0x0FFF6B7
SFLASH_MACRO_0_FREE_SFLASH696	0x0FFF6B8
SFLASH_MACRO_0_FREE_SFLASH697	0x0FFF6B9
SFLASH_MACRO_0_FREE_SFLASH698	0x0FFF6BA
SFLASH_MACRO_0_FREE_SFLASH699	0x0FFF6BB
SFLASH_MACRO_0_FREE_SFLASH700	0x0FFF6BC
SFLASH_MACRO_0_FREE_SFLASH701	0x0FFF6BD
SFLASH_MACRO_0_FREE_SFLASH702	0x0FFF6BE
SFLASH_MACRO_0_FREE_SFLASH703	0x0FFF6BF
SFLASH_MACRO_0_FREE_SFLASH704	0x0FFF6C0
SFLASH_MACRO_0_FREE_SFLASH705	0x0FFF6C1
SFLASH_MACRO_0_FREE_SFLASH706	0x0FFF6C2
SFLASH_MACRO_0_FREE_SFLASH707	0x0FFF6C3
SFLASH_MACRO_0_FREE_SFLASH708	0x0FFF6C4
SFLASH_MACRO_0_FREE_SFLASH709	0x0FFF6C5
SFLASH_MACRO_0_FREE_SFLASH710	0x0FFF6C6
SFLASH_MACRO_0_FREE_SFLASH711	0x0FFF6C7
SFLASH_MACRO_0_FREE_SFLASH712	0x0FFF6C8
SFLASH_MACRO_0_FREE_SFLASH713	0x0FFF6C9
SFLASH_MACRO_0_FREE_SFLASH714	0x0FFF6CA
SFLASH_MACRO_0_FREE_SFLASH715	0x0FFF6CB
SFLASH_MACRO_0_FREE_SFLASH716	0x0FFF6CC
SFLASH_MACRO_0_FREE_SFLASH717	0x0FFF6CD
SFLASH_MACRO_0_FREE_SFLASH718	0x0FFF6CE
SFLASH_MACRO_0_FREE_SFLASH719	0x0FFF6CF
SFLASH_MACRO_0_FREE_SFLASH720	0x0FFF6D0
SFLASH_MACRO_0_FREE_SFLASH721	0x0FFF6D1
SFLASH_MACRO_0_FREE_SFLASH722	0x0FFF6D2
SFLASH_MACRO_0_FREE_SFLASH723	0x0FFF6D3
SFLASH_MACRO_0_FREE_SFLASH724	0x0FFF6D4
SFLASH_MACRO_0_FREE_SFLASH725	0x0FFF6D5
SFLASH_MACRO_0_FREE_SFLASH726	0x0FFF6D6

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH727	0x0FFF6D7
SFLASH_MACRO_0_FREE_SFLASH728	0x0FFF6D8
SFLASH_MACRO_0_FREE_SFLASH729	0x0FFF6D9
SFLASH_MACRO_0_FREE_SFLASH730	0x0FFF6DA
SFLASH_MACRO_0_FREE_SFLASH731	0x0FFF6DB
SFLASH_MACRO_0_FREE_SFLASH732	0x0FFF6DC
SFLASH_MACRO_0_FREE_SFLASH733	0x0FFF6DD
SFLASH_MACRO_0_FREE_SFLASH734	0x0FFF6DE
SFLASH_MACRO_0_FREE_SFLASH735	0x0FFF6DF
SFLASH_MACRO_0_FREE_SFLASH736	0x0FFF6E0
SFLASH_MACRO_0_FREE_SFLASH737	0x0FFF6E1
SFLASH_MACRO_0_FREE_SFLASH738	0x0FFF6E2
SFLASH_MACRO_0_FREE_SFLASH739	0x0FFF6E3
SFLASH_MACRO_0_FREE_SFLASH740	0x0FFF6E4
SFLASH_MACRO_0_FREE_SFLASH741	0x0FFF6E5
SFLASH_MACRO_0_FREE_SFLASH742	0x0FFF6E6
SFLASH_MACRO_0_FREE_SFLASH743	0x0FFF6E7
SFLASH_MACRO_0_FREE_SFLASH744	0x0FFF6E8
SFLASH_MACRO_0_FREE_SFLASH745	0x0FFF6E9
SFLASH_MACRO_0_FREE_SFLASH746	0x0FFF6EA
SFLASH_MACRO_0_FREE_SFLASH747	0x0FFF6EB
SFLASH_MACRO_0_FREE_SFLASH748	0x0FFF6EC
SFLASH_MACRO_0_FREE_SFLASH749	0x0FFF6ED
SFLASH_MACRO_0_FREE_SFLASH750	0x0FFF6EE
SFLASH_MACRO_0_FREE_SFLASH751	0x0FFF6EF
SFLASH_MACRO_0_FREE_SFLASH752	0x0FFF6F0
SFLASH_MACRO_0_FREE_SFLASH753	0x0FFF6F1
SFLASH_MACRO_0_FREE_SFLASH754	0x0FFF6F2
SFLASH_MACRO_0_FREE_SFLASH755	0x0FFF6F3
SFLASH_MACRO_0_FREE_SFLASH756	0x0FFF6F4
SFLASH_MACRO_0_FREE_SFLASH757	0x0FFF6F5
SFLASH_MACRO_0_FREE_SFLASH758	0x0FFF6F6
SFLASH_MACRO_0_FREE_SFLASH759	0x0FFF6F7
SFLASH_MACRO_0_FREE_SFLASH760	0x0FFF6F8
SFLASH_MACRO_0_FREE_SFLASH761	0x0FFF6F9
SFLASH_MACRO_0_FREE_SFLASH762	0x0FFF6FA
SFLASH_MACRO_0_FREE_SFLASH763	0x0FFF6FB
SFLASH_MACRO_0_FREE_SFLASH764	0x0FFF6FC
SFLASH_MACRO_0_FREE_SFLASH765	0x0FFF6FD
SFLASH_MACRO_0_FREE_SFLASH766	0x0FFF6FE
SFLASH_MACRO_0_FREE_SFLASH767	0x0FFF6FF
SFLASH_MACRO_0_FREE_SFLASH768	0x0FFF700

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH769	0x0FFF701
SFLASH_MACRO_0_FREE_SFLASH770	0x0FFF702
SFLASH_MACRO_0_FREE_SFLASH771	0x0FFF703
SFLASH_MACRO_0_FREE_SFLASH772	0x0FFF704
SFLASH_MACRO_0_FREE_SFLASH773	0x0FFF705
SFLASH_MACRO_0_FREE_SFLASH774	0x0FFF706
SFLASH_MACRO_0_FREE_SFLASH775	0x0FFF707
SFLASH_MACRO_0_FREE_SFLASH776	0x0FFF708
SFLASH_MACRO_0_FREE_SFLASH777	0x0FFF709
SFLASH_MACRO_0_FREE_SFLASH778	0x0FFF70A
SFLASH_MACRO_0_FREE_SFLASH779	0x0FFF70B
SFLASH_MACRO_0_FREE_SFLASH780	0x0FFF70C
SFLASH_MACRO_0_FREE_SFLASH781	0x0FFF70D
SFLASH_MACRO_0_FREE_SFLASH782	0x0FFF70E
SFLASH_MACRO_0_FREE_SFLASH783	0x0FFF70F
SFLASH_MACRO_0_FREE_SFLASH784	0x0FFF710
SFLASH_MACRO_0_FREE_SFLASH785	0x0FFF711
SFLASH_MACRO_0_FREE_SFLASH786	0x0FFF712
SFLASH_MACRO_0_FREE_SFLASH787	0x0FFF713
SFLASH_MACRO_0_FREE_SFLASH788	0x0FFF714
SFLASH_MACRO_0_FREE_SFLASH789	0x0FFF715
SFLASH_MACRO_0_FREE_SFLASH790	0x0FFF716
SFLASH_MACRO_0_FREE_SFLASH791	0x0FFF717
SFLASH_MACRO_0_FREE_SFLASH792	0x0FFF718
SFLASH_MACRO_0_FREE_SFLASH793	0x0FFF719
SFLASH_MACRO_0_FREE_SFLASH794	0x0FFF71A
SFLASH_MACRO_0_FREE_SFLASH795	0x0FFF71B
SFLASH_MACRO_0_FREE_SFLASH796	0x0FFF71C
SFLASH_MACRO_0_FREE_SFLASH797	0x0FFF71D
SFLASH_MACRO_0_FREE_SFLASH798	0x0FFF71E
SFLASH_MACRO_0_FREE_SFLASH799	0x0FFF71F
SFLASH_MACRO_0_FREE_SFLASH800	0x0FFF720
SFLASH_MACRO_0_FREE_SFLASH801	0x0FFF721
SFLASH_MACRO_0_FREE_SFLASH802	0x0FFF722
SFLASH_MACRO_0_FREE_SFLASH803	0x0FFF723
SFLASH_MACRO_0_FREE_SFLASH804	0x0FFF724
SFLASH_MACRO_0_FREE_SFLASH805	0x0FFF725
SFLASH_MACRO_0_FREE_SFLASH806	0x0FFF726
SFLASH_MACRO_0_FREE_SFLASH807	0x0FFF727
SFLASH_MACRO_0_FREE_SFLASH808	0x0FFF728
SFLASH_MACRO_0_FREE_SFLASH809	0x0FFF729
SFLASH_MACRO_0_FREE_SFLASH810	0x0FFF72A

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH811	0x0FFF72B
SFLASH_MACRO_0_FREE_SFLASH812	0x0FFF72C
SFLASH_MACRO_0_FREE_SFLASH813	0x0FFF72D
SFLASH_MACRO_0_FREE_SFLASH814	0x0FFF72E
SFLASH_MACRO_0_FREE_SFLASH815	0x0FFF72F
SFLASH_MACRO_0_FREE_SFLASH816	0x0FFF730
SFLASH_MACRO_0_FREE_SFLASH817	0x0FFF731
SFLASH_MACRO_0_FREE_SFLASH818	0x0FFF732
SFLASH_MACRO_0_FREE_SFLASH819	0x0FFF733
SFLASH_MACRO_0_FREE_SFLASH820	0x0FFF734
SFLASH_MACRO_0_FREE_SFLASH821	0x0FFF735
SFLASH_MACRO_0_FREE_SFLASH822	0x0FFF736
SFLASH_MACRO_0_FREE_SFLASH823	0x0FFF737
SFLASH_MACRO_0_FREE_SFLASH824	0x0FFF738
SFLASH_MACRO_0_FREE_SFLASH825	0x0FFF739
SFLASH_MACRO_0_FREE_SFLASH826	0x0FFF73A
SFLASH_MACRO_0_FREE_SFLASH827	0x0FFF73B
SFLASH_MACRO_0_FREE_SFLASH828	0x0FFF73C
SFLASH_MACRO_0_FREE_SFLASH829	0x0FFF73D
SFLASH_MACRO_0_FREE_SFLASH830	0x0FFF73E
SFLASH_MACRO_0_FREE_SFLASH831	0x0FFF73F
SFLASH_MACRO_0_FREE_SFLASH832	0x0FFF740
SFLASH_MACRO_0_FREE_SFLASH833	0x0FFF741
SFLASH_MACRO_0_FREE_SFLASH834	0x0FFF742
SFLASH_MACRO_0_FREE_SFLASH835	0x0FFF743
SFLASH_MACRO_0_FREE_SFLASH836	0x0FFF744
SFLASH_MACRO_0_FREE_SFLASH837	0x0FFF745
SFLASH_MACRO_0_FREE_SFLASH838	0x0FFF746
SFLASH_MACRO_0_FREE_SFLASH839	0x0FFF747
SFLASH_MACRO_0_FREE_SFLASH840	0x0FFF748
SFLASH_MACRO_0_FREE_SFLASH841	0x0FFF749
SFLASH_MACRO_0_FREE_SFLASH842	0x0FFF74A
SFLASH_MACRO_0_FREE_SFLASH843	0x0FFF74B
SFLASH_MACRO_0_FREE_SFLASH844	0x0FFF74C
SFLASH_MACRO_0_FREE_SFLASH845	0x0FFF74D
SFLASH_MACRO_0_FREE_SFLASH846	0x0FFF74E
SFLASH_MACRO_0_FREE_SFLASH847	0x0FFF74F
SFLASH_MACRO_0_FREE_SFLASH848	0x0FFF750
SFLASH_MACRO_0_FREE_SFLASH849	0x0FFF751
SFLASH_MACRO_0_FREE_SFLASH850	0x0FFF752
SFLASH_MACRO_0_FREE_SFLASH851	0x0FFF753
SFLASH_MACRO_0_FREE_SFLASH852	0x0FFF754

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH853	0x0FFF755
SFLASH_MACRO_0_FREE_SFLASH854	0x0FFF756
SFLASH_MACRO_0_FREE_SFLASH855	0x0FFF757
SFLASH_MACRO_0_FREE_SFLASH856	0x0FFF758
SFLASH_MACRO_0_FREE_SFLASH857	0x0FFF759
SFLASH_MACRO_0_FREE_SFLASH858	0x0FFF75A
SFLASH_MACRO_0_FREE_SFLASH859	0x0FFF75B
SFLASH_MACRO_0_FREE_SFLASH860	0x0FFF75C
SFLASH_MACRO_0_FREE_SFLASH861	0x0FFF75D
SFLASH_MACRO_0_FREE_SFLASH862	0x0FFF75E
SFLASH_MACRO_0_FREE_SFLASH863	0x0FFF75F
SFLASH_MACRO_0_FREE_SFLASH864	0x0FFF760
SFLASH_MACRO_0_FREE_SFLASH865	0x0FFF761
SFLASH_MACRO_0_FREE_SFLASH866	0x0FFF762
SFLASH_MACRO_0_FREE_SFLASH867	0x0FFF763
SFLASH_MACRO_0_FREE_SFLASH868	0x0FFF764
SFLASH_MACRO_0_FREE_SFLASH869	0x0FFF765
SFLASH_MACRO_0_FREE_SFLASH870	0x0FFF766
SFLASH_MACRO_0_FREE_SFLASH871	0x0FFF767
SFLASH_MACRO_0_FREE_SFLASH872	0x0FFF768
SFLASH_MACRO_0_FREE_SFLASH873	0x0FFF769
SFLASH_MACRO_0_FREE_SFLASH874	0x0FFF76A
SFLASH_MACRO_0_FREE_SFLASH875	0x0FFF76B
SFLASH_MACRO_0_FREE_SFLASH876	0x0FFF76C
SFLASH_MACRO_0_FREE_SFLASH877	0x0FFF76D
SFLASH_MACRO_0_FREE_SFLASH878	0x0FFF76E
SFLASH_MACRO_0_FREE_SFLASH879	0x0FFF76F
SFLASH_MACRO_0_FREE_SFLASH880	0x0FFF770
SFLASH_MACRO_0_FREE_SFLASH881	0x0FFF771
SFLASH_MACRO_0_FREE_SFLASH882	0x0FFF772
SFLASH_MACRO_0_FREE_SFLASH883	0x0FFF773
SFLASH_MACRO_0_FREE_SFLASH884	0x0FFF774
SFLASH_MACRO_0_FREE_SFLASH885	0x0FFF775
SFLASH_MACRO_0_FREE_SFLASH886	0x0FFF776
SFLASH_MACRO_0_FREE_SFLASH887	0x0FFF777
SFLASH_MACRO_0_FREE_SFLASH888	0x0FFF778
SFLASH_MACRO_0_FREE_SFLASH889	0x0FFF779
SFLASH_MACRO_0_FREE_SFLASH890	0x0FFF77A
SFLASH_MACRO_0_FREE_SFLASH891	0x0FFF77B
SFLASH_MACRO_0_FREE_SFLASH892	0x0FFF77C
SFLASH_MACRO_0_FREE_SFLASH893	0x0FFF77D
SFLASH_MACRO_0_FREE_SFLASH894	0x0FFF77E

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH895	0x0FFF77F
SFLASH_MACRO_0_FREE_SFLASH896	0x0FFF780
SFLASH_MACRO_0_FREE_SFLASH897	0x0FFF781
SFLASH_MACRO_0_FREE_SFLASH898	0x0FFF782
SFLASH_MACRO_0_FREE_SFLASH899	0x0FFF783
SFLASH_MACRO_0_FREE_SFLASH900	0x0FFF784
SFLASH_MACRO_0_FREE_SFLASH901	0x0FFF785
SFLASH_MACRO_0_FREE_SFLASH902	0x0FFF786
SFLASH_MACRO_0_FREE_SFLASH903	0x0FFF787
SFLASH_MACRO_0_FREE_SFLASH904	0x0FFF788
SFLASH_MACRO_0_FREE_SFLASH905	0x0FFF789
SFLASH_MACRO_0_FREE_SFLASH906	0x0FFF78A
SFLASH_MACRO_0_FREE_SFLASH907	0x0FFF78B
SFLASH_MACRO_0_FREE_SFLASH908	0x0FFF78C
SFLASH_MACRO_0_FREE_SFLASH909	0x0FFF78D
SFLASH_MACRO_0_FREE_SFLASH910	0x0FFF78E
SFLASH_MACRO_0_FREE_SFLASH911	0x0FFF78F
SFLASH_MACRO_0_FREE_SFLASH912	0x0FFF790
SFLASH_MACRO_0_FREE_SFLASH913	0x0FFF791
SFLASH_MACRO_0_FREE_SFLASH914	0x0FFF792
SFLASH_MACRO_0_FREE_SFLASH915	0x0FFF793
SFLASH_MACRO_0_FREE_SFLASH916	0x0FFF794
SFLASH_MACRO_0_FREE_SFLASH917	0x0FFF795
SFLASH_MACRO_0_FREE_SFLASH918	0x0FFF796
SFLASH_MACRO_0_FREE_SFLASH919	0x0FFF797
SFLASH_MACRO_0_FREE_SFLASH920	0x0FFF798
SFLASH_MACRO_0_FREE_SFLASH921	0x0FFF799
SFLASH_MACRO_0_FREE_SFLASH922	0x0FFF79A
SFLASH_MACRO_0_FREE_SFLASH923	0x0FFF79B
SFLASH_MACRO_0_FREE_SFLASH924	0x0FFF79C
SFLASH_MACRO_0_FREE_SFLASH925	0x0FFF79D
SFLASH_MACRO_0_FREE_SFLASH926	0x0FFF79E
SFLASH_MACRO_0_FREE_SFLASH927	0x0FFF79F
SFLASH_MACRO_0_FREE_SFLASH928	0x0FFF7A0
SFLASH_MACRO_0_FREE_SFLASH929	0x0FFF7A1
SFLASH_MACRO_0_FREE_SFLASH930	0x0FFF7A2
SFLASH_MACRO_0_FREE_SFLASH931	0x0FFF7A3
SFLASH_MACRO_0_FREE_SFLASH932	0x0FFF7A4
SFLASH_MACRO_0_FREE_SFLASH933	0x0FFF7A5
SFLASH_MACRO_0_FREE_SFLASH934	0x0FFF7A6
SFLASH_MACRO_0_FREE_SFLASH935	0x0FFF7A7
SFLASH_MACRO_0_FREE_SFLASH936	0x0FFF7A8



Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH937	0x0FFF7A9
SFLASH_MACRO_0_FREE_SFLASH938	0x0FFF7AA
SFLASH_MACRO_0_FREE_SFLASH939	0x0FFF7AB
SFLASH_MACRO_0_FREE_SFLASH940	0x0FFF7AC
SFLASH_MACRO_0_FREE_SFLASH941	0x0FFF7AD
SFLASH_MACRO_0_FREE_SFLASH942	0x0FFF7AE
SFLASH_MACRO_0_FREE_SFLASH943	0x0FFF7AF
SFLASH_MACRO_0_FREE_SFLASH944	0x0FFF7B0
SFLASH_MACRO_0_FREE_SFLASH945	0x0FFF7B1
SFLASH_MACRO_0_FREE_SFLASH946	0x0FFF7B2
SFLASH_MACRO_0_FREE_SFLASH947	0x0FFF7B3
SFLASH_MACRO_0_FREE_SFLASH948	0x0FFF7B4
SFLASH_MACRO_0_FREE_SFLASH949	0x0FFF7B5
SFLASH_MACRO_0_FREE_SFLASH950	0x0FFF7B6
SFLASH_MACRO_0_FREE_SFLASH951	0x0FFF7B7
SFLASH_MACRO_0_FREE_SFLASH952	0x0FFF7B8
SFLASH_MACRO_0_FREE_SFLASH953	0x0FFF7B9
SFLASH_MACRO_0_FREE_SFLASH954	0x0FFF7BA
SFLASH_MACRO_0_FREE_SFLASH955	0x0FFF7BB
SFLASH_MACRO_0_FREE_SFLASH956	0x0FFF7BC
SFLASH_MACRO_0_FREE_SFLASH957	0x0FFF7BD
SFLASH_MACRO_0_FREE_SFLASH958	0x0FFF7BE
SFLASH_MACRO_0_FREE_SFLASH959	0x0FFF7BF
SFLASH_MACRO_0_FREE_SFLASH960	0x0FFF7C0
SFLASH_MACRO_0_FREE_SFLASH961	0x0FFF7C1
SFLASH_MACRO_0_FREE_SFLASH962	0x0FFF7C2
SFLASH_MACRO_0_FREE_SFLASH963	0x0FFF7C3
SFLASH_MACRO_0_FREE_SFLASH964	0x0FFF7C4
SFLASH_MACRO_0_FREE_SFLASH965	0x0FFF7C5
SFLASH_MACRO_0_FREE_SFLASH966	0x0FFF7C6
SFLASH_MACRO_0_FREE_SFLASH967	0x0FFF7C7
SFLASH_MACRO_0_FREE_SFLASH968	0x0FFF7C8
SFLASH_MACRO_0_FREE_SFLASH969	0x0FFF7C9
SFLASH_MACRO_0_FREE_SFLASH970	0x0FFF7CA
SFLASH_MACRO_0_FREE_SFLASH971	0x0FFF7CB
SFLASH_MACRO_0_FREE_SFLASH972	0x0FFF7CC
SFLASH_MACRO_0_FREE_SFLASH973	0x0FFF7CD
SFLASH_MACRO_0_FREE_SFLASH974	0x0FFF7CE
SFLASH_MACRO_0_FREE_SFLASH975	0x0FFF7CF
SFLASH_MACRO_0_FREE_SFLASH976	0x0FFF7D0
SFLASH_MACRO_0_FREE_SFLASH977	0x0FFF7D1
SFLASH_MACRO_0_FREE_SFLASH978	0x0FFF7D2

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH979	0x0FFF7D3
SFLASH_MACRO_0_FREE_SFLASH980	0x0FFF7D4
SFLASH_MACRO_0_FREE_SFLASH981	0x0FFF7D5
SFLASH_MACRO_0_FREE_SFLASH982	0x0FFF7D6
SFLASH_MACRO_0_FREE_SFLASH983	0x0FFF7D7
SFLASH_MACRO_0_FREE_SFLASH984	0x0FFF7D8
SFLASH_MACRO_0_FREE_SFLASH985	0x0FFF7D9
SFLASH_MACRO_0_FREE_SFLASH986	0x0FFF7DA
SFLASH_MACRO_0_FREE_SFLASH987	0x0FFF7DB
SFLASH_MACRO_0_FREE_SFLASH988	0x0FFF7DC
SFLASH_MACRO_0_FREE_SFLASH989	0x0FFF7DD
SFLASH_MACRO_0_FREE_SFLASH990	0x0FFF7DE
SFLASH_MACRO_0_FREE_SFLASH991	0x0FFF7DF
SFLASH_MACRO_0_FREE_SFLASH992	0x0FFF7E0
SFLASH_MACRO_0_FREE_SFLASH993	0x0FFF7E1
SFLASH_MACRO_0_FREE_SFLASH994	0x0FFF7E2
SFLASH_MACRO_0_FREE_SFLASH995	0x0FFF7E3
SFLASH_MACRO_0_FREE_SFLASH996	0x0FFF7E4
SFLASH_MACRO_0_FREE_SFLASH997	0x0FFF7E5
SFLASH_MACRO_0_FREE_SFLASH998	0x0FFF7E6
SFLASH_MACRO_0_FREE_SFLASH999	0x0FFF7E7
SFLASH_MACRO_0_FREE_SFLASH1000	0x0FFF7E8
SFLASH_MACRO_0_FREE_SFLASH1001	0x0FFF7E9
SFLASH_MACRO_0_FREE_SFLASH1002	0x0FFF7EA
SFLASH_MACRO_0_FREE_SFLASH1003	0x0FFF7EB
SFLASH_MACRO_0_FREE_SFLASH1004	0x0FFF7EC
SFLASH_MACRO_0_FREE_SFLASH1005	0x0FFF7ED
SFLASH_MACRO_0_FREE_SFLASH1006	0x0FFF7EE
SFLASH_MACRO_0_FREE_SFLASH1007	0x0FFF7EF
SFLASH_MACRO_0_FREE_SFLASH1008	0x0FFF7F0
SFLASH_MACRO_0_FREE_SFLASH1009	0x0FFF7F1
SFLASH_MACRO_0_FREE_SFLASH1010	0x0FFF7F2
SFLASH_MACRO_0_FREE_SFLASH1011	0x0FFF7F3
SFLASH_MACRO_0_FREE_SFLASH1012	0x0FFF7F4
SFLASH_MACRO_0_FREE_SFLASH1013	0x0FFF7F5
SFLASH_MACRO_0_FREE_SFLASH1014	0x0FFF7F6
SFLASH_MACRO_0_FREE_SFLASH1015	0x0FFF7F7
SFLASH_MACRO_0_FREE_SFLASH1016	0x0FFF7F8
SFLASH_MACRO_0_FREE_SFLASH1017	0x0FFF7F9
SFLASH_MACRO_0_FREE_SFLASH1018	0x0FFF7FA
SFLASH_MACRO_0_FREE_SFLASH1019	0x0FFF7FB
SFLASH_MACRO_0_FREE_SFLASH1020	0x0FFF7FC

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH1021	0x0FFF7FD
SFLASH_MACRO_0_FREE_SFLASH1022	0x0FFF7FE
SFLASH_MACRO_0_FREE_SFLASH1023	0x0FFF7FF
SFLASH_ALT_PROT_ROW0	0x0FFF800
SFLASH_ALT_PROT_ROW1	0x0FFF801
SFLASH_ALT_PROT_ROW2	0x0FFF802
SFLASH_ALT_PROT_ROW3	0x0FFF803
SFLASH_ALT_PROT_ROW4	0x0FFF804
SFLASH_ALT_PROT_ROW5	0x0FFF805
SFLASH_ALT_PROT_ROW6	0x0FFF806
SFLASH_ALT_PROT_ROW7	0x0FFF807
SFLASH_ALT_PROT_ROW8	0x0FFF808
SFLASH_ALT_PROT_ROW9	0x0FFF809
SFLASH_ALT_PROT_ROW10	0x0FFF80A
SFLASH_ALT_PROT_ROW11	0x0FFF80B
SFLASH_ALT_PROT_ROW12	0x0FFF80C
SFLASH_ALT_PROT_ROW13	0x0FFF80D
SFLASH_ALT_PROT_ROW14	0x0FFF80E
SFLASH_ALT_PROT_ROW15	0x0FFF80F
SFLASH_ALT_PROT_ROW16	0x0FFF810
SFLASH_ALT_PROT_ROW17	0x0FFF811
SFLASH_ALT_PROT_ROW18	0x0FFF812
SFLASH_ALT_PROT_ROW19	0x0FFF813
SFLASH_ALT_PROT_ROW20	0x0FFF814
SFLASH_ALT_PROT_ROW21	0x0FFF815
SFLASH_ALT_PROT_ROW22	0x0FFF816
SFLASH_ALT_PROT_ROW23	0x0FFF817
SFLASH_ALT_PROT_ROW24	0x0FFF818
SFLASH_ALT_PROT_ROW25	0x0FFF819
SFLASH_ALT_PROT_ROW26	0x0FFF81A
SFLASH_ALT_PROT_ROW27	0x0FFF81B
SFLASH_ALT_PROT_ROW28	0x0FFF81C
SFLASH_ALT_PROT_ROW29	0x0FFF81D
SFLASH_ALT_PROT_ROW30	0x0FFF81E
SFLASH_ALT_PROT_ROW31	0x0FFF81F
SFLASH_ALT_PROT_ROW32	0x0FFF820
SFLASH_ALT_PROT_ROW33	0x0FFF821
SFLASH_ALT_PROT_ROW34	0x0FFF822
SFLASH_ALT_PROT_ROW35	0x0FFF823
SFLASH_ALT_PROT_ROW36	0x0FFF824
SFLASH_ALT_PROT_ROW37	0x0FFF825
SFLASH_ALT_PROT_ROW38	0x0FFF826

Register Name	Address
SFLASH_ALT_PROT_ROW39	0x0FFF827
SFLASH_ALT_PROT_ROW40	0x0FFF828
SFLASH_ALT_PROT_ROW41	0x0FFF829
SFLASH_ALT_PROT_ROW42	0x0FFF82A
SFLASH_ALT_PROT_ROW43	0x0FFF82B
SFLASH_ALT_PROT_ROW44	0x0FFF82C
SFLASH_ALT_PROT_ROW45	0x0FFF82D
SFLASH_ALT_PROT_ROW46	0x0FFF82E
SFLASH_ALT_PROT_ROW47	0x0FFF82F
SFLASH_ALT_PROT_ROW48	0x0FFF830
SFLASH_ALT_PROT_ROW49	0x0FFF831
SFLASH_ALT_PROT_ROW50	0x0FFF832
SFLASH_ALT_PROT_ROW51	0x0FFF833
SFLASH_ALT_PROT_ROW52	0x0FFF834
SFLASH_ALT_PROT_ROW53	0x0FFF835
SFLASH_ALT_PROT_ROW54	0x0FFF836
SFLASH_ALT_PROT_ROW55	0x0FFF837
SFLASH_ALT_PROT_ROW56	0x0FFF838
SFLASH_ALT_PROT_ROW57	0x0FFF839
SFLASH_ALT_PROT_ROW58	0x0FFF83A
SFLASH_ALT_PROT_ROW59	0x0FFF83B
SFLASH_ALT_PROT_ROW60	0x0FFF83C
SFLASH_ALT_PROT_ROW61	0x0FFF83D
SFLASH_ALT_PROT_ROW62	0x0FFF83E
SFLASH_ALT_PROT_ROW63	0x0FFF83F
SFLASH_ALT_PROT_ROW64	0x0FFF840
SFLASH_ALT_PROT_ROW65	0x0FFF841
SFLASH_ALT_PROT_ROW66	0x0FFF842
SFLASH_ALT_PROT_ROW67	0x0FFF843
SFLASH_ALT_PROT_ROW68	0x0FFF844
SFLASH_ALT_PROT_ROW69	0x0FFF845
SFLASH_ALT_PROT_ROW70	0x0FFF846
SFLASH_ALT_PROT_ROW71	0x0FFF847
SFLASH_ALT_PROT_ROW72	0x0FFF848
SFLASH_ALT_PROT_ROW73	0x0FFF849
SFLASH_ALT_PROT_ROW74	0x0FFF84A
SFLASH_ALT_PROT_ROW75	0x0FFF84B
SFLASH_ALT_PROT_ROW76	0x0FFF84C
SFLASH_ALT_PROT_ROW77	0x0FFF84D
SFLASH_ALT_PROT_ROW78	0x0FFF84E
SFLASH_ALT_PROT_ROW79	0x0FFF84F
SFLASH_ALT_PROT_ROW80	0x0FFF850

Register Name	Address
SFLASH_ALT_PROT_ROW81	0x0FFF851
SFLASH_ALT_PROT_ROW82	0x0FFF852
SFLASH_ALT_PROT_ROW83	0x0FFF853
SFLASH_ALT_PROT_ROW84	0x0FFF854
SFLASH_ALT_PROT_ROW85	0x0FFF855
SFLASH_ALT_PROT_ROW86	0x0FFF856
SFLASH_ALT_PROT_ROW87	0x0FFF857
SFLASH_ALT_PROT_ROW88	0x0FFF858
SFLASH_ALT_PROT_ROW89	0x0FFF859
SFLASH_ALT_PROT_ROW90	0x0FFF85A
SFLASH_ALT_PROT_ROW91	0x0FFF85B
SFLASH_ALT_PROT_ROW92	0x0FFF85C
SFLASH_ALT_PROT_ROW93	0x0FFF85D
SFLASH_ALT_PROT_ROW94	0x0FFF85E
SFLASH_ALT_PROT_ROW95	0x0FFF85F
SFLASH_ALT_PROT_ROW96	0x0FFF860
SFLASH_ALT_PROT_ROW97	0x0FFF861
SFLASH_ALT_PROT_ROW98	0x0FFF862
SFLASH_ALT_PROT_ROW99	0x0FFF863
SFLASH_ALT_PROT_ROW100	0x0FFF864
SFLASH_ALT_PROT_ROW101	0x0FFF865
SFLASH_ALT_PROT_ROW102	0x0FFF866
SFLASH_ALT_PROT_ROW103	0x0FFF867
SFLASH_ALT_PROT_ROW104	0x0FFF868
SFLASH_ALT_PROT_ROW105	0x0FFF869
SFLASH_ALT_PROT_ROW106	0x0FFF86A
SFLASH_ALT_PROT_ROW107	0x0FFF86B
SFLASH_ALT_PROT_ROW108	0x0FFF86C
SFLASH_ALT_PROT_ROW109	0x0FFF86D
SFLASH_ALT_PROT_ROW110	0x0FFF86E
SFLASH_ALT_PROT_ROW111	0x0FFF86F
SFLASH_ALT_PROT_ROW112	0x0FFF870
SFLASH_ALT_PROT_ROW113	0x0FFF871
SFLASH_ALT_PROT_ROW114	0x0FFF872
SFLASH_ALT_PROT_ROW115	0x0FFF873
SFLASH_ALT_PROT_ROW116	0x0FFF874
SFLASH_ALT_PROT_ROW117	0x0FFF875
SFLASH_ALT_PROT_ROW118	0x0FFF876
SFLASH_ALT_PROT_ROW119	0x0FFF877
SFLASH_ALT_PROT_ROW120	0x0FFF878
SFLASH_ALT_PROT_ROW121	0x0FFF879
SFLASH_ALT_PROT_ROW122	0x0FFF87A

Register Name	Address
SFLASH_ALT_PROT_ROW123	0x0FFF87B
SFLASH_ALT_PROT_ROW124	0x0FFF87C
SFLASH_ALT_PROT_ROW125	0x0FFF87D
SFLASH_ALT_PROT_ROW126	0x0FFF87E
SFLASH_ALT_PROT_ROW127	0x0FFF87F
SFLASH_ALT_PROT_ROW128	0x0FFF880
SFLASH_ALT_PROT_ROW129	0x0FFF881
SFLASH_ALT_PROT_ROW130	0x0FFF882
SFLASH_ALT_PROT_ROW131	0x0FFF883
SFLASH_ALT_PROT_ROW132	0x0FFF884
SFLASH_ALT_PROT_ROW133	0x0FFF885
SFLASH_ALT_PROT_ROW134	0x0FFF886
SFLASH_ALT_PROT_ROW135	0x0FFF887
SFLASH_ALT_PROT_ROW136	0x0FFF888
SFLASH_ALT_PROT_ROW137	0x0FFF889
SFLASH_ALT_PROT_ROW138	0x0FFF88A
SFLASH_ALT_PROT_ROW139	0x0FFF88B
SFLASH_ALT_PROT_ROW140	0x0FFF88C
SFLASH_ALT_PROT_ROW141	0x0FFF88D
SFLASH_ALT_PROT_ROW142	0x0FFF88E
SFLASH_ALT_PROT_ROW143	0x0FFF88F
SFLASH_ALT_PROT_ROW144	0x0FFF890
SFLASH_ALT_PROT_ROW145	0x0FFF891
SFLASH_ALT_PROT_ROW146	0x0FFF892
SFLASH_ALT_PROT_ROW147	0x0FFF893
SFLASH_ALT_PROT_ROW148	0x0FFF894
SFLASH_ALT_PROT_ROW149	0x0FFF895
SFLASH_ALT_PROT_ROW150	0x0FFF896
SFLASH_ALT_PROT_ROW151	0x0FFF897
SFLASH_ALT_PROT_ROW152	0x0FFF898
SFLASH_ALT_PROT_ROW153	0x0FFF899
SFLASH_ALT_PROT_ROW154	0x0FFF89A
SFLASH_ALT_PROT_ROW155	0x0FFF89B
SFLASH_ALT_PROT_ROW156	0x0FFF89C
SFLASH_ALT_PROT_ROW157	0x0FFF89D
SFLASH_ALT_PROT_ROW158	0x0FFF89E
SFLASH_ALT_PROT_ROW159	0x0FFF89F
SFLASH_ALT_PROT_ROW160	0x0FFF8A0
SFLASH_ALT_PROT_ROW161	0x0FFF8A1
SFLASH_ALT_PROT_ROW162	0x0FFF8A2
SFLASH_ALT_PROT_ROW163	0x0FFF8A3
SFLASH_ALT_PROT_ROW164	0x0FFF8A4

Register Name	Address
SFLASH_ALT_PROT_ROW165	0x0FFF8A5
SFLASH_ALT_PROT_ROW166	0x0FFF8A6
SFLASH_ALT_PROT_ROW167	0x0FFF8A7
SFLASH_ALT_PROT_ROW168	0x0FFF8A8
SFLASH_ALT_PROT_ROW169	0x0FFF8A9
SFLASH_ALT_PROT_ROW170	0x0FFF8AA
SFLASH_ALT_PROT_ROW171	0x0FFF8AB
SFLASH_ALT_PROT_ROW172	0x0FFF8AC
SFLASH_ALT_PROT_ROW173	0x0FFF8AD
SFLASH_ALT_PROT_ROW174	0x0FFF8AE
SFLASH_ALT_PROT_ROW175	0x0FFF8AF
SFLASH_ALT_PROT_ROW176	0x0FFF8B0
SFLASH_ALT_PROT_ROW177	0x0FFF8B1
SFLASH_ALT_PROT_ROW178	0x0FFF8B2
SFLASH_ALT_PROT_ROW179	0x0FFF8B3
SFLASH_ALT_PROT_ROW180	0x0FFF8B4
SFLASH_ALT_PROT_ROW181	0x0FFF8B5
SFLASH_ALT_PROT_ROW182	0x0FFF8B6
SFLASH_ALT_PROT_ROW183	0x0FFF8B7
SFLASH_ALT_PROT_ROW184	0x0FFF8B8
SFLASH_ALT_PROT_ROW185	0x0FFF8B9
SFLASH_ALT_PROT_ROW186	0x0FFF8BA
SFLASH_ALT_PROT_ROW187	0x0FFF8BB
SFLASH_ALT_PROT_ROW188	0x0FFF8BC
SFLASH_ALT_PROT_ROW189	0x0FFF8BD
SFLASH_ALT_PROT_ROW190	0x0FFF8BE
SFLASH_ALT_PROT_ROW191	0x0FFF8BF
SFLASH_ALT_PROT_ROW192	0x0FFF8C0
SFLASH_ALT_PROT_ROW193	0x0FFF8C1
SFLASH_ALT_PROT_ROW194	0x0FFF8C2
SFLASH_ALT_PROT_ROW195	0x0FFF8C3
SFLASH_ALT_PROT_ROW196	0x0FFF8C4
SFLASH_ALT_PROT_ROW197	0x0FFF8C5
SFLASH_ALT_PROT_ROW198	0x0FFF8C6
SFLASH_ALT_PROT_ROW199	0x0FFF8C7
SFLASH_ALT_PROT_ROW200	0x0FFF8C8
SFLASH_ALT_PROT_ROW201	0x0FFF8C9
SFLASH_ALT_PROT_ROW202	0x0FFF8CA
SFLASH_ALT_PROT_ROW203	0x0FFF8CB
SFLASH_ALT_PROT_ROW204	0x0FFF8CC
SFLASH_ALT_PROT_ROW205	0x0FFF8CD
SFLASH_ALT_PROT_ROW206	0x0FFF8CE

Register Name	Address
SFLASH_ALT_PROT_ROW207	0x0FFF8CF
SFLASH_ALT_PROT_ROW208	0x0FFF8D0
SFLASH_ALT_PROT_ROW209	0x0FFF8D1
SFLASH_ALT_PROT_ROW210	0x0FFF8D2
SFLASH_ALT_PROT_ROW211	0x0FFF8D3
SFLASH_ALT_PROT_ROW212	0x0FFF8D4
SFLASH_ALT_PROT_ROW213	0x0FFF8D5
SFLASH_ALT_PROT_ROW214	0x0FFF8D6
SFLASH_ALT_PROT_ROW215	0x0FFF8D7
SFLASH_ALT_PROT_ROW216	0x0FFF8D8
SFLASH_ALT_PROT_ROW217	0x0FFF8D9
SFLASH_ALT_PROT_ROW218	0x0FFF8DA
SFLASH_ALT_PROT_ROW219	0x0FFF8DB
SFLASH_ALT_PROT_ROW220	0x0FFF8DC
SFLASH_ALT_PROT_ROW221	0x0FFF8DD
SFLASH_ALT_PROT_ROW222	0x0FFF8DE
SFLASH_ALT_PROT_ROW223	0x0FFF8DF
SFLASH_ALT_PROT_ROW224	0x0FFF8E0
SFLASH_ALT_PROT_ROW225	0x0FFF8E1
SFLASH_ALT_PROT_ROW226	0x0FFF8E2
SFLASH_ALT_PROT_ROW227	0x0FFF8E3
SFLASH_ALT_PROT_ROW228	0x0FFF8E4
SFLASH_ALT_PROT_ROW229	0x0FFF8E5
SFLASH_ALT_PROT_ROW230	0x0FFF8E6
SFLASH_ALT_PROT_ROW231	0x0FFF8E7
SFLASH_ALT_PROT_ROW232	0x0FFF8E8
SFLASH_ALT_PROT_ROW233	0x0FFF8E9
SFLASH_ALT_PROT_ROW234	0x0FFF8EA
SFLASH_ALT_PROT_ROW235	0x0FFF8EB
SFLASH_ALT_PROT_ROW236	0x0FFF8EC
SFLASH_ALT_PROT_ROW237	0x0FFF8ED
SFLASH_ALT_PROT_ROW238	0x0FFF8EE
SFLASH_ALT_PROT_ROW239	0x0FFF8EF
SFLASH_ALT_PROT_ROW240	0x0FFF8F0
SFLASH_ALT_PROT_ROW241	0x0FFF8F1
SFLASH_ALT_PROT_ROW242	0x0FFF8F2
SFLASH_ALT_PROT_ROW243	0x0FFF8F3
SFLASH_ALT_PROT_ROW244	0x0FFF8F4
SFLASH_ALT_PROT_ROW245	0x0FFF8F5
SFLASH_ALT_PROT_ROW246	0x0FFF8F6
SFLASH_ALT_PROT_ROW247	0x0FFF8F7
SFLASH_ALT_PROT_ROW248	0x0FFF8F8



Register Name	Address
SFLASH_ALT_PROT_ROW249	0x0FFF8F9
SFLASH_ALT_PROT_ROW250	0x0FFF8FA
SFLASH_ALT_PROT_ROW251	0x0FFF8FB
SFLASH_ALT_PROT_ROW252	0x0FFF8FC
SFLASH_ALT_PROT_ROW253	0x0FFF8FD
SFLASH_ALT_PROT_ROW254	0x0FFF8FE
SFLASH_ALT_PROT_ROW255	0x0FFF8FF
SFLASH_ALT_PP	0x0FFFB20
SFLASH_ALT_E	0x0FFFB24
SFLASH_ALT_P	0x0FFFB28
SFLASH_ALT_EA_E	0x0FFFB2C
SFLASH_ALT_EA_P	0x0FFFB30
SFLASH_ALT_ES_E	0x0FFFB34
SFLASH_ALT_ES_P_EO	0x0FFFB38
SFLASH_ALT_E_VCTAT	0x0FFFB3C
SFLASH_ALT_P_VCTAT	0x0FFFB3D

## 22.1.1 SFLASH\_PROT\_ROW0

Per Page Write Protection

Address: 0x0FFF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.2 SFLASH\_PROT\_ROW1

Per Page Write Protection

Address: 0x0FFF001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.3 SFLASH\_PROT\_ROW2

Per Page Write Protection

Address: 0x0FFF002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.4 SFLASH\_PROT\_ROW3

Per Page Write Protection

Address: 0x0FFF003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.5 SFLASH\_PROT\_ROW4

Per Page Write Protection

Address: 0x0FFF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.6 SFLASH\_PROT\_ROW5

Per Page Write Protection

Address: 0x0FFF005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.7 SFLASH\_PROT\_ROW6

Per Page Write Protection

Address: 0x0FFF006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.8 SFLASH\_PROT\_ROW7

Per Page Write Protection

Address: 0x0FFF007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.9 SFLASH\_PROT\_ROW8

Per Page Write Protection

Address: 0x0FFF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.10 SFLASH\_PROT\_ROW9

Per Page Write Protection

Address: 0x0FFF009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.11 SFLASH\_PROT\_ROW10

Per Page Write Protection

Address: 0x0FFF00A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.12 SFLASH\_PROT\_ROW11

Per Page Write Protection

Address: 0x0FFF00B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.13 SFLASH\_PROT\_ROW12

Per Page Write Protection

Address: 0x0FFF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.14 SFLASH\_PROT\_ROW13

Per Page Write Protection

Address: 0x0FFF00D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.15 SFLASH\_PROT\_ROW14

Per Page Write Protection

Address: 0x0FFF00E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.16 SFLASH\_PROT\_ROW15

Per Page Write Protection

Address: 0x0FFFF00F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.17 SFLASH\_PROT\_ROW16

Per Page Write Protection

Address: 0x0FFF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.18 SFLASH\_PROT\_ROW17

Per Page Write Protection

Address: 0x0FFF011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.19 SFLASH\_PROT\_ROW18

Per Page Write Protection

Address: 0x0FFF012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.20 SFLASH\_PROT\_ROW19

Per Page Write Protection

Address: 0x0FFF013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.21 SFLASH\_PROT\_ROW20

Per Page Write Protection

Address: 0x0FFF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.22 SFLASH\_PROT\_ROW21

Per Page Write Protection

Address: 0x0FFF015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.23 SFLASH\_PROT\_ROW22

Per Page Write Protection

Address: 0x0FFF016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.24 SFLASH\_PROT\_ROW23

Per Page Write Protection

Address: 0x0FFF017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.25 SFLASH\_PROT\_ROW24

Per Page Write Protection

Address: 0x0FFF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.26 SFLASH\_PROT\_ROW25

Per Page Write Protection

Address: 0x0FFF019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.27 SFLASH\_PROT\_ROW26

Per Page Write Protection

Address: 0x0FFF01A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.28 SFLASH\_PROT\_ROW27

Per Page Write Protection

Address: 0x0FFF01B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.29 SFLASH\_PROT\_ROW28

Per Page Write Protection

Address: 0x0FFF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.30 SFLASH\_PROT\_ROW29

Per Page Write Protection

Address: 0x0FFF01D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.31 SFLASH\_PROT\_ROW30

Per Page Write Protection

Address: 0x0FFF01E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.32 SFLASH\_PROT\_ROW31

Per Page Write Protection

Address: 0x0FFFF01F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.33 SFLASH\_PROT\_ROW32

Per Page Write Protection

Address: 0x0FFF020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.34 SFLASH\_PROT\_ROW33

Per Page Write Protection

Address: 0x0FFF021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.35 SFLASH\_PROT\_ROW34

Per Page Write Protection

Address: 0x0FFF022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.36 SFLASH\_PROT\_ROW35

Per Page Write Protection

Address: 0x0FFF023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.37 SFLASH\_PROT\_ROW36

Per Page Write Protection

Address: 0x0FFF024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.38 SFLASH\_PROT\_ROW37

Per Page Write Protection

Address: 0x0FFF025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.39 SFLASH\_PROT\_ROW38

Per Page Write Protection

Address: 0x0FFF026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.40 SFLASH\_PROT\_ROW39

Per Page Write Protection

Address: 0x0FFFF027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.41 SFLASH\_PROT\_ROW40

Per Page Write Protection

Address: 0x0FFF028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.42 SFLASH\_PROT\_ROW41

Per Page Write Protection

Address: 0x0FFF029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.43 SFLASH\_PROT\_ROW42

Per Page Write Protection

Address: 0x0FFF02A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.44 SFLASH\_PROT\_ROW43

Per Page Write Protection

Address: 0x0FFF02B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.45 SFLASH\_PROT\_ROW44

Per Page Write Protection

Address: 0x0FFF02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.46 SFLASH\_PROT\_ROW45

Per Page Write Protection

Address: 0x0FFF02D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.47 SFLASH\_PROT\_ROW46

Per Page Write Protection

Address: 0x0FFF02E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.48 SFLASH\_PROT\_ROW47

Per Page Write Protection

Address: 0x0FFFF02F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.49 SFLASH\_PROT\_ROW48

Per Page Write Protection

Address: 0x0FFF030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.50 SFLASH\_PROT\_ROW49

Per Page Write Protection

Address: 0x0FFF031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.51 SFLASH\_PROT\_ROW50

Per Page Write Protection

Address: 0x0FFF032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.52 SFLASH\_PROT\_ROW51

Per Page Write Protection

Address: 0x0FFF033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.53 SFLASH\_PROT\_ROW52

Per Page Write Protection

Address: 0x0FFF034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.54 SFLASH\_PROT\_ROW53

Per Page Write Protection

Address: 0x0FFF035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.55 SFLASH\_PROT\_ROW54

Per Page Write Protection

Address: 0x0FFF036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.56 SFLASH\_PROT\_ROW55

Per Page Write Protection

Address: 0x0FFF037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.57 SFLASH\_PROT\_ROW56

Per Page Write Protection

Address: 0x0FFF038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.58 SFLASH\_PROT\_ROW57

Per Page Write Protection

Address: 0x0FFF039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.59 SFLASH\_PROT\_ROW58

Per Page Write Protection

Address: 0x0FFF03A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.60 SFLASH\_PROT\_ROW59

Per Page Write Protection

Address: 0x0FFF03B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.61 SFLASH\_PROT\_ROW60

Per Page Write Protection

Address: 0x0FFF03C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.62 SFLASH\_PROT\_ROW61

Per Page Write Protection

Address: 0x0FFF03D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.63 SFLASH\_PROT\_ROW62

Per Page Write Protection

Address: 0x0FFF03E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.64 SFLASH\_PROT\_ROW63

Per Page Write Protection

Address: 0x0FFF03F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.65 SFLASH\_PROT\_PROTECTION

Protection Level

Address: 0x0FFFF0FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						None	
Name	None [7:2]						PROT_LEVEL [1:0]	

Bits	Name	Description
1 : 0	PROT_LEVEL	<p>Current Protection Mode - note that encoding is different from CPUSS_PROTECTION !! Default Value: X</p> <p><b>0x0: OPEN:</b> System is in OPEN mode</p> <p><b>0x1: VIRGIN:</b> System is in VIRGIN mode</p> <p><b>0x2: PROTECTED:</b> System is in PROTECTED mode</p> <p><b>0x3: KILL:</b> System is in KILL mode</p>

## 22.1.66 SFLASH\_AV\_PAIRS\_8B0

8b Addr/Value pair Section

Address: 0x0FFF100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.67 SFLASH\_AV\_PAIRS\_8B1

8b Addr/Value pair Section

Address: 0x0FFF101

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.68 SFLASH\_AV\_PAIRS\_8B2

8b Addr/Value pair Section

Address: 0x0FFF102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.69 SFLASH\_AV\_PAIRS\_8B3

8b Addr/Value pair Section

Address: 0x0FFF103

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.70 SFLASH\_AV\_PAIRS\_8B4

8b Addr/Value pair Section

Address: 0x0FFF104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.71 SFLASH\_AV\_PAIRS\_8B5

8b Addr/Value pair Section

Address: 0x0FFF105

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.72 SFLASH\_AV\_PAIRS\_8B6

8b Addr/Value pair Section

Address: 0x0FFF106

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.73 SFLASH\_AV\_PAIRS\_8B7

8b Addr/Value pair Section

Address: 0x0FFF107

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.74 SFLASH\_AV\_PAIRS\_8B8

8b Addr/Value pair Section

Address: 0x0FFF108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.75 SFLASH\_AV\_PAIRS\_8B9

8b Addr/Value pair Section

Address: 0x0FFF109

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.76 SFLASH\_AV\_PAIRS\_8B10

8b Addr/Value pair Section

Address: 0x0FFF10A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.77 SFLASH\_AV\_PAIRS\_8B11

8b Addr/Value pair Section

Address: 0x0FFF10B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.78 SFLASH\_AV\_PAIRS\_8B12

8b Addr/Value pair Section

Address: 0x0FFF10C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.79 SFLASH\_AV\_PAIRS\_8B13

8b Addr/Value pair Section

Address: 0x0FFF10D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.80 SFLASH\_AV\_PAIRS\_8B14

8b Addr/Value pair Section

Address: 0x0FFF10E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.81 SFLASH\_AV\_PAIRS\_8B15

8b Addr/Value pair Section

Address: 0x0FFFF10F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.82 SFLASH\_AV\_PAIRS\_8B16

8b Addr/Value pair Section

Address: 0x0FFFF110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.83 SFLASH\_AV\_PAIRS\_8B17

8b Addr/Value pair Section

Address: 0x0FFFF111

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.84 SFLASH\_AV\_PAIRS\_8B18

8b Addr/Value pair Section

Address: 0x0FFFF112

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.85 SFLASH\_AV\_PAIRS\_8B19

8b Addr/Value pair Section

Address: 0x0FFF113

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.86 SFLASH\_AV\_PAIRS\_8B20

8b Addr/Value pair Section

Address: 0x0FFFF114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.87 SFLASH\_AV\_PAIRS\_8B21

8b Addr/Value pair Section

Address: 0x0FFF115

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.88 SFLASH\_AV\_PAIRS\_8B22

8b Addr/Value pair Section

Address: 0x0FFF116

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.89 SFLASH\_AV\_PAIRS\_8B23

8b Addr/Value pair Section

Address: 0x0FFF117

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.90 SFLASH\_AV\_PAIRS\_8B24

8b Addr/Value pair Section

Address: 0x0FFF118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.91 SFLASH\_AV\_PAIRS\_8B25

8b Addr/Value pair Section

Address: 0x0FFFF119

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.92 SFLASH\_AV\_PAIRS\_8B26

8b Addr/Value pair Section

Address: 0x0FFFF11A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.93 SFLASH\_AV\_PAIRS\_8B27

8b Addr/Value pair Section

Address: 0x0FFFF11B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.94 SFLASH\_AV\_PAIRS\_8B28

8b Addr/Value pair Section

Address: 0x0FFFF11C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.95 SFLASH\_AV\_PAIRS\_8B29

8b Addr/Value pair Section

Address: 0x0FFFF11D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.96 SFLASH\_AV\_PAIRS\_8B30

8b Addr/Value pair Section

Address: 0x0FFFF11E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.97 SFLASH\_AV\_PAIRS\_8B31

8b Addr/Value pair Section

Address: 0x0FFFF11F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.98 SFLASH\_AV\_PAIRS\_8B32

8b Addr/Value pair Section

Address: 0x0FFF120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.99 SFLASH\_AV\_PAIRS\_8B33

8b Addr/Value pair Section

Address: 0x0FFFF121

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.100 SFLASH\_AV\_PAIRS\_8B34

8b Addr/Value pair Section

Address: 0x0FFF122

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.101 SFLASH\_AV\_PAIRS\_8B35

8b Addr/Value pair Section

Address: 0x0FFF123

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.102 SFLASH\_AV\_PAIRS\_8B36

8b Addr/Value pair Section

Address: 0x0FFF124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.103 SFLASH\_AV\_PAIRS\_8B37

8b Addr/Value pair Section

Address: 0x0FFF125

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.104 SFLASH\_AV\_PAIRS\_8B38

8b Addr/Value pair Section

Address: 0x0FFF126

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.105 SFLASH\_AV\_PAIRS\_8B39

8b Addr/Value pair Section

Address: 0x0FFFF127

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.106 SFLASH\_AV\_PAIRS\_8B40

8b Addr/Value pair Section

Address: 0x0FFF128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.107 SFLASH\_AV\_PAIRS\_8B41

8b Addr/Value pair Section

Address: 0x0FFF129

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.108 SFLASH\_AV\_PAIRS\_8B42

8b Addr/Value pair Section

Address: 0x0FFF12A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.109 SFLASH\_AV\_PAIRS\_8B43

8b Addr/Value pair Section

Address: 0x0FFF12B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.110 SFLASH\_AV\_PAIRS\_8B44

8b Addr/Value pair Section

Address: 0x0FFF12C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.111 SFLASH\_AV\_PAIRS\_8B45

8b Addr/Value pair Section

Address: 0x0FFF12D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.112 SFLASH\_AV\_PAIRS\_8B46

8b Addr/Value pair Section

Address: 0x0FFF12E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.113 SFLASH\_AV\_PAIRS\_8B47

8b Addr/Value pair Section

Address: 0x0FFFF12F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.114 SFLASH\_AV\_PAIRS\_8B48

8b Addr/Value pair Section

Address: 0x0FFFF130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.115 SFLASH\_AV\_PAIRS\_8B49

8b Addr/Value pair Section

Address: 0x0FFFF131

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.116 SFLASH\_AV\_PAIRS\_8B50

8b Addr/Value pair Section

Address: 0x0FFF132

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.117 SFLASH\_AV\_PAIRS\_8B51

8b Addr/Value pair Section

Address: 0x0FFF133

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.118 SFLASH\_AV\_PAIRS\_8B52

8b Addr/Value pair Section

Address: 0x0FFF134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.119 SFLASH\_AV\_PAIRS\_8B53

8b Addr/Value pair Section

Address: 0x0FFF135

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.120 SFLASH\_AV\_PAIRS\_8B54

8b Addr/Value pair Section

Address: 0x0FFF136

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.121 SFLASH\_AV\_PAIRS\_8B55

8b Addr/Value pair Section

Address: 0x0FFF137

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.122 SFLASH\_AV\_PAIRS\_8B56

8b Addr/Value pair Section

Address: 0x0FFF138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.123 SFLASH\_AV\_PAIRS\_8B57

8b Addr/Value pair Section

Address: 0x0FFF139

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.124 SFLASH\_AV\_PAIRS\_8B58

8b Addr/Value pair Section

Address: 0x0FFF13A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.125 SFLASH\_AV\_PAIRS\_8B59

8b Addr/Value pair Section

Address: 0x0FFF13B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.126 SFLASH\_AV\_PAIRS\_8B60

8b Addr/Value pair Section

Address: 0x0FFFF13C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.127 SFLASH\_AV\_PAIRS\_8B61

8b Addr/Value pair Section

Address: 0x0FFFF13D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.128 SFLASH\_AV\_PAIRS\_8B62

8b Addr/Value pair Section

Address: 0x0FFFF13E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.129 SFLASH\_AV\_PAIRS\_8B63

8b Addr/Value pair Section

Address: 0x0FFFF13F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.130 SFLASH\_AV\_PAIRS\_8B64

8b Addr/Value pair Section

Address: 0x0FFFF140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.131 SFLASH\_AV\_PAIRS\_8B65

8b Addr/Value pair Section

Address: 0x0FFFF141

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.132 SFLASH\_AV\_PAIRS\_8B66

8b Addr/Value pair Section

Address: 0x0FFFF142

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.133 SFLASH\_AV\_PAIRS\_8B67

8b Addr/Value pair Section

Address: 0x0FFFF143

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.134 SFLASH\_AV\_PAIRS\_8B68

8b Addr/Value pair Section

Address: 0x0FFF144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.135 SFLASH\_AV\_PAIRS\_8B69

8b Addr/Value pair Section

Address: 0x0FFF145

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.136 SFLASH\_AV\_PAIRS\_8B70

8b Addr/Value pair Section

Address: 0x0FFFF146

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.137 SFLASH\_AV\_PAIRS\_8B71

8b Addr/Value pair Section

Address: 0x0FFFF147

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.138 SFLASH\_AV\_PAIRS\_8B72

8b Addr/Value pair Section

Address: 0x0FFF148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.139 SFLASH\_AV\_PAIRS\_8B73

8b Addr/Value pair Section

Address: 0x0FFF149

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.140 SFLASH\_AV\_PAIRS\_8B74

8b Addr/Value pair Section

Address: 0x0FFF14A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.141 SFLASH\_AV\_PAIRS\_8B75

8b Addr/Value pair Section

Address: 0x0FFF14B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.142 SFLASH\_AV\_PAIRS\_8B76

8b Addr/Value pair Section

Address: 0x0FFF14C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.143 SFLASH\_AV\_PAIRS\_8B77

8b Addr/Value pair Section

Address: 0x0FFF14D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.144 SFLASH\_AV\_PAIRS\_8B78

8b Addr/Value pair Section

Address: 0x0FFF14E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.145 SFLASH\_AV\_PAIRS\_8B79

8b Addr/Value pair Section

Address: 0x0FFFF14F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.146 SFLASH\_AV\_PAIRS\_8B80

8b Addr/Value pair Section

Address: 0x0FFF150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.147 SFLASH\_AV\_PAIRS\_8B81

8b Addr/Value pair Section

Address: 0x0FFFF151

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.148 SFLASH\_AV\_PAIRS\_8B82

8b Addr/Value pair Section

Address: 0x0FFFF152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.149 SFLASH\_AV\_PAIRS\_8B83

8b Addr/Value pair Section

Address: 0x0FFFF153

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.150 SFLASH\_AV\_PAIRS\_8B84

8b Addr/Value pair Section

Address: 0x0FFF154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.151 SFLASH\_AV\_PAIRS\_8B85

8b Addr/Value pair Section

Address: 0x0FFF155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.152 SFLASH\_AV\_PAIRS\_8B86

8b Addr/Value pair Section

Address: 0x0FFF156

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.153 SFLASH\_AV\_PAIRS\_8B87

8b Addr/Value pair Section

Address: 0x0FFF157

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.154 SFLASH\_BLESS\_BB\_BUMP2

BLESS Bump bit for LDO BB, TXRX

Address: 0x0FFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	V2I [7:5]			V2I_RCAL [4:0]				

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	SY_IBIAS [15:13]			VBG_TRIM [12:10]			V2I [9:8]	

Bits	Name	Description
15 : 13	SY_IBIAS	3'b1xx: RCAL current bumped 3'b0xx: BG current bumped. 2'bx: represent current bump 01: +12.5%, 00: 0%, 11: -12.5%, 10:-25% Default Value: 0
12 : 10	VBG_TRIM	3d0: Trims the Bandgap voltage by 0% 3d1: Trims the Bandgap voltage by 1.6% 3d2: Trims the Bandgap voltage by 3.2% 3d3: Trims the Bandgap voltage by 4.8% 3d4: Trims the Bandgap voltage by 6.4% 3d5: Trims the Bandgap voltage by -4.8% 3d6: Trims the Bandgap voltage by -3.2% 3d7: Trims the Bandgap voltage by -1.6% Default Value: 0

## 22.1.154 SFLASH\_BLESS\_BB\_BUMP2 (continued)

9 : 5	V2I	<p>Bit[9]</p> <p>1: Error amp quiescent current is 5u</p> <p>0: Error amp quiescent current is 10u</p> <p>Bit[8:5]</p> <p>4d0: Trims the BGR current by 0%</p> <p>4d1: Trims the BGR current by -2.5%</p> <p>4d2: Trims the BGR current by -5%</p> <p>4d3: Trims the BGR current by -7.5%</p> <p>4d4: Trims the BGR current by -10%</p> <p>4d5: Trims the BGR current by -12.5%</p> <p>4d6: Trims the BGR current by -15%</p> <p>4d7: Trims the BGR current by -17.5%</p> <p>4d8: Trims the BGR current by 20%</p> <p>4d9: Trims the BGR current by 17.5%</p> <p>4d10: Trims the BGR current by 15%</p> <p>4d11: Trims the BGR current by 12.5%</p> <p>4d12: Trims the BGR current by 10%</p> <p>4d13: Trims the BGR current by 7.5%</p> <p>4d14: Trims the BGR current by 5%</p> <p>4d15: Trims the BGR current by 2.5%</p> <p>Default Value: 0</p>
4 : 0	V2I_RCAL	<p>Bit[4]</p> <p>1: Error amp quiescent current is 5u</p> <p>0: Error amp quiescent current is 10u</p> <p>Bit[3:0]</p> <p>4d0: Trims the RCAL current by 0%</p> <p>4d1: Trims the RCAL current by -2.5%</p> <p>4d2: Trims the RCAL current by -5%</p> <p>4d3: Trims the RCAL current by -7.5%</p> <p>4d4: Trims the RCAL current by -10%</p> <p>Default Value: 0</p>

## 22.1.155 SFLASH\_AV\_PAIRS\_8B88

8b Addr/Value pair Section

Address: 0x0FFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.156 SFLASH\_AV\_PAIRS\_8B89

8b Addr/Value pair Section

Address: 0x0FFF159

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.157 SFLASH\_BLESS\_BB\_XO

BLESS bump configuration 1

Address: 0x0FFF15A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	CTRL_VDDL_XO	CTRL_RC_FASTSTART_RES [6:5]		EN_AMPDET_FASTSTART	EN_AMPDET_CURMEAS	EN_CURMEAS	EN_RE_FASTSTART	DIS_XOCORE_SUPPLT

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	rev_bb_xo	CTRL_RPREF [14:13]		CTRL_VDDL_XB [12:10]			CTRL_VDDL_XO [9:8]	

Bits	Name	Description
15	rev_bb_xo	reserved for feature Default Value: 0
14 : 13	CTRL_RPREF	Controls the reference voltage fed as input to the regulators which generate vdd_xo and vdd_xb. 2d0 : 1.289V 2d0 : 1.227V 2d0 : 1.164V 2d0 : 1.382V Default Value: 0
12 : 10	CTRL_VDDL_XB	Controls the value of supply filter resistance in the inverter chain. This in turn controls the supply voltage at which the inverter chain runs. 3d0 : 1.028k 3d0 : 1.172k 3d0 : 1.367k 3d0 : 1.540k 3d0 : 1.889k 3d0 : 2.055k 3d0 : 0.503k 3d0 : 0.747k Default Value: 0
9 : 7	CTRL_VDDL_XO	Controls the value of supply filter resistance in the xo core. This in turn controls the supply voltage at which the core runs. 3d0 : 0.769k 3d0 : 0.877k 3d0 : 1.023k 3d0 : 1.152k 3d0 : 1.413k 3d0 : 1.537k 3d0 : 0.376k 3d0 : 0.559k Default Value: 0

## 22.1.157 SFLASH\_BLESS\_BB\_XO (continued)

6 : 5	CTRL_RC_FASTSTART_RES	Controls the time constant with which the surge current from rc_faststart block decays down to zero. 2d0 : 387us 2d1 : 309us 2d2 : 232us 2d3 : 464us Default Value: 0
4	EN_AMPDET_FASTSTART	This bit is used to force startup of the vtnbyr circuit in the biasgen_and_reg block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
3	EN_AMPDET_CURMEAS	This bit can be used to disable all the caps on both X1 node and X2 node. 1d0 : Caps Enabled 1d1 : Caps disabled. Even when all the caps are disabled, due to finite on/off ratio of the caps, the cap on both X1 and X2 node is still 3.69pF Default Value: 0
2	EN_CURMEAS	This bit is used to force startup of the positive feedback loop in the amplitude detect block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
1	EN_RE_FASTSTART	Enables/Disables the RC faststart block in the XO. When enabled, this block provides a surge current at xo startup to reduce the settling time of the XO. 1: RC Fast start in XO is enabled 0: RC Fast start in XO is disabled Default Value: 0
0	DIS_XOCORE_SUPFILT	Enables/Disables the supply filter of the XO core. 1: Disabled 0: Enabled Default Value: 0



## 22.1.158 SFLASH\_AV\_PAIRS\_8B90

8b Addr/Value pair Section

Address: 0x0FFF15A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.159 SFLASH\_AV\_PAIRS\_8B91

8b Addr/Value pair Section

Address: 0x0FFF15B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.160 SFLASH\_BLESS\_SY\_BUMP1

BLESS SY bump bits configuration 1

Address: 0x0FFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW			
HW Access	R	R		R	R			
Name	LDOLO_FORCE_STARTUP	IBIAS_LOPATH [6:5]		LOFB_POWER_SAVE	VCO [3:0]			

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDCPLPF [15:12]				LOPATH [11:8]			

Bits	Name	Description																		
15 : 12	PDCPLPF	<p>Bump for PD CP and LPF blocks.[2:0] is used to get range of -20%to +15% in 5% steps.</p> <table><thead><tr><th>ICP_BUMP[2:0]</th><th>ICP</th></tr></thead><tbody><tr><td>1 0 0</td><td>-20%</td></tr><tr><td>1 0 1</td><td>-15%</td></tr><tr><td>1 1 0</td><td>-10%</td></tr><tr><td>1 1 1</td><td>-05%</td></tr><tr><td>0 0 0</td><td>00%</td></tr><tr><td>0 0 1</td><td>05%</td></tr><tr><td>0 1 0</td><td>10%</td></tr><tr><td>0 1 1</td><td>15%.</td></tr></tbody></table> <p>Default Value: 0</p>	ICP_BUMP[2:0]	ICP	1 0 0	-20%	1 0 1	-15%	1 1 0	-10%	1 1 1	-05%	0 0 0	00%	0 0 1	05%	0 1 0	10%	0 1 1	15%.
ICP_BUMP[2:0]	ICP																			
1 0 0	-20%																			
1 0 1	-15%																			
1 1 0	-10%																			
1 1 1	-05%																			
0 0 0	00%																			
0 0 1	05%																			
0 1 0	10%																			
0 1 1	15%.																			
11 : 8	LOPATH	<p>Bump bits for LO path bulk bias. Goes to DIVN/FCAL/LOPATH for bumps. 2 bits for pBulk [3:2] and 2 bits for nBulk[1:0].</p> <table><thead><tr><th>bump</th><th>pbulk</th></tr></thead><tbody><tr><td>0 0</td><td>vddx-380mV</td></tr><tr><td>0 1</td><td>vddx-320mV</td></tr><tr><td>1 0</td><td>vddx-440mV</td></tr><tr><td>1 1</td><td>vddx</td></tr></tbody></table> <p>Default Value: 5</p>	bump	pbulk	0 0	vddx-380mV	0 1	vddx-320mV	1 0	vddx-440mV	1 1	vddx								
bump	pbulk																			
0 0	vddx-380mV																			
0 1	vddx-320mV																			
1 0	vddx-440mV																			
1 1	vddx																			
7	LDOLO_FORCE_STARTUP	<p>1: force start-up of the VT/R circuit in VCOLOPATH LCO</p> <p>0: no force start-up</p> <p>Default Value: 0</p>																		
6 : 5	IBIAS_LOPATH	<p>bump bits for clkbias in lopath</p> <table><thead><tr><th>bump</th><th>clk bias pM</th><th>clk bias nM</th></tr></thead><tbody><tr><td>0 0</td><td>vddo-vgsp</td><td>vgasn</td></tr><tr><td>0 1</td><td>vddlo-vgsp-100m</td><td>vgasn+100m</td></tr><tr><td>1 0</td><td>vddlo-vgsp-200m</td><td>vgasn+200m</td></tr><tr><td>1 1</td><td>vddlo-vgsp-400m</td><td>vgasn+400m</td></tr></tbody></table> <p>Default Value: 0</p>	bump	clk bias pM	clk bias nM	0 0	vddo-vgsp	vgasn	0 1	vddlo-vgsp-100m	vgasn+100m	1 0	vddlo-vgsp-200m	vgasn+200m	1 1	vddlo-vgsp-400m	vgasn+400m			
bump	clk bias pM	clk bias nM																		
0 0	vddo-vgsp	vgasn																		
0 1	vddlo-vgsp-100m	vgasn+100m																		
1 0	vddlo-vgsp-200m	vgasn+200m																		
1 1	vddlo-vgsp-400m	vgasn+400m																		

## 22.1.160 SFLASH\_BLESS\_SY\_BUMP1 (continued)

4	LOFB_POWERSAVE	1: enable powersave for LOFB buffer 0: disable powersave for LOFB buffer Default Value: 0
3 : 0	VCO	Bump bits for SY VCO block. Rt VCO (2 bits) - sy_bump1_vco [3:2] 00 ~ 50 Ohms 01 ~ 30 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms and Rb VCO (2 bits) - sy_bump1_vco[1:0] 00 ~ 58 Ohms 01 ~ 39 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms Default Value: 5

## 22.1.161 SFLASH\_AV\_PAIRS\_8B92

8b Addr/Value pair Section

Address: 0x0FFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.162 SFLASH\_AV\_PAIRS\_8B93

8b Addr/Value pair Section

Address: 0x0FFF15D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.163 SFLASH\_BLESS\_LDO

BLESS bump bit for LDO

Address: 0x0FFF15E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW		RW		
HW Access	R	R		R		R		
Name	BUMP_SY_LHV	BUMP_SY_LOPATH [6:5]		BUMP_SY_VCO [4:3]		BUMP_BALUM_HF [2:0]		

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			RW
HW Access	R				R			R
Name	REV_LDO [15:12]				BUMP_SY_FFFB [11:9]			BUMP_SY_LHV

Bits	Name	Description
15 : 12	REV_LDO	received for feature Default Value: 0
11 : 9	BUMP_SY_FFFB	3d0: FF and FB LDO outputs are 1.800V 3d1: FF and FB LDO outputs are 1.846V 3d2: FF and FB LDO outputs are 1.894V 3d3: FF and FB LDO outputs are 1.946V 3d4: FF and FB LDO outputs are 2.000V 3d5: FF and FB LDO outputs are 1.649V 3d6: FF and FB LDO outputs are 1.701V 3d7: FF and FB LDO outputs are 1.756V Default Value: 0
8 : 7	BUMP_SY_LHV	2d0: HV LDO outputs are 1.894V 2d1: HV LDO outputs are 2.000V 2d2: HV LDO outputs are 1.800V 2d3: HV LDO outputs are 1.846V Default Value: 0
6 : 5	BUMP_SY_LOPATH	2d0: LOPATH LDO outputs are 1.762V 2d1: LOPATH LDO outputs are 1.861V 2d2: LOPATH LDO outputs are 1.673V 2d3: LOPATH LDO outputs are 1.716V Default Value: 0
4 : 3	BUMP_SY_VCO	2d0: VCO LDO outputs are 1.413V 2d1: VCO LDO outputs are 1.494V 2d2: VCO LDO outputs are 1.329V 2d3: VCO LDO outputs are 1.371V Default Value: 0

### 22.1.163 SFLASH\_BLESS\_LDO (continued)

2 : 0	BUMP_BALUM_HF	3d0: HF LDO output is 1.800V 3d1: HF LDO output is 1.846V 3d2: HF LDO output is 1.894V 3d3: HF LDO output is 1.946V Default Value: 0
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## 22.1.164 SFLASH\_AV\_PAIRS\_8B94

8b Addr/Value pair Section

Address: 0x0FFF15E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.165 SFLASH\_AV\_PAIRS\_8B95

8b Addr/Value pair Section

Address: 0x0FFFF15F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.166 SFLASH\_AV\_PAIRS\_8B96

8b Addr/Value pair Section

Address: 0x0FFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.167 SFLASH\_AV\_PAIRS\_8B97

8b Addr/Value pair Section

Address: 0x0FFFF161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.168 SFLASH\_AV\_PAIRS\_8B98

8b Addr/Value pair Section

Address: 0x0FFF162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.169 SFLASH\_AV\_PAIRS\_8B99

8b Addr/Value pair Section

Address: 0x0FFF163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.170 SFLASH\_AV\_PAIRS\_8B100

8b Addr/Value pair Section

Address: 0x0FFF164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.171 SFLASH\_AV\_PAIRS\_8B101

8b Addr/Value pair Section

Address: 0x0FFF165

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.172 SFLASH\_AV\_PAIRS\_8B102

8b Addr/Value pair Section

Address: 0x0FFF166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.173 SFLASH\_AV\_PAIRS\_8B103

8b Addr/Value pair Section

Address: 0x0FFF167

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.174 SFLASH\_AV\_PAIRS\_8B104

8b Addr/Value pair Section

Address: 0x0FFF168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.175 SFLASH\_AV\_PAIRS\_8B105

8b Addr/Value pair Section

Address: 0x0FFF169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.176 SFLASH\_AV\_PAIRS\_8B106

8b Addr/Value pair Section

Address: 0x0FFF16A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.177 SFLASH\_AV\_PAIRS\_8B107

8b Addr/Value pair Section

Address: 0x0FFF16B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.178 SFLASH\_AV\_PAIRS\_8B108

8b Addr/Value pair Section

Address: 0x0FFF16C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.179 SFLASH\_AV\_PAIRS\_8B109

8b Addr/Value pair Section

Address: 0x0FFF16D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.180 SFLASH\_AV\_PAIRS\_8B110

8b Addr/Value pair Section

Address: 0x0FFF16E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.181 SFLASH\_AV\_PAIRS\_8B111

8b Addr/Value pair Section

Address: 0x0FFFF16F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.182 SFLASH\_AV\_PAIRS\_8B112

8b Addr/Value pair Section

Address: 0x0FFF170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.183 SFLASH\_AV\_PAIRS\_8B113

8b Addr/Value pair Section

Address: 0x0FFFF171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.184 SFLASH\_AV\_PAIRS\_8B114

8b Addr/Value pair Section

Address: 0x0FFF172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.185 SFLASH\_AV\_PAIRS\_8B115

8b Addr/Value pair Section

Address: 0x0FFF173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.186 SFLASH\_AV\_PAIRS\_8B116

8b Addr/Value pair Section

Address: 0x0FFF174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.187 SFLASH\_AV\_PAIRS\_8B117

8b Addr/Value pair Section

Address: 0x0FFF175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.188 SFLASH\_AV\_PAIRS\_8B118

8b Addr/Value pair Section

Address: 0x0FFF176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.189 SFLASH\_AV\_PAIRS\_8B119

8b Addr/Value pair Section

Address: 0x0FFF177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.190 SFLASH\_AV\_PAIRS\_8B120

8b Addr/Value pair Section

Address: 0x0FFF178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.191 SFLASH\_AV\_PAIRS\_8B121

8b Addr/Value pair Section

Address: 0x0FFF179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.192 SFLASH\_AV\_PAIRS\_8B122

8b Addr/Value pair Section

Address: 0x0FFF17A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.193 SFLASH\_AV\_PAIRS\_8B123

8b Addr/Value pair Section

Address: 0x0FFF17B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.194 SFLASH\_AV\_PAIRS\_8B124

8b Addr/Value pair Section

Address: 0x0FFF17C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.195 SFLASH\_AV\_PAIRS\_8B125

8b Addr/Value pair Section

Address: 0x0FFF17D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X



## 22.1.196 SFLASH\_AV\_PAIRS\_8B126

8b Addr/Value pair Section

Address: 0x0FFF17E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.197 SFLASH\_AV\_PAIRS\_8B127

8b Addr/Value pair Section

Address: 0x0FFFF17F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

## 22.1.198 SFLASH\_AV\_PAIRS\_32B0

32b Addr/Value pair Section

Address: 0x0FFF200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.199 SFLASH\_AV\_PAIRS\_32B1

32b Addr/Value pair Section

Address: 0x0FFF204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.200 SFLASH\_AV\_PAIRS\_32B2

32b Addr/Value pair Section

Address: 0x0FFF208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.201 SFLASH\_AV\_PAIRS\_32B3

32b Addr/Value pair Section

Address: 0x0FFFF20C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.202 SFLASH\_AV\_PAIRS\_32B4

32b Addr/Value pair Section

Address: 0x0FFF210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.203 SFLASH\_AV\_PAIRS\_32B5

32b Addr/Value pair Section

Address: 0x0FFFF214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X



## 22.1.204 SFLASH\_AV\_PAIRS\_32B6

32b Addr/Value pair Section

Address: 0x0FFF218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.205 SFLASH\_AV\_PAIRS\_32B7

32b Addr/Value pair Section

Address: 0x0FFFF21C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.206 SFLASH\_AV\_PAIRS\_32B8

32b Addr/Value pair Section

Address: 0x0FFF220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.207 SFLASH\_AV\_PAIRS\_32B9

32b Addr/Value pair Section

Address: 0x0FFF224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.208 SFLASH\_AV\_PAIRS\_32B10

32b Addr/Value pair Section

Address: 0x0FFF228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.209 SFLASH\_AV\_PAIRS\_32B11

32b Addr/Value pair Section

Address: 0x0FFFF22C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.210 SFLASH\_AV\_PAIRS\_32B12

32b Addr/Value pair Section

Address: 0x0FFFF230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.211 SFLASH\_AV\_PAIRS\_32B13

32b Addr/Value pair Section

Address: 0x0FFFF234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X



## 22.1.212 SFLASH\_AV\_PAIRS\_32B14

32b Addr/Value pair Section

Address: 0x0FFF238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.213 SFLASH\_AV\_PAIRS\_32B15

32b Addr/Value pair Section

Address: 0x0FFFF23C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

## 22.1.214 SFLASH\_CPUS\_WOUNDING

CPUS Wounding Register

Address: 0x0FFF240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Data to use for register Default Value: X

## 22.1.215 SFLASH\_SILICON\_ID

Silicon ID

Address: 0x0FFFF244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ID [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ID [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

## 22.1.216 SFLASH\_CPUSS\_PRIV\_RAM

RAM Privileged Limit

Address: 0x0FFF248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RAM_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RAM_PROT_LIMIT

Bits	Name	Description
8 : 0	RAM_PROT_LIMIT	<p>Indicates the limit where the privileged area of SRAM starts in increments of 256 Bytes.</p> <p>"0": Entire SRAM is Privileged.</p> <p>"1": First 256 Bytes are User accessible.</p> <p>Any number larger than the size of the SRAM indicates that the entire SRAM is user mode accessible.</p> <p>Default Value: 0</p>

## 22.1.217 SFLASH\_CPUSS\_PRIV\_ROM\_BROM

Boot ROM Privileged Limit

Address: 0x0FFF24A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BROM_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 0	BROM_PROT_LIMIT	<p>Indicates the limit where the privileged area of the Boot ROM partition starts in increments of 256 Bytes.</p> <p>"0": Entire Boot ROM is Privileged.</p> <p>"1": First 256 Bytes are User accessible.</p> <p>...</p> <p>BROM_PROT_LIMIT &gt;= "Boot ROM partition capacity": Entire Boot ROM partition is user mode accessible.</p> <p>Default Value: 0</p>

## 22.1.218 SFLASH\_CPUSS\_PRIV\_FLASH

Flash Privileged Limit

Address: 0x0FFFF24C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLASH_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					FLASH_PROT_LIMIT [10:8]		

Bits	Name	Description
10 : 0	FLASH_PROT_LIMIT	<p>Indicates the limit where the privileged area of flash starts in increments of 256 Bytes.</p> <p>"0": Entire flash is Privileged.</p> <p>"1": First 256 Bytes are User accessible.</p> <p>Any number larger than the size of the flash indicates that the entire flash is user mode accessible. Note that SuperVisory rows are always User accessible.</p> <p>If FLASH_PROT_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using SYSREQ.</p> <p>Default Value: 0</p>

## 22.1.219 SFLASH\_CPUSS\_PRIV\_ROM\_SROM

System ROM Privileged Limit

Address: 0x0FFFF24E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SROM_PROT_LIMIT [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SROM_PROT_LIMIT [9:8]	

Bits	Name	Description
9 : 0	SROM_PROT_LIMIT	<p>Indicates the limit where the privileged area of System ROM partition starts in increments of 256 Bytes. The limit is wrt. the start of the ROM memory (start of the Boot ROM partition).</p> <p>SROM_PROT_LIMIT * 256 Byte &lt;= "Boot ROM partition capacity": Entire System ROM is Privileged.</p> <p>SROM_PROT_LIMIT * 256 Byte &gt; "Boot ROM partition capacity": First SROM_PROT_LIMIT * 256 - "Boot ROM partition capacity" Bytes are User accessible.</p> <p>...</p> <p>SROM_PROT_LIMIT &gt;= "ROM capacity": Entire System ROM is user mode accessible.</p> <p>Default Value: 0</p>



## 22.1.220 SFLASH\_HIB\_KEY\_DELAY

Hibernate wakeup value for PWR\_KEY\_DELAY

Address: 0x0FFFF250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

## 22.1.221 SFLASH\_DPSLP\_KEY\_DELAY

DeepSleep wakeup value for PWR\_KEY\_DELAY

Address: 0x0FFF252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

## 22.1.222 SFLASH\_SWD\_CONFIG

SWD pinout selector (not present in TSG4/TSG5-M)

Address: 0x0FFF254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							None
Name	None [7:1]							SWD_SELECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X

## 22.1.223 SFLASH\_INITIAL\_SPCIF\_TRIM\_M1\_DAC0

FLASH IDAC trim used during boot

Address: 0x0FFF255

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	SLOPE [7:5]			IDAC [4:0]				

Bits	Name	Description
7 : 5	SLOPE	See SPCIF_TRIM1 Default Value: 0
4 : 0	IDAC	See SPCIF_TRIM1 Default Value: 0

## 22.1.224 SFLASH\_SWD\_LISTEN

Listen Window Length

Address: 0x0FFF258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CYCLES [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CYCLES [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	CYCLES [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

## 22.1.225 SFLASH\_FLASH\_START

Flash Image Start Address

Address: 0x0FFFF25C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ADDRESS [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ADDRESS [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	ADDRESS [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

## 22.1.226 SFLASH\_CSD\_TRIM1\_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFF260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

## 22.1.227 SFLASH\_CSD\_TRIM2\_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF261

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X



## 22.1.228 SFLASH\_CSD\_TRIM1\_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

## 22.1.229 SFLASH\_CSD\_TRIM2\_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF263

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

## 22.1.230 SFLASH\_SAR\_TEMP\_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFF264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

## 22.1.231 SFLASH\_SAR\_TEMP\_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFF266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

## 22.1.232 SFLASH\_SKIP\_CHECKSUM

Checksum Skip Option Register

Address: 0x0FFF269

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SKIP [7:0]							

Bits	Name	Description
7 : 0	SKIP	0: Perform checksum check (see CHECKSUM fuel below) 1: Skip checksum check >1: Undefined - do not use Default Value: X

## 22.1.233 SFLASH\_PROT\_VIRGINKEY0

Virgin Protection Mode Key

Address: 0x0FFF270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 22.1.234 SFLASH\_PROT\_VIRGINKEY1

Virgin Protection Mode Key

Address: 0x0FFFF271

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 22.1.235 SFLASH\_PROT\_VIRGINKEY2

Virgin Protection Mode Key

Address: 0x0FFF272

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X



## 22.1.236 SFLASH\_PROT\_VIRGINKEY3

Virgin Protection Mode Key

Address: 0x0FFFF273

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 22.1.237 SFLASH\_PROT\_VIRGINKEY4

Virgin Protection Mode Key

Address: 0x0FFFF274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 22.1.238 SFLASH\_PROT\_VIRGINKEY5

Virgin Protection Mode Key

Address: 0x0FFFF275

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 22.1.239 SFLASH\_PROT\_VIRGINKEY6

Virgin Protection Mode Key

Address: 0x0FFF276

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 22.1.240 SFLASH\_PROT\_VIRGINKEY7

Virgin Protection Mode Key

Address: 0x0FFFF277

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

## 22.1.241 SFLASH\_DIE\_LOT0

Lot Number (3 bytes)

Address: 0x0FFF278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

## 22.1.242 SFLASH\_DIE\_LOT1

Lot Number (3 bytes)

Address: 0x0FFFF279

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

## 22.1.243 SFLASH\_DIE\_LOT2

Lot Number (3 bytes)

Address: 0x0FFF27A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X



## 22.1.244 SFLASH\_DIE\_WAFER

Wafer Number

Address: 0x0FFFF27B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	WAFER [7:0]							

Bits	Name	Description
7 : 0	WAFER	Wafer Number Default Value: X

## 22.1.245 SFLASH\_DIE\_X

X Position on Wafer, CRI Pass/Fail Bin

Address: 0x0FFFF27C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	X [7:0]							

Bits	Name	Description
7 : 0	X	X Position Default Value: X

## 22.1.246 SFLASH\_DIE\_Y

Y Position on Wafer, CHI Pass/Fail Bin

Address: 0x0FFFF27D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	Y [7:0]							

Bits	Name	Description
7 : 0	Y	Y Position Default Value: X

## 22.1.247 SFLASH\_DIE\_SORT

Sort1/2/3 Pass/Fail Bin

Address: 0x0FFFF27E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		None	None	None	None	None	None
Name	None [7:6]		ENG_PASS	CHI_PASS	CRI_PASS	S3_PASS	S2_PASS	S1_PASS

Bits	Name	Description
5	ENG_PASS	ENG Pass Bin Default Value: X
4	CHI_PASS	CHI Pass Bin (1) or 0 (Fail Bin) Default Value: X
3	CRI_PASS	CRI Pass Bin (1) or 0 (Fail Bin) Default Value: X
2	S3_PASS	SORT3 Pass Bin (1) or 0 (Fail Bin) Default Value: X
1	S2_PASS	SORT2 Pass Bin (1) or 0 (Fail Bin) Default Value: X
0	S1_PASS	SORT1 Pass Bin (1) or 0 (Fail Bin) Default Value: X

## 22.1.248 SFLASH\_DIE\_MINOR

Minor Revision Number

Address: 0x0FFFF27F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Minor revision number Default Value: X

## 22.1.249 SFLASH\_PE\_TE\_DATA0

PE/TE Data

Address: 0x0FFF300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.250 SFLASH\_PE\_TE\_DATA1

PE/TE Data

Address: 0x0FFFF301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.251 SFLASH\_PE\_TE\_DATA2

PE/TE Data

Address: 0x0FFF302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 22.1.252 SFLASH\_PE\_TE\_DATA3

PE/TE Data

Address: 0x0FFF303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.253 SFLASH\_PE\_TE\_DATA4

PE/TE Data

Address: 0x0FFF304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.254 SFLASH\_PE\_TE\_DATA5

PE/TE Data

Address: 0x0FFF305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.255 SFLASH\_PE\_TE\_DATA6

PE/TE Data

Address: 0x0FFFF306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.256 SFLASH\_PE\_TE\_DATA7

PE/TE Data

Address: 0x0FFF307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.257 SFLASH\_PE\_TE\_DATA8

PE/TE Data

Address: 0x0FFF308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.258 SFLASH\_PE\_TE\_DATA9

PE/TE Data

Address: 0x0FFFF309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.259 SFLASH\_PE\_TE\_DATA10

PE/TE Data

Address: 0x0FFF30A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 22.1.260 SFLASH\_PE\_TE\_DATA11

PE/TE Data

Address: 0x0FFF30B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.261 SFLASH\_PE\_TE\_DATA12

PE/TE Data

Address: 0x0FFFF30C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.262 SFLASH\_PE\_TE\_DATA13

PE/TE Data

Address: 0x0FFFF30D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.263 SFLASH\_PE\_TE\_DATA14

PE/TE Data

Address: 0x0FFF30E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.264 SFLASH\_PE\_TE\_DATA15

PE/TE Data

Address: 0x0FFFF30F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.265 SFLASH\_PE\_TE\_DATA16

PE/TE Data

Address: 0x0FFF310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.266 SFLASH\_PE\_TE\_DATA17

PE/TE Data

Address: 0x0FFFF311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.267 SFLASH\_PE\_TE\_DATA18

PE/TE Data

Address: 0x0FFFF312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 22.1.268 SFLASH\_PE\_TE\_DATA19

PE/TE Data

Address: 0x0FFF313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.269 SFLASH\_PE\_TE\_DATA20

PE/TE Data

Address: 0x0FFFF314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.270 SFLASH\_PE\_TE\_DATA21

PE/TE Data

Address: 0x0FFF315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.271 SFLASH\_PE\_TE\_DATA22

PE/TE Data

Address: 0x0FFF316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.272 SFLASH\_PE\_TE\_DATA23

PE/TE Data

Address: 0x0FFFF317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.273 SFLASH\_PE\_TE\_DATA24

PE/TE Data

Address: 0x0FFF318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.274 SFLASH\_PE\_TE\_DATA25

PE/TE Data

Address: 0x0FFF319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.275 SFLASH\_PE\_TE\_DATA26

PE/TE Data

Address: 0x0FFFF31A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X



## 22.1.276 SFLASH\_PE\_TE\_DATA27

PE/TE Data

Address: 0x0FFF31B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.277 SFLASH\_PE\_TE\_DATA28

PE/TE Data

Address: 0x0FFFF31C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.278 SFLASH\_PE\_TE\_DATA29

PE/TE Data

Address: 0x0FFFF31D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.279 SFLASH\_PE\_TE\_DATA30

PE/TE Data

Address: 0x0FFFF31E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.280 SFLASH\_PE\_TE\_DATA31

PE/TE Data

Address: 0x0FFFF31F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

## 22.1.281 SFLASH\_PP

Preprogram Settings

Address: 0x0FFF320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.282 SFLASH\_E

Erase Settings

Address: 0x0FFF324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.283 SFLASH\_P

Program Settings

Address: 0x0FFF328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X



## 22.1.284 SFLASH\_EA\_E

Erase All - Erase Settings

Address: 0x0FFF32C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.285 SFLASH\_EA\_P

Erase All - Program Settings

Address: 0x0FFF330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.286 SFLASH\_ES\_E

Erase Sector - Erase Settings

Address: 0x0FFF334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.287 SFLASH\_ES\_P\_EO

Erase Sector - Program EO Settings

Address: 0x0FFFF338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.288 SFLASH\_E\_VCTAT

Bandgap Trim Register

Address: 0x0FFF33C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

## 22.1.289 SFLASH\_P\_VCTAT

Bandgap Trim Register

Address: 0x0FFF33D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_EN ABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

## 22.1.290 SFLASH\_IMO\_MAXF0

Max frequency for trim pair

Address: 0x0FFF340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

## 22.1.291 SFLASH\_IMO\_ABS0

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFF341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X



## 22.1.292 SFLASH\_IMO\_TMPCO0

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFF342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 22.1.293 SFLASH\_IMO\_MAXF1

Max frequency for trim pair

Address: 0x0FFF343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

## 22.1.294 SFLASH\_IMO\_ABS1

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFF344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

## 22.1.295 SFLASH\_IMO\_TMPCO1

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 22.1.296 SFLASH\_IMO\_MAXF2

Max frequency for trim pair

Address: 0x0FFF346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

## 22.1.297 SFLASH\_IMO\_ABS2

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFF347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

## 22.1.298 SFLASH\_IMO\_TMPCO2

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFF348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 22.1.299 SFLASH\_IMO\_MAXF3

Max frequency for trim pair

Address: 0x0FFF349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X



## 22.1.300 SFLASH\_IMO\_ABS3

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFF34A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

## 22.1.301 SFLASH\_IMO\_TMPCO3

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFF34B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 22.1.302 SFLASH\_IMO\_ABS4

Value for PWR\_BG\_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFF34C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None		RW					
<b>HW Access</b>	None		None					
<b>Name</b>	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

## 22.1.303 SFLASH\_IMO\_TMPCO4

Value for PWR\_BG\_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF34D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

## 22.1.304 SFLASH\_IMO\_TRIM0

IMO Trim Register (SRSSv2)

Address: 0x0FFF350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.305 SFLASH\_IMO\_TRIM1

IMO Trim Register (SRSSv2)

Address: 0x0FFF351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.306 SFLASH\_IMO\_TRIM2

IMO Trim Register (SRSSv2)

Address: 0x0FFF352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.307 SFLASH\_IMO\_TRIM3

IMO Trim Register (SRSSv2)

Address: 0x0FFFF353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 22.1.308 SFLASH\_IMO\_TRIM4

IMO Trim Register (SRSSv2)

Address: 0x0FFF354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.309 SFLASH\_IMO\_TRIM5

IMO Trim Register (SRSSv2)

Address: 0x0FFF355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.310 SFLASH\_IMO\_TRIM6

IMO Trim Register (SRSSv2)

Address: 0x0FFF356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.311 SFLASH\_IMO\_TRIM7

IMO Trim Register (SRSSv2)

Address: 0x0FFF357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.312 SFLASH\_IMO\_TRIM8

IMO Trim Register (SRSSv2)

Address: 0x0FFF358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.313 SFLASH\_IMO\_TRIM9

IMO Trim Register (SRSSv2)

Address: 0x0FFF359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.314 SFLASH\_IMO\_TRIM10

IMO Trim Register (SRSSv2)

Address: 0x0FFF35A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.315 SFLASH\_IMO\_TRIM11

IMO Trim Register (SRSSv2)

Address: 0x0FFF35B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 22.1.316 SFLASH\_IMO\_TRIM12

IMO Trim Register (SRSSv2)

Address: 0x0FFF35C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.317 SFLASH\_IMO\_TRIM13

IMO Trim Register (SRSSv2)

Address: 0x0FFF35D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.318 SFLASH\_IMO\_TRIM14

IMO Trim Register (SRSSv2)

Address: 0x0FFF35E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.319 SFLASH\_IMO\_TRIM15

IMO Trim Register (SRSSv2)

Address: 0x0FFF35F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.320 SFLASH\_IMO\_TRIM16

IMO Trim Register (SRSSv2)

Address: 0x0FFF360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.321 SFLASH\_IMO\_TRIM17

IMO Trim Register (SRSSv2)

Address: 0x0FFF361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.322 SFLASH\_IMO\_TRIM18

IMO Trim Register (SRSSv2)

Address: 0x0FFFF362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.323 SFLASH\_IMO\_TRIM19

IMO Trim Register (SRSSv2)

Address: 0x0FFFF363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 22.1.324 SFLASH\_IMO\_TRIM20

IMO Trim Register (SRSSv2)

Address: 0x0FFF364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.325 SFLASH\_IMO\_TRIM21

IMO Trim Register (SRSSv2)

Address: 0x0FFF365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.326 SFLASH\_IMO\_TRIM22

IMO Trim Register (SRSSv2)

Address: 0x0FFF366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.327 SFLASH\_IMO\_TRIM23

IMO Trim Register (SRSSv2)

Address: 0x0FFF367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.328 SFLASH\_IMO\_TRIM24

IMO Trim Register (SRSSv2)

Address: 0x0FFF368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.329 SFLASH\_IMO\_TRIM25

IMO Trim Register (SRSSv2)

Address: 0x0FFF369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.330 SFLASH\_IMO\_TRIM26

IMO Trim Register (SRSSv2)

Address: 0x0FFF36A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.331 SFLASH\_IMO\_TRIM27

IMO Trim Register (SRSSv2)

Address: 0x0FFF36B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 22.1.332 SFLASH\_IMO\_TRIM28

IMO Trim Register (SRSSv2)

Address: 0x0FFF36C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.333 SFLASH\_IMO\_TRIM29

IMO Trim Register (SRSSv2)

Address: 0x0FFF36D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.334 SFLASH\_IMO\_TRIM30

IMO Trim Register (SRSSv2)

Address: 0x0FFF36E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.335 SFLASH\_IMO\_TRIM31

IMO Trim Register (SRSSv2)

Address: 0x0FFF36F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.336 SFLASH\_IMO\_TRIM32

IMO Trim Register (SRSSv2)

Address: 0x0FFF370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.337 SFLASH\_IMO\_TRIM33

IMO Trim Register (SRSSv2)

Address: 0x0FFF371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.338 SFLASH\_IMO\_TRIM34

IMO Trim Register (SRSSv2)

Address: 0x0FFF372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.339 SFLASH\_IMO\_TRIM35

IMO Trim Register (SRSSv2)

Address: 0x0FFFF373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 22.1.340 SFLASH\_IMO\_TRIM36

IMO Trim Register (SRSSv2)

Address: 0x0FFFF374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.341 SFLASH\_IMO\_TRIM37

IMO Trim Register (SRSSv2)

Address: 0x0FFF375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.342 SFLASH\_IMO\_TRIM38

IMO Trim Register (SRSSv2)

Address: 0x0FFF376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.343 SFLASH\_IMO\_TRIM39

IMO Trim Register (SRSSv2)

Address: 0x0FFF377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.344 SFLASH\_IMO\_TRIM40

IMO Trim Register (SRSSv2)

Address: 0x0FFF378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.345 SFLASH\_IMO\_TRIM41

IMO Trim Register (SRSSv2)

Address: 0x0FFF379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.346 SFLASH\_IMO\_TRIM42

IMO Trim Register (SRSSv2)

Address: 0x0FFF37A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.347 SFLASH\_IMO\_TRIM43

IMO Trim Register (SRSSv2)

Address: 0x0FFFF37B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X



## 22.1.348 SFLASH\_IMO\_TRIM44

IMO Trim Register (SRSSv2)

Address: 0x0FFF37C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.349 SFLASH\_IMO\_TRIM45

IMO Trim Register (SRSSv2)

Address: 0x0FFF37D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

## 22.1.350 SFLASH\_CHECKSUM

Boot Checksum

Address: 0x0FFF3FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CHECKSUM [7:0]							

  

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CHECKSUM [15:8]							

Bits	Name	Description
15 : 0	CHECKSUM	Checksum of fixed data checked during boot. This checksum covers all of rows 1,2,3 of macro 0 + row 3 of macro 1 (except this checksum, and row 3 of macro 1 only if it exists). Default Value: X

## 22.1.351 SFLASH\_MACRO\_0\_FREE\_SFLASH0

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.352 SFLASH\_MACRO\_0\_FREE\_SFLASH1

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF401

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.353 SFLASH\_MACRO\_0\_FREE\_SFLASH2

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF402

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.354 SFLASH\_MACRO\_0\_FREE\_SFLASH3

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF403

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.355 SFLASH\_MACRO\_0\_FREE\_SFLASH4

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.356 SFLASH\_MACRO\_0\_FREE\_SFLASH5

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF405

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.357 SFLASH\_MACRO\_0\_FREE\_SFLASH6

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF406

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.358 SFLASH\_MACRO\_0\_FREE\_SFLASH7

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF407

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.359 SFLASH\_MACRO\_0\_FREE\_SFLASH8

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.360 SFLASH\_MACRO\_0\_FREE\_SFLASH9

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF409

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.361 SFLASH\_MACRO\_0\_FREE\_SFLASH10

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF40A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.362 SFLASH\_MACRO\_0\_FREE\_SFLASH11

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF40B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.363 SFLASH\_MACRO\_0\_FREE\_SFLASH12

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.364 SFLASH\_MACRO\_0\_FREE\_SFLASH13

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF40D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.365 SFLASH\_MACRO\_0\_FREE\_SFLASH14

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF40E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.366 SFLASH\_MACRO\_0\_FREE\_SFLASH15

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF40F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.367 SFLASH\_MACRO\_0\_FREE\_SFLASH16

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.368 SFLASH\_MACRO\_0\_FREE\_SFLASH17

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF411

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.369 SFLASH\_MACRO\_0\_FREE\_SFLASH18

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF412

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.370 SFLASH\_MACRO\_0\_FREE\_SFLASH19

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF413

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.371 SFLASH\_MACRO\_0\_FREE\_SFLASH20

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.372 SFLASH\_MACRO\_0\_FREE\_SFLASH21

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF415

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.373 SFLASH\_MACRO\_0\_FREE\_SFLASH22

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF416

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.374 SFLASH\_MACRO\_0\_FREE\_SFLASH23

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF417

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.375 SFLASH\_MACRO\_0\_FREE\_SFLASH24

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.376 SFLASH\_MACRO\_0\_FREE\_SFLASH25

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF419

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.377 SFLASH\_MACRO\_0\_FREE\_SFLASH26

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF41A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.378 SFLASH\_MACRO\_0\_FREE\_SFLASH27

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF41B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.379 SFLASH\_MACRO\_0\_FREE\_SFLASH28

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.380 SFLASH\_MACRO\_0\_FREE\_SFLASH29

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF41D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.381 SFLASH\_MACRO\_0\_FREE\_SFLASH30

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF41E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.382 SFLASH\_MACRO\_0\_FREE\_SFLASH31

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF41F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.383 SFLASH\_MACRO\_0\_FREE\_SFLASH32

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.384 SFLASH\_MACRO\_0\_FREE\_SFLASH33

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF421

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.385 SFLASH\_MACRO\_0\_FREE\_SFLASH34

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF422

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.386 SFLASH\_MACRO\_0\_FREE\_SFLASH35

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF423

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.387 SFLASH\_MACRO\_0\_FREE\_SFLASH36

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.388 SFLASH\_MACRO\_0\_FREE\_SFLASH37

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF425

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.389 SFLASH\_MACRO\_0\_FREE\_SFLASH38

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF426

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.390 SFLASH\_MACRO\_0\_FREE\_SFLASH39

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF427

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.391 SFLASH\_MACRO\_0\_FREE\_SFLASH40

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.392 SFLASH\_MACRO\_0\_FREE\_SFLASH41

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF429

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.393 SFLASH\_MACRO\_0\_FREE\_SFLASH42

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF42A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.394 SFLASH\_MACRO\_0\_FREE\_SFLASH43

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF42B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.395 SFLASH\_MACRO\_0\_FREE\_SFLASH44

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF42C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.396 SFLASH\_MACRO\_0\_FREE\_SFLASH45

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF42D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.397 SFLASH\_MACRO\_0\_FREE\_SFLASH46

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF42E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.398 SFLASH\_MACRO\_0\_FREE\_SFLASH47

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF42F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.399 SFLASH\_MACRO\_0\_FREE\_SFLASH48

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.400 SFLASH\_MACRO\_0\_FREE\_SFLASH49

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF431

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.401 SFLASH\_MACRO\_0\_FREE\_SFLASH50

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF432

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.402 SFLASH\_MACRO\_0\_FREE\_SFLASH51

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF433

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.403 SFLASH\_MACRO\_0\_FREE\_SFLASH52

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.404 SFLASH\_MACRO\_0\_FREE\_SFLASH53

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF435

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.405 SFLASH\_MACRO\_0\_FREE\_SFLASH54

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF436

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.406 SFLASH\_MACRO\_0\_FREE\_SFLASH55

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF437

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.407 SFLASH\_MACRO\_0\_FREE\_SFLASH56

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.408 SFLASH\_MACRO\_0\_FREE\_SFLASH57

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF439

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.409 SFLASH\_MACRO\_0\_FREE\_SFLASH58

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF43A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.410 SFLASH\_MACRO\_0\_FREE\_SFLASH59

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF43B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.411 SFLASH\_MACRO\_0\_FREE\_SFLASH60

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF43C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.412 SFLASH\_MACRO\_0\_FREE\_SFLASH61

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF43D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.413 SFLASH\_MACRO\_0\_FREE\_SFLASH62

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF43E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.414 SFLASH\_MACRO\_0\_FREE\_SFLASH63

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF43F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.415 SFLASH\_MACRO\_0\_FREE\_SFLASH64

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.416 SFLASH\_MACRO\_0\_FREE\_SFLASH65

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF441

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.417 SFLASH\_MACRO\_0\_FREE\_SFLASH66

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF442

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.418 SFLASH\_MACRO\_0\_FREE\_SFLASH67

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF443

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.419 SFLASH\_MACRO\_0\_FREE\_SFLASH68

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.420 SFLASH\_MACRO\_0\_FREE\_SFLASH69

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF445

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.421 SFLASH\_MACRO\_0\_FREE\_SFLASH70

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF446

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.422 SFLASH\_MACRO\_0\_FREE\_SFLASH71

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF447

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.423 SFLASH\_MACRO\_0\_FREE\_SFLASH72

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.424 SFLASH\_MACRO\_0\_FREE\_SFLASH73

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF449

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.425 SFLASH\_MACRO\_0\_FREE\_SFLASH74

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF44A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.426 SFLASH\_MACRO\_0\_FREE\_SFLASH75

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF44B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.427 SFLASH\_MACRO\_0\_FREE\_SFLASH76

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF44C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.428 SFLASH\_MACRO\_0\_FREE\_SFLASH77

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF44D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.429 SFLASH\_MACRO\_0\_FREE\_SFLASH78

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF44E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.430 SFLASH\_MACRO\_0\_FREE\_SFLASH79

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF44F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.431 SFLASH\_MACRO\_0\_FREE\_SFLASH80

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.432 SFLASH\_MACRO\_0\_FREE\_SFLASH81

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF451

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.433 SFLASH\_MACRO\_0\_FREE\_SFLASH82

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF452

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.434 SFLASH\_MACRO\_0\_FREE\_SFLASH83

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF453

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.435 SFLASH\_MACRO\_0\_FREE\_SFLASH84

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.436 SFLASH\_MACRO\_0\_FREE\_SFLASH85

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF455

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.437 SFLASH\_MACRO\_0\_FREE\_SFLASH86

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF456

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.438 SFLASH\_MACRO\_0\_FREE\_SFLASH87

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF457

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.439 SFLASH\_MACRO\_0\_FREE\_SFLASH88

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.440 SFLASH\_MACRO\_0\_FREE\_SFLASH89

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF459

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.441 SFLASH\_MACRO\_0\_FREE\_SFLASH90

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF45A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.442 SFLASH\_MACRO\_0\_FREE\_SFLASH91

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF45B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.443 SFLASH\_MACRO\_0\_FREE\_SFLASH92

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF45C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.444 SFLASH\_MACRO\_0\_FREE\_SFLASH93

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF45D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.445 SFLASH\_MACRO\_0\_FREE\_SFLASH94

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF45E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.446 SFLASH\_MACRO\_0\_FREE\_SFLASH95

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF45F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.447 SFLASH\_MACRO\_0\_FREE\_SFLASH96

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.448 SFLASH\_MACRO\_0\_FREE\_SFLASH97

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF461

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.449 SFLASH\_MACRO\_0\_FREE\_SFLASH98

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF462

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.450 SFLASH\_MACRO\_0\_FREE\_SFLASH99

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF463

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.451 SFLASH\_MACRO\_0\_FREE\_SFLASH100

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.452 SFLASH\_MACRO\_0\_FREE\_SFLASH101

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF465

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.453 SFLASH\_MACRO\_0\_FREE\_SFLASH102

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF466

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.454 SFLASH\_MACRO\_0\_FREE\_SFLASH103

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF467

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.455 SFLASH\_MACRO\_0\_FREE\_SFLASH104

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.456 SFLASH\_MACRO\_0\_FREE\_SFLASH105

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF469

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.457 SFLASH\_MACRO\_0\_FREE\_SFLASH106

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF46A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.458 SFLASH\_MACRO\_0\_FREE\_SFLASH107

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF46B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.459 SFLASH\_MACRO\_0\_FREE\_SFLASH108

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF46C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.460 SFLASH\_MACRO\_0\_FREE\_SFLASH109

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF46D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.461 SFLASH\_MACRO\_0\_FREE\_SFLASH110

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF46E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.462 SFLASH\_MACRO\_0\_FREE\_SFLASH111

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF46F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.463 SFLASH\_MACRO\_0\_FREE\_SFLASH112

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.464 SFLASH\_MACRO\_0\_FREE\_SFLASH113

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF471

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.465 SFLASH\_MACRO\_0\_FREE\_SFLASH114

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF472

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.466 SFLASH\_MACRO\_0\_FREE\_SFLASH115

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF473

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.467 SFLASH\_MACRO\_0\_FREE\_SFLASH116

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.468 SFLASH\_MACRO\_0\_FREE\_SFLASH117

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF475

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.469 SFLASH\_MACRO\_0\_FREE\_SFLASH118

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF476

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.470 SFLASH\_MACRO\_0\_FREE\_SFLASH119

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF477

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.471 SFLASH\_MACRO\_0\_FREE\_SFLASH120

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.472 SFLASH\_MACRO\_0\_FREE\_SFLASH121

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF479

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.473 SFLASH\_MACRO\_0\_FREE\_SFLASH122

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF47A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.474 SFLASH\_MACRO\_0\_FREE\_SFLASH123

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF47B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.475 SFLASH\_MACRO\_0\_FREE\_SFLASH124

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF47C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.476 SFLASH\_MACRO\_0\_FREE\_SFLASH125

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF47D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.477 SFLASH\_MACRO\_0\_FREE\_SFLASH126

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.478 SFLASH\_MACRO\_0\_FREE\_SFLASH127

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.479 SFLASH\_MACRO\_0\_FREE\_SFLASH128

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.480 SFLASH\_MACRO\_0\_FREE\_SFLASH129

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF481

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.481 SFLASH\_MACRO\_0\_FREE\_SFLASH130

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF482

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.482 SFLASH\_MACRO\_0\_FREE\_SFLASH131

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF483

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.483 SFLASH\_MACRO\_0\_FREE\_SFLASH132

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.484 SFLASH\_MACRO\_0\_FREE\_SFLASH133

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF485

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.485 SFLASH\_MACRO\_0\_FREE\_SFLASH134

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF486

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.486 SFLASH\_MACRO\_0\_FREE\_SFLASH135

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF487

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.487 SFLASH\_MACRO\_0\_FREE\_SFLASH136

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.488 SFLASH\_MACRO\_0\_FREE\_SFLASH137

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF489

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.489 SFLASH\_MACRO\_0\_FREE\_SFLASH138

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF48A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.490 SFLASH\_MACRO\_0\_FREE\_SFLASH139

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF48B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.491 SFLASH\_MACRO\_0\_FREE\_SFLASH140

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF48C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.492 SFLASH\_MACRO\_0\_FREE\_SFLASH141

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF48D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.493 SFLASH\_MACRO\_0\_FREE\_SFLASH142

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF48E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.494 SFLASH\_MACRO\_0\_FREE\_SFLASH143

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF48F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.495 SFLASH\_MACRO\_0\_FREE\_SFLASH144

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.496 SFLASH\_MACRO\_0\_FREE\_SFLASH145

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF491

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.497 SFLASH\_MACRO\_0\_FREE\_SFLASH146

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF492

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.498 SFLASH\_MACRO\_0\_FREE\_SFLASH147

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF493

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.499 SFLASH\_MACRO\_0\_FREE\_SFLASH148

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF494

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.500 SFLASH\_MACRO\_0\_FREE\_SFLASH149

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF495

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.501 SFLASH\_MACRO\_0\_FREE\_SFLASH150

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF496

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.502 SFLASH\_MACRO\_0\_FREE\_SFLASH151

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF497

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.503 SFLASH\_MACRO\_0\_FREE\_SFLASH152

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.504 SFLASH\_MACRO\_0\_FREE\_SFLASH153

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF499

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.505 SFLASH\_MACRO\_0\_FREE\_SFLASH154

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF49A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.506 SFLASH\_MACRO\_0\_FREE\_SFLASH155

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF49B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.507 SFLASH\_MACRO\_0\_FREE\_SFLASH156

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF49C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.508 SFLASH\_MACRO\_0\_FREE\_SFLASH157

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF49D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.509 SFLASH\_MACRO\_0\_FREE\_SFLASH158

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF49E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.510 SFLASH\_MACRO\_0\_FREE\_SFLASH159

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF49F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.511 SFLASH\_MACRO\_0\_FREE\_SFLASH160

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.512 SFLASH\_MACRO\_0\_FREE\_SFLASH161

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.513 SFLASH\_MACRO\_0\_FREE\_SFLASH162

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.514 SFLASH\_MACRO\_0\_FREE\_SFLASH163

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.515 SFLASH\_MACRO\_0\_FREE\_SFLASH164

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.516 SFLASH\_MACRO\_0\_FREE\_SFLASH165

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.517 SFLASH\_MACRO\_0\_FREE\_SFLASH166

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.518 SFLASH\_MACRO\_0\_FREE\_SFLASH167

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.519 SFLASH\_MACRO\_0\_FREE\_SFLASH168

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.520 SFLASH\_MACRO\_0\_FREE\_SFLASH169

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.521 SFLASH\_MACRO\_0\_FREE\_SFLASH170

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.522 SFLASH\_MACRO\_0\_FREE\_SFLASH171

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.523 SFLASH\_MACRO\_0\_FREE\_SFLASH172

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.524 SFLASH\_MACRO\_0\_FREE\_SFLASH173

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.525 SFLASH\_MACRO\_0\_FREE\_SFLASH174

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.526 SFLASH\_MACRO\_0\_FREE\_SFLASH175

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.527 SFLASH\_MACRO\_0\_FREE\_SFLASH176

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.528 SFLASH\_MACRO\_0\_FREE\_SFLASH177

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.529 SFLASH\_MACRO\_0\_FREE\_SFLASH178

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.530 SFLASH\_MACRO\_0\_FREE\_SFLASH179

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.531 SFLASH\_MACRO\_0\_FREE\_SFLASH180

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.532 SFLASH\_MACRO\_0\_FREE\_SFLASH181

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.533 SFLASH\_MACRO\_0\_FREE\_SFLASH182

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.534 SFLASH\_MACRO\_0\_FREE\_SFLASH183

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.535 SFLASH\_MACRO\_0\_FREE\_SFLASH184

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.536 SFLASH\_MACRO\_0\_FREE\_SFLASH185

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.537 SFLASH\_MACRO\_0\_FREE\_SFLASH186

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.538 SFLASH\_MACRO\_0\_FREE\_SFLASH187

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.539 SFLASH\_MACRO\_0\_FREE\_SFLASH188

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.540 SFLASH\_MACRO\_0\_FREE\_SFLASH189

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.541 SFLASH\_MACRO\_0\_FREE\_SFLASH190

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.542 SFLASH\_MACRO\_0\_FREE\_SFLASH191

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.543 SFLASH\_MACRO\_0\_FREE\_SFLASH192

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.544 SFLASH\_MACRO\_0\_FREE\_SFLASH193

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.545 SFLASH\_MACRO\_0\_FREE\_SFLASH194

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.546 SFLASH\_MACRO\_0\_FREE\_SFLASH195

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.547 SFLASH\_MACRO\_0\_FREE\_SFLASH196

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.548 SFLASH\_MACRO\_0\_FREE\_SFLASH197

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.549 SFLASH\_MACRO\_0\_FREE\_SFLASH198

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.550 SFLASH\_MACRO\_0\_FREE\_SFLASH199

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.551 SFLASH\_MACRO\_0\_FREE\_SFLASH200

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.552 SFLASH\_MACRO\_0\_FREE\_SFLASH201

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.553 SFLASH\_MACRO\_0\_FREE\_SFLASH202

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.554 SFLASH\_MACRO\_0\_FREE\_SFLASH203

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.555 SFLASH\_MACRO\_0\_FREE\_SFLASH204

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.556 SFLASH\_MACRO\_0\_FREE\_SFLASH205

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.557 SFLASH\_MACRO\_0\_FREE\_SFLASH206

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.558 SFLASH\_MACRO\_0\_FREE\_SFLASH207

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.559 SFLASH\_MACRO\_0\_FREE\_SFLASH208

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.560 SFLASH\_MACRO\_0\_FREE\_SFLASH209

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.561 SFLASH\_MACRO\_0\_FREE\_SFLASH210

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.562 SFLASH\_MACRO\_0\_FREE\_SFLASH211

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.563 SFLASH\_MACRO\_0\_FREE\_SFLASH212

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.564 SFLASH\_MACRO\_0\_FREE\_SFLASH213

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.565 SFLASH\_MACRO\_0\_FREE\_SFLASH214

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.566 SFLASH\_MACRO\_0\_FREE\_SFLASH215

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.567 SFLASH\_MACRO\_0\_FREE\_SFLASH216

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.568 SFLASH\_MACRO\_0\_FREE\_SFLASH217

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.569 SFLASH\_MACRO\_0\_FREE\_SFLASH218

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.570 SFLASH\_MACRO\_0\_FREE\_SFLASH219

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.571 SFLASH\_MACRO\_0\_FREE\_SFLASH220

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.572 SFLASH\_MACRO\_0\_FREE\_SFLASH221

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.573 SFLASH\_MACRO\_0\_FREE\_SFLASH222

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.574 SFLASH\_MACRO\_0\_FREE\_SFLASH223

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.575 SFLASH\_MACRO\_0\_FREE\_SFLASH224

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.576 SFLASH\_MACRO\_0\_FREE\_SFLASH225

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.577 SFLASH\_MACRO\_0\_FREE\_SFLASH226

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.578 SFLASH\_MACRO\_0\_FREE\_SFLASH227

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.579 SFLASH\_MACRO\_0\_FREE\_SFLASH228

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.580 SFLASH\_MACRO\_0\_FREE\_SFLASH229

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.581 SFLASH\_MACRO\_0\_FREE\_SFLASH230

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.582 SFLASH\_MACRO\_0\_FREE\_SFLASH231

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.583 SFLASH\_MACRO\_0\_FREE\_SFLASH232

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.584 SFLASH\_MACRO\_0\_FREE\_SFLASH233

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.585 SFLASH\_MACRO\_0\_FREE\_SFLASH234

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.586 SFLASH\_MACRO\_0\_FREE\_SFLASH235

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.587 SFLASH\_MACRO\_0\_FREE\_SFLASH236

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.588 SFLASH\_MACRO\_0\_FREE\_SFLASH237

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.589 SFLASH\_MACRO\_0\_FREE\_SFLASH238

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.590 SFLASH\_MACRO\_0\_FREE\_SFLASH239

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.591 SFLASH\_MACRO\_0\_FREE\_SFLASH240

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.592 SFLASH\_MACRO\_0\_FREE\_SFLASH241

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.593 SFLASH\_MACRO\_0\_FREE\_SFLASH242

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.594 SFLASH\_MACRO\_0\_FREE\_SFLASH243

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.595 SFLASH\_MACRO\_0\_FREE\_SFLASH244

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.596 SFLASH\_MACRO\_0\_FREE\_SFLASH245

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.597 SFLASH\_MACRO\_0\_FREE\_SFLASH246

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.598 SFLASH\_MACRO\_0\_FREE\_SFLASH247

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.599 SFLASH\_MACRO\_0\_FREE\_SFLASH248

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.600 SFLASH\_MACRO\_0\_FREE\_SFLASH249

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.601 SFLASH\_MACRO\_0\_FREE\_SFLASH250

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.602 SFLASH\_MACRO\_0\_FREE\_SFLASH251

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.603 SFLASH\_MACRO\_0\_FREE\_SFLASH252

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.604 SFLASH\_MACRO\_0\_FREE\_SFLASH253

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.605 SFLASH\_MACRO\_0\_FREE\_SFLASH254

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF4FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.606 SFLASH\_MACRO\_0\_FREE\_SFLASH255

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.607 SFLASH\_MACRO\_0\_FREE\_SFLASH256

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.608 SFLASH\_MACRO\_0\_FREE\_SFLASH257

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF501

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.609 SFLASH\_MACRO\_0\_FREE\_SFLASH258

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF502

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.610 SFLASH\_MACRO\_0\_FREE\_SFLASH259

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF503

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.611 SFLASH\_MACRO\_0\_FREE\_SFLASH260

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF504

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.612 SFLASH\_MACRO\_0\_FREE\_SFLASH261

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF505

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.613 SFLASH\_MACRO\_0\_FREE\_SFLASH262

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF506

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.614 SFLASH\_MACRO\_0\_FREE\_SFLASH263

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF507

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.615 SFLASH\_MACRO\_0\_FREE\_SFLASH264

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF508

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.616 SFLASH\_MACRO\_0\_FREE\_SFLASH265

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF509

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.617 SFLASH\_MACRO\_0\_FREE\_SFLASH266

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF50A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.618 SFLASH\_MACRO\_0\_FREE\_SFLASH267

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF50B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.619 SFLASH\_MACRO\_0\_FREE\_SFLASH268

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF50C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.620 SFLASH\_MACRO\_0\_FREE\_SFLASH269

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF50D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.621 SFLASH\_MACRO\_0\_FREE\_SFLASH270

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF50E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.622 SFLASH\_MACRO\_0\_FREE\_SFLASH271

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF50F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.623 SFLASH\_MACRO\_0\_FREE\_SFLASH272

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.624 SFLASH\_MACRO\_0\_FREE\_SFLASH273

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF511

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.625 SFLASH\_MACRO\_0\_FREE\_SFLASH274

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF512

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.626 SFLASH\_MACRO\_0\_FREE\_SFLASH275

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF513

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.627 SFLASH\_MACRO\_0\_FREE\_SFLASH276

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF514

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.628 SFLASH\_MACRO\_0\_FREE\_SFLASH277

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF515

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.629 SFLASH\_MACRO\_0\_FREE\_SFLASH278

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF516

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.630 SFLASH\_MACRO\_0\_FREE\_SFLASH279

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF517

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.631 SFLASH\_MACRO\_0\_FREE\_SFLASH280

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.632 SFLASH\_MACRO\_0\_FREE\_SFLASH281

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF519

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.633 SFLASH\_MACRO\_0\_FREE\_SFLASH282

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF51A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.634 SFLASH\_MACRO\_0\_FREE\_SFLASH283

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF51B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.635 SFLASH\_MACRO\_0\_FREE\_SFLASH284

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF51C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.636 SFLASH\_MACRO\_0\_FREE\_SFLASH285

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF51D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.637 SFLASH\_MACRO\_0\_FREE\_SFLASH286

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF51E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.638 SFLASH\_MACRO\_0\_FREE\_SFLASH287

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF51F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.639 SFLASH\_MACRO\_0\_FREE\_SFLASH288

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.640 SFLASH\_MACRO\_0\_FREE\_SFLASH289

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF521

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.641 SFLASH\_MACRO\_0\_FREE\_SFLASH290

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF522

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.642 SFLASH\_MACRO\_0\_FREE\_SFLASH291

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF523

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.643 SFLASH\_MACRO\_0\_FREE\_SFLASH292

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF524

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.644 SFLASH\_MACRO\_0\_FREE\_SFLASH293

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF525

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.645 SFLASH\_MACRO\_0\_FREE\_SFLASH294

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF526

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.646 SFLASH\_MACRO\_0\_FREE\_SFLASH295

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF527

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.647 SFLASH\_MACRO\_0\_FREE\_SFLASH296

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF528

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.648 SFLASH\_MACRO\_0\_FREE\_SFLASH297

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF529

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.649 SFLASH\_MACRO\_0\_FREE\_SFLASH298

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF52A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.650 SFLASH\_MACRO\_0\_FREE\_SFLASH299

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF52B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.651 SFLASH\_MACRO\_0\_FREE\_SFLASH300

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF52C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.652 SFLASH\_MACRO\_0\_FREE\_SFLASH301

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF52D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.653 SFLASH\_MACRO\_0\_FREE\_SFLASH302

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF52E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.654 SFLASH\_MACRO\_0\_FREE\_SFLASH303

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF52F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.655 SFLASH\_MACRO\_0\_FREE\_SFLASH304

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.656 SFLASH\_MACRO\_0\_FREE\_SFLASH305

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF531

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.657 SFLASH\_MACRO\_0\_FREE\_SFLASH306

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF532

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.658 SFLASH\_MACRO\_0\_FREE\_SFLASH307

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF533

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.659 SFLASH\_MACRO\_0\_FREE\_SFLASH308

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF534

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.660 SFLASH\_MACRO\_0\_FREE\_SFLASH309

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF535

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.661 SFLASH\_MACRO\_0\_FREE\_SFLASH310

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF536

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.662 SFLASH\_MACRO\_0\_FREE\_SFLASH311

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF537

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.663 SFLASH\_MACRO\_0\_FREE\_SFLASH312

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF538

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.664 SFLASH\_MACRO\_0\_FREE\_SFLASH313

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF539

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.665 SFLASH\_MACRO\_0\_FREE\_SFLASH314

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF53A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.666 SFLASH\_MACRO\_0\_FREE\_SFLASH315

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF53B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.667 SFLASH\_MACRO\_0\_FREE\_SFLASH316

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF53C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.668 SFLASH\_MACRO\_0\_FREE\_SFLASH317

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF53D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.669 SFLASH\_MACRO\_0\_FREE\_SFLASH318

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF53E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.670 SFLASH\_MACRO\_0\_FREE\_SFLASH319

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF53F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.671 SFLASH\_MACRO\_0\_FREE\_SFLASH320

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.672 SFLASH\_MACRO\_0\_FREE\_SFLASH321

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF541

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.673 SFLASH\_MACRO\_0\_FREE\_SFLASH322

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF542

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.674 SFLASH\_MACRO\_0\_FREE\_SFLASH323

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF543

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.675 SFLASH\_MACRO\_0\_FREE\_SFLASH324

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.676 SFLASH\_MACRO\_0\_FREE\_SFLASH325

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF545

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.677 SFLASH\_MACRO\_0\_FREE\_SFLASH326

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF546

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.678 SFLASH\_MACRO\_0\_FREE\_SFLASH327

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF547

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.679 SFLASH\_MACRO\_0\_FREE\_SFLASH328

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.680 SFLASH\_MACRO\_0\_FREE\_SFLASH329

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF549

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.681 SFLASH\_MACRO\_0\_FREE\_SFLASH330

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF54A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.682 SFLASH\_MACRO\_0\_FREE\_SFLASH331

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF54B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.683 SFLASH\_MACRO\_0\_FREE\_SFLASH332

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF54C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.684 SFLASH\_MACRO\_0\_FREE\_SFLASH333

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF54D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.685 SFLASH\_MACRO\_0\_FREE\_SFLASH334

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF54E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.686 SFLASH\_MACRO\_0\_FREE\_SFLASH335

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF54F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.687 SFLASH\_MACRO\_0\_FREE\_SFLASH336

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF550

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.688 SFLASH\_MACRO\_0\_FREE\_SFLASH337

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF551

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.689 SFLASH\_MACRO\_0\_FREE\_SFLASH338

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF552

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.690 SFLASH\_MACRO\_0\_FREE\_SFLASH339

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF553

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.691 SFLASH\_MACRO\_0\_FREE\_SFLASH340

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF554

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.692 SFLASH\_MACRO\_0\_FREE\_SFLASH341

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF555

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.693 SFLASH\_MACRO\_0\_FREE\_SFLASH342

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF556

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.694 SFLASH\_MACRO\_0\_FREE\_SFLASH343

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF557

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.695 SFLASH\_MACRO\_0\_FREE\_SFLASH344

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF558

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.696 SFLASH\_MACRO\_0\_FREE\_SFLASH345

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF559

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.697 SFLASH\_MACRO\_0\_FREE\_SFLASH346

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF55A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.698 SFLASH\_MACRO\_0\_FREE\_SFLASH347

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF55B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.699 SFLASH\_MACRO\_0\_FREE\_SFLASH348

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF55C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.700 SFLASH\_MACRO\_0\_FREE\_SFLASH349

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF55D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.701 SFLASH\_MACRO\_0\_FREE\_SFLASH350

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF55E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.702 SFLASH\_MACRO\_0\_FREE\_SFLASH351

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF55F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.703 SFLASH\_MACRO\_0\_FREE\_SFLASH352

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF560

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.704 SFLASH\_MACRO\_0\_FREE\_SFLASH353

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF561

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.705 SFLASH\_MACRO\_0\_FREE\_SFLASH354

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF562

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.706 SFLASH\_MACRO\_0\_FREE\_SFLASH355

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF563

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.707 SFLASH\_MACRO\_0\_FREE\_SFLASH356

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF564

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.708 SFLASH\_MACRO\_0\_FREE\_SFLASH357

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF565

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.709 SFLASH\_MACRO\_0\_FREE\_SFLASH358

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF566

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.710 SFLASH\_MACRO\_0\_FREE\_SFLASH359

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF567

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.711 SFLASH\_MACRO\_0\_FREE\_SFLASH360

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF568

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.712 SFLASH\_MACRO\_0\_FREE\_SFLASH361

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF569

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.713 SFLASH\_MACRO\_0\_FREE\_SFLASH362

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF56A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.714 SFLASH\_MACRO\_0\_FREE\_SFLASH363

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF56B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.715 SFLASH\_MACRO\_0\_FREE\_SFLASH364

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF56C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.716 SFLASH\_MACRO\_0\_FREE\_SFLASH365

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF56D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.717 SFLASH\_MACRO\_0\_FREE\_SFLASH366

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF56E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.718 SFLASH\_MACRO\_0\_FREE\_SFLASH367

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF56F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.719 SFLASH\_MACRO\_0\_FREE\_SFLASH368

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF570

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.720 SFLASH\_MACRO\_0\_FREE\_SFLASH369

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF571

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.721 SFLASH\_MACRO\_0\_FREE\_SFLASH370

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF572

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.722 SFLASH\_MACRO\_0\_FREE\_SFLASH371

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF573

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.723 SFLASH\_MACRO\_0\_FREE\_SFLASH372

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF574

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.724 SFLASH\_MACRO\_0\_FREE\_SFLASH373

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF575

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.725 SFLASH\_MACRO\_0\_FREE\_SFLASH374

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF576

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.726 SFLASH\_MACRO\_0\_FREE\_SFLASH375

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF577

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.727 SFLASH\_MACRO\_0\_FREE\_SFLASH376

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF578

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.728 SFLASH\_MACRO\_0\_FREE\_SFLASH377

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF579

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.729 SFLASH\_MACRO\_0\_FREE\_SFLASH378

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF57A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.730 SFLASH\_MACRO\_0\_FREE\_SFLASH379

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF57B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.731 SFLASH\_MACRO\_0\_FREE\_SFLASH380

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF57C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.732 SFLASH\_MACRO\_0\_FREE\_SFLASH381

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF57D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.733 SFLASH\_MACRO\_0\_FREE\_SFLASH382

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF57E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.734 SFLASH\_MACRO\_0\_FREE\_SFLASH383

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF57F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.735 SFLASH\_MACRO\_0\_FREE\_SFLASH384

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.736 SFLASH\_MACRO\_0\_FREE\_SFLASH385

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF581

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.737 SFLASH\_MACRO\_0\_FREE\_SFLASH386

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF582

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.738 SFLASH\_MACRO\_0\_FREE\_SFLASH387

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF583

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.739 SFLASH\_MACRO\_0\_FREE\_SFLASH388

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF584

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.740 SFLASH\_MACRO\_0\_FREE\_SFLASH389

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF585

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.741 SFLASH\_MACRO\_0\_FREE\_SFLASH390

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF586

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.742 SFLASH\_MACRO\_0\_FREE\_SFLASH391

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF587

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.743 SFLASH\_MACRO\_0\_FREE\_SFLASH392

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF588

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.744 SFLASH\_MACRO\_0\_FREE\_SFLASH393

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF589

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.745 SFLASH\_MACRO\_0\_FREE\_SFLASH394

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF58A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.746 SFLASH\_MACRO\_0\_FREE\_SFLASH395

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF58B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.747 SFLASH\_MACRO\_0\_FREE\_SFLASH396

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF58C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.748 SFLASH\_MACRO\_0\_FREE\_SFLASH397

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF58D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.749 SFLASH\_MACRO\_0\_FREE\_SFLASH398

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF58E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.750 SFLASH\_MACRO\_0\_FREE\_SFLASH399

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF58F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.751 SFLASH\_MACRO\_0\_FREE\_SFLASH400

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF590

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.752 SFLASH\_MACRO\_0\_FREE\_SFLASH401

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF591

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.753 SFLASH\_MACRO\_0\_FREE\_SFLASH402

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF592

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.754 SFLASH\_MACRO\_0\_FREE\_SFLASH403

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF593

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.755 SFLASH\_MACRO\_0\_FREE\_SFLASH404

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF594

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.756 SFLASH\_MACRO\_0\_FREE\_SFLASH405

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF595

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.757 SFLASH\_MACRO\_0\_FREE\_SFLASH406

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF596

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.758 SFLASH\_MACRO\_0\_FREE\_SFLASH407

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF597

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.759 SFLASH\_MACRO\_0\_FREE\_SFLASH408

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF598

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.760 SFLASH\_MACRO\_0\_FREE\_SFLASH409

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF599

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.761 SFLASH\_MACRO\_0\_FREE\_SFLASH410

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF59A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.762 SFLASH\_MACRO\_0\_FREE\_SFLASH411

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF59B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.763 SFLASH\_MACRO\_0\_FREE\_SFLASH412

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF59C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.764 SFLASH\_MACRO\_0\_FREE\_SFLASH413

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF59D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.765 SFLASH\_MACRO\_0\_FREE\_SFLASH414

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF59E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.766 SFLASH\_MACRO\_0\_FREE\_SFLASH415

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF59F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.767 SFLASH\_MACRO\_0\_FREE\_SFLASH416

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.768 SFLASH\_MACRO\_0\_FREE\_SFLASH417

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.769 SFLASH\_MACRO\_0\_FREE\_SFLASH418

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.770 SFLASH\_MACRO\_0\_FREE\_SFLASH419

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.771 SFLASH\_MACRO\_0\_FREE\_SFLASH420

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.772 SFLASH\_MACRO\_0\_FREE\_SFLASH421

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.773 SFLASH\_MACRO\_0\_FREE\_SFLASH422

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.774 SFLASH\_MACRO\_0\_FREE\_SFLASH423

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.775 SFLASH\_MACRO\_0\_FREE\_SFLASH424

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.776 SFLASH\_MACRO\_0\_FREE\_SFLASH425

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.777 SFLASH\_MACRO\_0\_FREE\_SFLASH426

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.778 SFLASH\_MACRO\_0\_FREE\_SFLASH427

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.779 SFLASH\_MACRO\_0\_FREE\_SFLASH428

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.780 SFLASH\_MACRO\_0\_FREE\_SFLASH429

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.781 SFLASH\_MACRO\_0\_FREE\_SFLASH430

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.782 SFLASH\_MACRO\_0\_FREE\_SFLASH431

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.783 SFLASH\_MACRO\_0\_FREE\_SFLASH432

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.784 SFLASH\_MACRO\_0\_FREE\_SFLASH433

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.785 SFLASH\_MACRO\_0\_FREE\_SFLASH434

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.786 SFLASH\_MACRO\_0\_FREE\_SFLASH435

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.787 SFLASH\_MACRO\_0\_FREE\_SFLASH436

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.788 SFLASH\_MACRO\_0\_FREE\_SFLASH437

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.789 SFLASH\_MACRO\_0\_FREE\_SFLASH438

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.790 SFLASH\_MACRO\_0\_FREE\_SFLASH439

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.791 SFLASH\_MACRO\_0\_FREE\_SFLASH440

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.792 SFLASH\_MACRO\_0\_FREE\_SFLASH441

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.793 SFLASH\_MACRO\_0\_FREE\_SFLASH442

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.794 SFLASH\_MACRO\_0\_FREE\_SFLASH443

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.795 SFLASH\_MACRO\_0\_FREE\_SFLASH444

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.796 SFLASH\_MACRO\_0\_FREE\_SFLASH445

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.797 SFLASH\_MACRO\_0\_FREE\_SFLASH446

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.798 SFLASH\_MACRO\_0\_FREE\_SFLASH447

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.799 SFLASH\_MACRO\_0\_FREE\_SFLASH448

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.800 SFLASH\_MACRO\_0\_FREE\_SFLASH449

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.801 SFLASH\_MACRO\_0\_FREE\_SFLASH450

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.802 SFLASH\_MACRO\_0\_FREE\_SFLASH451

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.803 SFLASH\_MACRO\_0\_FREE\_SFLASH452

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.804 SFLASH\_MACRO\_0\_FREE\_SFLASH453

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.805 SFLASH\_MACRO\_0\_FREE\_SFLASH454

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.806 SFLASH\_MACRO\_0\_FREE\_SFLASH455

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.807 SFLASH\_MACRO\_0\_FREE\_SFLASH456

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.808 SFLASH\_MACRO\_0\_FREE\_SFLASH457

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.809 SFLASH\_MACRO\_0\_FREE\_SFLASH458

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.810 SFLASH\_MACRO\_0\_FREE\_SFLASH459

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.811 SFLASH\_MACRO\_0\_FREE\_SFLASH460

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.812 SFLASH\_MACRO\_0\_FREE\_SFLASH461

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.813 SFLASH\_MACRO\_0\_FREE\_SFLASH462

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.814 SFLASH\_MACRO\_0\_FREE\_SFLASH463

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.815 SFLASH\_MACRO\_0\_FREE\_SFLASH464

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.816 SFLASH\_MACRO\_0\_FREE\_SFLASH465

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.817 SFLASH\_MACRO\_0\_FREE\_SFLASH466

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.818 SFLASH\_MACRO\_0\_FREE\_SFLASH467

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.819 SFLASH\_MACRO\_0\_FREE\_SFLASH468

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.820 SFLASH\_MACRO\_0\_FREE\_SFLASH469

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.821 SFLASH\_MACRO\_0\_FREE\_SFLASH470

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.822 SFLASH\_MACRO\_0\_FREE\_SFLASH471

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.823 SFLASH\_MACRO\_0\_FREE\_SFLASH472

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.824 SFLASH\_MACRO\_0\_FREE\_SFLASH473

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.825 SFLASH\_MACRO\_0\_FREE\_SFLASH474

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.826 SFLASH\_MACRO\_0\_FREE\_SFLASH475

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.827 SFLASH\_MACRO\_0\_FREE\_SFLASH476

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.828 SFLASH\_MACRO\_0\_FREE\_SFLASH477

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.829 SFLASH\_MACRO\_0\_FREE\_SFLASH478

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.830 SFLASH\_MACRO\_0\_FREE\_SFLASH479

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.831 SFLASH\_MACRO\_0\_FREE\_SFLASH480

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.832 SFLASH\_MACRO\_0\_FREE\_SFLASH481

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.833 SFLASH\_MACRO\_0\_FREE\_SFLASH482

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.834 SFLASH\_MACRO\_0\_FREE\_SFLASH483

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.835 SFLASH\_MACRO\_0\_FREE\_SFLASH484

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.836 SFLASH\_MACRO\_0\_FREE\_SFLASH485

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.837 SFLASH\_MACRO\_0\_FREE\_SFLASH486

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.838 SFLASH\_MACRO\_0\_FREE\_SFLASH487

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.839 SFLASH\_MACRO\_0\_FREE\_SFLASH488

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.840 SFLASH\_MACRO\_0\_FREE\_SFLASH489

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.841 SFLASH\_MACRO\_0\_FREE\_SFLASH490

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.842 SFLASH\_MACRO\_0\_FREE\_SFLASH491

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.843 SFLASH\_MACRO\_0\_FREE\_SFLASH492

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.844 SFLASH\_MACRO\_0\_FREE\_SFLASH493

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.845 SFLASH\_MACRO\_0\_FREE\_SFLASH494

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.846 SFLASH\_MACRO\_0\_FREE\_SFLASH495

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.847 SFLASH\_MACRO\_0\_FREE\_SFLASH496

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.848 SFLASH\_MACRO\_0\_FREE\_SFLASH497

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.849 SFLASH\_MACRO\_0\_FREE\_SFLASH498

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.850 SFLASH\_MACRO\_0\_FREE\_SFLASH499

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.851 SFLASH\_MACRO\_0\_FREE\_SFLASH500

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.852 SFLASH\_MACRO\_0\_FREE\_SFLASH501

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.853 SFLASH\_MACRO\_0\_FREE\_SFLASH502

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.854 SFLASH\_MACRO\_0\_FREE\_SFLASH503

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.855 SFLASH\_MACRO\_0\_FREE\_SFLASH504

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.856 SFLASH\_MACRO\_0\_FREE\_SFLASH505

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.857 SFLASH\_MACRO\_0\_FREE\_SFLASH506

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.858 SFLASH\_MACRO\_0\_FREE\_SFLASH507

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.859 SFLASH\_MACRO\_0\_FREE\_SFLASH508

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.860 SFLASH\_MACRO\_0\_FREE\_SFLASH509

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.861 SFLASH\_MACRO\_0\_FREE\_SFLASH510

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.862 SFLASH\_MACRO\_0\_FREE\_SFLASH511

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF5FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.863 SFLASH\_MACRO\_0\_FREE\_SFLASH512

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.864 SFLASH\_MACRO\_0\_FREE\_SFLASH513

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF601

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.865 SFLASH\_MACRO\_0\_FREE\_SFLASH514

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF602

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.866 SFLASH\_MACRO\_0\_FREE\_SFLASH515

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF603

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.867 SFLASH\_MACRO\_0\_FREE\_SFLASH516

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF604

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.868 SFLASH\_MACRO\_0\_FREE\_SFLASH517

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF605

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.869 SFLASH\_MACRO\_0\_FREE\_SFLASH518

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF606

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.870 SFLASH\_MACRO\_0\_FREE\_SFLASH519

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF607

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.871 SFLASH\_MACRO\_0\_FREE\_SFLASH520

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.872 SFLASH\_MACRO\_0\_FREE\_SFLASH521

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF609

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.873 SFLASH\_MACRO\_0\_FREE\_SFLASH522

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF60A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.874 SFLASH\_MACRO\_0\_FREE\_SFLASH523

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF60B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.875 SFLASH\_MACRO\_0\_FREE\_SFLASH524

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF60C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.876 SFLASH\_MACRO\_0\_FREE\_SFLASH525

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF60D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.877 SFLASH\_MACRO\_0\_FREE\_SFLASH526

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF60E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.878 SFLASH\_MACRO\_0\_FREE\_SFLASH527

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF60F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.879 SFLASH\_MACRO\_0\_FREE\_SFLASH528

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.880 SFLASH\_MACRO\_0\_FREE\_SFLASH529

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF611

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.881 SFLASH\_MACRO\_0\_FREE\_SFLASH530

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF612

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.882 SFLASH\_MACRO\_0\_FREE\_SFLASH531

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF613

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.883 SFLASH\_MACRO\_0\_FREE\_SFLASH532

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF614

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.884 SFLASH\_MACRO\_0\_FREE\_SFLASH533

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF615

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.885 SFLASH\_MACRO\_0\_FREE\_SFLASH534

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF616

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.886 SFLASH\_MACRO\_0\_FREE\_SFLASH535

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF617

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.887 SFLASH\_MACRO\_0\_FREE\_SFLASH536

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.888 SFLASH\_MACRO\_0\_FREE\_SFLASH537

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF619

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.889 SFLASH\_MACRO\_0\_FREE\_SFLASH538

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF61A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.890 SFLASH\_MACRO\_0\_FREE\_SFLASH539

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF61B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.891 SFLASH\_MACRO\_0\_FREE\_SFLASH540

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF61C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.892 SFLASH\_MACRO\_0\_FREE\_SFLASH541

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF61D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.893 SFLASH\_MACRO\_0\_FREE\_SFLASH542

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.894 SFLASH\_MACRO\_0\_FREE\_SFLASH543

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.895 SFLASH\_MACRO\_0\_FREE\_SFLASH544

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.896 SFLASH\_MACRO\_0\_FREE\_SFLASH545

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF621

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.897 SFLASH\_MACRO\_0\_FREE\_SFLASH546

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF622

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.898 SFLASH\_MACRO\_0\_FREE\_SFLASH547

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF623

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.899 SFLASH\_MACRO\_0\_FREE\_SFLASH548

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF624

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.900 SFLASH\_MACRO\_0\_FREE\_SFLASH549

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF625

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.901 SFLASH\_MACRO\_0\_FREE\_SFLASH550

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF626

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.902 SFLASH\_MACRO\_0\_FREE\_SFLASH551

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF627

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.903 SFLASH\_MACRO\_0\_FREE\_SFLASH552

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF628

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.904 SFLASH\_MACRO\_0\_FREE\_SFLASH553

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF629

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.905 SFLASH\_MACRO\_0\_FREE\_SFLASH554

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF62A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.906 SFLASH\_MACRO\_0\_FREE\_SFLASH555

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF62B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.907 SFLASH\_MACRO\_0\_FREE\_SFLASH556

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF62C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.908 SFLASH\_MACRO\_0\_FREE\_SFLASH557

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF62D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.909 SFLASH\_MACRO\_0\_FREE\_SFLASH558

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF62E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.910 SFLASH\_MACRO\_0\_FREE\_SFLASH559

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF62F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.911 SFLASH\_MACRO\_0\_FREE\_SFLASH560

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF630

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.912 SFLASH\_MACRO\_0\_FREE\_SFLASH561

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF631

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.913 SFLASH\_MACRO\_0\_FREE\_SFLASH562

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF632

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.914 SFLASH\_MACRO\_0\_FREE\_SFLASH563

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF633

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.915 SFLASH\_MACRO\_0\_FREE\_SFLASH564

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF634

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.916 SFLASH\_MACRO\_0\_FREE\_SFLASH565

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF635

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.917 SFLASH\_MACRO\_0\_FREE\_SFLASH566

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF636

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.918 SFLASH\_MACRO\_0\_FREE\_SFLASH567

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF637

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.919 SFLASH\_MACRO\_0\_FREE\_SFLASH568

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF638

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.920 SFLASH\_MACRO\_0\_FREE\_SFLASH569

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF639

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.921 SFLASH\_MACRO\_0\_FREE\_SFLASH570

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF63A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.922 SFLASH\_MACRO\_0\_FREE\_SFLASH571

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF63B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.923 SFLASH\_MACRO\_0\_FREE\_SFLASH572

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF63C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.924 SFLASH\_MACRO\_0\_FREE\_SFLASH573

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF63D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.925 SFLASH\_MACRO\_0\_FREE\_SFLASH574

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF63E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.926 SFLASH\_MACRO\_0\_FREE\_SFLASH575

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF63F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.927 SFLASH\_MACRO\_0\_FREE\_SFLASH576

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.928 SFLASH\_MACRO\_0\_FREE\_SFLASH577

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF641

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.929 SFLASH\_MACRO\_0\_FREE\_SFLASH578

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF642

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.930 SFLASH\_MACRO\_0\_FREE\_SFLASH579

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF643

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.931 SFLASH\_MACRO\_0\_FREE\_SFLASH580

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.932 SFLASH\_MACRO\_0\_FREE\_SFLASH581

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF645

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.933 SFLASH\_MACRO\_0\_FREE\_SFLASH582

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF646

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.934 SFLASH\_MACRO\_0\_FREE\_SFLASH583

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF647

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.935 SFLASH\_MACRO\_0\_FREE\_SFLASH584

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.936 SFLASH\_MACRO\_0\_FREE\_SFLASH585

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF649

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.937 SFLASH\_MACRO\_0\_FREE\_SFLASH586

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF64A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.938 SFLASH\_MACRO\_0\_FREE\_SFLASH587

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF64B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.939 SFLASH\_MACRO\_0\_FREE\_SFLASH588

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF64C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.940 SFLASH\_MACRO\_0\_FREE\_SFLASH589

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF64D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.941 SFLASH\_MACRO\_0\_FREE\_SFLASH590

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF64E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.942 SFLASH\_MACRO\_0\_FREE\_SFLASH591

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF64F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.943 SFLASH\_MACRO\_0\_FREE\_SFLASH592

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF650

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.944 SFLASH\_MACRO\_0\_FREE\_SFLASH593

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF651

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.945 SFLASH\_MACRO\_0\_FREE\_SFLASH594

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF652

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.946 SFLASH\_MACRO\_0\_FREE\_SFLASH595

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF653

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.947 SFLASH\_MACRO\_0\_FREE\_SFLASH596

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF654

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.948 SFLASH\_MACRO\_0\_FREE\_SFLASH597

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF655

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.949 SFLASH\_MACRO\_0\_FREE\_SFLASH598

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF656

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.950 SFLASH\_MACRO\_0\_FREE\_SFLASH599

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF657

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.951 SFLASH\_MACRO\_0\_FREE\_SFLASH600

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF658

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.952 SFLASH\_MACRO\_0\_FREE\_SFLASH601

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF659

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.953 SFLASH\_MACRO\_0\_FREE\_SFLASH602

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF65A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.954 SFLASH\_MACRO\_0\_FREE\_SFLASH603

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF65B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.955 SFLASH\_MACRO\_0\_FREE\_SFLASH604

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF65C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.956 SFLASH\_MACRO\_0\_FREE\_SFLASH605

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF65D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.957 SFLASH\_MACRO\_0\_FREE\_SFLASH606

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF65E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.958 SFLASH\_MACRO\_0\_FREE\_SFLASH607

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF65F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.959 SFLASH\_MACRO\_0\_FREE\_SFLASH608

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF660

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.960 SFLASH\_MACRO\_0\_FREE\_SFLASH609

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF661

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.961 SFLASH\_MACRO\_0\_FREE\_SFLASH610

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF662

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.962 SFLASH\_MACRO\_0\_FREE\_SFLASH611

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF663

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.963 SFLASH\_MACRO\_0\_FREE\_SFLASH612

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF664

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.964 SFLASH\_MACRO\_0\_FREE\_SFLASH613

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF665

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.965 SFLASH\_MACRO\_0\_FREE\_SFLASH614

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF666

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.966 SFLASH\_MACRO\_0\_FREE\_SFLASH615

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF667

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.967 SFLASH\_MACRO\_0\_FREE\_SFLASH616

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF668

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.968 SFLASH\_MACRO\_0\_FREE\_SFLASH617

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF669

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.969 SFLASH\_MACRO\_0\_FREE\_SFLASH618

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF66A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.970 SFLASH\_MACRO\_0\_FREE\_SFLASH619

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF66B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.971 SFLASH\_MACRO\_0\_FREE\_SFLASH620

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF66C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.972 SFLASH\_MACRO\_0\_FREE\_SFLASH621

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF66D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.973 SFLASH\_MACRO\_0\_FREE\_SFLASH622

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF66E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.974 SFLASH\_MACRO\_0\_FREE\_SFLASH623

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF66F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.975 SFLASH\_MACRO\_0\_FREE\_SFLASH624

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF670

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.976 SFLASH\_MACRO\_0\_FREE\_SFLASH625

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF671

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.977 SFLASH\_MACRO\_0\_FREE\_SFLASH626

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF672

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.978 SFLASH\_MACRO\_0\_FREE\_SFLASH627

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF673

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.979 SFLASH\_MACRO\_0\_FREE\_SFLASH628

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF674

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.980 SFLASH\_MACRO\_0\_FREE\_SFLASH629

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF675

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.981 SFLASH\_MACRO\_0\_FREE\_SFLASH630

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF676

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.982 SFLASH\_MACRO\_0\_FREE\_SFLASH631

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF677

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.983 SFLASH\_MACRO\_0\_FREE\_SFLASH632

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF678

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.984 SFLASH\_MACRO\_0\_FREE\_SFLASH633

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF679

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.985 SFLASH\_MACRO\_0\_FREE\_SFLASH634

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF67A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.986 SFLASH\_MACRO\_0\_FREE\_SFLASH635

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF67B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.987 SFLASH\_MACRO\_0\_FREE\_SFLASH636

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF67C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.988 SFLASH\_MACRO\_0\_FREE\_SFLASH637

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF67D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.989 SFLASH\_MACRO\_0\_FREE\_SFLASH638

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF67E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.990 SFLASH\_MACRO\_0\_FREE\_SFLASH639

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF67F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.991 SFLASH\_MACRO\_0\_FREE\_SFLASH640

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.992 SFLASH\_MACRO\_0\_FREE\_SFLASH641

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF681

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.993 SFLASH\_MACRO\_0\_FREE\_SFLASH642

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF682

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.994 SFLASH\_MACRO\_0\_FREE\_SFLASH643

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF683

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.995 SFLASH\_MACRO\_0\_FREE\_SFLASH644

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF684

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.996 SFLASH\_MACRO\_0\_FREE\_SFLASH645

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF685

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.997 SFLASH\_MACRO\_0\_FREE\_SFLASH646

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF686

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.998 SFLASH\_MACRO\_0\_FREE\_SFLASH647

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF687

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.999 SFLASH\_MACRO\_0\_FREE\_SFLASH648

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF688

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1000SFLASH\_MACRO\_0\_FREE\_SFLASH649

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF689

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1001SFLASH\_MACRO\_0\_FREE\_SFLASH650

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF68A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1002SFLASH\_MACRO\_0\_FREE\_SFLASH651

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF68B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1003SFLASH\_MACRO\_0\_FREE\_SFLASH652

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF68C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1004SFLASH\_MACRO\_0\_FREE\_SFLASH653

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF68D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1005SFLASH\_MACRO\_0\_FREE\_SFLASH654

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF68E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1006SFLASH\_MACRO\_0\_FREE\_SFLASH655

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF68F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1007SFLASH\_MACRO\_0\_FREE\_SFLASH656

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF690

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1008SFLASH\_MACRO\_0\_FREE\_SFLASH657

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF691

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1009SFLASH\_MACRO\_0\_FREE\_SFLASH658

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF692

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1010SFLASH\_MACRO\_0\_FREE\_SFLASH659

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF693

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1011SFLASH\_MACRO\_0\_FREE\_SFLASH660

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF694

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1012SFLASH\_MACRO\_0\_FREE\_SFLASH661

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF695

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1013SFLASH\_MACRO\_0\_FREE\_SFLASH662

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF696

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1014SFLASH\_MACRO\_0\_FREE\_SFLASH663

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF697

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1015SFLASH\_MACRO\_0\_FREE\_SFLASH664

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF698

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1016SFLASH\_MACRO\_0\_FREE\_SFLASH665

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF699

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1017SFLASH\_MACRO\_0\_FREE\_SFLASH666

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF69A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1018SFLASH\_MACRO\_0\_FREE\_SFLASH667

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF69B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1019SFLASH\_MACRO\_0\_FREE\_SFLASH668

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF69C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1020SFLASH\_MACRO\_0\_FREE\_SFLASH669

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF69D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1021SFLASH\_MACRO\_0\_FREE\_SFLASH670

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF69E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1022SFLASH\_MACRO\_0\_FREE\_SFLASH671

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF69F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1023SFLASH\_MACRO\_0\_FREE\_SFLASH672

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1024SFLASH\_MACRO\_0\_FREE\_SFLASH673

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1025SFLASH\_MACRO\_0\_FREE\_SFLASH674

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1026SFLASH\_MACRO\_0\_FREE\_SFLASH675

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1027SFLASH\_MACRO\_0\_FREE\_SFLASH676

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1028SFLASH\_MACRO\_0\_FREE\_SFLASH677

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1029SFLASH\_MACRO\_0\_FREE\_SFLASH678

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1030SFLASH\_MACRO\_0\_FREE\_SFLASH679

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1031SFLASH\_MACRO\_0\_FREE\_SFLASH680

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1032SFLASH\_MACRO\_0\_FREE\_SFLASH681

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1033SFLASH\_MACRO\_0\_FREE\_SFLASH682

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1034SFLASH\_MACRO\_0\_FREE\_SFLASH683

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1035SFLASH\_MACRO\_0\_FREE\_SFLASH684

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1036SFLASH\_MACRO\_0\_FREE\_SFLASH685

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1037SFLASH\_MACRO\_0\_FREE\_SFLASH686

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1038SFLASH\_MACRO\_0\_FREE\_SFLASH687

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1039SFLASH\_MACRO\_0\_FREE\_SFLASH688

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1040SFLASH\_MACRO\_0\_FREE\_SFLASH689

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1041SFLASH\_MACRO\_0\_FREE\_SFLASH690

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1042SFLASH\_MACRO\_0\_FREE\_SFLASH691

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1043SFLASH\_MACRO\_0\_FREE\_SFLASH692

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1044SFLASH\_MACRO\_0\_FREE\_SFLASH693

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1045SFLASH\_MACRO\_0\_FREE\_SFLASH694

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1046SFLASH\_MACRO\_0\_FREE\_SFLASH695

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1047SFLASH\_MACRO\_0\_FREE\_SFLASH696

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1048SFLASH\_MACRO\_0\_FREE\_SFLASH697

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1049SFLASH\_MACRO\_0\_FREE\_SFLASH698

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1050SFLASH\_MACRO\_0\_FREE\_SFLASH699

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1051SFLASH\_MACRO\_0\_FREE\_SFLASH700

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1052SFLASH\_MACRO\_0\_FREE\_SFLASH701

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1053SFLASH\_MACRO\_0\_FREE\_SFLASH702

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1054SFLASH\_MACRO\_0\_FREE\_SFLASH703

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1055SFLASH\_MACRO\_0\_FREE\_SFLASH704

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1056SFLASH\_MACRO\_0\_FREE\_SFLASH705

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1057SFLASH\_MACRO\_0\_FREE\_SFLASH706

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1058SFLASH\_MACRO\_0\_FREE\_SFLASH707

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1059SFLASH\_MACRO\_0\_FREE\_SFLASH708

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1060SFLASH\_MACRO\_0\_FREE\_SFLASH709

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1061SFLASH\_MACRO\_0\_FREE\_SFLASH710

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1062SFLASH\_MACRO\_0\_FREE\_SFLASH711

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1063SFLASH\_MACRO\_0\_FREE\_SFLASH712

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1064SFLASH\_MACRO\_0\_FREE\_SFLASH713

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1065SFLASH\_MACRO\_0\_FREE\_SFLASH714

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1066SFLASH\_MACRO\_0\_FREE\_SFLASH715

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1067SFLASH\_MACRO\_0\_FREE\_SFLASH716

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1068SFLASH\_MACRO\_0\_FREE\_SFLASH717

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1069SFLASH\_MACRO\_0\_FREE\_SFLASH718

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1070SFLASH\_MACRO\_0\_FREE\_SFLASH719

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1071SFLASH\_MACRO\_0\_FREE\_SFLASH720

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1072SFLASH\_MACRO\_0\_FREE\_SFLASH721

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1073SFLASH\_MACRO\_0\_FREE\_SFLASH722

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1074SFLASH\_MACRO\_0\_FREE\_SFLASH723

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1075SFLASH\_MACRO\_0\_FREE\_SFLASH724

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1076SFLASH\_MACRO\_0\_FREE\_SFLASH725

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1077SFLASH\_MACRO\_0\_FREE\_SFLASH726

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1078SFLASH\_MACRO\_0\_FREE\_SFLASH727

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1079SFLASH\_MACRO\_0\_FREE\_SFLASH728

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1080SFLASH\_MACRO\_0\_FREE\_SFLASH729

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1081SFLASH\_MACRO\_0\_FREE\_SFLASH730

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1082SFLASH\_MACRO\_0\_FREE\_SFLASH731

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1083SFLASH\_MACRO\_0\_FREE\_SFLASH732

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1084SFLASH\_MACRO\_0\_FREE\_SFLASH733

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1085SFLASH\_MACRO\_0\_FREE\_SFLASH734

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1086SFLASH\_MACRO\_0\_FREE\_SFLASH735

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1087SFLASH\_MACRO\_0\_FREE\_SFLASH736

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1088SFLASH\_MACRO\_0\_FREE\_SFLASH737

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1089SFLASH\_MACRO\_0\_FREE\_SFLASH738

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1090SFLASH\_MACRO\_0\_FREE\_SFLASH739

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1091SFLASH\_MACRO\_0\_FREE\_SFLASH740

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1092SFLASH\_MACRO\_0\_FREE\_SFLASH741

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1093SFLASH\_MACRO\_0\_FREE\_SFLASH742

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1094SFLASH\_MACRO\_0\_FREE\_SFLASH743

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1095SFLASH\_MACRO\_0\_FREE\_SFLASH744

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1096SFLASH\_MACRO\_0\_FREE\_SFLASH745

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1097SFLASH\_MACRO\_0\_FREE\_SFLASH746

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1098SFLASH\_MACRO\_0\_FREE\_SFLASH747

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1099SFLASH\_MACRO\_0\_FREE\_SFLASH748

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1100SFLASH\_MACRO\_0\_FREE\_SFLASH749

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1101SFLASH\_MACRO\_0\_FREE\_SFLASH750

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1102SFLASH\_MACRO\_0\_FREE\_SFLASH751

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1103SFLASH\_MACRO\_0\_FREE\_SFLASH752

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1104SFLASH\_MACRO\_0\_FREE\_SFLASH753

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1105SFLASH\_MACRO\_0\_FREE\_SFLASH754

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1106SFLASH\_MACRO\_0\_FREE\_SFLASH755

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1107SFLASH\_MACRO\_0\_FREE\_SFLASH756

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1108SFLASH\_MACRO\_0\_FREE\_SFLASH757

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1109SFLASH\_MACRO\_0\_FREE\_SFLASH758

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1110SFLASH\_MACRO\_0\_FREE\_SFLASH759

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1111 SFLASH\_MACRO\_0\_FREE\_SFLASH760

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1112SFLASH\_MACRO\_0\_FREE\_SFLASH761

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1113SFLASH\_MACRO\_0\_FREE\_SFLASH762

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1114SFLASH\_MACRO\_0\_FREE\_SFLASH763

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1115SFLASH\_MACRO\_0\_FREE\_SFLASH764

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1116SFLASH\_MACRO\_0\_FREE\_SFLASH765

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1117SFLASH\_MACRO\_0\_FREE\_SFLASH766

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1118SFLASH\_MACRO\_0\_FREE\_SFLASH767

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF6FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1119SFLASH\_MACRO\_0\_FREE\_SFLASH768

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1120SFLASH\_MACRO\_0\_FREE\_SFLASH769

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF701

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1121SFLASH\_MACRO\_0\_FREE\_SFLASH770

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF702

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1122SFLASH\_MACRO\_0\_FREE\_SFLASH771

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF703

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1123SFLASH\_MACRO\_0\_FREE\_SFLASH772

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1124SFLASH\_MACRO\_0\_FREE\_SFLASH773

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF705

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1125SFLASH\_MACRO\_0\_FREE\_SFLASH774

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF706

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1126SFLASH\_MACRO\_0\_FREE\_SFLASH775

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF707

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1127SFLASH\_MACRO\_0\_FREE\_SFLASH776

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1128SFLASH\_MACRO\_0\_FREE\_SFLASH777

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF709

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1129SFLASH\_MACRO\_0\_FREE\_SFLASH778

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF70A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1130SFLASH\_MACRO\_0\_FREE\_SFLASH779

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF70B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1131SFLASH\_MACRO\_0\_FREE\_SFLASH780

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF70C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1132SFLASH\_MACRO\_0\_FREE\_SFLASH781

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF70D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1133SFLASH\_MACRO\_0\_FREE\_SFLASH782

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF70E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1134SFLASH\_MACRO\_0\_FREE\_SFLASH783

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF70F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1135SFLASH\_MACRO\_0\_FREE\_SFLASH784

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1136SFLASH\_MACRO\_0\_FREE\_SFLASH785

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF711

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1137SFLASH\_MACRO\_0\_FREE\_SFLASH786

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF712

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1138SFLASH\_MACRO\_0\_FREE\_SFLASH787

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF713

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1139SFLASH\_MACRO\_0\_FREE\_SFLASH788

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF714

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1140SFLASH\_MACRO\_0\_FREE\_SFLASH789

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF715

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1141SFLASH\_MACRO\_0\_FREE\_SFLASH790

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF716

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1142SFLASH\_MACRO\_0\_FREE\_SFLASH791

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF717

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1143SFLASH\_MACRO\_0\_FREE\_SFLASH792

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF718

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1144SFLASH\_MACRO\_0\_FREE\_SFLASH793

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF719

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1145SFLASH\_MACRO\_0\_FREE\_SFLASH794

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF71A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1146SFLASH\_MACRO\_0\_FREE\_SFLASH795

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF71B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1147SFLASH\_MACRO\_0\_FREE\_SFLASH796

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF71C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1148SFLASH\_MACRO\_0\_FREE\_SFLASH797

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF71D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1149SFLASH\_MACRO\_0\_FREE\_SFLASH798

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF71E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1150SFLASH\_MACRO\_0\_FREE\_SFLASH799

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF71F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1151SFLASH\_MACRO\_0\_FREE\_SFLASH800

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1152SFLASH\_MACRO\_0\_FREE\_SFLASH801

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF721

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1153SFLASH\_MACRO\_0\_FREE\_SFLASH802

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF722

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1154SFLASH\_MACRO\_0\_FREE\_SFLASH803

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF723

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1155SFLASH\_MACRO\_0\_FREE\_SFLASH804

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF724

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1156SFLASH\_MACRO\_0\_FREE\_SFLASH805

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF725

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1157SFLASH\_MACRO\_0\_FREE\_SFLASH806

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF726

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1158SFLASH\_MACRO\_0\_FREE\_SFLASH807

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF727

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1159SFLASH\_MACRO\_0\_FREE\_SFLASH808

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF728

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1160SFLASH\_MACRO\_0\_FREE\_SFLASH809

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF729

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1161SFLASH\_MACRO\_0\_FREE\_SFLASH810

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF72A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1162SFLASH\_MACRO\_0\_FREE\_SFLASH811

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF72B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1163SFLASH\_MACRO\_0\_FREE\_SFLASH812

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF72C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1164SFLASH\_MACRO\_0\_FREE\_SFLASH813

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF72D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1165SFLASH\_MACRO\_0\_FREE\_SFLASH814

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF72E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1166SFLASH\_MACRO\_0\_FREE\_SFLASH815

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF72F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1167SFLASH\_MACRO\_0\_FREE\_SFLASH816

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF730

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1168SFLASH\_MACRO\_0\_FREE\_SFLASH817

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF731

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1169SFLASH\_MACRO\_0\_FREE\_SFLASH818

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF732

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1170SFLASH\_MACRO\_0\_FREE\_SFLASH819

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF733

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1171SFLASH\_MACRO\_0\_FREE\_SFLASH820

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF734

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1172SFLASH\_MACRO\_0\_FREE\_SFLASH821

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF735

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1173SFLASH\_MACRO\_0\_FREE\_SFLASH822

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF736

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1174SFLASH\_MACRO\_0\_FREE\_SFLASH823

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF737

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1175SFLASH\_MACRO\_0\_FREE\_SFLASH824

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF738

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1176SFLASH\_MACRO\_0\_FREE\_SFLASH825

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF739

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1177SFLASH\_MACRO\_0\_FREE\_SFLASH826

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF73A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1178SFLASH\_MACRO\_0\_FREE\_SFLASH827

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF73B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1179SFLASH\_MACRO\_0\_FREE\_SFLASH828

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF73C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1180SFLASH\_MACRO\_0\_FREE\_SFLASH829

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF73D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1181SFLASH\_MACRO\_0\_FREE\_SFLASH830

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF73E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1182SFLASH\_MACRO\_0\_FREE\_SFLASH831

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF73F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1183SFLASH\_MACRO\_0\_FREE\_SFLASH832

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF740

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1184SFLASH\_MACRO\_0\_FREE\_SFLASH833

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF741

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1185SFLASH\_MACRO\_0\_FREE\_SFLASH834

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF742

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1186SFLASH\_MACRO\_0\_FREE\_SFLASH835

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF743

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1187SFLASH\_MACRO\_0\_FREE\_SFLASH836

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF744

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1188SFLASH\_MACRO\_0\_FREE\_SFLASH837

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF745

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1189SFLASH\_MACRO\_0\_FREE\_SFLASH838

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF746

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1190SFLASH\_MACRO\_0\_FREE\_SFLASH839

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF747

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1191SFLASH\_MACRO\_0\_FREE\_SFLASH840

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF748

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1192SFLASH\_MACRO\_0\_FREE\_SFLASH841

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF749

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1193SFLASH\_MACRO\_0\_FREE\_SFLASH842

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF74A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1194SFLASH\_MACRO\_0\_FREE\_SFLASH843

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF74B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1195SFLASH\_MACRO\_0\_FREE\_SFLASH844

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF74C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1196SFLASH\_MACRO\_0\_FREE\_SFLASH845

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF74D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1197SFLASH\_MACRO\_0\_FREE\_SFLASH846

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF74E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1198SFLASH\_MACRO\_0\_FREE\_SFLASH847

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF74F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1199SFLASH\_MACRO\_0\_FREE\_SFLASH848

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF750

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1200SFLASH\_MACRO\_0\_FREE\_SFLASH849

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF751

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1201SFLASH\_MACRO\_0\_FREE\_SFLASH850

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF752

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1202SFLASH\_MACRO\_0\_FREE\_SFLASH851

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF753

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1203SFLASH\_MACRO\_0\_FREE\_SFLASH852

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF754

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1204SFLASH\_MACRO\_0\_FREE\_SFLASH853

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF755

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1205SFLASH\_MACRO\_0\_FREE\_SFLASH854

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF756

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1206SFLASH\_MACRO\_0\_FREE\_SFLASH855

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF757

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1207SFLASH\_MACRO\_0\_FREE\_SFLASH856

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF758

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1208SFLASH\_MACRO\_0\_FREE\_SFLASH857

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF759

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1209SFLASH\_MACRO\_0\_FREE\_SFLASH858

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF75A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1210SFLASH\_MACRO\_0\_FREE\_SFLASH859

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF75B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1211SFLASH\_MACRO\_0\_FREE\_SFLASH860

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF75C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1212SFLASH\_MACRO\_0\_FREE\_SFLASH861

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF75D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1213SFLASH\_MACRO\_0\_FREE\_SFLASH862

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF75E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1214SFLASH\_MACRO\_0\_FREE\_SFLASH863

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF75F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1215SFLASH\_MACRO\_0\_FREE\_SFLASH864

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF760

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1216SFLASH\_MACRO\_0\_FREE\_SFLASH865

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF761

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1217SFLASH\_MACRO\_0\_FREE\_SFLASH866

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF762

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1218SFLASH\_MACRO\_0\_FREE\_SFLASH867

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF763

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1219SFLASH\_MACRO\_0\_FREE\_SFLASH868

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF764

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1220SFLASH\_MACRO\_0\_FREE\_SFLASH869

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF765

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1221SFLASH\_MACRO\_0\_FREE\_SFLASH870

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF766

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1222SFLASH\_MACRO\_0\_FREE\_SFLASH871

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF767

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1223SFLASH\_MACRO\_0\_FREE\_SFLASH872

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF768

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1224SFLASH\_MACRO\_0\_FREE\_SFLASH873

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF769

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1225SFLASH\_MACRO\_0\_FREE\_SFLASH874

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF76A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1226SFLASH\_MACRO\_0\_FREE\_SFLASH875

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF76B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1227SFLASH\_MACRO\_0\_FREE\_SFLASH876

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF76C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1228SFLASH\_MACRO\_0\_FREE\_SFLASH877

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF76D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1229SFLASH\_MACRO\_0\_FREE\_SFLASH878

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF76E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1230SFLASH\_MACRO\_0\_FREE\_SFLASH879

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF76F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1231SFLASH\_MACRO\_0\_FREE\_SFLASH880

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF770

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1232SFLASH\_MACRO\_0\_FREE\_SFLASH881

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF771

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1233SFLASH\_MACRO\_0\_FREE\_SFLASH882

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF772

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1234SFLASH\_MACRO\_0\_FREE\_SFLASH883

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF773

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1235SFLASH\_MACRO\_0\_FREE\_SFLASH884

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF774

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1236SFLASH\_MACRO\_0\_FREE\_SFLASH885

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF775

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1237SFLASH\_MACRO\_0\_FREE\_SFLASH886

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF776

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1238SFLASH\_MACRO\_0\_FREE\_SFLASH887

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF777

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1239SFLASH\_MACRO\_0\_FREE\_SFLASH888

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF778

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1240SFLASH\_MACRO\_0\_FREE\_SFLASH889

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF779

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1241SFLASH\_MACRO\_0\_FREE\_SFLASH890

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF77A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1242SFLASH\_MACRO\_0\_FREE\_SFLASH891

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF77B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1243SFLASH\_MACRO\_0\_FREE\_SFLASH892

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF77C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1244SFLASH\_MACRO\_0\_FREE\_SFLASH893

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF77D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1245SFLASH\_MACRO\_0\_FREE\_SFLASH894

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF77E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1246SFLASH\_MACRO\_0\_FREE\_SFLASH895

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF77F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1247SFLASH\_MACRO\_0\_FREE\_SFLASH896

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF780

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1248SFLASH\_MACRO\_0\_FREE\_SFLASH897

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF781

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1249SFLASH\_MACRO\_0\_FREE\_SFLASH898

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF782

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1250SFLASH\_MACRO\_0\_FREE\_SFLASH899

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF783

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1251SFLASH\_MACRO\_0\_FREE\_SFLASH900

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF784

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1252SFLASH\_MACRO\_0\_FREE\_SFLASH901

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF785

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1253SFLASH\_MACRO\_0\_FREE\_SFLASH902

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF786

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1254SFLASH\_MACRO\_0\_FREE\_SFLASH903

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF787

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1255SFLASH\_MACRO\_0\_FREE\_SFLASH904

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF788

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1256SFLASH\_MACRO\_0\_FREE\_SFLASH905

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF789

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1257SFLASH\_MACRO\_0\_FREE\_SFLASH906

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF78A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1258SFLASH\_MACRO\_0\_FREE\_SFLASH907

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF78B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1259SFLASH\_MACRO\_0\_FREE\_SFLASH908

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF78C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1260SFLASH\_MACRO\_0\_FREE\_SFLASH909

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF78D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1261SFLASH\_MACRO\_0\_FREE\_SFLASH910

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF78E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1262SFLASH\_MACRO\_0\_FREE\_SFLASH911

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF78F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1263SFLASH\_MACRO\_0\_FREE\_SFLASH912

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF790

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1264SFLASH\_MACRO\_0\_FREE\_SFLASH913

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF791

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1265SFLASH\_MACRO\_0\_FREE\_SFLASH914

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF792

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1266SFLASH\_MACRO\_0\_FREE\_SFLASH915

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF793

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1267SFLASH\_MACRO\_0\_FREE\_SFLASH916

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF794

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1268SFLASH\_MACRO\_0\_FREE\_SFLASH917

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF795

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1269SFLASH\_MACRO\_0\_FREE\_SFLASH918

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF796

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1270SFLASH\_MACRO\_0\_FREE\_SFLASH919

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF797

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1271SFLASH\_MACRO\_0\_FREE\_SFLASH920

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF798

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1272SFLASH\_MACRO\_0\_FREE\_SFLASH921

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF799

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1273SFLASH\_MACRO\_0\_FREE\_SFLASH922

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF79A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1274SFLASH\_MACRO\_0\_FREE\_SFLASH923

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF79B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1275SFLASH\_MACRO\_0\_FREE\_SFLASH924

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF79C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1276SFLASH\_MACRO\_0\_FREE\_SFLASH925

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF79D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1277SFLASH\_MACRO\_0\_FREE\_SFLASH926

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF79E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1278SFLASH\_MACRO\_0\_FREE\_SFLASH927

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF79F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1279SFLASH\_MACRO\_0\_FREE\_SFLASH928

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1280SFLASH\_MACRO\_0\_FREE\_SFLASH929

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1281SFLASH\_MACRO\_0\_FREE\_SFLASH930

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1282SFLASH\_MACRO\_0\_FREE\_SFLASH931

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1283SFLASH\_MACRO\_0\_FREE\_SFLASH932

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1284SFLASH\_MACRO\_0\_FREE\_SFLASH933

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1285SFLASH\_MACRO\_0\_FREE\_SFLASH934

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1286SFLASH\_MACRO\_0\_FREE\_SFLASH935

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1287SFLASH\_MACRO\_0\_FREE\_SFLASH936

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1288SFLASH\_MACRO\_0\_FREE\_SFLASH937

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1289SFLASH\_MACRO\_0\_FREE\_SFLASH938

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1290SFLASH\_MACRO\_0\_FREE\_SFLASH939

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1291SFLASH\_MACRO\_0\_FREE\_SFLASH940

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1292SFLASH\_MACRO\_0\_FREE\_SFLASH941

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1293SFLASH\_MACRO\_0\_FREE\_SFLASH942

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1294SFLASH\_MACRO\_0\_FREE\_SFLASH943

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1295SFLASH\_MACRO\_0\_FREE\_SFLASH944

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1296SFLASH\_MACRO\_0\_FREE\_SFLASH945

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1297SFLASH\_MACRO\_0\_FREE\_SFLASH946

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1298SFLASH\_MACRO\_0\_FREE\_SFLASH947

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1299SFLASH\_MACRO\_0\_FREE\_SFLASH948

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1300SFLASH\_MACRO\_0\_FREE\_SFLASH949

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1301SFLASH\_MACRO\_0\_FREE\_SFLASH950

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1302SFLASH\_MACRO\_0\_FREE\_SFLASH951

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1303SFLASH\_MACRO\_0\_FREE\_SFLASH952

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1304SFLASH\_MACRO\_0\_FREE\_SFLASH953

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1305SFLASH\_MACRO\_0\_FREE\_SFLASH954

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1306SFLASH\_MACRO\_0\_FREE\_SFLASH955

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1307SFLASH\_MACRO\_0\_FREE\_SFLASH956

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1308SFLASH\_MACRO\_0\_FREE\_SFLASH957

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1309SFLASH\_MACRO\_0\_FREE\_SFLASH958

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1310SFLASH\_MACRO\_0\_FREE\_SFLASH959

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1311SFLASH\_MACRO\_0\_FREE\_SFLASH960

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1312SFLASH\_MACRO\_0\_FREE\_SFLASH961

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1313SFLASH\_MACRO\_0\_FREE\_SFLASH962

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1314SFLASH\_MACRO\_0\_FREE\_SFLASH963

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1315SFLASH\_MACRO\_0\_FREE\_SFLASH964

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1316SFLASH\_MACRO\_0\_FREE\_SFLASH965

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1317SFLASH\_MACRO\_0\_FREE\_SFLASH966

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1318SFLASH\_MACRO\_0\_FREE\_SFLASH967

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1319SFLASH\_MACRO\_0\_FREE\_SFLASH968

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1320SFLASH\_MACRO\_0\_FREE\_SFLASH969

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1321SFLASH\_MACRO\_0\_FREE\_SFLASH970

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1322SFLASH\_MACRO\_0\_FREE\_SFLASH971

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1323SFLASH\_MACRO\_0\_FREE\_SFLASH972

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1324SFLASH\_MACRO\_0\_FREE\_SFLASH973

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1325SFLASH\_MACRO\_0\_FREE\_SFLASH974

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1326SFLASH\_MACRO\_0\_FREE\_SFLASH975

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1327SFLASH\_MACRO\_0\_FREE\_SFLASH976

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1328SFLASH\_MACRO\_0\_FREE\_SFLASH977

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1329SFLASH\_MACRO\_0\_FREE\_SFLASH978

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1330SFLASH\_MACRO\_0\_FREE\_SFLASH979

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1331SFLASH\_MACRO\_0\_FREE\_SFLASH980

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1332SFLASH\_MACRO\_0\_FREE\_SFLASH981

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1333SFLASH\_MACRO\_0\_FREE\_SFLASH982

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1334SFLASH\_MACRO\_0\_FREE\_SFLASH983

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1335SFLASH\_MACRO\_0\_FREE\_SFLASH984

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1336SFLASH\_MACRO\_0\_FREE\_SFLASH985

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1337SFLASH\_MACRO\_0\_FREE\_SFLASH986

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1338SFLASH\_MACRO\_0\_FREE\_SFLASH987

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1339SFLASH\_MACRO\_0\_FREE\_SFLASH988

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1340SFLASH\_MACRO\_0\_FREE\_SFLASH989

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1341SFLASH\_MACRO\_0\_FREE\_SFLASH990

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1342SFLASH\_MACRO\_0\_FREE\_SFLASH991

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1343SFLASH\_MACRO\_0\_FREE\_SFLASH992

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1344SFLASH\_MACRO\_0\_FREE\_SFLASH993

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1345SFLASH\_MACRO\_0\_FREE\_SFLASH994

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1346SFLASH\_MACRO\_0\_FREE\_SFLASH995

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1347SFLASH\_MACRO\_0\_FREE\_SFLASH996

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1348SFLASH\_MACRO\_0\_FREE\_SFLASH997

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1349SFLASH\_MACRO\_0\_FREE\_SFLASH998

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1350SFLASH\_MACRO\_0\_FREE\_SFLASH999

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1351SFLASH\_MACRO\_0\_FREE\_SFLASH1000

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1352SFLASH\_MACRO\_0\_FREE\_SFLASH1001

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1353SFLASH\_MACRO\_0\_FREE\_SFLASH1002

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1354SFLASH\_MACRO\_0\_FREE\_SFLASH1003

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1355SFLASH\_MACRO\_0\_FREE\_SFLASH1004

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1356SFLASH\_MACRO\_0\_FREE\_SFLASH1005

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1357SFLASH\_MACRO\_0\_FREE\_SFLASH1006

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1358SFLASH\_MACRO\_0\_FREE\_SFLASH1007

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1359SFLASH\_MACRO\_0\_FREE\_SFLASH1008

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1360SFLASH\_MACRO\_0\_FREE\_SFLASH1009

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1361 SFLASH\_MACRO\_0\_FREE\_SFLASH1010

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1362SFLASH\_MACRO\_0\_FREE\_SFLASH1011

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1363SFLASH\_MACRO\_0\_FREE\_SFLASH1012

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1364SFLASH\_MACRO\_0\_FREE\_SFLASH1013

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1365SFLASH\_MACRO\_0\_FREE\_SFLASH1014

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1366SFLASH\_MACRO\_0\_FREE\_SFLASH1015

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1367SFLASH\_MACRO\_0\_FREE\_SFLASH1016

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1368SFLASH\_MACRO\_0\_FREE\_SFLASH1017

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1369SFLASH\_MACRO\_0\_FREE\_SFLASH1018

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1370SFLASH\_MACRO\_0\_FREE\_SFLASH1019

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1371SFLASH\_MACRO\_0\_FREE\_SFLASH1020

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X



## 22.1.1372SFLASH\_MACRO\_0\_FREE\_SFLASH1021

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1373SFLASH\_MACRO\_0\_FREE\_SFLASH1022

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1374SFLASH\_MACRO\_0\_FREE\_SFLASH1023

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFF7FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommitted storage byte in Supervisory Flash Default Value: X

## 22.1.1375SFLASH\_ALT\_PROT\_ROW0

Per Page Write Protection

Address: 0x0FFF800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1376SFLASH\_ALT\_PROT\_ROW1

Per Page Write Protection

Address: 0x0FFF801

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1377SFLASH\_ALT\_PROT\_ROW2

Per Page Write Protection

Address: 0x0FFF802

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1378SFLASH\_ALT\_PROT\_ROW3

Per Page Write Protection

Address: 0x0FFF803

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1379SFLASH\_ALT\_PROT\_ROW4

Per Page Write Protection

Address: 0x0FFF804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1380SFLASH\_ALT\_PROT\_ROW5

Per Page Write Protection

Address: 0x0FFF805

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1381SFLASH\_ALT\_PROT\_ROW6

Per Page Write Protection

Address: 0x0FFF806

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1382SFLASH\_ALT\_PROT\_ROW7

Per Page Write Protection

Address: 0x0FFF807

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1383SFLASH\_ALT\_PROT\_ROW8

Per Page Write Protection

Address: 0x0FFF808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1384SFLASH\_ALT\_PROT\_ROW9

Per Page Write Protection

Address: 0x0FFF809

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1385SFLASH\_ALT\_PROT\_ROW10

Per Page Write Protection

Address: 0x0FFF80A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1386SFLASH\_ALT\_PROT\_ROW11

Per Page Write Protection

Address: 0x0FFF80B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1387SFLASH\_ALT\_PROT\_ROW12

Per Page Write Protection

Address: 0x0FFF80C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.138SFLASH\_ALT\_PROT\_ROW13

Per Page Write Protection

Address: 0x0FFF80D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1389SFLASH\_ALT\_PROT\_ROW14

Per Page Write Protection

Address: 0x0FFF80E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1390SFLASH\_ALT\_PROT\_ROW15

Per Page Write Protection

Address: 0x0FFFF80F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1391SFLASH\_ALT\_PROT\_ROW16

Per Page Write Protection

Address: 0x0FFF810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1392SFLASH\_ALT\_PROT\_ROW17

Per Page Write Protection

Address: 0x0FFFF811

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1393SFLASH\_ALT\_PROT\_ROW18

Per Page Write Protection

Address: 0x0FFF812

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1394SFLASH\_ALT\_PROT\_ROW19

Per Page Write Protection

Address: 0x0FFFF813

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1395SFLASH\_ALT\_PROT\_ROW20

Per Page Write Protection

Address: 0x0FFFF814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1396SFLASH\_ALT\_PROT\_ROW21

Per Page Write Protection

Address: 0x0FFF815

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1397SFLASH\_ALT\_PROT\_ROW22

Per Page Write Protection

Address: 0x0FFF816

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1398SFLASH\_ALT\_PROT\_ROW23

Per Page Write Protection

Address: 0x0FFF817

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1399SFLASH\_ALT\_PROT\_ROW24

Per Page Write Protection

Address: 0x0FFF818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1400SFLASH\_ALT\_PROT\_ROW25

Per Page Write Protection

Address: 0x0FFF819

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1401SFLASH\_ALT\_PROT\_ROW26

Per Page Write Protection

Address: 0x0FFF81A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1402SFLASH\_ALT\_PROT\_ROW27

Per Page Write Protection

Address: 0x0FFF81B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1403SFLASH\_ALT\_PROT\_ROW28

Per Page Write Protection

Address: 0x0FFF81C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1404SFLASH\_ALT\_PROT\_ROW29

Per Page Write Protection

Address: 0x0FFF81D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1405SFLASH\_ALT\_PROT\_ROW30

Per Page Write Protection

Address: 0x0FFF81E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1406SFLASH\_ALT\_PROT\_ROW31

Per Page Write Protection

Address: 0x0FFFF81F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1407SFLASH\_ALT\_PROT\_ROW32

Per Page Write Protection

Address: 0x0FFF820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1408SFLASH\_ALT\_PROT\_ROW33

Per Page Write Protection

Address: 0x0FFF821

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1409SFLASH\_ALT\_PROT\_ROW34

Per Page Write Protection

Address: 0x0FFF822

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1410SFLASH\_ALT\_PROT\_ROW35

Per Page Write Protection

Address: 0x0FFF823

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1411SFLASH\_ALT\_PROT\_ROW36

Per Page Write Protection

Address: 0x0FFF824

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1412SFLASH\_ALT\_PROT\_ROW37

Per Page Write Protection

Address: 0x0FFF825

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1413SFLASH\_ALT\_PROT\_ROW38

Per Page Write Protection

Address: 0x0FFF826

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1414SFLASH\_ALT\_PROT\_ROW39

Per Page Write Protection

Address: 0x0FFF827

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1415SFLASH\_ALT\_PROT\_ROW40

Per Page Write Protection

Address: 0x0FFF828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1416SFLASH\_ALT\_PROT\_ROW41

Per Page Write Protection

Address: 0x0FFF829

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1417SFLASH\_ALT\_PROT\_ROW42

Per Page Write Protection

Address: 0x0FFF82A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1418SFLASH\_ALT\_PROT\_ROW43

Per Page Write Protection

Address: 0x0FFF82B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1419SFLASH\_ALT\_PROT\_ROW44

Per Page Write Protection

Address: 0x0FFF82C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1420SFLASH\_ALT\_PROT\_ROW45

Per Page Write Protection

Address: 0x0FFF82D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1421SFLASH\_ALT\_PROT\_ROW46

Per Page Write Protection

Address: 0x0FFF82E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1422SFLASH\_ALT\_PROT\_ROW47

Per Page Write Protection

Address: 0x0FFF82F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1423SFLASH\_ALT\_PROT\_ROW48

Per Page Write Protection

Address: 0x0FFF830

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1424SFLASH\_ALT\_PROT\_ROW49

Per Page Write Protection

Address: 0x0FFFF831

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1425SFLASH\_ALT\_PROT\_ROW50

Per Page Write Protection

Address: 0x0FFF832

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1426SFLASH\_ALT\_PROT\_ROW51

Per Page Write Protection

Address: 0x0FFF833

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1427SFLASH\_ALT\_PROT\_ROW52

Per Page Write Protection

Address: 0x0FFF834

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1428SFLASH\_ALT\_PROT\_ROW53

Per Page Write Protection

Address: 0x0FFF835

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1429SFLASH\_ALT\_PROT\_ROW54

Per Page Write Protection

Address: 0x0FFF836

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1430SFLASH\_ALT\_PROT\_ROW55

Per Page Write Protection

Address: 0x0FFF837

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1431SFLASH\_ALT\_PROT\_ROW56

Per Page Write Protection

Address: 0x0FFF838

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1432SFLASH\_ALT\_PROT\_ROW57

Per Page Write Protection

Address: 0x0FFF839

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1433SFLASH\_ALT\_PROT\_ROW58

Per Page Write Protection

Address: 0x0FFF83A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1434SFLASH\_ALT\_PROT\_ROW59

Per Page Write Protection

Address: 0x0FFF83B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1435SFLASH\_ALT\_PROT\_ROW60

Per Page Write Protection

Address: 0x0FFF83C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1436SFLASH\_ALT\_PROT\_ROW61

Per Page Write Protection

Address: 0x0FFF83D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1437SFLASH\_ALT\_PROT\_ROW62

Per Page Write Protection

Address: 0x0FFF83E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1438SFLASH\_ALT\_PROT\_ROW63

Per Page Write Protection

Address: 0x0FFF83F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1439SFLASH\_ALT\_PROT\_ROW64

Per Page Write Protection

Address: 0x0FFF840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1440SFLASH\_ALT\_PROT\_ROW65

Per Page Write Protection

Address: 0x0FFF841

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1441SFLASH\_ALT\_PROT\_ROW66

Per Page Write Protection

Address: 0x0FFF842

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1442SFLASH\_ALT\_PROT\_ROW67

Per Page Write Protection

Address: 0x0FFF843

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1443SFLASH\_ALT\_PROT\_ROW68

Per Page Write Protection

Address: 0x0FFF844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1444SFLASH\_ALT\_PROT\_ROW69

Per Page Write Protection

Address: 0x0FFF845

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1445SFLASH\_ALT\_PROT\_ROW70

Per Page Write Protection

Address: 0x0FFF846

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1446SFLASH\_ALT\_PROT\_ROW71

Per Page Write Protection

Address: 0x0FFF847

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1447SFLASH\_ALT\_PROT\_ROW72

Per Page Write Protection

Address: 0x0FFF848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1448SFLASH\_ALT\_PROT\_ROW73

Per Page Write Protection

Address: 0x0FFF849

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1449SFLASH\_ALT\_PROT\_ROW74

Per Page Write Protection

Address: 0x0FFF84A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1450SFLASH\_ALT\_PROT\_ROW75

Per Page Write Protection

Address: 0x0FFF84B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1451SFLASH\_ALT\_PROT\_ROW76

Per Page Write Protection

Address: 0x0FFF84C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1452SFLASH\_ALT\_PROT\_ROW77

Per Page Write Protection

Address: 0x0FFF84D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1453SFLASH\_ALT\_PROT\_ROW78

Per Page Write Protection

Address: 0x0FFF84E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1454SFLASH\_ALT\_PROT\_ROW79

Per Page Write Protection

Address: 0x0FFF84F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1455SFLASH\_ALT\_PROT\_ROW80

Per Page Write Protection

Address: 0x0FFF850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1456SFLASH\_ALT\_PROT\_ROW81

Per Page Write Protection

Address: 0x0FFF851

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1457SFLASH\_ALT\_PROT\_ROW82

Per Page Write Protection

Address: 0x0FFF852

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1458SFLASH\_ALT\_PROT\_ROW83

Per Page Write Protection

Address: 0x0FFF853

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1459SFLASH\_ALT\_PROT\_ROW84

Per Page Write Protection

Address: 0x0FFF854

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1460SFLASH\_ALT\_PROT\_ROW85

Per Page Write Protection

Address: 0x0FFF855

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1461SFLASH\_ALT\_PROT\_ROW86

Per Page Write Protection

Address: 0x0FFF856

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1462SFLASH\_ALT\_PROT\_ROW87

Per Page Write Protection

Address: 0x0FFF857

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1463SFLASH\_ALT\_PROT\_ROW88

Per Page Write Protection

Address: 0x0FFF858

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1464SFLASH\_ALT\_PROT\_ROW89

Per Page Write Protection

Address: 0x0FFF859

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1465SFLASH\_ALT\_PROT\_ROW90

Per Page Write Protection

Address: 0x0FFF85A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1466SFLASH\_ALT\_PROT\_ROW91

Per Page Write Protection

Address: 0x0FFF85B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1467SFLASH\_ALT\_PROT\_ROW92

Per Page Write Protection

Address: 0x0FFF85C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1468SFLASH\_ALT\_PROT\_ROW93

Per Page Write Protection

Address: 0x0FFF85D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1469SFLASH\_ALT\_PROT\_ROW94

Per Page Write Protection

Address: 0x0FFF85E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1470SFLASH\_ALT\_PROT\_ROW95

Per Page Write Protection

Address: 0x0FFFF85F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1471SFLASH\_ALT\_PROT\_ROW96

Per Page Write Protection

Address: 0x0FFF860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1472SFLASH\_ALT\_PROT\_ROW97

Per Page Write Protection

Address: 0x0FFF861

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1473SFLASH\_ALT\_PROT\_ROW98

Per Page Write Protection

Address: 0x0FFF862

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1474SFLASH\_ALT\_PROT\_ROW99

Per Page Write Protection

Address: 0x0FFF863

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1475SFLASH\_ALT\_PROT\_ROW100

Per Page Write Protection

Address: 0x0FFF864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1476SFLASH\_ALT\_PROT\_ROW101

Per Page Write Protection

Address: 0x0FFF865

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1477SFLASH\_ALT\_PROT\_ROW102

Per Page Write Protection

Address: 0x0FFF866

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1478SFLASH\_ALT\_PROT\_ROW103

Per Page Write Protection

Address: 0x0FFF867

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1479SFLASH\_ALT\_PROT\_ROW104

Per Page Write Protection

Address: 0x0FFF868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1480SFLASH\_ALT\_PROT\_ROW105

Per Page Write Protection

Address: 0x0FFF869

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1481SFLASH\_ALT\_PROT\_ROW106

Per Page Write Protection

Address: 0x0FFF86A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1482SFLASH\_ALT\_PROT\_ROW107

Per Page Write Protection

Address: 0x0FFF86B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1483SFLASH\_ALT\_PROT\_ROW108

Per Page Write Protection

Address: 0x0FFF86C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1484SFLASH\_ALT\_PROT\_ROW109

Per Page Write Protection

Address: 0x0FFF86D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1485SFLASH\_ALT\_PROT\_ROW110

Per Page Write Protection

Address: 0x0FFF86E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1486SFLASH\_ALT\_PROT\_ROW111

Per Page Write Protection

Address: 0x0FFF86F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1487SFLASH\_ALT\_PROT\_ROW112

Per Page Write Protection

Address: 0x0FFF870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1488SFLASH\_ALT\_PROT\_ROW113

Per Page Write Protection

Address: 0x0FFF871

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1489SFLASH\_ALT\_PROT\_ROW114

Per Page Write Protection

Address: 0x0FFF872

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1490SFLASH\_ALT\_PROT\_ROW115

Per Page Write Protection

Address: 0x0FFF873

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1491SFLASH\_ALT\_PROT\_ROW116

Per Page Write Protection

Address: 0x0FFF874

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1492SFLASH\_ALT\_PROT\_ROW117

Per Page Write Protection

Address: 0x0FFF875

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1493SFLASH\_ALT\_PROT\_ROW118

Per Page Write Protection

Address: 0x0FFF876

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1494SFLASH\_ALT\_PROT\_ROW119

Per Page Write Protection

Address: 0x0FFF877

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1495SFLASH\_ALT\_PROT\_ROW120

Per Page Write Protection

Address: 0x0FFF878

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1496SFLASH\_ALT\_PROT\_ROW121

Per Page Write Protection

Address: 0x0FFF879

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1497SFLASH\_ALT\_PROT\_ROW122

Per Page Write Protection

Address: 0x0FFF87A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1498SFLASH\_ALT\_PROT\_ROW123

Per Page Write Protection

Address: 0x0FFF87B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1499SFLASH\_ALT\_PROT\_ROW124

Per Page Write Protection

Address: 0x0FFF87C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1500SFLASH\_ALT\_PROT\_ROW125

Per Page Write Protection

Address: 0x0FFF87D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1501SFLASH\_ALT\_PROT\_ROW126

Per Page Write Protection

Address: 0x0FFF87E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1502SFLASH\_ALT\_PROT\_ROW127

Per Page Write Protection

Address: 0x0FFF87F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1503SFLASH\_ALT\_PROT\_ROW128

Per Page Write Protection

Address: 0x0FFF880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1504SFLASH\_ALT\_PROT\_ROW129

Per Page Write Protection

Address: 0x0FFF881

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1505SFLASH\_ALT\_PROT\_ROW130

Per Page Write Protection

Address: 0x0FFF882

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1506SFLASH\_ALT\_PROT\_ROW131

Per Page Write Protection

Address: 0x0FFF883

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1507SFLASH\_ALT\_PROT\_ROW132

Per Page Write Protection

Address: 0x0FFF884

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1508SFLASH\_ALT\_PROT\_ROW133

Per Page Write Protection

Address: 0x0FFF885

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1509SFLASH\_ALT\_PROT\_ROW134

Per Page Write Protection

Address: 0x0FFF886

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1510SFLASH\_ALT\_PROT\_ROW135

Per Page Write Protection

Address: 0x0FFF887

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1511SFLASH\_ALT\_PROT\_ROW136

Per Page Write Protection

Address: 0x0FFF888

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1512SFLASH\_ALT\_PROT\_ROW137

Per Page Write Protection

Address: 0x0FFF889

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1513SFLASH\_ALT\_PROT\_ROW138

Per Page Write Protection

Address: 0x0FFF88A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1514SFLASH\_ALT\_PROT\_ROW139

Per Page Write Protection

Address: 0x0FFF88B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1515SFLASH\_ALT\_PROT\_ROW140

Per Page Write Protection

Address: 0x0FFF88C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1516SFLASH\_ALT\_PROT\_ROW141

Per Page Write Protection

Address: 0x0FFF88D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1517SFLASH\_ALT\_PROT\_ROW142

Per Page Write Protection

Address: 0x0FFF88E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1518SFLASH\_ALT\_PROT\_ROW143

Per Page Write Protection

Address: 0x0FFF88F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1519SFLASH\_ALT\_PROT\_ROW144

Per Page Write Protection

Address: 0x0FFF890

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1520SFLASH\_ALT\_PROT\_ROW145

Per Page Write Protection

Address: 0x0FFF891

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1521SFLASH\_ALT\_PROT\_ROW146

Per Page Write Protection

Address: 0x0FFF892

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1522SFLASH\_ALT\_PROT\_ROW147

Per Page Write Protection

Address: 0x0FFF893

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1523SFLASH\_ALT\_PROT\_ROW148

Per Page Write Protection

Address: 0x0FFF894

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1524SFLASH\_ALT\_PROT\_ROW149

Per Page Write Protection

Address: 0x0FFF895

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1525SFLASH\_ALT\_PROT\_ROW150

Per Page Write Protection

Address: 0x0FFF896

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1526SFLASH\_ALT\_PROT\_ROW151

Per Page Write Protection

Address: 0x0FFF897

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1527SFLASH\_ALT\_PROT\_ROW152

Per Page Write Protection

Address: 0x0FFF898

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1528SFLASH\_ALT\_PROT\_ROW153

Per Page Write Protection

Address: 0x0FFF899

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1529SFLASH\_ALT\_PROT\_ROW154

Per Page Write Protection

Address: 0x0FFF89A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1530SFLASH\_ALT\_PROT\_ROW155

Per Page Write Protection

Address: 0x0FFF89B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1531SFLASH\_ALT\_PROT\_ROW156

Per Page Write Protection

Address: 0x0FFF89C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1532SFLASH\_ALT\_PROT\_ROW157

Per Page Write Protection

Address: 0x0FFF89D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1533SFLASH\_ALT\_PROT\_ROW158

Per Page Write Protection

Address: 0x0FFF89E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1534SFLASH\_ALT\_PROT\_ROW159

Per Page Write Protection

Address: 0x0FFF89F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1535SFLASH\_ALT\_PROT\_ROW160

Per Page Write Protection

Address: 0x0FFF8A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1536SFLASH\_ALT\_PROT\_ROW161

Per Page Write Protection

Address: 0x0FFF8A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1537SFLASH\_ALT\_PROT\_ROW162

Per Page Write Protection

Address: 0x0FFF8A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1538SFLASH\_ALT\_PROT\_ROW163

Per Page Write Protection

Address: 0x0FFF8A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1539SFLASH\_ALT\_PROT\_ROW164

Per Page Write Protection

Address: 0x0FFF8A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1540SFLASH\_ALT\_PROT\_ROW165

Per Page Write Protection

Address: 0x0FFF8A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1541SFLASH\_ALT\_PROT\_ROW166

Per Page Write Protection

Address: 0x0FFF8A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1542SFLASH\_ALT\_PROT\_ROW167

Per Page Write Protection

Address: 0x0FFF8A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1543SFLASH\_ALT\_PROT\_ROW168

Per Page Write Protection

Address: 0x0FFF8A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1544SFLASH\_ALT\_PROT\_ROW169

Per Page Write Protection

Address: 0x0FFF8A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1545SFLASH\_ALT\_PROT\_ROW170

Per Page Write Protection

Address: 0x0FFFF8AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1546SFLASH\_ALT\_PROT\_ROW171

Per Page Write Protection

Address: 0x0FFFF8AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1547SFLASH\_ALT\_PROT\_ROW172

Per Page Write Protection

Address: 0x0FFFF8AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1548SFLASH\_ALT\_PROT\_ROW173

Per Page Write Protection

Address: 0x0FFFF8AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1549SFLASH\_ALT\_PROT\_ROW174

Per Page Write Protection

Address: 0x0FFFF8AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1550SFLASH\_ALT\_PROT\_ROW175

Per Page Write Protection

Address: 0x0FFF8AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1551SFLASH\_ALT\_PROT\_ROW176

Per Page Write Protection

Address: 0x0FFF8B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1552SFLASH\_ALT\_PROT\_ROW177

Per Page Write Protection

Address: 0x0FFF8B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1553SFLASH\_ALT\_PROT\_ROW178

Per Page Write Protection

Address: 0x0FFF8B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1554SFLASH\_ALT\_PROT\_ROW179

Per Page Write Protection

Address: 0x0FFF8B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1555SFLASH\_ALT\_PROT\_ROW180

Per Page Write Protection

Address: 0x0FFF8B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1556SFLASH\_ALT\_PROT\_ROW181

Per Page Write Protection

Address: 0x0FFF8B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1557SFLASH\_ALT\_PROT\_ROW182

Per Page Write Protection

Address: 0x0FFF8B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1558SFLASH\_ALT\_PROT\_ROW183

Per Page Write Protection

Address: 0x0FFF8B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1559SFLASH\_ALT\_PROT\_ROW184

Per Page Write Protection

Address: 0x0FFF8B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1560SFLASH\_ALT\_PROT\_ROW185

Per Page Write Protection

Address: 0x0FFF8B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1561SFLASH\_ALT\_PROT\_ROW186

Per Page Write Protection

Address: 0x0FFFF8BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1562SFLASH\_ALT\_PROT\_ROW187

Per Page Write Protection

Address: 0x0FFFF8BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1563SFLASH\_ALT\_PROT\_ROW188

Per Page Write Protection

Address: 0x0FFFF8BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1564SFLASH\_ALT\_PROT\_ROW189

Per Page Write Protection

Address: 0x0FFFF8BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1565SFLASH\_ALT\_PROT\_ROW190

Per Page Write Protection

Address: 0x0FFFF8BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1566SFLASH\_ALT\_PROT\_ROW191

Per Page Write Protection

Address: 0x0FFF8BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1567SFLASH\_ALT\_PROT\_ROW192

Per Page Write Protection

Address: 0x0FFF8C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1568SFLASH\_ALT\_PROT\_ROW193

Per Page Write Protection

Address: 0x0FFF8C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1569SFLASH\_ALT\_PROT\_ROW194

Per Page Write Protection

Address: 0x0FFF8C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1570SFLASH\_ALT\_PROT\_ROW195

Per Page Write Protection

Address: 0x0FFF8C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1571SFLASH\_ALT\_PROT\_ROW196

Per Page Write Protection

Address: 0x0FFF8C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1572SFLASH\_ALT\_PROT\_ROW197

Per Page Write Protection

Address: 0x0FFF8C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1573SFLASH\_ALT\_PROT\_ROW198

Per Page Write Protection

Address: 0x0FFF8C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1574SFLASH\_ALT\_PROT\_ROW199

Per Page Write Protection

Address: 0x0FFF8C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1575SFLASH\_ALT\_PROT\_ROW200

Per Page Write Protection

Address: 0x0FFF8C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1576SFLASH\_ALT\_PROT\_ROW201

Per Page Write Protection

Address: 0x0FFF8C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1577SFLASH\_ALT\_PROT\_ROW202

Per Page Write Protection

Address: 0x0FFFF8CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1578SFLASH\_ALT\_PROT\_ROW203

Per Page Write Protection

Address: 0x0FFFF8CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1579SFLASH\_ALT\_PROT\_ROW204

Per Page Write Protection

Address: 0x0FFFF8CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1580SFLASH\_ALT\_PROT\_ROW205

Per Page Write Protection

Address: 0x0FFFF8CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1581SFLASH\_ALT\_PROT\_ROW206

Per Page Write Protection

Address: 0x0FFFF8CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1582SFLASH\_ALT\_PROT\_ROW207

Per Page Write Protection

Address: 0x0FFFF8CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1583SFLASH\_ALT\_PROT\_ROW208

Per Page Write Protection

Address: 0x0FFF8D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1584SFLASH\_ALT\_PROT\_ROW209

Per Page Write Protection

Address: 0x0FFF8D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1585SFLASH\_ALT\_PROT\_ROW210

Per Page Write Protection

Address: 0x0FFF8D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1586SFLASH\_ALT\_PROT\_ROW211

Per Page Write Protection

Address: 0x0FFF8D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1587SFLASH\_ALT\_PROT\_ROW212

Per Page Write Protection

Address: 0x0FFF8D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1588SFLASH\_ALT\_PROT\_ROW213

Per Page Write Protection

Address: 0x0FFF8D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1589SFLASH\_ALT\_PROT\_ROW214

Per Page Write Protection

Address: 0x0FFF8D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1590SFLASH\_ALT\_PROT\_ROW215

Per Page Write Protection

Address: 0x0FFF8D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1591SFLASH\_ALT\_PROT\_ROW216

Per Page Write Protection

Address: 0x0FFF8D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1592SFLASH\_ALT\_PROT\_ROW217

Per Page Write Protection

Address: 0x0FFF8D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1593SFLASH\_ALT\_PROT\_ROW218

Per Page Write Protection

Address: 0x0FFFF8DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1594SFLASH\_ALT\_PROT\_ROW219

Per Page Write Protection

Address: 0x0FFFF8DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1595SFLASH\_ALT\_PROT\_ROW220

Per Page Write Protection

Address: 0x0FFFF8DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1596SFLASH\_ALT\_PROT\_ROW221

Per Page Write Protection

Address: 0x0FFFF8DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1597SFLASH\_ALT\_PROT\_ROW222

Per Page Write Protection

Address: 0x0FFFF8DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1598SFLASH\_ALT\_PROT\_ROW223

Per Page Write Protection

Address: 0x0FFFF8DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1599SFLASH\_ALT\_PROT\_ROW224

Per Page Write Protection

Address: 0x0FFF8E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1600SFLASH\_ALT\_PROT\_ROW225

Per Page Write Protection

Address: 0x0FFF8E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1601SFLASH\_ALT\_PROT\_ROW226

Per Page Write Protection

Address: 0x0FFF8E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1602SFLASH\_ALT\_PROT\_ROW227

Per Page Write Protection

Address: 0x0FFF8E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1603SFLASH\_ALT\_PROT\_ROW228

Per Page Write Protection

Address: 0x0FFF8E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1604SFLASH\_ALT\_PROT\_ROW229

Per Page Write Protection

Address: 0x0FFF8E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1605SFLASH\_ALT\_PROT\_ROW230

Per Page Write Protection

Address: 0x0FFF8E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1606SFLASH\_ALT\_PROT\_ROW231

Per Page Write Protection

Address: 0x0FFF8E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1607SFLASH\_ALT\_PROT\_ROW232

Per Page Write Protection

Address: 0x0FFF8E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1608SFLASH\_ALT\_PROT\_ROW233

Per Page Write Protection

Address: 0x0FFF8E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1609SFLASH\_ALT\_PROT\_ROW234

Per Page Write Protection

Address: 0x0FFFF8EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1610SFLASH\_ALT\_PROT\_ROW235

Per Page Write Protection

Address: 0x0FFFF8EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1611SFLASH\_ALT\_PROT\_ROW236

Per Page Write Protection

Address: 0x0FFFF8EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1612SFLASH\_ALT\_PROT\_ROW237

Per Page Write Protection

Address: 0x0FFFF8ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1613SFLASH\_ALT\_PROT\_ROW238

Per Page Write Protection

Address: 0x0FFFF8EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1614SFLASH\_ALT\_PROT\_ROW239

Per Page Write Protection

Address: 0x0FFF8EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1615SFLASH\_ALT\_PROT\_ROW240

Per Page Write Protection

Address: 0x0FFF8F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1616SFLASH\_ALT\_PROT\_ROW241

Per Page Write Protection

Address: 0x0FFF8F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1617SFLASH\_ALT\_PROT\_ROW242

Per Page Write Protection

Address: 0x0FFF8F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1618SFLASH\_ALT\_PROT\_ROW243

Per Page Write Protection

Address: 0x0FFF8F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1619SFLASH\_ALT\_PROT\_ROW244

Per Page Write Protection

Address: 0x0FFF8F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1620SFLASH\_ALT\_PROT\_ROW245

Per Page Write Protection

Address: 0x0FFF8F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1621SFLASH\_ALT\_PROT\_ROW246

Per Page Write Protection

Address: 0x0FFF8F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1622SFLASH\_ALT\_PROT\_ROW247

Per Page Write Protection

Address: 0x0FFFF8F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1623SFLASH\_ALT\_PROT\_ROW248

Per Page Write Protection

Address: 0x0FFF8F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1624SFLASH\_ALT\_PROT\_ROW249

Per Page Write Protection

Address: 0x0FFF8F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1625SFLASH\_ALT\_PROT\_ROW250

Per Page Write Protection

Address: 0x0FFF8FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1626SFLASH\_ALT\_PROT\_ROW251

Per Page Write Protection

Address: 0x0FFF8FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1627SFLASH\_ALT\_PROT\_ROW252

Per Page Write Protection

Address: 0x0FFFF8FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X



## 22.1.1628SFLASH\_ALT\_PROT\_ROW253

Per Page Write Protection

Address: 0x0FFFF8FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1629SFLASH\_ALT\_PROT\_ROW254

Per Page Write Protection

Address: 0x0FFF8FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1630SFLASH\_ALT\_PROT\_ROW255

Per Page Write Protection

Address: 0x0FFF8FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

## 22.1.1631SFLASH\_ALT\_PP

Preprogram Settings

Address: 0x0FFFB20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.1632SFLASH\_ALT\_E

Erase Settings

Address: 0x0FFFB24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.1633SFLASH\_ALT\_P

Program Settings

Address: 0x0FFFB28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.1634SFLASH\_ALT\_EA\_E

Erase All - Erase Settings

Address: 0x0FFFB2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.1635SFLASH\_ALT\_EA\_P

Erase All - Program Settings

Address: 0x0FFFFB30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X



## 22.1.1636SFLASH\_ALT\_ES\_E

Erase Sector - Erase Settings

Address: 0x0FFFFB34

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.1637SFLASH\_ALT\_ES\_P\_EO

Erase Sector - Program EO Settings

Address: 0x0FFFFB38

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spdif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

## 22.1.1638SFLASH\_ALT\_E\_VCTAT

Bandgap Trim Register

Address: 0x0FFFB3C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_EN ABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

## 22.1.1639SFLASH\_ALT\_P\_VCTAT

Bandgap Trim Register

Address: 0x0FFFFB3D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
<b>SW Access</b>	None	RW	RW		RW			
<b>HW Access</b>	None	None	None		None			
<b>Name</b>	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

## 23 SPC Interface (SPCIF) Registers



This section discusses the SPCIF registers. It lists all the registers in mapping tables, in address order.

### 23.1 Register Details

Register Name	Address
<a href="#">SPCIF_GEOMETRY</a>	0x40110000
<a href="#">SPCIF_INTR</a>	0x401107F0
<a href="#">SPCIF_INTR_SET</a>	0x401107F4
<a href="#">SPCIF_INTR_MASK</a>	0x401107F8
<a href="#">SPCIF_INTR_MASKED</a>	0x401107FC

## 23.1.1 SPCIF\_GEOMETRY

Flash/NVL geometry information

Address: 0x40110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FLASH [7:0]							
Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	FLASH [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	R		R		R			
HW Access	W		W		W			
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	RW	R						
HW Access	None	W						
Name	DE_CPD_LP	NVL [30:24]						

Bits	Name	Description
31	DE_CPD_LP	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM. Default Value: 0
30 : 24	NVL	NVLatch size in Byte multiples (chip dependent): "0": 0 Bytes "1": 1 Byte ... "127": 127 Bytes Default Value: Undefined

### 23.1.1 SPCIF\_GEOMETRY (continued)

23 : 22	FLASH_ROW	<p>Page size in 64 Byte multiples (chip dependent):</p> <p>"0": 64 byte</p> <p>"1": 128 byte</p> <p>"2": 192 byte</p> <p>"3": 256 byte</p> <p>The page size is used to determine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE).</p> <p>Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes.</p> <p>Default Value: Undefined</p>
21 : 20	NUM_FLASH	<p>Number of flash macros (chip dependent):</p> <p>"0": 1 flash macro</p> <p>"1": 2 flash macros</p> <p>"2": 3 flash macros</p> <p>"3": 4 flash macros</p> <p>Default Value: Undefined</p>
19 : 16	SFLASH	<p>Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together:</p> <p>"0": 256 Bytes.</p> <p>"1": 2*256 Bytes.</p> <p>...</p> <p>"15": 16*256 Bytes.</p> <p>Default Value: Undefined</p>
15 : 0	FLASH	<p>Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together:</p> <p>"0": 256 Bytes.</p> <p>"1": 2*256 Bytes.</p> <p>...</p> <p>"65535": 65536*256 Bytes.</p> <p>Default Value: Undefined</p>

## 23.1.2 SPCIF\_INTR

SPCIF interrupt request register

Address: 0x401107F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Timer counter value reaches "0". Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0



## 23.1.3 SPCIF\_INTR\_SET

SPCIF interrupt set request register

Address: 0x401107F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Write INTR_SET field with '1' to set corresponding INTR field. Default Value: 0

## 23.1.4 SPCIF\_INTR\_MASK

SPCIF interrupt mask register

Address: 0x401107F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Mask for corresponding field in INTR register. Default Value: 0

## 23.1.5 SPCIF\_INTR\_MASKED

SPCIF interrupt masked request register

Address: 0x401107FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Logical and of corresponding request and mask fields. Default Value: 0

## 24 TCPWM Registers



This section discusses the TCPWM registers. It lists all the registers in mapping tables, in address order.

---

### 24.1 Register Details

Register Name	Address
<a href="#">TCPWM_CTRL</a>	0x40200000
<a href="#">TCPWM_CMD</a>	0x40200008
<a href="#">TCPWM_INTR_CAUSE</a>	0x4020000C

## 24.1.1 TCPWM\_CTRL

TCPWM control register 0.

Address: 0x40200000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				COUNTER_ENABLED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	COUNTER_ENABLED	<p>Counter enables for counters 0 up to CNT_NR-1.</p> <p>'0': counter disabled.</p> <p>'1': counter enabled.</p> <p>Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes:</p> <ul style="list-style-type: none"> <li>- the associated counter triggers in the CMD register are set to '0'.</li> <li>- the counter's interrupt cause fields in counter's INTR register.</li> <li>- the counter's status fields in counter's STATUS register..</li> <li>- the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match").</li> <li>- the counter's line outputs ("line_out" and "line_compl_out").</li> </ul> <p>Default Value: 0</p>

## 24.1.2 TCPWM\_CMD

TCPWM command register.

Address: 0x40200008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [7:4]				COUNTER_CAPTURE [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [15:12]				COUNTER_RELOAD [11:8]			
Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [23:20]				COUNTER_STOP [19:16]			
Bits	31	30	29	28	27	26	25	24
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [31:28]				COUNTER_START [27:24]			

Bits	Name	Description
27 : 24	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
19 : 16	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
11 : 8	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
3 : 0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

## 24.1.3 TCPWM\_INTR\_CAUSE

TCPWM Counter interrupt cause register.

Address: 0x4020000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				COUNTER_INT [3:0]			
Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

## 25 Test (TST) Registers



This section discusses the TST registers. It lists all the registers in mapping tables, in address order.

---

### 25.1 Register Details

Register Name	Address
<a href="#">TST_MODE</a>	0x40030014



## 25.1.1 TST\_MODE

Test Mode Control Register

Address: 0x40030014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	
HW Access	None					RW	None	
Name	None [7:3]					SWD_CONNECTED	None [1:0]	

  

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

  

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

  

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	None					
HW Access	R	RW	None					
Name	TEST_MODE	POR_BYPASS	None [29:24]					

Bits	Name	Description
31	TEST_MODE	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image. Default Value: 0
30	POR_BYPASS	This bit is set during POR bypass mode. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below). Default Value: 0
2	SWD_CONNECTED	0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) (Note: this bit replaces TST_CTRL.SWD_CONNECTED) Default Value: 0

# Revision History



## Revision History

Document Title: CYBL1XXXX Family Programmable Radio-on-Chip With BLE (PRoC® BLE) Registers Technical Reference Manual (TRM)				
Document Number: 001-93112				
Revision	ECN#	Issue Date	Origin of Change	Description of Change
**	4417938	06/29/2014	SKUV	Specification for new silicon.
*A	4605909	12/24/2014	GCG	Updated register description as per production silicon.
*B	4683570	06/08/2014	UDYG	Updated System Resource Sub System Registers Updated SCB Registers Updated Supervisory Flash (128 KB) Registers Added Supervisory Flash (256 KB) Registers
*C	5144090	02/25/2016	UDYG	Update title of the document Added BLE Sub System Version 2 Registers Added DMA Controller Registers Added DMA Descriptor Registers