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Continuity of document content

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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY96640 series is based on Cypress advanced F²MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F²MC-16LX family thus allowing for easy migration of F²MC-16LX Software to the new F²MC-16FX products.

F²MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz to 8MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

■ Technology

0.18µm CMOS

■ CPU

- F²MC-16FX CPU
- Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
- 8-byte instruction queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

■ System clock

- On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
- 4MHz to 8MHz crystal oscillator (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 8MHz external clock for devices with fast clock input feature
- 32.768kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
- Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
- The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
- Low Power Consumption - 13 operating modes (different Run, Sleep, Timer, Stop modes)

■ On-chip voltage regulator

Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption

■ Low voltage detection function

Reset is generated when supply voltage falls below programmable reference voltage

■ Code Security

Protects Flash Memory content from unintended read-out

■ DMA

Automatic transfer function independent of CPU, can be assigned freely to resources

■ Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

■ CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1Mbps
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

■ USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

■ I²C

- Up to 400kbps
- Master and Slave functionality, 7-bit and 10-bit addressing

■ A/D converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function
- Scan Disable Function

■ Source Clock Timers

Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

- **Hardware Watchdog Timer**
 - Hardware watchdog timer is active after reset
 - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- **Reload Timers**
 - 16-bit wide
 - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
 - Event count function
- **Free-Running Timers**
 - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
 - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- **Input Capture Units**
 - 16-bit wide
 - Signals an interrupt upon external event
 - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- **Output Compare Units**
 - 16-bit wide
 - Signals an interrupt when a match with Free-running Timer occurs
 - A pair of compare registers can be used to generate an output signal
- **Programmable Pulse Generator**
 - 16-bit down counter, cycle and duty setting registers
 - Can be used as 2×8 -bit PPG
 - Interrupt at trigger, counter borrow and/or duty match
 - PWM operation and one-shot operation
 - Internal prescaler allows 1, $1/4$, $1/16$, $1/64$ of peripheral clock as counter clock or of selected Reload timer underflow as clock input
 - Can be triggered by software or reload timer
 - Can trigger ADC conversion
 - Timing point capture
 - Start delay
- **Quadrature Position/Revolution Counter (QPRC)**
 - Up/down count mode, Phase difference count mode, Count mode with direction
 - 16-bit position counter
 - 16-bit revolution counter
 - Two 16-bit compare registers with interrupt
 - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable
- **Real Time Clock**
 - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
 - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
 - Read/write accessible second/minute/hour registers
 - Can signal interrupts every half second/second/minute/hour/day
 - Internal clock divider and prescaler provide exact 1s clock
- **External Interrupts**
 - Edge or Level sensitive
 - Interrupt mask bit per channel
 - Each available CAN channel RX has an external interrupt for wake-up
 - Selected USART channels SIN have an external interrupt for wake-up
- **Non Maskable Interrupt**
 - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
 - Once enabled, cannot be disabled other than by reset
 - High or Low level sensitive
 - Pin shared with external interrupt 0
- **I/O Ports**
 - Most of the external pins can be used as general purpose I/O
 - All push-pull outputs (except when used as I²C SDA/SCL line)
 - Bit-wise programmable as input/output or peripheral signal
 - Bit-wise programmable input enable
 - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
 - Bit-wise programmable pull-up resistor
- **Built-in On Chip Debugger (OCD)**
 - One-wire debug tool interface
 - Break function:
 - Hardware break: 6 points (shared with code event)
 - Software break: 4096 points
 - Event function
 - Code event: 6 points (shared with hardware break)
 - Data event: 6 points
 - Event sequencer: 2 levels + reset
 - Execution time measurement function
 - Trace function: 42 branches
 - Security function
- **Flash Memory**
 - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
 - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
 - Supports automatic programming, Embedded Algorithm
 - Write/Erase/Erase-Suspend/Resume commands
 - A flag indicating completion of the automatic algorithm
 - Erase can be performed on each sector individually
 - Sector protection
 - Flash Security feature to protect the content of the Flash
 - Low voltage detection during Flash erases or writes

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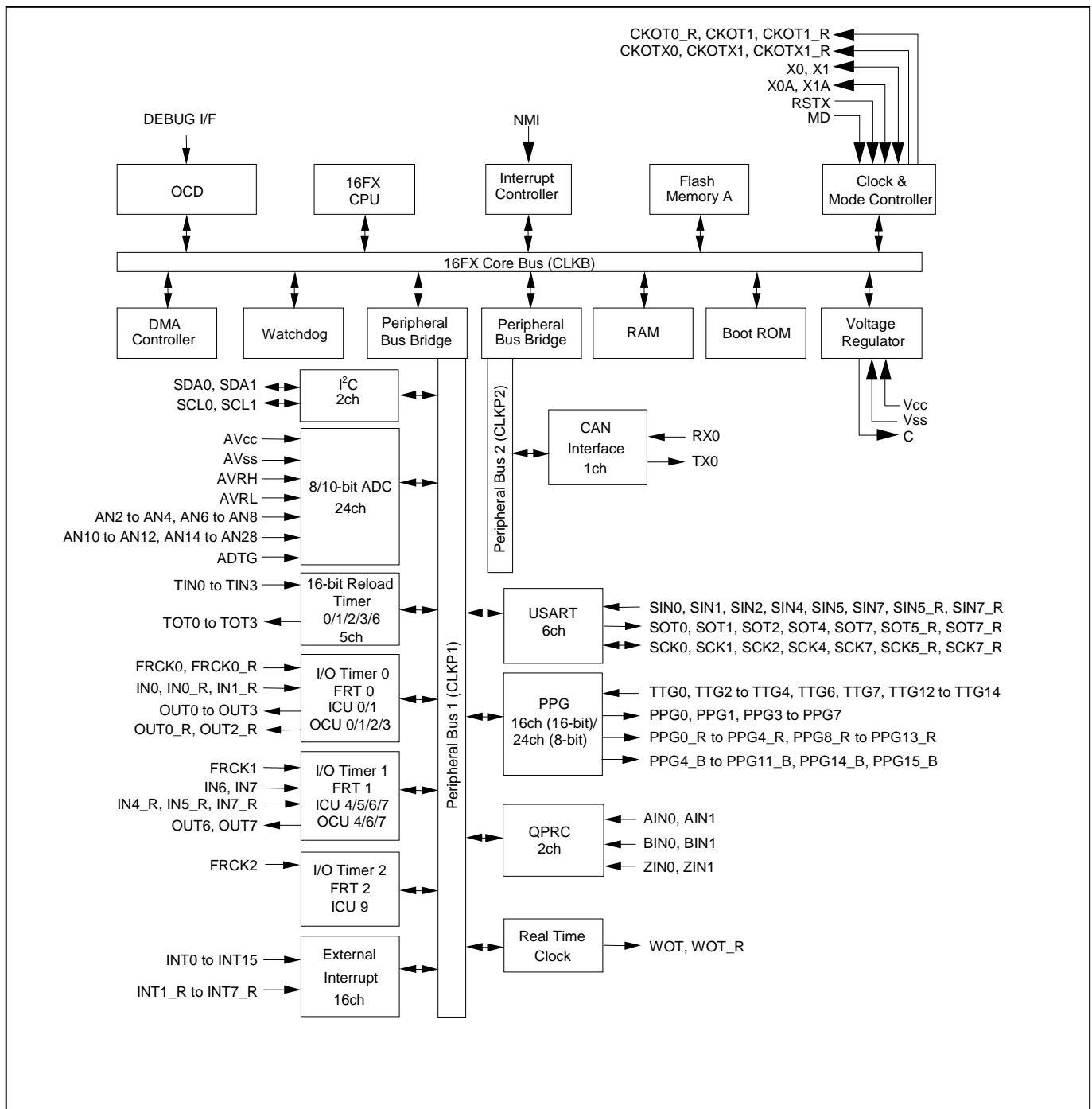
1. Product Lineup

Features		CY96640	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
64.5KB + 32KB	10KB	CY96F643R, CY96F643A	Product Options R: MCU with CAN A: MCU without CAN
128.5KB + 32KB	16KB	CY96F645R, CY96F645A	
256.5KB + 32KB	24KB	CY96F646R	
384.5KB + 32KB	28KB	CY96F647R	
Package		LQFP-100 LQ1100	
DMA		4ch	
USART		6ch	LIN-USART 0 to 2/4/5/7
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO	No	
I ² C		2ch	I ² C 0/1
8/10-bit A/D Converter		24ch	AN 2 to 4/6 to 8/10 to 12/14 to 28
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	No	
16-bit Reload Timer (RLT)		5ch	RLT 0 to 3/6
16-bit Free-Running Timer (FRT)		3ch	FRT 0 to 2
16-bit Input Capture Unit (ICU)		7ch (1 channel for LIN-USART)	ICU 0/1/4 to 7/9 (ICU 9 for LIN-USART)
16-bit Output Compare Unit (OCU)		7ch	OCU 0 to 4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)		16ch (16-bit) / 24ch (8-bit)	PPG 0 to 15
	with Timing point capture	Yes	
	with Start delay	Yes	
	with Ramp	No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 0 32 Message Buffers
External Interrupts (INT)		16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		79 (Dual clock mode) 81 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note:

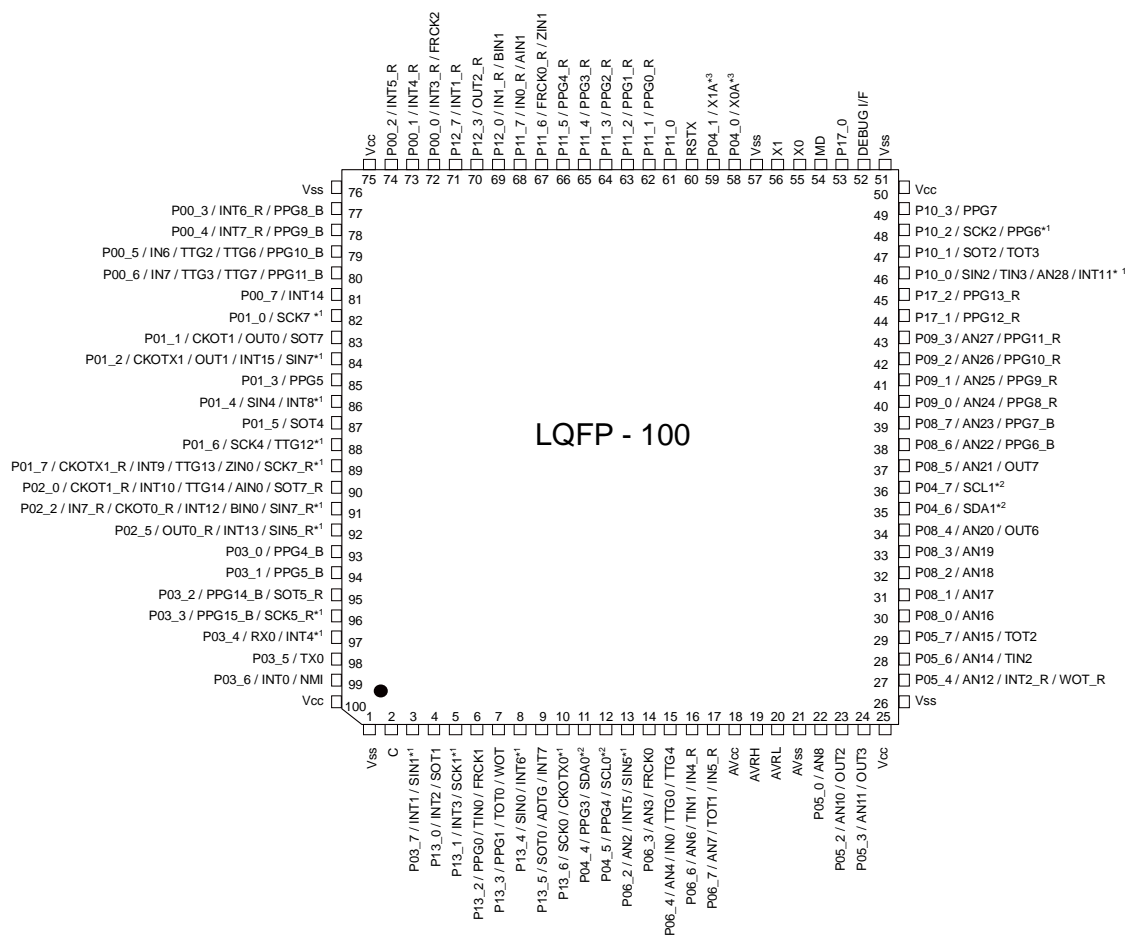
All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.

2. Block Diagram



3. Pin Assignment

(Top view)



(LQ100)

*1: CMOS input level only

*2: CMOS input level only for I²C

*3: Please set ROM Configuration Block (RCB) to use the subclock.

Other than those above, general-purpose pins have only automotive input level.

4. Pin Description

Pin Name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVRL	ADC	A/D converter low reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
CKOTXn_R	Clock Output function	Relocated Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
FRCKn	Free-Running Timer	Free-Running Timer n input pin
FRCKn_R	Free-Running Timer	Relocated Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SCLn	I ² C	I ² C interface n clock I/O input/output pin
SDAn	I ² C	I ² C interface n serial data I/O input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin

Pin Name	Feature	Description
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin
WOT	RTC	Real Time clock output pin
WOT_R	RTC	Relocated Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin

5. Pin Circuit Type

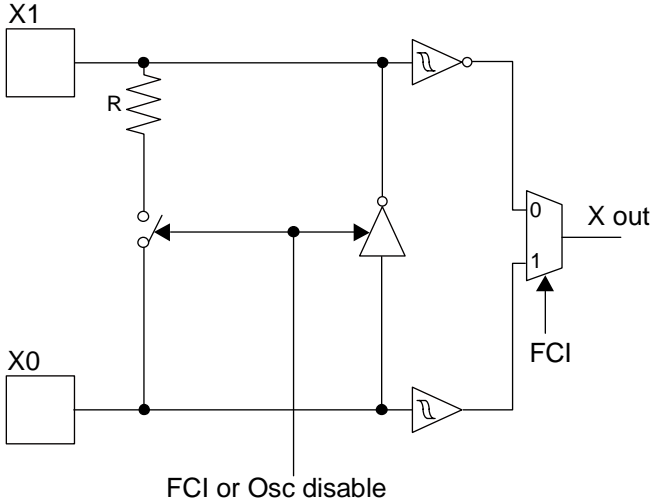
Pin No.	I/O Circuit Type*	Pin Name
1	Supply	Vss
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	M	P13_1 / INT3 / SCK1
6	H	P13_2 / PPG0 / TIN0 / FRCK1
7	H	P13_3 / PPG1 / TOT0 / WOT
8	M	P13_4 / SIN0 / INT6
9	H	P13_5 / SOT0 / ADTG / INT7
10	M	P13_6 / SCK0 / CKOTX0
11	N	P04_4 / PPG3 / SDA0
12	N	P04_5 / PPG4 / SCL0
13	I	P06_2 / AN2 / INT5 / SIN5
14	K	P06_3 / AN3 / FRCK0
15	K	P06_4 / AN4 / IN0 / TTG0 / TTG4
16	K	P06_6 / AN6 / TIN1 / IN4_R
17	K	P06_7 / AN7 / TOT1 / IN5_R
18	Supply	AVcc
19	G	AVRH
20	G	AVRL
21	Supply	AVss
22	K	P05_0 / AN8
23	K	P05_2 / AN10 / OUT2
24	K	P05_3 / AN11 / OUT3
25	Supply	Vcc
26	Supply	Vss
27	K	P05_4 / AN12 / INT2_R / WOT_R
28	K	P05_6 / AN14 / TIN2
29	K	P05_7 / AN15 / TOT2
30	K	P08_0 / AN16
31	K	P08_1 / AN17
32	K	P08_2 / AN18
33	K	P08_3 / AN19
34	K	P08_4 / AN20 / OUT6
35	N	P04_6 / SDA1
36	N	P04_7 / SCL1
37	K	P08_5 / AN21 / OUT7
38	K	P08_6 / AN22 / PPG6_B

Pin No.	I/O Circuit Type*	Pin Name
39	K	P08_7 / AN23 / PPG7_B
40	K	P09_0 / AN24 / PPG8_R
41	K	P09_1 / AN25 / PPG9_R
42	K	P09_2 / AN26 / PPG10_R
43	K	P09_3 / AN27 / PPG11_R
44	H	P17_1 / PPG12_R
45	H	P17_2 / PPG13_R
46	I	P10_0 / SIN2 / TIN3 / AN28 / INT11
47	H	P10_1 / SOT2 / TOT3
48	M	P10_2 / SCK2 / PPG6
49	H	P10_3 / PPG7
50	Supply	Vcc
51	Supply	Vss
52	O	DEBUG I/F
53	H	P17_0
54	C	MD
55	A	X0
56	A	X1
57	Supply	Vss
58	B	P04_0 / X0A
59	B	P04_1 / X1A
60	C	RSTX
61	H	P11_0
62	H	P11_1 / PPG0_R
63	H	P11_2 / PPG1_R
64	H	P11_3 / PPG2_R
65	H	P11_4 / PPG3_R
66	H	P11_5 / PPG4_R
67	H	P11_6 / FRCK0_R / ZIN1
68	H	P11_7 / IN0_R / AIN1
69	H	P12_0 / IN1_R / BIN1
70	H	P12_3 / OUT2_R
71	H	P12_7 / INT1_R
72	H	P00_0 / INT3_R / FRCK2
73	H	P00_1 / INT4_R
74	H	P00_2 / INT5_R
75	Supply	Vcc
76	Supply	Vss
77	H	P00_3 / INT6_R / PPG8_B

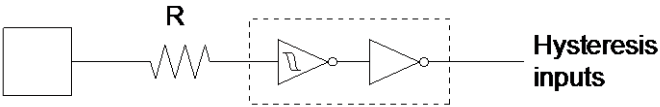
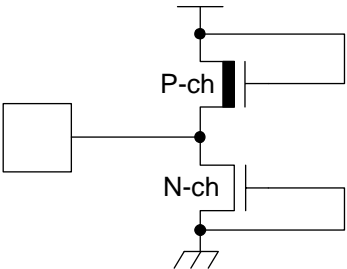
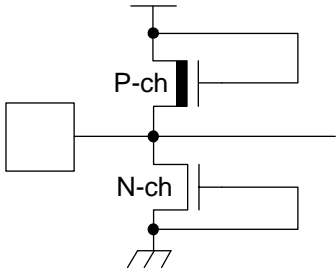
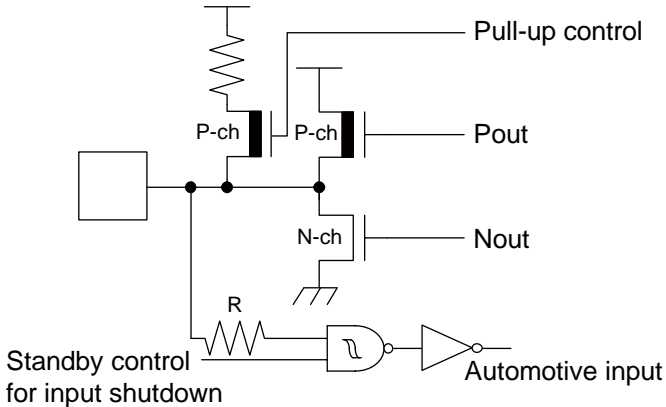
Pin No.	I/O Circuit Type*	Pin Name
78	H	P00_4 / INT7_R / PPG9_B
79	H	P00_5 / IN6 / TTG2 / TTG6 / PPG10_B
80	H	P00_6 / IN7 / TTG3 / TTG7 / PPG11_B
81	H	P00_7 / INT14
82	M	P01_0 / SCK7
83	H	P01_1 / CKOT1 / OUT0 / SOT7
84	M	P01_2 / CKOTX1 / OUT1 / INT15 / SIN7
85	H	P01_3 / PPG5
86	M	P01_4 / SIN4 / INT8
87	H	P01_5 / SOT4
88	M	P01_6 / SCK4 / TTG12
89	M	P01_7 / CKOTX1_R / INT9 / TTG13 / ZIN0 / SCK7_R
90	H	P02_0 / CKOT1_R / INT10 / TTG14 / AIN0 / SOT7_R
91	M	P02_2 / IN7_R / CKOT0_R / INT12 / BIN0 / SIN7_R
92	M	P02_5 / OUT0_R / INT13 / SIN5_R
93	H	P03_0 / PPG4_B
94	H	P03_1 / PPG5_B
95	H	P03_2 / PPG14_B / SOT5_R
96	M	P03_3 / PPG15_B / SCK5_R
97	M	P03_4 / RX0 / INT4
98	H	P03_5 / TX0
99	H	P03_6 / INT0 / NMI
100	Supply	Vcc

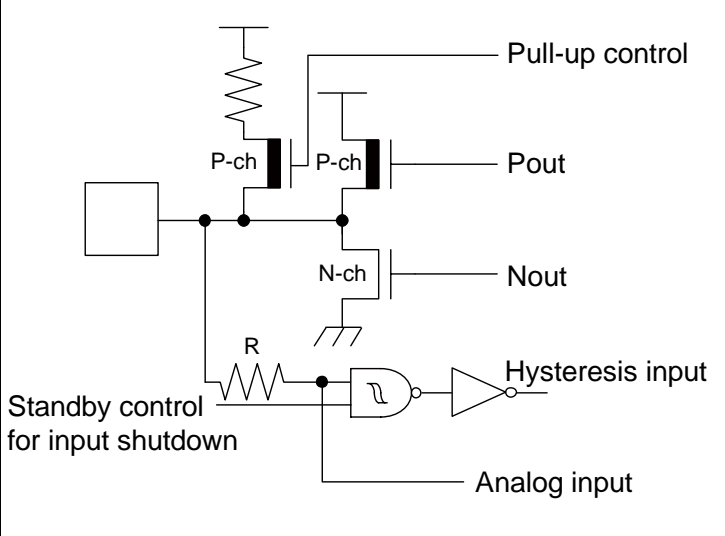
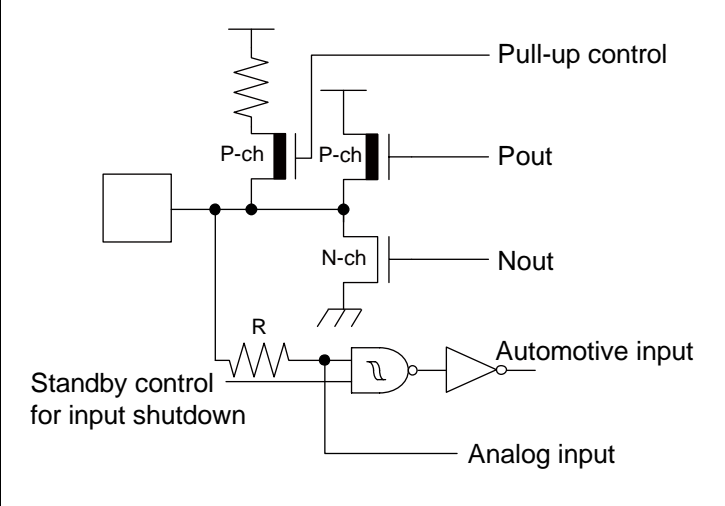
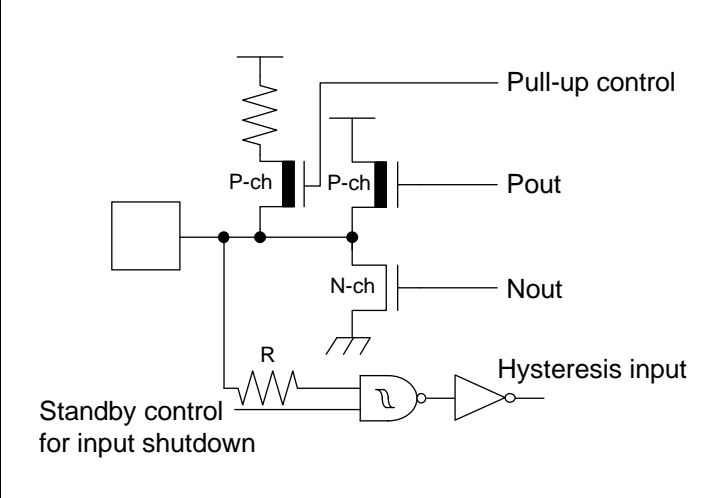
*: See "I/O Circuit Type" for details on the I/O circuit types.

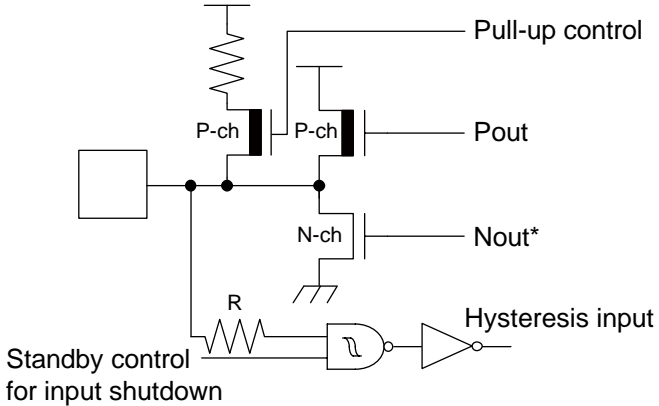
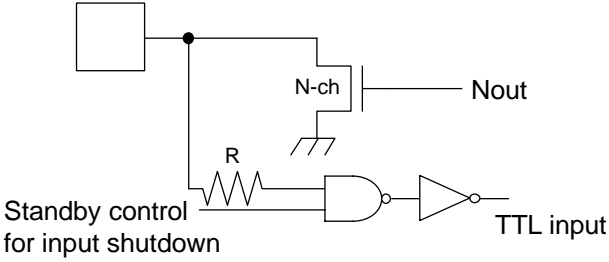
6. I/O Circuit Type

Type	Circuit	Remarks
A	 <p style="text-align: center;">FCI or Osc disable</p>	<p>High-speed oscillation circuit:</p> <ul style="list-style-type: none"> • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 1.0MΩ • The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
B	<p>The diagram illustrates a low-speed oscillation circuit shared with GPIO functionality. It features two identical input/output stages. Each stage includes a pull-up resistor, P-ch and N-ch transistors (Pout, Nout), a feedback resistor R, and an automotive input with a pull-up resistor. A central block contains an oscillator circuit with inputs X1A and X0A, a feedback resistor R, and an FCI input to an X out multiplexer. A control line 'FCI or Osc disable' is connected to the oscillator circuit.</p>	<p>Low-speed oscillation circuit shared with GPIO functionality:</p> <ul style="list-style-type: none"> • Feedback resistor = approx. $5.0M\Omega$ • GPIO functionality selectable (CMOS level output ($I_{OL} = 4mA$, $I_{OH} = -4mA$), Automotive input with input shutdown function and programmable pull-up resistor)

Type	Circuit	Remarks
C		<p>CMOS hysteresis input pin</p>
F		<p>Power supply input protection circuit</p>
G		<ul style="list-style-type: none"> • A/D converter ref+ (AVRH)/ ref- (AVRL) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH/AVRL
H		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4mA$, $I_{OH} = -4mA$) • Automotive input with input shutdown function • Programmable pull-up resistor

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor • Analog input
K		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
M		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor

Type	Circuit	Remarks
N	 <p>The diagram shows a CMOS output stage. A pull-up resistor is connected to the output node. Two P-channel MOSFETs (P-ch) are connected to the output node, controlled by a 'Pull-up control' signal. An N-channel MOSFET (N-ch) is connected to the output node and ground, controlled by an 'Nout*' signal. A 'Standby control for input shutdown' signal is connected to the input of an AND gate through a resistor 'R'. The output of the AND gate is connected to the input of an inverter, which produces the 'Hysteresis input' signal.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor <p>*: N-channel transistor has slew rate control according to I²C spec, irrespective of usage.</p>
O	 <p>The diagram shows an open-drain output stage. An N-channel MOSFET (N-ch) is connected to the output node and ground, controlled by an 'Nout' signal. A 'Standby control for input shutdown' signal is connected to the input of an AND gate through a resistor 'R'. The output of the AND gate is connected to the input of an inverter, which produces the 'TTL input' signal.</p>	<ul style="list-style-type: none"> • Open-drain I/O • Output 25mA, $V_{CC} = 2.7\text{V}$ • TTL input

7. Memory Map

FF:FFFF _H	USER ROM*1
DE:0000 _H DD:FFFF _H	Reserved
10:0000 _H	Boot-ROM
0F:C000 _H	Peripheral
0E:9000 _H	Reserved
01:0000 _H	ROM/RAM MIRROR
00:8000 _H	Internal RAM bank0
RAMSTART0*2	Reserved
00:0C00 _H	Peripheral
00:0380 _H	GPR*3
00:0180 _H	DMA
00:0100 _H	Reserved
00:00F0 _H	Reserved
00:0000 _H	Peripheral

*1: For details about USER ROM area, see “User Rom Memory Map For Flash Devices” on the following pages.

*2: For RAMSTART Addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. RAMSTART Addresses

Devices	Bank 0 RAM Size	RAMSTART0
CY96F643	10KB	00:5A00 _H
CY96F645	16KB	00:4200 _H
CY96F646	24KB	00:2200 _H
CY96F647	28KB	00:1200 _H

9. User Rom Memory Map For Flash Devices

		CY96F643	CY96F645	CY96F646	CY96F647				
CPU mode address	Flash memory mode address	Flash size 64.5KB + 32KB	Flash size 128.5KB + 32KB	Flash size 256.5KB + 32KB	Flash size 384.5KB + 32KB				
FF:FFFF _H	3F:FFFF _H	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A			
FF:0000 _H	3F:0000 _H	Reserved	Reserved	Reserved	Reserved				
FE:FFFF _H	3E:FFFF _H						SA38 - 64KB	SA38 - 64KB	SA38 - 64KB
FE:0000 _H	3E:0000 _H						SA37 - 64KB	SA37 - 64KB	SA37 - 64KB
FD:FFFF _H	3D:FFFF _H						SA36 - 64KB	SA36 - 64KB	SA36 - 64KB
FD:0000 _H	3D:0000 _H								SA35 - 64KB
FC:FFFF _H	3C:FFFF _H								SA34 - 64KB
FC:0000 _H	3C:0000 _H								
FB:FFFF _H	3B:FFFF _H								
FB:0000 _H	3B:0000 _H								
FA:FFFF _H	3A:FFFF _H								
FA:0000 _H	3A:0000 _H								
FS:FFFF _H									
DF:A000 _H						Bank B of Flash A			
DF:9FFF _H	1F:9FFF _H	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB				
DF:8000 _H	1F:8000 _H	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB				
DF:7FFF _H	1F:7FFF _H	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB				
DF:6000 _H	1F:6000 _H	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB				
DF:5FFF _H	1F:5FFF _H					Bank A of Flash A			
DF:4000 _H	1F:4000 _H	SAS - 512B*	SAS - 512B*	SAS - 512B*	SAS - 512B*				
DF:3FFF _H	1F:3FFF _H	Reserved	Reserved	Reserved	Reserved				
DF:2000 _H	1F:2000 _H								
DF:1FFF _H	1F:1FFF _H								
DF:0000 _H	1F:0000 _H								
DE:FFFF _H									
DE:0000 _H									

*: Physical address area of SAS-512B is from DF: 0000_H to DF:01FF_H.
 Others (from DF:0200_H to DF:1FFF_H) is mirror area of SAS-512B.
 Sector SAS contains the ROM configuration block RCBA at CPU address DF: 0000_H -DF: 01FF_H.
 SAS cannot be used for E²PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96640		
Pin Number	USART Number	Normal Function
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
46	USART2	SIN2
47		SOT2
48		SCK2
86	USART4	SIN4
87		SOT4
88		SCK4

11. Interrupt Vector Table

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
0	3FC _H	CALLV0	No	-	CALLV instruction
1	3F8 _H	CALLV1	No	-	CALLV instruction
2	3F4 _H	CALLV2	No	-	CALLV instruction
3	3F0 _H	CALLV3	No	-	CALLV instruction
4	3EC _H	CALLV4	No	-	CALLV instruction
5	3E8 _H	CALLV5	No	-	CALLV instruction
6	3E4 _H	CALLV6	No	-	CALLV instruction
7	3E0 _H	CALLV7	No	-	CALLV instruction
8	3DC _H	RESET	No	-	Reset vector
9	3D8 _H	INT9	No	-	INT9 instruction
10	3D4 _H	EXCEPTION	No	-	Undefined instruction execution
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Clock Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	LVDI	No	16	Low Voltage Detector
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	EXTINT1	Yes	18	External Interrupt 1
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	EXTINT5	Yes	22	External Interrupt 5
23	3A0 _H	EXTINT6	Yes	23	External Interrupt 6
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	EXTINT8	Yes	25	External Interrupt 8
26	394 _H	EXTINT9	Yes	26	External Interrupt 9
27	390 _H	EXTINT10	Yes	27	External Interrupt 10
28	38C _H	EXTINT11	Yes	28	External Interrupt 11
29	388 _H	EXTINT12	Yes	29	External Interrupt 12
30	384 _H	EXTINT13	Yes	30	External Interrupt 13
31	380 _H	EXTINT14	Yes	31	External Interrupt 14
32	37C _H	EXTINT15	Yes	32	External Interrupt 15
33	378 _H	CAN0	No	33	CAN Controller 0
34	374 _H	-	-	34	Reserved
35	370 _H	-	-	35	Reserved
36	36C _H	-	-	36	Reserved
37	368 _H	-	-	37	Reserved
38	364 _H	PPG0	Yes	38	Programmable Pulse Generator 0

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
39	360 _H	PPG1	Yes	39	Programmable Pulse Generator 1
40	35C _H	PPG2	Yes	40	Programmable Pulse Generator 2
41	358 _H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 _H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350 _H	PPG5	Yes	43	Programmable Pulse Generator 5
44	34C _H	PPG6	Yes	44	Programmable Pulse Generator 6
45	348 _H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344 _H	PPG8	Yes	46	Programmable Pulse Generator 8
47	340 _H	PPG9	Yes	47	Programmable Pulse Generator 9
48	33C _H	PPG10	Yes	48	Programmable Pulse Generator 10
49	338 _H	PPG11	Yes	49	Programmable Pulse Generator 11
50	334 _H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330 _H	PPG13	Yes	51	Programmable Pulse Generator 13
52	32C _H	PPG14	Yes	52	Programmable Pulse Generator 14
53	328 _H	PPG15	Yes	53	Programmable Pulse Generator 15
54	324 _H	-	-	54	Reserved
55	320 _H	-	-	55	Reserved
56	31C _H	-	-	56	Reserved
57	318 _H	-	-	57	Reserved
58	314 _H	RLT0	Yes	58	Reload Timer 0
59	310 _H	RLT1	Yes	59	Reload Timer 1
60	30C _H	RLT2	Yes	60	Reload Timer 2
61	308 _H	RLT3	Yes	61	Reload Timer 3
62	304 _H	-	-	62	Reserved
63	300 _H	-	-	63	Reserved
64	2FC _H	RLT6	Yes	64	Reload Timer 6
65	2F8 _H	ICU0	Yes	65	Input Capture Unit 0
66	2F4 _H	ICU1	Yes	66	Input Capture Unit 1
67	2F0 _H	-	-	67	Reserved
68	2EC _H	-	-	68	Reserved
69	2E8 _H	ICU4	Yes	69	Input Capture Unit 4
70	2E4 _H	ICU5	Yes	70	Input Capture Unit 5
71	2E0 _H	ICU6	Yes	71	Input Capture Unit 6
72	2DC _H	ICU7	Yes	72	Input Capture Unit 7
73	2D8 _H	-	-	73	Reserved
74	2D4 _H	ICU9	Yes	74	Input Capture Unit 9
75	2D0 _H	-	-	75	Reserved
76	2CC _H	-	-	76	Reserved
77	2C8 _H	OCU0	Yes	77	Output Compare Unit 0
78	2C4 _H	OCU1	Yes	78	Output Compare Unit 1
79	2C0 _H	OCU2	Yes	79	Output Compare Unit 2
80	2BC _H	OCU3	Yes	80	Output Compare Unit 3

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
81	2B8 _H	OCU4	Yes	81	Output Compare Unit 4
82	2B4 _H	-	-	82	Reserved
83	2B0 _H	OCU6	Yes	83	Output Compare Unit 6
84	2AC _H	OCU7	Yes	84	Output Compare Unit 7
85	2A8 _H	-	-	85	Reserved
86	2A4 _H	-	-	86	Reserved
87	2A0 _H	-	-	87	Reserved
88	29C _H	-	-	88	Reserved
89	298 _H	FRT0	Yes	89	Free-Running Timer 0
90	294 _H	FRT1	Yes	90	Free-Running Timer 1
91	290 _H	FRT2	Yes	91	Free-Running Timer 2
92	28C _H	-	-	92	Reserved
93	288 _H	RTC0	No	93	Real Time Clock
94	284 _H	CAL0	No	94	Clock Calibration Unit
95	280 _H	-	-	95	Reserved
96	27C _H	IIC0	Yes	96	I ² C interface 0
97	278 _H	IIC1	Yes	97	I ² C interface 1
98	274 _H	ADC0	Yes	98	A/D Converter 0
99	270 _H	-	-	99	Reserved
100	26C _H	-	-	100	Reserved
101	268 _H	LINR0	Yes	101	LIN USART 0 RX
102	264 _H	LINT0	Yes	102	LIN USART 0 TX
103	260 _H	LINR1	Yes	103	LIN USART 1 RX
104	25C _H	LINT1	Yes	104	LIN USART 1 TX
105	258 _H	LINR2	Yes	105	LIN USART 2 RX
106	254 _H	LINT2	Yes	106	LIN USART 2 TX
107	250 _H	-	-	107	Reserved
108	24C _H	-	-	108	Reserved
109	248 _H	LINR4	Yes	109	LIN USART 4 RX
110	244 _H	LINT4	Yes	110	LIN USART 4 TX
111	240 _H	LINR5	Yes	111	LIN USART 5 RX
112	23C _H	LINT5	Yes	112	LIN USART 5 TX
113	238 _H	-	-	113	Reserved
114	234 _H	-	-	114	Reserved
115	230 _H	LINR7	Yes	115	LIN USART 7 RX
116	22C _H	LINT7	Yes	116	LIN USART 7 TX
117	228 _H	-	-	117	Reserved
118	224 _H	-	-	118	Reserved
119	220 _H	-	-	119	Reserved
120	21C _H	-	-	120	Reserved

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
121	218 _H	-	-	121	Reserved
122	214 _H	-	-	122	Reserved
123	210 _H	-	-	123	Reserved
124	20C _H	-	-	124	Reserved
125	208 _H	-	-	125	Reserved
126	204 _H	-	-	126	Reserved
127	200 _H	-	-	127	Reserved
128	1FC _H	-	-	128	Reserved
129	1F8 _H	-	-	129	Reserved
130	1F4 _H	-	-	130	Reserved
131	1F0 _H	-	-	131	Reserved
132	1EC _H	-	-	132	Reserved
133	1E8 _H	FLASHA	Yes	133	Flash memory A interrupt
134	1E4 _H	-	-	134	Reserved
135	1E0 _H	-	-	135	Reserved
136	1DC _H	-	-	136	Reserved
137	1D8 _H	QPRC0	Yes	137	Quad Position/Revolution counter 0
138	1D4 _H	QPRC1	Yes	138	Quad Position/Revolution counter 1
139	1D0 _H	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	1CC _H	-	-	140	Reserved
141	1C8 _H	-	-	141	Reserved
142	1C4 _H	-	-	142	Reserved
143	1C0 _H	-	-	143	Reserved

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

12.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame
CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

13. Handling Devices

Special Care is Required for the following when Handling the Device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- SMC power supply pins
- Serial communication
- Mode Pin (MD)

13.1 Latch-Up Prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

13.2 Unused Pins Handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than $2k\Omega$.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External Clock Usage

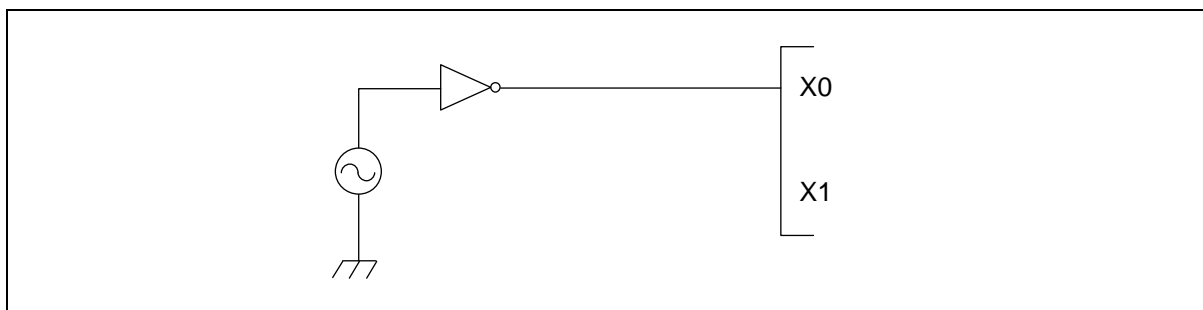
The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 Single Phase External Clock for Main Oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.

And supply 1.8V power to the external clock.

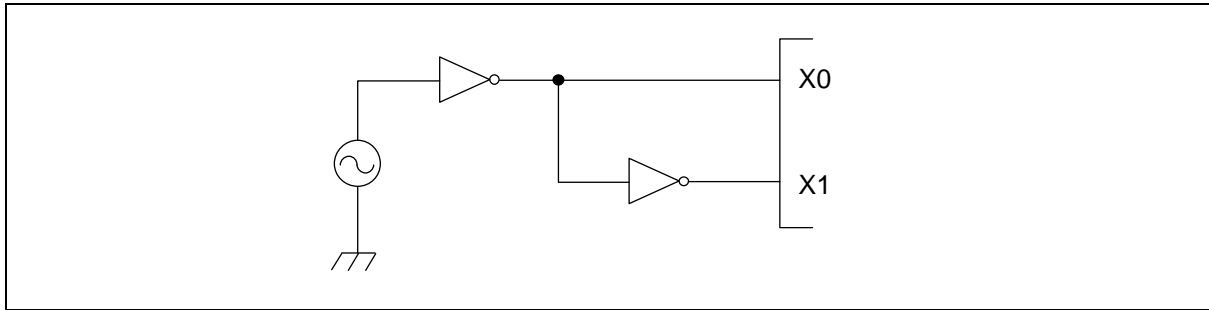


13.3.2 Single Phase External Clock for Sub Oscillator

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

13.3.3 Opposite Phase External Clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



13.4 Notes on PLL Clock Mode Operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.5 Power Supply Pins (V_{CC}/V_{SS})

It is required that all V_{CC} -level as well as all V_{SS} -level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at V_{CC} pin must use the one of a capacity value that is larger than C_s .

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about $0.1\mu\text{F}$ between V_{CC} and V_{SS} pins as close as possible to V_{CC} and V_{SS} pins.

13.6 Crystal Oscillator and ceramic resonator Circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines and to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.7 Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, $AVRH$ must not exceed AV_{CC} . Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.8 Pin Handling when not using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 μ s from 0.2V to 2.7V.

13.10 Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/ μ s or less in instantaneous fluctuation for power supply switching.

13.11 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.12 Mode Pin (MD)

Connect the mode pin directly to V_{CC} or V_{SS} pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to V_{CC} or V_{SS} pin and provide a low-impedance connection.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	V _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	
Analog power supply voltage*1	AV _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _{CC} = AV _{CC} *2
Analog reference voltage*1	AVRH, AVRL	-	V _{SS} - 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVRH, AV _{CC} ≥ AVRL, AVRH > AVRL, AVRL ≥ AV _{SS}
Input voltage*1	V _I	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _I ≤ V _{CC} + 0.3V*3
Output voltage*1	V _O	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _O ≤ V _{CC} + 0.3V*3
Maximum Clamp Current	I _{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins *4
Total Maximum Clamp Current	Σ I _{CLAMP}	-	-	26	mA	Applicable to general purpose I/O pins *4
"L" level maximum output current	I _{OL}	-	-	15	mA	
"L" level average output current	I _{OLAV}	-	-	4	mA	
"L" level maximum overall output current	ΣI _{OL}	-	-	66	mA	
"L" level average overall output current	ΣI _{OLAV}	-	-	33	mA	
"H" level maximum output current	I _{OH}	-	-	-15	mA	
"H" level average output current	I _{OHAV}	-	-	-4	mA	
"H" level maximum overall output current	ΣI _{OH}	-	-	-66	mA	
"H" level average overall output current	ΣI _{OHAV}	-	-	-33	mA	
Power consumption*5	P _D	T _A = +125°C	-	416*6	mW	
Operating ambient temperature	T _A	-	-40	+125*7	°C	
Storage temperature	T _{STG}	-	-55	+150	°C	

*1: This parameter is based on V_{SS} = AV_{SS} = 0V.

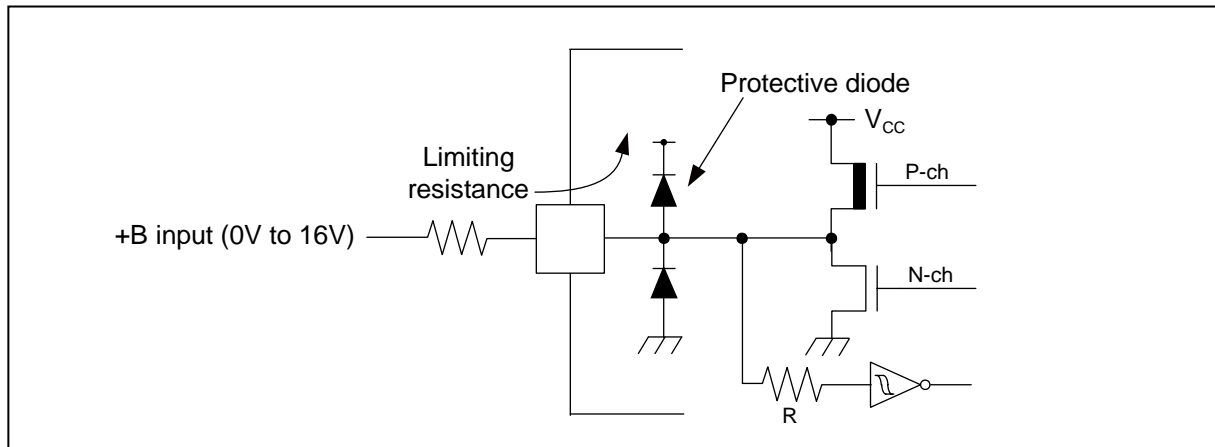
*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of standard ports depend on V_{CC}.

*4: Applicable to all general purpose I/O pins (Pnn_m).

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
- Sample recommended circuits:



- *5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
 The actual power dissipation depends on the customer application and can be calculated as follows:
 $P_D = P_{IO} + P_{INT}$
 $P_{IO} = \sum (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
 $P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
 I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
 I_A is the analog current consumption into AV_{CC} .
- *6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.
- *7: Write/erase to a large sector in flash memory is warranted with $T_A \leq + 105^\circ\text{C}$.

WARNING

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V _{CC} , AV _{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C _S	0.5	1.0 to 3.9	4.7	μF	1.0μF (Allowance within ± 50%) 3.9μF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V _{CC} must use the one of a capacity value that is larger than C _S .

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC Characteristics

14.3.1 Current Rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes ^{*1}	I _{CCPLL}	V _{CC}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz	-	27	-	mA	T _A = +25°C
			Flash 0 wait	-	-	37	mA	T _A = +105°C
			(CLKRC and CLKSC stopped)	-	-	38.5	mA	T _A = +125°C
	I _{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	-	3.5	-	mA	T _A = +25°C
			Flash 0 wait	-	-	8	mA	T _A = +105°C
			(CLKPLL, CLKSC and CLKRC stopped)	-	-	9.5	mA	T _A = +125°C
	I _{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz	-	1.8	-	mA	T _A = +25°C
			Flash 0 wait	-	-	6	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	7.5	mA	T _A = +125°C
	I _{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz	-	0.16	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3.5	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	5	mA	T _A = +125°C
	I _{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	-	0.1	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3.3	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKRC stopped)	-	-	4.8	mA	T _A = +125°C

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes*1	I _{CCSPLL}	V _{CC}	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	8.5	-	mA	T _A = +25°C
				-	-	14	mA	T _A = +105°C
				-	-	15.5	mA	T _A = +125°C
	I _{CCSMAN}		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	1	-	mA	T _A = +25°C
				-	-	4.5	mA	T _A = +105°C
				-	-	6	mA	T _A = +125°C
	I _{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.6	-	mA	T _A = +25°C
				-	-	3.8	mA	T _A = +105°C
				-	-	5.3	mA	T _A = +125°C
	I _{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.07	-	mA	T _A = +25°C
				-	-	2.8	mA	T _A = +105°C
				-	-	4.3	mA	T _A = +125°C
	I _{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T _A = +25°C
				-	-	2.5	mA	T _A = +105°C
				-	-	4	mA	T _A = +125°C

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes*2	I _{CCTPLL}	V _{CC}	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2250	μA	T _A = +25°C
				-	-	3220	μA	T _A = +105°C
				-	-	4025	μA	T _A = +125°C
	I _{CCTMAIN}		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	330	μA	T _A = +25°C
				-	-	1195	μA	T _A = +105°C
				-	-	2165	μA	T _A = +125°C
	I _{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	215	μA	T _A = +25°C
				-	-	1095	μA	T _A = +105°C
				-	-	2075	μA	T _A = +125°C
	I _{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	μA	T _A = +25°C
				-	-	905	μA	T _A = +105°C
				-	-	1880	μA	T _A = +125°C
	I _{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	μA	T _A = +25°C
				-	-	885	μA	T _A = +105°C
				-	-	1850	μA	T _A = +125°C

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode*3	I _{CCH}	V _{CC}	-	-	20	60	μA	T _A = +25°C
				-	-	880	μA	T _A = +105°C
				-	-	1845	μA	T _A = +125°C
Flash Power Down current	I _{CCFLASHPD}		-	-	36	70	μA	
Power supply current for active Low Voltage detector*4	I _{CCLVLD}		Low voltage detector enabled	-	5	-	μA	T _A = +25°C
				-	-	12.5	μA	T _A = +125°C
Flash Write/ Erase current*5	I _{CCFLASH}	-	-	12.5	-	mA	T _A = +25°C	
			-	-	20	mA	T _A = +125°C	

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32 kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, I_{CCFLASHPD} must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32 kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, I_{CCFLASHPD} must be added to the Power supply current.

*4: When low voltage detector is enabled, I_{CCLVLD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, I_{CCFLASH} must be added to Power supply current.

14.3.2 Pin Characteristics
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C)$

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V _{IH}	Port inputs Pnn_m	-	V _{CC} × 0.7	-	V _{CC} + 0.3	V	CMOS Hysteresis input
			-	V _{CC} × 0.8	-	V _{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V _{IHX0S}	X0	External clock in "Fast Clock Input mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V _{IHX0AS}	X0A	External clock in "Oscillation mode"	V _{CC} × 0.8	-	V _{CC} + 0.3	V	
	V _{IHR}	RSTX	-	V _{CC} × 0.8	-	V _{CC} + 0.3	V	CMOS Hysteresis input
	V _{IHM}	MD	-	V _{CC} - 0.3	-	V _{CC} + 0.3	V	CMOS Hysteresis input
	V _{IHD}	DEBUG I/F	-	2.0	-	V _{CC} + 0.3	V	TTL Input
"L" level input voltage	V _{IL}	Port inputs Pnn_m	-	V _{SS} - 0.3	-	V _{CC} × 0.3	V	CMOS Hysteresis input
			-	V _{SS} - 0.3	-	V _{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V _{ILX0S}	X0	External clock in "Fast Clock Input mode"	V _{SS}	-	VD × 0.2	V	VD=1.8V±0.15V
	V _{ILX0AS}	X0A	External clock in "Oscillation mode"	V _{SS} - 0.3	-	V _{CC} × 0.2	V	
	V _{ILR}	RSTX	-	V _{SS} - 0.3	-	V _{CC} × 0.2	V	CMOS Hysteresis input
	V _{ILM}	MD	-	V _{SS} - 0.3	-	V _{SS} + 0.3	V	CMOS Hysteresis input
	V _{ILD}	DEBUG I/F	-	V _{SS} - 0.3	-	0.8	V	TTL Input

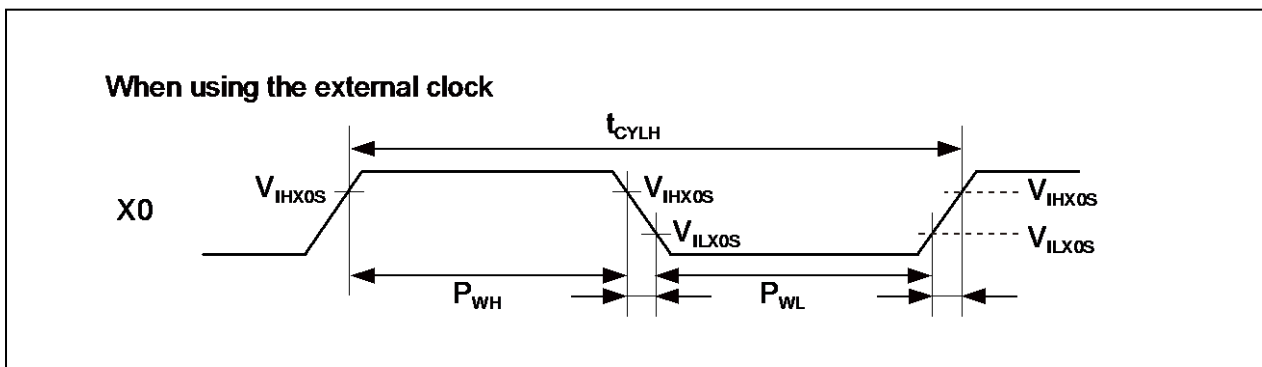
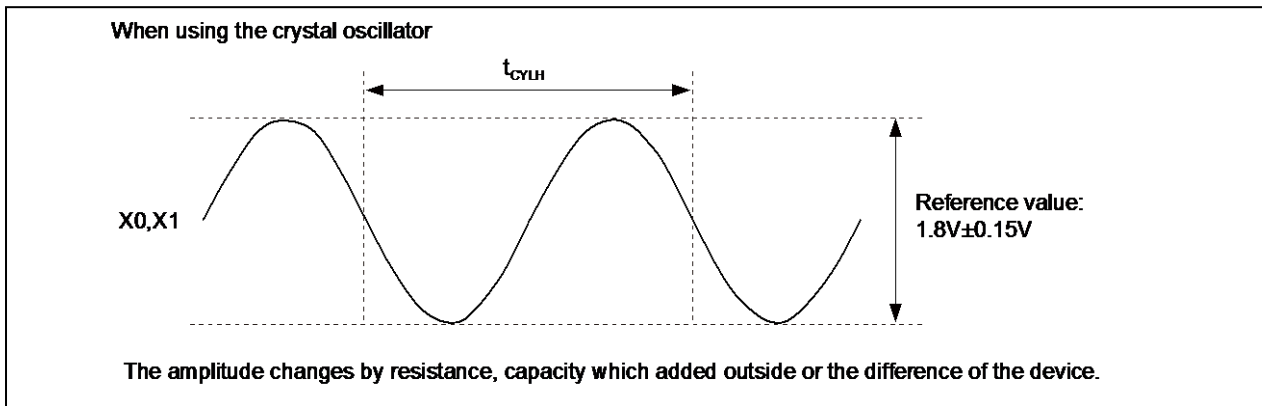
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V _{OH4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -4mA 2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA	V _{CC} - 0.5	-	V _{CC}	V	
	V _{OH3}	3mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -3mA 2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA	V _{CC} - 0.5	-	V _{CC}	V	
"L" level output voltage	V _{OL4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OL} = +4mA 2.7V ≤ V _{CC} < 4.5V I _{OL} = +1.7mA	-	-	0.4	V	
	V _{OL3}	3mA type	2.7V ≤ V _{CC} < 5.5V I _{OL} = +3mA	-	-	0.4	V	
	V _{OLD}	DEBUG I/F	V _{CC} = 2.7V I _{OL} = +25mA	0	-	0.25	V	
Input leak current	I _{IL}	Pnn_m	V _{SS} < V _I < V _{CC} AV _{SS} , AV _{RL} < V _I < AV _{CC} , AV _{RH}	- 1	-	+ 1	μA	
Pull-up resistance value	R _{PU}	Pnn_m	V _{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C _{IN}	Other than C, V _{CC} , V _{SS} , AV _{CC} , AV _{SS} , AV _{RH} , AV _{RL}	-	-	5	15	pF	

14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$)

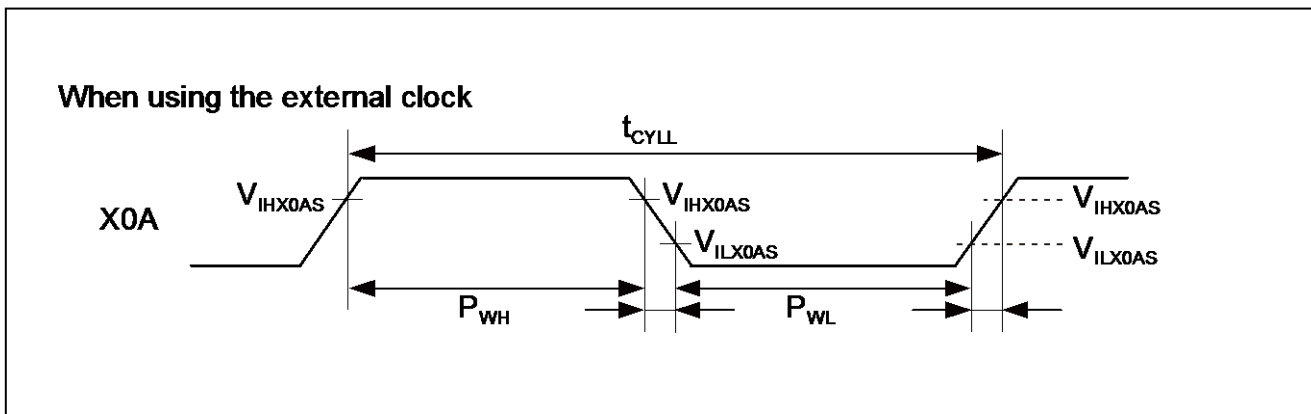
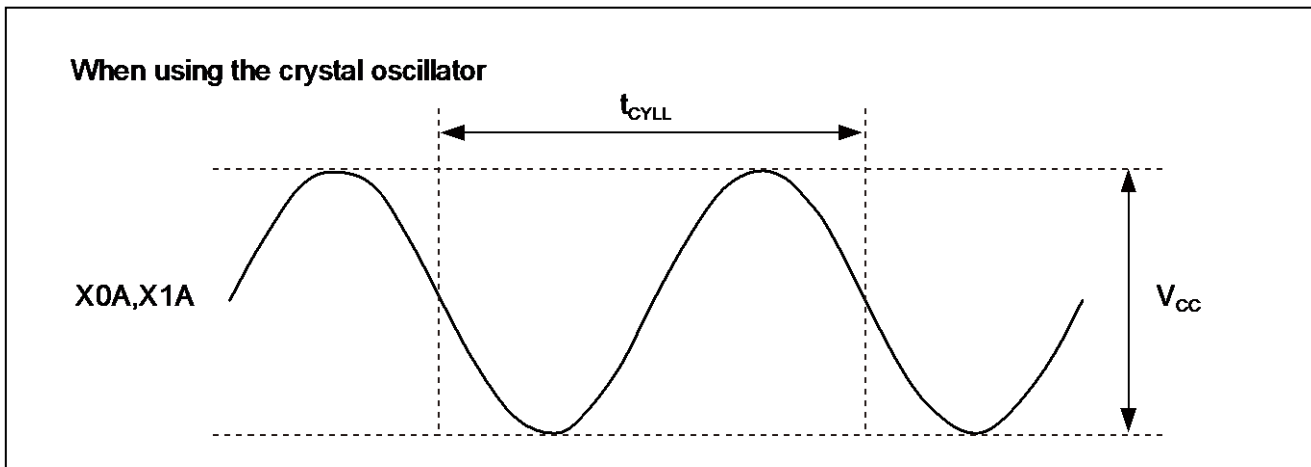
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f _c	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f _{FCI}	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	t _{CYLIH}	-	125	-	-	ns	
Input clock pulse width	P _{WH} , P _{WL}	-	55	-	-	ns	



14.4.2 Sub Clock Input Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100		kHz
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	μs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL} , P_{WL}/t_{CYLL}	30	-	70	%	



14.4.3 Built-in RC Oscillation Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4		MHz
RC clock stabilization time	t_{RCSTAB}	80	160	320	μs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	μs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 Internal Clock Timing

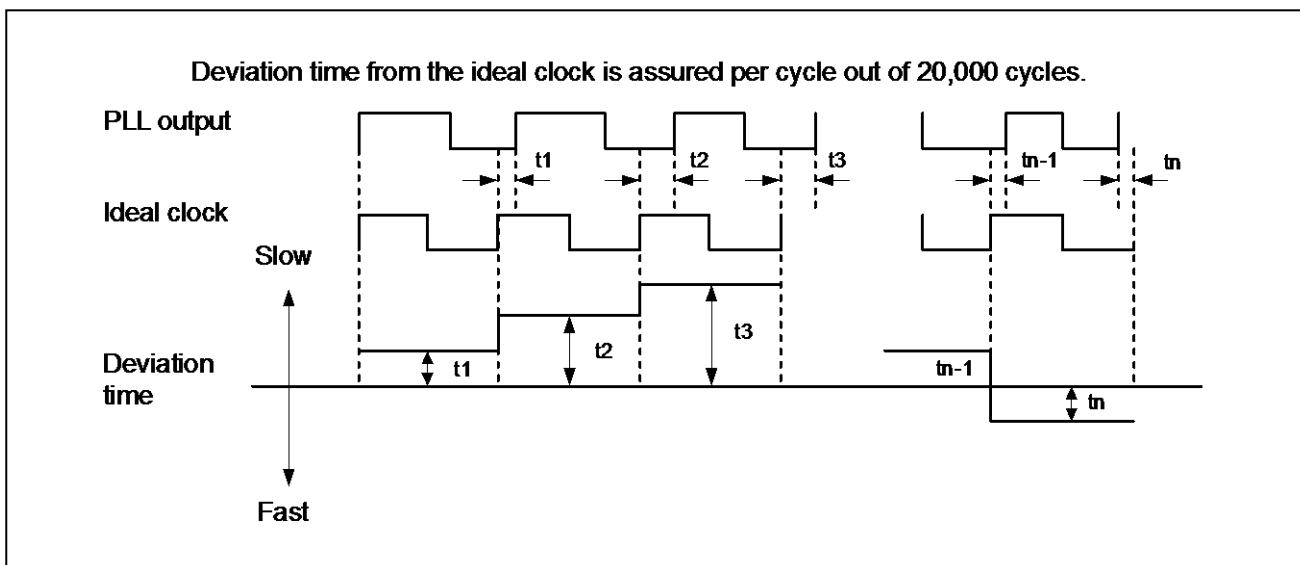
($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.5 Operating Conditions of PLL

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

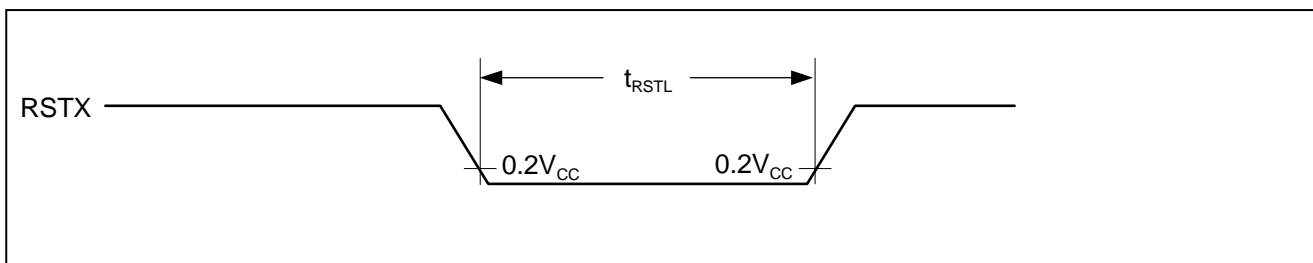
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) $\geq 4MHz$



14.4.6 Reset Input

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

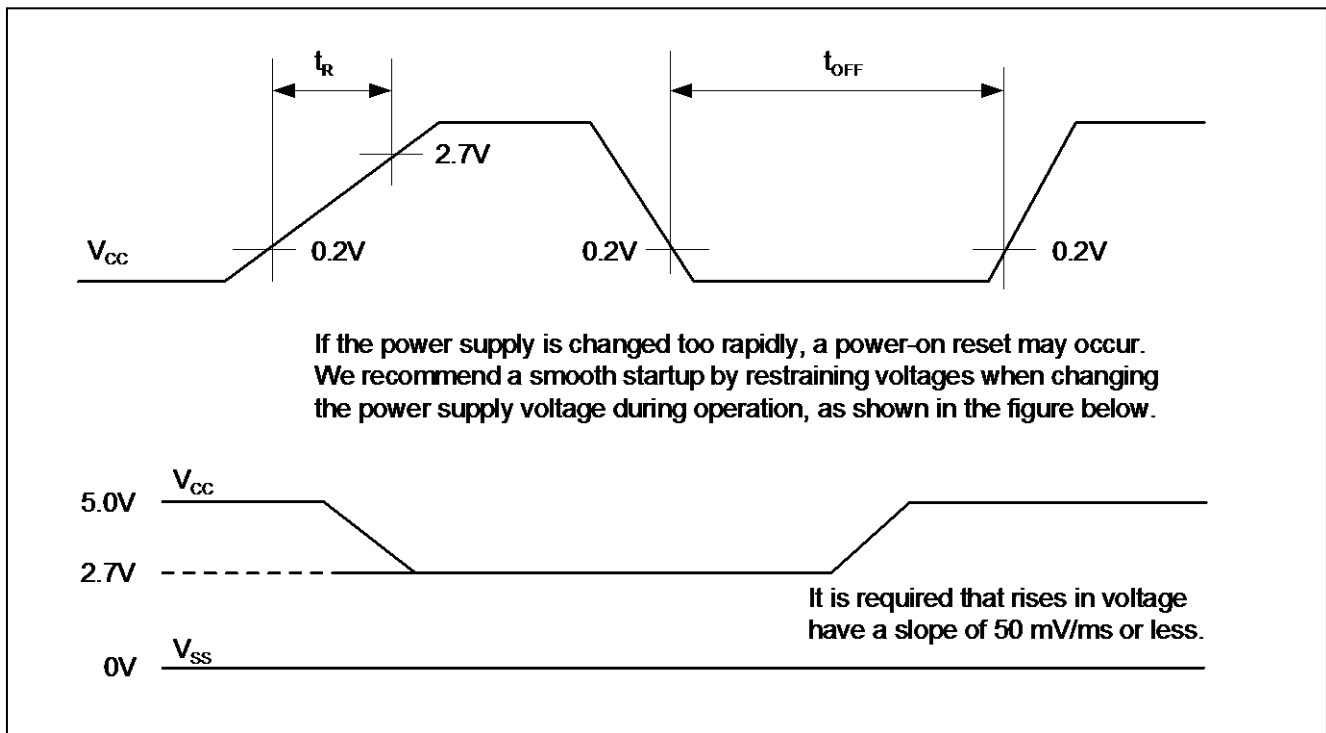
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	μs
Rejection of reset input time			1	-	μs



14.4.7 Power-on Reset Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms



14.4.8 USART Timing
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C, C_L=50pF)$

Parameter	Symbol	Pin Name	Conditions	4.5V ≤ V _{CC} < 5.5V		2.7V ≤ V _{CC} < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKn	Internal shift clock mode	4t _{CLKP1}	-	4t _{CLKP1}	-	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t _{OVSHI}	SCKn, SOTn		N × t _{LKP1} - 20*	-	N × t _{CLKP1} - 30*	-	ns
SIN → SCK ↑ setup time	t _{IVSHI}	SCKn, SINn		t _{CLKP1} + 45	-	t _{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	t _{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCKn	External shift clock mode	t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
Serial clock "H" pulse width	t _{SHSL}	SCKn		t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCKn, SOTn		-	2t _{CLKP1} + 45	-	2t _{CLKP1} + 55	ns
SIN → SCK ↑ setup time	t _{IVSHE}	SCKn, SINn		t _{CLKP1} /2 + 10	-	t _{CLKP1} /2 + 10	-	ns
SCK ↑ → SIN hold time	t _{SHIXE}	SCKn, SINn		t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
SCK fall time	t _F	SCKn		-	20	-	20	ns
SCK rise time	t _R	SCKn	-	20	-	20	ns	

Notes:

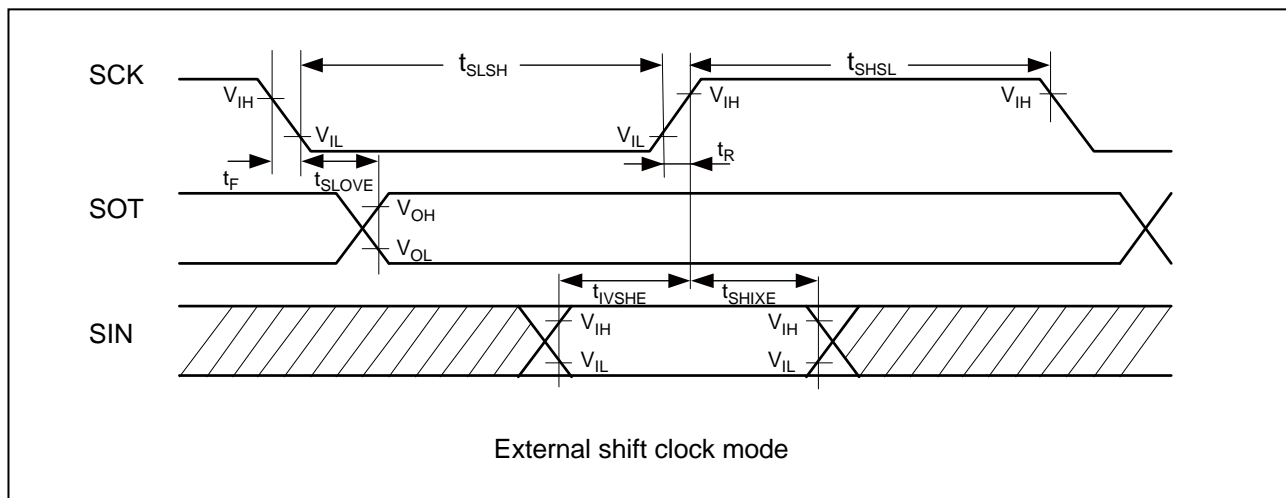
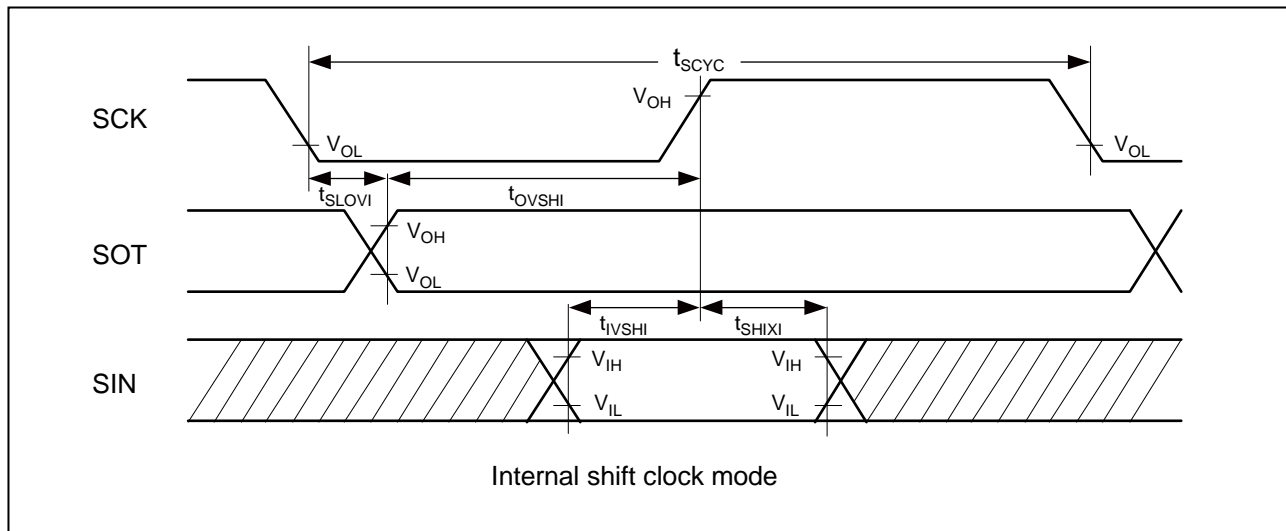
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "CY96600 series HARDWARE MANUAL".
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number. For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

- If t_{SCYC} = 2 × k × t_{CLKP1}, then N = k, where k is an integer > 2
- If t_{SCYC} = (2 × k + 1) × t_{CLKP1}, then N = k + 1, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}, 6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}, 8 \times t_{CLKP1}$	4
...	...

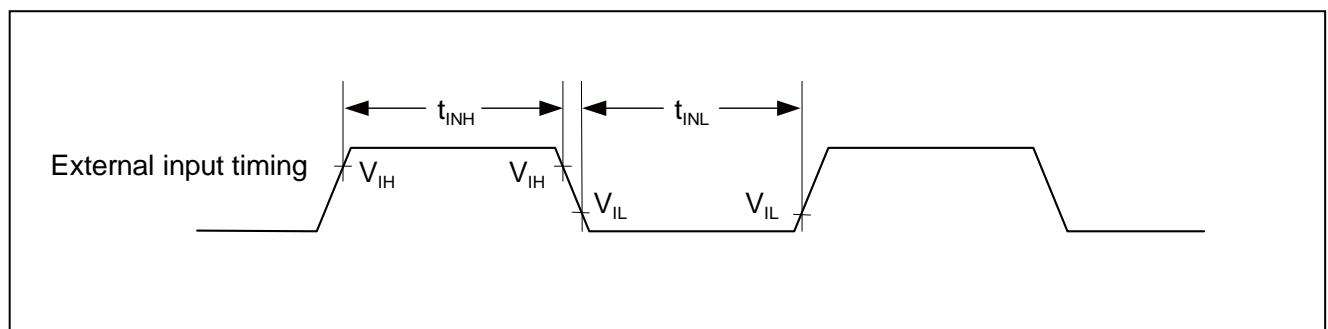


14.4.9 External Input Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH} , t_{INL}	Pnn_m	$2t_{CLKP1} + 200$ ($t_{CLKP1} = 1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG				A/D Converter trigger input
		TINn				Reload Timer
		TTGn				PPG trigger input
		FRCKn, FRCKn_R				Free-Running Timer input clock
		INn, INn_R				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R				External Interrupt
		NMI	Non-Maskable Interrupt			
				200	-	ns

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.4.10 I²C Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Typical Mode		High-Speed Mode ^{*4}		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	C _L = 50pF, R = (V _p /I _{OL}) ^{*1}	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t _{HDSTA}		4.0	-	0.6	-	μs
SCL clock "L" width	t _{LOW}		4.7	-	1.3	-	μs
SCL clock "H" width	t _{HIGH}		4.0	-	0.6	-	μs
(Repeated) START condition setup time SCL ↑ → SDA ↓	t _{SUSTA}		4.7	-	0.6	-	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45 ^{*2}	0	0.9 ^{*3}	μs
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	t _{SUSTO}		4.0	-	0.6	-	μs
Bus free time between "STOP condition" and "START condition"	t _{BUS}		4.7	-	1.3	-	μs
Pulse width of spikes which will be suppressed by input noise filter	t _{SP}	-	0	(1-1.5) × t _{CLKP1} ^{*5}	0	(1-1.5) × t _{CLKP1} ^{*5}	ns

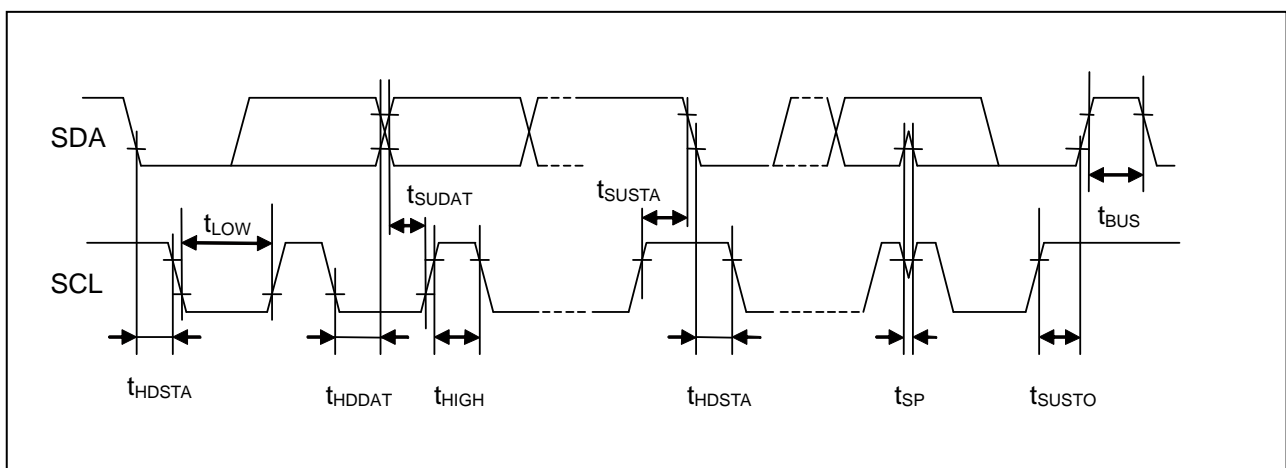
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

*4: For use at over 100 kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

*5: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.



14.5 A/D Converter
14.5.1 Electrical Characteristics for the A/D Converter
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C)$

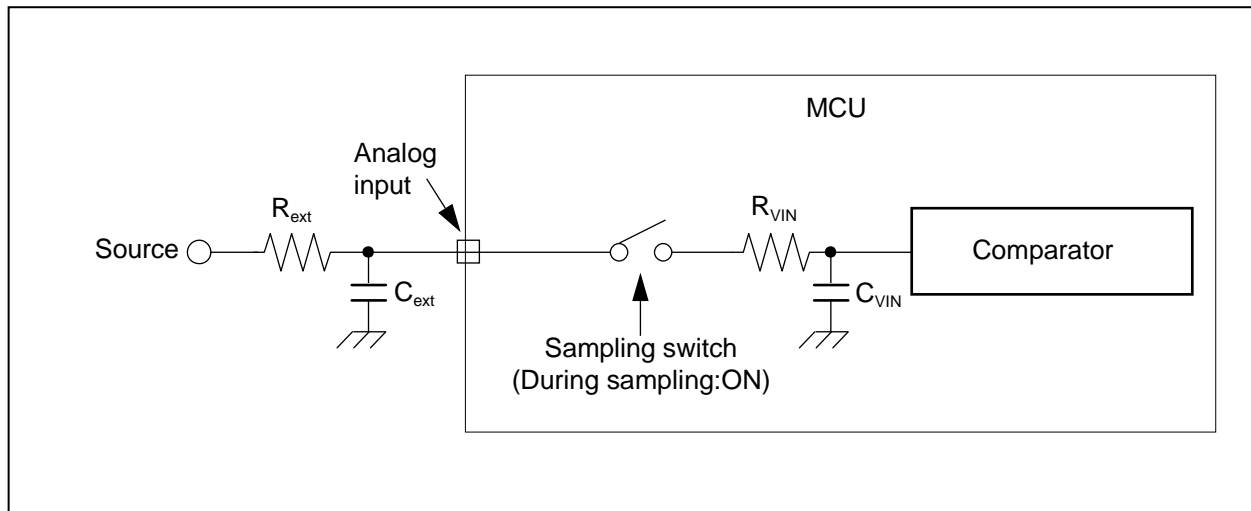
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V _{OT}	ANn	Typ - 20	AVRL + 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V _{FST}	ANn	Typ - 20	AVRH - 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	μs	4.5V ≤ AV _{CC} ≤ 5.5V
			2.2	-	8.0	μs	2.7V ≤ AV _{CC} < 4.5V
Sampling time*	-	-	0.5	-	-	μs	4.5V ≤ AV _{CC} ≤ 5.5V
			1.2	-	-	μs	2.7V ≤ AV _{CC} < 4.5V
Power supply current	I _A	AV _{CC}	-	2.0	3.1	mA	A/D Converter active
	I _{AH}		-	-	3.3	μA	A/D Converter not operated
Reference power supply current (between AVRH and AVRL)	I _R	AVRH	-	520	810	μA	A/D Converter active
	I _{RH}		-	-	1.0	μA	A/D Converter not operated
Analog input capacity	C _{VIN}	ANn	-	-	15.9	pF	
Analog impedance	R _{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV _{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV _{CC} < 4.5V
Analog port input current (during conversion)	I _{AIN}	ANn	- 0.3	-	+ 0.3	μA	AV _{SS} , AVRL < V _{AIN} < AV _{CC} , AVRH
Analog input voltage	V _{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	-	AVRH	AV _{CC} - 0.1	-	AV _{CC}	V	
	-	AVRL	AV _{SS}	-	AV _{SS} + 0.1	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

14.5.2 Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (T_{samp}) depends on the external driving impedance R_{ext} , the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext} : External driving impedance

C_{ext} : Capacitance of PCB at A/D converter input

C_{VIN} : Analog input capacity (I/O, analog switch and ADC are contained)

R_{VIN} : Analog input impedance (I/O, analog switch and ADC are contained)

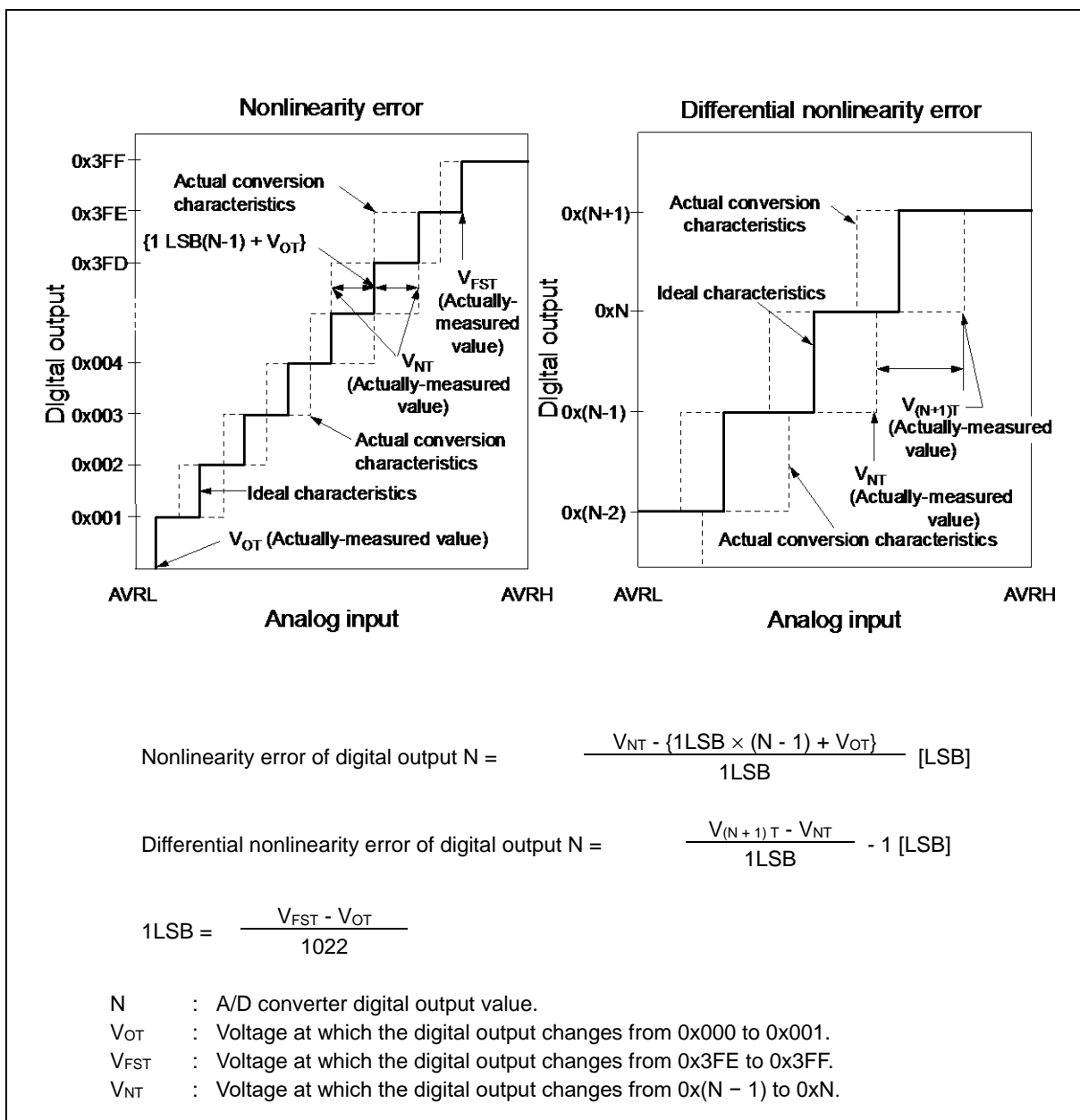
The following approximation formula for the replacement model above can be used:

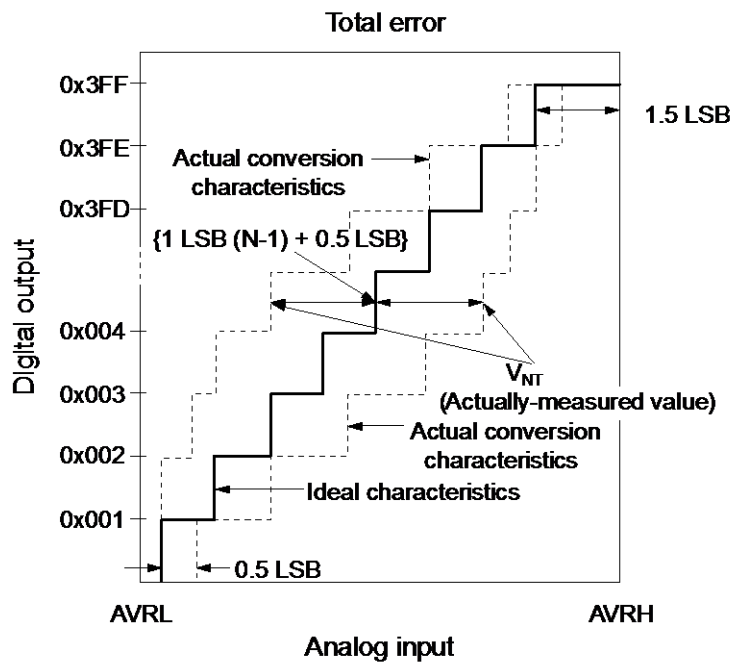
$$T_{\text{samp}} = 7.62 \times (R_{\text{ext}} \times C_{\text{ext}} + (R_{\text{ext}} + R_{\text{VIN}}) \times C_{\text{VIN}})$$

- Do not select a sampling time below the absolute minimum permitted value.
($0.5\mu\text{s}$ for $4.5\text{V} \leq AV_{\text{CC}} \leq 5.5\text{V}$, $1.2\mu\text{s}$ for $2.7\text{V} \leq AV_{\text{CC}} < 4.5\text{V}$)
- If the sampling time cannot be sufficient, connect a capacitor of about $0.1\mu\text{F}$ to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AV_{\text{RH}} - AV_{\text{RL}}|$ becomes smaller.

14.5.3 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111).
- Differential nonlinearity error: Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage : Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.





$$1\text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{\text{NT}} - \{1\text{LSB} \times (\text{N} - 1) + 0.5\text{LSB}\}}{1\text{LSB}}$$

N : A/D converter digital output value.

V_{NT} : Voltage at which the digital output changes from 0x(N+1) to 0xN.

V_{OT} (Ideal value) = AVRL + 0.5LSB[V]

V_{FST} (Ideal value) = AVRH - 1.5LSB[V]

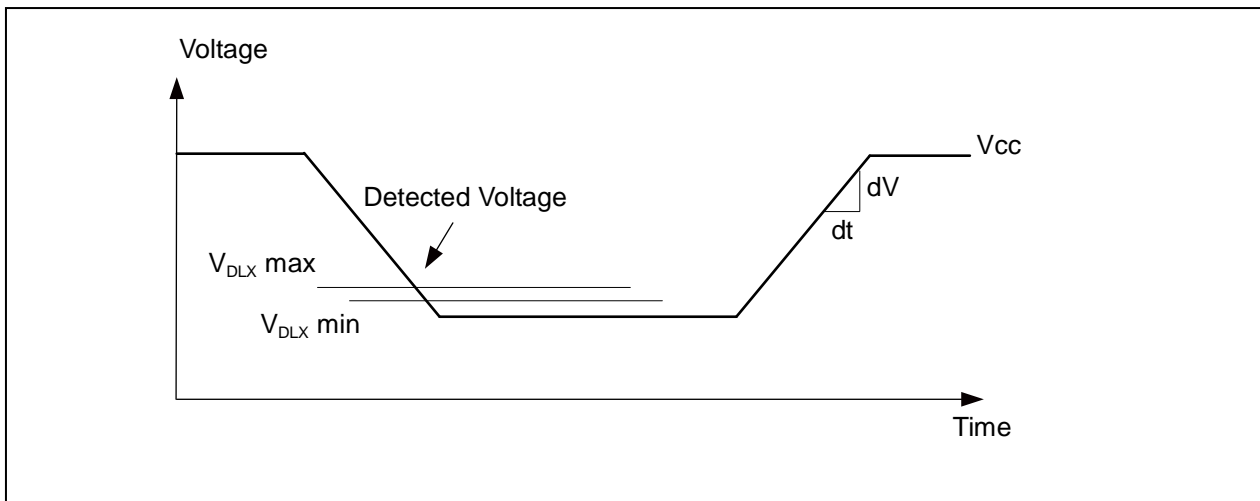
14.6 Low Voltage Detection Function Characteristics

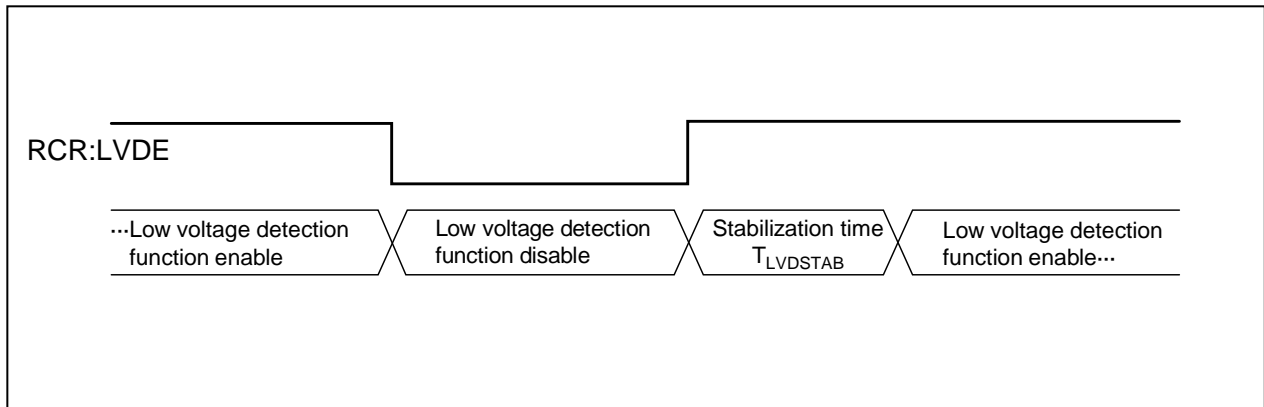
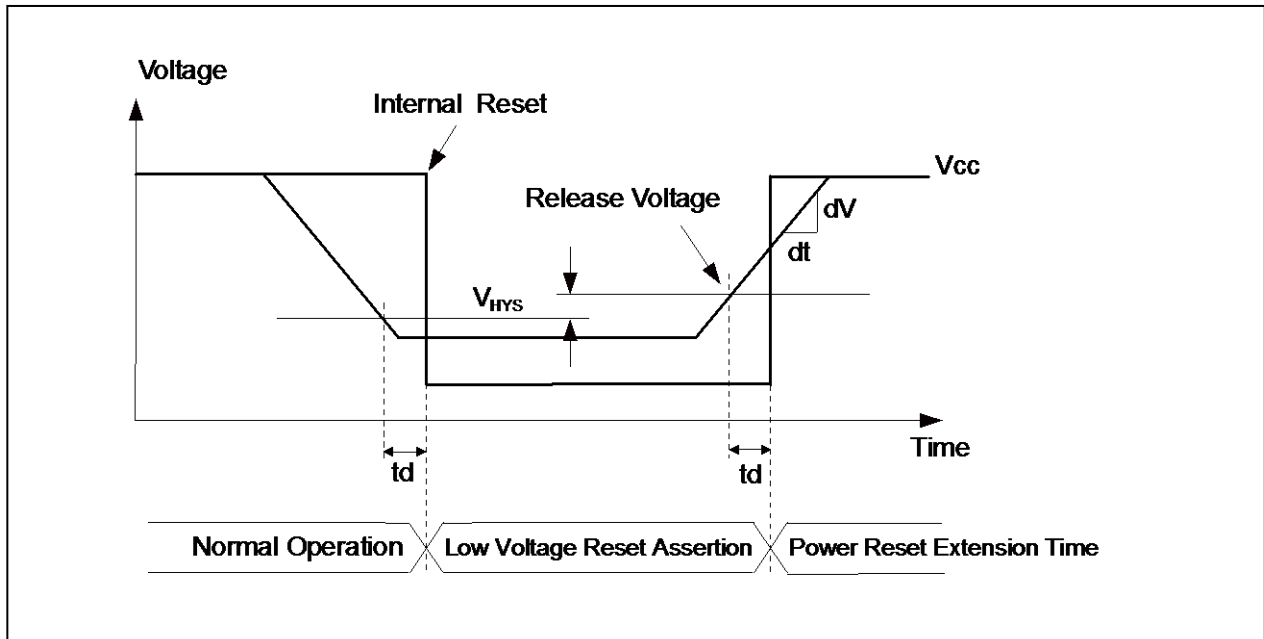
($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage*1	V_{DL0}	CILCR:LVL = 0000 _B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001 _B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010 _B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011 _B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100 _B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111 _B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001 _B	3.91	4.20	4.49	V
Power supply voltage change rate*2	dV/dt	-	- 0.004	-	+ 0.004	V/ μ s
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	75	μ s	
Detection delay time	t_d	-	-	30	μ s	

*1: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.





14.7 Flash Memory Write/Erase Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq +105^{\circ}C$	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq +105^{\circ}C$	-	25	400	μs	Not including system-level overhead time.
	Small Sector	-	-	25	400	μs	
Chip erase time		$T_A \leq +105^{\circ}C$	-	11.51	55.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage ($-0.004V/\mu s$ to $+0.004V/\mu s$) after the external power falls below the detection voltage (V_{DLX})^{*1}.

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20^{*2}
10,000	10^{*2}
100,000	5^{*2}

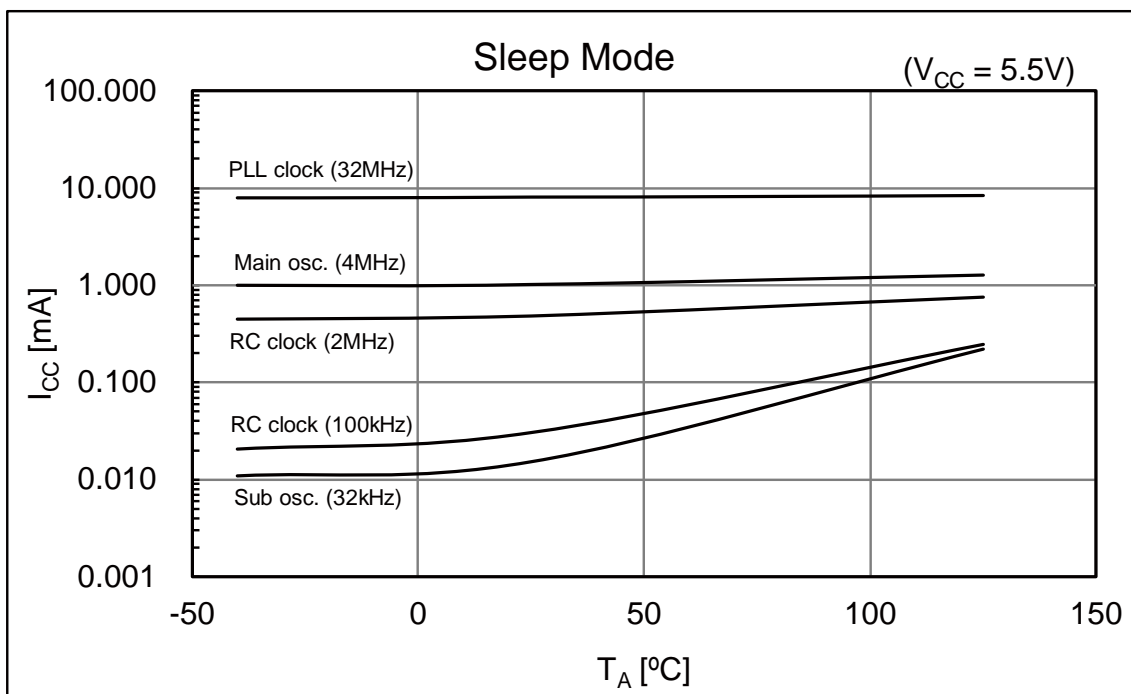
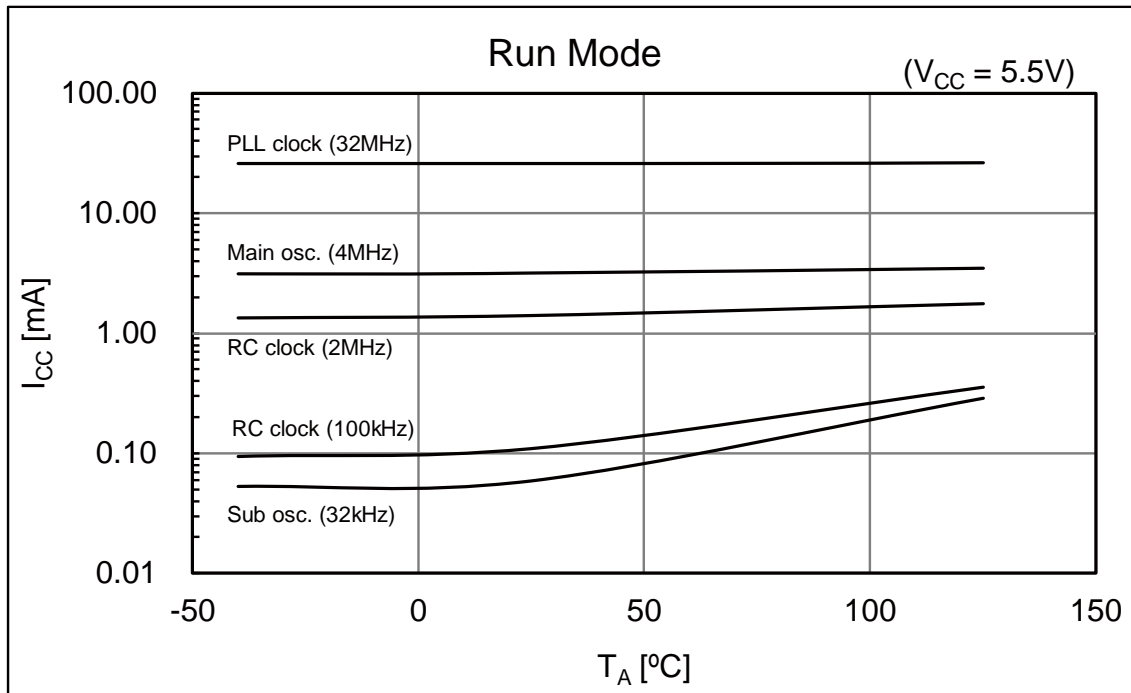
*1: See "14.6 Low Voltage Detection Function Characteristics".

*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^{\circ}C$).

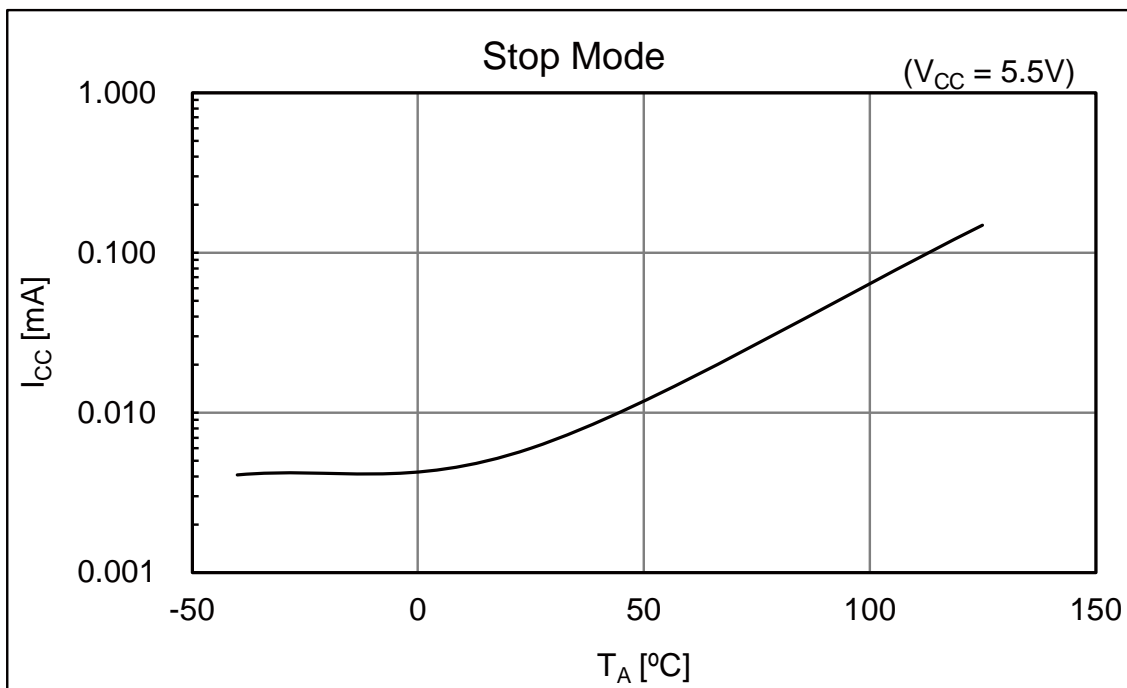
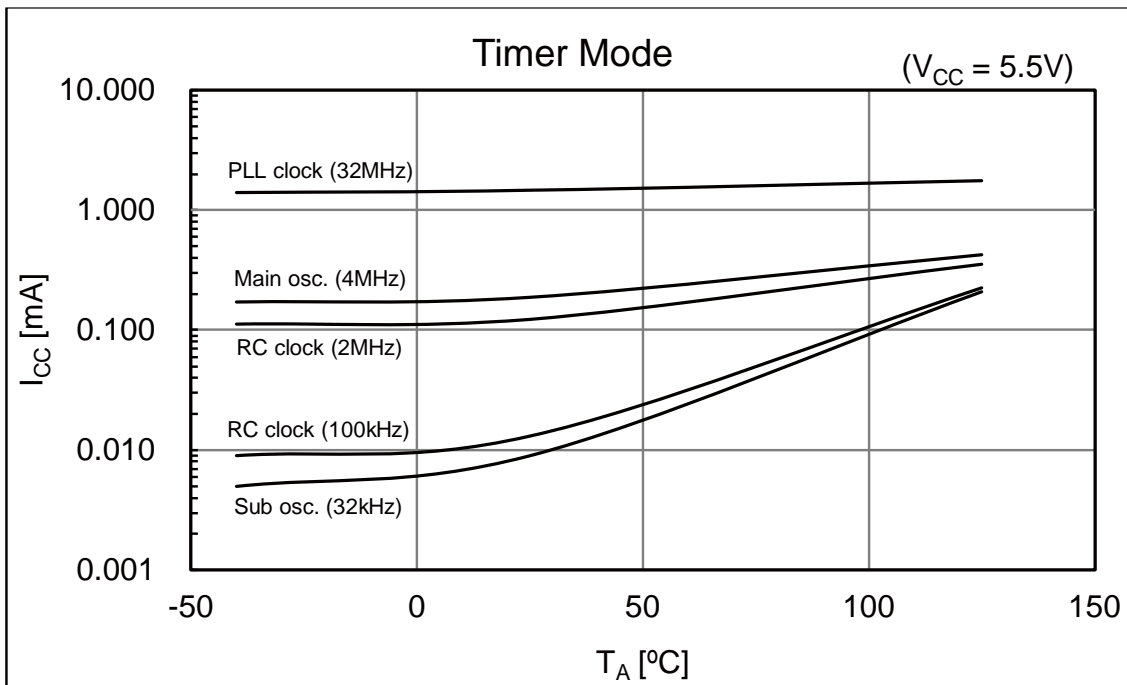
15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■ CY96F647



■ CY96F647



■ Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

16. Ordering Information

MCU with CAN Controller

Part Number	Flash Memory	Package*
CY96F643RBPMC-GS-UJE1	Flash A (96.5KB)	100-pin plastic LQFP (LQI100)
CY96F646RBPMC-GS-UJE1	Flash A (288.5KB)	100-pin plastic LQFP (LQI100)
CY96F646RBPMC-GS-UJE2		
CY96F647RBPMC-GS-UJE1	Flash A (416.5KB)	100-pin plastic LQFP (LQI100)
CY96F647RBPMC-GS-UJE2		

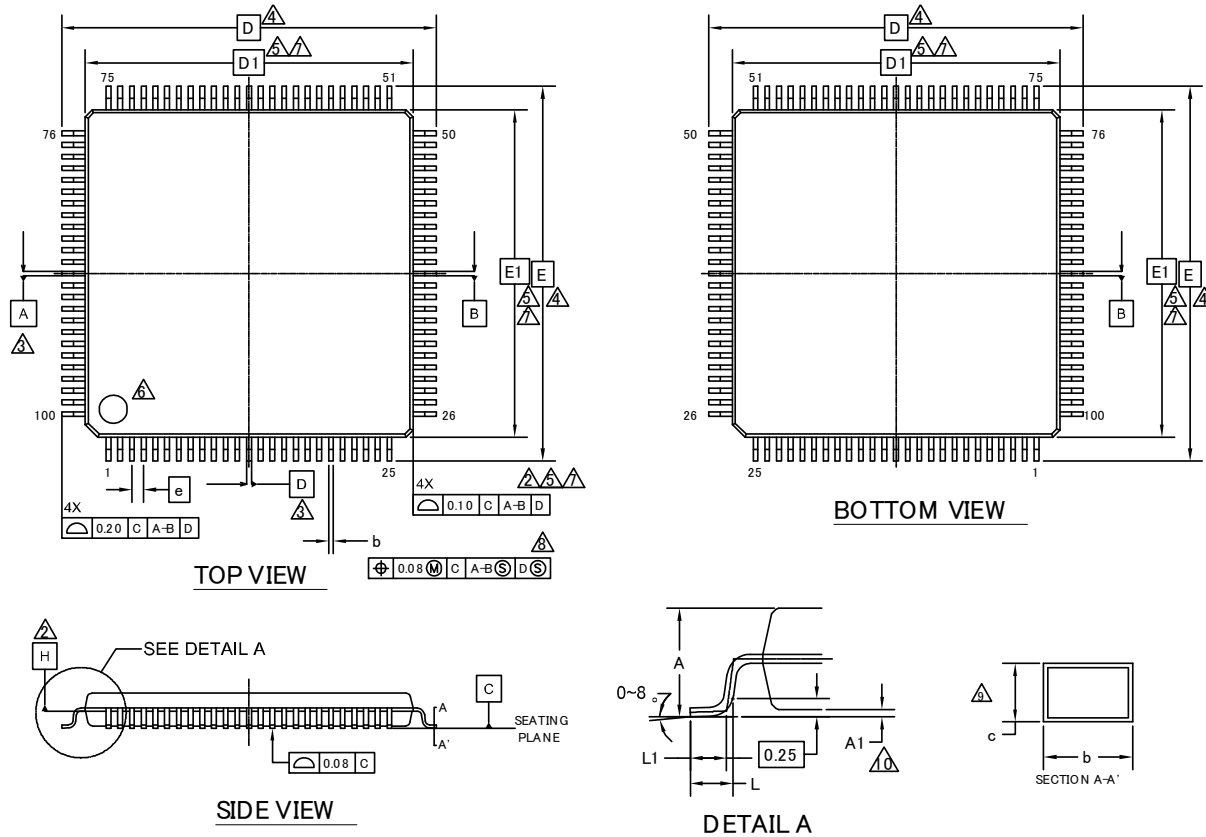
*: For details about package, see "Package Dimension".

MCU without CAN Controller

Part Number	Flash Memory	Package*
CY96F643ABPMC-GS-UJE1	Flash A (96.5KB)	100-pin plastic LQFP (LQI100)
CY96F645ABPMC-GS-UJE2	Flash A (160.5KB)	100-pin plastic LQFP (LQI100)

*: For details about package, see "Package Dimension".

17. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11500 *A

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQ1100, REV*A

18. Major Changes

Spancion Publication Number: MB96640_DS704-00009

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
4	Features	Changed the description of "External Interrupts" Interrupt mask and pending bit per channel → Interrupt mask bit per channel
26 to 29	Handling Precautions	Added a section
37	Electrical Characteristics 3. DC Characteristics (1) Current Rating	Changed the Conditions for I_{CCSRCH} $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz,$ → $CLKS1/2 = CLKP1/2 = CLKRC = 2MHz,$
		Changed the Conditions for I_{CCSRCL} $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz$ → $CLKS1/2 = CLKP1/2 = CLKRC = 100kHz$
38		Changed the Conditions for I_{CCTPLL} PLL Timer mode with $CLKP1 = 32MHz$ → PLL Timer mode with $CLKPLL = 32MHz$
		Changed the Value of "Power supply current in Timer modes" I_{CCTPLL} Typ: $2485\mu A \rightarrow 1800\mu A$ ($T_A = +25^\circ C$) Max: $2715\mu A \rightarrow 2250\mu A$ ($T_A = +25^\circ C$) Max: $4095\mu A \rightarrow 3220\mu A$ ($T_A = +105^\circ C$) Max: $5065\mu A \rightarrow 4025\mu A$ ($T_A = +125^\circ C$)
		Changed the Conditions for I_{CCTRCL} RC Timer mode with $CLKRC = 100kHz,$ $SMCR:LPMSS = 0$ ($CLKPLL, CLKMC$ and $CLKSC$ stopped) → RC Timer mode with $CLKRC = 100kHz$ ($CLKPLL, CLKMC$ and $CLKSC$ stopped)
39		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. → The current for "On Chip Debugger" part is not included.
50	4. AC Characteristics (10) I ² C timing	Added parameter, "Noise filter" and an annotation *5 for it Added t_{SP} to the figure
52	5. A/D Converter (2) Accuracy and Setting of the A/D Converter Sampling Time	Deleted the unit "[Min]" from approximation formula of Sampling time
57	7. Flash Memory Write/Erase Characteristics	Changed the condition ($V_{CC} = AV_{CC} = 2.7V$ to $5.5V, V_D = 1.8V \pm 0.15V, V_{SS} = AV_{SS} = 0V, T_A = -40^\circ C$ to $+125^\circ C$) → ($V_{CC} = AV_{CC} = 2.7V$ to $5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^\circ C$ to $+125^\circ C$)

Page	Section	Change Results
57	Electrical Characteristics 7. Flash Memory Write/Erase Characteristics	<p>Changed the Note</p> <p>While the Flash memory is written or erased, shutdown of the external power (VCC) is prohibited. In the application system where the external power (VCC) might be shut down while writing, be sure to turn the power off by using an external voltage detector.</p> <p>→</p> <p>While the Flash memory is written or erased, shutdown of the external power (VCC) is prohibited. In the application system where the external power (VCC) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.</p>
Revision 2.1		
-	-	Company name and layout design change

NOTE: Please see “Document History” about later revised information.

Page	Section	Change Results
Rev. *B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
5, 7, 60, 61	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-100P-M20 → LQ1100
60	16. Ordering Information	<p>Revised Marketing Part Numbers as follows:</p> <p>Before)</p> <p>MCU with CAN controller</p> <p>MB96F643RBPMC-GSE1 MB96F643RBPMC-GSE2 MB96F645RBPMC-GSE1 MB96F645RBPMC-GSE2 MB96F646RBPMC-GSE1 MB96F646RBPMC-GSE2 MB96F647RBPMC-GSE1 MB96F647RBPMC-GSE2</p> <p>MCU without CAN controller</p> <p>MB96F643ABPMC-GSE1 MB96F643ABPMC-GSE2 MB96F645ABPMC-GSE1 MB96F645ABPMC-GSE2</p> <p>After)</p> <p>MCU with CAN controller</p> <p>CY96F643RBPMC-GS-UJE1 CY96F646RBPMC-GS-UJE1 CY96F646RBPMC-GS-UJE2 CY96F647RBPMC-GS-UJE1 CY96F647RBPMC-GS-UJE2</p> <p>MCU without CAN controller</p> <p>CY96F643ABPMC-GS-UJE1 CY96F645ABPMC-GS-UJE2</p>

Document History

Document Title: CY96640 Series, F²MC-16FX 16-Bit Microcontroller

Document Number: 002-04713

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04713. No change to document contents or format.
*A	5149634	KSUN	02/25/2016	Updated to Cypress template.
*B	6033802	MIYH	01/16/2018	Updated Document Title to read as "CY96640 Series, F ² MC-16FX 16-Bit Microcontroller". Replaced MB96640 Series with CY96640 Series in all instances across the document. Changed the prefix of all MPNs from MB to CY in all instances across the document. Updated Ordering Information. For details, please see 18. Major Changes.
*C	6600034	KSUN	06/20/2019	Updated to new template.

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