The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

MB91F467RC

FR60, MB91460R Series, 32-bit Microcontroller Datasheet

MB91460R series is a line of the general-purpose 32-bit RISC microcontrollers designed for embedded control applications such as consumer devices and vehicle system, which require high-speed real-time processing. MB91460R series uses the FR60 CPU compatible with the FR family CPUs.

MB91460R series contains the LIN-USART and CAN controller.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- Maximum operating frequency: 80 MHz (oscillation frequency 4 MHz, 20 multiplier (PLL clock multiplication method))
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation instructions, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi load store instructions: Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving): 6 cycles (16 priority levels)
- Harvard architecture enabling simultaneous execution of both program access and data access
- Instructions compatible with the FR family

Internal Peripheral Resources

- Flash memory capacity: 1088 Kbytes
- Internal RAM capacity: 0 Wait access 16 Kbytes + 1 Wait access 32 Kbytes + 16 Kbytes
  (Instruction/data common RAM)
- General-purpose port: Maximum 138 ports
- DMAC (DMA Controller)

Maximum of 5 channels for simultaneous operation is possible. (1 channel for external-to-external)

3 transfer sources (external pin/internal peripheral/software)

Activation source can be selected using software.

Addressing mode with 32-bit full address indication (increment/decrement/fixed)

Transfer mode (demand transfer/burst transfer/step transfer/block transfer)

Fly-by transfer support (between external I/O and memory)

Transfer data size selection 8/16/32-bit

Multi-byte transfer enabled (by software)

DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)

- A/D converter (sequential comparison)

10-bit resolution: 16 channels

Conversion time: 3 µs (peripheral macro operation clock at 16.67 MHz)

- External interrupt input: 16 channels

Pins shared with RX pins of CAN0 and CAN1

- Bit search module (for REALOS)

Function of searching for the first “0” data/ “1” data/change bit position in 1 word from the MSB (upper bit)

- LIN-USART (full duplex double buffer): 7 channels

Clock synchronous/asynchronous selectable

Sync-break detection

Internal dedicated baud rate generator

- I^2C bus interface (400 kbps supported): 3 channels

Master/slave sending and receiving

Arbitration function, clock synchronization function

- CAN controller (C-CAN): 2 channels

Maximum transfer speed: 1 Mbps

32 sent/received message buffers

- 16-bit PPG timer: 8 channels
- 16-bit reload timer: 5 channels
- 16-bit free-run timer: 4 channels (1 channel each for ICU and OCU)
- Input capture: 4 channels (work with free-run timer)
- Output compare: 4 channels (work with free-run timer)
- Watchdog timer

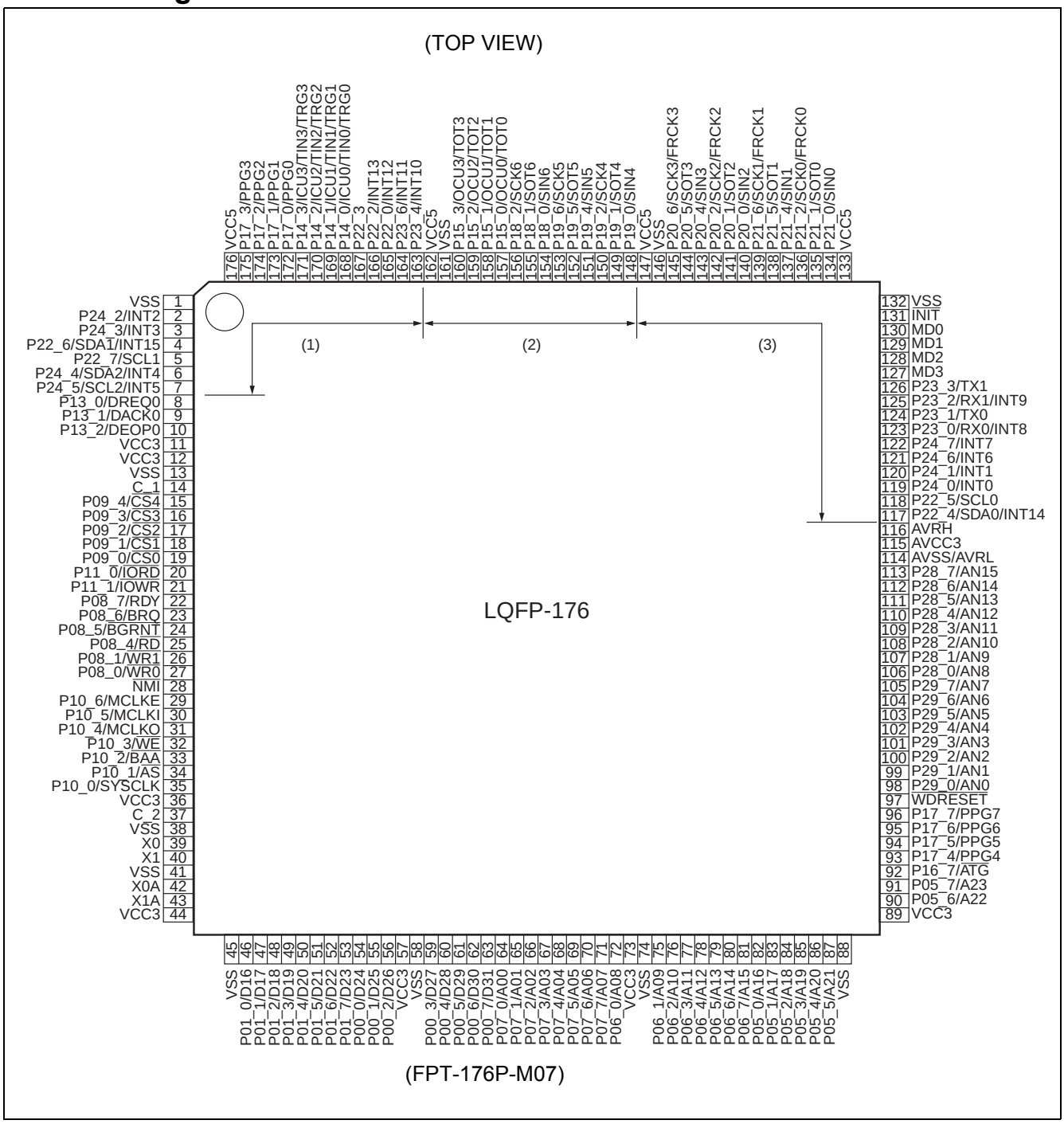
Watchdog reset output pin available

- Real-time clock
- Low-power consumption mode: Sleep/stop/shutdown mode function
- Clock modulator

- Sub clock calibration
- Main oscillation stabilization wait timer
- Sub oscillation stabilization wait timer
- Package: LQFP-176 (FPT-176P-M07)
- CMOS 0.18 μm technology
- 3 V/5 V power supplies [Internal logic is kept at 1.8 V by step-down circuit, some I/Os have the withstand voltage of 5.0 V]
- Operating temperature range: between − 40°C and + 85°C

Contents

1. Pin Assignment



Note:

(1) to (3) are 3.3 V/5 V pin supported pin, and can set 3.3 V and 5 V to the voltage in each block. I^2C pin in (1) can be inputted at 5 V power supply. However, 3.3 V of the input threshold value is used as the standard value regardless of the power supply voltage. If 5 V is set in (1) or (2), also set 5 V to (3).

2. Pin Description

Pin no.	Pin name	I/O	I/O circuit type[1]	Description
2	P24_2	I/O	D	General-purpose input/output port
	INT2			External interrupt input pin
3	P24_3	I/O	D	General-purpose input/output port
	INT3			External interrupt input pin
4	P22_6	I/O Open Drain	C	General-purpose input/output port
	SDA1			I^2C bus DATA input/output pin
	INT15			External interrupt input pin
5	P22_7	I/O Open Drain	C	General-purpose input/output port
	SCL1			I^2C bus Clock input/output pin
6	P24_4	I/O Open Drain	C	General-purpose input/output port
	SDA2			I^2C bus DATA input/output pin
	INT4			External interrupt input pin
7	P24_5	I/O Open Drain	C	General-purpose input/output port
	SCL2			I^2C bus Clock input/output pin
	INT5			External interrupt input pin
8	P13_0	I/O	H	General-purpose input/output port
	DREQ0			DMA external transfer request input pin
9	P13_1	I/O	H	General-purpose input/output port
	DACK0			DMA external transfer acknowledgement output pin
10	P13_2	I/O	H	General-purpose input/output port
	DEOP0			DMA external transfer EOP (End of Process) output pin
15	P09_4	I/O	H	General-purpose input/output port
	$\overline{CS4}$			Chip select 4 output pin
16	P09_3	I/O	H	General-purpose input/output port
	$\overline{CS3}$			Chip select 3 output pin
17	P09_2	I/O	H	General-purpose input/output port
	$\overline{CS2}$			Chip select 2 output pin
18	P09_1	I/O	H	General-purpose input/output port
	$\overline{CS1}$			Chip select 1 output pin
19	P09_0	I/O	H	General-purpose input/output port
	$\overline{CS0}$			Chip select 0 output pin
20	P11_0	I/O	H	General-purpose input/output port
	$\overline{IORD}$			Read strobe output pin at DMA flyby transfer

Pin no.	Pin name	I/O	I/O circuit type[1]	Description
21	P11_1	I/O	H	General-purpose input/output port
	$\overline{\text{IOWR}}$			Write strobe output pin at DMA flyby transfer
22	P08_7	I/O	H	General-purpose input/output port
	RDY			External ready input pin
23	P08_6	I/O	H	General-purpose input/output port
	BRQ			External bus release request input pin
24	P08_5	I/O	H	General-purpose input/output port
	$\overline{\text{BGRNT}}$			External bus release reception output pin
25	P08_4	I/O	H	General-purpose input/output port
	$\overline{\text{RD}}$			External read strobe output pin
26	P08_1	I/O	H	General-purpose input/output port
	$\overline{\text{WR1}}$			External write strobe output pin (DQMU signal when using SDRAM)
27	P08_0	I/O	H	General-purpose input/output port
	$\overline{\text{WR0}}$			External write strobe output pin (DQML signal when using SDRAM)
28	$\overline{\text{NMI}}$	I	H	NMI (Non Maskable Interrupt) input pin
29	P10_6	I/O	H	General-purpose input/output port
	MCLKE			Clock enable output signal pin for SDRAM
30	P10_5	I/O	H	General-purpose input/output port
	MCLKI			Clock input pin for SDRAM
31	P10_4	I/O	H	General-purpose input/output port
	MCLKO			Clock output pin for SDRAM
32	P10_3	I/O	H	General-purpose input/output port
	$\overline{\text{WE}}$			External write enable signal pin
33	P10_2	I/O	H	General-purpose input/output port
	$\overline{\text{BAA}}$			Address advance output pin for burst mode FLASH memory
34	P10_1	I/O	H	General-purpose input/output port
	$\overline{\text{AS}}$			Address strobe output pin
35	P10_0	I/O	H	General-purpose input/output port
	SYSCLK			System clock output pin
39	X0	–	G	Clock (oscillation) input pin
40	X1	–	G	Clock (oscillation) output pin
42	X0A	–	G	Sub lock (oscillation) input pin
43	X1A	–	G	Sub lock (oscillation) output pin

Pin no.	Pin name	I/O	I/O circuit type[1]	Description
46 to 53	P01_0 to P01_7	I/O	H	General-purpose input/output ports
	D16 to D23			External data buses (D16 to D23)
54 to 56, 59 to 63	P00_0 to P00_7	I/O	H	General-purpose input/output ports
	D24 to D31			External data buses (D24 to D31)
64 to 71	P07_0 to P07_7	I/O	H	General-purpose input/output ports
	A00 to A07			External address buses (A00 to A07)
72, 75 to 81	P06_0 to P06_7	I/O	H	General-purpose input/output ports
	A08 to A15			External address buses (A08 to A15)
82 to 87, 90, 91	P05_0 to P05_7	I/O	H	General-purpose input/output ports
	A16 to A23			External address buses (A16 to A23)
92	P16_7	I/O	H	General-purpose input/output ports
	$\overline{ATG}$			A/D converter external trigger input
93 to 96	P17_4 to P17_7	I/O	H	General-purpose input/output ports
	PPG4 to PPG7			PPG timer output pin
97	$\overline{WDRESET}$	O	I	Watchdog reset output pin
98 to 105	P29_0 to P29_7	I/O	F	General-purpose input/output ports
	AN0 to AN7			Analog input pins for A/D converter
106 to 113	P28_0 to P28_7	I/O	F	General-purpose input/output ports
	AN8 to AN15			Analog input pins for A/D converter
117	P22_4	I/O Open Drain	C	General-purpose input/output port
	SDA0			I^2C bus DATA input/output pin
	INT14			External interrupt input pin
118	P22_5	I/O Open Drain	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin
119, 120	P24_0, P24_1	I/O	D	General-purpose input/output ports
	INT0, INT1			External interrupt input pins Can be used as a source for recovering from shutdown
121, 122	P24_6, P24_7	I/O	D	General-purpose input/output port
	INT6, INT7			External interrupt input pin Can be used as a source for recovering from shutdown

Pin no.	Pin name	I/O	I/O circuit type[1]	Description
123	P23_0	I/O	D	General-purpose input/output port
	RX0			RX input/output pin of CAN0
	INT8			External interrupt input pin Can be used as a source for recovering from shutdown
124	P23_1	I/O	D	General-purpose input/output port
	TX0			TX output pin of CAN0
125	P23_2	I/O	D	General-purpose input/output port
	RX1			RX input/output pin of CAN1
	INT9			External interrupt input pin Can be used as a source for recovering from shutdown
126	P23_3	I/O	D	General-purpose input/output port
	TX1			TX output pin of CAN1
127	MD3	I	A	Mode setting pins
128, 129, 130	MD0	I	J	
131	$\overline{\text{INIT}}$	I	B	External reset input pin
134	P21_0	I/O	D	General-purpose input/output port
	SIN0			Data input pin of UART0
135	P21_1	I/O	D	General-purpose input/output port
	SOT0			Data output pin of UART0
136	P21_2	I/O	D	General-purpose input/output port
	SCK0			Clock input/output pin of UART0
	FRCK0			External clock input pin of free-run timer0
137	P21_4	I/O	D	General-purpose input/output port
	SIN1			Data input pin of UART1
138	P21_5	I/O	D	General-purpose input/output port
	SOT1			Data output pin of UART1
139	P21_6	I/O	D	General-purpose input/output port
	SCK1			Clock input/output pin of UART1
	FRCK1			External clock input pin of free-run timer 1
140	P20_0	I/O	D	General-purpose input/output port
	SIN2			Data input pin of UART2
141	P20_1	I/O	D	General-purpose input/output port
	SOT2			Data output pin of UART2

Pin no.	Pin name	I/O	I/O circuit type[1]	Description
142	P20_2	I/O	D	General-purpose input/output port
	SCK2			Clock input/output pin of UART2
	FRCK2			External clock input pin of free-run timer 2
143	P20_4	I/O	D	General-purpose input/output port
	SIN3			Data input pin of UART3
144	P20_5	I/O	D	General-purpose input/output port
	SOT3			Data output pin of UART3
145	P20_6	I/O	D	General-purpose input/output port
	SCK3			Clock input pin of UART3
	FRCK3			External clock input pin of free-run timer 3
148	P19_0	I/O	D	General-purpose input/output port
	SIN4			Data input pin of UART4
149	P19_1	I/O	D	General-purpose input/output port
	SOT4			Data output pin of UART4
150	P19_2	I/O	D	General-purpose input/output port
	SCK4			Clock input/output pin of UART4
151	P19_4	I/O	D	General-purpose input/output port
	SIN5			Data input pin of UART5
152	P19_5	I/O	D	General-purpose input/output port
	SOT5			Data output pin of UART5
153	P19_6	I/O	D	General-purpose input/output port
	SCK5			Clock input/output pin of UART5
154	P18_0	I/O	D	General-purpose input/output port
	SIN6			Data input pin of UART6
155	P18_1	I/O	D	General-purpose input/output port
	SOT6			Data output pin of UART6
156	P18_2	I/O	D	General-purpose input/output port
	SCK6			Clock input/output pin of UART6
157 to 160	P15_0 to P15_3	I/O	D	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
163, 164	P23_4, P23_6	I/O	D	General-purpose input/output port
	INT10, INT11			External interrupt input pin

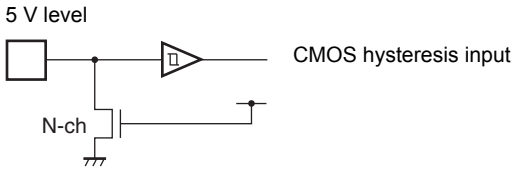
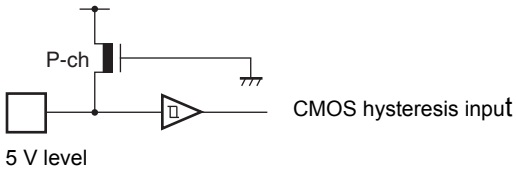
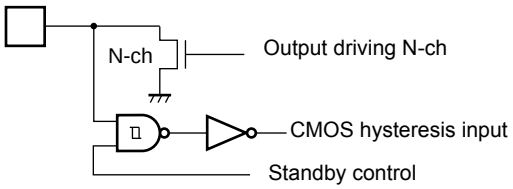
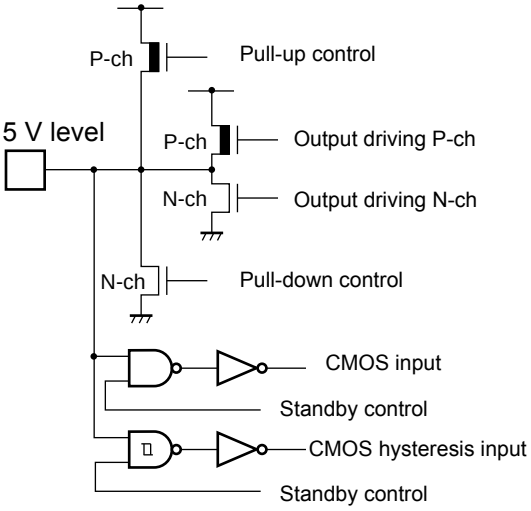
Pin no.	Pin name	I/O	I/O circuit type[1]	Description
165, 166	P22_0, P22_2	I/O	D	General-purpose input/output port
	INT12, INT13			External interrupt input pin
167	P22_3	I/O	D	General-purpose input/output port
168 to 171	P14_0 to P14_3	I/O	D	General-purpose input/output ports
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TRG0 to TRG3			External trigger input pins of PPG
172 to 175	P17_0 to P17_3	I/O	D	General-purpose input/output ports
	PPG0 to PPG3			PPG timer output pins

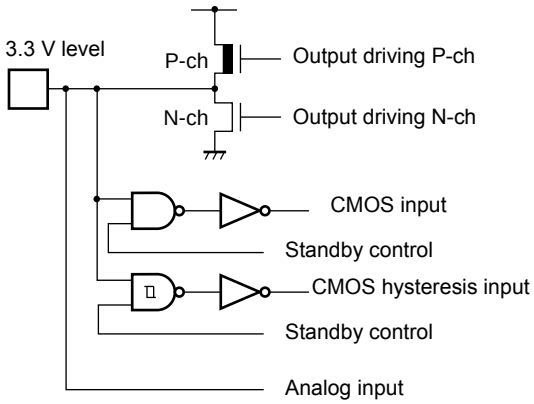
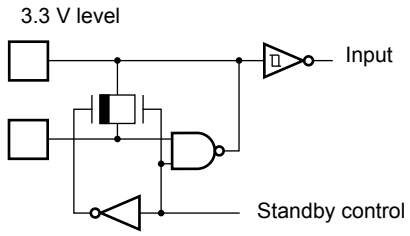
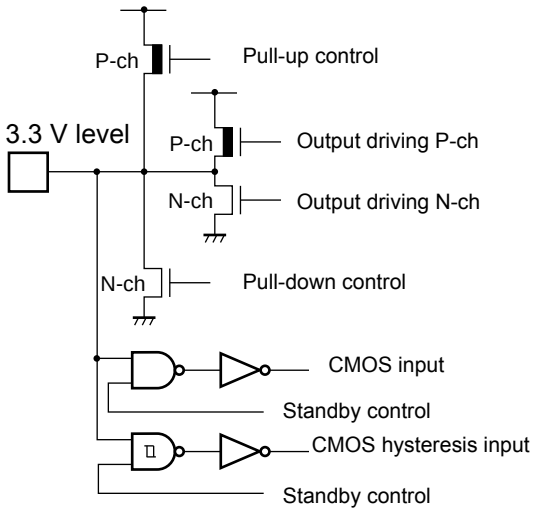
1. For I/O circuit type, refer to "I/O Circuit Type".

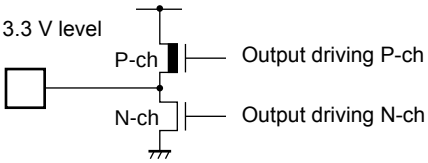
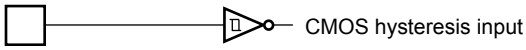
2.1 Power supply/GND pins

Pin number	Pin name	I/O	Function
1, 13, 38, 41, 45, 58, 74, 88, 132, 146, 161	VSS	(V_{SS})	GND pins
11, 12, 36, 44, 57, 73, 89	VCC3	($V_{CC}3$)	3.3 V power supply pins
133, 147	VCC5	($V_{CC}5$)	5 V power supply pins. These pins are I/O power supplies corresponding to 117 to 145 pins. The corresponding I/O pin operates at 3.3 V when supplying 3.3 V, and at 5 V when supplying 5V. Be sure to supply 5 V if more than one 5V operating pin is specified, or 5V is supplied at pin 162 or pin 176.
162	VCC5	($V_{CC}5$)	5 V power supply pin. This pin is an I/O power supply corresponding to 148 to 160 pins. The corresponding I/O pin operates at 3.3 V when supplying 3.3 V, and at 5V when supplying 5 V. Be sure to supply 5 V if more than one 5 V operating pin is specified.
176	VCC5	($V_{CC}5$)	5 V power supply pin. This pin is an I/O power supply corresponding to 2 to 7, 163 to 175 pins. The corresponding I/O pin operates at 3.3 V when supplying 3.3 V, and at 5 V when supplying 5 V. Be sure to supply 5 V if more than one 5 V operating pin is specified.
114	AVSS/AVRL	(AV_{SS})	Analog GND pin for A/D converter
115	AVCC3	($AV_{CC}3$)	3.3 V power supply pin for A/D converter
116	AVRH	(AVRH)	Reference power supply pin for A/D converter
14	C_1	–	Capacitor connection pin for internal regulator Connect to a capacitance of 4.7 μF.
37	C_2	–	Capacitor connection pin for internal regulator Connect to a capacitance of 4.7 μF.

3. I/O Circuit Type

Type	Circuit type	Remarks
A		5 V CMOS hysteresis input With 50 kΩ pull-down
B		5 V CMOS hysteresis input With 50 kΩ pull-up
C		I/O pin for I^2C Withstand voltage of 5 V (with standby control)
D		5 V CMOS output 5 V CMOS input 5 V CMOS hysteresis level input With pull-up/pull-down control (with standby control)

Type	Circuit type	Remarks
F		3.3 V CMOS output 3.3 V CMOS input 3.3 V CMOS hysteresis level input Analog input (with standby control)
G		3.3 V oscillation cell
H		3.3 V CMOS output 3.3 V CMOS input 3.3 V CMOS hysteresis level input With pull-up/pull-down control (with standby control)

Type	Circuit type	Remarks
I		3.3 V CMOS output
J		5 V CMOS hysteresis input

4. Handling Devices

4.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than V_{CC} or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rating is applied between VCC5 pin (VCC3 pin) and VSS pin. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, when using a CMOS IC, do not exceed the maximum rating.

4.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor.

4.3 Power Supply Pins

In MB91460R series, devices including multiple VCC5 pin (VCC3 pin) and VSS pin are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pin and GND pin must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the VCC5 pin (VCC3 pin) pins and VSS pin of the MB91460R series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between VCC5 pin (VCC3 pin) and VSS pin near this device. This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μF to C_1 and C_2 pins for the regulator.

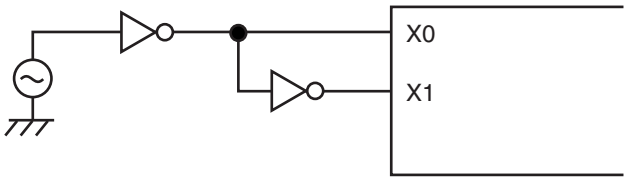
4.4 Crystal Oscillator Circuit

Noise in proximity to the X0 and X1 (X0A, X1A) pins can cause abnormal operation in this device. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are placed as close together as possible.
The use of printed circuit board architecture in which the X0 and X1 (X0A, X1A) pins are surrounded by ground contributes to stable operation and is strongly recommended.
Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

4.5 Notes on using External Clock

In principle, when using external clock, supply a clock to the X0 pin and X1 pin simultaneously. Also, an opposite phase clock to the X0 pin must be supplied to the X1 pin. However, in this case the stop mode (oscillation stop mode) must not be used (This is because the X1 pin stops at ”H” output in STOP mode).

Figure 1. Example of using external clock (normal)



Note: Stop mode (oscillation stop mode) cannot be used.

4.6 Mode Pins (MD0 to MD3)

When using mode pins, connect them directly to VCC5 pin (VCC3 pin) or VSS pin. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and VCC5 pin (VCC3 pin) or VSS pin on the printed circuit board as possible and connect them with low impedance.

4.7 Power-on Sequences for 3.3 V and 5 V

- Immediately after power-on, keep “L” level input to the $\overline{\text{INIT}}$ pin for the oscillation stabilization wait time (8 ms) to ensure the oscillation stabilization wait time for the oscillator circuit.
- There is no power-on sequences.
- When executing a reset cancellation (changing $\overline{\text{INIT}}$ pin from “L” level to “H” level), be sure to execute it while 3 V and 5 V power supplies are stable.

4.8 Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Cypress will not guarantee results of operations if such failure occurs.

4.9 External Bus Setting

This model guarantees the maximum frequency of 40 MHz for the external bus clock SYSCLK. Setting the base clock frequency to 80 MHz without changing the initial value of DIVR1 (external bus base clock division setting register) sets the external bus frequency also to 80 MHz. Before changing the base clock frequency, set SYSCLK not exceeding 40 MHz.

4.10 Pull-up Control

Connecting a pull-up resistor to the pin serving as an external bus pin cannot guarantee the AC standard.

4.11 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

4.12 Notes on PS register

Since some instructions process the PS register in advance, the exceptional operations may cause a break in the interrupt process routine or an update of display contents of the flag in the PS register when the debugger is being used. In either case, as the device is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified.

- **The following operations may be performed when the instruction immediately followed by a DIV0U/DIV0S instruction accepts a user interrupt/NMI, executes a step, or breaks in response to a data event or emulator menu.**
  - -D0 and D1 flags are updated in advance.
  - -An EIT process routine (user interrupt/NMI or emulator) is executed.
  - -Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).
- The following operations are performed when each instruction of OR CCR, ST ILM, MOV Ri and PS is executed to enable interrupts while a user interrupt/NMI source has been occurring.
  - -The PS register is updated in advance.
  - -An EIT process routine (user interrupt/NMI or emulator) is executed.
  - -Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as that in 1).

5. Notes On Debugger

5.1 Step execution of RETI instruction

In the environment where interrupts occur frequently when stepping, only the corresponding interrupt process routines are repeated. As the result of that, the main routine and low-interrupt-level programs are not executed (For example, if an interrupt to the time base timer is enabled, a break always occurs at the beginning of the time base routine when stepping RETI) .

Disable the corresponding interrupts when the debug on the corresponding interrupt process routines becomes unnecessary.

5.2 Break function

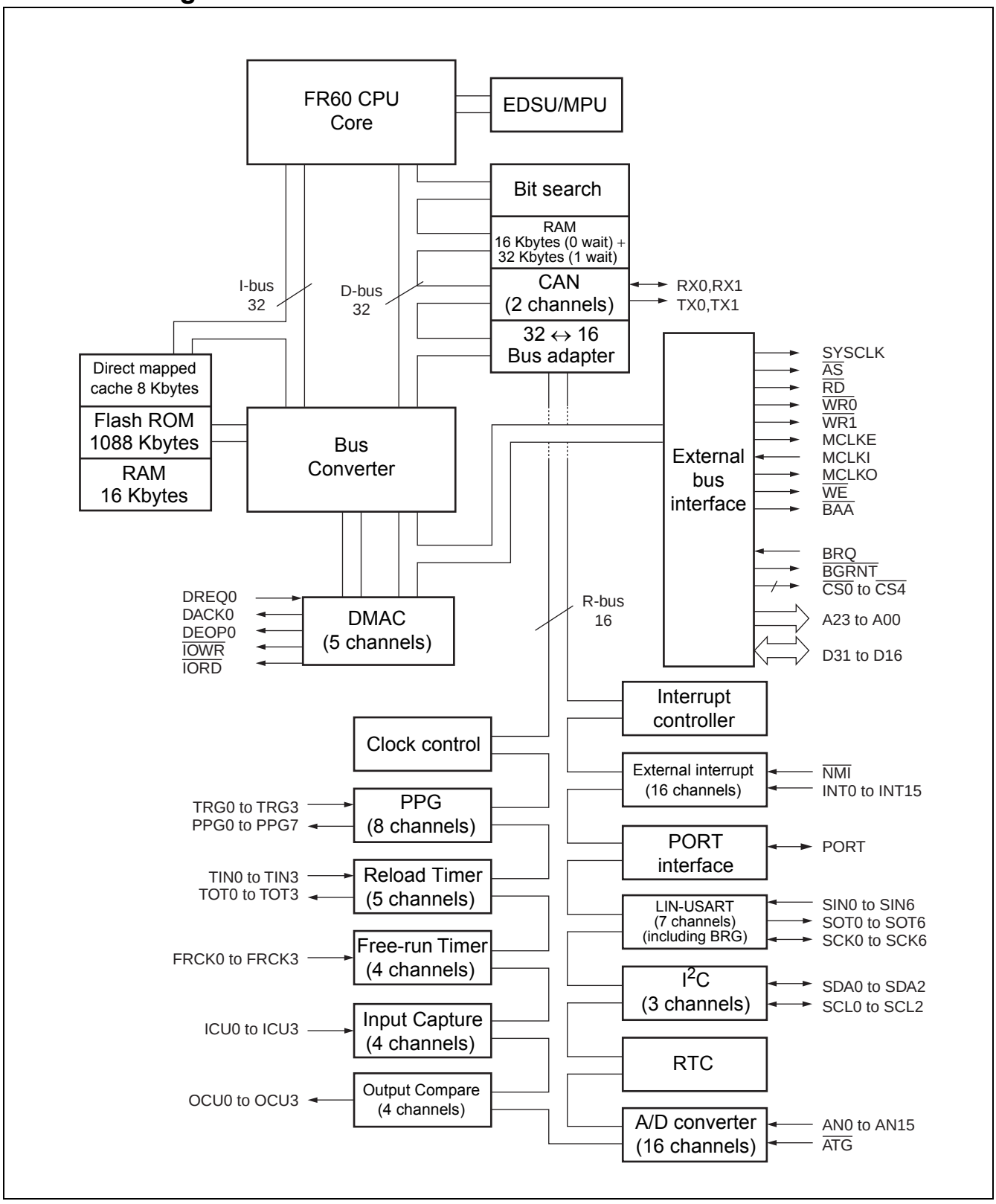
If the target address of a hardware break (including an event break) is set to the address currently contained in the system stack pointer or in the area containing the stack pointer, the user program causes a break after execution of one instruction even though there is no actual data access instruction in the user program.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of a hardware break (including an event break).

5.3 Operand break

If a stack pointer exists in the area which is set as the DSU operand break, malfunctions may occur. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

6. Block Diagram



7. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

7.1 Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- Linear memory space: 4 Gbytes
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  - Quick response speed (6 cycles)
  - Multiple-interrupt support
  - Level mask function (16 levels)
- Enhanced instructions for I/O operation
  - Memory-to-memory transfer instructions
  - Bit processing instructions
- Basic instruction word length: 16 bits
- Low-power Consumption
  Sleep mode/stop mode/shutdown mode

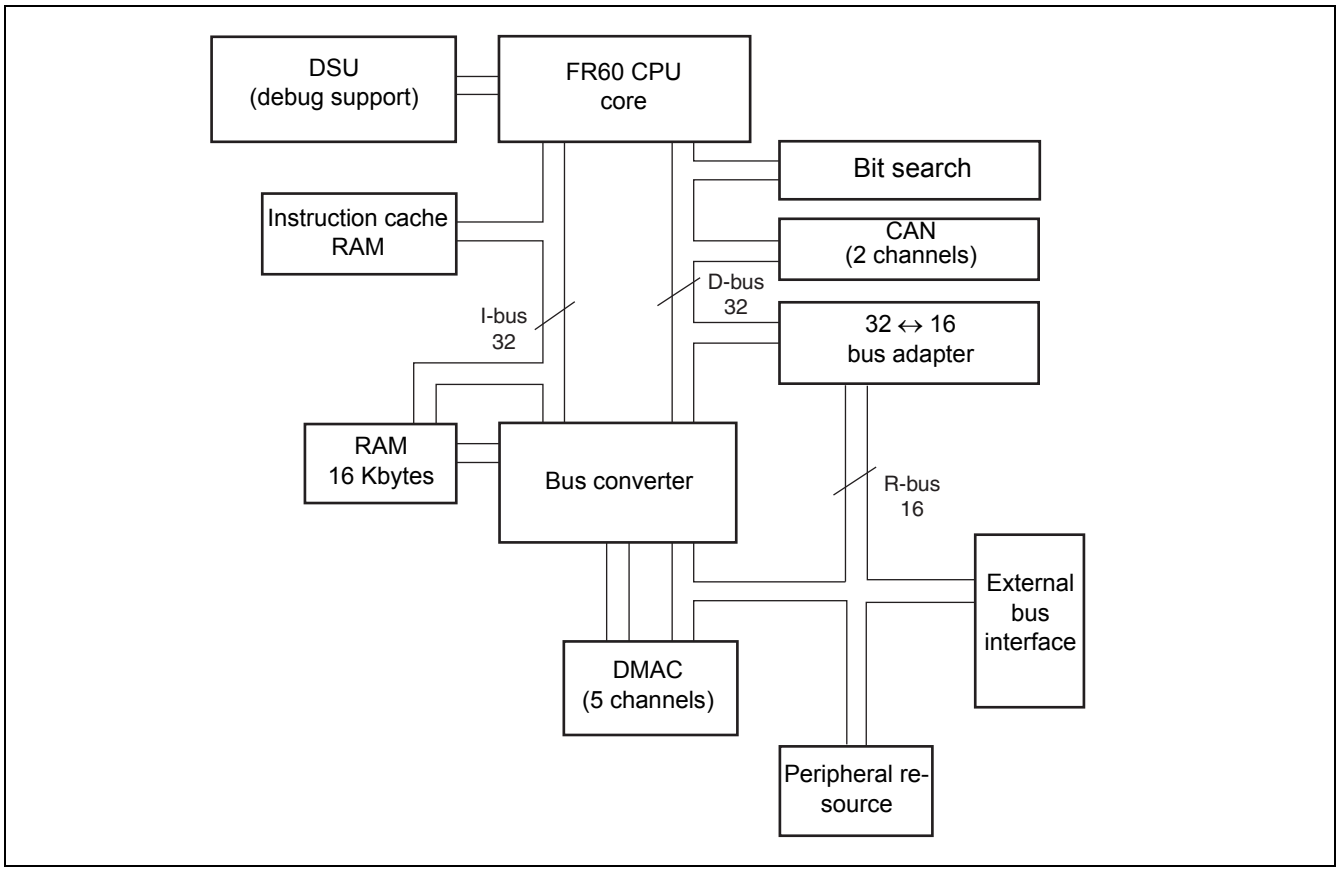
7.2 Internal Architecture

The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.

A 32-bit ↔ 16-bit bus adapter is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.

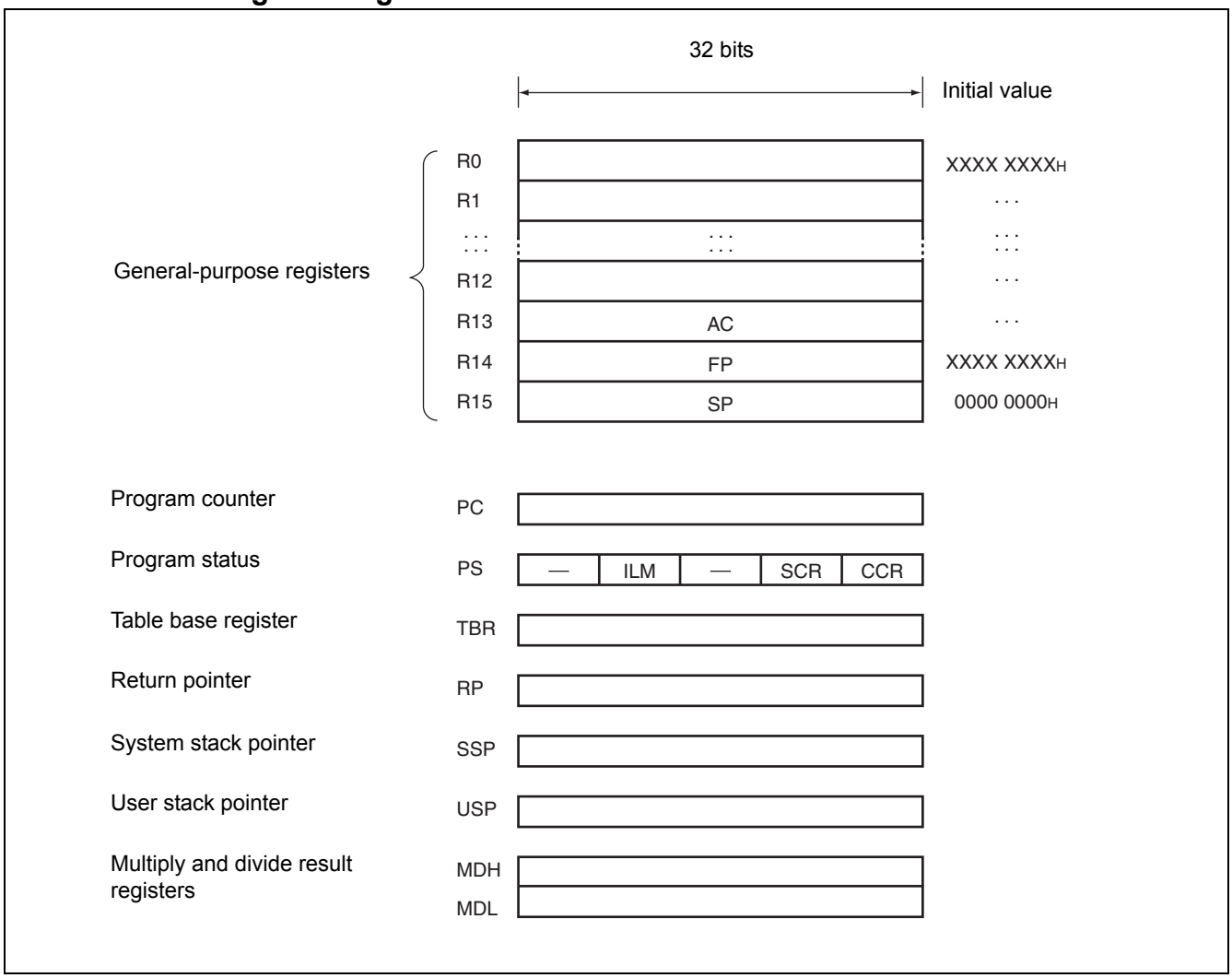
A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

The following figure shows the internal architecture structure.



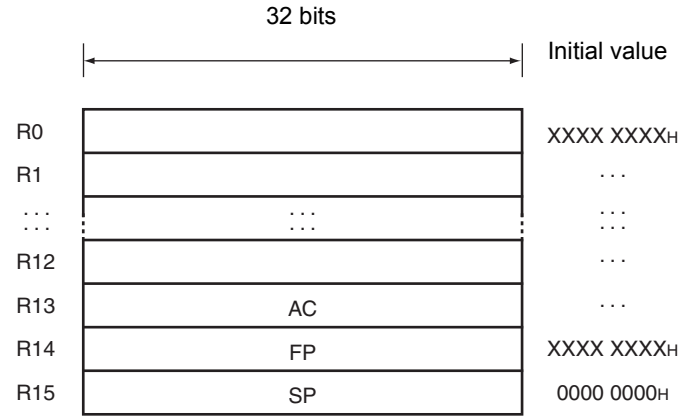
7.3 Programming Model

7.3.1 Basic Programming Model



7.4 Registers

7.4.1 General-Purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13: Virtual accumulator

R14: Frame pointer

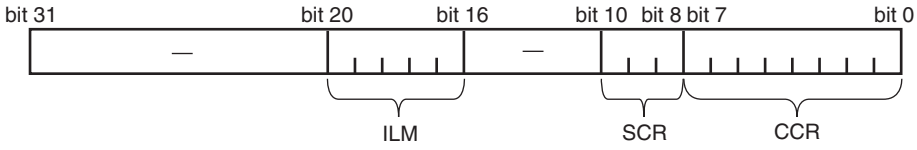
R15: Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

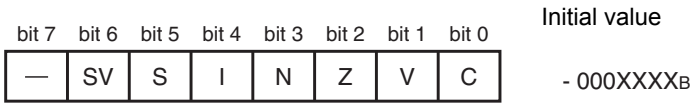
7.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



7.4.3 CCR (Condition Code Register)



SV: Supervisor flag

S: Stack flag

I: Interrupt enable flag

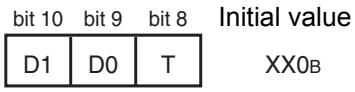
N: Negative enable flag

Z: Zero flag

V: Overflow flag

C: Carry flag

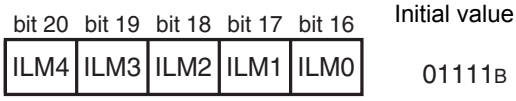
7.4.4 SCR (System Condition Register)



Flag for step multiplication (D1, D0)
This flag stores interim data during execution of step multiplication.

Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

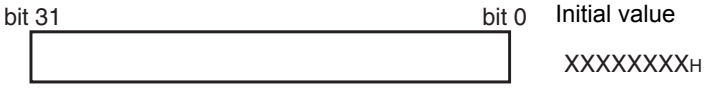
7.4.5 ILM



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111_B” at reset.

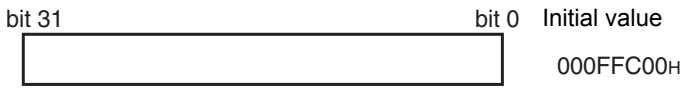
7.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

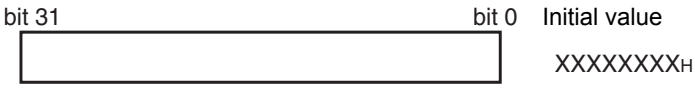
7.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

7.4.8 RP (Return Pointer)



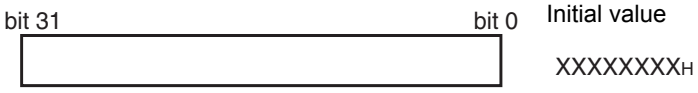
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

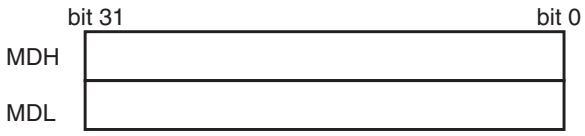
7.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

7.4.10 Multiply & Divide Registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

8. Mode Setting

In the FR family, the mode pins (MD2, MD1, MD0) and the mode register (MODR) are used to set the operating mode.

8.1 Mode Pins

The three pins MD2, MD1, MD0 are used to specify the mode vector fetch related settings.

Settings other than shown in the table are not allowed.

Mode pins[1]			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	Bus width is set by mode register.

1. Always use MD3 with “0”.

Note: The FR family does not support the external mode vector fetch using multiplex bus.

8.2 Mode Register (MODR)

The data written to the mode register using mode vector fetch is called mode data.

After the mode register (MODR) is set, the device operates according to the operation mode set in this register.

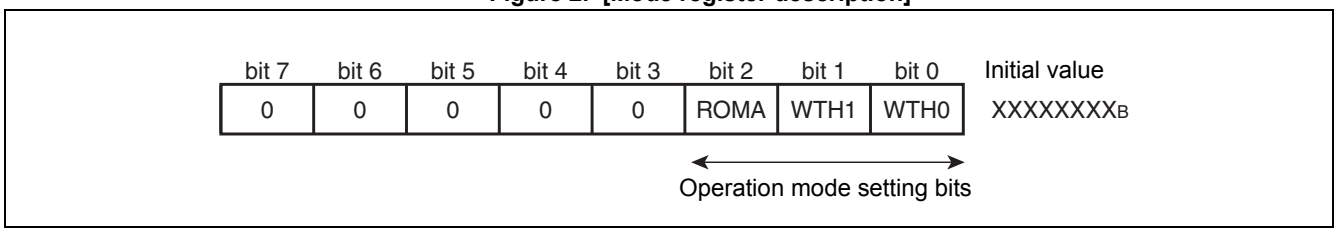
The mode register is set by all reset sources. User programs cannot write data to the mode register.

Rewriting is allowed in the emulator mode. In this case, use an 8-bit length data transfer instruction.

A 16/32-bit length transfer instruction cannot be used for writing.

Description of the mode register is given below.

Figure 2. [Mode register description]



8.2.1 [bit7 to bit3] Reserved bits

Be sure to set these bits to "00000_B".

Operation is not guaranteed when any value other than "00000_B" is set.

8.2.2 [bit2] ROMA (Internal Enable Bit)

The ROMA bit is used to set whether to enable the internal F-bus RAM and F-bus ROM areas.

ROMA	Function	Remarks
0	External ROM mode	Internal F-bus RAM becomes valid. The internal ROM area (40000_H to $FFFFF_H$) is used as an external area.
1	Internal ROM mode	Internal F-bus RAM and F-bus ROM become valid.

8.2.3 [bit1, bit0] WTH1, WTH0 (Bus width setting bits)

These bits are used to set the bus width to be used in the external bus mode.

When the operation mode is the external bus mode, these values are set in bits DBW1 and DBW0 in ACR0 (CS0 area).

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	–	Setting disabled
1	1	Single chip mode	Single chip mode

9. Memory Space

9.1 Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area
The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

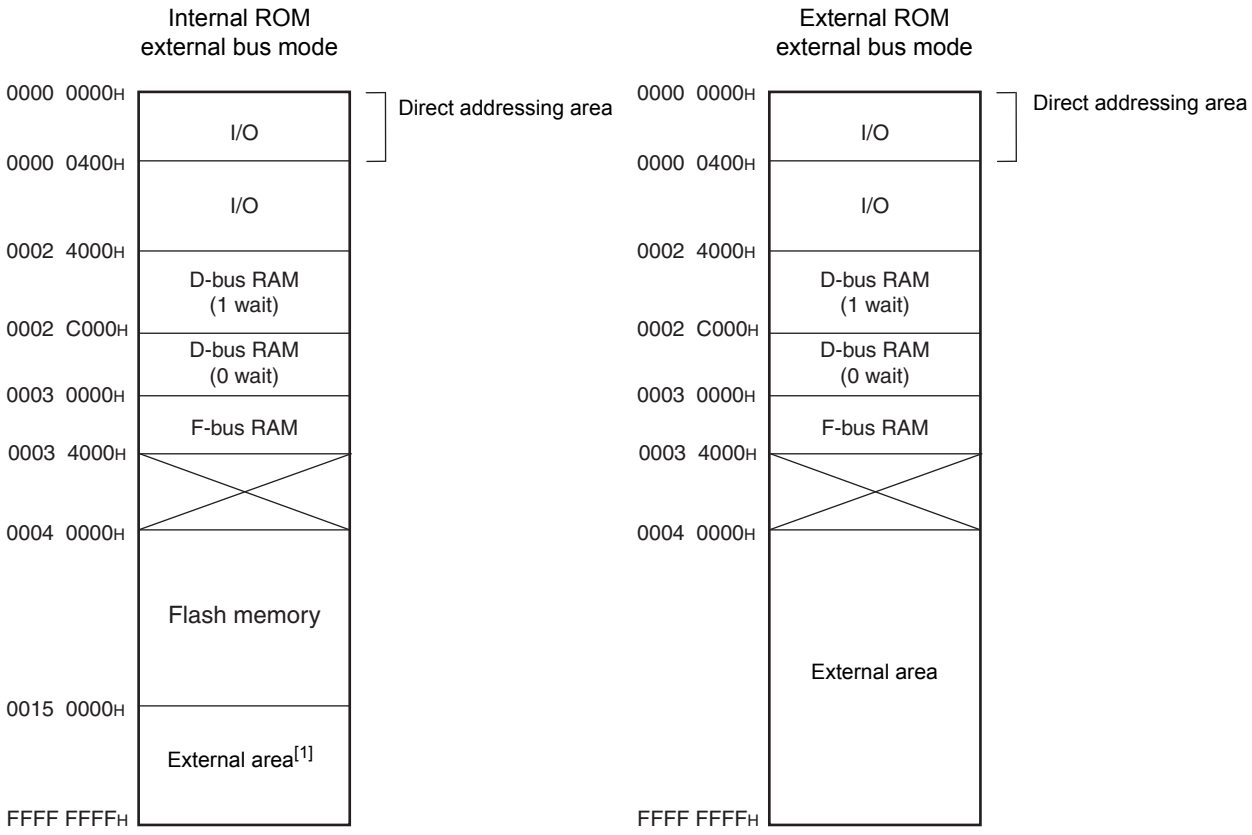
The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access: 000_H to $0FF_H$

Half word access: 000_H to $1FF_H$

Word data access: 000_H to $3FF_H$

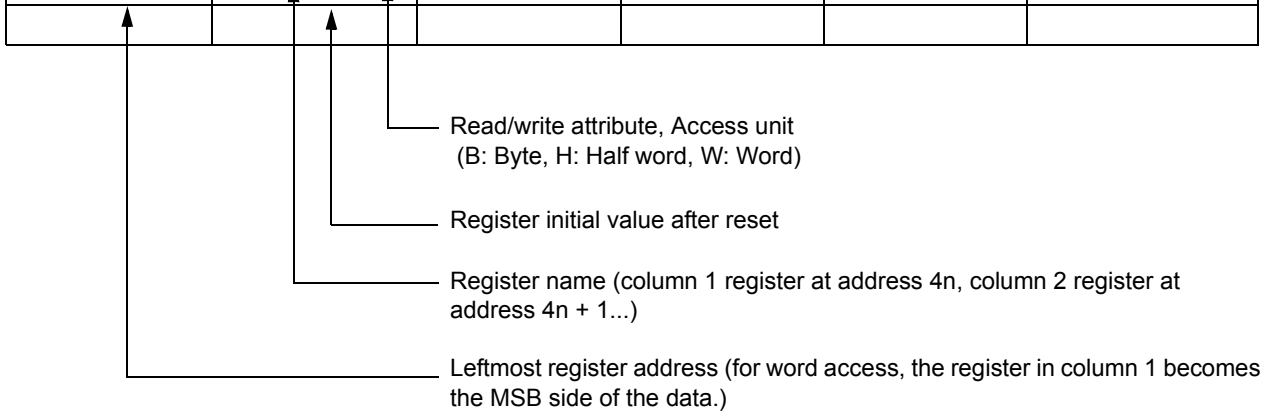
9.2 Memory Map



1. The region from 150000_H may not be able to be used as an external region, depending on the CS region setting.

10. I/O Map

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W]B XXXXXXXX	PDR1 [R/W]B XXXXXXXX	PDR2 [R/W]B XXXXXXXX	PDR3 [R/W]B XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:
" 1 ": Initial value " 1 "
" 0 ": Initial value " 0 "
" X ": Initial value " undefined "
" - ": No physical register at this location
" * ": The same value as value of WTH bit
Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] B, H XXXXXXXX	PDR01 [R/W] B, H XXXXXXXX	Reserved		Port Data Register
000004_H	Reserved	PDR05 [R/W] B, H XXXXXXXX	PDR06 [R/W] B, H XXXXXXXX	PDR07 [R/W] B, H XXXXXXXX	
000008_H	PDR08 [R/W] B, H XXXX - - XX	PDR09 [R/W] B, H - - - XXXXX	PDR10 [R/W] B, H - XXXXXXX	PDR11 [R/W] B, H - - - - - - XX	
$00000C_H$	Reserved	PDR13 [R/W] B, H - - - - - XXX	PDR14 [R/W] B, H - - - - XXXX	PDR15 [R/W] B, H - - - - XXXX	
000010_H	PDR16 [R/W] B, H X - - - - - - -	PDR17 [R/W] B, H XXXXXXXX	PDR18 [R/W] B, H - - - - - XXX	PDR19 [R/W] B, H - XXX - XXX	
000014_H	PDR20 [R/W] B, H - XXX - XXX	PDR21 [R/W] B, H - XXX - XXX	PDR22 [R/W] B, H XXXXXX - X	PDR23 [R/W] B, H - X - XXXXX	
000018_H	PDR24 [R/W] B, H XXXXXXXX	Reserved			
$00001C_H$	PDR28 [R/W] B, H XXXXXXXX	PDR29 [R/W] B, H XXXXXXXX	Reserved		
000020_H to $00002C_H$	Reserved				Reserved
000030_H	EIRR0 [R/W] B 00000000	ENIR0 [R/W] B 00000000	ELVR0 [R/W] B, H 00000000 00000000		External Interrupt (INT 0 to INT 7) NMI
000034_H	EIRR1 [R/W] B 00000000	ENIR1 [R/W] B 00000000	ELVR1 [R/W] B, H 00000000 00000000		External Interrupt (INT 8 to INT 15)
000038_H	DICR [R/W] B - - - - - - - 0	HRCL [R/W] B 0 - - 11111	Reserved		DLYI/I-unit
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W, W] B, H, W 00000000	SMR00 [R/W, W] B, H, W 00000000	SSR00 [R/W, R] B, H, W 00001000	RDR00/TDR00 [R/W] B, H, W 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] B, H 00000X00	ECCR00 [R/W, R, W] B, H -00000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000048_H	SCR01 [R/W, W] B, H, W 00000000	SMR01 [R/W, W] B, H, W 00000000	SSR01 [R/W, R] B, H, W 00001000	RDR01/TDR01 [R/W] B, H, W 00000000	LIN-USART 1
$00004C_H$	ESCR01 [R/W] B, H 00000X00	ECCR01 [R/W, R, W] B, H -00000XX	Reserved		
000050_H	SCR02 [R/W, W] B, H, W 00000000	SMR02 [R/W, W] B, H, W 00000000	SSR02 [R/W, R] B, H, W 00001000	RDR02/TDR02 [R/W] B, H, W 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] B, H 00000X00	ECCR02 [R/W, R, W] B, H -00000XX	Reserved		
000058_H	SCR03 [R/W, W] B, H, W 00000000	SMR03 [R/W, W] B, H, W 00000000	SSR03 [R/W, R] B, H, W 00001000	RDR03/TDR03 [R/W] B, H, W 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] B, H 00000X00	ECCR03 [R/W, R, W] B, H -00000XX	Reserved		
000060_H	SCR04 [R/W, W] B, H, W 00000000	SMR04 [R/W, W] B, H, W 00000000	SSR04 [R/W, R] B, H, W 00001000	RDR04/TDR04 [R/W] B, H, W 00000000	LIN-USART 4
000064_H	ESCR04 [R/W] B, H 00000X00	ECCR04 [R/W, R, W] B, H -00000XX	Reserved		
000068_H	SCR05 [R/W, W] B, H, W 00000000	SMR05 [R/W, W] B, H, W 00000000	SSR05 [R/W, R] B, H, W 00001000	RDR05/TDR05 [R/W] B, H, W 00000000	LIN-USART 5
$00006C_H$	ESCR05 [R/W] B, H 00000X00	ECCR05 [R/W, R, W] B, H -00000XX	Reserved		
000070_H	SCR06 [R/W, W] B, H, W 00000000	SMR06 [R/W, W] B, H, W 00000000	SSR06 [R/W, R] B, H, W 00001000	RDR06/TDR06 [R/W] B, H, W 00000000	LIN-USART 6
000074_H	ESCR06 [R/W] B, H 00000X00	ECCR06 [R/W, R, W] B, H -00000XX	Reserved		
000078_H, $00007C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000080_H	BGR100 [R/W] B, H, W 00000000	BGR000 [R/W] B, H, W 00000000	BGR101 [R/W] B, H, W 00000000	BGR001 [R/W] B, H, W 00000000	Baud rate Generator LIN-USART 0 to 6
000084_H	BGR104 [R/W] B, H, W 00000000	BGR004 [R/W] B, H, W 00000000	BGR105 [R/W] B, H, W 00000000	BGR005 [R/W] B, H, W 00000000	
000088_H	BGR106 [R/W] B, H, W 00000000	BGR006 [R/W] B, H, W 00000000	BGR107 [R/W] B, H, W 00000000	BGR007 [R/W] B, H, W 00000000	
$00008C_H$	BGR102 [R/W] B, H, W 00000000	BGR002 [R/W] B, H, W 00000000	Reserved		
000090_H to $0000CC_H$	Reserved				Reserved
$0000D0_H$	IBCR0 [R/W] B, H 00000000	IBSR0 [R] B, H 00000000	ITBAH0 [R/W] B, H - - - - - - 00	ITBAL0 [R/W] B, H 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] B, H 00 - - - - 11	ITMKL0 [R/W] B, H 11111111	ISMK0 [R/W] B, H 01111111	ISBA0 [R/W] B, H - 0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] B, H 00000000	ICCR0 [R/W] B - 0011111	Reserved	
$0000DC_H$	IBCR1 [R/W] B, H 00000000	IBSR1 [R] B, H 00000000	ITBAH1 [R/W] B, H - - - - - - 00	ITBAL1 [R/W] B, H 00000000	I^2C 1
$0000E0_H$	ITMKH1 [R/W] B, H 00 - - - - 11	ITMKL1 [R/W] B, H 11111111	ISMK1 [R/W] B, H 01111111	ISBA1 [R/W] B, H - 0000000	
$0000E4_H$	Reserved	IDAR1 [R/W] B, H 00000000	ICCR1 [R/W] B - 0011111	Reserved	
$0000E8_H$ to $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] B, H 00110010 00010000		Reserved	GCN20 [R/W] B - - - - 0000	PPG Control 0 to 3
000104_H	GCN11 [R/W] B, H 00110010 00010000		Reserved	GCN21 [R/W] B - - - - 0000	PPG Control 4 to 7
000108_H, $00010C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000110_H	PTMR00 [R] H 11111111 11111111		PCSR00 [W] H XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] H XXXXXXXX XXXXXXXX		PCNH00 [R/W] B, H 0000000 -	PCNL00 [R/W] B, H 000000 - 0	
000118_H	PTMR01 [R] H 11111111 11111111		PCSR01 [W] H XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] H XXXXXXXX XXXXXXXX		PCNH01 [R/W] B, H 0000000 -	PCNL01 [R/W B, H] 000000 - 0	
000120_H	PTMR02 [R] H 11111111 11111111		PCSR02 [W] H XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] H XXXXXXXX XXXXXXXX		PCNH02 [R/W] B, H 0000000 -	PCNL02 [R/W] B, H 000000 - 0	
000128_H	PTMR03 [R] H 11111111 11111111		PCSR03 [W] H XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] H XXXXXXXX XXXXXXXX		PCNH03 [R/W] B, H 0000000 -	PCNL03 [R/W] B, H 000000 - 0	
000130_H	PTMR04 [R] H 11111111 11111111		PCSR04 [W] H XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] H XXXXXXXX XXXXXXXX		PCNH04 [R/W] B, H 0000000 -	PCNL04 [R/W] B, H 000000 - 0	
000138_H	PTMR05 [R] H 11111111 11111111		PCSR05 [W] H XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] H XXXXXXXX XXXXXXXX		PCNH05 [R/W] B, H 0000000 -	PCNL05 [R/W] B, H 000000 - 0	
000140_H	PTMR06 [R] H 11111111 11111111		PCSR06 [W] H XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] H XXXXXXXX XXXXXXXX		PCNH06 [R/W] B, H 0000000 -	PCNL06 [R/W] B, H 000000 - 0	
000148_H	PTMR07 [R] H 11111111 11111111		PCSR07 [W] H XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] H XXXXXXXX XXXXXXXX		PCNH07 [R/W] B, H 0000000 -	PCNL07 [R/W] B, H 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000170_H to $00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] B 00000000	Reserved	ICS23 [R/W] B 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] H XXXXXXXX XXXXXXXX		IPCP1 [R] H XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] H XXXXXXXX XXXXXXXX		IPCP3 [R] H XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] H - - - 0 - - 00 0000 - - 00		OCS23 [R/W] H - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] H XXXXXXXX XXXXXXXX		OCCP1 [R/W] H XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] H XXXXXXXX XXXXXXXX		OCCP3 [R/W] H XXXXXXXX XXXXXXXX		
000198_H, $00019C_H$	Reserved				Reserved
$0001A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] B, H 00000000	ADCS0 [R/W] B, H 00000000	ADCR1 [R] B, H 000000XX	ADCR0 [R] B, H XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] B, H 00010000	ADCT0 [R/W] B, H 00101100	ADSCH [R/W] B, H - - - 00000	ADECH [R/W] B, H - - - 00000	
$0001AC_H$	Reserved	ACSR0 [R/W] B, H - 11XXX00	Reserved		Alarm Comparator 0
$0001B0_H$	TMRLR0 [W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
$0001B4_H$	Reserved		TMCSRH0 [R/W] B, H - - - 00000	TMCSRL0 [R/W] B, H 0 - 000000	
$0001B8_H$	TMRLR1 [W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
$0001BC_H$	Reserved		TMCSRH1 [R/W] B, H - - - 00000	TMCSRL1 [R/W] B, H 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
$0001C0_H$	TMRLR2 [W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] B, H - - - 00000	TMCSRL2 [R/W] B, H 0 - 000000	
$0001C8_H$	TMRLR3 [W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
$0001CC_H$	Reserved		TMCSRH3 [R/W] B, H - - - 00000	TMCSRL3 [R/W] B, H 0 - 000000	
$0001D0_H$ to $0001E4_H$	Reserved				Reserved
$0001E8_H$	TMRLR7 [W] H XXXXXXXX XXXXXXXX		TMR7 [R] H XXXXXXXX XXXXXXXX		Reload Timer 7 (A/D converter)
$0001EC_H$	Reserved		TMCSRH7 [R/W] B, H - - - 00000	TMCSRL7 [R/W] B, H 0 - 000000	
$0001F0_H$	TCDT0 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
$0001F4_H$	TCDT1 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
$0001F8_H$	TCDT2 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
$0001FC_H$	TCDT3 [R/W] H XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)
000200_H	DMACA0 [R/W] B, H, W [1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] B, H, W [1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] B, H, W [1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
000218_H	DMACA3 [R/W] B, H, W [1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
$00021C_H$	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] B, H, W [1] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] B, H, W 00 - - 0000	Reserved			
000244_H to 000364_H	Reserved				Reserved
000368_H	IBCR2 [R/W] B, H 00000000	IBSR2 [R] B, H 00000000	ITBAH2 [R/W] B, H - - - - - - 00	ITBAL2 [R/W] B, H 00000000	I^2C 2
$00036C_H$	ITMKH2 [R/W] B, H 00 - - - - 11	ITMKL2 [R/W] B, H 11111111	ISMK2 [R/W] B, H 01111111	ISBA2 [R/W] B, H - 0000000	
000370_H	Reserved	IDAR2 [R/W] B, H 00000000	ICCR2 [R/W] B - 0011111	Reserved	
000374_H to $00038C_H$	Reserved				Reserved
000390_H	ROMS [R] 11111111 00000000		Reserved		ROM Select Register
000394_H to $0003EC_H$	Reserved				Reserved
$0003F0_H$	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
000400_H to $00043C_H$	Reserved				Reserved
000440_H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt Control Unit
000444_H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448_H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	Reserved	ICR11 [R/W] B, H, W ---11111	
$00044C_H$	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	Reserved		
000450_H	ICR16 [R/W] B, H, W ---11111	Reserved		ICR19 [R/W] B, H, W ---11111	Interrupt Control
000454_H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458_H	Reserved	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
$00045C_H$	Reserved	ICR29 [R/W] B, H, W ---11111	Reserved		
000460_H	Reserved				
000464_H	Reserved		ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468_H	Reserved		ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
$00046C_H$	Reserved				
000470_H	ICR48 [R/W] B, H, W ---11111	ICR49 [R/W] B, H, W ---11111	ICR50 [R/W] B, H, W ---11111	ICR51 [R/W] B, H, W ---11111	
000474_H	Reserved				
000478_H	Reserved		ICR58 [R/W] B, H, W ---11111	ICR59 [R/W] B, H, W ---11111	

Address	Register				Block
	+0	+1	+2	+3	
$00047C_H$	Reserved	ICR61 [R/W] B, H, W ---11111	ICR62 [R/W] B, H, W ---11111	ICR63 [R/W] B, H, W ---11111	Interrupt Control
000480_H	RSRR [R/W] B, H, W 10000000	STCR [R/W] B, H, W 00110011	TBCR [R/W] B, H, W 00XXX - 00	CTBR [W] B, H, W XXXXXXXX	Clock Control
000484_H	CLKR [R/W] B, H, W ---- 0000	WPR [W] B, H, W XXXXXXXX	DIVR0 [R/W] B, H, W 00000011	DIVR1 [R/W] B, H, W 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] B, H - - - 00000	PLLDIVN [R/W] B, H - - - 00000	PLLDIVG [R/W] B, H - - - 00000	PLLMULG [W] B, H 00000000	PLL Interface
000490_H	PLLCTRL [R/W] B, H - - - - 0000	Reserved			
000494_H to $00049C_H$	Reserved				Reserved
$0004A0_H$	Reserved	WTCER [R/W] B, H - - - - - - 00	WTCR [R/W] B, H 00000000 000 - 00 - 0		Real Time Clock
$0004A4_H$	Reserved	WTBR [R/W] B, B, H - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] B, H - - - 00000	WTMR [R/W] B, H - - 000000	WTSR [R/W] B - - 000000	Reserved	
$0004AC_H$	Reserved		CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulation
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] B, H 0 - - - 0000	Reserved			CAN (Clock Control)
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	Reserved		Low Voltage Detection

Address	Register				Block
	+0	+1	+2	+3	
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilization Wait Timer
$0004CC_H$	OSCCR [R/W] - - - - - - - 0	Reserved			Main- Oscillation Standby Control
$0004D4_H$	SHDE [R/W] B 0 - - - - - - -	Reserved	EXTE [R/W] B, H 00000000	EXTF [R/W] B, H 00000000	Shutdown control
$0004D8_H$	EXTLV [R/W] B, H 00000000 00000000		Reserved		
$0004DC_H$ to $00063C_H$	Reserved				Reserved
000640_H	ASR0 [R/W] B, H, W 00000000 00000000		ACR0 [R/W] B, H, W 1111**00 00100000		External Bus Unit
000644_H	ASR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		ACR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		ACR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		ACR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		ACR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000654_H to $00065C_H$	Reserved				
000660_H	AWR0 [R/W] B, H, W 01001111 11111011		AWR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		Reserved		
$00066C_H$	Reserved				Reserved
000670_H	MCRA [R/W] B, H, W XXXXXXXX	MCRB [R/W] B, H, W XXXXXXXX	Reserved		External Bus Unit
000674_H	Reserved				
000678_H	IORW0 [R/W] B, H, W XXXXXXXX	IORW1 [R/W] B, H, W XXXXXXXX	IORW2 [R/W] B, H, W XXXXXXXX	Reserved	
$00067C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000680_H	CSER [R/W] B, H, W 00000001	CHER [R/W] B, H, W 11111111	Reserved	TCR [R/W] B, H, W 00000000	External Bus Unit
000684_H	RCRH [R/W] B, H, W 00XXXXXX	RCRL [R/W] B, H, W XXXX0XXX	Reserved		
000688_H to $0007F8_H$	Reserved				Reserved
$0007FC_H$	Reserved	MODR [W] B XXXXXXXX	Reserved		Mode Register
000800_H to $000BFC_H$	Reserved				Reserved
$000C00_H$	Reserved			IOS [R/W] 00000000	I-Unit
$000C04_H$ to $000CFC_H$	Reserved				Reserved
$000D00_H$	PDRD00 [R] B, H XXXXXXXX	PDRD01 [R] B, H XXXXXXXX	Reserved		Port Data Direct Read Register
$000D04_H$	Reserved	PDRD05 [R] B, H XXXXXXXX	PDRD06 [R] B, H XXXXXXXX	PDRD07 [R] B, H XXXXXXXX	
$000D08_H$	PDRD08 [R] B, H XXXX - - XX	PDRD09 [R] B, H - - - XXXXX	PDRD10 [R] B, H - XXXXXXX	PDRD11 [R] B, H - - - - - - XX	
$000D0C_H$	Reserved	PDRD13 [R] B, H - - - - - XXX	PDRD14 [R] B, H - - - - XXXX	PDRD15 [R] B, H - - - - XXXX	
$000D10_H$	PDRD16 [R] B, H X - - - - - - -	PDRD17 [R] B, H XXXXXXXX	PDRD18 [R] B, H - - - - - XXX	PDRD19 [R] B, H - XXX - XXX	
$000D14_H$	PDRD20 [R] B, H - XXX - XXX	PDRD21 [R] B, H - XXX - XXX	PDRD22 [R] B, H XXXXXX - X	PDRD23 [R] B, H - X - XXXXX	
$000D18_H$	PDRD24 [R] B, H XXXXXXXX	Reserved			
$000D1C_H$	PDRD28 [R] B, H XXXXXXXX	PDRD29 [R] B, H XXXXXXXX	Reserved		
$000D20_H$ to $000D3C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000D40_H$	DDR00 [R/W] B, H 00000000	DDR01 [R/W] B, H 00000000	Reserved		Port Direction Register
$000D44_H$	Reserved	DDR05 [R/W] B, H 00000000	DDR06 [R/W] B, H 00000000	DDR07 [R/W] B, H 00000000	
$000D48_H$	DDR08 [R/W] B, H 0000 - - 00	DDR09 [R/W] B, H - - - 00000	DDR10 [R/W] B, H - 0000000	DDR11 [R/W] B, H - - - - - - 00	
$000D4C_H$	Reserved	DDR13 [R/W] B, H - - - - - 000	DDR14 [R/W] B, H - - - - 0000	DDR15 [R/W] B, H - - - - 0000	
$000D50_H$	DDR16 [R/W] B, H 0 - - - - - - -	DDR17 [R/W] B, H 00000000	DDR18 [R/W] B, H - - - - - 000	DDR19 [R/W] B, H - 000 - 000	
$000D54_H$	DDR20 [R/W] B, H - 000 - 000	DDR21 [R/W] B, H - 000 - 000	DDR22 [R/W] B, H 000000 - 0	DDR23 [R/W] B, H - 0 - 00000	
$000D58_H$	DDR24 [R/W] B, H 00000000	Reserved			
$000D5C_H$	DDR28 [R/W] B, H 00000000	DDR29 [R/W] B, H 00000000	Reserved		
$000D60_H$ to $000D7C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000D80_H$	PFR00 [R/W] B, H 11111111	PFR01 [R/W] B, H 11111111	Reserved		Port Function Register
$000D84_H$	Reserved	PFR05 [R/W] B, H 11111111	PFR06 [R/W] B, H 11111111	PFR07 [R/W] B, H 11111111	
$000D88_H$	PFR08 [R/W] B, H 1111 - - 11	PFR09 [R/W] B, H - - - 11111	PFR10 [R/W] B, H - 1111111	PFR11 [R/W] B, H - - - - - - 00	
$000D8C_H$	Reserved	PFR13 [R/W] B, H - - - - - 000	PFR14 [R/W] B, H - - - - 0000	PFR15 [R/W] B, H - - - - 0000	
$000D90_H$	PFR16 [R/W] B, H 0 - - - - - - -	PFR17 [R/W] B, H 00000000	PFR18 [R/W] B, H - - - - - 000	PFR19 [R/W] B, H - 000 - 000	
$000D94_H$	PFR20 [R/W] B, H - 000 - 000	PFR21 [R/W] B, H - 000 - 000	PFR22 [R/W] B, H 000000 - 0	PFR23 [R/W] B, H - 0 - 00000	
$000D98_H$	PFR24 [R/W] B, H 00000000	Reserved			
$000D9C_H$	PFR28 [R/W] B, H 00000000	PFR29 [R/W] B, H 00000000	Reserved		
$000DA0_H$ to $000DC4_H$	Reserved				Reserved
$000DC8_H$	Reserved		EPFR10 [R/W] B, H - - 00 - - - 0	Reserved	Extended Port Function Register
$000DCC_H$	Reserved	EPFR13 [R/W] B, H - - - - - 0 - -	EPFR14 [R/W] B, H - - - - 0000	EPFR15 [R/W] B, H - - - - 0000	
$000DD0_H$	EPFR16 [R/W] B, H 0 - - - - - - -	Reserved	EPFR18 [R/W] B, H - - - - - 0 - -	EPFR19 [R/W] B, H - 0 - - - 0 - -	
$000DD4_H$	EPFR20 [R/W] B, H - 0 - - - 0 - -	EPFR21 [R/W] B, H - 0 - - - 0 - -	Reserved		
$000DD8_H$, $000DDC_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000DE0_H$ to $000DFC_H$	Reserved				Reserved
$000E00_H$	PODR00 [R/W] B, H 00000000	PODR01 [R/W] B, H 00000000	Reserved		Port Output Select Register
$000E04_H$	Reserved	PODR05 [R/W] B, H 00000000	PODR06 [R/W] B, H 00000000	PODR07 [R/W] B, H 00000000	
$000E08_H$	PODR08 [R/W] B, H 0000 - - 00	PODR09 [R/W] B, H - - - 00000	PODR10 [R/W] B, H - 0000000	PODR11 [R/W] B, H - - - - - - 00	
$000E0C_H$	Reserved	PODR13 [R/W] B, H - - - - - 000	PODR14 [R/W] B, H - - - - 0000	PODR15 [R/W] B, H - - - - 0000	
$000E10_H$	PODR16 [R/W] B, H 0 - - - - - - -	PODR17 [R/W] B, H 00000000	PODR18 [R/W] B, H - - - - - 000	PODR19 [R/W] B, H - 000 - 000	
$000E14_H$	PODR20 [R/W] B, H - 000 - 000	PODR21 [R/W] B, H - 000 - 000	PODR22 [R/W] B, H - - - - 00 - 0	PODR23 [R/W] B, H - 0 - 00000	
$000E18_H$	PODR24 [R/W] B, H 00000000	Reserved			
$000E1C_H$	PODR28 [R/W] B, H 00000000	PODR29 [R/W] B, H 00000000	Reserved		
$000E20_H$ to $000E3C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000E40_H$	PILR00 [R/W] B, H 00000000	PILR01 [R/W] B, H 00000000	Reserved		Input Level Select Register
$000E44_H$	Reserved	PILR05 [R/W] B, H 00000000	PILR06 [R/W] B, H 00000000	PILR07 [R/W] B, H 00000000	
$000E48_H$	PILR08 [R/W] B, H 0000 - - 00	PILR09 [R/W] B, H - - - 00000	PILR10 [R/W] B, H - 0000000	PILR11 [R/W] B, H - - - - - - 00	
$000E4C_H$	Reserved	PILR13 [R/W] B, H - - - - - 000	PILR14 [R/W] B, H - - - - 0000	PILR15 [R/W] B, H - - - - 0000	
$000E50_H$	PILR16 [R/W] B, H 0 - - - - - - -	PILR17 [R/W] B, H 00000000	PILR18 [R/W] B, H - - - - - 000	PILR19 [R/W] B, H - 000 - 000	
$000E54_H$	PILR20 [R/W] B, H - 000 - 000	PILR21 [R/W] B, H - 000 - 000	PILR22 [R/W] B, H 000000 - 0	PILR23 [R/W] B, H - 0 - 00000	
$000E58_H$	PILR24 [R/W] B, H 00000000	Reserved			
$000E5C_H$	PILR28 [R/W] B, H 00000000	PILR29 [R/W] B, H 00000000	Reserved		
$000E60_H$ to $000E7C_H$	Reserved				Reserved
$000E80_H$ to $000E88_H$	Reserved				Port Input Level Select Register
$000E8C_H$	Reserved		EPILR14 [R/W] B, H - - - - 0000	EPILR15 [R/W] B, H - - - - 0000	
$000E90_H$	Reserved	EPILR17 [R/W] B, H - - - - 0000	EPILR18 [R/W] B, H 000000 - 0	EPILR19 [R/W] B, H - 000 - 000	
$000E94_H$	EPILR20 [R/W] B, H - 000 - 000	EPILR21 [R/W] B, H - 000 - 000	EPILR22 [R/W] B, H - - - - 00 - 0	EPILR23 [R/W] B, H - 0 - 00000	
$000E98_H$	EPILR24 [R/W] B, H 00 - - 0000	Reserved			

Address	Register				Block
	+0	+1	+2	+3	
$000E9C_H$ to $000EBC_H$	Reserved				Reserved
$000EC0_H$	PPER00 [R/W] B, H 00000000	PPER01 [R/W] B, H 00000000	Reserved		Port Pull-Up/Pull-Down Enable Register
$000EC4_H$	Reserved	PPER05 [R/W] B, H 00000000	PPER06 [R/W] B, H 00000000	PPER07 [R/W] B, H 00000000	
$000EC8_H$	PPER08 [R/W] B, H 0000 - - 00	PPER09 [R/W] B, H - - - 00000	PPER10 [R/W] B, H - 0000000	PPER11 [R/W] B, H - - - - - - 00	
$000ECC_H$	Reserved	PPER13 [R/W] B, H - - - - - 000	PPER14 [R/W] B, H - - - - 0000	PPER15 [R/W] B, H - - - - 0000	
$000ED0_H$	PPER16 [R/W] B, H 0 - - - - - - -	PPER17 [R/W] B, H 00000000	PPER18 [R/W] B, H - - - - - 000	PPER19 [R/W] B, H - 000 - 000	
$000ED4_H$	PPER20 [R/W] B, H - 000 - 000	PPER21 [R/W] B, H - 000 - 000	PPER22 [R/W] B, H - - - - 00 - 0	PPER23 [R/W] B, H - 0 - 00000	
$000ED8_H$	PPER24 [R/W] B, H 00 - - 0000	Reserved			
$000EDC_H$	PPER28 [R/W] B, H 00000000	PPER29 [R/W] B, H 00000000	Reserved		
$000EE0_H$ to $000EFC_H$	Reserved				Reserved
$000F00_H$	PPCR00 [R/W] B, H 11111111	PPCR01 [R/W] B, H 11111111	Reserved		Port Pull-Up/Pull-Down Control Register
$000F04_H$	Reserved	PPCR05 [R/W] B, H 11111111	PPCR06 [R/W] B, H 11111111	PPCR07 [R/W] B, H 11111111	
$000F08_H$	PPCR08 [R/W] B, H 1111 - -11	PPCR09 [R/W] B, H - - - 11111	PPCR10 [R/W] B, H - 1111111	PPCR11 [R/W] B, H - - - - - -11	

Address	Register				Block
	+0	+1	+2	+3	
$000F0C_H$	Reserved	PPCR13 [R/W] B, H - - - - - 111	PPCR14 [R/W] B, H - - - - 1111	PPCR15 [R/W] B, H - - - - 1111	Port Pull-Up/Pull-Down Control Register
$000F10_H$	PPCR16 [R/W] B, H 1 - - - - - - -	PPCR17 [R/W] B, H 11111111	PPCR18 [R/W] B, H - - - - - 111	PPCR19 [R/W] B, H - 111 - 111	
$000F14_H$	PPCR20 [R/W] B, H - 111 - 111	PPCR21 [R/W] B, H - 111 - 111	PPCR22 [R/W] B, H 111111 - 1	PPCR23 [R/W] B, H - 1 - 11111	
$000F18_H$	PPCR24 [R/W] B, H 11 - - 1111	Reserved			
$000F1C_H$	PPCR28 [R/W] B, H 11111111	PPCR29 [R/W] B, H 11111111	Reserved		
$000F20_H$ to $000F3C_H$	Reserved				Reserved
001000_H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $005FFC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
006000_H to $006FFC_H$	Reserved				Reserved
007000_H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - - 00000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - - 00000 00000000 00000000				
007014_H to $00BFFC_H$	Reserved				Reserved
$00C000_H$	CTRLR0 [R/W] B, H 00000000 00000001		STATR0 [R/W] B, H 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] B, H, W 00000000 00000000		BTR0 [R/W] B, H, W 00100011 00000001		
$00C008_H$	INTR0 [R] B, H, W 00000000 00000000		TESTR0 [R/W] B, H, W 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] B, H, W 00000000 00000000		Reserved		
$00C010_H$	IF1CREQ0 [R/W] B, H 00000000 00000001		IF1CMSK0 [R/W] B, H 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] B, H, W 11111111 11111111		IF1MSK10 [R/W] B, H, W 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] B, H, W 00000000 00000000		IF1ARB10 [R/W] B, H, W 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] B, H, W 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] B, H, W 00000000 00000000		IF1DTA20 [R/W] B, H, W 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] B, H 00000000 00000000		IF1DTB20 [R/W] B, H 00000000 00000000		
$00C028_H$, $00C02C_H$	Reserved				
$00C030_H$	IF1DTA20 [R/W] B, H, W 00000000 00000000		IF1DTA10 [R/W] B, H, W 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C034_H$	IF1DTB20 [R/W] B, H, W 00000000 00000000		IF1DTB10 [R/W] B, H, W 00000000 00000000		CAN 0 IF 1 Register
$00C038_H$, $00C03C_H$	Reserved				
$00C040_H$	IF2CREQ0 [R/W] B, H 00000000 00000001		IF2CMSK0 [R/W] B, H 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] B, H, W 11111111 11111111		IF2MSK10 [R/W] B, H, W 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] B, H, W 00000000 00000000		IF2ARB10 [R/W] B, H, W 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] B, H, W 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] B, H, W 00000000 00000000		IF2DTA20 [R/W] B, H, W 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] B, H, W 00000000 00000000		IF2DTB20 [R/W] B, H, W 00000000 00000000		
$00C058_H$, $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] B, H, W 00000000 00000000		IF2DTA10 [R/W] B, H, W 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] B, H, W 00000000 00000000		IF2DTB10 [R/W] B, H, W 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				
$00C080_H$	TREQR20 [R] B, H, W 00000000 00000000		TREQR10 [R] B, H, W 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved				
$00C090_H$	NEWDT20 [R] B, H, W 00000000 00000000		NEWDT10 [R] B, H, W 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved				
$00C0A0_H$	INTPND20 [R] B, H, W 00000000 00000000		INTPND10 [R] B, H, W 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C0A4_H$ to $00C0AC_H$	Reserved				CAN 0 Status Flags
$00C0B0_H$	MSGVAL20 [R] B, H, W 00000000 00000000		MSGVAL10 [R] B, H, W 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved				Reserved
$00C100_H$	CTRLR1 [R/W] B, H 00000000 00000001		STATR1 [R/W] B, H 00000000 00000000		CAN 1 Control Register
$00C104_H$	ERRCNT1 [R] B, H, W 00000000 00000000		BTR1 [R/W] B, H, W 00100011 00000001		
$00C108_H$	INTR1 [R] B, H, W 00000000 00000000		TESTR1 [R/W] B, H, W 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] B, H, W 00000000 00000000		Reserved		
$00C110_H$	IF1CREQ1 [R/W] B, H 00000000 00000001		IF1CMSK1 [R/W] B, H 00000000 00000000		CAN 1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] B, H, W 11111111 11111111		IF1MSK11 [R/W] B, H, W 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] B, H, W 00000000 00000000		IF1ARB11 [R/W] B, H, W 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] B, H, W 00000000 00000000		Reserved		
$00C120_H$	IF1DTA11 [R/W] B, H, W 00000000 00000000		IF1DTA21 [R/W] B, H, W 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] B, H, W 00000000 00000000		IF1DTB21 [R/W] B, H, W 00000000 00000000		
$00C128_H$, $00C12C_H$	Reserved				
$00C130_H$	IF1DTA21 [R/W] B, H, W 00000000 00000000		IF1DTA11 [R/W] B, H, W 00000000 00000000		
$00C134_H$	IF1DTB21 [R/W] B, H, W 00000000 00000000		IF1DTB11 [R/W] B, H, W 00000000 00000000		
$00C138_H$, $00C13C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C140_H$	IF2CREQ1 [R/W] B, H 00000000 00000001		IF2CMSK1 [R/W] B, H 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] B, H, W 11111111 11111111		IF2MSK11 [R/W] B, H, W 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] B, H, W 00000000 00000000		IF2ARB11 [R/W] B, H, W 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] B, H, W 00000000 00000000		Reserved		
$00C150_H$	IF2DTA11 [R/W] B, H, W 00000000 00000000		IF2DTA21 [R/W] B, H, W 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] B, H, W 00000000 00000000		IF2DTB21 [R/W] B, H, W 00000000 00000000		
$00C158_H$, $00C15C_H$	Reserved				
$00C160_H$	IF2DTA21 [R/W] B, H, W 00000000 00000000		IF2DTA11 [R/W] B, H, W 00000000 00000000		
$00C164_H$	IF2DTB21 [R/W] B, H, W 00000000 00000000		IF2DTB11 [R/W] B, H, W 00000000 00000000		
$00C168_H$ to $00C17C_H$	Reserved				
$00C180_H$	TREQR21 [R] B, H, W 00000000 00000000		TREQR11 [R] B, H, W 00000000 00000000		CAN 1 Status Flags
$00C184_H$	TREQR41 [R] B, H, W 00000000 00000000		TREQR31 [R] B, H, W 00000000 00000000		
$00C188_H$, $00C18C_H$	Reserved				
$00C190_H$	NEWDT21 [R] B, H, W 00000000 00000000		NEWDT11 [R] B, H, W 00000000 00000000		
$00C194_H$	NEWDT41 [R] B, H, W 00000000 00000000		NEWDT31 [R] B, H, W 00000000 00000000		
$00C198_H$, $00C19C_H$	Reserved				
$00C1A0_H$	INTPND21 [R] B, H, W 00000000 00000000		INTPND11 [R] B, H, W 00000000 00000000		
$00C1A4_H$	INTPND41 [R] B, H, W 00000000 00000000		INTPND31 [R] B, H, W 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C1A8_H$, $00C1AC_H$	Reserved				CAN 1 Status Flags
$00C1B0_H$	MSGVAL21 [R] B, H, W 00000000 00000000		MSGVAL11 [R] B, H, W 00000000 00000000		
$00C1B4_H$	MSGVAL41 [R] B, H, W 00000000 00000000		MSGVAL31 [R] B, H, W 00000000 00000000		
$00C1B8_H$ to $00EFFC_H$	Reserved				
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				Reserved
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ to $027FFC_H$	Reserved				Reserved
024000_H to $02BFFC_H$	D-RAM 32 Kbytes: 024000_H to $02BFFC_H$ (data: 1 wait)				D-RAM 32 Kbytes
$02C000_H$ to $02FFFC_H$	D-RAM 16 Kbytes: $02C000_H$ to $02FFFC_H$ (data: 0 wait)				D-RAM 16 Kbytes
030000_H to $033FFC_H$	I-/D-RAM size is 16 Kbytes: 030000_H to $033FFC_H$ (instruction: 0 wait, data: 1 wait)				I-/D-RAM 16 Kbytes
034000_H to $03FFFC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
040000_H to $05FFFC_H$	ROMS00 area (128 Kbytes)				Memory area
060000_H to $07FFFC_H$	ROMS01 area (128 Kbytes)				
080000_H to $09FFFC_H$	ROMS02 area (128 Kbytes)				
$0A0000_H$ to $0BFFFC_H$	ROMS03 area (128 Kbytes)				
$0C0000_H$ to $0DFFFC_H$	ROMS04 area (128 Kbytes)				
$0E0000_H$ to $0FFFF4_H$	ROMS05 area (128 Kbytes)				
$0FFFF8_H$	Mode Vector				Reset/Mode Vector
$0FFFFC_H$	Reset Vector				
100000_H to $13FFFC_H$	ROMS06 area (256 Kbytes)				Memory area
140000_H to $17FFFC_H$	ROMS07 area (256 Kbytes)				
180000_H to $4FFFFC_H$	Reserved				Reserved

1. The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed in bytes.

11. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level		Interrupt vector[1]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	–	–	$3FC_H$	$000FFFFC_H$	
Mode vector	1	01	–	–	$3F8_H$	$000FFFF8_H$	
System reserved	2	02	–	–	$3F4_H$	$000FFFF4_H$	
System reserved	3	03	–	–	$3F0_H$	$000FFFF0_H$	
System reserved	4	04	–	–	$3EC_H$	$000FFFEC_H$	
CPU supervisor mode (INT #5 instruction)	5	05	–	–	$3E8_H$	$000FFFE8_H$	
Memory Protection exception	6	06	–	–	$3E4_H$	$000FFFE4_H$	
System reserved	7	07	–	–	$3E0_H$	$000FFFE0_H$	
System reserved	8	08	–	–	$3DC_H$	$000FFFDC_H$	
INTE instruction	9	09	–	–	$3D8_H$	$000FFFD8_H$	
System reserved	10	0A	–	–	$3D4_H$	$000FFFD4_H$	
System reserved	11	0B	–	–	$3D0_H$	$000FFFD0_H$	
System reserved	12	0C	–	–	$3CC_H$	$000FFFCC_H$	
System reserved	13	0D	–	–	$3C8_H$	$000FFFC8_H$	
Undefined instruction exception	14	0E	–	–	$3C4_H$	$000FFFC4_H$	
NMI request	15	0F	15 (F_H) fixed		$3C0_H$	$000FFFC0_H$	
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	
External Interrupt 9	25	19			398_H	$000FFF98_H$	
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	
External Interrupt 11	27	1B			390_H	$000FFF90_H$	

Interrupt	Interrupt number		Interrupt level		Interrupt vector[1]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	
External Interrupt 13	29	1D			388_H	$000FFF88_H$	
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	
External Interrupt 15	31	1F			380_H	$000FFF80_H$	
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4
Reload Timer 1	33	21			378_H	$000FFF78_H$	5
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	
Reload Timer 3	35	23			370_H	$000FFF70_H$	
System reserved	36	24	ICR10	$44A_H$	$36C_H$	$000FFF6C_H$	
System reserved	37	25			368_H	$000FFF68_H$	
System reserved	38	26	ICR11	$44B_H$	364_H	$000FFF64_H$	
Reload Timer 7	39	27			360_H	$000FFF60_H$	
Free Run Timer 0	40	28	ICR12	$44C_H$	$35C_H$	$000FFF5C_H$	
Free Run Timer 1	41	29			358_H	$000FFF58_H$	
Free Run Timer 2	42	2A	ICR13	$44D_H$	354_H	$000FFF54_H$	
Free Run Timer 3	43	2B			350_H	$000FFF50_H$	
System reserved	44	2C	ICR14	$44E_H$	$34C_H$	$000FFF4C_H$	
System reserved	45	2D			348_H	$000FFF48_H$	
System reserved	46	2E	ICR15	$44F_H$	344_H	$000FFF44_H$	
System reserved	47	2F			340_H	$000FFF40_H$	
CAN 0	48	30	ICR16	450_H	$33C_H$	$000FFF3C_H$	
CAN 1	49	31			338_H	$000FFF38_H$	
System reserved	50	32	ICR17	451_H	334_H	$000FFF34_H$	
System reserved	51	33			330_H	$000FFF30_H$	
System reserved	52	34	ICR18	452_H	$32C_H$	$000FFF2C_H$	
System reserved	53	35			328_H	$000FFF28_H$	
LIN-USART 0 RX	54	36	ICR19	453_H	324_H	$000FFF24_H$	6
LIN-USART 0 TX	55	37			320_H	$000FFF20_H$	7
LIN-USART 1 RX	56	38	ICR20	454_H	$31C_H$	$000FFF1C_H$	8
LIN-USART 1 TX	57	39			318_H	$000FFF18_H$	9
LIN-USART 2 RX	58	3A	ICR21	455_H	314_H	$000FFF14_H$	
LIN-USART 2 TX	59	3B			310_H	$000FFF10_H$	
LIN-USART 3 RX	60	3C	ICR22	456_H	$30C_H$	$000FFF0C_H$	
LIN-USART 3 TX	61	3D			308_H	$000FFF08_H$	

Interrupt	Interrupt number		Interrupt level		Interrupt vector[1]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved	62	3E	ICR23[3]	457_H	304_H	$000FFF04_H$	
Delayed Interrupt	63	3F			300_H	$000FFF00_H$	
System reserved[2]	64	40	(ICR24)	(458_H)	$2FC_H$	$000FFEFC_H$	
System reserved[2]	65	41			$2F8_H$	$000FFEF8_H$	
LIN-USART 4 RX	66	42	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10
LIN-USART 4 TX	67	43			$2F0_H$	$000FFEF0_H$	11
LIN-USART 5 RX	68	44	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12
LIN-USART 5 TX	69	45			$2E8_H$	$000FFEE8_H$	13
LIN-USART 6 RX	70	46	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	
LIN-USART 6 TX	71	47			$2E0_H$	$000FFEE0_H$	
System reserved	72	48	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	
System reserved	73	49			$2D8_H$	$000FFED8_H$	
I^2C 0 / I^2C 2	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	
I^2C 1	75	4B			$2D0_H$	$000FFED0_H$	
System reserved	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	
System reserved	77	4D			$2C8_H$	$000FFEC8_H$	
System reserved	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	
System reserved	79	4F			$2C0_H$	$000FFEC0_H$	
System reserved	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	
System reserved	81	51			$2B8_H$	$000FFEB8_H$	
System reserved	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	
System reserved	83	53			$2B0_H$	$000FFEB0_H$	
System reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	
System reserved	85	55			$2A8_H$	$000FFEA8_H$	
System reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	
System reserved	87	57			$2A0_H$	$000FFEA0_H$	
System reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	
System reserved	89	59			298_H	$000FFE98_H$	
System reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	
System reserved	91	5B			290_H	$000FFE90_H$	
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	
Input Capture 1	93	5D			288_H	$000FFE88_H$	
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	
Input Capture 3	95	5F			280_H	$000FFE80_H$	

Interrupt	Interrupt number		Interrupt level		Interrupt vector[1]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved	96	60	ICR40	468_H	$27C_H$	$000FFE7C_H$	
System reserved	97	61			278_H	$000FFE78_H$	
System reserved	98	62	ICR41	469_H	274_H	$000FFE74_H$	
System reserved	99	63			270_H	$000FFE70_H$	
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	
Output Compare 1	101	65			268_H	$000FFE68_H$	
Output Compare 2	102	66	ICR43	$46B_H$	264_H	$000FFE64_H$	
Output Compare 3	103	67			260_H	$000FFE60_H$	
System reserved	104	68	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	
System reserved	105	69			258_H	$000FFE58_H$	
System reserved	106	6A	ICR45	$46D_H$	254_H	$000FFE54_H$	
System reserved	107	6B			250_H	$000FFE50_H$	
System reserved	108	6C	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	
System reserved	109	6D			248_H	$000FFE48_H$	
System reserved	110	6E	ICR47[3]	$46F_H$	244_H	$000FFE44_H$	
System reserved	111	6F			240_H	$000FFE40_H$	
Prog. Pulse Gen. 0	112	70	ICR48	470_H	$23C_H$	$000FFE3C_H$	15
Prog. Pulse Gen. 1	113	71			238_H	$000FFE38_H$	
Prog. Pulse Gen. 2	114	72	ICR49	471_H	234_H	$000FFE34_H$	
Prog. Pulse Gen. 3	115	73			230_H	$000FFE30_H$	
Prog. Pulse Gen. 4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	
Prog. Pulse Gen. 5	117	75			228_H	$000FFE28_H$	
Prog. Pulse Gen. 6	118	76	ICR51	473_H	224_H	$000FFE24_H$	
Prog. Pulse Gen. 7	119	77			220_H	$000FFE20_H$	
System reserved	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	
System reserved	121	79			218_H	$000FFE18_H$	
System reserved	122	7A	ICR53	475_H	214_H	$000FFE14_H$	
System reserved	123	7B			210_H	$000FFE10_H$	
System reserved	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	
System reserved	125	7D			208_H	$000FFE08_H$	
System reserved	126	7E	ICR55	477_H	204_H	$000FFE04_H$	
System reserved	127	7F			200_H	$000FFE00_H$	
System reserved	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	
System reserved	129	81			$1F8_H$	$000FFDF8_H$	

Interrupt	Interrupt number		Interrupt level		Interrupt vector[1]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	
System reserved	131	83			$1F0_H$	$000FFDF0_H$	
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14
System reserved	135	87			$1E0_H$	$000FFDE0_H$	
System reserved	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	
System reserved	137	89			$1D8_H$	$000FFDD8_H$	
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	
System reserved	139	8B			$1D0_H$	$000FFDD0_H$	
Timebase Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	
System reserved	144	90	–	–	$1BC_H$	000FFDBC	
Used by the INT instruction.	145 to 255	91 to FF	–	–	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	

1. The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top address of the EIT vector table. The default vector address are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset.
2. Used by REALOS
3. ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0C03 : IOS[0])

12. Electrical Characteristics

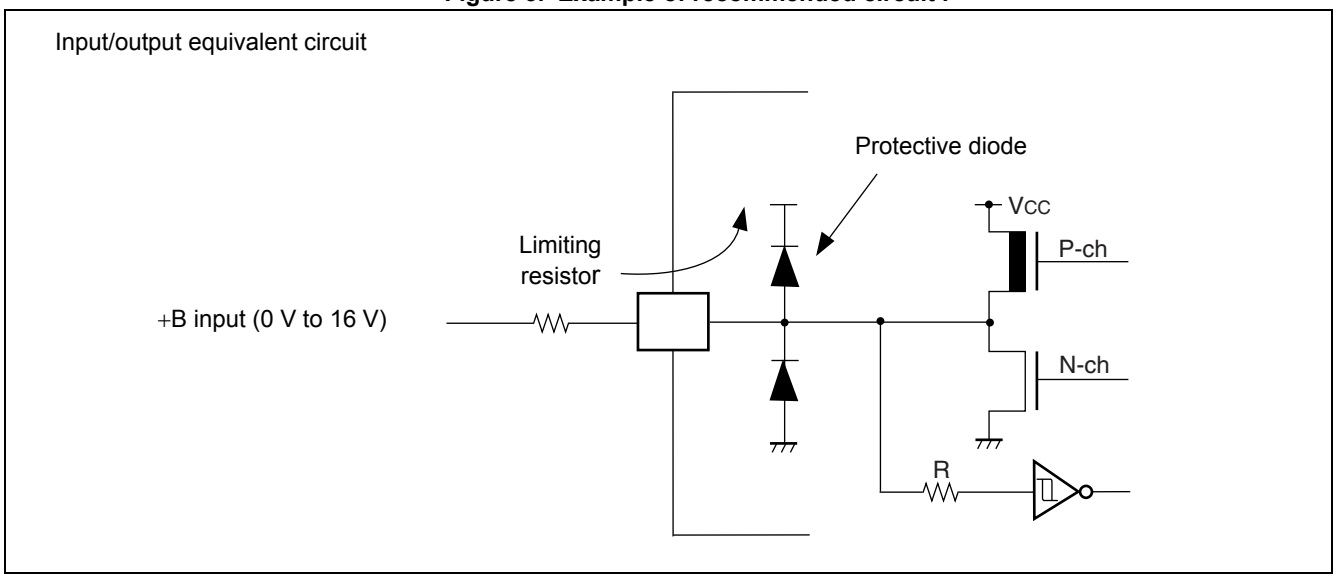
12.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage 1[1]	$V_{CC}3$	Vss − 0.5	Vss + 4.0	V	
Power supply voltage 2[1]	$V_{CC}5$	Vss − 0.5	Vss + 6.0	V	
Analog power supply voltage[1]	$AV_{CC}3$	Vss − 0.5	Vss + 4.0	V	[2]
Analog power supply voltage[1]	AVRH	Vss − 0.5	Vss + 4.0	V	[2]
Input voltage 1[1]	V_{I1}	Vss − 0.3	Vcc3 + 0.3	V	[3]
Input voltage 2[1]	V_{I2}	Vss − 0.3	Vcc5 + 0.3	V	[3]
Analog pin input voltage[1]	V_{IA}	Vss − 0.3	AVcc3 + 0.3	V	
Output voltage 1[1]	V_{O1}	Vss − 0.3	Vcc3 + 0.3	V	[3]
Output voltage 2[1]	V_{O2}	Vss − 0.3	Vcc5 + 0.3	V	[3]
Maximum clamp current	I_{CLAMP}	− 2.0	+ 2.0	mA	[4]
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	−	20	mA	[4]
“L” level maximum output current	I_{OL}	−	10	mA	[5]
“L” level average output current	I_{OLAV}	−	8	mA	[6]
“L” level total maximum output current	ΣI_{OL}	−	100	mA	
“L” level total average output current	ΣI_{OLAV}	−	50	mA	[7]
“H” level maximum output current	I_{OH}	−	− 10	mA	[5]
“H” level average output current	I_{OHAV}	−	− 4	mA	[6]
“H” level total maximum output current	ΣI_{OH}	−	− 50	mA	
“H” level total average output current	ΣI_{OHAV}	−	− 20	mA	[7]
Power consumption	P_D	−	1000	mW	
Operation ambient temperature	T_A	− 40	+ 85	°C	
Storage temperature	Tstg	− 55	+ 125	°C	

1. The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.
2. Be careful not to exceed “V_{CC} + 0.3 V”, for example, when the power is turned on. Also, do not let $AV_{CC}3$ exceed $V_{CC}3$.
3. V_I and V_O should not exceed “V_{CC} + 0.3 V”. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.
4.

- Relevant pins : Pins that are used as I/O ports or that are shared as I/O ports
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal is an input signal exceeding V_{CC} voltage. The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that, when the microcontroller drive current is low as in low power consumption mode, the +B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that, if the +B signal is input exists when the microcontroller is off (not fixed at 0 V) , power is supplied through the pin, possibly causing the microcontroller to operate imperfectly.
- Note that, if the +B input exists when the power supply is turned on, power is supplied through the pin, possibly resulting in a power-supply voltage at which a power-on reset does not work.
- Be careful not to let the +B input pin open.

Figure 3. Example of recommended circuit :



5. The maximum output current is the peak value for a single pin.
6. The average output current is the average current for a single pin over a period of 100 ms.
7. The total average output current is the average current for all pins over a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

12.2 Recommended Operating Conditions

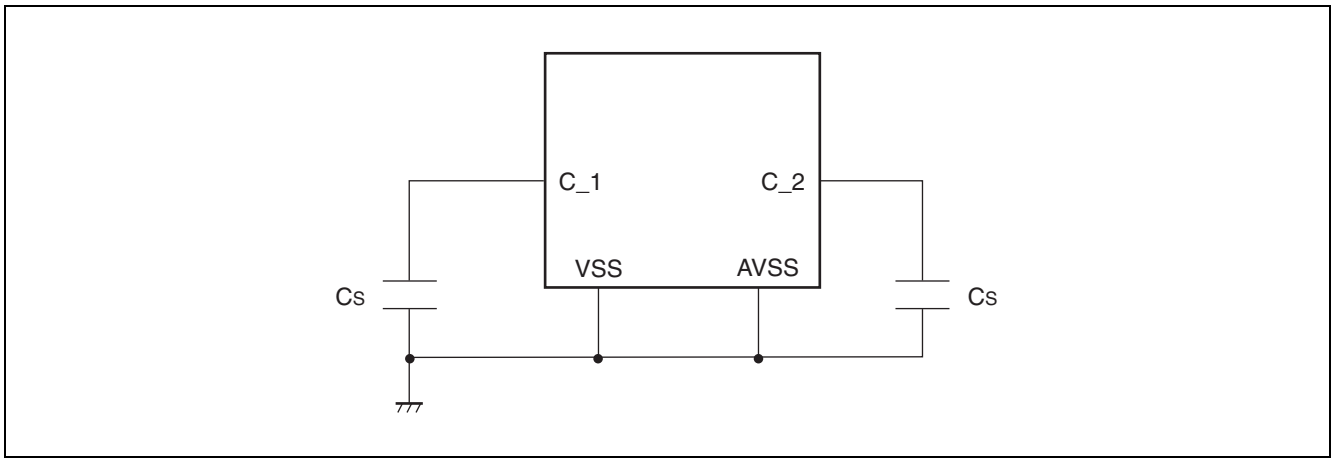
(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}5$	4.5	–	5.5	V	
	$V_{CC}3$	3.0	–	3.6	V	
	$AV_{CC}3$	3.0	–	3.6	V	
Smoothing capacitor	C_S	–	4.7 (accuracy within ± 50%)	–	µF	Use a ceramic capacitor or a capacitor having the similar frequency characteristic. For a smoothing capacitor of VCC5 pin (VCC3 pin) , use one having a capacitance value greater than C_S.
Operating temperature	T_A	− 40	–	+ 85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



12.3 DC Characteristics

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	CMOS hysteresis input	–	0.8 × V_{CC}	–	V_{CC} + 0.3	V	[2]
	V_{IH2}	CMOS hysteresis input	–	0.7 × V_{CC}	–	V_{CC} + 0.3	V	
	V_{IH3}	CMOS input	–	0.7 × V_{CC}	–	V_{CC} + 0.3	V	[1]
	V_{IH4}	Automotive input	–	0.8 × V_{CC}	–	V_{CC} + 0.3	V	
	V_{IH5}	I^2C input	–	0.7 × $V_{CC}3$	–	$V_{CC}5$ + 0.3	V	
"L" level input voltage	V_{IL1}	CMOS hysteresis input	–	V_{SS} – 0.3	–	0.2 × V_{CC}	V	[2]
	V_{IL2}	CMOS hysteresis input	–	V_{SS} – 0.3	–	0.3 × V_{CC}	V	
	V_{IL3}	CMOS input	–	V_{SS} – 0.3	–	0.3 × V_{CC}	V	[1]
	V_{IL4}	Automotive input	–	V_{SS} – 0.3	–	0.5 × V_{CC}	V	
	V_{IL5}	I^2C input	–	V_{SS} – 0.3	–	0.3 × $V_{CC}3$	V	
"H" level output voltage	V_{OH1}	3.3 V, 5 V switch pin	V_{CC} = 5.0 V, I_{OH} = 5.0 mA/ V_{CC} = 3.3 V, I_{OH} = 2.0 mA	V_{CC} – 0.5	–	–	V	
	V_{OH2}	3.3 V dedicated pin	$V_{CC}3$ = 3.3 V, I_{OH} = 4.0 mA	$V_{CC}3$ – 0.5	–	–	V	
"L" level output voltage	V_{OL1}	3.3 V, 5 V switch pin	V_{CC} = 5.0 V, I_{OL} = 5.0 mA/ V_{CC} = 3.3 V, I_{OL} = 2.0 mA	–	–	0.4	V	
	V_{OL2}	3.3 V dedicated pin	$V_{CC}3$ = 3.3 V, I_{OL} = 4.0 mA	–	–	0.4	V	
	V_{OL3}	I^2C pin	$V_{CC}3$ = 3.3 V, I_{OL} = 3.0 mA	–	–	0.4	V	
Input leak current	I_{IL}	Input pin	V_{CC} = AV_{CC} = 5.0 V, V_{SS} < VI < V_{CC}	–5	–	+ 5	µA	
Pull-up resistance value	R_{UP}	$\overline{INIT}$, pull-up pin	–	25	50	100	kΩ	

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-down resistance value	R_{DOWN}	MD3, Pull-up pin	–	25	50	100	kΩ	
Power supply current	$I_{CC}3$	VCC3	CPU core : 80 MHz, External bus : 40 MHz (no-load) , Peripheral macro : 10 MHz, CAN : 20 MHz	–	120	150	mA	
	$I_{CC}5$	VCC5	–	–	15	20	mA	
	I_{CCH}	VCC3	+ 85 °C	–	1	3	mA	At stop
	I_{CCH}	VCC3	+ 85 °C	–	10	50	μA	At shut-down
Input capacitance	C_{IN}	Except VCC, VSS, AVCC3, AVSS, AVRH	–	–	5	15	pF	

[1]: Only 3.3 V pins and MD0 pin, MD1 pin and MD2 pin as I/O power supply
[2]: Including the $\overline{INIT}$ pin, MD3 pin, and $\overline{NMI}$ pin.

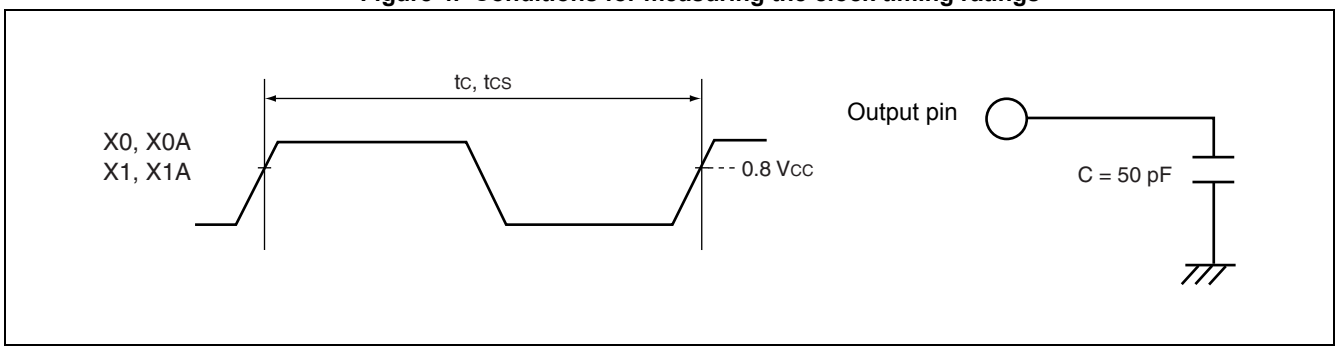
12.4 AC Characteristics

12.4.1 Clock Timing

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.4	–	4.2	MHz	Main clock
Clock cycle time	t_C	X0 X1	238	–	294	ns	
Clock frequency	f_{CS}	X0A X1A	32	–	100	kHz	Sub clock
Clock cycle time	t_{CS}	X0A X1A	10	–	31.25	µs	
Internal operation clock frequency	f_{CP}	–	0.032	–	80	MHz	CPU
	f_{CPP}		0.032	–	20	MHz	Peripheral
	f_{CPT}		0.032	–	40	MHz	External bus
	f_{CAN}		–	–	20	MHz	Clock after divided by CAN prescaler
Internal operation clock cycle time	t_{CP}	–	12.5	–	31250	ns	CPU
	t_{CPP}		50	–	31250	ns	Peripheral
	t_{CPT}		25	–	31250	ns	External bus
	t_{CAN}		50	–	–	ns	Clock after divided by CAN prescaler

Figure 4. Conditions for measuring the clock timing ratings

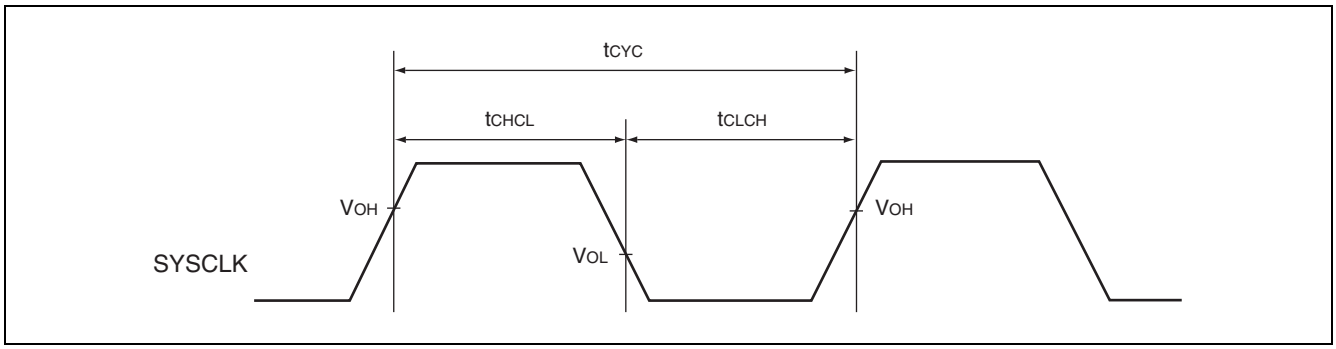


12.4.2 Clock Output Timing

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 4.5 V to 5.5 V, Vss = AVss = 0 V, T_A = - 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	–	t_{CPT}	–	ns	[1]
SYSCLK↑→SYSCLK↓	t_{CHCL}	SYSCLK		12.5	108.5	ns	
SYSCLK↓→SYSCLK↑	t_{CLCH}	SYSCLK		12.5	108.5	ns	

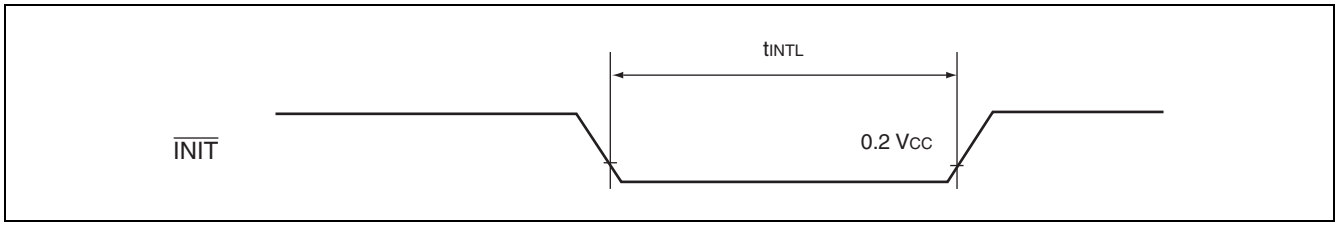
1. t_{CYC} is the frequency of 1 clock cycle.



12.4.3 Reset Input

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 4.5 V to 5.5 V, Vss = AVss = 0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
$\overline{INIT}$ input time (at power-on, at return from shutdown mode)	t_{INTL}	$\overline{INIT}$	–	8	–	ms
$\overline{INIT}$ input time (other than the above)				20	–	µs



12.4.4 Interrupt Characteristics for Recover from Shutdown

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 4.5 V to 5.5 V, Vss = AVss = 0 V, T_A = – 40 °C to + 85 °C)

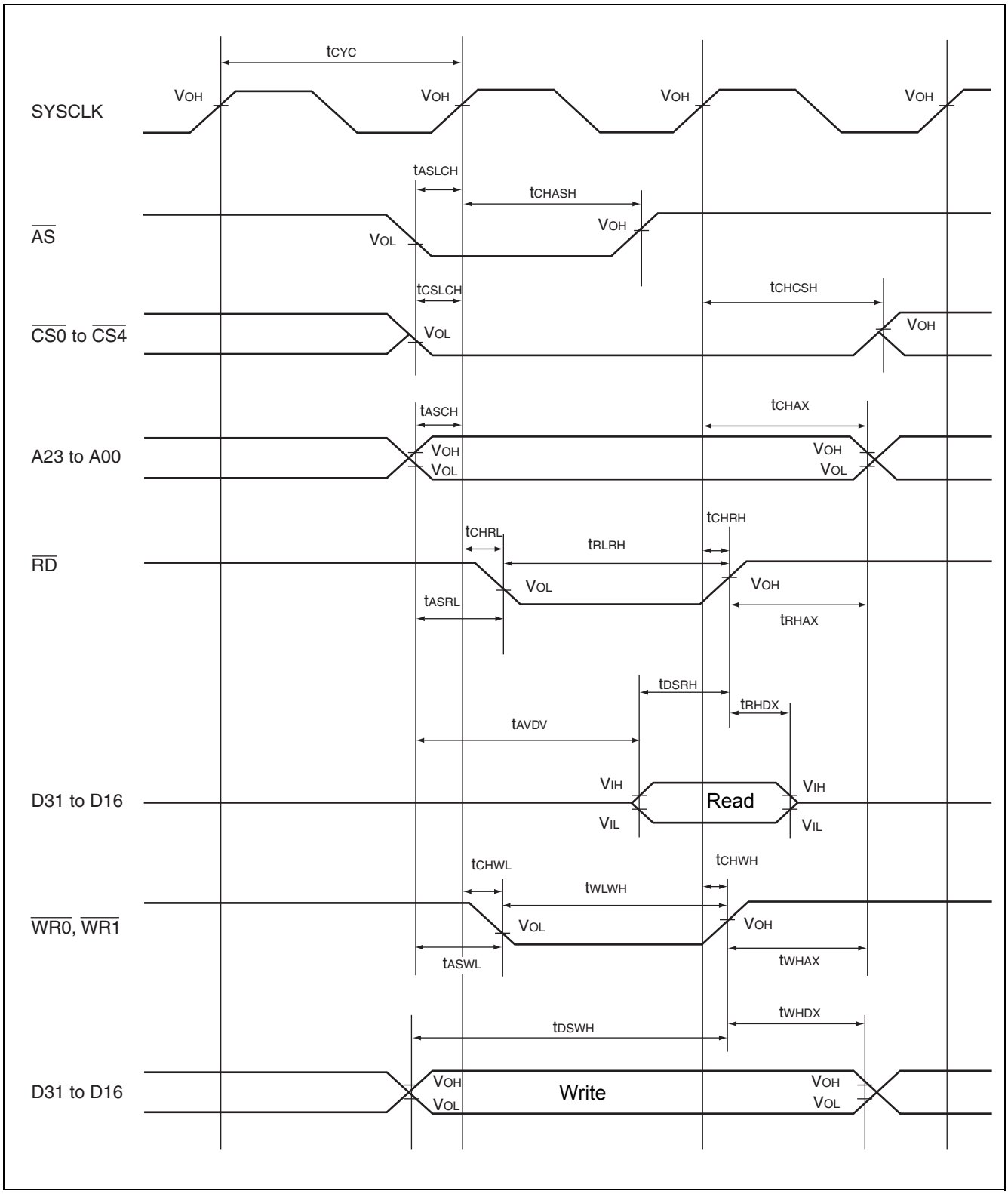
Parameter	Condition	Value		Unit
		Min	Max	
Interrupt input time (If using level interrupt during recover from shutdown)	–	500	–	µs

12.4.5 Normal Bus Access Read/write Operation

($V_{CC}3$ = 3.0 V to 3.6 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS4}$ setup	t_{CSLCH}	SYSCLK $\overline{CS0}$ to $\overline{CS4}$		3	-	ns	
	t_{CSDLCH}			- 3	-	ns	
$\overline{CS0}$ to $\overline{CS4}$ hold	t_{CHCSH}			3	$t_{CYC}/2$ + 6	ns	
Address setup	t_{ASCH}	SYSCLK A23 to A00		3	-	ns	
	t_{ASWL}	$\overline{WR0}$, $\overline{WR1}$ A23 to A00		3	-	ns	
	t_{ASRL}	$\overline{RD}$ A23 to A00		3	-	ns	
Address hold	t_{CHAX}	SYSCLK A23 to A00		3	$t_{CYC}/2$ + 6	ns	
	t_{WHAX}	$\overline{WR0}$, $\overline{WR1}$ A23 to A00		3	-	ns	
	t_{RHAX}	$\overline{RD}$ A23 to A00		3	-	ns	
Valid address/valid data input time	t_{AVDV}	A23 to A00 D31 to D16		-	3/2 × t_{CYC} - 15	ns	[1]
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	SYSCLK $\overline{WR0}$, $\overline{WR1}$		-	6	ns	
	t_{CHWH}			-	6	ns	
Data setup time ($\overline{WRn}$ rising)	t_{DSWH}	D31 to D16 $\overline{WR0}$, $\overline{WR1}$		t_{CYC} - 3	-	ns	
Data hold time ($\overline{WRn}$ rising)	t_{WHDX}	D31 to D16 $\overline{WR0}$, $\overline{WR1}$		3	-	ns	
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		t_{CYC} - 3	-	ns	
$\overline{RD}$ delay time	t_{CHRL}	SYSCLK $\overline{RD}$		-	6	ns	
	t_{CHRH}			-	6	ns	
Data setup time ($\overline{RD}$ rising)	t_{DSRH}	D31 to D16 $\overline{RD}$		20	-	ns	
Data hold time ($\overline{RD}$ rising)	t_{RHDX}	D31 to D16 $\overline{RD}$		0	-	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} - 3	-	ns	
$\overline{AS}$ setup time	t_{ASLCH}	SYSCLK $\overline{AS}$		3	-	ns	
$\overline{AS}$ hold time	t_{CHASH}			3	$t_{CYC}/2$ + 6	ns	

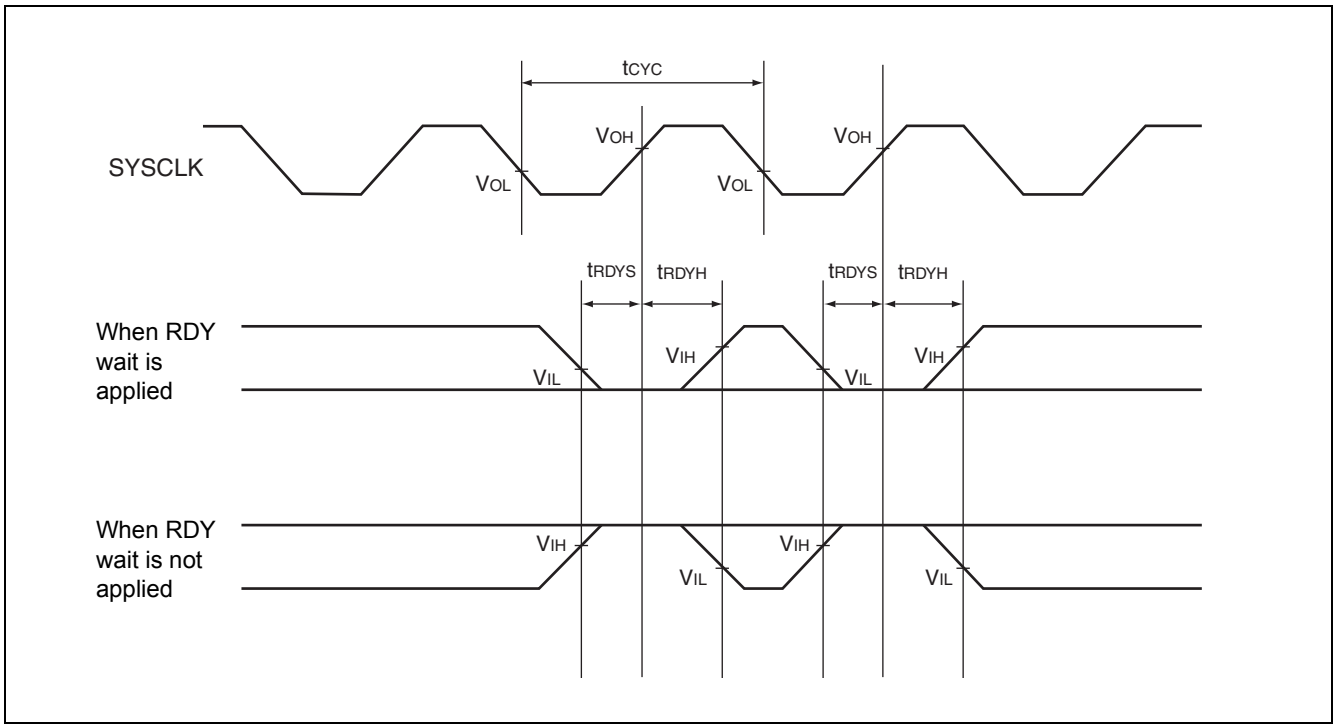
1. When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{CYC} × the number of cycles added for the delay) to this rating.


tCYC
SYSCLK
VOH
VOH
VOH
VOH
tASLCH
tCHASH
AS
VOL
VOH
tCSLCH
tCHCSH
CS0 to CS4
VOL
VOH
tASCH
tCHAX
A23 to A00
VOH
VOL
VOH
VOL
tCHRH
tCHRL
tRLRH
RD
VOL
VOH
tASRL
tRHAX
tDSRH
tRHDX
tAVDV
VIH
VIL
Read
VIH
VIL
D31 to D16
tCHWL
tCHWH
tWLWH
WR0, WR1
VOL
VOH
tASWL
tWHAX
tWHDX
tDSWH
VOH
VOL
Write
VOH
VOL
D31 to D16

12.4.6 Ready Input Timing

($V_{CC}3$ = 3.0 V to 3.6 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
RDY setup time→ SYSCLK↓	t_{RDYS}	SYSCLK RDY	-	10	-	ns
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK RDY		0	-	ns

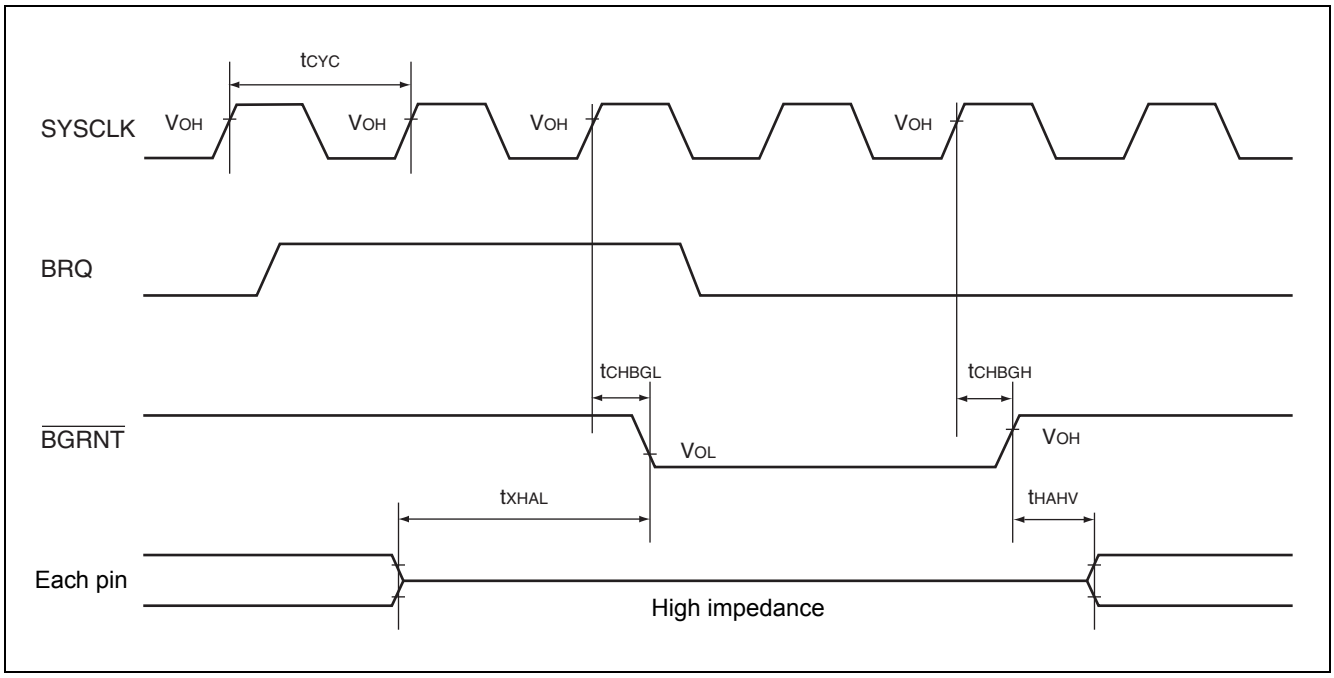


12.4.7 Hold Timing

($V_{CC}3$ = 3.0 V to 3.6 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	SYSCLK $\overline{\text{BGRNT}}$	–	–	10	ns
	t_{CHBGH}			3	10	ns
$\overline{\text{BGRNT}}$ rising from pin floating	t_{XHAL}	–		t_{CYC} – 10	t_{CYC} + 10	ns
$\overline{\text{BGRNT}}$ rising from pin valid	t_{HAHV}	$\overline{\text{BGRNT}}$		t_{CYC} – 10	t_{CYC} + 10	ns

Note: After a BRQ is captured, a minimum of 1 cycle is required before $\overline{\text{BGRNT}}$ changes.



12.4.8 LIN-USART Timing

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 4.5 V to 5.5 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK6	Internal shift clock mode	$5t_{CYCP}$	-	ns
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK6, SOT0 to SOT6		- 50	+ 50	ns
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK6, SIN0 to SIN6		t_{CYCP} + 80	-	ns
SCK↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK6, SIN0 to SIN6		0	-	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK6	External shift clock mode	t_{CYCP} + 10	-	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK6		$3t_{CYCP}$	-	ns
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK6, SOT0 to SOT6		-	150	ns
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK6, SIN0 to SIN6		30	-	ns
SCK↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK6, SIN0 to SIN6		t_{CYCP} + 30	-	ns
SCK rising time	t_F	SCK0 to SCK6		-	10	ns
SCK falling time	t_R	SCK0 to SCK6		-	10	ns

Notes:

- Above values are AC characteristics for CLK synchronous mode.
- t_{CYCP} is the cycle time of the peripheral clock.

Figure 5. Internal shift clock mode

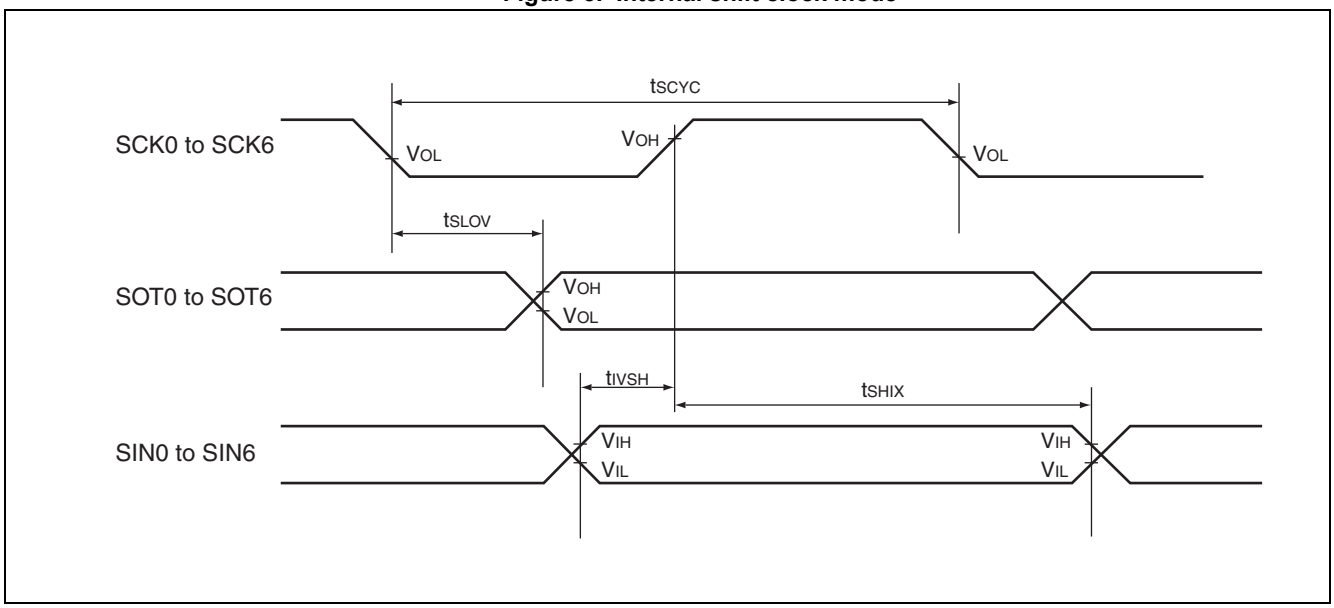
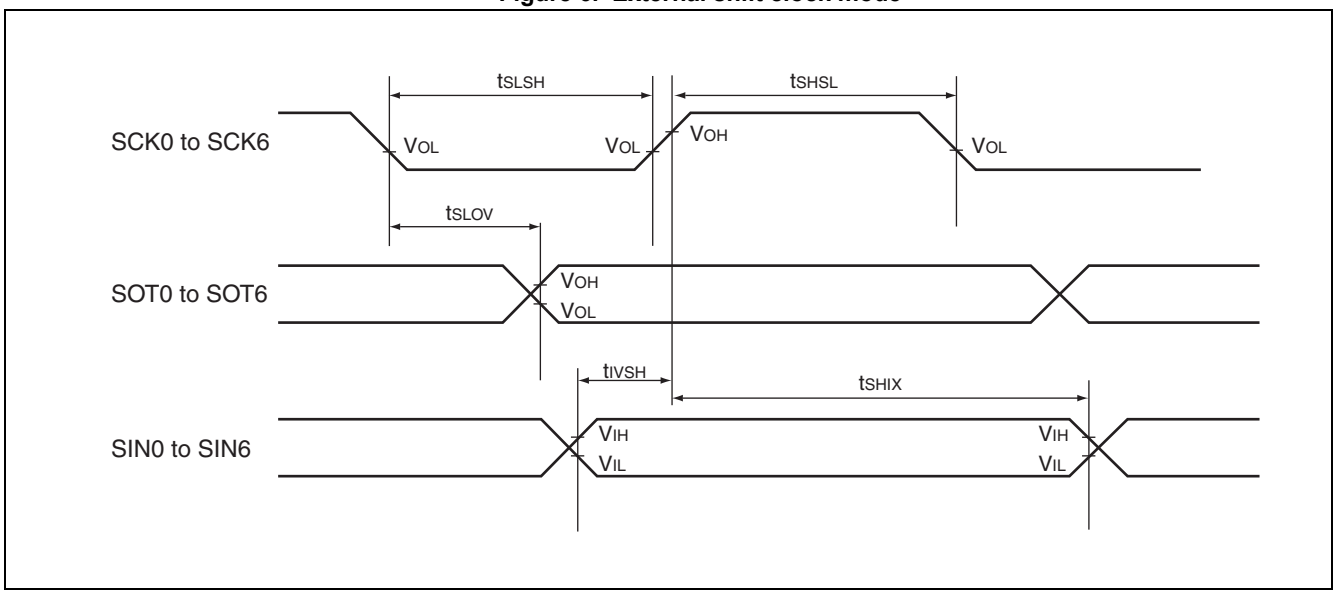


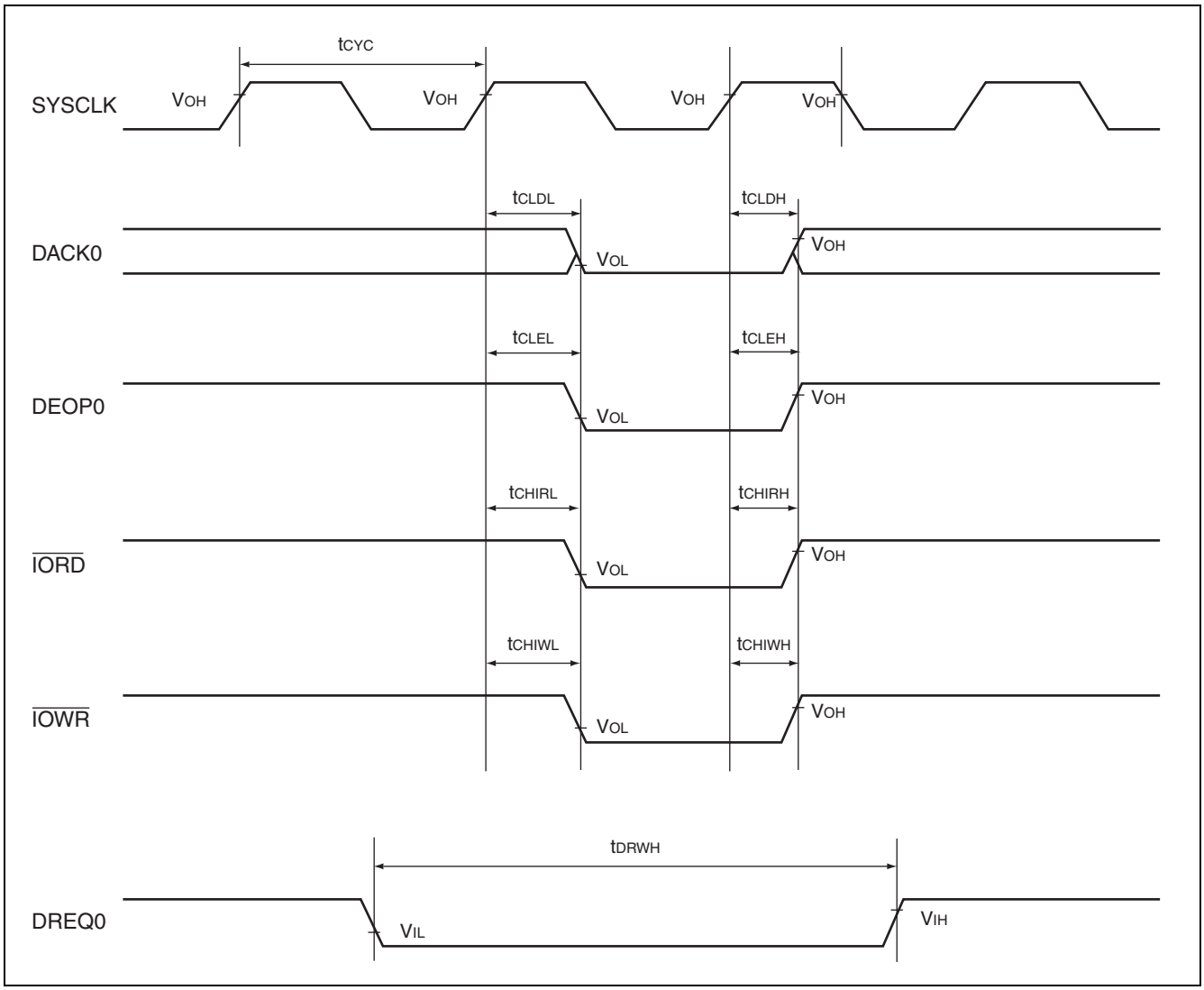
Figure 6. External shift clock mode



12.4.9 DMA Controller Timing

($V_{CC}3$ = 3.0 V to 3.6 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
DREQ0 input pulse	t_{DRWH}	DREQ0	–	–	10	ns
DACK0 delay time	t_{CLDL}	DACK0		–	10	ns
	t_{CLDH}			–	10	ns
DEOP0 delay time	t_{CLEL}	DEOP0		–	10	ns
	t_{CLEH}			–	10	ns
$\overline{IORD}$ delay time	t_{CHIRL}	$\overline{IORD}$		–	10	ns
	t_{CHIRH}			–	10	ns
$\overline{IOWR}$ delay time	t_{CHIWL}	$\overline{IOWR}$		–	10	ns
	t_{CHIWH}			–	10	ns

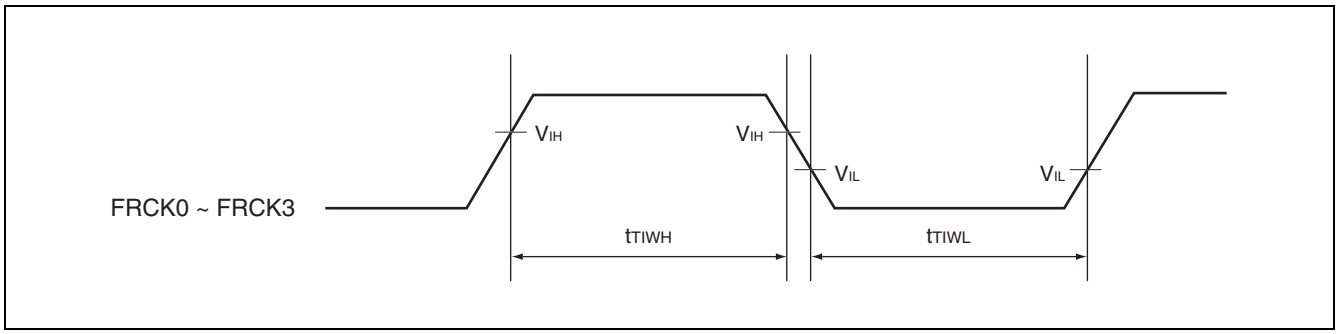


12.4.10 Free-Run Timer Clock

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 4.0 V to 5.5 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}, t_{TIWL}	FRCK0 to FRCK3	–	$4t_{CYCP}$	–	ns

Note: t_{CYCP} is the cycle time of the peripheral clock.

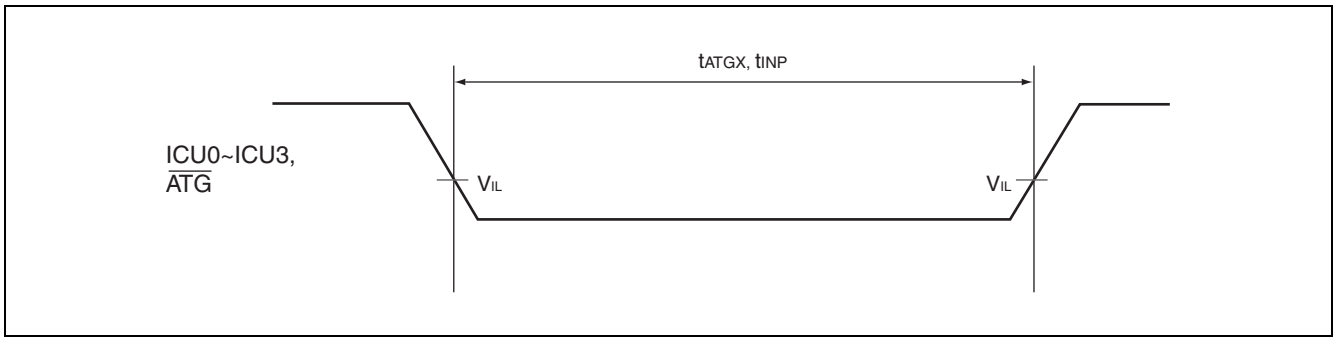


12.4.11 Trigger input timing

($V_{CC}3$ = 3.0 V to 3.6 V, $V_{CC}5$ = 4.0 V to 5.5 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICU0 to ICU3	–	$5t_{CYCP}$	–	ns
A/D converter trigger	t_{ATGX}	$\overline{ATG}$	–	$5t_{CYCP}$	–	ns

Note: t_{CYCP} is the cycle time of the peripheral clock.



12.5 Electrical Characteristics for A/D Converter

($V_{CC}3$ = 3.0 V to 3.6 V, Vss = AVss = 0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error[1]	–	–	–	–	±3	LSB	At AVcc3 = 3.3 V, AVRH = 3.3 V
Linearity error[1]	–	–	–	–	±2.5	LSB	
Differential linearity error[1]	–	–	–	–	±1.9	LSB	
Zero transition voltage[1]	V_{OT}	AN0 to AN15	AVRL–1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale transition voltage[1]	V_{FST}	AN0 to AN15	AVRH–3.5 LSB	AVRH–1.5 LSB	AVRH + 0.5 LSB	V	
Conversion time	–	–	3[2]	–	–	µs	
Analog port input current	I_{AIN}	AN0 to AN15	–	–	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN15	AV_{SS}	–	AVRH	V	
Reference voltage	–	AVRH	AV_{SS}	–	$AV_{CC}3$	V	
Analog power supply current (analog + digital)	I_A	AVCC3	–	1.5	2.5	mA	Including reference supply
	I_{AH}[3]		–	–	10	µA	
Analog input equivalent capacity	Cin	AN0 to AN15	–	–	11.0	pF	
Analog input equivalent resistance	Rin	AN0 to AN15	–	–	12.1	kΩ	
Output impedance of analog signal source	Rext	–	–	–	4.2	kΩ	

1. Standard value in the CPU sleep state
2. Please adjust the peripheral clock and conversion time setting register so as not to become less than 3µs.
3. The current when A/D converter is not operating, or in the CPU stop mode (at $V_{CC}3 = AV_{CC}3 = AVRH = 3.3$ V).

12.5.1 Cautions Relating to the A/D Converter

The diagram below shows the equivalent circuit of the sampling circuit in the A/D converter.

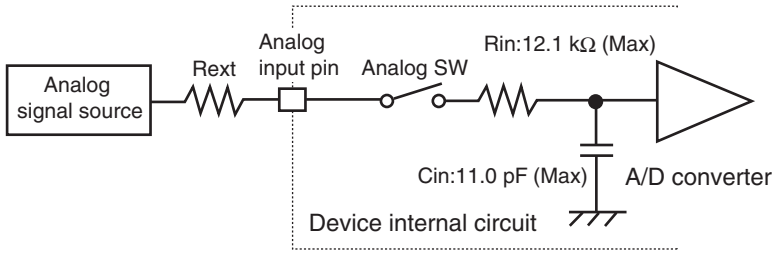
The output impedance of the external circuit connected to the analog input must satisfy the following criteria.

- The recommended output impedance for the external circuit is 4.2 kΩ or less.
- If an external capacitor is used, remember to consider the capacitive voltage divider effect due to the external capacitor and the internal capacitor in the chip. Accordingly, an external capacitance several thousand times that of the internal capacitance is recommended.
- The analog voltage sampling period may be too short if the output impedance of the external circuit is high.In this case, select Rext and Tsamp such that they satisfy the following condition.

  Rext = Tsamp/ (7 × Cin) - Rin

  Rext : Output impedance of the analog signal source
  Tsamp : Sampling time
  Cin : Equivalent capacitance of analog input
  Rin : Equivalent resistance of analog input

Input impedance



12.5.2 Definition of A/D Converter Terms

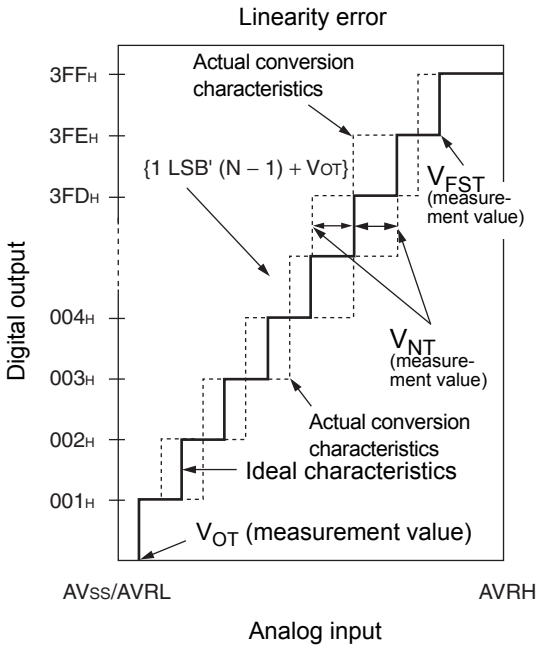
■ Resolution
Analog variation that is recognizable by an A/D converter.

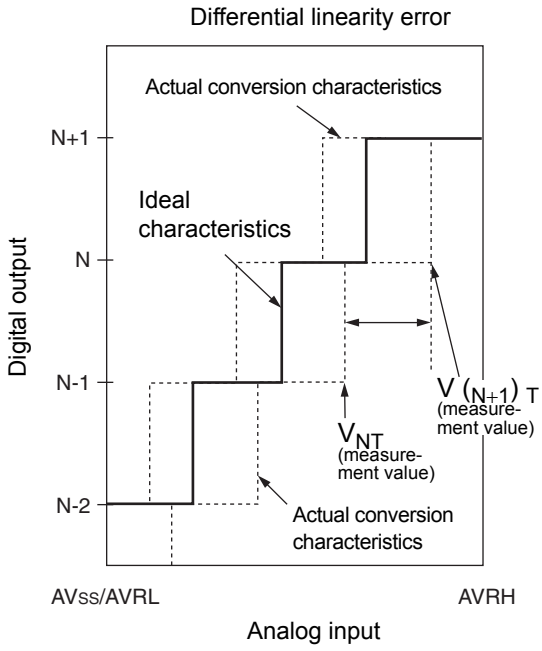
■ Linearity error
Deviation between actual conversion characteristics and a straight line connecting zero transition point ("00 0000 0000_B" ↔ "00 0000 0001_B") and full scale transition point ("11 1111 1110_B "↔ "11 1111 1111_B").

■ Differential linearity error
Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

■ Total error
This error indicates the difference between actual and theoretical values, including the zero transition error/ full scale transition error/linearity error.

■



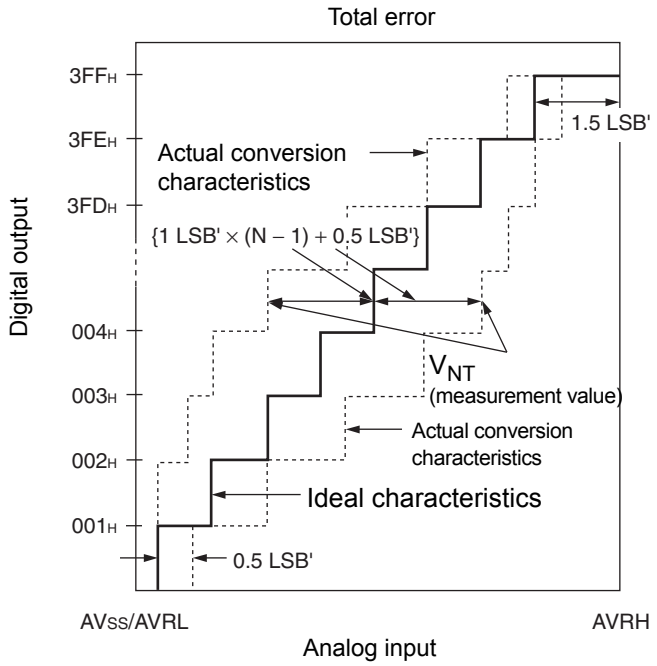


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB' \times (N - 1) + V_{OT}\}}{1LSB'} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB'} \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N: A/D converter digital output value
V_{OT}: A voltage at which digital output transits from 000_H to 001_H
V_{FST}: A voltage at which digital output transits from $3FE_H$ to $3FF_H$
V_{NT}: A voltage at which digital output transitions from N−1 to N



$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}}{1024} \text{ [V]}$$

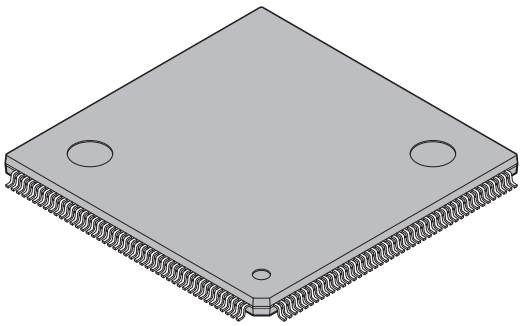
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N: A/D converter digital output value
V_{NT}: A voltage at which digital output transits from (N + 1) to N
V_{OT}' (ideal value) = AV_{SS} + 0.5 LSB' [V]
V_{FST}' (ideal value) = AVRH – 1.5 LSB' [V]

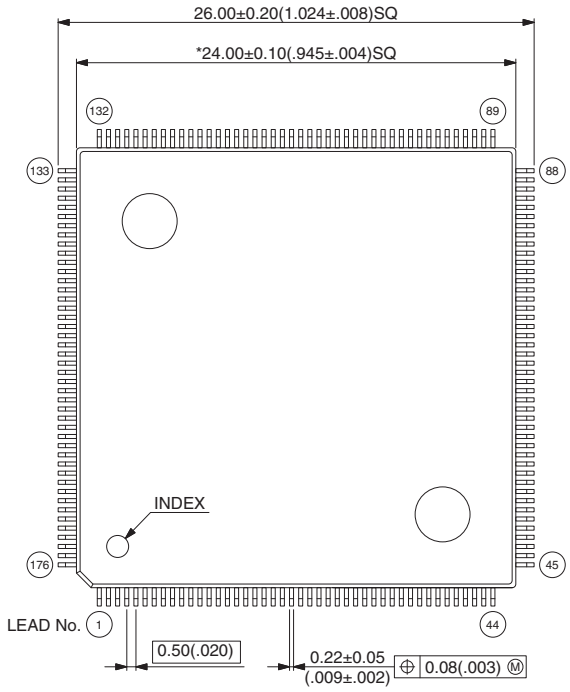
13. Ordering Information

Part number	Package	Remarks
MB91F467RCPMC-GSE1	176-pin plastic LQFP (FPT-176P-M07)	Lead-free package

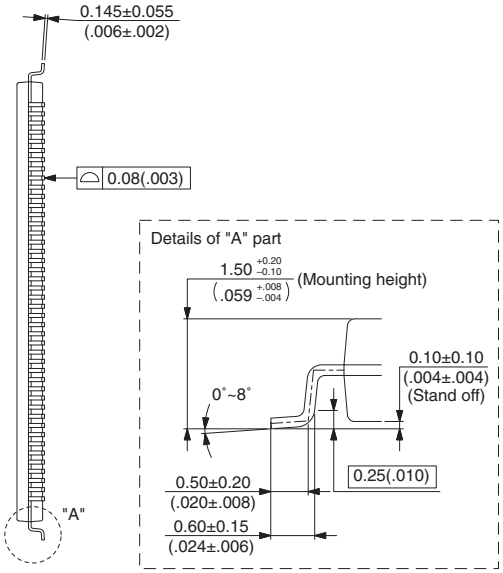
14. Package Dimension

176-pin plastic LQFP		
 (FPT-176P-M07)	Lead pitch	0.50 mm
	Package width × package length	24.0 × 24.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP-0176-2424-0.50

176-pin plastic LQFP
(FPT-176P-M07)



Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

15. Main Changes in this Edition

Spansion Publication Number: DS07-16603-3E

Page	Section	Change Results
4	1. Pin Assignment	Corrected the pin name for pin number 176. VCO5 → VCC5
6	2. Pin Description	Corrected the description of pin number 27.
7		Corrected the pin number. 72, 76 to 81 → 72, 75 to 81
9, 10		Added 163 to 175 pins in description of pin number 176.
11	3. I/O Circuit Type	Deleted the description of “pull-up” from circuit type column of type A. Deleted the description of “pull-down” from circuit type column of type B.
15	4. Handling Devices	Added the item “Serial communication”.
62	12. Electrical Characteristics 12.3. DC characteristics	Item: Changed the pin name for “Pull-down resistance value”. INIT, pull-up pin → MD3, pull-down pin
64	12.4. AC characteristics	Added the item “(4) Interrupt characteristics for recover from shutdown”.
74	12.4.10 Free-run timer clock	Added V_{IH}, V_{IL} to the timing chart.
	12.4.11Trigger input timing	Added V_{IL} to the timing chart.

NOTE: Please see “Document History” for later revised information.

Document History

Document Title: MB91F467RC, FR60, MB91460R Series, 32-bit Microcontroller Datasheet Document Number: 002-04598				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	10/26/2009	Migrated to Cypress and assigned document number 002-04598. No change to document contents or format.
*A	5232531	AKIH	06/23/2016	Updated to Cypress template

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

ARM and Cortex are the trademarks of ARM Limited in the EU and other countries