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CY91460Q Series

FR60 32-bit Microcontroller

CY91460Q series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART and CAN controllers.

Note: Differences versus CY91F469GB are marked in red color.

Features

FR60 CPU Core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal Peripheral Resources

- General-purpose ports : Maximum 205 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously (including 2 external channels).
  - 3 transfer sources (external pin/internal peripheral/software)
  - Activation source can be selected using software
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Fly-by transfer support (between external I/O and memory)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type): 2 modules
  - ADC 0: 10-bit resolution: 32 channels
  - ADC 1: 10-bit resolution: 8 channels
  - Conversion time: minimum 1 µs
- External interrupt inputs : 32 channels
  - 12 channels shared with CAN RX, LIN-USART SIN, I^2C SDA or I^2C SCL pins
  - 16 channels shared with ADC input pins
- Bit search module (for REALOS)
  - Function to search from the MSB (most significant bit) for the position of the first “0”, “1”, or changed bit in a word
- LIN-USART (full duplex double buffer): 12 channels, 8 channels with FIFO
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
  - LIN-USART 8-11 with asynchronous operation only
- I^2C bus interface (supports 400 kbps): 3 channel
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 3 channels
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Sound generator : 1 channelTone frequency : PWM frequency divide-by-two (reload value + 1)
- Alarm comparator : 2 channelsMonitor external voltage Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : 16 channels
- 16-bit PFM timer : 1 channel
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 9 channels (1 channel each for ICU and OCU)
- Input capture: 10 channels (operates in conjunction with the free-run timer)
- Output compare: 8 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 4 channels (4*8-bit or 2*16-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Supply Supervisor: Low voltage detection circuit for external $V_{DD}5$ and internal 1.8V core voltage

- Clock supervisor
  - Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor
- Sub-clock calibration
  - Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer
  - Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  - Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

Package and Technology

- Package : 320-pin plastic BGA (BYA320)
- CMOS 0.18 µm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 105°C/+125°C[a]

a. For maximum ambient temperature $T_{A(max)}$, See “Ordering Information” on page 145.

Contents

1. Product Lineup

Feature	CY91F469QA
Max. core frequency (CLKB)	100MHz at 1.9V *1 88MHz at 1.8V *2
Max. resource frequency (CLKP)	50MHz
Max. external bus freq. (CLKT)	50MHz
Max. CAN frequency (CLKCAN)	50MHz
Technology	0.18µm
Flash memory	2112 KByte
Flash Protection	yes
Flash CRC calculation	yes
D-RAM	64 KByte
ID-RAM	32 KByte
Flash-cache (F-cache)	16 KBytes
External bus cache (I-cache)	4 KBytes
Boot-ROM / BI-ROM	4 KByte
MMU/MPU	MPU (8 ch) *3
DMA	5 ch
Software-Watchdog	yes
Hardware-Watchdog (RC osc. based)	yes
Bit Search	yes
RTC	1 ch
Free Running Timer	9 ch
ICU	10 ch
OCU	8 ch
Reload Timer	8 ch
PPG 16-bit	16 ch
PFM 16-bit	1 ch
Sound Generator	1 ch
Up/Down Counter (8/16-bit)	4 ch (8-bit) / 2 ch (16-bit)
C_CAN	3 ch (32msg)
LIN-USART	4 ch + 4 ch FIFO + 4 ch FIFO (asynchronous)
I2C (400k)	3 ch
FR external bus	yes (28bit addr, 32bit data, 8 chip selects)

Feature	CY91F469QA
External Interrupts	32 ch
NMI Interrupts	
General IO ports	205
ADC (10 bit)	32 ch + 8 ch
Alarm Comparator	2 ch
Reset input (INITX)	yes
Hardware Standby Input (HSTX)	no
Clock Modulator	yes
Low power mode	yes
Supply Supervisor	yes
Clock Supervisor	yes
Main clock oscillator	4MHz
Sub clock oscillator	32kHz
RC Oscillator	100kHz / 2MHz
PLL	x 25
DSU4	no
EDSU	yes (16 BP) *3
JTAG Boundary Scan	yes
Supply Voltage	3V / 5V
Regulator	yes
Power Consumption	< 2 W
Temperature Range (T_A)	-40..$T_{A(max)}$ °C *4
Package	BGA320
Power on to PLL run	< 20 ms
Flash Download Time	< 8 sec typical

*1: At 1.9V main regulator voltage. In order to enter this mode please set REGSEL_FLASHSEL=1 and REGSEL_MAINSEL=1.

*2: At 1.8V main regulator voltage (default).

*3: MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

*4: For maximum ambient temperature $T_{A(max)}$, see “Ordering Information” on page 145.

2. Pin Assignment

2.1 CY91F469QA

(TOP VIEW)

▲	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	1	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	A
B	2	77	144	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128	57	B
C	3	78	145	204	203	202	201	200	199	198	197	196	195	194	193	192	191	190	127	56	C
D	4	79	146	205	256	255	254	253	252	251	250	249	248	247	246	245	244	189	126	55	D
E	5	80	147	206													243	188	125	54	E
F	6	81	148	207													242	187	124	53	F
G	7	82	149	208			257	284	283	282	281	280	279	278			241	186	123	52	G
H	8	83	150	209			258	285	304	303	302	301	300	277			240	185	122	51	H
J	9	84	151	210			259	286	305	316	315	314	299	276			239	184	121	50	J
K	10	85	152	211			260	287	306	317	320	313	298	275			238	183	120	49	K
L	11	86	153	212			261	288	307	318	319	312	297	274			237	182	119	48	L
M	12	87	154	213			262	289	308	309	310	311	296	273			236	181	118	47	M
N	13	88	155	214			263	290	291	292	293	294	295	272			235	180	117	46	N
P	14	89	156	215			264	265	266	267	268	269	270	271			234	179	116	45	P
R	15	90	157	216													233	178	115	44	R
T	16	91	158	217													232	177	114	43	T
U	17	92	159	218	219	220	221	222	223	224	225	226	227	228	229	230	231	176	113	42	U
V	18	93	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	112	41	V
W	19	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	40	W
Y	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

BYA320

3. Pin Description

3.1 CY91F469QA

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
B1	2	P24_1	I/O	A	General-purpose input/output port
		INT1			External interrupt input pin
C1	3	P13_0	I/O	A	General-purpose input/output port
		DREQ0			DMA external transfer request input
D1	4	P13_1	I/O	A	General-purpose input/output port
		DACKX0			DMA external transfer acknowledge output pin
E1	5	P13_3	I/O	A	General-purpose input/output port
		DEOP0			DMA external transfer EOP (End of Process) output pin
F1	6	P13_6	I/O	A	General-purpose input/output port
		DEOTX1			DMA external transfer EOT (End of Track) output pin
		DEOP1			DMA external transfer EOP (End of Process) output pin
G1	7	P11_1	I/O	A	General-purpose input/output port
		IOWRX			DMA memory to I/O fly-by transfer output pin
H1	8	P09_3	I/O	A	General-purpose input/output port
		CSX3			Chip select output pin
J1	9	P09_6	I/O	A	General-purpose input/output port
		CSX6			Chip select output pin
K1	10	P08_2	I/O	A	General-purpose input/output port
		WRX2			External write strobe output pin
L1	11	P08_5	I/O	A	General-purpose input/output port
		BGRNTX			External bus release reception output pin
M1	12	P07_1	I/O	A	General-purpose input/output port
		A1			Signal pin of external address bus (bit1)
N1	13	P07_5	I/O	A	General-purpose input/output port
		A5			Signal pin of external address bus (bit5)
P1	14	P06_0	I/O	A	General-purpose input/output port
		A8			Signal pin of external address bus (bit8)
R1	15	P06_4	I/O	A	General-purpose input/output port
		A12			Signal pin of external address bus (bit12)
T1	16	P06_7	I/O	A	General-purpose input/output port
		A15			Signal pin of external address bus (bit15)
U1	17	P05_3	I/O	A	General-purpose input/output port
		A19			Signal pin of external address bus (bit19)
V1	18	P05_6	I/O	A	General-purpose input/output port
		A22			Signal pin of external address bus (bit22)

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
W1	19	P04_1	I/O	A	General-purpose input/output port
		A25			Signal pin of external address bus (bit25)
Y2	21	P04_3	I/O	A	General-purpose input/output port
		A27			Signal pin of external address bus (bit27)
Y3	22	P03_1	I/O	A	General-purpose input/output port
		D1			Signal pin of external data bus (bit1)
Y4	23	P03_4	I/O	A	General-purpose input/output port
		D4			Signal pin of external data bus (bit4)
Y5	24	P02_0	I/O	A	General-purpose input/output port
		D8			Signal pin of external data bus (bit8)
Y6	25	P02_3	I/O	A	General-purpose input/output port
		D11			Signal pin of external data bus (bit11)
Y7	26	P02_7	I/O	A	General-purpose input/output port
		D15			Signal pin of external data bus (bit15)
Y8	27	P01_2	I/O	A	General-purpose input/output port
		D18			Signal pin of external data bus (bit18)
Y9	28	P01_6	I/O	A	General-purpose input/output port
		D22			Signal pin of external data bus (bit22)
Y10	29	P00_1	I/O	A	General-purpose input/output port
		D25			Signal pin of external data bus (bit25)
Y11	30	P00_5	I/O	A	General-purpose input/output port
		D29			Signal pin of external data bus (bit29)
Y12	31	P00_6	I/O	A	General-purpose input/output port
		D30			Signal pin of external data bus (bit30)
Y13	32	P00_7	I/O	A	General-purpose input/output port
		D31			Signal pin of external data bus (bit31)
Y14	33	P10_4	I/O	A	General-purpose input/output port
		MCLKO			Clock output pin for memory
Y16	35	MONCLK	O	M	Clock monitor pin
W20	40	P21_0	I/O	A	General-purpose input/output port
		SIN0			Data input pin of USART0
V20	41	P21_4	I/O	A	General-purpose input/output port
		SIN1			Data input pin of USART1
U20	42	P20_0	I/O	A	General-purpose input/output port
		SIN2			Data input pin of USART2
		AIN0			Up/down counter input pin

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
T20	43	P20_4	I/O	A	General-purpose input/output port
		SIN3			Data input pin of USART3
		AIN1			Up/down counter input pin
R20	44	P19_0	I/O	A	General-purpose input/output port
		SIN4			Data input pin of USART4
P20	45	P19_2	I/O	A	General-purpose input/output port
		SCK4			Clock input/output pin of USART4
		CK4			External clock input pin of free-run timer 4
N20	46	X1	---	J1	Clock (oscillation) output
M20	47	P18_2	I/O	B	General-purpose input/output port
		SCK6			Clock input/output pin of USART6
		ZIN2			Up/down counter input pin
		CK6			External clock input pin of free-run timer 6
		AN42			Analog input pin of A/D converter (second A/D macro)
L20	48	P18_6	I/O	B	General-purpose input/output port
		SCK7			Clock input/output pin of USART7
		ZIN3			Up/down counter input pin
		CK7			External clock input pin of free-run timer 7
		AN46			Analog input pin of A/D converter (second A/D macro)
K20	49	P17_2	I/O	B	General-purpose input/output port
		PPG2			PPG timer output pins
		AN34			Analog input pin of A/D converter (second A/D macro)
J20	50	P17_6	I/O	B	General-purpose input/output port
		PPG6			PPG timer output pins
		AN38			Analog input pin of A/D converter (second A/D macro)
H20	51	P23_2	I/O	A	General-purpose input/output port
		RX1			RX input/output pin of CAN1
		INT9			External interrupt input pin
G20	52	P34_1	I/O	A	General-purpose input/output port
		SOT10			Data output of USART10
F20	53	P35_1	I/O	A	General-purpose input/output port
		SOT8			Data output of USART8
E20	54	P29_4	I/O	B	General-purpose input/output port
		AN4			Analog input pin of A/D converter
D20	55	P28_0	I/O	B	General-purpose input/output port
		AN8			Analog input pin of A/D converter

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
C20	56	P28_3	I/O	B	General-purpose input/output port
		AN11			Analog input pin of A/D converter
B20	57	P28_5	I/O	B	General-purpose input/output port
		AN13			Analog input pin of A/D converter
A19	59	P28_7	I/O	B	General-purpose input/output port
		AN15			Analog input pin of A/D converter
A17	61	P27_2	I/O	B	General-purpose input/output port
		AN18			Analog input pin of A/D converter
		INT18			External interrupt pin
A14	64	P26_0	I/O	B	General-purpose input/output port
		AN24			Analog input pin of A/D converter
		INT24			External interrupt pin
A13	65	P35_4	I/O	A	General-purpose input/output port
		SIN9			Data input of USART9
		INT12			External interrupt input pin
A12	66	P35_5	I/O	A	General-purpose input/output port
		SOT9			Data output pin of USART9
A11	67	P22_3	I/O	A	General-purpose input/output port
		TX5			TX output pin of CAN5
A10	68	P22_6	I/O	C	General-purpose input/output port
		SDA1			I^2C bus data input/output pin (open drain)
		INT15			External interrupt input pin
		ICU8			Input capture input pin [2]
A9	69	P14_2	I/O	A	General-purpose input/output port
		ICU2			Input capture input pin
		TIN2			External trigger input pin of reload timer
		TTG10/2			External trigger input pin of PPG timer
A8	70	P14_6	I/O	A	General-purpose input/output port
		ICU6			Input capture input pin
		TIN6			Input capture input pin
		TTG14/6			External trigger input pin of PPG timer
A7	71	P16_1	I/O	A	General-purpose input/output port
		PPG9			Output pin of PPG timer
A6	72	P16_5	I/O	A	General-purpose input/output port
		PPG13			Output pin of PPG timer
		SG0			SG0 output pin of sound generator

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
A5	73	P15_0	I/O	A	General-purpose input/output port
		OCU0			Output compare output pin
		TOT0			Reload timer output pin
A4	74	P15_4	I/O	A	General-purpose input/output port
		OCU4			Output compare output pin
		TOT4			Reload timer output pin
A3	75	P15_7	I/O	A	General-purpose input/output port
		OCU7			Output compare output pin
		TOT7			Reload timer output pin
A2	76	P24_0	I/O	A	General-purpose input/output port
		INT0			External interrupt input pin
B2	77	P24_2	I/O	A	General-purpose input/output port
		INT2			External interrupt input pin
C2	78	P34_4	I/O	A	General-purpose input/output port
		INT4			External interrupt input pin
		SIN11			Data input pin of USART11
D2	79	P13_2	I/O	A	General-purpose input/output port
		DEOTX0			DMA external transfer EOT (End of Track) output pin
		DEOP0			DMA external transfer EOP (End of Process) output pin
E2	80	P13_4	I/O	A	General-purpose input/output port
		DREQ1			DMA external transfer request input
F2	81	P13_7	I/O	A	General-purpose input/output port
		DEOP1			DMA external transfer EOP (End of Process) output pin
G2	82	P09_0	I/O	A	General-purpose input/output port
		CSX0			Chip select output pin
H2	83	P09_4	I/O	A	General-purpose input/output port
		CSX4			Chip select output pin
J2	84	P09_7	I/O	A	General-purpose input/output port
		CSX7			Chip select output pin
K2	85	P08_3	I/O	A	General-purpose input/output port
		WRX3			External write strobe output pin
L2	86	P08_6	I/O	A	General-purpose input/output port
		BRQ			External bus release request input pin
M2	87	P07_2	I/O	A	General-purpose input/output port
		A2			Signal pin of external address bus (bit2)
N2	88	P07_6	I/O	A	General-purpose input/output port
		A6			Signal pin of external address bus (bit6)

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
P2	89	P06_1	I/O	A	General-purpose input/output port
		A9			Signal pin of external address bus (bit9)
R2	90	P06_5	I/O	A	General-purpose input/output port
		A13			Signal pin of external address bus (bit13)
T2	91	P05_0	I/O	A	General-purpose input/output port
		A16			Signal pin of external address bus (bit16)
U2	92	P05_4	I/O	A	General-purpose input/output port
		A20			Signal pin of external address bus (bit20)
V2	93	P05_7	I/O	A	General-purpose input/output port
		A23			Signal pin of external address bus (bit23)
W2	94	P04_2	I/O	A	General-purpose input/output port
		A26			Signal pin of external address bus (bit26)
W3	95	P03_0	I/O	A	General-purpose input/output port
		D0			Signal pin of external data bus (bit0)
W4	96	P03_3	I/O	A	General-purpose input/output port
		D3			Signal pin of external data bus (bit3)
W5	97	P03_7	I/O	A	General-purpose input/output port
		D7			Signal pin of external data bus (bit7)
W6	98	P02_2	I/O	A	General-purpose input/output port
		D10			Signal pin of external data bus (bit10)
W7	99	P02_6	I/O	A	General-purpose input/output port
		D14			Signal pin of external data bus (bit14)
W8	100	P01_1	I/O	A	General-purpose input/output port
		D17			Signal pin of external data bus (bit17)
W9	101	P01_5	I/O	A	General-purpose input/output port
		D21			Signal pin of external data bus (bit21)
W10	102	P00_0	I/O	A	General-purpose input/output port
		D24			Signal pin of external data bus (bit24)
W11	103	P00_4	I/O	A	General-purpose input/output port
		D28			Signal pin of external data bus (bit28)
W12	104	P10_1	I/O	A	General-purpose input/output port
		ASX			Address strobe output pin
W13	105	P10_0	I/O	A	General-purpose input/output port
		SYSCLK			Clock output pin for external bus
W14	106	P10_5	I/O	A	General-purpose input/output port
		MCLKI			Clock input pin for memory
W15	107	TDO	O	M	Boundary Scan Test Data Out pin

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
W16	108	TDI	I	H	Boundary Scan Test Data In pin
W17	109	TRST	I	I	Boundary Scan Test Reset pin
W18	110	P21_2	I/O	A	General-purpose input/output port
		SCK0			Clock input/output pin of USART0
		CK0/8			External clock input pin of free-run timer 0 + 8
W19	111	P21_1	I/O	A	General-purpose input/output port
		SOT0			Data output pin of USART0
V19	112	P21_5	I/O	A	General-purpose input/output port
		SOT1			Data output pin of USART1
U19	113	P20_1	I/O	A	General-purpose input/output port
		SOT2			Data output pin of USART2
		BIN0			Up/down counter input pin
T19	114	X0A	---	J2	Sub clock (oscillation) input
R19	115	P19_1	I/O	A	General-purpose input/output port
		SOT4			Data output pin of USART4
P19	116	P19_4	I/O	A	General-purpose input/output port
		SIN5			Data input pin of USART5
N19	117	P18_0	I/O	A	General-purpose input/output port
		SIN6			Data input pin of USART6
		AIN2			Up/down counter input pin
M19	118	X0	---	J1	Clock (oscillation) input
L19	119	P17_0	I/O	A	General-purpose input/output port
		PPG0			Output pin of PPG timer
K19	120	P17_3	I/O	B	General-purpose input/output port
		PPG3			Output pin of PPG timer
		AN35			Analog input pin of A/D converter (second A/D macro)
J19	121	P17_7	I/O	B	General-purpose input/output port
		PPG7			Output pin of PPG timer
		AN39			Analog input pin of A/D converter (second A/D macro)
H19	122	P23_3	I/O	A	General-purpose input/output port
		TX1			TX output pin of CAN1
G19	123	P35_0	I/O	A	General-purpose input/output port
		SIN8			Data input of USART8
		INT11			External interrupt input pin
F19	124	P29_2	I/O	B	General-purpose input/output port
		AN2			Analog input pin of A/D converter

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
E19	125	P29_5	I/O	B	General-purpose input/output port
		AN5			Analog input pin of A/D converter
D19	126	P28_1	I/O	B	General-purpose input/output port
		AN9			Analog input pin of A/D converter
C19	127	P28_4	I/O	B	General-purpose input/output port
		AN12			Analog input pin of A/D converter
B19	128	P28_6	I/O	B	General-purpose input/output port
		AN14			Analog input pin of A/D converter
B18	129	P27_0	I/O	B	General-purpose input/output port
		AN16			Analog input pin of A/D converter
		INT16			External interrupt pin
B17	130	P27_3	I/O	B	General-purpose input/output port
		AN19			Analog input pin of A/D converter
		INT19			External interrupt pin
B16	131	P27_5	I/O	B	General-purpose input/output port
		AN21			Analog input pin of A/D converter
		INT21			External interrupt pin
B15	132	P27_7	I/O	B	General-purpose input/output port
		AN23			Analog input pin of A/D converter
		INT23			External interrupt pin
B14	133	P26_1	I/O	B	General-purpose input/output port
		AN25			Analog input pin of A/D converter
		INT25			External interrupt pin
B13	134	P26_4	I/O	B	General-purpose input/output port
		AN28			Analog input pin of A/D converter
		INT28			External interrupt pin
B12	135	P22_2	I/O	A	General-purpose input/output port
		RX5			RX input/output pin of CAN5
		INT13			External interrupt input pin
B11	136	P24_4	I/O	C	General-purpose input/output port
		SDA2			I^2C bus data input/output pin (open drain)
		INT14			External interrupt input pin
B10	137	P22_7	I/O	C	General-purpose input/output port
		SCL1			I^2C bus clock input/output pin (open drain)
		ICU9			Input capture input pin [3]

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
B9	138	P14_3	I/O	A	General-purpose input/output port
		ICU3			Input capture input pin
		TIN3			External trigger input pin of reload timer
		TTG11/3			External trigger input pin of PPG timer
B8	139	P14_7	I/O	A	General-purpose input/output port
		ICU7			Input capture input pin
		TIN7			External trigger input pin of reload timer
		TTG15/7			External trigger input pin of PPG timer
B7	140	P16_2	I/O	A	General-purpose input/output port
		PPG10			Output pin of PPG timer
B6	141	P16_6	I/O	A	General-purpose input/output port
		PPG14			Output pin of PPG timer
		PFM			Pulse frequency modulator output pin
B5	142	P15_1	I/O	A	General-purpose input/output port
		OCU1			Output compare output pin
		TOT1			Reload timer output pin
B4	143	P15_5	I/O	A	General-purpose input/output port
		OCU5			Output compare output pin
		TOT5			Reload timer output pin
B3	144	P24_3	I/O	A	General-purpose input/output port
		INT3			External interrupt input pin
C3	145	P34_5	I/O	A	General-purpose input/output port
		INT5			External interrupt input pin
		SOT11			Data output pin of USART11
D3	146	P24_6	I/O	C	General-purpose input/output port
		INT6			External interrupt input pin
		SDA3			I^2C bus data input/output pin (open drain)
E3	147	P13_5	I/O	A	General-purpose input/output port
		DACKX1			DMA external transfer acknowledge output pin
F3	148	P11_0	I/O	A	General-purpose input/output port
		IORDX			Output pin for DMA I/O to memory fly-by transfer
G3	149	P09_1	I/O	A	General-purpose input/output port
		CSX1			Chip select output pin
H3	150	P09_5	I/O	A	General-purpose input/output port
		CSX5			Chip select output pin
J3	151	P08_0	I/O	A	General-purpose input/output port
		WRX0			External write strobe output pin

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
K3	152	P08_4	I/O	A	General-purpose input/output port
		RDX			External read strobe output pin
L3	153	P08_7	I/O	A	General-purpose input/output port
		RDY			External ready input pin
M3	154	P07_3	I/O	A	General-purpose input/output port
		A3			Signal pin of external address bus (bit3)
N3	155	P07_7	I/O	A	General-purpose input/output port
		A7			Signal pin of external address bus (bit7)
P3	156	P06_2	I/O	A	General-purpose input/output port
		A10			Signal pin of external address bus (bit10)
R3	157	P06_6	I/O	A	General-purpose input/output port
		A14			Signal pin of external address bus (bit14)
T3	158	P05_1	I/O	A	General-purpose input/output port
		A17			Signal pin of external address bus (bit17)
U3	159	P05_5	I/O	A	General-purpose input/output port
		A21			Signal pin of external address bus (bit21)
V3	160	P04_0	I/O	A	General-purpose input/output port
		A24			Signal pin of external address bus (bit24)
V4	161	P03_2	I/O	A	General-purpose input/output port
		D2			Signal pin of external data bus (bit2)
V5	162	P03_6	I/O	A	General-purpose input/output port
		D6			Signal pin of external data bus (bit6)
V6	163	P02_1	I/O	A	General-purpose input/output port
		D9			Signal pin of external data bus (bit9)
V7	164	P02_5	I/O	A	General-purpose input/output port
		D13			Signal pin of external data bus (bit13)
V8	165	P01_0	I/O	A	General-purpose input/output port
		D16			Signal pin of external data bus (bit16)
V9	166	P01_4	I/O	A	General-purpose input/output port
		D20			Signal pin of external data bus (bit20)
V10	167	P01_7	I/O	A	General-purpose input/output port
		D23			Signal pin of external data bus (bit23)
V11	168	P00_3	I/O	A	General-purpose input/output port
		D27			Signal pin of external data bus (bit27)
V12	169	P10_6	I/O	A	General-purpose input/output port
		MCLKE			Clock enable signal pin for memory

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
V13	170	P10_2	I/O	A	General-purpose input/output port
		BAAX			Burst address advance output pin
V14	171	TMS	I	H	Boundary Scan Test Mode Select pin
V15	172	MD_2	I	G	Mode setting pins
V16	173	MD_1	I	G	
V17	174	MD_0	I	G	
V18	175	P21_6	I/O	A	General-purpose input/output port
		SCK1			Clock input/output pin of USART1
		CK1			External clock input pin of free-run timer 1
U18	176	P20_2	I/O	A	General-purpose input/output port
		SCK2			Clock input/output pin of USART2
		ZIN0			Up/down counter input pin
		CK2			External clock input pin of free-run timer 2
T18	177	P20_5	I/O	A	General-purpose input/output port
		SOT3			Data output pin of USART3
		BIN1			Up/down counter input pin
R18	178	X1A	---	J2	Sub clock (oscillation) output
P18	179	P19_5	I/O	A	General-purpose input/output port
		SOT5			Data output pin of USART2
N18	180	P18_1	I/O	A	General-purpose input/output port
		SOT6			Data output pin of USART6
		BIN2			Up/down counter input pin
M18	181	P18_4	I/O	A	General-purpose input/output port
		SIN7			Data input pin of USART7
		AIN3			Up/down counter input pin
L18	182	P17_1	I/O	A	General-purpose input/output port
		PPG1			PPG timer output pin
K18	183	P17_4	I/O	B	General-purpose input/output port
		PPG4			PPG timer output pin
		AN36			Analog input pin of A/D converter (second A/D macro)
J18	184	P23_0	I/O	A	General-purpose input/output port
		RX0			RX input/output pin of CAN0
		INT8			External interrupt input pin
H18	185	P34_0	I/O	A	General-purpose input/output port
		SIN10			Data input of USART10
		INT10			External interrupt input pin

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
G18	186	P29_0	I/O	B	General-purpose input/output port
		AN0			Analog input pin of A/D converter
F18	187	P29_3	I/O	B	General-purpose input/output port
		AN3			Analog input pin of A/D converter
E18	188	P29_6	I/O	B	General-purpose input/output port
		AN6			Analog input pin of A/D converter
D18	189	P28_2	I/O	B	General-purpose input/output port
		AN10			Analog input pin of A/D converter
C18	190	P27_1	I/O	B	General-purpose input/output port
		AN17			Analog input pin of A/D converter
		INT17			External interrupt pin
C17	191	P27_4	I/O	B	General-purpose input/output port
		AN20			Analog input pin of A/D converter
		INT20			External interrupt pin
C16	192	ALARM_0	I	N	Alarm comparator input pin
C15	193	ALARM_1	I	N	Alarm comparator input pin
C14	194	P26_2	I/O	B	General-purpose input/output port
		AN26			Analog input pin of A/D converter
		INT26			External interrupt pin
C13	195	P26_5	I/O	B	General-purpose input/output port
		AN29			Analog input pin of A/D converter
		INT29			External interrupt pin
C12	196	P26_6	I/O	B	General-purpose input/output port
		AN30			Analog input pin of A/D converter
		INT30			External interrupt pin
C11	197	P24_5	I/O	C	General-purpose input/output port
		SCL2			I^2C bus clock input/output pin (open drain)
C10	198	P14_0	I/O	A	General-purpose input/output port
		ICU0			Input capture input pin
		TIN0			External trigger input pin of reload timer
		TTG8/0			External trigger input pin of PPG timer
C9	199	P14_4	I/O	A	General-purpose input/output port
		ICU4			Input capture input pin
		TIN4			External trigger input pin of reload timer
		TTG12/4			External trigger input pin of PPG timer
C8	200	P16_0	I/O	A	General-purpose input/output port
		PPG8			Output pin of PPG timer

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
C7	201	P16_3	I/O	A	General-purpose input/output port
		PPG11			Output pin of PPG timer
C6	202	P16_7	I/O	A	General-purpose input/output port
		PPG15			Output pin of PPG timer
		ATGX			A/D converter external trigger input pin
C5	203	P15_2	I/O	A	General-purpose input/output port
		OCU2			Output compare output pin
		TOT2			Reload timer output pin
C4	204	P15_6	I/O	A	General-purpose input/output port
		OCU6			Output compare output pin
		TOT6			Reload timer output pin
E4	206	P24_7	I/O	C	General-purpose input/output port
		INT7			External interrupt input pin
		SCL3			I^2C bus clock input/output pin (open drain)
G4	208	P09_2	I/O	A	General-purpose input/output port
		CSX2			Chip select output pin
J4	210	P08_1	I/O	A	General-purpose input/output port
		WRX1			External write strobe output pin
L4	212	P07_0	I/O	A	General-purpose input/output port
		A0			Signal pin of external address bus (bit0)
M4	213	P07_4	I/O	A	General-purpose input/output port
		A4			Signal pin of external address bus (bit4)
P4	215	P06_3 A11	I/O	A	General-purpose input/output port
					Signal pin of external address bus (bit11)
T4	217	P05_2	I/O	A	General-purpose input/output port
		A18			Signal pin of external address bus (bit18)
U5	219	P03_5	I/O	A	General-purpose input/output port
		D5			Signal pin of external data bus (bit5)
U7	221	P02_4	I/O	A	General-purpose input/output port
		D12			Signal pin of external data bus (bit12)
U9	223	P01_3	I/O	A	General-purpose input/output port
		D19			Signal pin of external data bus (bit19)
U11	225	P00_2	I/O	A	General-purpose input/output port
		D26			Signal pin of external data bus (bit26)
U12	226	P10_3	I/O	A	General-purpose input/output port
		WEX			Write enable output pin
U14	228	TCK	I	I	Boundary Scan Test Clock input pin

JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
U16	230	INITX	I	H	External reset input pin
T17	232	P20_6	I/O	A	General-purpose input/output port
		SCK3			Clock input/output pin of USART3
		ZIN1			Up/down counter input pin
		CK3			External clock input pin of free-run timer 3
P17	234	P19_6	I/O	A	General-purpose input/output port
		SCK5			Clock input/output pin of USART5
		CK5			External clock input pin of free-run timer 5
M17	236	P18_5	I/O	A	General-purpose input/output port
		SOT7			Data output pin of USART7
		BIN3			Up/down counter input pin
K17	238	P17_5	I/O	B	General-purpose input/output port
		PPG5			Output pin of PPG timer
		AN37			Analog input pin of A/D converter (second A/D macro)
J17	239	P23_1	I/O	A	General-purpose input/output port
		TX0			TX output pin of CAN0
G17	241	P29_1	I/O	B	General-purpose input/output port
		AN1			Analog input pin of A/D converter
E17	243	P29_7	I/O	B	General-purpose input/output port
		AN7			Analog input pin of A/D converter
D16	245	P27_6	I/O	B	General-purpose input/output port
		AN22			Analog input pin of A/D converter
		INT22			External interrupt pin
D14	247	P26_3	I/O	B	General-purpose input/output port
		AN27			Analog input pin of A/D converter
		INT27			External interrupt pin
D12	249	P26_7	I/O	B	General-purpose input/output port
		AN31			Analog input pin of A/D converter
		INT31			External interrupt pin
D10	251	P14_1	I/O	A	General-purpose input/output port
		ICU1			Input capture input pin
		TIN1			External trigger input pin of reload timer
		TTG9/1			External trigger input pin of PPG timer
D9	252	P14_5	I/O	A	General-purpose input/output port
		ICU5			Input capture input pin
		TIN5			External trigger input pin of reload timer
		TTG13/5			External trigger input pin of PPG timer

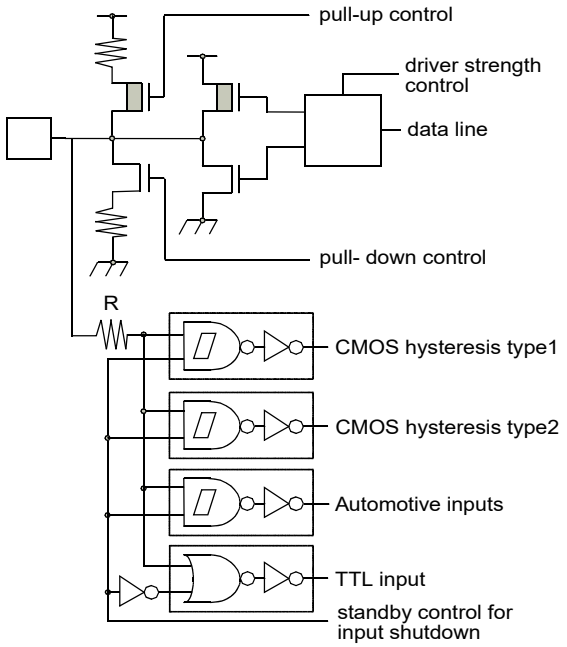
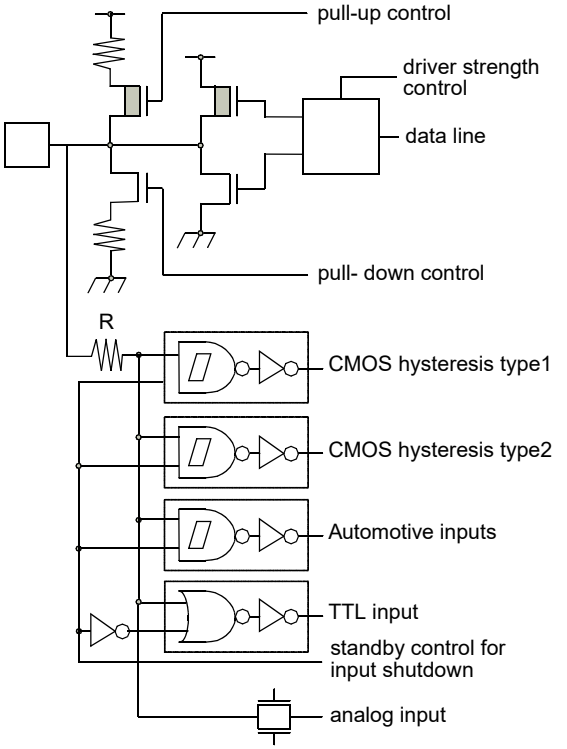
JEDEC	Pin No.	Pin Name	I/O	I/O Circuit Type [1]	Description
D7	254	P16_4	I/O	A	General-purpose input/output port
		PPG12			PPG timer output pin
		SGA			SGA output pin of sound generator
D5	256	P15_3	I/O	A	General-purpose input/output port
		OCU3			Output compare output pin
		TOT3			Reload timer output pin

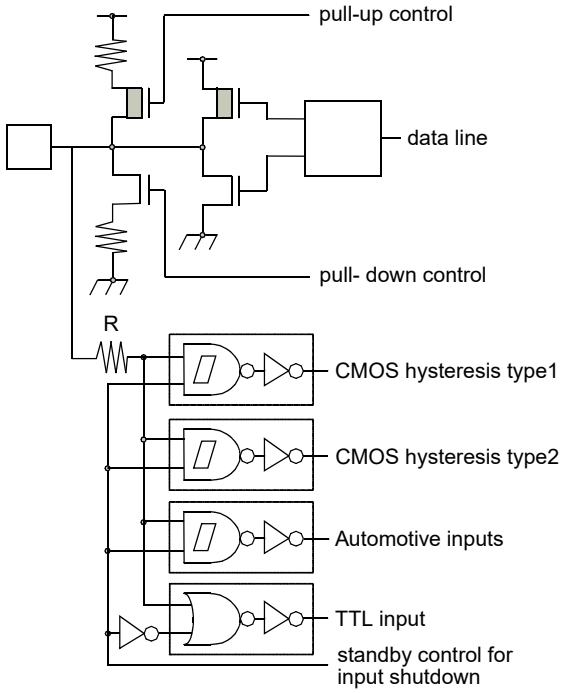
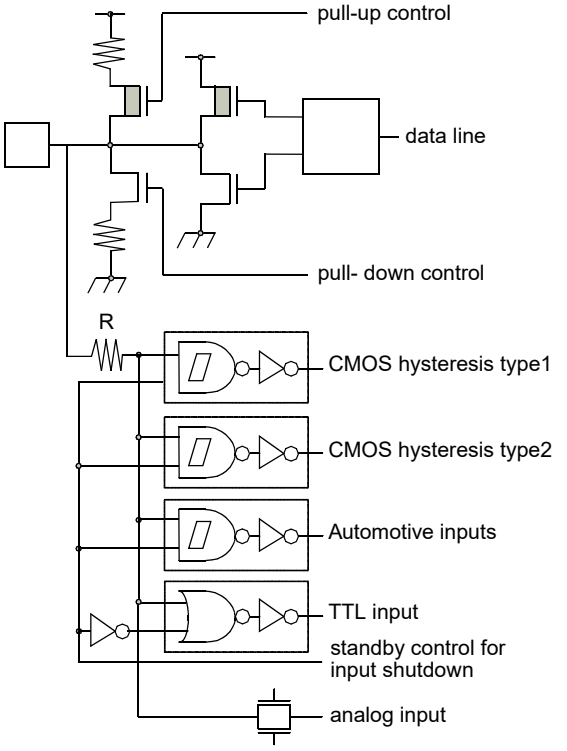
1. For information about the I/O circuit type, refer to “4. I/O Circuit Types”.
2. For usage of ICU8, PFR22[7] must be cleared and DDR22[7] should be cleared.
3. For usage of ICU9, PFR22[6] must be cleared and DDR22[6] should be cleared.

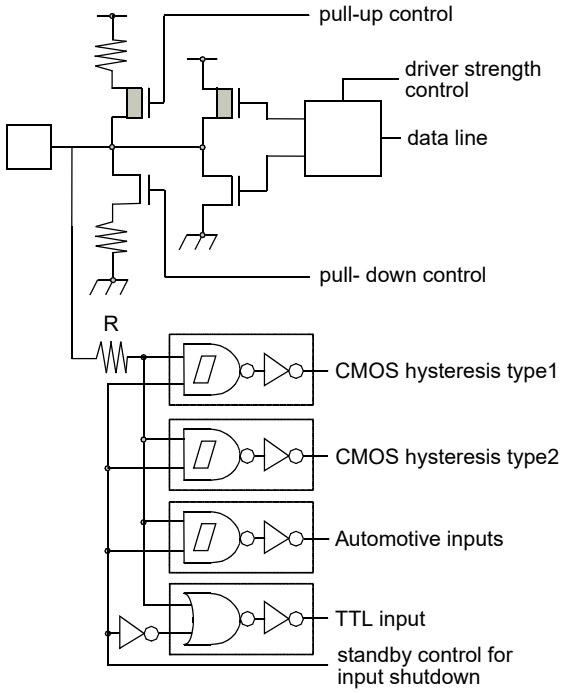
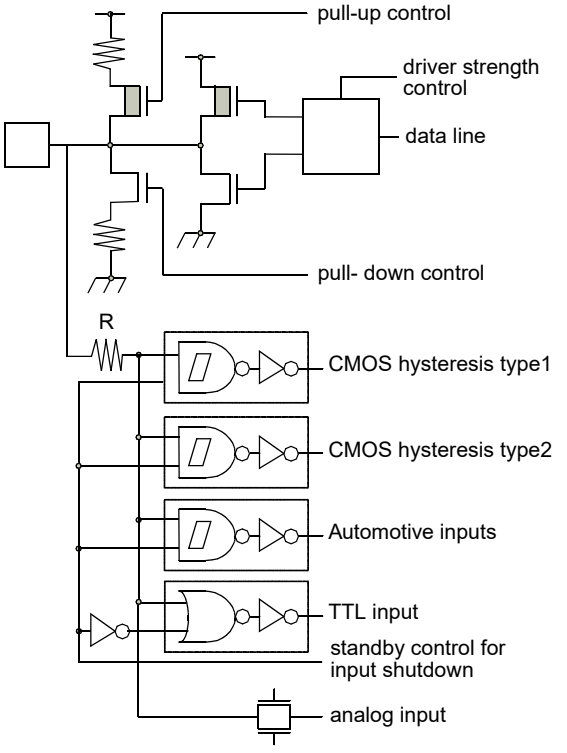
[Power supply/Ground pins]

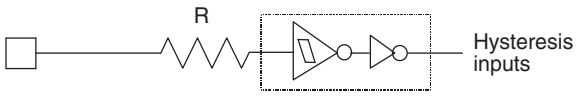
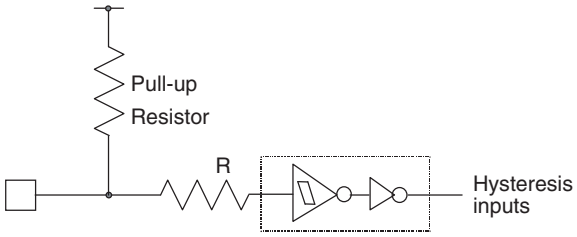
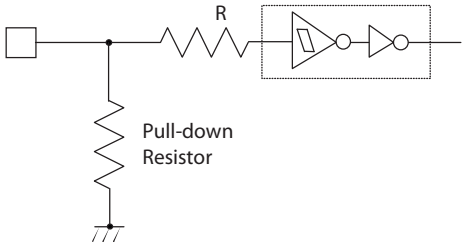
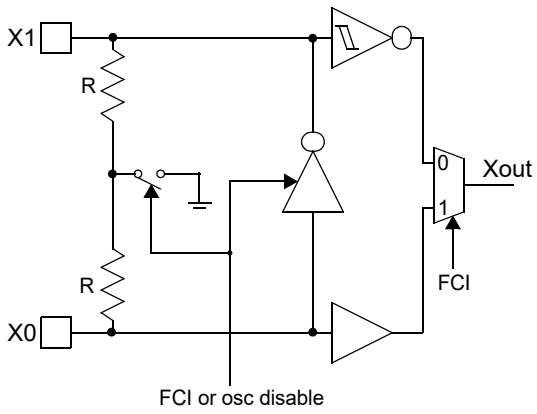
Pin No. (JEDEC)	Pin Name	Description
1 (A1),20(Y1),34(Y15),39 (Y20), 58 (A20),205 (D4),209 (H4), 214 (N4),218 (U4),222 (U8), 227 (U13),231 (U17),235 (N17), 240 (H17),244 (D17),248 (D13), 253 (D8) 257 to 320 (G7..G14....P7..P14)	VSS	GND pins
233 (R17),237 (L17),242 (F17), 246 (D15),250 (D11),255 (D6)	VDD5	Power supply pins
207 (F4), 211 (K4),216 (R4), 220 (U6),224 (U10),229 (U15)	VDD35	Power supply pins for external bus
36 (Y17),37(Y18)	VDD5R	Power supply pin for internal regulator
60 (A18)	AVSS	Analog GND pin for A/D converter
63 (A15)	AVCC5	Power supply pin for A/D converter
62 (A16)	AVRH5	Reference power supply pin for A/D converter
38(Y19)	VCC18C	Capacitor connection pin for internal regulator

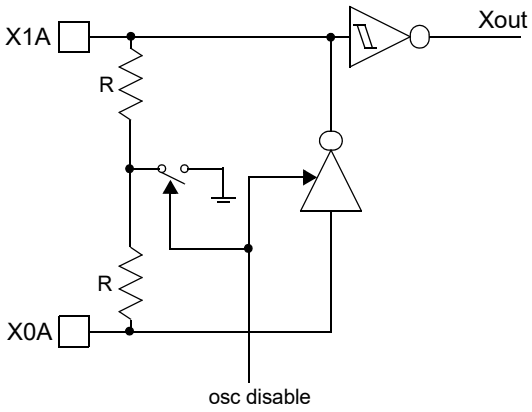
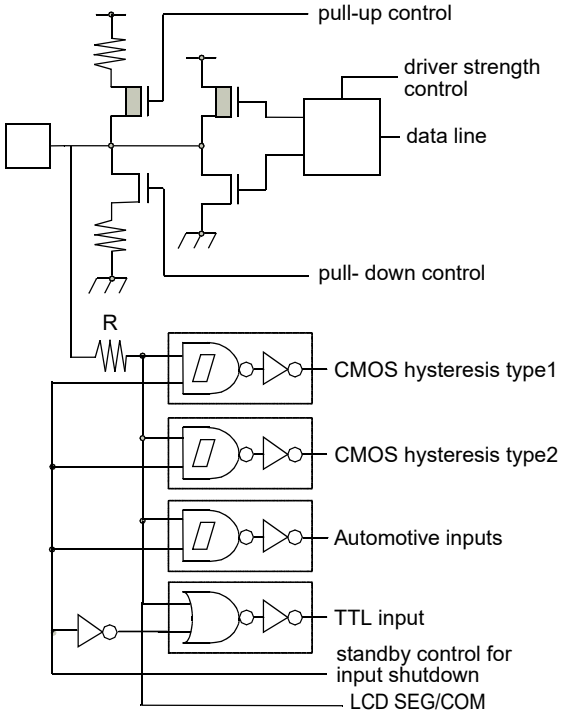
4. I/O Circuit Types

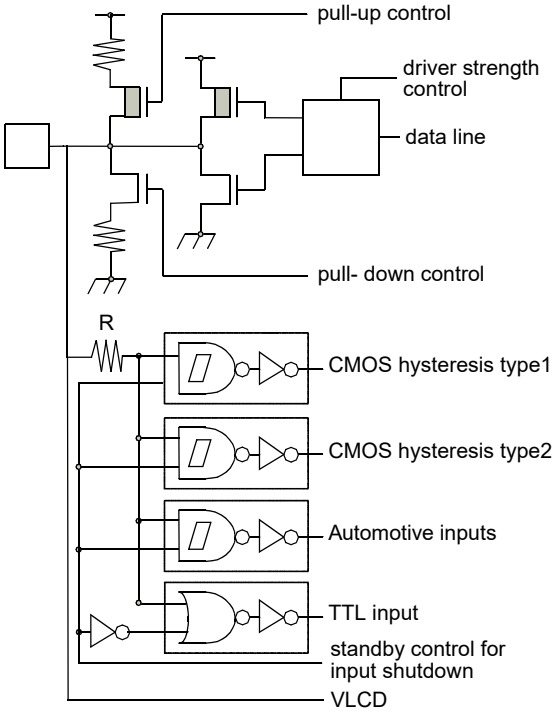
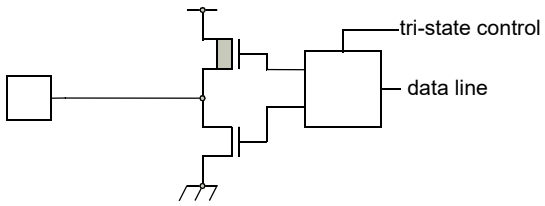
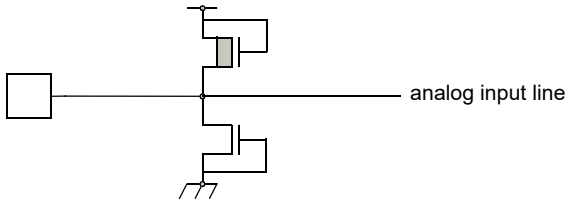
Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

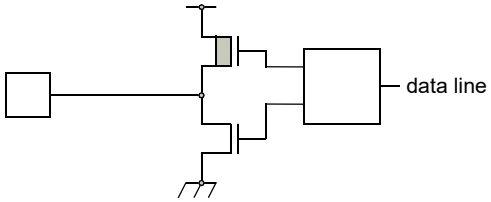
Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
I		CMOS Hysteresis input pin Pull-down resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.

Type	Circuit	Remarks
J2		Low-speed oscillation circuit: • Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output

Type	Circuit	Remarks
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

Type	Circuit	Remarks
O		CMOS level output (I_{OL} = 5mA, I_{OH} = -5mA)

5. Special Port / Resource Assignments

In general, the port / resource assignments and the necessary register settings (PFR, EPFR) are described in the CY91460 series hardware manual. The assignments of CY91460Q series are different on some ports. This chapter explains the differences and the settings needed to enable the resources.

5.1 Overview of Special Port / Resource Assignments

- CY91460Q series has a second A/D converter (ADC1), serving the channels AN34-39, AN42 and AN46. These analog channels are added to P17[7:2], P18[6] and P18[2].
- CY91460Q series has 16 more external interrupts (INT16-31), added to ports 27 and 26.
- The following external interrupts are re-located to other ports then described in the hardware manual: INT4, INT5, INT10, INT11, INT12, INT14.
- CY91460Q series has 2 more Input Capture Units (ICU8, ICU9) and one more Free Run Timer (FRT8).
- CY91460Q series has different initial function of the external bus IOs

5.2 The Second A/D Converter (ADC1)

The second ADC is of the same macro type then ADC0 (10 bit, 1µs), and it has the same register set.
For the addresses, please refer to the IO MAP at address 0x5E0 to 0x5EB.
The external trigger signal (ATGX) for ADC1 comes from port P16[7] and is the same as for ADC0.
The internal trigger signal for ADC1 comes from Reload Timer 7 and is the same as for ADC0.
The analog input channels are assigned to the following bits of Ports 17 and 18:

Port 17								Func.	Enabled by
P17[7]	P17[6]	P17[5]	P17[4]	P17[3]	P17[2]	P17[1]	P17[0]	GPIO	PFR17=0
PPG7	PPG6	PPG5	PPG4	PPG3	PPG2	PPG1	PPG0	PPG	PFR17=1
AN39	**AN38**	**AN37**	**AN36**	**AN35**	**AN34**	**-**	**-**	**ADC1**	**AD1ER**[m-32]=1

Port 18								Func.	Enabled by
-	P18[6]	P18[5]	P18[4]	-	P18[2]	P18[1]	P18[0]	GPIO	PFR18=0
-	SCK7	SOT7	SIN7	-	SCK6	SOT6	SIN6	LIN	PFR18=1, EPFR18=0
	ZIN3, CK7	BIN3	AIN3	-	ZIN2, CK6	BIN2	AIN2	UDC, FRT	PFR18=1, EPFR18=1
-	**AN46**	**-**	**-**	**-**	**AN42**	**-**	**-**	**ADC1**	**AD1ER**[m-32]=1

m = 32 to 46 (ADC channel)

The analog channel IO is enabled independently of PFR/EPFR. It only depends on the appropriate **AD1ER**[n] bit (ADC channel enable). If an analog channel is enabled, the digital input stages are disabled by hardware. **Analog overwrites digital input.**

5.3 The Additional External Interrupts (INT16-31)

The additional external interrupts are controlled by a second external interrupt controller having similar register set.
For the addresses, please refer to the IO MAP at address 0xC04 to 0xC0B.
The new interrupt functions are assigned to the ports 26 and 27:

Port 26								Func.	Enabled by
P26[7]	P26[6]	P26[5]	P26[4]	P26[3]	P26[2]	P26[1]	P26[0]	GPIO	PFR26=0
-	-	-	-	-	-	-	-	[SMC]	PFR26=1, EPFR26=0
AN31	AN30	AN29	AN28	AN27	AN26	AN25	AN24	ADC0	PFR26=1, EPFR26=1
INT31	**INT30**	**INT29**	**INT28**	**INT27**	**INT26**	**INT25**	**INT24**	**INT**	**PFR27=1, EPFR27=1, ENIR3[m-24]=1 and ADERH[an-16]=0**

Port 27								Func.	Enabled by
P27[7]	P27[6]	P27[5]	P27[4]	P27[3]	P27[2]	P27[1]	P27[0]	GPIO	PFR27=0
-	-	-	-	-	-	-	-	[SMC]	PFR27=1, EPFR27=0
AN23	AN22	AN21	AN20	AN19	AN18	AN17	AN16	ADC0	PFR27=1, EPFR27=1
INT23	**INT22**	**INT21**	**INT20**	**INT19**	**INT218**	**INT17**	**INT16**	**INT**	**PFR27=1, EPFR27=1, ENIR2[m-16]=1 and ADERH[an-16]=0**

m = 16 to 31 (INT channel)
an = 16 to 31 (ADC channel)

Note: CY91460Q series does not have Stepper Motor Controllers (SMC). On other devices of CY91460 series, the SMC lines are located on ports 25 to 27 and enabled by setting PFR=1, EPFR=0.

The new interrupts are assinged to ports having analog functions (SMC, ADC).
If an analog function is enabled on a pin, then all digital input functionality of this pin is disabled by hardware, and it is not possible to use the interrupt function. Analog overwrites digital input!

The ADC functions are enabled by setting PFR=1, EPFR=1 and ADREH=1 (ADERH is ADC channel enable register of ADC0. If the ADC functions are enabled, the digital input lines are disabled. CMOS-Schmitt, Automotive and CMOS-2 level input lines keep their value (bus holder behaviour) while the TTL input line is tied to low level. In this state, external interrupts cannot be used.
If the analog functions are disabled (ADREH=0), the interrupt can be used after setting the appropriate interrupt channel enable bit in ENIR2/EINR3 register as well as PFR and EPFR. Setting these registers enables the digital input stages for wakeup in STOP mode.

5.4 Re-located External Interrupts (INT4, INT5, INT10, INT11, INT12, INT14)

The re-located interrupts are assigned to ports different to other devices of CY91460 series:

Port 24		Port 35			Port 34			Func.	Enabled by
P24[4]		P35[4]	P35[0]		P34[5]	P34[4]	P34[0]	GPIO	PFR=0
SDA2		-	-		-	-	-	[LCD]	PFR=1, EPFR=0
-		SIN9	SIN8		SOT11	SIN11	SIN10	I2C/ LIN	PFR=1, EPFR=1
INT14		**INT12**	**INT11**		**INT5**	**INT4**	**INT10**	**ADC1**	**ENIR1/0**[m]=1

Note: CY91460Q series does not have the LCD Controller.
On other devices of CY91460 series, the LCD lines are located on ports 30 to 36 and enabled by setting PFR=1, EPFR=0. This setting would disable the digital input lines on other devices. To keep the software compatible to the new evaluation device, avoid setting PFR=1 & EPFR=0.

Note: Take care about INT5 because it is attached to SOT11 (LIN-USART output direction if PFR=EPFR=1!)
If the LCD function is disabled, the interrupt can be used after setting the appropriate interrupt channel enable bit in ENIR0/EINR1 register. Setting ENIR0/ENIR1 enables the digital input stages for wakeup in STOP mode. But setting ENIR does **not** switch the port direction to input mode. The user should take care that the port is operating in input direction before expecting external interrupts.

5.5 Input Capture Units (ICU8,9) and Free Run Timer (FRT8)

CY91460Q series has 2 more ICUs and one more FRT. The assignments are the following:

Port 22			Port 21		Func.	Enabled by	Comments
P22[7]	P22[6]		P21[2]		GPIO	PFR=0	
SCL1	SDA1		SCK0		I2C / LIN	PFR=1	Port 22 does not have EPFR.
-	INT15		-		INT	PFR=1	Port 22 does not have EPFR.
-	-		CK0**/8**		FRT	PFR=1, EPFR=1	PFR=1 & EPFR=1 just switches the port 21[2] to input direction. FRT8 uses the same input signal as FRT0.
ICU9	**ICU8**		**-**		**ICU**	**PFR=1 or PFR=0**	PFR switches the ICU input signal between LIN-USART.LSYNC and the pin.

PFR22[7:6] switch the input signals of the ICU modules 9 and 8:

PFR	Value	ICU input connection
PFR22[7]	0	ICU9 input is connected to port 22[7] input line (default)
	1	ICU9 input is connected to the LSYNC output of LIN-USART9
PFR22[6]	0	ICU8 input is connected to port 22[6] input line (default)
	1	ICU8 input is connected to the LSYNC output of LIN-USART8

Note: For ICU0-7, this multiplexing is controlled by EPFR14 register.

5.6 External Bus Function After Reset

Older devices of CY91460 series switch on the external bus after reset by setting the PFR registers of the ports 00 to 10. This behaviour appears in external vector fetch mode (MD[2:0]=001) as well as in internal vector fetch mode (MD[2:0]=000).
New devices of CY91460 series (including CY91460Q) do **not** switch on the external bus in internal vector fetch mode (MD[2:0]=000).

6. Handling Devices

6.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$) or less than ($V_{SS}5$) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

6.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

6.3 Power Supply Pins

In CY91460Q series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the CY91460Q series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

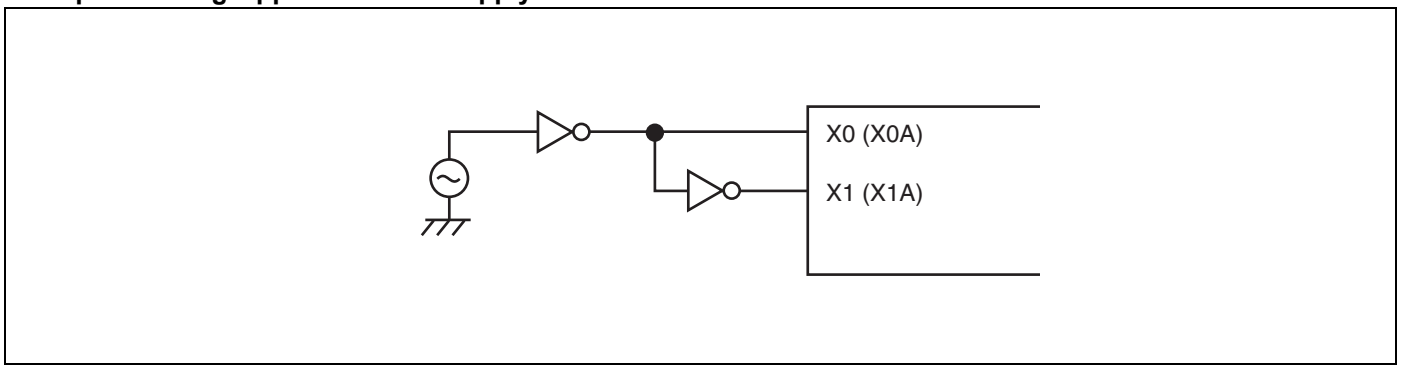
6.4 Crystal Oscillator Circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

6.5 Notes on Using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Example of Using Opposite Phase Supply



6.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

6.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

6.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

6.9 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event,
the operation before and after the EIT always proceeds according to specification.

The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

(a) a user interrupt or NMI is accepted;

(b) single-step execution is performed;

(c) execution breaks due to a data event or from the emulator menu.

1. D0 and D1 flags are updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.

1. The PS register is updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

7. Notes on Debugger

7.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

7.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

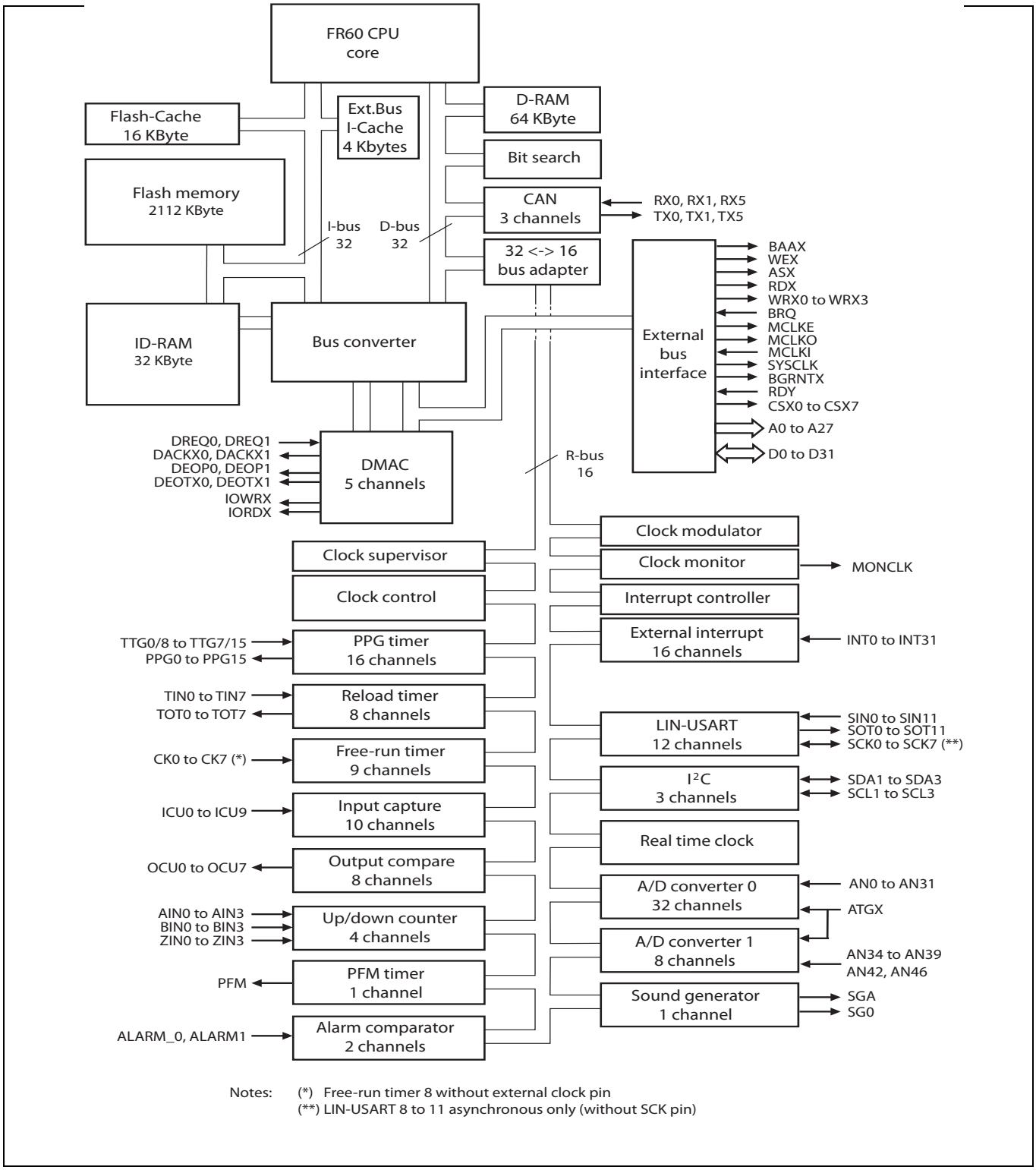
To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

7.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

8. Block Diagram

8.1 CY91F469QA



Notes: (*) Free-run timer 8 without external clock pin
(**) LIN-USART 8 to 11 asynchronous only (without SCK pin)

9. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

9.1 Features

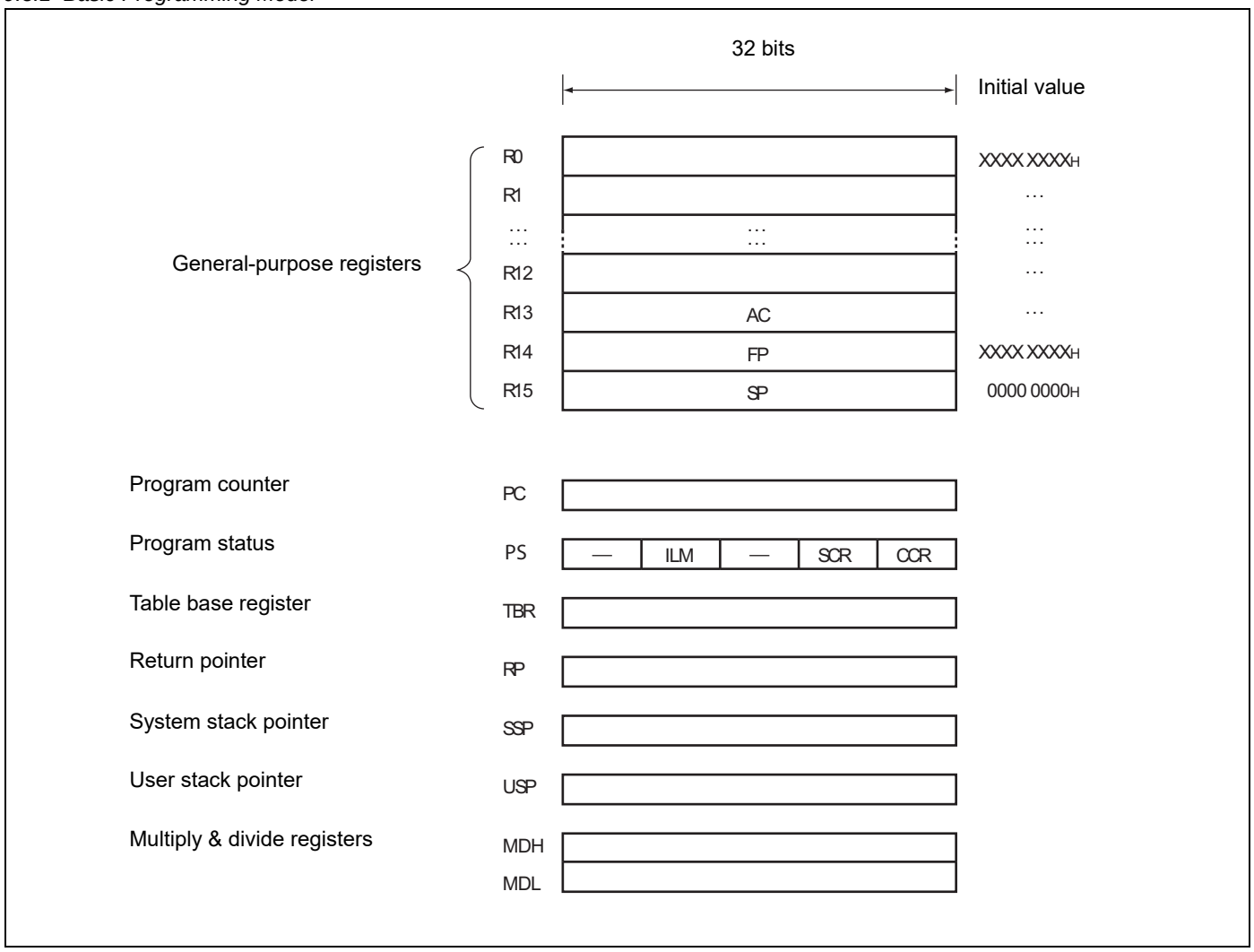
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

9.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

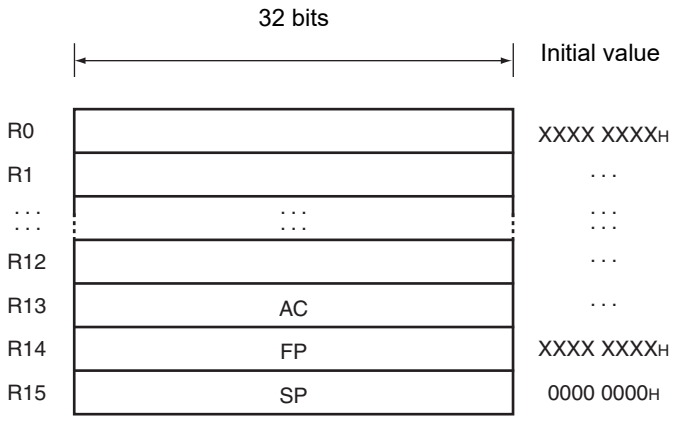
9.3 Programming Model

9.3.1 Basic Programming Model



9.4 Registers

9.4.1 General-purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

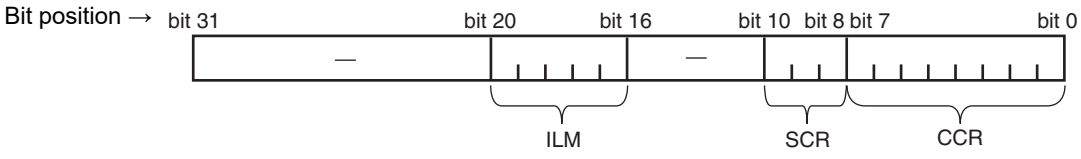
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

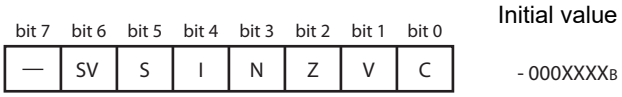
9.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



9.4.3 CCR (Condition Code Register)



SV : Supervisor flag

S : Stack flag

I : Interrupt enable flag

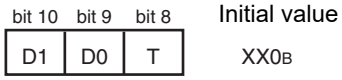
N : Negative enable flag

Z : Zero flag

V : Overflow flag

C : Carry flag

9.4.4 SCR (System Condition Register)



Flag for step division (D1, D0)

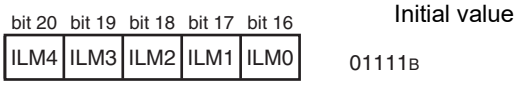
This flag stores interim data during execution of step division.

Step trace trap flag (T)

This flag indicates whether the step trace trap is enabled or disabled.

The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

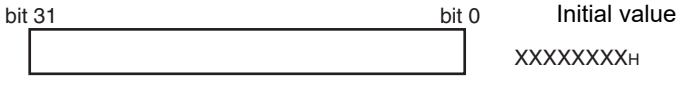
9.4.5 ILM (Interrupt Level Mask Register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111_B” at reset.

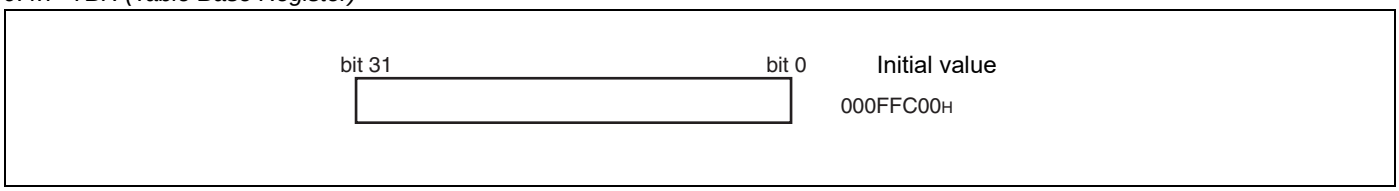
9.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

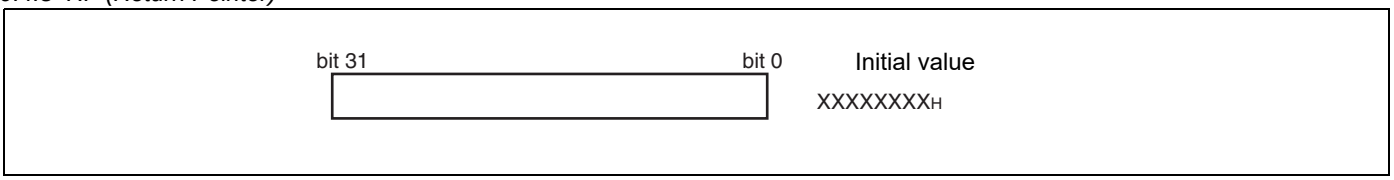
9.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

9.4.8 RP (Return Pointer)



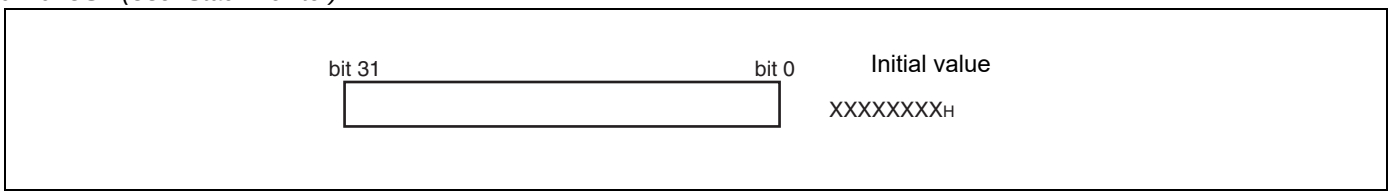
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

9.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

9.4.10 Multiply & Divide Registers

These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

10. Embedded Program/Data Memory (Flash)

10.1 Flash Features

- CY91F469QA: 2112 Kbytes (32 × 64 Kbytes + 8 × 8 Kbytes = 16.5 Mbits)
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0x0024:8000 - 0x0024:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

10.2 Operation Modes

1. 64-bit CPU mode:
   - CPU reads and executes programs in word (32-bit) length units.
   - Flash writing is not possible.
   - Actual Flash Memory access is performed in d-word (64-bit) length units.
2. 32-bit CPU mode :
   - CPU reads and executes programs in word (32-bit) length units.
   - Actual Flash Memory access is performed in word (32-bit) length units.
3. 16-bit CPU mode :
   - CPU reads and writes in half-word (16-bit) length units.
   - Program execution from the Flash is not possible.
   - Actual Flash Memory access is performed in half-word (16-bit) length units.

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching”.

10.3 Flash Access in CPU Mode

10.3.1 Flash Configuration

Flash Memory Map CY91F469QA

Address									
0024:FFFFh 0024:C000h	SA6 (8KB)				SA7 (8KB)				ROMS10
0024:BFFFh 0024:8000h	SA4 (8KB)				SA5 (8KB)				
0024:7FFFh 0024:4000h	SA2 (8KB)				SA3 (8KB)				
0024:3FFFh 0024:0000h	SA0 (8KB)				SA1 (8KB)				
0023:FFFFh 0022:0000h	SA38 (64KB)				SA39 (64KB)				
0021:FFFFh 0020:0000h	SA36 (64KB)				SA37 (64KB)				
001F:FFFFh 001E:0000h	SA34 (64KB)				SA35 (64KB)				ROMS9
001D:FFFFh 001C:0000h	SA32 (64KB)				SA33 (64KB)				
001B:FFFFh 001A:0000h	SA30 (64KB)				SA31 (64KB)				ROMS8
0019:FFFFh 0018:0000h	SA28 (64KB)				SA29 (64KB)				
0017:FFFFh 0016:0000h	SA26 (64KB)				SA27 (64KB)				ROMS7
0015:FFFFh 0014:0000h	SA24 (64KB)				SA25 (64KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit write mode	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit write mode	dat[31:0]				dat[31:0]				

10.3.2 Flash Access Timing Settings in CPU Mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) and voltage supplies for Flash read and write access.

Flash Read Timing Settings (Synchronous Read)

Core Clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Flash/Main Supply Voltage
to 24 MHz	0	0	0	-	1	1.9V *1
to 48 MHz	0	0	1	-	2	1.9V *1
to 100 MHz	1	1	3	-	4	1.9V *1

Flash Write Timing Settings (Synchronous Write)

Core Clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Flash/Main Supply Voltage
to 16 MHz	0	-	-	0	3	1.9V *1
to 32 MHz	0	-	-	0	4	1.9V *1
to 48 MHz	0	-	-	0	5	1.9V *1
to 64 MHz	1	-	-	0	6	1.9V *1
to 96 MHz	1	-	-	0	7	1.9V *1
to 100 MHz	1	-	-	1	8	1.9V *1

*1: In order to enter this mode please set REGSEL_FLASHSEL=1 and REGSEL_MAINSEL=1.

10.3.3 Address Mapping from CPU to Parallel Programming Mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

Address Mapping CY91F469QA

CPU Address (addr)	Condition	Flash Sectors	FA (Flash Address) Calculation
24:0000h to 24:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
24:0000h to 24:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2- (addr/2)%4 + addr%4 - 05:0000h + 00:2000h
04:0000h to 23:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22, SA24, SA26, SA28, SA30, SA32, SA34, SA36, SA38 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 1C:0000h
04:0000h to 23:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23, SA25, SA27, SA29, SA31, SA33, SA35, SA37, SA39 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 1C:0000h + 01:0000h

Note: FA result is without 40:0000h offset for parallel Flash programming.
Set offset by keeping FA[22] = 1 as described in section “Parallel Flash programming mode”.

10.4 Parallel Flash Programming Mode

10.4.1 Flash Configuration in Parallel Flash Programming Mode

Parallel Flash Programming Mode (MD[2:0] = 111):

CY91F469QA

FA[21:0]	
003F:FFFFh 003F:0000h	SA39 (64KB)
003E:FFFFh 003E:0000h	SA38 (64KB)
003D:FFFFh 003D:0000h	SA37 (64KB)
003C:FFFFh 003C:0000h	SA36 (64KB)
003B:FFFFh 003B:0000h	SA35 (64KB)
003A:FFFFh 003A:0000h	SA34 (64KB)
0039:FFFFh 0039:0000h	SA33 (64KB)
0038:FFFFh 0038:0000h	SA32 (64KB)
0037:FFFFh 0037:0000h	SA31 (64KB)
0036:FFFFh 0036:0000h	SA30 (64KB)
0035:FFFFh 0035:0000h	SA29 (64KB)
0034:FFFFh 0034:0000h	SA28 (64KB)
0033:FFFFh 0033:0000h	SA27 (64KB)
0032:FFFFh 0032:0000h	SA26 (64KB)
0031:FFFFh 0031:0000h	SA25 (64KB)
0030:FFFFh 0030:0000h	SA24 (64KB)
002F:FFFFh 002F:0000h	SA23 (64KB)
002E:FFFFh 002E:0000h	SA22 (64KB)
002D:FFFFh 002D:0000h	SA21 (64KB)
002C:FFFFh 002C:0000h	SA20 (64KB)
002B:FFFFh 002B:0000h	SA19 (64KB)

002A:FFFFh 002A:0000h	SA18 (64KB)
0029:FFFFh 0029:0000h	SA17 (64KB)
0028:FFFFh 0028:0000h	SA16 (64KB)
0027:FFFFh 0027:0000h	SA15 (64KB)
0026:FFFFh 0026:0000h	SA14 (64KB)
0025:FFFFh 0025:0000h	SA13 (64KB)
0024:FFFFh 0024:0000h	SA12 (64KB)
0023:FFFFh 0023:0000h	SA11 (64KB)
0022:FFFFh 0022:0000h	SA10 (64KB)
0021:FFFFh 0021:0000h	SA9 (64KB)
0020:FFFFh 0020:0000h	SA8 (64KB)
001F:FFFFh 001F:E000h	SA7 (8KB)
001F:DFFFh 001F:C000h	SA6 (8KB)
001F:BFFFh 001F:A000h	SA5 (8KB)
001F:9FFFh 001F:8000h	SA4 (8KB)
001F:7FFFh 001F:6000h	SA3 (8KB)
001F:5FFFh 001F:4000h	SA2 (8KB)
001F:3FFFh 001F:2000h	SA1 (8KB)
001F:1FFFh 001F:0000h	SA0 (8KB)

	FA[1:0]=00	FA[1:0]=10
I6bit write mod	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[22] = 1

10.4.2 Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 16.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External Pins	FR-CPU Mode	CY91F469QA External Pins			Comment
		Flash Memory Mode	Normal Function	Pin Number	
—	INITX	—	INITX	U16 (230)	
RESET	—	FRSTX	P00_6	Y12 (31)	
—	—	MD_2	MD_2	V15 (172)	Set to '1'
—	—	MD_1	MD_1	V16 (173)	Set to '1'
—	—	MD_0	MD_0	V17 (174)	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	P00_0	W10 (102)	
BYTE	Internally fixed to 'H'	BYTEX	P00_2	U11 (225)	
WE	Internal control signal + control via interface circuit	WEX	P01_2	Y8 (27)	
OE		OEX	P01_1	W8 (100)	
CE		CEX	P01_0	V8 (165)	
—		ATDIN	P01_4	V9 (166)	Set to '0'
—		EQIN	P01_3	U9 (233)	Set to '0'
—		TESTX	P00_3	V11 (168)	Set to '1'
—		RDYI	P00_1	Y10 (29)	Set to '0'
A-1	Internal address bus	FA0	P14_6	A8 (70)	Set to '0'
A0 to A7		FA1 to FA8	P16_0 to P16_7	0: C8 (200) 1: A7(71), 2: B7(140), 3: C7(201), 4: D7(254), 5: A6(72), 6: B6(141), 7: C6(202)	

(Continued)

(Continued)

MBM29LV400TC External Pins	FR-CPU Mode	CY91F469QA External Pins			Comment
		Flash Memory Mode	Normal Function	Pin Number	
A8 to A15	Internal address bus	FA9 to FA16	P15_0 to P15_7	0: A5(73), 1: B5(142), 2: C5(203), 3: D5(256), 4: A4(74), 5: B4(143), 6: C4(204), 7: A3(75)	
A16 to A20		FA17 to FA21	P14_0 to P14_4	0: C10(198), 1: D10(251), 2: A9(69), 3: B9(138), 4: C9(199)	
—		FA22	GP14_5	D9 (252)	Set to ‘1’
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P03_0 to P03_7	0: W3(95), 1: Y3(22), 2: V4(161), 3: W4(96), 4: Y4(23), 5: U5(219), 6: V5(162), 7: W5(97)	
DQ8 to DQ15		DQ8 to DQ15	P02_0 to P02_7	0: Y5(24), 1: V6(163), 2: W6(98), 3: Y6(25), 4: U7(221), 5: V7(164), 6: W7(99), 7: Y7(26)	

10.5 Poweron Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on : 2.76 ms
- Minimum wait time after INITX rising : 1.0 ms

10.6 Flash Security

10.6.1 Vector Addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x24:8000 BSV1: 0x24:8004
FSV2: 0x24:8008 BSV2: 0x24:800C

10.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to “0”	set to “0”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “0”	set to “1”	set to “0”	Write Protection (all device modes, without exception)
set all to “0”	set to “0”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes)
set all to “0”	set to “1”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “0”	Write Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes except IN-TVEC mode MD[2:0] = “000”)

FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1 [15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to “0”	set to “1”	
FSV1[1]	SA1	set to “0”	set to “1”	
FSV1[2]	SA2	set to “0”	set to “1”	
FSV1[3]	SA3	set to “0”	set to “1”	
FSV1[4]	SA4	set to “0”	—	write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[8]	—	set to “0”	set to “1”	not available
FSV1[9]	—	set to “0”	set to “1”	not available
FSV1[10]	—	set to “0”	set to “1”	not available
FSV1[11]	—	set to “0”	set to “1”	not available
FSV1[12]	—	set to “0”	set to “1”	not available
FSV1[13]	—	set to “0”	set to “1”	not available
FSV1[14]	—	set to “0”	set to “1”	not available
FSV1[15]	—	set to “0”	set to “1”	not available

Note : It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section “Flash access in CPU mode” for an overview about the sector organization of the Flash Memory.

10.6.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 Kbytes sectors. It is only evaluated if write protection bit FSV1 [17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to “0”	set to “1”	
FSV2[1]	SA9	set to “0”	set to “1”	
FSV2[2]	SA10	set to “0”	set to “1”	
FSV2[3]	SA11	set to “0”	set to “1”	
FSV2[4]	SA12	set to “0”	set to “1”	
FSV2[5]	SA13	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[12]	SA20	set to “0”	set to “1”	
FSV2[13]	SA21	set to “0”	set to “1”	
FSV2[14]	SA22	set to “0”	set to “1”	
FSV2[15]	SA23	set to “0”	set to “1”	
FSV2[16]	SA24	set to “0”	set to “1”	
FSV2[17]	SA25	set to “0”	set to “1”	
FSV2[18]	SA26	set to “0”	set to “1”	
FSV2[19]	SA27	set to “0”	set to “1”	
FSV2[20]	SA28	set to “0”	set to “1”	
FSV2[21]	SA29	set to “0”	set to “1”	
FSV2[22]	SA30	set to “0”	set to “1”	
FSV2[23]	SA31	set to “0”	set to “1”	
FSV2[24]	SA32	set to “0”	set to “1”	
FSV2[25]	SA33	set to “0”	set to “1”	
FSV2[26]	SA34	set to “0”	set to “1”	
FSV2[27]	SA35	set to “0”	set to “1”	
FSV2[28]	SA36	set to “0”	set to “1”	
FSV2[29]	SA37	set to “0”	set to “1”	
FSV2[30]	SA38	set to “0”	set to “1”	
FSV2[31]	SA39	set to “0”	set to “1”	

Note : See section “Flash access in CPU mode” for an overview about the sector organization of the Flash Memory.

10.7 Notes About Flash Memory CRC Calculation

The Flash Security macro contains a feature to calculate the 32-bit checksum over addresses located in the Flash Memory address space. This feature is described in the CY91460 Series Hardware Manual, chapter 55.4.1 “Flash Security Control Register”.

Additional notes are given here:

The CRC calculation runs on the internal RC clock. It is recommended to switch the RC clock frequency to 2 MHz for shortening the calculation time. However, the CPU clock (CLKB) must be faster then RC clock, otherwise the CRC calculation may not start correctly.

11. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct Addressing Area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

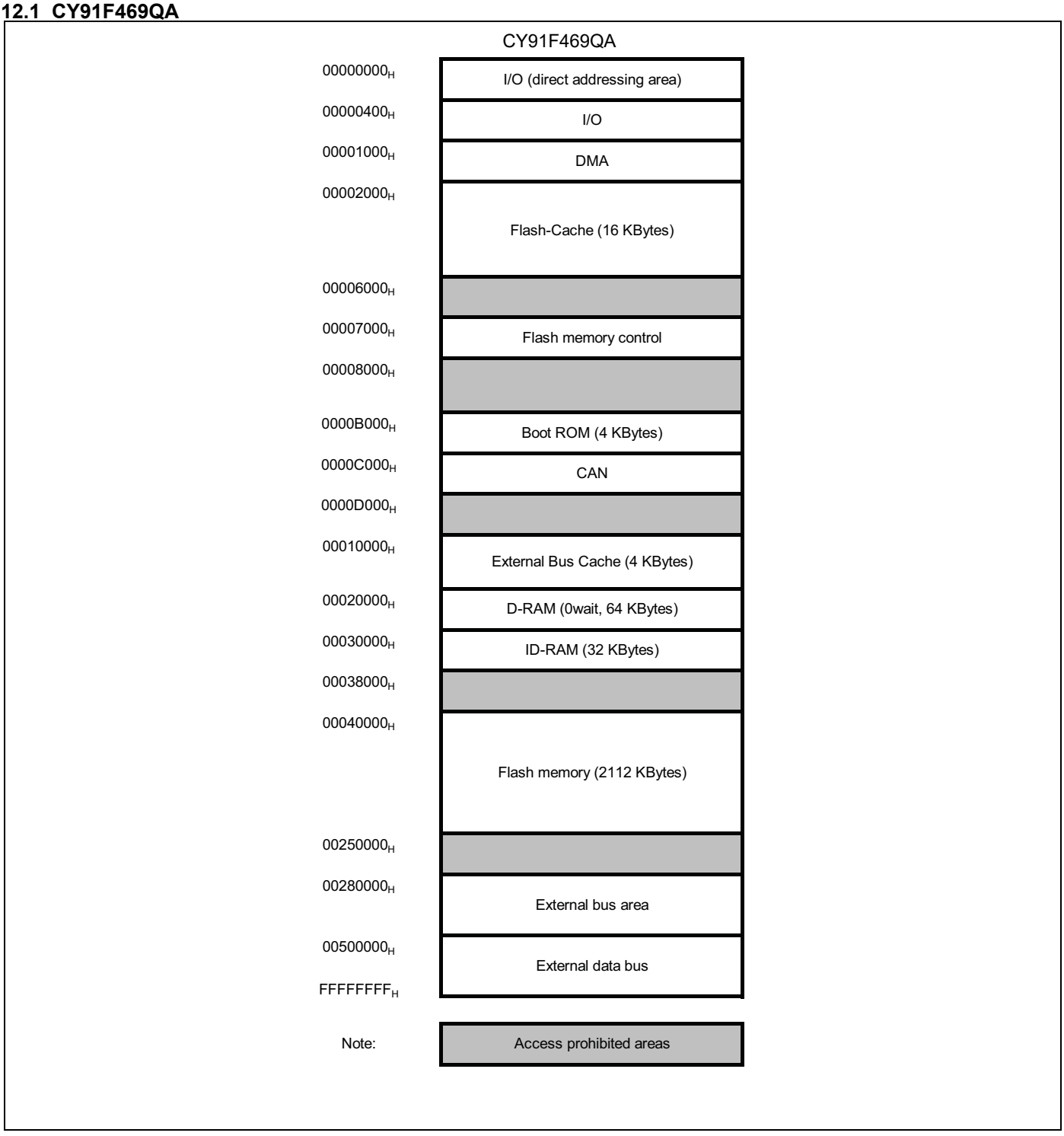
Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

12. Memory Maps

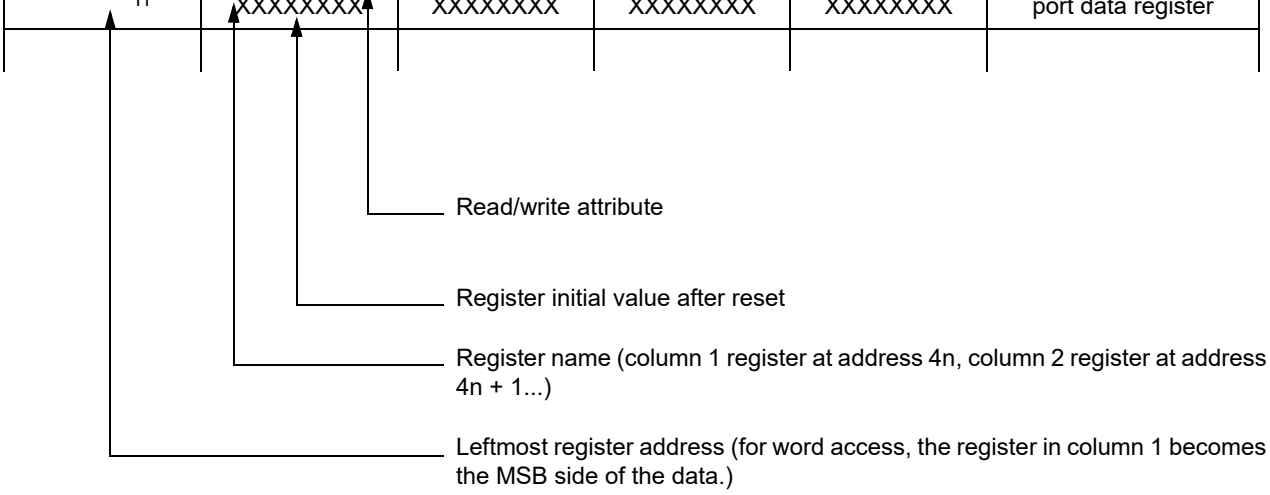
12.1 CY91F469QA



13. I/O Map

13.1 CY91F469QA

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note : Initial values of register bits are represented as follows:

" 1 " : Initial value "1"
" 0 " : Initial value "0"
" X " : Initial value "undefined"
" - " : No physical register at this location
Access is barred with an undefined data access attribute.

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	PDR02 [R/W] XXXXXXXX	PDR03 [R/W] XXXXXXXX	General Purpose IO Port Data Register
000004_H	PDR04 [R/W] - - - - XXXX	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] XXXXXXXX	PDR09 [R/W] XXXXXXXX	PDR10 [R/W] - XXXXXXX	PDR11 [R/W] - - - - - - XX	
$00000C_H$	reserved	PDR13 [R/W] XXXXXXXX	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - XXX - XXX	PDR22 [R/W] XX - - XX - -	PDR23 [R/W] - - - - XXXX	
000018_H	PDR24 [R/W] XXXXXXXX	reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	reserved	reserved	
000020_H	reserved	reserved	PDR34 [R/W] - - XX - -XX	PDR35 [R/W] - - XX - -XX	
000024_H - $00002C_H$	reserved				reserved
000030_H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		Ext. INT 0-7 NMI
000034_H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		Ext. INT 8-15
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	reserved		DLYI/I-unit
$00003C_H$	reserved				reserved
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	reserved		
000048_H	SCR01 [R/W,W] 00000000	SMR01 [R/W,W] 00000000	SSR01 [R/W,R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
$00004C_H$	ESCR01 [R/W] 00000X00	ECCR01 [R/W,R,W] -00000XX	reserved		
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	reserved		

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000058_H	SCR03[R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR02 [R/W] 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	reserved		
000060_H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070_H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078_H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baudrate Generator LIN-USART 0-7
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090_H - $0000CC_H$	reserved				reserved
$0000D0_H$ - 0000D8H	reserved				reserved
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I2C 1
$0000E0_H$	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
$0000E4_H$	reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] 00011111	reserved	

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$0000E8_H$ - $0000FC_H$	reserved				reserved
000100_H	GCN10 [R/W] 00110010 00010000		reserved	GCN20 [R/W] - - - - 0000	PPG Control 0-3
000104_H	GCN11 [R/W] 00110010 00010000		reserved	GCN21 [R/W] - - - - 0000	PPG Control 4-7
000108_H	GCN12 [R/W] 00110010 00010000		reserved	GCN22 [R/W] - - - - 0000	PPG Control 8-11
$00010C_H$	reserved				reserved
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	Pulse Frequency Modulator
000174_H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178_H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
$00017C_H$	reserved				reserved
000180_H	reserved	ICS01 [R/W] 00000000	reserved	ICS23 [R/W] 00000000	Input Capture 0-3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0-3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter 0
$0001A4_H$	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	reserved	ACSR0 [R/W] 011XXX00	reserved	ACSR1 [R/W] 011XXX00	Alarm Comparator 0-1
$0001B0_H$	TMRLRC0 [W] XXXXXXXX XXXXXXXX		TMRC0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0-1)
$0001B4_H$	reserved		TMCSRCH0 [R/W] - - - 00000	TMCSRCL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLRC1 [W] XXXXXXXX XXXXXXXX		TMRC1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2-3)
$0001BC_H$	reserved		TMCSRCH1 [R/W] - - - 00000	TMCSRCL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLRC2 [W] XXXXXXXX XXXXXXXX		TMRC2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4-5)
$0001C4_H$	reserved		TMCSRCH2 [R/W] - - - 00000	TMCSRCL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLRC3 [W] XXXXXXXX XXXXXXXX		TMRC3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6-7)
$0001CC_H$	reserved		TMCSRCH3 [R/W] - - - 00000	TMCSRCL3 [R/W] 0 - 000000	
$0001D0_H$	TMRLRC4 [W] XXXXXXXX XXXXXXXX		TMRC4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8-9)
$0001D4_H$	reserved		TMCSRCH4 [R/W] - - - 00000	TMCSRCL4 [R/W] 0 - 000000	
$0001D8_H$	TMRLRC5 [W] XXXXXXXX XXXXXXXX		TMRC5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG10-11)
$0001DC_H$	reserved		TMCSRCH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLRC6 [W] XXXXXXXX XXXXXXXX		TMRC6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12-13)
$0001E4_H$	reserved		TMCSRCH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMRC7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14-15) (A/D Converter)
$0001EC_H$	reserved		TMCSRCH7 [R/W] - - - 00000	TMCSRCL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] 00000000 00000000		reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0-1)
$0001F4_H$	TCDT1 [R/W] 00000000 00000000		reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2-3)
$0001F8_H$	TCDT2 [R/W] 00000000 00000000		reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0-1)
$0001FC_H$	TCDT3 [R/W] 00000000 00000000		reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2-3)
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 0
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 1
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 2
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 3
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 4
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H - $00023C_H$	reserved				reserved
000240_H	DMACR [R/W] 00 - - 0000	reserved			DMAC Control
000244_H - $00027C_H$	reserved				reserved

	Register				
Address	+0	+1	+2	+3	Block
000280_H	SCR08 [R/W,W] 00000000	SMR08 [R/W,W] 00000000	SSR08 [R/W,R] 00001000	RDR08/TDR08 [R/W] 00000000	LIN-USART (FIFO) 8
000284_H	ESCR08 [R/W] 00000X00	ECCR08 [R/W,R,W] -00000XX	FSR08 [R] - - - 00000	FCR08 [R/W] 0001 - 000	
000288_H	SCR09 [R/W,W] 00000000	SMR09 [R/W,W] 00000000	SSR09 [R/W,R] 00001000	RDR09/TDR09 [R/W] 00000000	LIN-USART (FIFO) 9
$00028C_H$	ESCR09 [R/W] 00000X00	ECCR09 [R/W,R,W] -00000XX	FSR09 [R] - - - 00000	FCR09 [R/W] 0001 - 000	
000290_H	SCR10 [R/W,W] 00000000	SMR10 [R/W,W] 00000000	SSR10 [R/W,R] 00001000	RDR10/TDR10 [R/W] 00000000	LIN-USART (FIFO) 10
000294_H	ESCR10 [R/W] 00000X00	ECCR10 [R/W,R,W] -00000XX	FSR10 [R] - - - 00000	FCR10 [R/W] 0001 - 000	
000298_H	SCR11 [R/W,W] 00000000	SMR11 [R/W,W] 00000000	SSR11 [R/W,R] 00001000	RDR11/TDR11 [R/W] 00000000	LIN-USART (FIFO) 11
$00029C_H$	ESCR11 [R/W] 00000X00	ECCR11 [R/W,R,W] -00000XX	FSR11 [R] - - - 00000	FCR11 [R/W] 0001 - 000	
$0002A0_H$ - $0002BC_H$	reserved				reserved
$0002C0_H$	BGR108 [R/W] 00000000	BGR008 [R/W] 00000000	BGR109 [R/W] 00000000	BGR009 [R/W] 00000000	Baudrate Generator LIN-USART 8-11
$0002C4_H$	BGR110 [R/W] 00000000	BGR010 [R/W] 00000000	BGR111 [R/W] 00000000	BGR011 [R/W] 00000000	
$0002C8_H$ - $0002CC_H$	reserved				reserved
$0002D0_H$	reserved	ICS45 [R/W] 00000000	reserved	ICS67 [R/W] 00000000	Input Capture 4-7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - -0 - -00 0000 - -00		OCS67 [R/W] - - -0 - -00 0000 - -00		Output Compare 4-7
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
$0002E8_H$ - $0002EC_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$0002F0_H$	TCDT4 [R/W] 00000000 00000000		reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4-5)
$0002F4_H$	TCDT5 [R/W] 00000000 00000000		reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6-7)
$0002F8_H$	TCDT6 [R/W] 00000000 00000000		reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4-5)
$0002FC_H$	TCDT7 [R/W] 00000000 00000000		reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6-7)
000300_H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0-1
000304_H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	reserved	UDCS0 [R/W] 00000000	
000308_H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	reserved	UDCS1 [R/W] 00000000	
$00030C_H$	reserved				reserved
000310_H	UDRC3 [W] 00000000	UDRC2 [W] 00000000	UDCR3 [R] 00000000	UDCR2 [R] 00000000	Up/Down Counter 2-3
000314_H	UDCCH2 [R/W] 00000000	UDCCL2 [R/W] 00001000	reserved	UDCS2 [R/W] 00000000	
000318_H	UDCCH3 [R/W] 00000000	UDCCL3 [R/W] 00001000	reserved	UDCS3 [R/W] 00000000	
$00031C_H$	reserved				reserved
000320_H	GCN13 [R/W] 00110010 00010000		reserved	GCN23 [R/W] - - - - 0000	PPG Control 12-15
000324_H - $00032C_H$	reserved				reserved
000330_H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334_H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338_H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
$00033C_H$	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340_H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344_H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000348_H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
$00034C_H$	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350_H - 000364_H	reserved				reserved
000368_H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] - - - - - - 00	ITBAL2 [R/W] 00000000	I2C 2
$00036C_H$	ITMKH2 [R/W] 00 - - - - 11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] - 0000000	
000370_H	reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] 00011111	reserved	
000374_H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] - - - - - - 00	ITBAL3 [R/W] 00000000	I2C 3
000378_H	ITMKH3 [R/W] 00 - - - - 11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] - 0000000	
$00037C_H$	reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] 00011111	reserved	
000380_H - $00038C_H$	reserved				reserved
000390_H	ROMS [R] 11111000 00000000		reserved		ROM Select register
000394_H - $0003BC_H$	reserved				reserved
$0003C0_H$	reserved				I-Cache
$0003C4_H$	reserved			ISIZE [R/W] - - - - - - 10	
$0003C8_H$ - $0003E0_H$	reserved				reserved
$0003E4_H$	reserved			ICHCR [R/W] 0 - 000000	I-Cache
$0003E8_H$ - $0003EC_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H - $00043C_H$	reserved				reserved
000440_H	ICR00 [R/W] - - - 11111	ICR01 [R/W] - - - 11111	ICR02 [R/W] - - - 11111	ICR03 [R/W] - - - 11111	Interrupt Control register
000444_H	ICR04 [R/W] - - - 11111	ICR05 [R/W] - - - 11111	ICR06 [R/W] - - - 11111	ICR07 [R/W] - - - 11111	
000448_H	ICR08 [R/W] - - - 11111	ICR09 [R/W] - - - 11111	ICR10 [R/W] - - - 11111	ICR11 [R/W] - - - 11111	
$00044C_H$	ICR12 [R/W] - - - 11111	ICR13 [R/W] - - - 11111	ICR14 [R/W] - - - 11111	ICR15 [R/W] - - - 11111	
000450_H	ICR16 [R/W] - - - 11111	ICR17 [R/W] - - - 11111	ICR18 [R/W] - - - 11111	ICR19 [R/W] - - - 11111	
000454_H	ICR20 [R/W] - - - 11111	ICR21 [R/W] - - - 11111	ICR22 [R/W] - - - 11111	ICR23 [R/W] - - - 11111	
000458_H	ICR24 [R/W] - - - 11111	ICR25 [R/W] - - - 11111	ICR26 [R/W] - - - 11111	ICR27 [R/W] - - - 11111	
$00045C_H$	ICR28 [R/W] - - - 11111	ICR29 [R/W] - - - 11111	ICR30 [R/W] - - - 11111	ICR31 [R/W] - - - 11111	
000460_H	ICR32 [R/W] - - - 11111	ICR33 [R/W] - - - 11111	ICR34 [R/W] - - - 11111	ICR35 [R/W] - - - 11111	
000464_H	ICR36 [R/W] - - - 11111	ICR37 [R/W] - - - 11111	ICR38 [R/W] - - - 11111	ICR39 [R/W] - - - 11111	
000468_H	ICR40 [R/W] - - - 11111	ICR41 [R/W] - - - 11111	ICR42 [R/W] - - - 11111	ICR43 [R/W] - - - 11111	
$00046C_H$	ICR44 [R/W] - - - 11111	ICR45 [R/W] - - - 11111	ICR46 [R/W] - - - 11111	ICR47 [R/W] - - - 11111	
000470_H	ICR48 [R/W] - - - 11111	ICR49 [R/W] - - - 11111	ICR50 [R/W] - - - 11111	ICR51 [R/W] - - - 11111	
000474_H	ICR52 [R/W] - - - 11111	ICR53 [R/W] - - - 11111	ICR54 [R/W] - - - 11111	ICR55 [R/W] - - - 11111	
000478_H	ICR56 [R/W] - - - 11111	ICR57 [R/W] - - - 11111	ICR58 [R/W] - - - 11111	ICR59 [R/W] - - - 11111	
$00047C_H$	ICR60 [R/W] - - - 11111	ICR61 [R/W] - - - 11111	ICR62 [R/W] - - - 11111	ICR63 [R/W] - - - 11111	

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX – 00	CTBR [W] XXXXXXXX	Clock Control Unit
000484_H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	reserved				reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Clock Gear Unit
000490_H	PLLCTRL [R/W] - - - - 0000	reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498_H	PORTEN [R/W] - - - - - - 00	reserved			Port Input Enable Control
$00049C_H$	reserved				reserved
$0004A0_H$	reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 – 00 – 0		Watchdog Timer
$0004A4_H$	reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	reserved	
$0004AC_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector /Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration Unit of Sub Oscillation
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		reserved	CMCR [R/W] - 001 - - 00	Clock Modulation
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - 0 - - - 00[1]	reserved		CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] -000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	LV Detection / Hardware-Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 000 - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer
$0004CC_H$	OSCCR [R/W] - - - - - - 00	reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - X - - 00	Main- Oscillation Standby Control Main/Sub Regulator Control

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$0004D0_H$ - $0005DC_H$	reserved				reserved
$0005E0_H$	AD1ERH [R/W] 00000000 00000000		AD1ERL [R/W] 00000000 00000000		A/D Converter 1
$0005E4_H$	AD1CS1 [R/W] 00000000	AD1CS0 [R/W] 00000000	AD1CR1 [R] 000000XX	AD1CR0 [R] XXXXXXXX	
$0005E8_H$	AD1CT1 [R/W] 00010000	AD1CT0 [R/W] 00101100	AD1SCH [R/W] - - - 00000	AD1ECH [R/W] - - - 00000	
$0005EC_H$	reserved				
$0005F0_H$	reserved	ICS89 [R/W] 00000000	reserved	reserved	Input Capture 8-9
$0005F4_H$	IPCP8 [R] XXXXXXXX XXXXXXXX		IPCP9 [R] XXXXXXXX XXXXXXXX		
$0005F8_H$	reserved		rederved		
$0005FC_H$ - 000604_H	reserved				reserved
000608_H	TCDT8 [R/W] 00000000 00000000		reserved	TCCS8 [R/W] 00000000	Free Running Timer 8 (ICU 8-9)
$00060C_H$ - $00063C_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000[2]		External Bus Unit
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
$00065C_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660_H	AWR0 [R/W] 01111111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
$00066C_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670_H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	reserved		External Bus Unit
000674_H	reserved				
000678_H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
$00067C_H$	reserved				
000680_H	CSER [R/W] 00000001	CHER [R/W] 11111111	reserved	TCR [R/W] 0000****[3]	
000684_H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	reserved		
000688_H - $0007F8_H$	reserved				reserved
$0007FC_H$	reserved	MODR [W] XXXXXXXX	reserved		Mode Register
000800_H - $000BFC_H$	reserved				reserved
$000C00_H$	reserved			IOS [R/W] *[4] - - - - - -10	I-Unit

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$000C04_H$	EIRR2 [R/W] XXXXXXXX	ENIR2 [R/W] 00000000	ELVR2 [R/W] 00000000 00000000		Ext. INT 16-23
$000C08_H$	EIRR3 [R/W] XXXXXXXX	ENIR3 [R/W] 00000000	ELVR3 [R/W] 00000000 00000000		Ext. INT 24-31
$000C0C_H$ - $000CFC_H$	reserved				reserved
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	PDRD02 [R] XXXXXXXX	PDRD03 [R] XXXXXXXX	General IO Port Direct Read Data register
$000D04_H$	PDRD04 [R] - - - - XXXX	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] XXXXXXXX	PDRD09 [R] XXXXXXXX	PDRD10 [R] - XXXXXXX	PDRD11 [R] - - - - - - XX	
$000D0C_H$	reserved	PDRD13 [R] XXXXXXXX	PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
$000D14_H$	PDRD20 [R] - XXX - XXX	PDRD21 [R] - XXX - XXX	PDRD22 [R] XX - - XX - -	PDRD23 [R] - - - - XXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	reserved		
$000D20_H$	reserved	reserved	PDRD34 [R] - - XX - -XX	PDRD35 [R] - - XX - -XX	
$000D24_H$ - $000D3C_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	DDR02 [R/W] 00000000	DDR03 [R/W] 00000000	General IO Port Data Direction register
$000D44_H$	DDR04 [R/W] - - - - 0000	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] 00000000	DDR09 [R/W] 00000000	DDR10 [R/W] - 0000000	DDR11 [R/W] - - - - - - 00	
$000D4C_H$	reserved	DDR13 [R/W] 00000000	DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
$000D54_H$	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - 000 - 000	DDR22 [R/W] 00 - - 00 - -	DDR23 [R/W] - - - - 0000	
$000D58_H$	DDR24 [R/W] 00000000	reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	reserved		
$000D60_H$	reserved	reserved	DDR34 [R/W] - - 00 - - 00	DDR35 [R/W] - - 00 - - 00	
$000D64_H$ - $000D7C_H$	reserved				reserved
$000D80_H$	PFR00 [R/W] **00000000** [5] **11111111**	PFR01 [R/W] **00000000** [5] **11111111**	PFR02 [R/W] **00000000** [5] **11111111**	PFR03 [R/W] **00000000** [5] **11111111**	Port Function register
$000D84_H$	PFR04 [R/W] **- - - - 0000** [5] **- - - - 1111**	PFR05 [R/W] **00000000** [5] **11111111**	PFR06 [R/W] **00000000** [5] **11111111**	PFR07 [R/W] **00000000** [5] **11111111**	
$000D88_H$	PFR08 [R/W] **00000000** [5] **11111111**	PFR09 [R/W] **00000000** [5] **11111111**	PFR10 [R/W] **-0000000** [5] **-1111111**	PFR11 [R/W] - - - - - - 00	
$000D8C_H$	reserved	PFR13 [R/W] 00000000	PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
$000D90_H$	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - 000 - 000	PFR22 [R/W] 00 - - 00 - -	PFR23 [R/W] - - - - 0000	
$000D98_H$	PFR24 [R/W] 00000000	reserved	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
$000D9C_H$	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	reserved		
$000DA0_H$	reserved	reserved	PFR34 [R/W] - - 00 - -00	PFR35 [R/W] - - 00 - -00	
$000DA4_H$ - $000DC4_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$000DC8_H$	reserved		EPFR10 [R/W] - - 00 - - - 0	reserved	Extended Port Function register
$000DCC_H$	reserved	EPFR13 [R/W] - 0 - - - 0 - -	EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
$000DD0_H$	EPFR16 [R/W] 0000 - - - -	reserved	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0 - - - 0 - -	
$000DD4_H$	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] - 0 - - - 0 - -	reserved		
$000DD8_H$	reserved		EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
$000DDC_H$	reserved				
$000DE0_H$	reserved		EPFR34 [R/W] - - 00 - - 00	EPFR35 [R/W] - - 00 - - 00	
$000DE4_H$ - $000DFC_H$	reserved				reserved
$000E00_H$	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	PODR02 [R/W] 00000000	PODR03 [R/W] 00000000	Port Output Drive Strength control
$000E04_H$	PODR04 [R/W] - - - - 0000	PODR05 [R/W] 00000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
$000E08_H$	PODR08 [R/W] 00000000	PODR09 [R/W] 00000000	PODR10 [R/W] - 0000000	PODR11 [R/W] - - - - - - 00	
$000E0C_H$	reserved	PODR13 [R/W] 00000000	PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
$000E10_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
$000E14_H$	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - 000 - 000	PODR22 [R/W] 00 - - 00 - -	PODR23 [R/W] - - - - 0000	
$000E18_H$	PODR24 [R/W] 00000000	reserved	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
$000E1C_H$	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	reserved		
$000E20_H$	reserved	reserved	PODR34 [R/W] - - 00 - - 00	PODR35 [R/W] - - 00 - - 00	
$000E24_H$ - $000E3C_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$000E40_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	PILR02 [R/W] 00000000	PILR03 [R/W] 00000000	Port Input Level selection register
$000E44_H$	PILR04 [R/W] - - - - 0000	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
$000E48_H$	PILR08 [R/W] 00000000	PILR09 [R/W] 00000000	PILR10 [R/W] - 0000000	PILR11 [R/W] - - - - - - 00	
$000E4C_H$	reserved	PILR13 [R/W] 00000000	PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - 000 - 000	PILR19 [R/W] - 000 - 000	
$000E54_H$	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - 000 - 000	PILR22 [R/W] 00 - - 00 - -	PILR23 [R/W] - - - - 0000	
$000E58_H$	PILR24 [R/W] 00000000	reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	reserved		
$000E60_H$	reserved	reserved	PILR34 [R/W] - - 00 - - 00	PILR35 [R/W] - - 00 - - 00	
$000E64_H$ - $000E7C_H$	reserved				reserved
$000E80_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	EPILR02 [R/W] 00000000	EPILR03 [R/W] 00000000	Extended Port Input Level selection register
$000E84_H$	EPILR04 [R/W] - - - - 0000	EPILR05 [R/W] 00000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
$000E88_H$	EPILR08 [R/W] 00000000	EPILR09 [R/W] 00000000	EPILR10 [R/W] - 0000000	EPILR11 [R/W] - - - - - - 00	
$000E8C_H$	reserved	EPILR13 [R/W] 00000000	EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - 000 - 000	EPILR22 [R/W] 00 - - 00 - -	EPILR23 [R/W] - - - - 0000	
$000E98_H$	EPILR24 [R/W] 00000000	reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	reserved		
$000EA0_H$	reserved	reserved	EPILR34 [R/W] - - 00 - - 00	EPILR35 [R/W] - - 00 - - 00	
$000EA4_H$ - $000EBC_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	PPER02 [R/W] 00000000	PPER03 [R/W] 00000000	Port Pull-Up/Down Enable register
$000EC4_H$	PPER04 [R/W] - - - - 0000	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 00000000	PPER09 [R/W] 00000000	PPER10 [R/W] - 0000000	PPER11 [R/W] - - - - - - 00	
$000ECC_H$	reserved	PPER13 [R/W] 00000000	PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - 000 - 000	PPER22 [R/W] 00 - - 00 - -	PPER23 [R/W] - - - - 0000	
$000ED8_H$	PPER24 [R/W] 00000000	reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	reserved		
$000EE0_H$	reserved	reserved	PPER34 [R/W] - - 00 - - 00	PPER35 [R/W] - - 00 - - 00	
$000EE4_H$ - $000EFC_H$	reserved				reserved
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	PPCR02 [R/W] 11111111	PPCR03 [R/W] 11111111	Port Pull-Up/Down Control register
$000F04_H$	PPCR04 [R/W] - - - - 1111	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 11111111	PPCR09 [R/W] 11111111	PPCR10 [R/W] - 1111111	PPCR11 [R/W] - - - - - - 11	
$000F0C_H$	reserved	PPCR13 [R/W] 11111111	PPCR14 [R/W] 11111111	PPCR15 [R/W] 11111111	
$000F10_H$	PPCR16 [R/W] 11111111	PPCR17 [R/W] 11111111	PPCR18 [R/W] - 111 - 111	PPCR19 [R/W] - 111 - 111	
$000F14_H$	PPCR20 [R/W] - 111 - 111	PPCR21 [R/W] - 111 - 111	PPCR22 [R/W] 00 - - 00 - -	PPCR23 [R/W] - - - - 0000	
$000F18_H$	PPCR24 [R/W] 11111111	reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	reserved		
$000F20_H$	reserved	reserved	PPCR34 [R/W] - - 00 - - 00	PPCR35 [R/W] - - 00 - - 00	
$000F24_H$ - $000FFC_H$	reserved				reserved

Address	Register +0	+1	+2	+3	Block
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H - $01FFC_H$	reserved				reserved
002000_H - $005FFC_H$	CY91F469QA Instruction RAM/Flash Cache size is 16KB				Instruction RAM/Flash Cache
006000_H - $006FFC_H$	reserved				reserved
007000_H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ F-Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - 000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - 000000 00000000 00000000				
007014_H - $007FFC_H$	reserved				reserved
008000_H - $00BFFC_H$	CY91F469QA Boot-ROM size is 4 Kbytes (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		reserved		
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$ - $00C02C_H$	reserved				reserved
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		CAN 0 IF 1 Register mirror
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
$00C038_H$ - $00C03C_H$	reserved				reserved
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00C058_H$ - $00C05C_H$	reserved				reserved
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		CAN 0 IF 2 Register mirror
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ - $00C07C_H$	reserved				reserved
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$	TREQR40 [R] 00000000 00000000		TREQR30 [R] 00000000 00000000		
$00C088_H$	TREQR60 [R] 00000000 00000000		TREQR50 [R] 00000000 00000000		
$00C08C_H$	TREQR80 [R] 00000000 00000000		TREQR70 [R] 00000000 00000000		
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$	NEWDT40 [R] 00000000 00000000		NEWDT30 [R] 00000000 00000000		
$00C098_H$	NEWDT60 [R] 00000000 00000000		NEWDT50 [R] 00000000 00000000		
$00C09C_H$	NEWDT80 [R] 00000000 00000000		NEWDT70 [R] 00000000 00000000		
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$	INTPND40 [R] 00000000 00000000		INTPND30 [R] 00000000 00000000		
$00C0A8_H$	INTPND60 [R] 00000000 00000000		INTPND50 [R] 00000000 00000000		
$00C0AC_H$	INTPND80 [R] 00000000 00000000		INTPND70 [R] 00000000 00000000		
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$	MSGVAL40 [R] 00000000 00000000		MSGVAL30 [R] 00000000 00000000		
$00C0B8_H$	MSGVAL60 [R] 00000000 00000000		MSGVAL50 [R] 00000000 00000000		
$00C0BC_H$	MSGVAL80 [R] 00000000 00000000		MSGVAL70 [R] 00000000 00000000		

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00C0C0_H$ - $00C0FC_H$	reserved				reserved
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		reserved		
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		reserved		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$ - $00C12C_H$	reserved				reserved
$00C130_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		CAN 1 IF 1 Register mirror
$00C134_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
$00C138_H$ - $00C13C_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		reserved		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$ - $00C15C_H$	reserved				reserved
$00C160_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		CAN 1 IF 2 Register mirror
$00C164_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
$00C168_H$ - $00C17C_H$	reserved				reserved

	Register				
Address	+0	+1	+2	+3	Block
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
$00C184_H$	TREQR41 [R] 00000000 00000000		TREQR31 [R] 00000000 00000000		
$00C188_H$	TREQR61 [R] 00000000 00000000		TREQR51 [R] 00000000 00000000		
$00C18C_H$	TREQR81 [R] 00000000 00000000		TREQR71 [R] 00000000 00000000		
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$	NEWDT41 [R] 00000000 00000000		NEWDT31 [R] 00000000 00000000		
$00C198_H$	NEWDT61 [R] 00000000 00000000		NEWDT51 [R] 00000000 00000000		
$00C19C_H$	NEWDT81 [R] 00000000 00000000		NEWDT71 [R] 00000000 00000000		
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
$00C1A4_H$	INTPND41 [R] 00000000 00000000		INTPND31 [R] 00000000 00000000		
$00C1A8_H$	INTPND61 [R] 00000000 00000000		INTPND51 [R] 00000000 00000000		
$00C1AC_H$	INTPND81 [R] 00000000 00000000		INTPND71 [R] 00000000 00000000		
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$	MSGVAL41 [R] 00000000 00000000		MSGVAL31 [R] 00000000 00000000		
$00C1B8_H$	MSGVAL61 [R] 00000000 00000000		MSGVAL51 [R] 00000000 00000000		
$00C1BC_H$	MSGVAL81 [R] 00000000 00000000		MSGVAL71 [R] 00000000 00000000		
$00C1C0_H$ - $00C4FC_H$	reserved				reserved
$00C500_H$	CTRLR5 [R/W] 00000000 00000001		STATR5 [R/W] 00000000 00000000		CAN 5 Control Register
$00C504_H$	ERRCNT5 [R] 00000000 00000000		BTR5 [R/W] 00100011 00000001		
$00C508_H$	INTR5 [R] 00000000 00000000		TESTR5 [R/W] 00000000 X0000000		
$00C50C_H$	BRPE5 [R/W] 00000000 00000000		reserved		

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00C510_H$	IF1CREQ5 [R/W] 00000000 00000001		IF1CMSK5 [R/W] 00000000 00000000		CAN 5 IF 1 Register
$00C514_H$	IF1MSK25 [R/W] 11111111 11111111		IF1MSK15 [R/W] 11111111 11111111		
$00C518_H$	IF1ARB25 [R/W] 00000000 00000000		IF1ARB15 [R/W] 00000000 00000000		
$00C51C_H$	IF1MCTR5 [R/W] 00000000 00000000		reserved		
$00C520_H$	IF1DTA15 [R/W] 00000000 00000000		IF1DTA25 [R/W] 00000000 00000000		
$00C524_H$	IF1DTB15 [R/W] 00000000 00000000		IF1DTB25 [R/W] 00000000 00000000		
$00C528_H$ - $00C52C_H$	reserved				reserved
$00C530_H$	IF1DTA25 [R/W] 00000000 00000000		IF1DTA15 [R/W] 00000000 00000000		CAN 5 IF 1 Register mirror
$00C534_H$	IF1DTB25 [R/W] 00000000 00000000		IF1DTB15 [R/W] 00000000 00000000		
$00C538_H$ - $00C53C_H$	reserved				reserved
$00C540_H$	IF2CREQ5 [R/W] 00000000 00000001		IF2CMSK5 [R/W] 00000000 00000000		CAN 5 IF 2 Register
$00C544_H$	IF2MSK25 [R/W] 11111111 11111111		IF2MSK15 [R/W] 11111111 11111111		
$00C548_H$	IF2ARB25 [R/W] 00000000 00000000		IF2ARB15 [R/W] 00000000 00000000		
$00C54C_H$	IF2MCTR5 [R/W] 00000000 00000000		reserved		
$00C550_H$	IF2DTA15 [R/W] 00000000 00000000		IF2DTA25 [R/W] 00000000 00000000		
$00C554_H$	IF2DTB15 [R/W] 00000000 00000000		IF2DTB25 [R/W] 00000000 00000000		
$00C558_H$ - $00C55C_H$	reserved				reserved
$00C560_H$	IF2DTA25 [R/W] 00000000 00000000		IF2DTA15 [R/W] 00000000 00000000		CAN 5 IF 2 Register mirror
$00C564_H$	IF2DTB25 [R/W] 00000000 00000000		IF2DTB15 [R/W] 00000000 00000000		
$00C568_H$ - $00C57C_H$	reserved				reserved

	Register				
Address	+0	+1	+2	+3	Block
$00C580_H$	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags
$00C584_H$	TREQR45 [R] 00000000 00000000		TREQR35 [R] 00000000 00000000		
$00C588_H$	TREQR65 [R] 00000000 00000000		TREQR55 [R] 00000000 00000000		
$00C58C_H$	TREQR85 [R] 00000000 00000000		TREQR75 [R] 00000000 00000000		
$00C590_H$	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
$00C594_H$	NEWDT45 [R] 00000000 00000000		NEWDT35 [R] 00000000 00000000		
$00C598_H$	NEWDT65 [R] 00000000 00000000		NEWDT55 [R] 00000000 00000000		
$00C59C_H$	NEWDT85 [R] 00000000 00000000		NEWDT75 [R] 00000000 00000000		
$00C5A0_H$	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
$00C5A4_H$	INTPND45 [R] 00000000 00000000		INTPND35 [R] 00000000 00000000		
$00C5A8_H$	INTPND65 [R] 00000000 00000000		INTPND55 [R] 00000000 00000000		
$00C5AC_H$	INTPND85 [R] 00000000 00000000		INTPND75 [R] 00000000 00000000		
$00C5B0_H$	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
$00C5B4_H$	MSGVAL45 [R] 00000000 00000000		MSGVAL35 [R] 00000000 00000000		
$00C5B8_H$	MSGVAL65 [R] 00000000 00000000		MSGVAL55 [R] 00000000 00000000		
$00C5BC_H$	MSGVAL85 [R] 00000000 00000000		MSGVAL75 [R] 00000000 00000000		
$00C5C0_H$ - $00EFFC_H$	reserved				reserved

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU Control + IRQ
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ - $00F01C_H$	reserved				reserved
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				EDSU / MPU Control
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ - $00F07C_H$	reserved				reserved
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU ch. 0
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU ch. 1
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

	Register				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU ch. 2
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU ch. 3
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ - $00FFFC_H$	reserved				reserved
010000_H - $013FFC_H$	Cache TAG way 1 (010000_H - $0107FC_H$)				2 Way Set Associative I-Cache 4 KB
014000_H - $017FFC_H$	Cache TAG way 2 (014000_H - $0147FC_H$)				
018000_H - $01BFFC_H$	Cache RAM way 1 (018000_H - $0187FC_H$)				
$01C000_H$ - $01FFFC_H$	Cache RAM way 2 $01C000_H$ - $01C7FC_H$)				
020000_H - $02FFFC_H$	CY91F469QA D-RAM size is 64 KB (data access is 0 waitcycles)				Data-RAM
030000_H - $037FFC_H$	CY91F469QA I-/D-RAM size is 32 KB (instruction access is 0 waitcycles, data access is 1 waitcycle)				Instruction/ Data RAM
380000_H - $03FFFC_H$	reserved				reserved

1. depends on the number of available CAN channels
2. ACR0[11:10] depends on bus width setting in Mode vector fetch information
3. TCR[3:0] INIT value = 0000, keeps value after RST
4. Always write 1 to IOS[1] !
5. External Bus PFR registers are initial 0x00 in internal vector fetch mode (MD=000) and 0xff otherwise.

13.2 Flash memory and external bus area

32bit read/write	dat[31:0]				dat[31:0]				Block
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000_H to $05FFFF_H$	SA8 (64kB)				SA9 (64kB)				ROMS0
060000_H to $07FFFF_H$	SA10 (64kB)				SA11 (64kB)				ROMS1
080000_H to $09FFFF_H$	SA12 (64kB)				SA13 (64kB)				ROMS2
$0A0000_H$ to $0BFFFF_H$	SA14 (64kB)				SA15 (64kB)				ROMS3
$0C0000_H$ to $0DFFFF_H$	SA16 (64kB)				SA17 (64kB)				ROMS4
$0E0000_H$ to $0FFFF0_H$	SA18 (64kB)				SA19 (64kB)				ROMS5
$0FFFF8_H$	FMV [R] $06\ 00\ 00\ 00_H$				FRV [R] $00\ 00\ BF\ F8_H$				
100000_H to $11FFFF_H$	SA20 (64kB)				SA21 (64kB)				ROMS6
120000_H to $13FFFF_H$	SA22 (64kB)				SA23 (64kB)				
140000_H to $15FFFF_H$	SA24 (64kB)				SA25 (64kB)				ROMS7
160000_H to $17FFFF_H$	SA26 (64kB)				SA27 (64kB)				
180000_H to $19FFFF_H$	SA28 (64kB)				SA29 (64kB)				ROMS8
$1A0000_H$ to $1BFFFF_H$	SA30 (64kB)				SA31 (64kB)				
$1C0000_H$ to $1DFFFF_H$	SA32 (64kB)				SA33 (64kB)				ROMS9
$1E0000_H$ to $1FFFFF_H$	SA34 (64kB)				SA35 (64kB)				

32bit read/write	dat[31:0]				dat[31:0]				Block
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
200000_H to $21FFFF_H$	SA36 (64kB)				SA37 (64kB)				ROMS10
220000_H to $23FFFF_H$	SA38 (64kB)				SA39 (64kB)				
240000_H to $243FFF_H$	SA0 (8kB)				SA1 (8kB)				
244000_H to $247FFF_H$	SA2 (8kB)				SA3 (8kB)				
248000_H to $24BFFF_H$	SA4 (8kB)				SA5 (8kB)				
$24C000_H$ to $24FFFF_H$	SA6 (8kB)				SA7 (8kB)				
250000_H to $27FFFF_H$	reserved								
280000_H to $2FFFF8_H$	External Bus Area								ROMS11
300000_H to $37FFF8_H$									ROMS12
380000_H to $3FFFF8_H$									ROMS13
400000_H to $47FFF8_H$									ROMS14
480000_H to $4FFFF8_H$									ROMS15

Note: Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read.

14. Interrupt Vector Table

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		DMA Resource Number
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
Reset	0	00	—	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	—	$3EC_H$	$000FFFEC_H$	—
CPU supervisor mode (INT #5 instruction) *5	5	05	—	—	$3E8_H$	$000FFFE8_H$	—
Memory Protection exception *5	6	06	—	—	$3E4_H$	$000FFFE4_H$	—
System reserved	7	07	—	—	$3E0_H$	$000FFFE0_H$	—
System reserved	8	08	—	—	$3DC_H$	$000FFFDC_H$	—
System reserved	9	09	—	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	—	$3D0_H$	$000FFFD0_H$	—
System reserved	12	0C	—	—	$3CC_H$	$000FFFCC_H$	—
System reserved	13	0D	—	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	—
External Interrupt 0 External Interrupt 16	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16 **136**
External Interrupt 1 External Interrupt 17	17	11			$3B8_H$	$000FFFB8_H$	1, 17 **137**
External Interrupt 2 External Interrupt 18	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18 **138**
External Interrupt 3 External Interrupt 19	19	13			$3B0_H$	$000FFFB0_H$	3, 19 **139**
External Interrupt 4 External Interrupt 20	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20 **140**
External Interrupt 5 External Interrupt 21	21	15			$3A8_H$	$000FFFA8_H$	21 **141**
External Interrupt 6 External Interrupt 22	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22 **142**
External Interrupt 7 External Interrupt 23	23	17			$3A0_H$	$000FFFA0_H$	23 **143**
External Interrupt 8 External Interrupt 24	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	—
External Interrupt 9 External Interrupt 25	25	19			398_H	$000FFF98_H$	—

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		DMA Resource Number
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
External Interrupt 10 External Interrupt 26	26	1A	ICR05	445_H	394_H	$000FFF94_H$	—
External Interrupt 11 External Interrupt 27	27	1B			390_H	$000FFF90_H$	—
External Interrupt 12 External Interrupt 28	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	—
External Interrupt 13 External Interrupt 29	29	1D			388_H	$000FFF88_H$	—
External Interrupt 14 External Interrupt 30	30	1E	ICR07	447_H	384_H	$000FFF84_H$	—
External Interrupt 15 External Interrupt 31	31	1F			380_H	$000FFF80_H$	—
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35
Reload Timer 4	36	24	ICR10	$44A_H$	$36C_H$	$000FFF6C_H$	36
Reload Timer 5	37	25			368_H	$000FFF68_H$	37
Reload Timer 6	38	26	ICR11	$44B_H$	364_H	$000FFF64_H$	38
Reload Timer 7	39	27			360_H	$000FFF60_H$	39
Free Run Timer 0 Free Run Timer 8	40	28	ICR12	$44C_H$	$35C_H$	$000FFF5C_H$	40 176
Free Run Timer 1	41	29			358_H	$000FFF58_H$	41
Free Run Timer 2	42	2A	ICR13	$44D_H$	354_H	$000FFF54_H$	42
Free Run Timer 3	43	2B			350_H	$000FFF50_H$	43
Free Run Timer 4	44	2C	ICR14	$44E_H$	$34C_H$	$000FFF4C_H$	44
Free Run Timer 5	45	2D			348_H	$000FFF48_H$	45
Free Run Timer 6	46	2E	ICR15	$44F_H$	344_H	$000FFF44_H$	46
Free Run Timer 7	47	2F			340_H	$000FFF40_H$	47
CAN 0	48	30	ICR16	450_H	$33C_H$	$000FFF3C_H$	—
CAN 1	49	31			338_H	$000FFF38_H$	—
reserved	50	32	ICR17	451_H	334_H	$000FFF34_H$	—
reserved	51	33			330_H	$000FFF30_H$	—
reserved	52	34	ICR18	452_H	$32C_H$	$000FFF2C_H$	—
CAN 5	53	35			328_H	$000FFF28_H$	—
LIN-USART 0 RX	54	36	ICR19	453_H	324_H	$000FFF24_H$	6, 48
LIN-USART 0 TX	55	37			320_H	$000FFF20_H$	7, 49

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		DMA Resource Number
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
LIN-USART 1 RX	56	38	ICR20	454_H	$31C_H$	$000FFF1C_H$	8, 50
LIN-USART 1 TX	57	39			318_H	$000FFF18_H$	9, 51
LIN-USART 2 RX	58	3A	ICR21	455_H	314_H	$000FFF14_H$	52
LIN-USART 2 TX	59	3B			310_H	$000FFF10_H$	53
LIN-USART 3 RX	60	3C	ICR22	456_H	$30C_H$	$000FFF0C_H$	54
LIN-USART 3 TX	61	3D			308_H	$000FFF08_H$	55
System reserved	62	3E	ICR23 *3	457_H	304_H	$000FFF04_H$	—
Delayed Interrupt	63	3F			300_H	$000FFF00_H$	—
System reserved *4	64	40	(ICR24)	(458_H)	$2FC_H$	$000FFEFC_H$	—
System reserved *4	65	41			$2F8_H$	$000FFEF8_H$	—
LIN-USART (FIFO) 4 RX	66	42	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10, 56
LIN-USART (FIFO) 4 TX	67	43			$2F0_H$	$000FFEF0_H$	11, 57
LIN-USART (FIFO) 5 RX	68	44	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12, 58
LIN-USART (FIFO) 5 TX	69	45			$2E8_H$	$000FFEE8_H$	13, 59
LIN-USART (FIFO) 6 RX	70	46	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	60
LIN-USART (FIFO) 6 TX	71	47			$2E0_H$	$000FFEE0_H$	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	62
LIN-USART (FIFO) 7 TX	73	49			$2D8_H$	$000FFED8_H$	63
I2C 2	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	—
I2C 1 / I2C 3	75	4B			$2D0_H$	$000FFED0_H$	—
LIN-USART (FIFO) 8 RX	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
LIN-USART (FIFO) 8 TX	77	4D			$2C8_H$	$000FFEC8_H$	65
LIN-USART (FIFO) 9 RX	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	66
LIN-USART (FIFO) 9 TX	79	4F			$2C0_H$	$000FFEC0_H$	67
LIN-USART (FIFO) 10 RX	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	68
LIN-USART (FIFO) 10 TX	81	51			$2B8_H$	$000FFEB8_H$	69
LIN-USART (FIFO) 11 RX	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	70
LIN-USART (FIFO) 11 TX	83	53			$2B0_H$	$000FFEB0_H$	71
System reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	72
System reserved	85	55			$2A8_H$	$000FFEA8_H$	73
System reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	74
System reserved	87	57			$2A0_H$	$000FFEA0_H$	75
System reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	76
System reserved	89	59			298_H	$000FFE98_H$	77
System reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	78
System reserved	91	5B			290_H	$000FFE90_H$	79

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		DMA Resource Number
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
Input Capture 0 Input Capture 8	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	80 180
Input Capture 1 Input Capture 9	93	5D			288_H	$000FFE88_H$	81 181
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	5F			280_H	$000FFE80_H$	83
Input Capture 4	96	60	ICR40	468_H	$27C_H$	$000FFE7C_H$	84
Input Capture 5	97	61			278_H	$000FFE78_H$	85
Input Capture 6	98	62	ICR41	469_H	274_H	$000FFE74_H$	86
Input Capture 7	99	63			270_H	$000FFE70_H$	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	88
Output Compare 1	101	65			268_H	$000FFE68_H$	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	$000FFE64_H$	90
Output Compare 3	103	67			260_H	$000FFE60_H$	91
Output Compare 4	104	68	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	92
Output Compare 5	105	69			258_H	$000FFE58_H$	93
Output Compare 6	106	6A	ICR45	$46D_H$	254_H	$000FFE54_H$	94
Output Compare 7	107	6B			250_H	$000FFE50_H$	95
Sound Generator	108	6C	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	—
Phase Frequency Modulator	109	6D			248_H	$000FFE48_H$	—
System reserved	110	6E	ICR47 *3	$46F_H$	244_H	$000FFE44_H$	—
System reserved	111	6F			240_H	$000FFE40_H$	—
PPG0	112	70	ICR48	470_H	$23C_H$	$000FFE3C_H$	15, 96
PPG1	113	71			238_H	$000FFE38_H$	97
PPG2	114	72	ICR49	471_H	234_H	$000FFE34_H$	98
PPG3	115	73			230_H	$000FFE30_H$	99
PPG4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG5	117	75			228_H	$000FFE28_H$	101
PPG6	118	76	ICR51	473_H	224_H	$000FFE24_H$	102
PPG7	119	77			220_H	$000FFE20_H$	103
PPG8	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	104
PPG9	121	79			218_H	$000FFE18_H$	105
PPG10	122	7A	ICR53	475_H	214_H	$000FFE14_H$	106
PPG11	123	7B			210_H	$000FFE10_H$	107
PPG12	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108
PPG13	125	7D			208_H	$000FFE08_H$	109

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		DMA Resource Number
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
PPG14	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110
PPG15	127	7F			200_H	$000FFE00_H$	111
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	—
Up/Down Counter 1	129	81			$1F8_H$	$000FFDF8_H$	—
Up/Down Counter 2	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	—
Up/Down Counter 3	131	83			$1F0_H$	$000FFDF0_H$	—
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	—
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	—
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
A/D Converter 1	135	87			$1E0_H$	$000FFDE0_H$	113
Alarm Comparator 0	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	—
Alarm Comparator 1	137	89			$1D8_H$	$000FFDD8_H$	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	—
System reserved	139	8B			$1D0_H$	$000FFDD0_H$	—
Timebase Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	—
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	—
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	—
Security vector	144	90	—	—	$1BC_H$	$000FFDBC_H$	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	—

*1 : The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.

*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])

*4 : Used by REALOS

*5 : Memory Protection Unit (MPU) support

15. Recommended Settings

15.1 PLL and Clockgear Settings

Please note that for CY91F469QA core base clock frequencies above 88MHz can only be achieved with 1.9V core supply voltage *1.

Please see "Absolute Maximum Ratings" on page 96 to find the maximum allowed frequency of Core Base Clock (fCLKB) at high temperature.

Recommended PLL Divider and Clockgear Settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	1.8V	1.9V
	DIVM	DIVN	DIVG	MULG	MULG			
4	2	25	16	24	200	100	no	yes
4	2	24	16	24	192	96	no	yes
4	2	23	16	24	184	92	no	yes
4	2	22	16	24	176	88	yes	yes
4	2	21	16	20	168	84	yes	yes
4	2	20	16	20	160	80	yes	yes
4	2	19	16	20	152	76	yes	yes
4	2	18	16	20	144	72	yes	yes
4	2	17	16	16	136	68	yes	yes
4	2	16	16	16	128	64	yes	yes
4	2	15	16	16	120	60	yes	yes
4	2	14	16	16	112	56	yes	yes
4	2	13	16	12	104	52	yes	yes
4	2	12	16	12	96	48	yes	yes
4	2	11	16	12	88	44	yes	yes
4	4	10	16	24	160	40	yes	yes
4	4	9	16	24	144	36	yes	yes
4	4	8	16	24	128	32	yes	yes
4	4	7	16	24	112	28	yes	yes
4	6	6	16	24	144	24	yes	yes
4	8	5	16	28	160	20	yes	yes
4	10	4	16	32	160	16	yes	yes
4	12	3	16	32	144	12	yes	yes

*1: In order to enter this mode please set REGSEL_FLASHSEL=1 and REGSEL_MAINSEL=1 (HWM Chapter 52.3.1)

15.2 Clock Modulator Settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

If Fmax exceeds 88MHz the core supply voltage needs to be set to 1.9V. Please refer to flash access time settings (section 2.3.2.2) to setup the correct voltage according to Fmax in the table below.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Please see "Absolute Maximum Ratings" on page 96 to find the maximum allowed frequency of Fmax (fCLKB) at high temperature.

Clock Modulator Settings, Frequency Range and Supported Supply Voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	88	79.5	98.5	
1	3	026F	84	76.1	93.8	
1	3	026F	80	72.6	89.1	
1	5	02AE	80	68.7	95.8	
2	3	046E	80	68.7	95.8	
1	3	026F	76	69.1	84.5	
1	5	02AE	76	65.3	90.8	
1	7	02ED	76	62	98.1	
2	3	046E	76	65.3	90.8	
3	3	066D	76	62	98.1	
1	3	026F	72	65.5	79.9	
1	5	02AE	72	62	85.8	
1	7	02ED	72	58.8	92.7	
2	3	046E	72	62	85.8	
3	3	066D	72	58.8	92.7	
1	3	026F	68	62	75.3	
1	5	02AE	68	58.7	80.9	
1	7	02ED	68	55.7	87.3	
1	9	032C	68	53	95	
2	3	046E	68	58.7	80.9	
2	5	04AC	68	53	95	
3	3	066D	68	55.7	87.3	
4	3	086C	68	53	95	
1	3	026F	64	58.5	70.7	
1	5	02AE	64	55.3	75.9	
1	7	02ED	64	52.5	82	
1	9	032C	64	49.9	89.1	
1	11	036B	64	47.6	97.6	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	3	046E	64	55.3	75.9	
2	5	04AC	64	49.9	89.1	
3	3	066D	64	52.5	82	
4	3	086C	64	49.9	89.1	
5	3	0A6B	64	47.6	97.6	
1	3	026F	60	54.9	66.1	
1	5	02AE	60	51.9	71	
1	7	02ED	60	49.3	76.7	
1	9	032C	60	46.9	83.3	
1	11	036B	60	44.7	91.3	
2	3	046E	60	51.9	71	
2	5	04AC	60	46.9	83.3	
3	3	066D	60	49.3	76.7	
4	3	086C	60	46.9	83.3	
5	3	0A6B	60	44.7	91.3	
1	3	026F	56	51.4	61.6	
1	5	02AE	56	48.6	66.1	
1	7	02ED	56	46.1	71.4	
1	9	032C	56	43.8	77.6	
1	11	036B	56	41.8	84.9	
1	13	03AA	56	39.9	93.8	
2	3	046E	56	48.6	66.1	
2	5	04AC	56	43.8	77.6	
2	7	04EA	56	39.9	93.8	
3	3	066D	56	46.1	71.4	
3	5	06AA	56	39.9	93.8	
4	3	086C	56	43.8	77.6	
5	3	0A6B	56	41.8	84.9	
6	3	0C6A	56	39.9	93.8	
1	3	026F	52	47.8	57	
1	5	02AE	52	45.2	61.2	
1	7	02ED	52	42.9	66.1	
1	9	032C	52	40.8	71.8	
1	11	036B	52	38.8	78.6	
1	13	03AA	52	37.1	86.8	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	03E9	52	35.5	96.9	
2	3	046E	52	45.2	61.2	
2	5	04AC	52	40.8	71.8	
2	7	04EA	52	37.1	86.8	
3	3	066D	52	42.9	66.1	
3	5	06AA	52	37.1	86.8	
4	3	086C	52	40.8	71.8	
5	3	0A6B	52	38.8	78.6	
6	3	0C6A	52	37.1	86.8	
7	3	0E69	52	35.5	96.9	
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	

(Continued)

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Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	
8	3	1068	44	28.9	92.1	
1	3	026F	40	37	43.6	
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	
9	3	1267	40	25.3	95.8	
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	11	036B	36	27.1	53.8	
1	13	03AA	36	25.8	59.3	
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	

(Continued)

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Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
5	5	0AA6	32	19.5	89.1	
6	3	0C6A	32	23	52.5	
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	

16. Electrical Characteristics

16.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1*1	$V_{DD}5R$	− 0.3	+ 6.0	V	
Power supply voltage 2*1	$V_{DD}5$	− 0.3	+ 6.0	V	
Power supply voltage 4*1	$V_{DD}35$	− 0.3	+ 6.0	V	
Relationship of the supply voltages	$AV_{CC}5$	$V_{DD}5$-0.3	$V_{DD}5$+0.3	V	At least one pin of the Ports 25 to 29 (ANn) is used as digital input or output
		$V_{SS}5$-0.3	$V_{DD}5$+0.3	V	All pins of the Ports 25 to 29 (ANn) follow the condition of V_{IA}
Analog power supply voltage*1	$AV_{CC}5$	− 0.3	+ 6.0	V	*2
Analog reference power supply voltage*1	AVRH	− 0.3	+ 6.0	V	*2
Input voltage 1*1	V_{I1}	Vss5 − 0.3	$V_{DD}5$ + 0.3	V	
Input voltage 2*1	V_{I2}	Vss5 − 0.3	$V_{DD}35$ + 0.3	V	External bus
Analog pin input voltage*1	V_{IA}	AVss5 − 0.3	AVcc5 + 0.3	V	
Output voltage 1*1	V_{O1}	Vss5 − 0.3	$V_{DD}5$ + 0.3	V	
Output voltage 2*1	V_{O2}	Vss5 − 0.3	$V_{DD}35$ + 0.3	V	External bus
Maximum clamp current	I_{CLAMP}	− 4.0	+ 4.0	mA	*3
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*3
“L” level maximum output current*4	I_{OL}	—	10	mA	
“L” level average output current*5	I_{OLAV}	—	8	mA	
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*6	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*4	I_{OH}	—	− 10	mA	
“H” level average output current*5	I_{OHAV}	—	− 4	mA	
“H” level total maximum output current	ΣI_{OH}	—	− 100	mA	
“H” level total average output current*6	ΣI_{OHAV}	—	− 25	mA	

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted operating frequency CY91F469QA, CY91F469QAH	$f_{max, CLKB}$	—	100	MHz	$T_A \leq 105°C$, main regulator set to 1.9V
	$f_{max, CLKP}$	—	50		
	$f_{max, CLKT}$	—	50		
	$f_{max, CLKCAN}$	—	50		
Permitted operating frequency CY91F469QAH	$f_{max, CLKB}$	—	96	MHz	$T_A \leq 125°C$, main regulator set to 1.9V
	$f_{max, CLKP}$	—	48		
	$f_{max, CLKT}$	—	48		
	$f_{max, CLKCAN}$	—	48		
Permitted operating frequency CY91F469QA, CY91F469QAH	$f_{max, CLKB}$	—	88	MHz	$T_A \leq 105°C$, main regulator set to 1.8V
	$f_{max, CLKP}$	—	44		
	$f_{max, CLKT}$	—	44		
	$f_{max, CLKCAN}$	—	44		
Permitted operating frequency CY91F469QAH	$f_{max, CLKB}$	—	84	MHz	$T_A \leq 125°C$, main regulator set to 1.8V
	$f_{max, CLKP}$	—	42		
	$f_{max, CLKT}$	—	42		
	$f_{max, CLKCAN}$	—	42		
Permitted power consumption *7	P_D	—	2000 *8	mW	$T_A \leq 85°C$
		—	1300 *8		$T_A \leq 105°C$
		—	800 *8		$T_A \leq 115°C$
		—	2000 *8		$T_A \leq 105°C$, no Flash program/erase *9 *10
		—	1800 *8		$T_A \leq 115°C$, no Flash program/erase *9 *10
		—	1300 *8		$T_A \leq 125°C$, no Flash program/erase *9 *10
Operating temperature	T_A	− 40	$T_{A(max)}$	°C	For $T_{A(max)}$, refer to the ordering information
Storage temperature	Tstg	− 55	+ 150	°C	

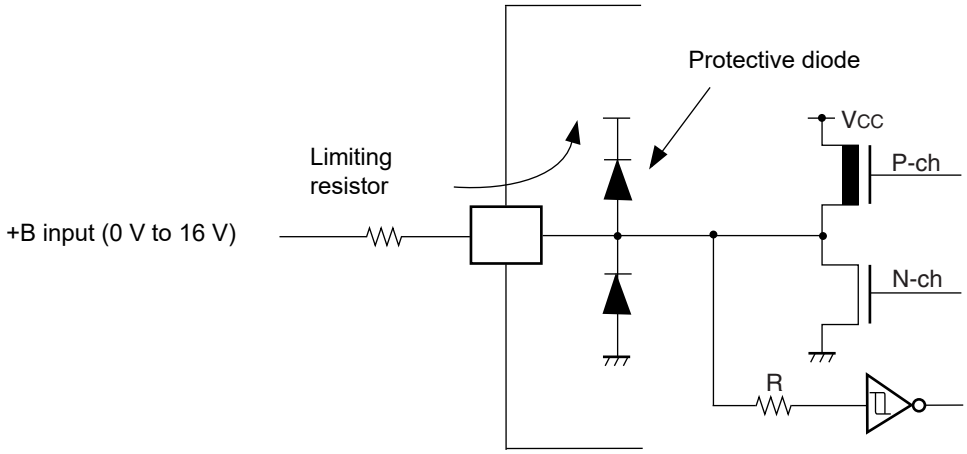
*1 : The parameter is based on $V_{SS}5 = AV_{SS}5 = 0.0$ V.

*2 : $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.

*3 :
- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time , either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.

- Do not leave +B input pins open.
- Example of recommended circuit :

Input/output Equivalent Circuit



*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

*7 : The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (|V_{SS}-V_{OL}| * I_{OL} + |V_{DD}-V_{OH}| * I_{OH})$(IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * I_A + AVRH5 * I_R$ (internal power dissipation)

*8 : Worst case value for the BGA package mounted on a 4-layer PCB at specified T_A without air flow.

*9 : Please contact Fujitsu's representative for reliability limitations when using under these conditions.

*10:Applicable only for devices with $T_{A(max)} \geq T_A$.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

16.2 Recommended Operating Conditions

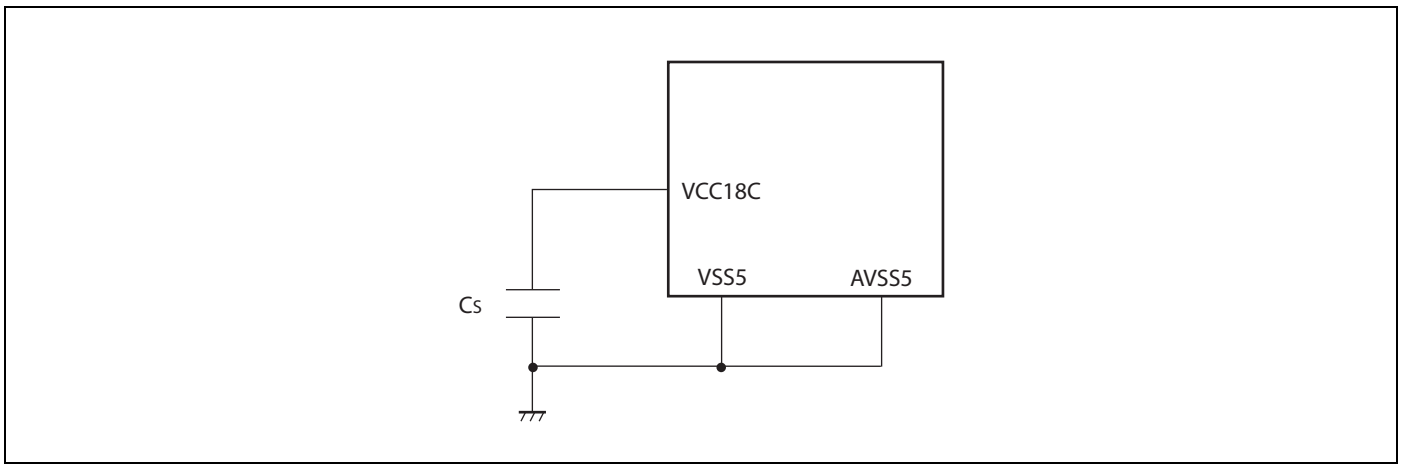
($V_{SS}5 = AV_{SS}5 = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	—	5.5	V	
	$V_{DD}5R$	3.0	—	5.5	V	Internal regulator
	$V_{DD}35$	3.0	—	5.5	V	External bus
	$AV_{CC}5$	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	—	4.7	—	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Operating temperature	T_A	− 40	—	$T_{A(max)}$	°C	For $T_{A(max)}$, see the ordering information
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{discharge}$ = 1.5kΩ $C_{discharge}$ = 100pF
RC Oscillator	$f_{RC100kHz}$	50	100	200	kHz	$VDD_{CORE} \geq 1.65V$
	f_{RC2MHz}	1	2	4	MHz	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



16.3 DC Characteristics

Note: In the following tables, "V_{DD}" means $V_{DD}35$ for pins of ext. bus or $V_{DD}5$ for other pins.
In the following tables, "V_{SS}" means $V_{SS}5$ for all pins.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40°C$ to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V_{DD}	—	V_{DD} + 0.3	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V_{DD}	—	V_{DD} + 0.3	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				0.74 × V_{DD}	—	V_{DD} + 0.3	V	3 V ≤ V_{DD} < 4.5 V
		—	AUTOMOTIVE Hysteresis input is selected	0.8 × V_{DD}	—	V_{DD} + 0.3	V	
		—	Port inputs if TTL input is selected	2.0	—	V_{DD} + 0.3	V	
	V_{IHR}	INITX	—	0.8 × V_{DD}	—	V_{DD} + 0.3	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_2 to MD_0	—	V_{DD} − 0.3	—	V_{DD} + 0.3	V	Mode input pins
	V_{IHX0S}	X0, X0A	—	2.5	—	V_{DD} + 0.3	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	—	0.8 × V_{DD}	—	V_{DD} + 0.3	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V_{SS} − 0.3	—	0.2 × V_{DD}	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V_{SS} − 0.3	—	0.3 × V_{DD}	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	V_{SS} − 0.3	—	0.5 × V_{DD}	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				V_{SS} − 0.3	—	0.46 × V_{DD}	V	3 V ≤ V_{DD} < 4.5 V
		—	Port inputs if TTL input is selected	V_{SS} − 0.3	—	0.8	V	
	V_{ILR}	INITX	—	V_{SS} − 0.3	—	0.2 × V_{DD}	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_2 to MD_0	—	V_{SS} − 0.3	—	V_{SS} + 0.3	V	Mode input pins
	V_{ILXDS}	X0, X0A	—	V_{SS} − 0.3	—	0.5	V	External clock in "Oscillation mode"

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40°C$ to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	—	V_{SS} − 0.3	—	0.2 × V_{DD}	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = − 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = − 1.6mA	V_{DD} − 0.5	—	—	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = − 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = − 3mA	V_{DD} − 0.5	—	—	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = − 3mA	V_{DD} − 0.5	—	—	V	
Output “L“ voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 1.6mA	—	—	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 3mA	—	—	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 3mA	—	—	0.4	V	
Input leakage current	I_{IL}	Pnn_m*[1]	3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=25°C	− 1	—	+ 1	µA	$V_{SS}5 < V_I < V_{DD}$
			3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ $T_A=T_{A(max)}$	− 3	—	+ 3		

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.

($V_{DD}5$ = $AV_{CC}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Analog input leakage current	I_{AIN}	ANn *1	3.0V ≤ V_{DD} ≤ 5.5V T_A=25°C	− 1	—	+ 1	µA	$AV_{SS}5 < V_I < AV_{CC}5$, $AV_{SS}5 < V_I$ < AVRH5
			3.0V ≤ V_{DD} ≤ 5.5V T_A=$T_{A(max)}$	− 3	—	+ 3	µA	
Pull-up resistance	R_{UP}	Pnn_m *2 INITX	3.0V ≤V_{DD} ≤3.6V	40	100	160	kΩ	
			4.5V ≤V_{DD} ≤5.5V	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m *3	3.0V ≤V_{DD} ≤3.6V	40	100	180	kΩ	
			4.5V ≤V_{DD} ≤5.5V	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, AV_{SS}, AVRH5	f = 1 MHz	-	5	15	pF	
Power supply current CY91F469QA CY91F469QAH	I_{CC}	$V_{DD}5R$	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	—	140	170	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25°C	—	50	210	µA	At stop mode *4
			T_A = + 105°C	—	0.6	2.8	mA	
			T_A = + 125°C	—	1.4	5.8	mA	
			T_A = + 25°C	—	120	560	µA	RTC : 4 MHz mode *4
			T_A = + 105°C	—	0.7	3.2	mA	
			T_A = + 125°C	—	1.5	7.2	mA	
			T_A = + 25°C	—	70	310	µA	RTC : 100 kHz mode *4 32 kHz mode *5
			T_A = + 105°C	—	0.65	3.0	mA	
			T_A = + 125°C	—	1.45	6.0	mA	
	I_{LVE}	$V_{DD}5$	—	—	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	—	—	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	—	—	250	500	µA	Main clock (4 MHz)
			—	—	20	40	µA	Sub clock (32 kHz)

1. ANn includes all pins where AN channels are enabled.
2. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
3. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
4. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.
5. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled, RC oscillator disabled. Additional current consumption of Sub oscillator I_{OSC} has to be taken into account.

16.4 A/D Converter Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40°C$ to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	− 3	—	+ 3	LSB	
Nonlinearity error	—	—	− 2.5	—	+ 2.5	LSB	
Differential nonlinearity error	—	—	− 1.9	—	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL−1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH−3.5 LSB	AVRH−1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	—	0.6	—	t.b.d.*1	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	—	t.b.d. *1	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	—	0.4	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	—	1.0	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	—	—	11	pF	
Input resistance	R_{IN}	ANn	—	—	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			—	—	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	− 1	—	+ 1	µA	T_A = + 25°C
			− 3	—	+ 3	µA	$T_A = T_{A(max)}$
Analog input voltage range	V_{AIN}	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	

1. Paramater is under re-evaluation.

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

(Continued)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	—	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	—	$AV_{CC}5 \times 0.25$	V	
Power supply current	I_A	$AV_{CC}5$	—	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	—	—	5	µA	A/D Converter not operated *1
Reference voltage current	I_R	AVRH5	—	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	—	—	5	µA	A/D Converter not operated *2

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

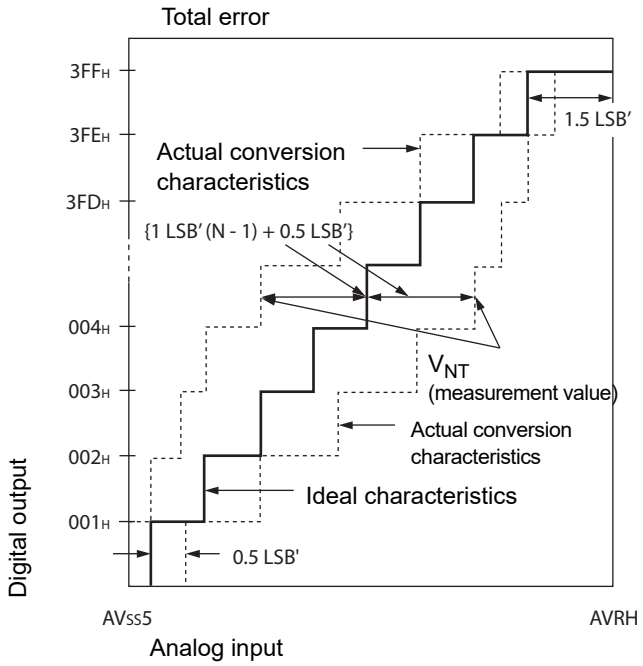
*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

Sampling Time Calculation
$T_{samp} = (2.6\ kOhm + R_{EXT}) \times 11pF \times 7$; for $4.5V \leq AV_{CC}5 \leq 5.5V$
$T_{samp} = (12.1\ kOhm + R_{EXT}) \times 11pF \times 7$; for $3.0V \leq AV_{CC}5 \leq 4.5V$

Conversion Time Calculation
$T_{conv} = T_{samp} + T_{comp}$

Definition of A/D Converter Terms

- Resolution
  Analog variation that is recognizable by the A/D converter.
- Nonlinearity error
  Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).
- Differential nonlinearity error
  Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error
  This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.

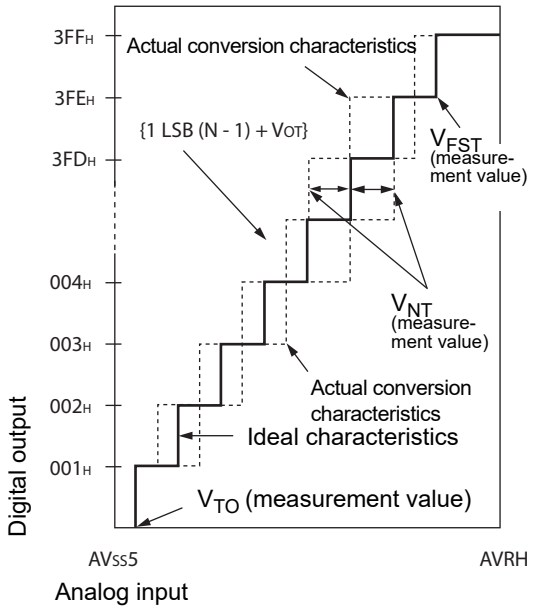


$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}5}{1024} \text{ [V]}$$

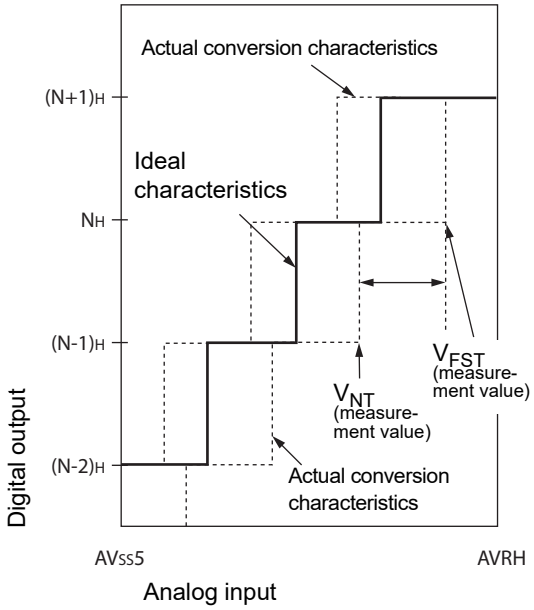
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5\ LSB'$ [V]
V_{FST}' (ideal value) = $AVRH - 1.5\ LSB'$ [V]
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

16.5 Alarm Comparator Characteristics

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$	—	25	40	µA	Alarm comparator enabled in fast mode (per channel) *1
	I_{A5ALMS}		—	7	10	µA	Alarm comparator enabled in normal mode (per channel) *1
	I_{A5ALMH}		—	—	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM_n	− 1	—	+ 1	µA	T_A=25°C
			− 3	—	+ 3	µA	$T_A=T_{A(max)}$
ALARM pin input voltage range	V_{ALIN}		0	—	$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78$ − 3%	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78$ + 3%	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36$ − 5%	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36$ + 5%	V	
Alarm hysteresis voltage	V_{IAHYS}		50	—	250	mV	
Alarm input resistance	R_{IN}		5	—	—	MΩ	
Comparison time	t_{COMPF}		—	0.1	0.2	µs	Alarm comparator enabled in fast mode *1
	t_{COMPS}		—	1	2	µs	Alarm comparator enabled in normal mode *1

Note: *1 : The fast Alarm Comparator mode is enabled by setting ACSR.MD=1
Setting ACSR.MD=0 sets the normal mode.

16.6 FLASH Memory Program/erase Characteristics

16.6.1 CY91F469QA

(T_A = 25°C, Vcc = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	n*0.5	n*2.0	s	n is the number of Flash sector of the device
Word (16 or 32-bit width) programming time	-	6	100	µs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

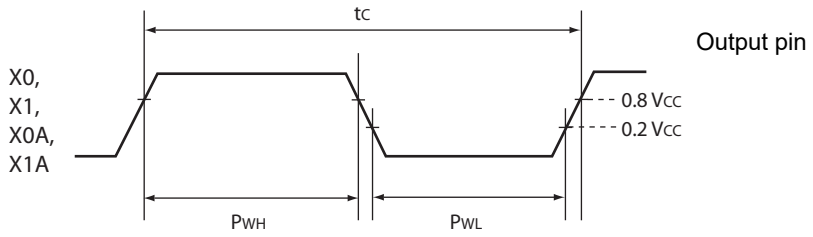
16.7 AC Characteristics

16.7.1 Clock Timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

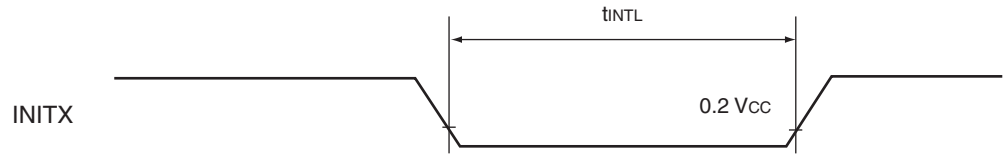
Clock timing conditions



16.7.2 Reset input Ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	10	—	ms
INITX input time (other than the above)				20	—	µs



16.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
- All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - T_a = -40°C to $T_{A(max)}$
  - C_l = 50 pF (load capacity value of pins when testing)
  - VOL = 0.2 x $V_{DD}5$
  - VOH = 0.8 x $V_{DD}5$
  - EPILR = 0, PILR = 1 (Automotive Level == worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40°C to $T_{A(max)}$)

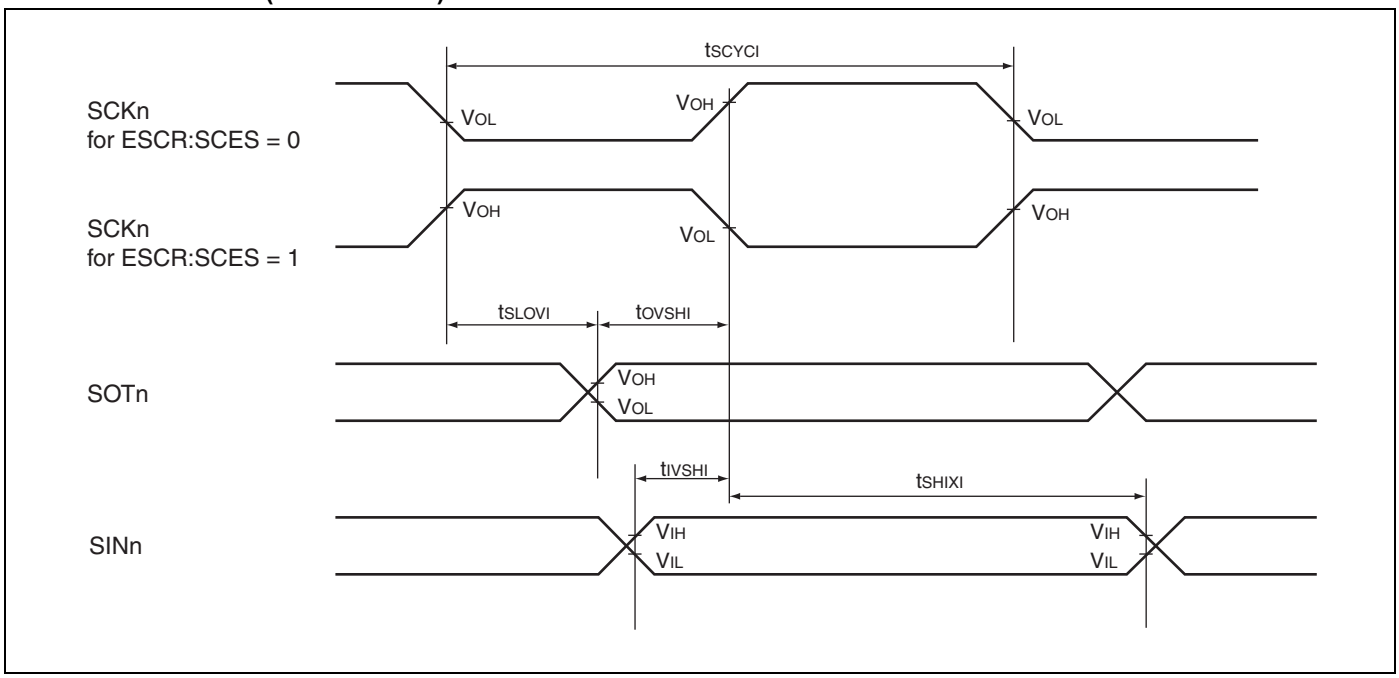
Parameter	Symbol	Pin Name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	—	4 t_{CLKP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		− 30	30	− 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} − 30*	—	m × t_{CLKP} − 20*	—	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	—	t_{CLKP} + 45	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	—	0	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		—	2 t_{CLKP} + 55	—	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	—	10	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK rising time	t_{FE}	SCKn		—	20	—	20	ns
SCK falling time	t_{RE}	SCKn		—	20	—	20	ns

* : Parameter m depends on t_{SCYCI} and can be calculated as :

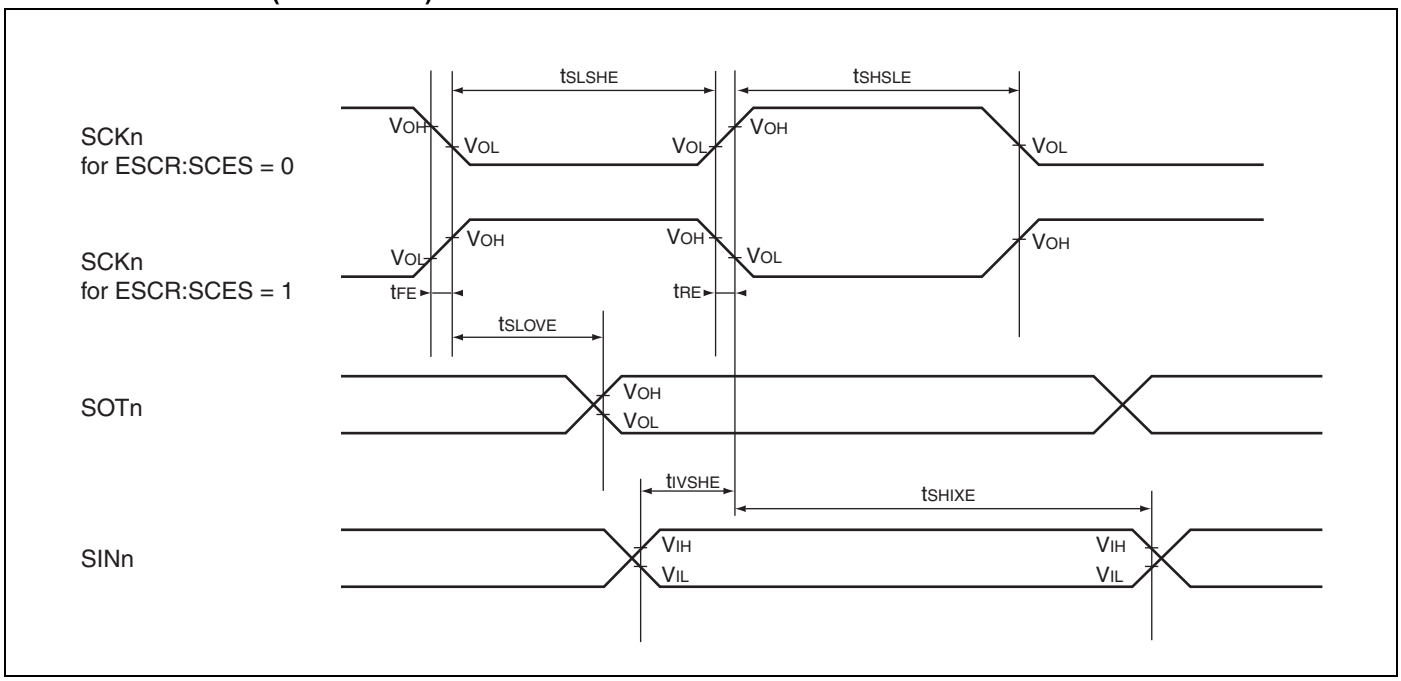
- if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2
- if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

Notes :
- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

Internal Clock Mode (Master Mode)



External clock mode (slave mode)



16.7.4 I^2C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = − 40°C to $T_{A(max)}$
  - C_l = 50 pF
  - VOL = 0.3 × $V_{DD}5$
  - VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

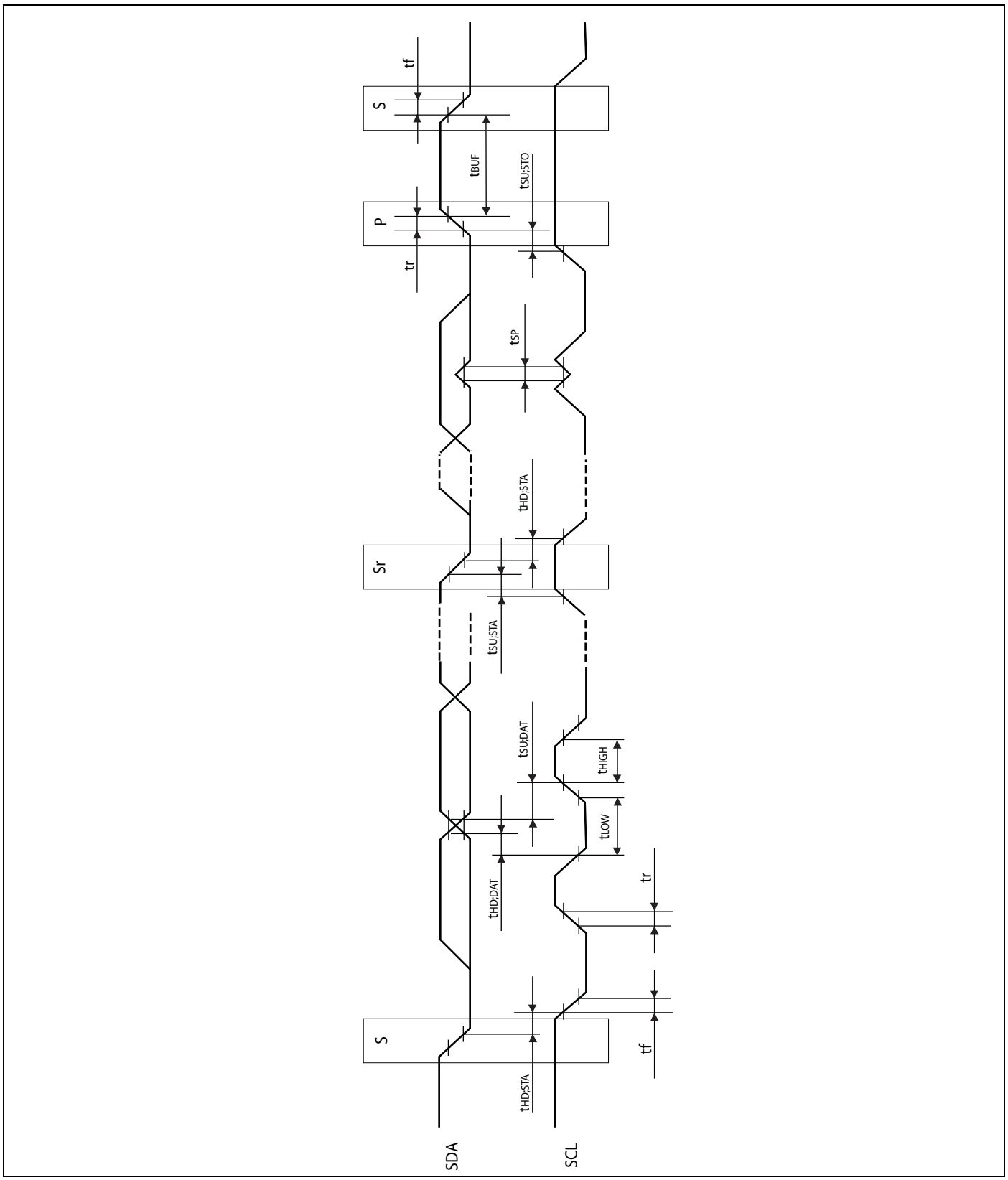
Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	—	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	—	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	—	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	—	µs	
Data hold time for I^2C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	—	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	—	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

*1 : The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I2C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

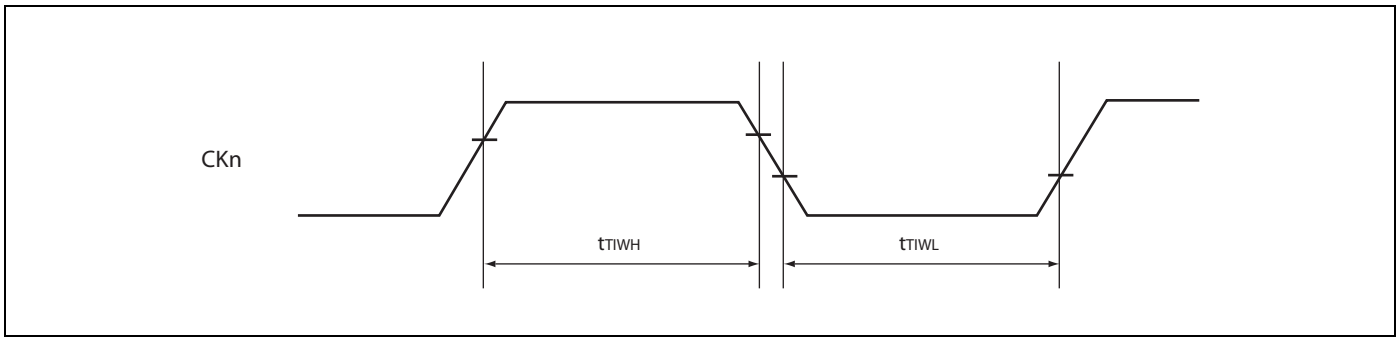

tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
S
tf
tHD;STA
SDA
SCL

16.7.5 Free-run Timer Clock

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	—	$4t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.

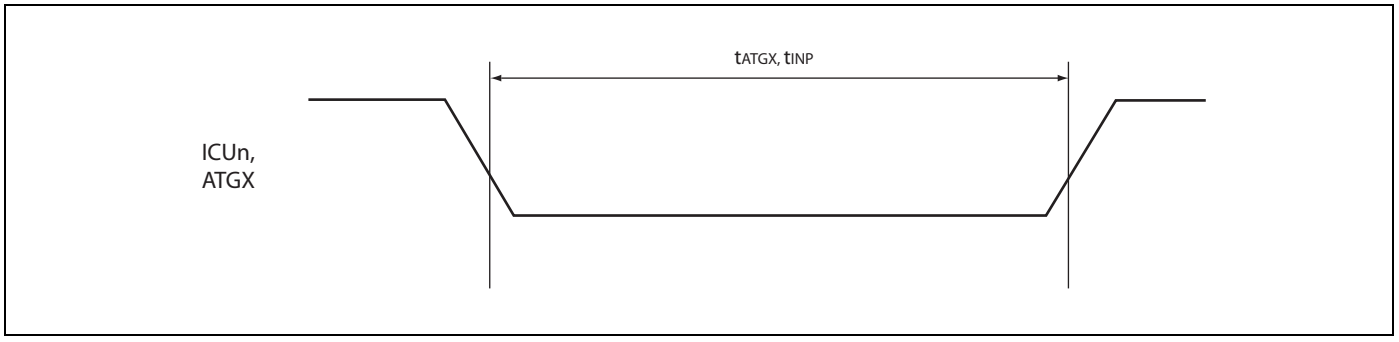


16.7.6 Trigger Input Timing

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.



16.7.7 External Bus AC Timings at $V_{DD}35$ = 4.5 to 5.5 V

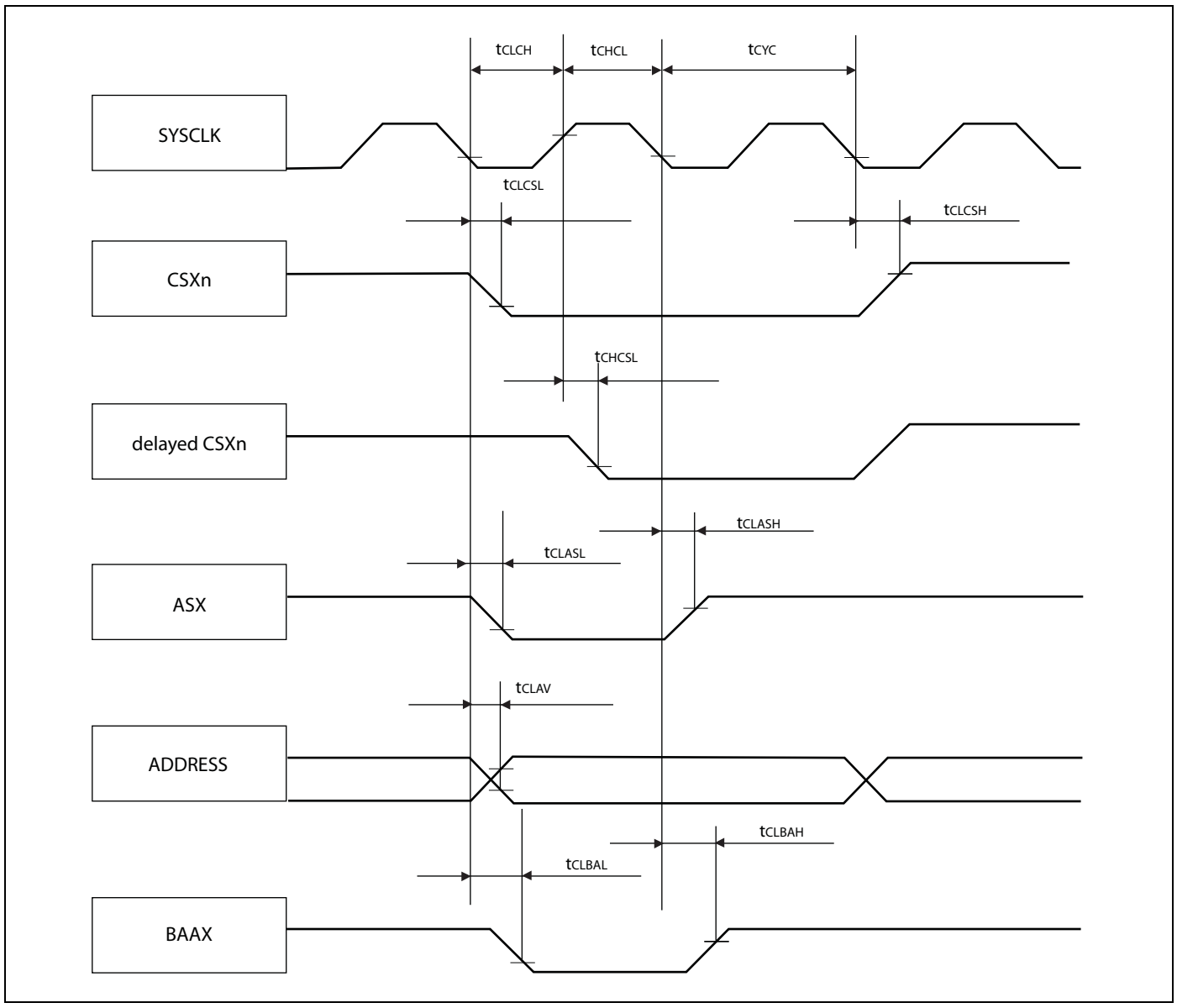
- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 5 mA
  - $V_{SS}5$ = 0 V
  - Ta = − 40°C to $T_{A(max)}$
  - C_l = 50 pF
  - VOL = 0.2 × $V_{DD}35$
  - VOH = 0.8 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = = worst case)

Basic Timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 × t_{CLKT} − 4	1/2 × t_{CLKT} + 5	ns
	t_{CHCL}		1/2 × t_{CLKT} − 5	1/2 × t_{CLKT} + 4	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	9	ns
	t_{CLCSH}		—	8	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		− 2	8	ns
SYSCLK ↓ to ASX delay time	t_{CLASL}	SYSCLK ASX	—	8	ns
	t_{CLASH}		—	7	ns
SYSCLK ↓ to BAAX delay time	t_{CLBAL}	SYSCLK BAAX	—	5	ns
	t_{CLBAH}		- 2	—	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A27 to A0	—	10	ns

Note : t_{CLKT} is the cycle time of the external bus clock.

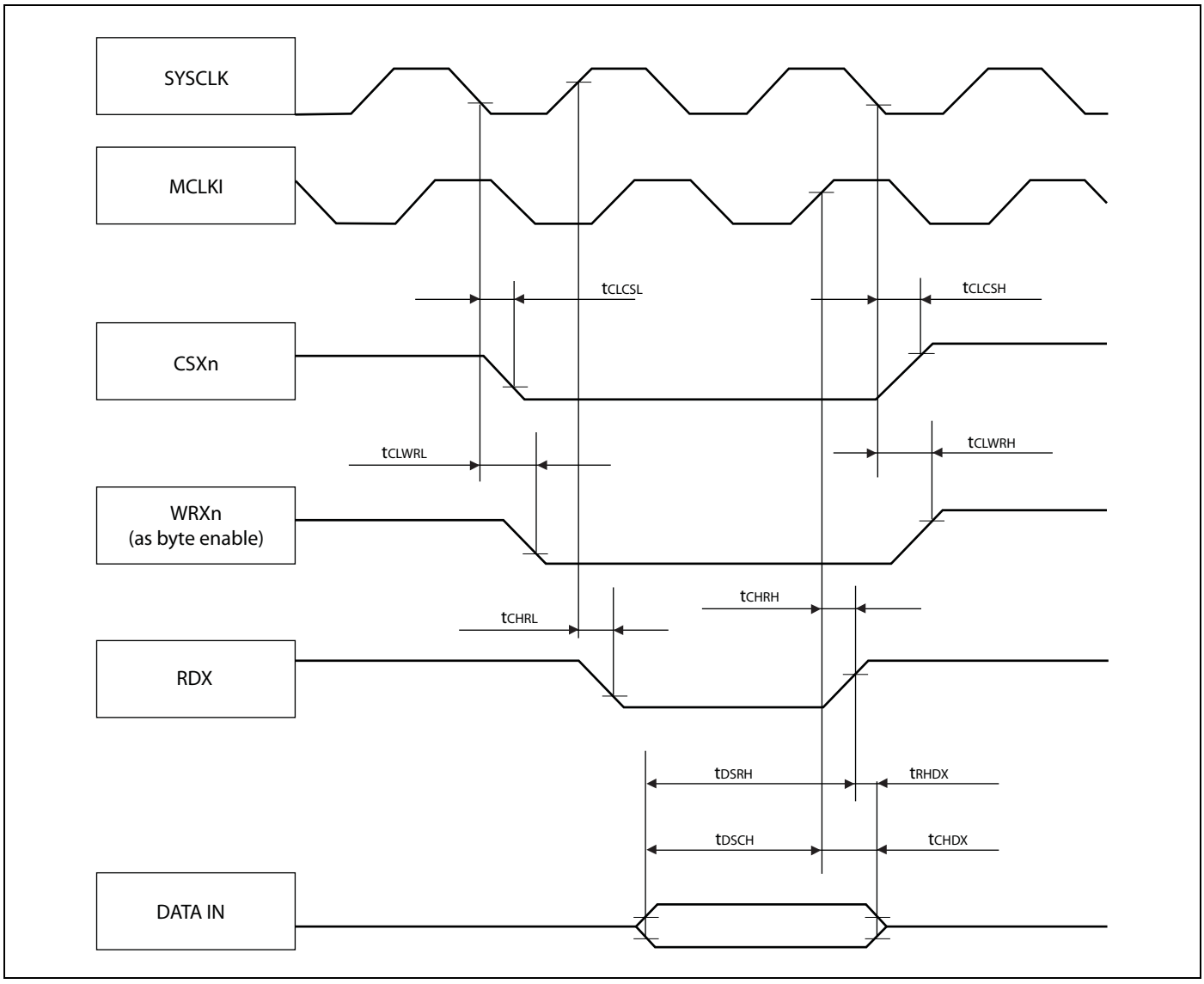

tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Synchronous/Asynchronous Read Access with External MCLKI Input

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↑ /MCLKI ↑ to RDX delay time	t_{CHRL}	SYSCLK RDX	− 2	7	ns
	t_{CHRH}	MCLKI RDX	10	20	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	20	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	t_{RHDX}	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	t_{DSCH}	MCLKI D31 to D0	1	—	ns
MCLKI ↑ to Data valid hold time	t_{CHDX}	MCLKI D31 to D0	3	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	SYSCLK WRXn	—	9	ns
	t_{CLWRH}		− 1	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	9	ns
	t_{CLCSH}		—	8	ns

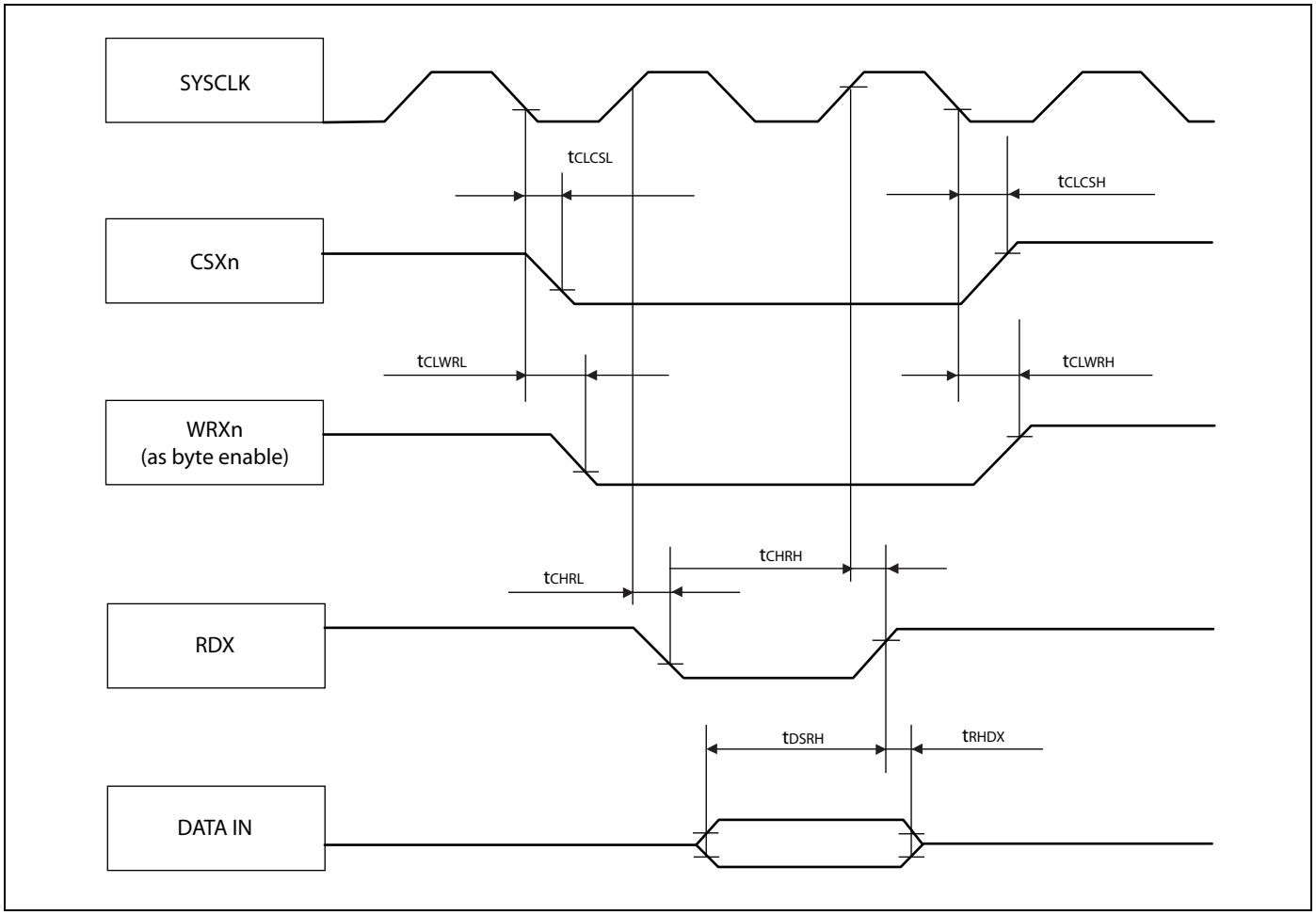
Note: The usage of the external feedback from MCLKO to MCLKI is not recommended.


SYSCLK
MCLKI
tCLCSL
tCLCSH
CSXn
tCLWRL
tCLWRH
WRXn
(as byte enable)
tCHRH
tCHRL
RDX
tDSRH
tRHDX
tDSCH
tCHDX
DATA IN

Synchronous/Asynchronous Read Access with Internal MCLKO --> MCLKI Feedback

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

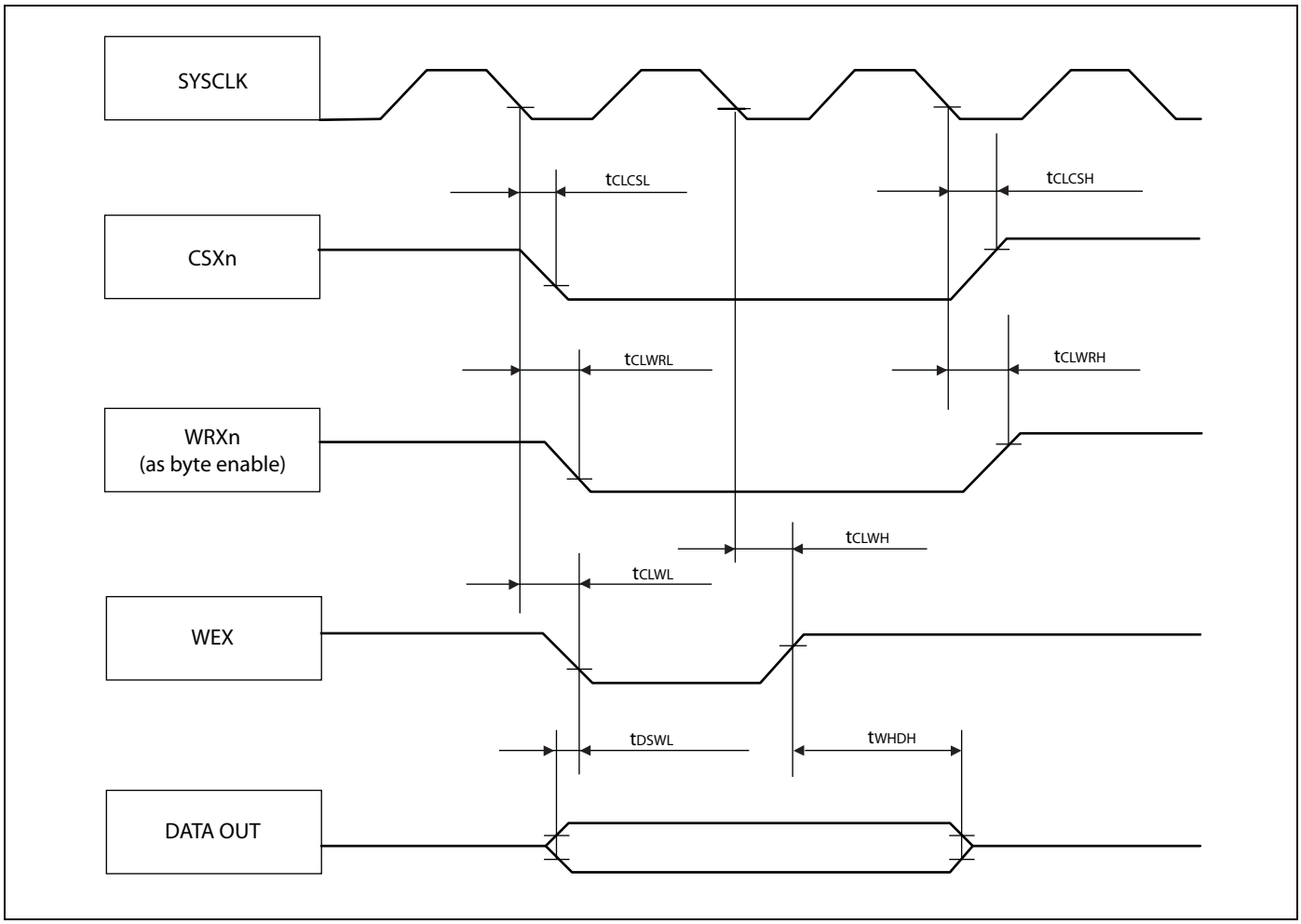
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	t_{CHRL}	SYSCLK RDX	− 2	7	ns
	t_{CHRH}		− 2	4	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	19	—	ns
RDX ↑ to Data valid hold time (internal MCLKO → MCLKI /MCLKI feedback)	t_{RHDX}	RDX D31 to D0	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	SYSCLK WRXn	—	9	ns
	t_{CLWRH}		− 1	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	9	ns
	t_{CLCSH}		—	8	ns



Synchronous Write Access - Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

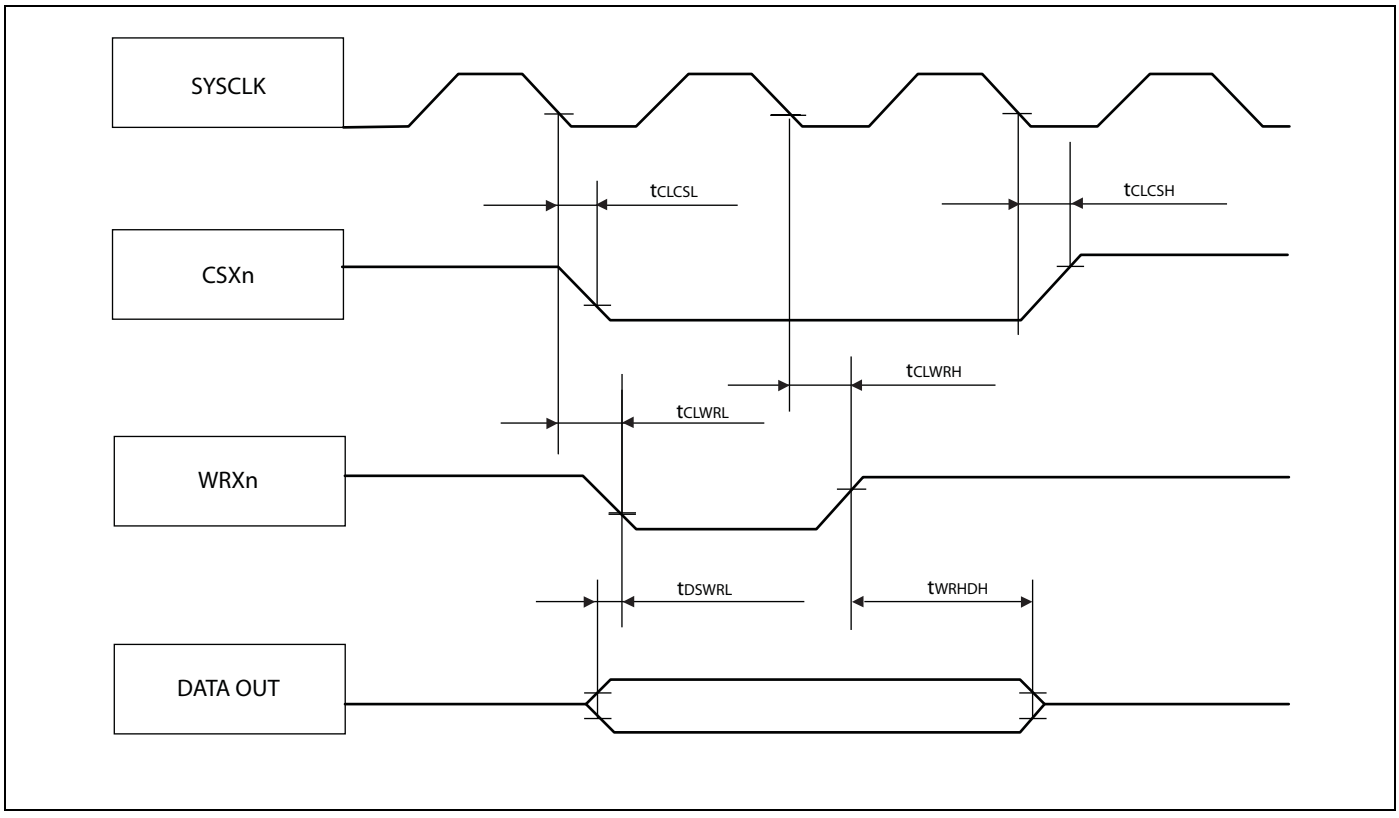
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to WEX delay time	t_{CLWL}	SYSCLK WEX	—	8	ns
	t_{CLWH}		- 2	—	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	− 5	—	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	t_{CLKT} − 10	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	SYSCLK WRXn	—	9	ns
	t_{CLWRH}		− 1	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	9	ns
	t_{CLCSH}		—	8	ns



Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

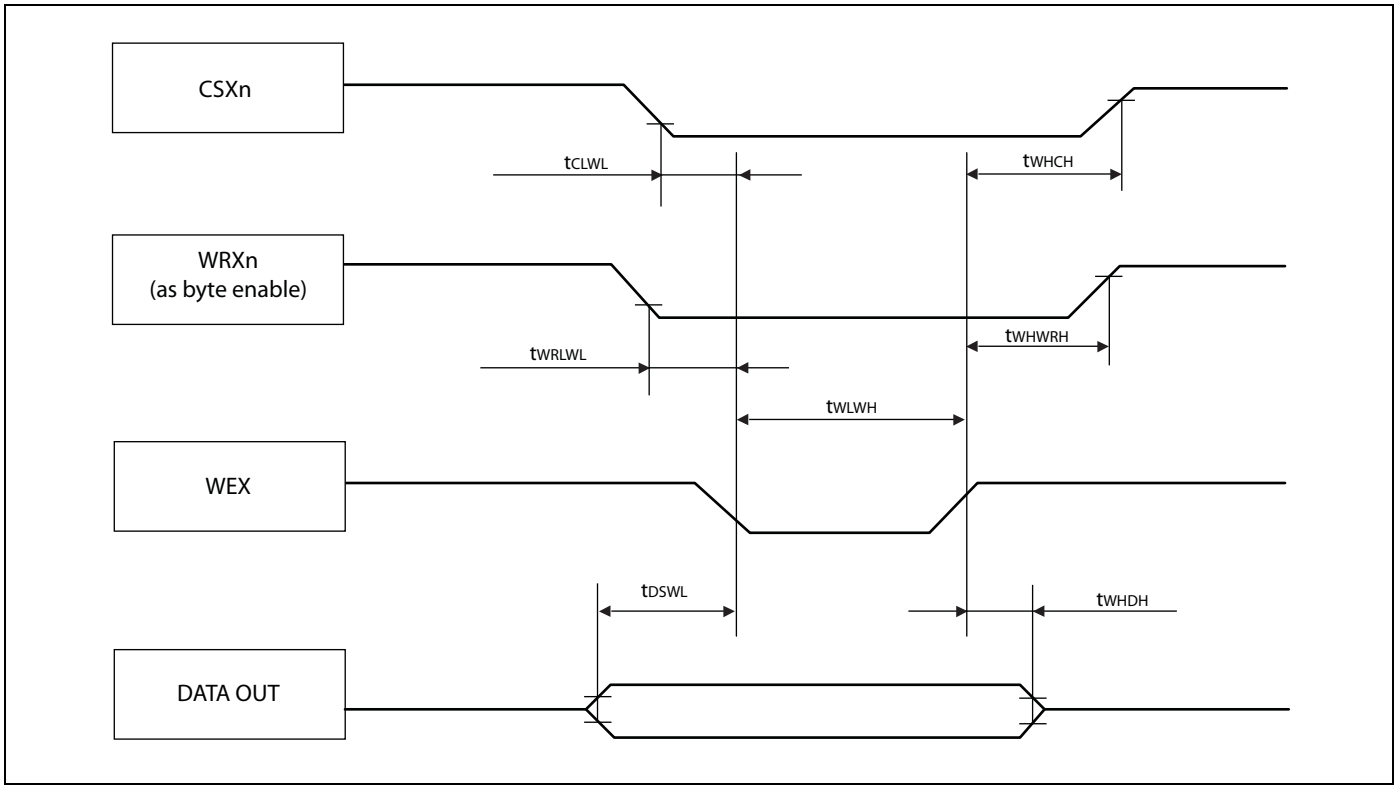
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	t_{CLWRL}	SYSCLK WRXn	—	9	ns
	t_{CLWRH}		− 1	—	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	− 6	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} − 10	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	9	ns
	t_{CLCSH}		—	8	ns



Asynchronous Write Access - Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

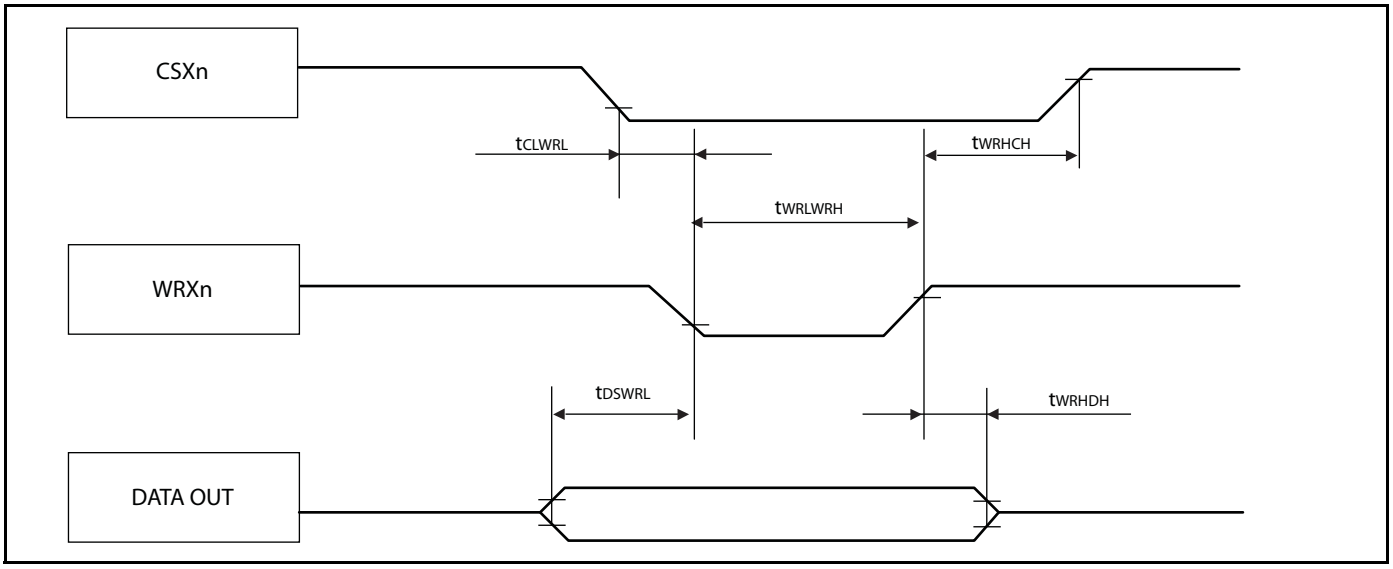
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	t_{WLWH}	WEX	t_{CLKT} − 6	—	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	1/2 × t_{CLKT} − 9	—	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	1/2 × t_{CLKT} − 7	—	ns
WEX to WRXn delay time	t_{WRLWL}	WEX WRXn	—	1/2 × t_{CLKT} + 2	ns
	t_{WHWRH}		1/2 × t_{CLKT} − 1	—	ns
WEX to CSXn delay time	t_{CLWL}	WEX CSXn	—	1/2 × t_{CLKT} - 1	ns
	t_{WHCH}		1/2 × t_{CLKT} + 1	—	ns



Asynchronous Write Access - No Byte Control Type

(V_{DD}35 = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

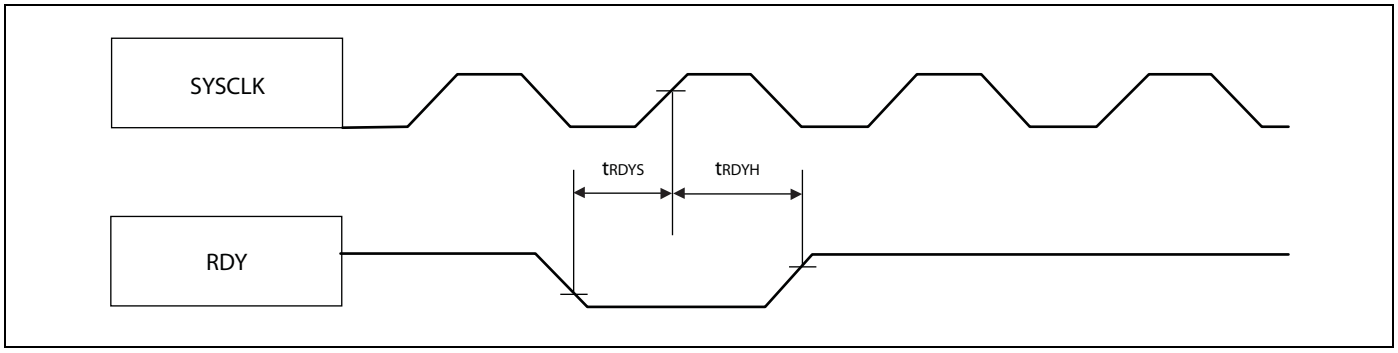
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	t_{WRLWRH}	WRXn	t_{CLKT} − 6	—	ns
Data valid to WRXn ↓ setup time	t^{DSWRL}	WRXn D31 to D0	1/2 × t_{CLKT} − 9	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	1/2 × t_{CLKT} − 7	—	ns
WRXn to CSXn delay time	t_{CLWRL}	WRXn CSXn	—	1/2 × t_{CLKT} − 1	ns
	t_{WRHCH}		1/2 × t_{CLKT} + 1	—	ns



RDY Waitcycle Insertion

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
RDY setup time	t_{RDYS}	SYSCLK RDY	19	—	ns
RDY hold time	t_{RDYH}	SYSCLK RDY	0	—	ns

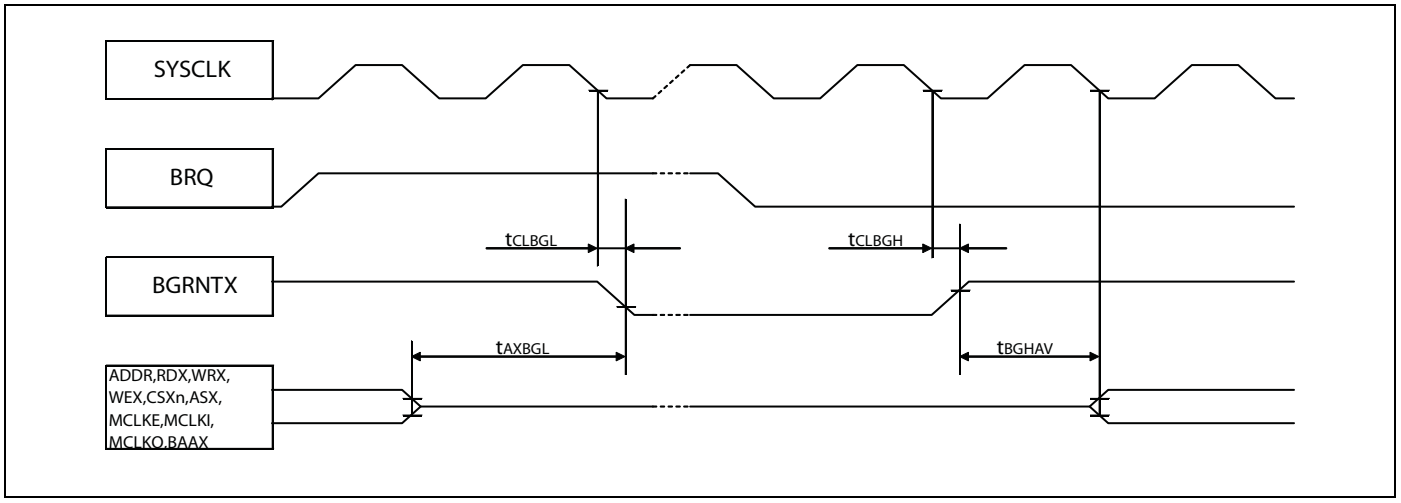


Bus Hold Timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to BGRNTX delay time	t_{CLBGL}	SYSCLK BGRNTX	—	5	ns
	t_{CLBGH}		—	5	ns
Bus HIZ to BGRNTX ↓	t_{AXBGL}	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	t_{CLKT} + 2	—	ns
BGRNTX ↑ to Bus drive	t_{BGHAV}		t_{CLKT} + 1	—	ns

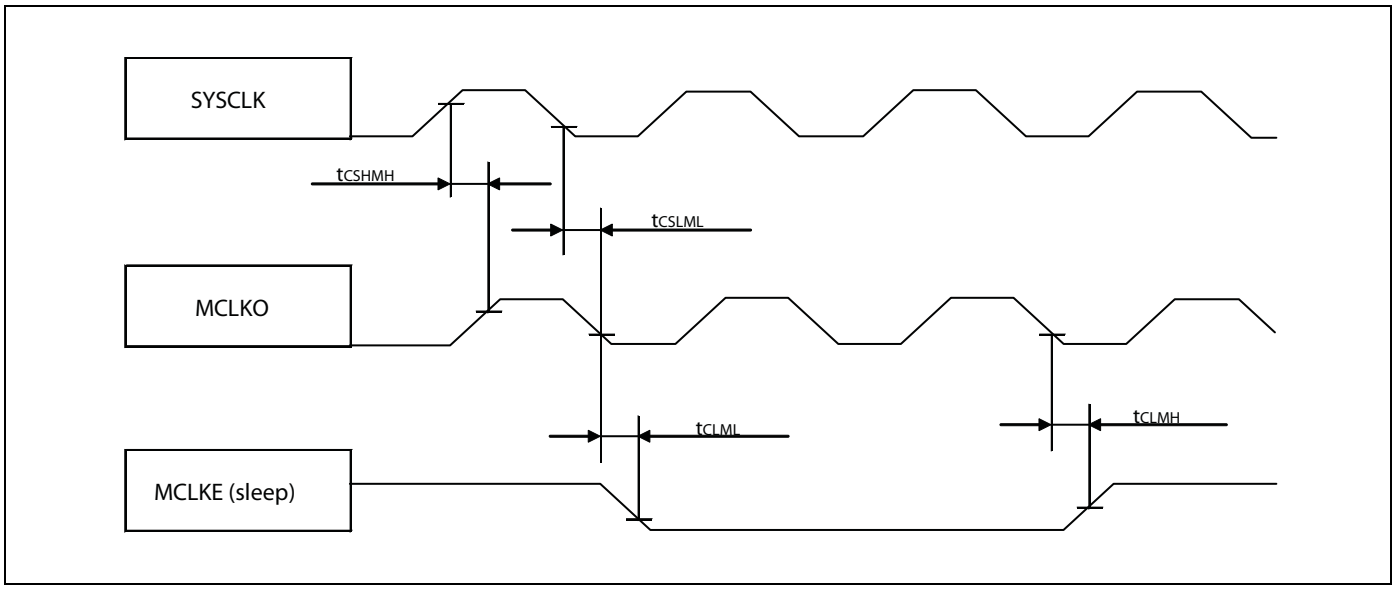
Note : BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX).
It must be kept High as long as the bus shall be hold.
After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.



Clock Relationships

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK to MCLKO	t_{CSHMH}	SYSCLK MCLKO	1	5	ns
	t_{CSLML}		0	2	ns
MCLKO ↓ to MCLKE (in sleep mode)	t_{CLML}	MCLKO MCLKE	—	5	ns
	t_{CLMH}		– 3	—	ns

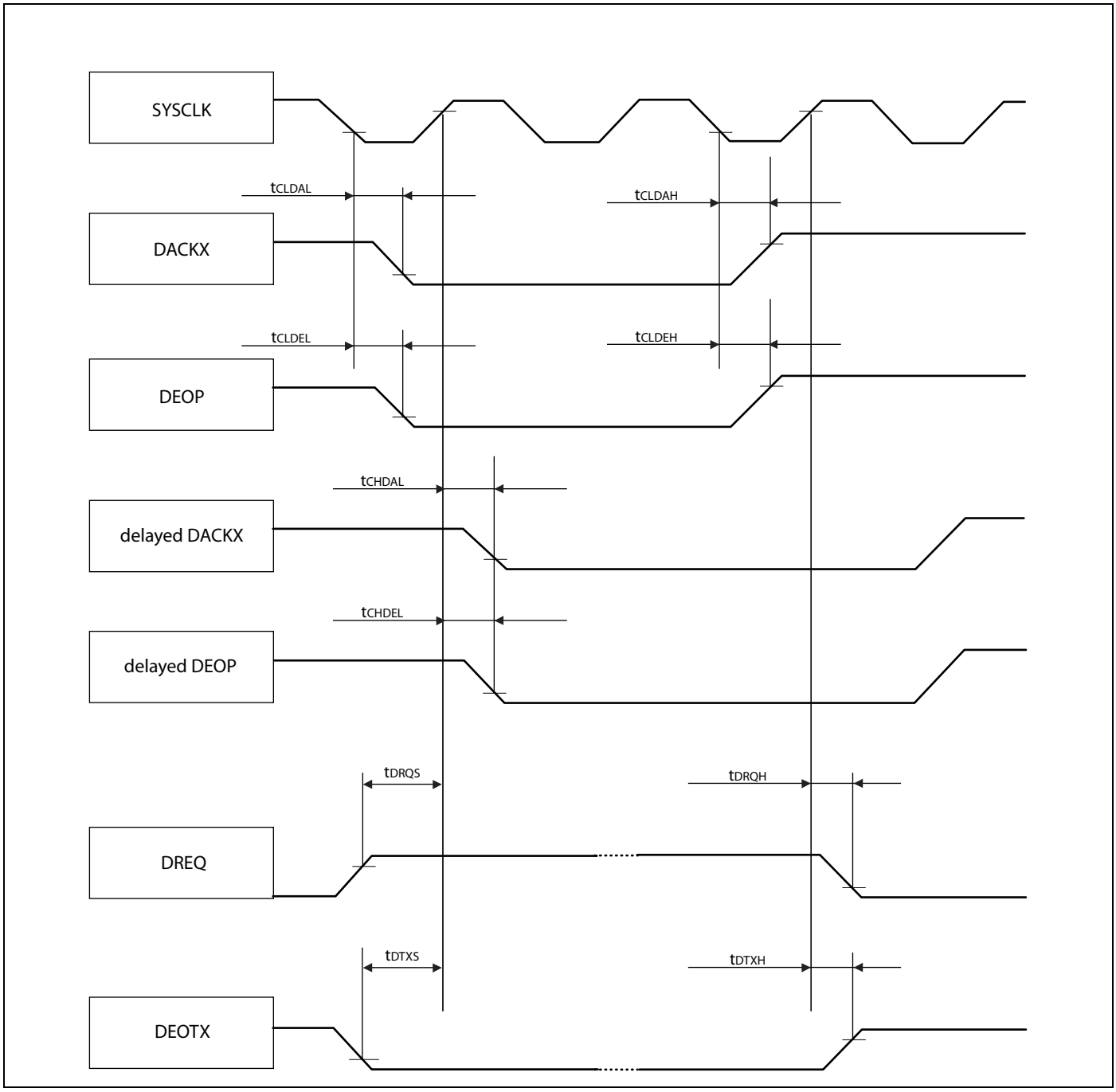


DMA Transfer

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to DACKX delay time	t_{CLDAL}	SYSCLK DACKXn	—	8	ns
	t_{CLDAH}		—	8	ns
SYSCLK ↓ to DEOP delay time	t_{CLDEL}	SYSCLK DEOPn	—	7	ns
	t_{CLDEH}		—	9	ns
SYSCLK ↑ to DACKX delay time (ADDR → CS delayed)	t_{CHDAL}	SYSCLK DACKXn	− 1	8	ns
SYSCLK ↑ to DEOP delay time (ADDR → CS delayed)	t_{CHDEL}	SYSCLK DEOPn	− 1	8	ns
DREQ setup time	t_{DRQS}	SYSCLK DREQn	19	—	ns
DREQ hold time	t_{DRQH}	SYSCLK DREQn	0	—	ns
DEOTXn setup time	t_{DTXS}	SYSCLK DEOTXn	20	—	ns
DEOTXn hold time	t_{DTXH}	SYSCLK DEOTXn	0	—	ns

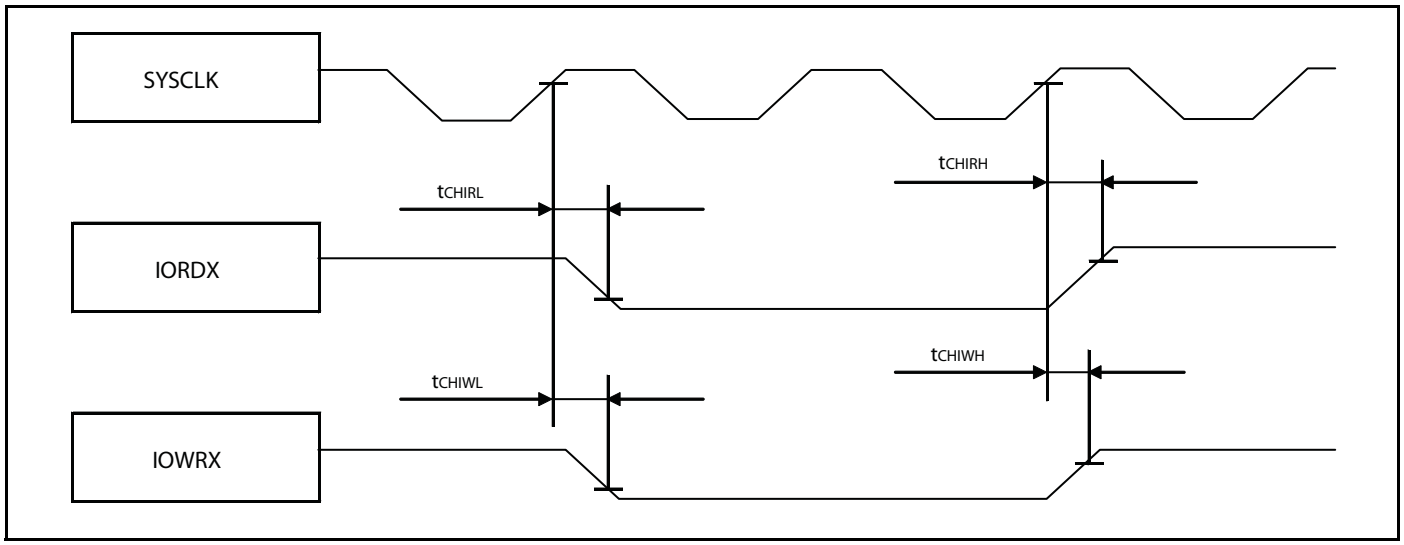
Note : DREQ and DEOTX must be applied for at least 5 × t_{CLKT} to ensure that they are really sampled and evaluated. Under best case conditions (DMA not busy) only setup and hold times are required.


SYSCLK
tCLDAL
tCLDAH
DACKX
tCLDEL
tCLDEH
DEOP
tCHDAL
delayed DACKX
tCHDEL
delayed DEOP
tDRQS
tDRQH
DREQ
tDTXS
tDTXH
DEOTX

DMA Flyby Transfer

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↑ to IORDX delay time	t_{CHIRL}	SYSCLK IORDX	- 2	8	ns
	t_{CHIRH}		0	4	ns
SYSCLK ↑ to IOWRX delay time	t_{CHIWL}	SYSCLK IOWRX	- 2	8	ns
	t_{CHIWH}		- 1	3	ns



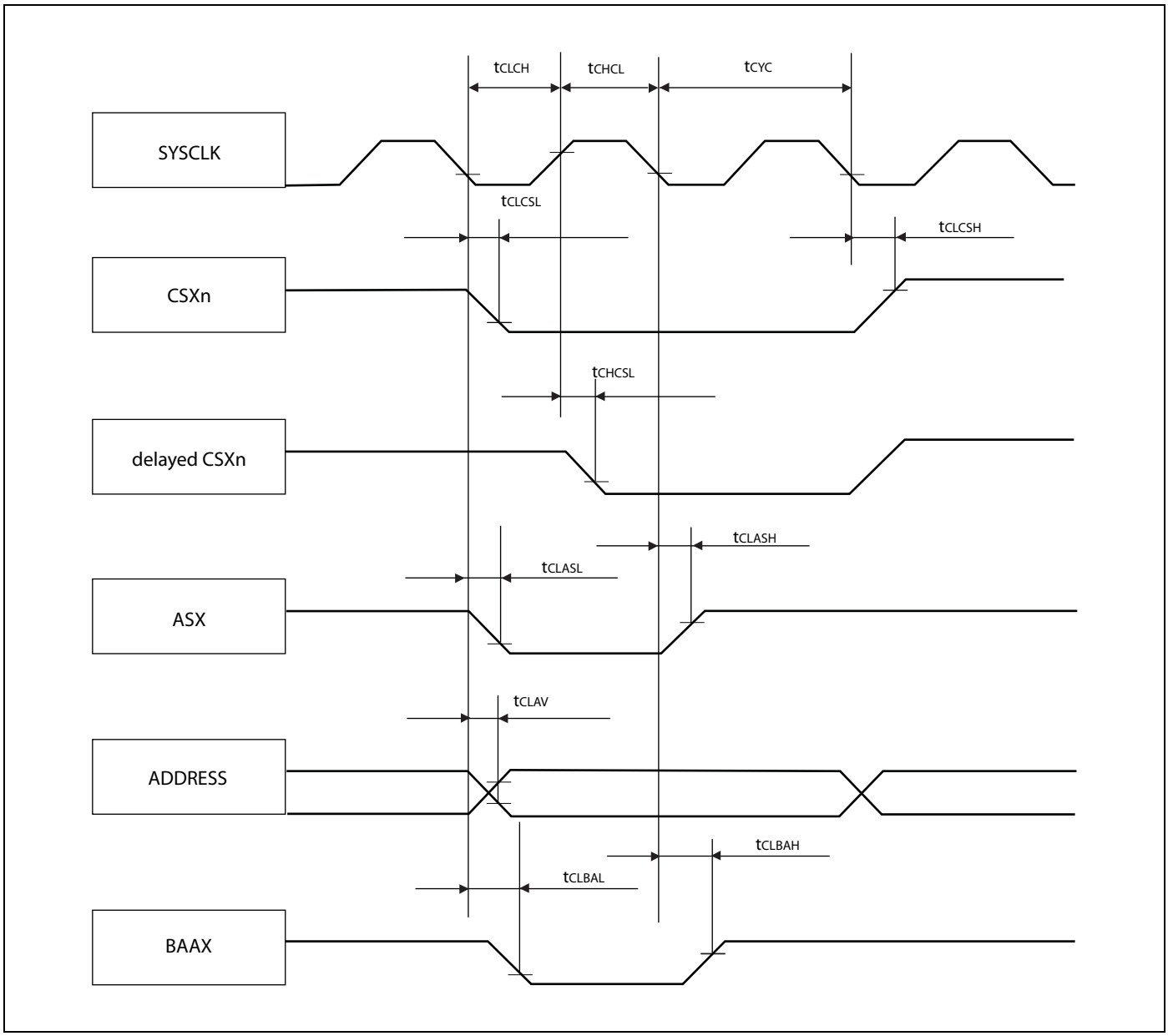
16.7.8 External Bus AC Timings at $V_{DD}35$ = 3.0 to 4.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 3.0 V to 4.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = − 40°C to $T_{A(max)}$
  - C_l = 50 pF
  - VOL = 0.2 × $V_{DD}35$
  - VOH = 0.8 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = = worst case)

Basic Timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 × t_{CLKT} − 1	1/2 × t_{CLKT} + 3	ns
	t_{CHCL}		1/2 × t_{CLKT} − 3	1/2 × t_{CLKT} + 1	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	9	ns
	t_{CLCSH}		—	7	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		− 1	4	ns
SYSCLK ↓ to ASX delay time	t_{CLASL}	SYSCLK ASX	—	5	ns
	t_{CLASH}		—	6	ns
SYSCLK ↓ to BAAX delay time	t_{CLBAL}	SYSCLK BAAX	—	6	ns
	t_{CLBAH}		0	—	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A27 to A0	—	13	ns

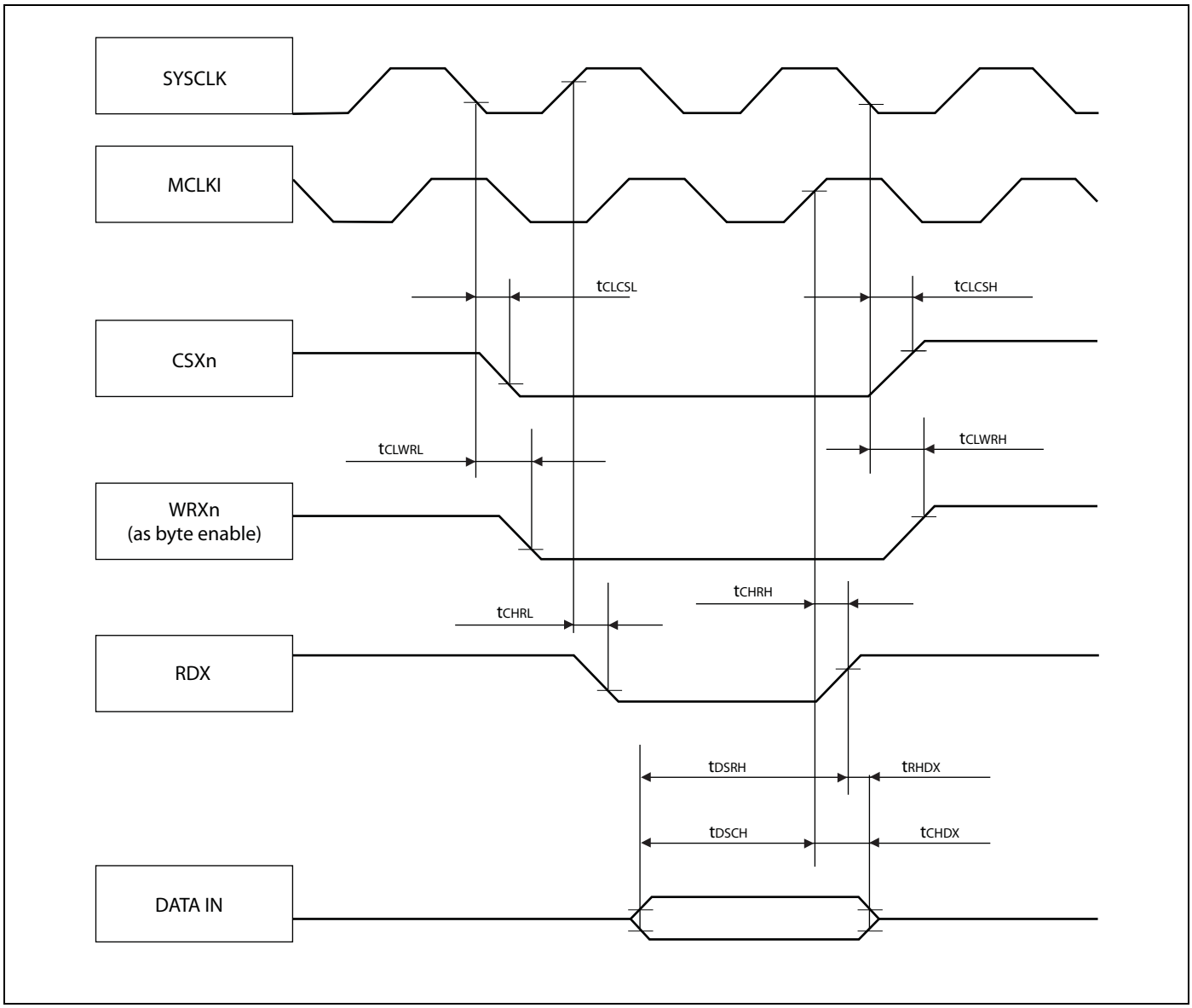

tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Synchronous/Asynchronous Read Access with External MCLKI Input

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↑/MCLKI ↑ to RDX delay time	t_{CHRL}	SYSCLK RDX	− 1	3	ns
	t_{CHRH}	MCLKI RDX	11	25	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	25	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	t_{RHDX}	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	t_{DSCH}	MCLKI D31 to D0	1	—	ns
MCLKI ↑ to Data valid hold time	t_{CHDX}	MCLKI D31 to D0	3	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	SYSCLK WRXn	—	5	ns
	t_{CLWRH}		- 1	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	5	ns
	t_{CLCSH}		—	6	ns

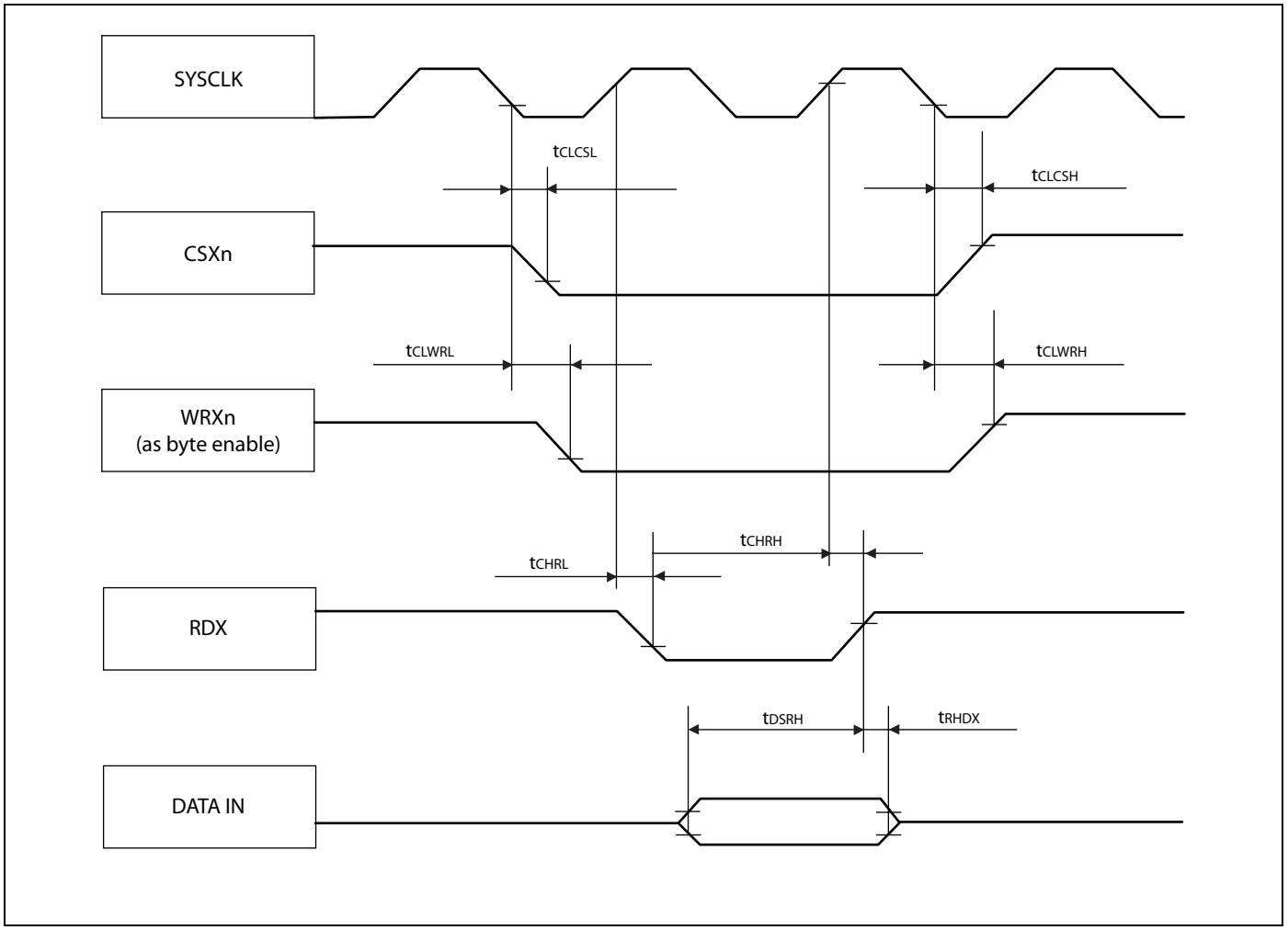
Note: The usage of the external feedback from MCLKO to MCLKI is not recommended.


SYSCLK
MCLKI
tCLCSL
tCLCSH
CSXn
tCLWRL
tCLWRH
WRXn
(as byte enable)
tCHRH
tCHRL
RDX
tDSRH
tRHDX
tDSCH
tCHDX
DATA IN

Synchronous/Asynchronous Read Access with Internal MCLKO --> MCLKI Feedback

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

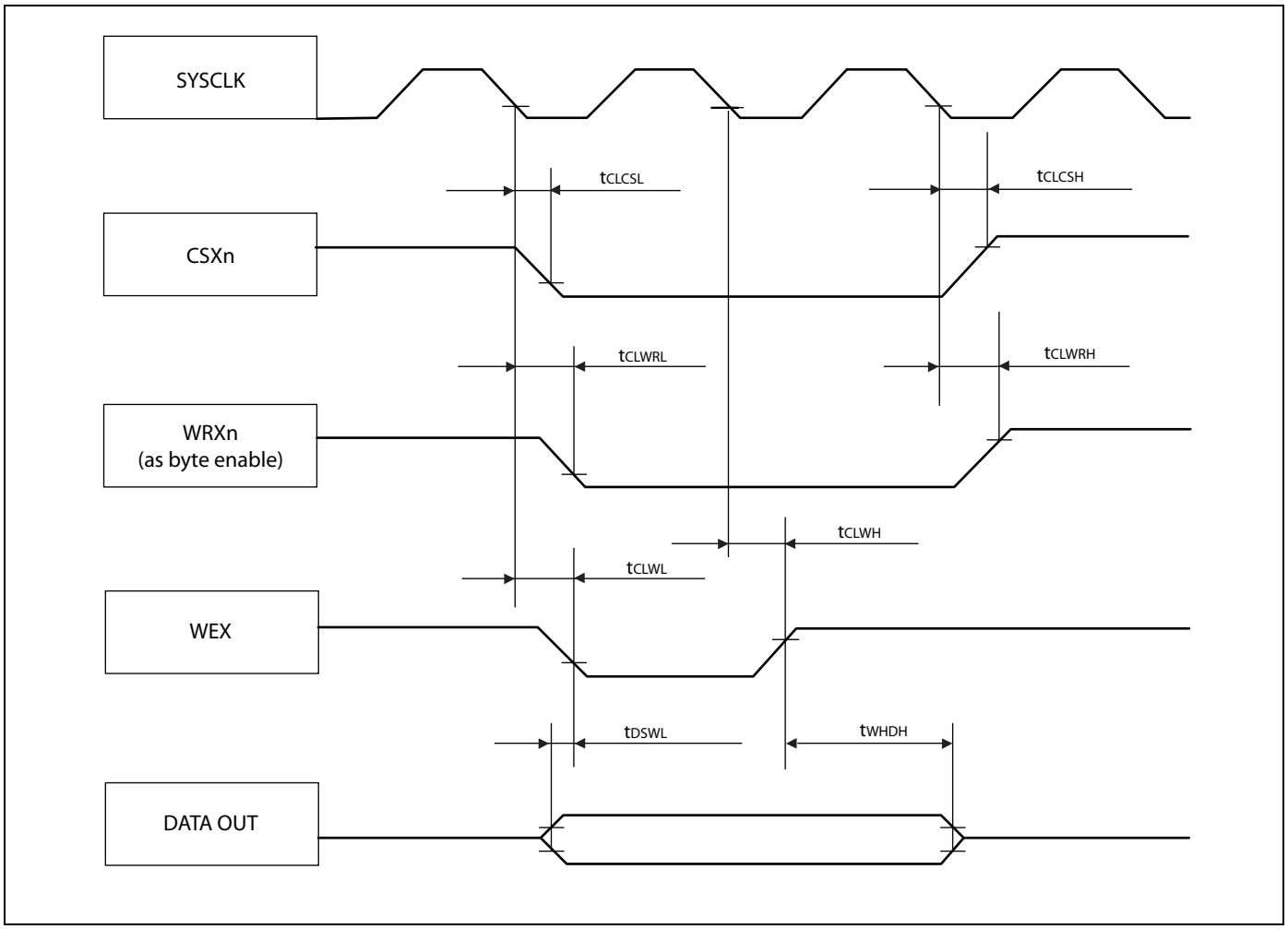
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	t_{CHRL}	SYSCLK RDX	− 1	3	ns
	t_{CHRH}		− 2	4	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	25	—	ns
RDX ↑ to Data valid hold time (internal MCLKO → MCLKI / /MCLKI feedback)	t_{RHDX}	RDX D31 to D0	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	SYSCLK WRXn	—	5	ns
	t_{CLWRH}		- 1	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	5	ns
	t_{CLCSH}		—	6	ns



Synchronous Write Access - Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

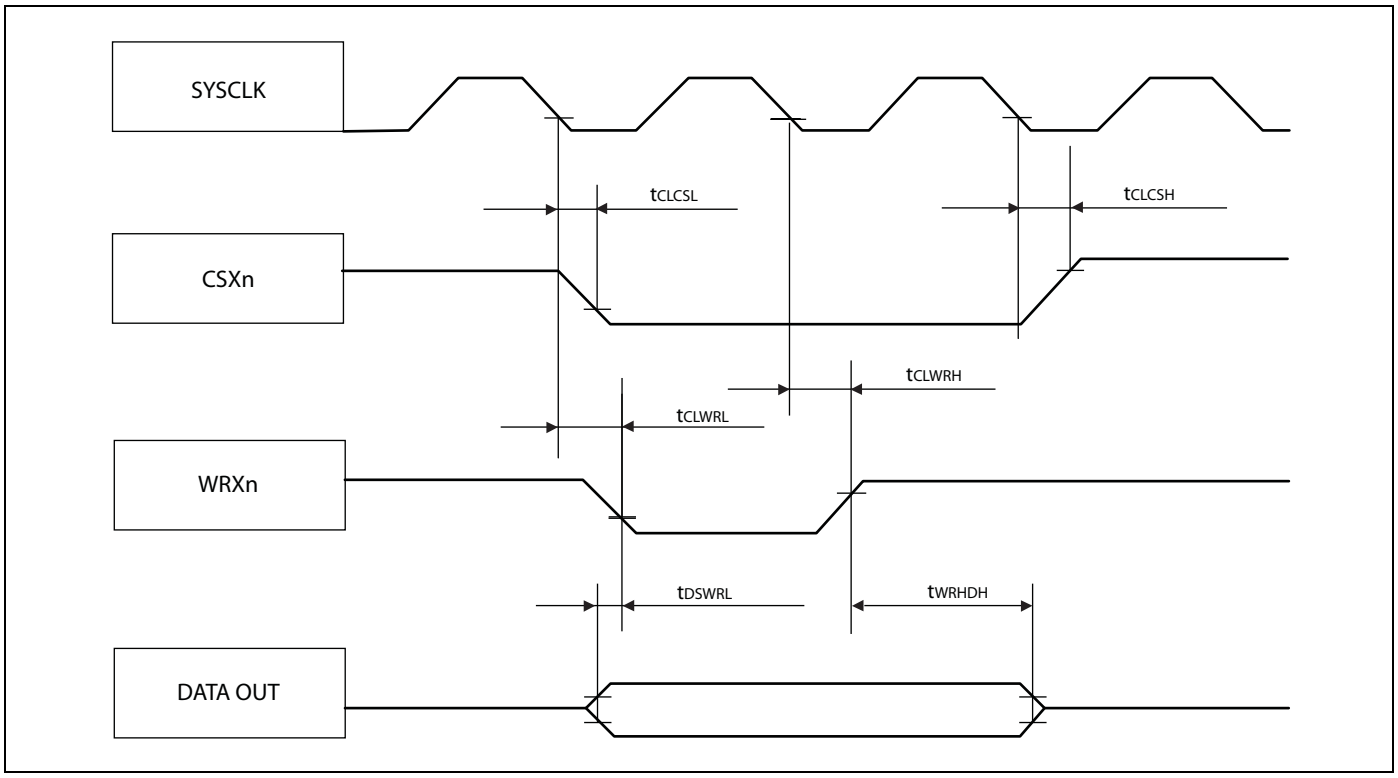
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to WEX delay time	t_{CLWL}	SYSCLK WEX	—	5	ns
	t_{CLWH}		- 1	—	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	− 11	—	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	t_{CLKT} − 13	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	SYSCLK WRXn	—	5	ns
	t_{CLWRH}		- 1	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	5	ns
	t_{CLCSH}		—	6	ns



Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

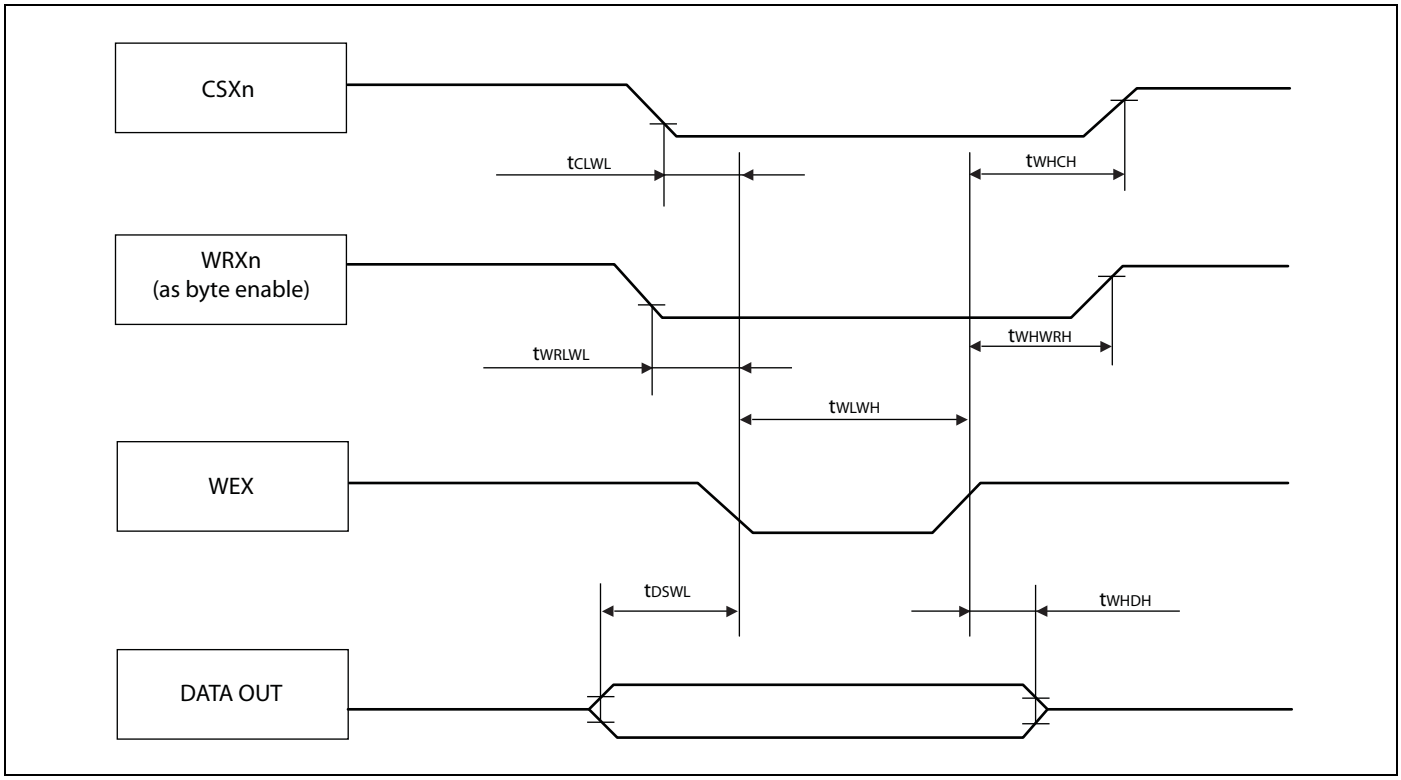
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	t_{CLWRL}	SYSCLK WRXn	—	5	ns
	t_{CLWRH}		- 1	—	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	− 11	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} − 13	—	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	5	ns
	t_{CLCSH}		—	6	ns



Asynchronous Write Access - Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

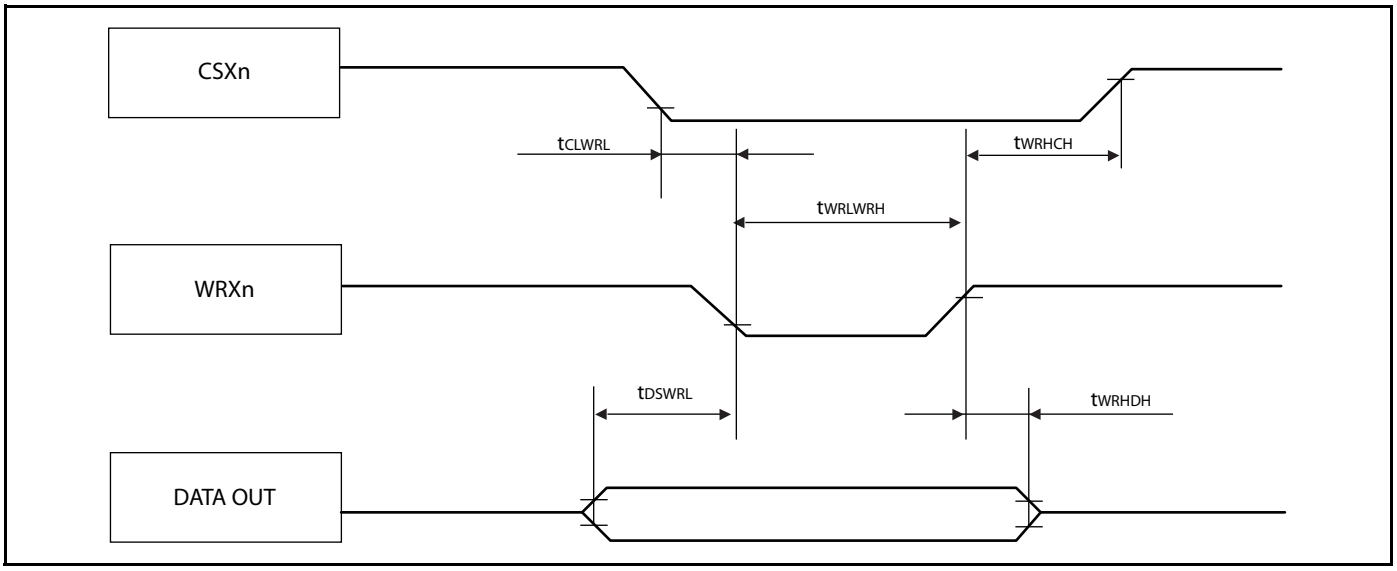
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	t_{WLWH}	WEX	t_{CLKT} − 4	—	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	1/2 × t_{CLKT} − 12	—	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	1/2 × t_{CLKT} − 11	—	ns
WEX to WRXn delay time	t_{WRLWL}	WEX WRXn	—	1/2 × t_{CLKT} + 1	ns
	t_{WHWRH}		1/2 × t_{CLKT} − 1	—	ns
WEX to CSXn delay time	t_{CLWL}	WEX CSXn	—	1/2 × t_{CLKT} − 1	ns
	t_{WHCH}		1/2 × t_{CLKT} + 1	—	ns



Asynchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

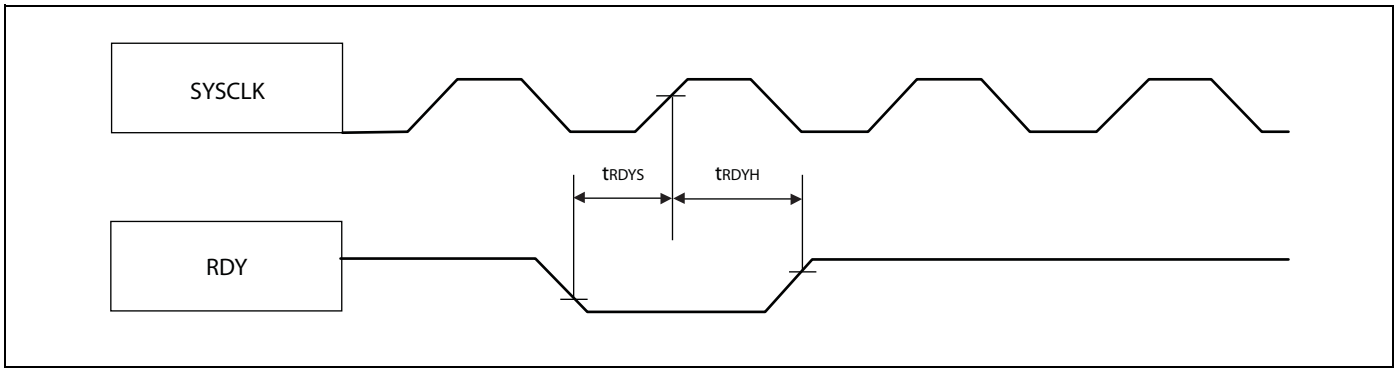
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	t_{WRLWRH}	WRXn	t_{CLKT} − 3	—	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	1/2 × t_{CLKT} − 12	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	1/2 × t_{CLKT} − 11	—	ns
WRXn to CSXn delay time	t_{CLWRL}	WRXn CSXn	—	1/2 × t_{CLKT} − 1	ns
	t_{WRHCH}		1/2 × t_{CLKT} + 1	—	ns



RDY Waitcycle Insertion

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
RDY setup time	t_{RDYS}	SYSCLK RDY	24	—	ns
RDY hold time	t_{RDYH}	SYSCLK RDY	0	—	ns

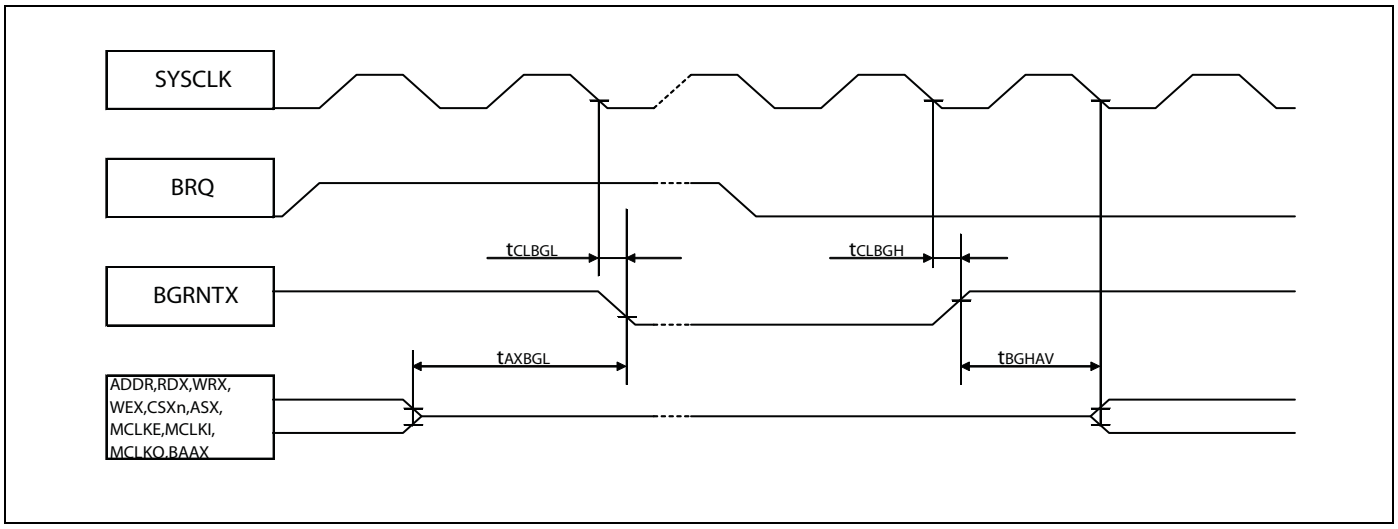


Bus Hold Timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to BGRNTX delay time	t_{CLBGL}	SYSCLK BGRNTX	—	5	ns
	t_{CLBGH}		—	6	ns
Bus HIZ to BGRNTX ↓	t_{AXBGL}	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	t_{CLKT} + 2	—	ns
BGRNTX ↑ to Bus drive	t_{BGHAV}		t_{CLKT} - 2	—	ns

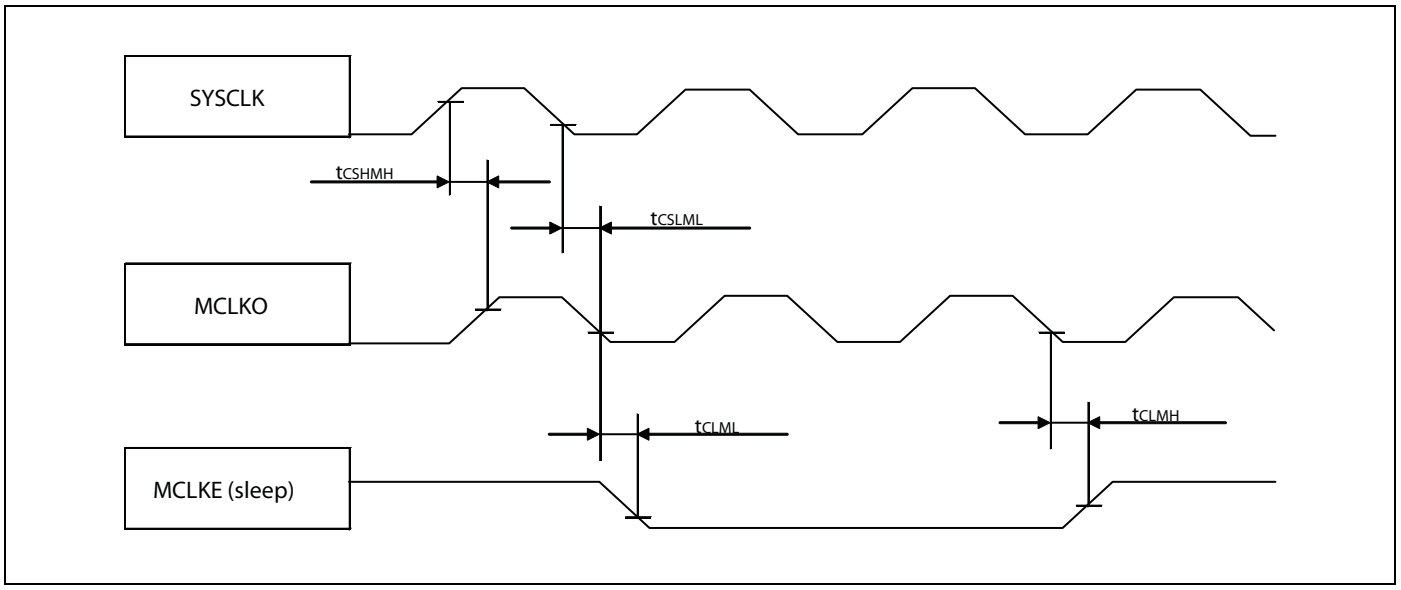
Note : BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX).
It must be kept High as long as the bus shall be hold.
After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.



Clock Relationships

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK to MCLKO	t_{CSHMH}	SYSCLK MCLKO	1	5	ns
	t_{CSLML}		0	2	ns
MCLKO ↓ to MCLKE (in sleep mode)	t_{CLML}	MCLKO MCLKE	—	4	ns
	t_{CLMH}		- 3	—	ns

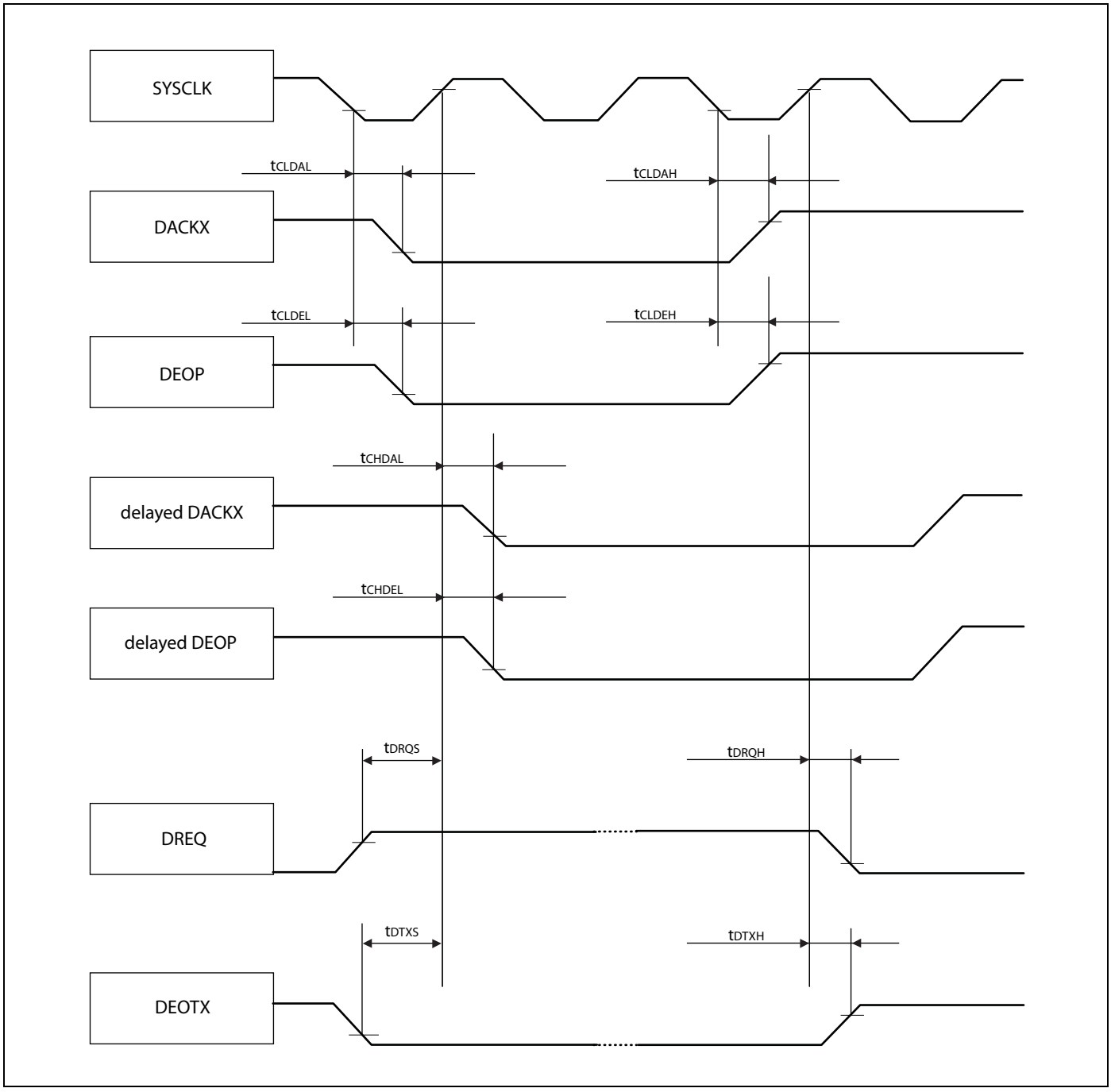


DMA Transfer

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to $T_{A(max)}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↓ to DACKX delay time	t_{CLDAL}	SYSCLK DACKXn	—	9	ns
	t_{CLDAH}		—	7	ns
SYSCLK ↓ to DEOP delay time	t_{CLDEL}	SYSCLK DEOPn	—	8	ns
	t_{CLDEH}		—	7	ns
SYSCLK ↑ to DACKX delay time (ADDR → CS delayed)	t_{CHDAL}	SYSCLK DACKXn	0	8	ns
SYSCLK ↑ to DEOP delay time (ADDR → CS delayed)	t_{CHDEL}	SYSCLK DEOPn	− 1	8	ns
DREQ setup time	t_{DRQS}	SYSCLK DREQn	25	—	ns
DREQ hold time	t_{DRQH}	SYSCLK DREQn	0	—	ns
DEOTXn setup time	t_{DTXS}	SYSCLK DEOTXn	26	—	ns
DEOTXn hold time	t_{DTXH}	SYSCLK DEOTXn	0	—	ns

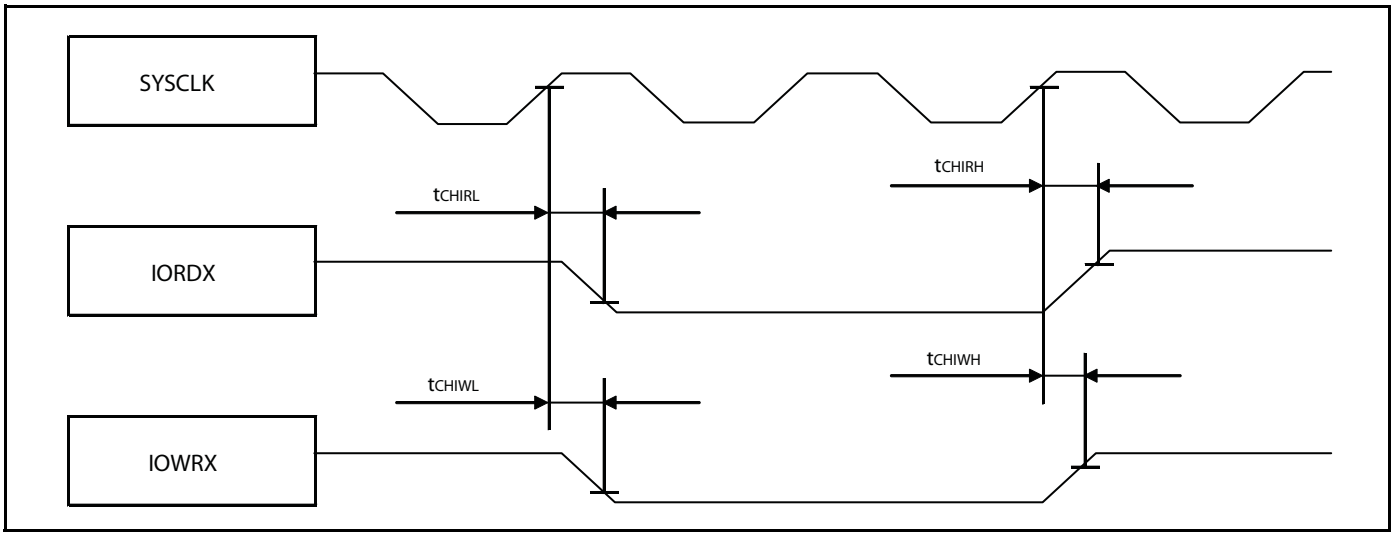
Note : DREQ and DEOTX must be applied for at least 5 × t_{CLKT} to ensure that they are really sampled and evaluated. Under best case conditions (DMA not busy) only setup and hold times are required.


SYSCLK
tCLDAL
tCLDAH
DACKX
tCLDEL
tCLDEH
DEOP
tCHDAL
delayed DACKX
tCHDEL
delayed DEOP
tDRQS
tDRQH
DREQ
tDTXS
tDTXH
DEOTX

DMA Flyby Transfer

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40°C to $T_{A(max)}$)

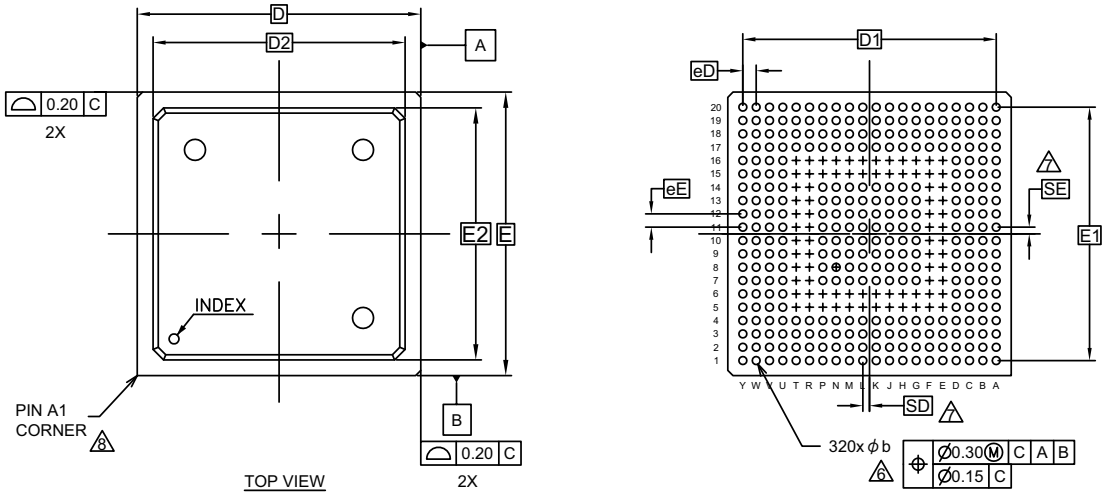
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
SYSCLK ↑ to IORDX delay time	t_{CHIRL}	SYSCLK IORDX	- 1	6	ns
	t_{CHIRH}		- 2	3	ns
SYSCLK ↑ to IOWRX delay time	t_{CHIWL}	SYSCLK IOWRX	0	5	ns
	t_{CHIWH}		- 2	3	ns



17. Ordering Information

Part Number	Package	Maximum ambient temperature $T_{A(max)}$	Remarks
CY91F469QAHPB-GS-UJE1	320-pin plastic BGA (BYA320)	+ 125°C	Lead-free package

18. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	2.46
A1	0.35	——	——
D	27.00 BSC		
E	27.00 BSC		
D1	24.00 BSC		
E 1	24.00 BSC		
MD	20		
ME	20		
n	320		
Φb	0.60	0.75	0.90
eD	1.27 BSC		
eE	1.27 BSC		
SD / SE	0.635		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. JEDEC SPECIFICATION NO. REF: N/A.

002-16414 **

19. Revision History

Version	Date	Remark
2.0	2008-01-28	Initial version
2.1	2008-02-05	Pins 257 to 320 are GND.
2.2	2008-02-11	The CANs have only 32-message buffers
2.3	2008-02-15	Corrected product lineup: No NMI function, updated disclaimer at the end
2.4	2008-02-21	ICU8,9: PFR must be 0, DDR recommended 0
2.5	2008-02-22	Corrected naming and size of Flash-cache (F-cache)
2.6	2008-04-30	- IO MAP: initial values for LVSEL + REGSEL corrected - Pin 110: CK0 --> CK0/8 (added Free Run Timer 8) - Flash memory operation modes: Added note about the "flash access mode switching" incl. Boot ROM start address - Flash parallel programming: wait times after power-on / INIT added - External Bus AC spec: T_{AXBGL} values corrected - IO Map: removed INT Relocation control registers (was reservation only) - INT Vector Table: Added resource numbers for INT16-23 - added chapter SPECIAL PORT / RESOURCE ASSIGNMENTS
2.7	2008-05-05	INT Vector Table: Added resource numbers for FRT8 and ICU8,9
2.8	2008-05-08	Updated the section about re-located interrupts (Ports 34+35)
2.9	2008-08-18	- Corrected I/O circuit type of P24_4 from A to C. - SPECIAL PORT / RESOURCE ASSIGNMENTS: corrected the notes that only digital inputs (no outputs) are disabled if an analog function (ADC) is enabled on this port. - FLASH: Corrected a typo in the note about the "flash access mode switching" incl. address in Boot ROM; added section "Poweron Sequence in parallel programming mode" - IO CIRCUIT TYPE: fixed typos in Remarks - "Notes on PS register" updated - IO Map: Initial values of PFR00 - PFR10 corrected (depend on MD=000) - INT Vector Table: Added Resource number for ADC1 (RN=113); corrected the footnotes - Electrical Characteristics: removed the note that analog input/output pins cannot accept +B signal input. - DC Characteristics: Updated I_{IL} and I_{AIN}, updated I_{LVE} and $I_{LVI,}$ corrected values of Pull up/down resistances, updated and re-ordered the table footnotes - ADC Characteristics: fixed the typos regarding "nonlinearity error" - fixed offset between input channels
2.10	2008-08-19	DC characteristics: updated the current consumption values I_{CC}, I_{CCH} (target values based on MB91F469G)
2.11	2008-09-23	I/O MAP: Removed the notes about new INT disable feature, added bookmarks inside IO MAP Added note to IOS register (addr. 0xC03) "always write 1 to IOS[1]"

Version	Date	Remark
2.12	2008-11-07	PIN Definitions: Corrected pin 145 into P34_5 Flash Security Vector FSV2: Corrected typo in table header Embedded Program/Data Memory (Flash): Added section 7 “Notes About Flash Memory CRC Calculation” (CLKB must be faster then the RC clock) Block Diagram: Added External Bus Instruction Cache Special Port/Resource Assignments: Corrected section “The Additional External Interrupts” (PFR/EPFR/ADERH settings)
2.13	2009-01-09	Special Port/Resource Assignments: Re-located External Interrupts: Corrected that SDA2 is enabled by PFR24 (not by EPFR24) IO Map: Added EPFR34, EPFR35 at address 0x00DE2, 0x00DE3 IO Map: Corrected the table header (address +0,+1,+2,+3) DC characteristics: corrected the current consumption values I_{CC}, I_{CCH}

20. Major Changes

Spansion Publication Number: DS07-16614-1E

Page	Section	Change Results
26	I/O Circuit Types	Changed the table of Type I. Pull-down resistor value: 50 kW approx. → Pull-down resistor value: 50 kΩ approx.
107	Electrical Characteristics 4. A/D converter characteristics	Changed the table of “Zero reading voltage”. AVRL – 1.5 → AVRL – 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V Changed the table of Full scale reading voltage. AVRH – 3.5 → AVRH – 3.5 LSB AVRH – 1.5 → AVRH – 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V
115	7.3. LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V	Changed the sentences. - Ta = -40 °C to +105 × °C → - Ta = -40 °C to +105 °C

NOTE: Please see “Document History” about later revised information.

Page	Section	Change Results
Rev. *B		
—	Changed marketing part numbers from prefix MB to prefix CY.	
2 6 147 148	Features 2.Pin Assignment 16.Ordering Information 17.Package Dimension	Modified package description to JEDEC description.
147	16.Ordering Information	Changed Marketing Part Number as follows: - before) MB91F469QAPB-GSE1 - after) CY91F469QAHPB-GS-UJE1
Rev. *C		
1	Features Internal peripheral resources	Renamed the Low Voltage detection → Supply Supervisor
2	Features Package and technology	Changed Operating temperature range upper limit from + 105°C → + 105°C / + 125°C and added footnote about $T_{A(max)}$
4	Product Lineup Software-Watchdog	Renamed "Watchdog timer" → "Software watchdog" Renamed "Watchdog timer (RC osc. based)" → "Hardware-Watchdog (RC osc. based)"
5	Product Lineup Temperature Range (TA)	Changed the symbol of ambient temperature from "Ta" into "T_A", changed CY91F469Q upper limit from 105°C → “$T_{A(max)}$”
5	Product Lineup Power Consumption	Changed the value from < 1W → < 2W

Page	Section	Change Results
38	CPU and Control Unit 9.3 Programming model 9.3.1 Basic programming model	Corrected the name of program status register from "RS" → "PS"
59, 61, 65	I/O Map TCDT0 [R/W] to TCDT8 [R/W]	Free Run Timer 0-8: Changed the TCDT register initialization value from 0xXXXX → 0x0000 (by RST)
60	I/O Map LIN-USART (FIFO) 11	Corrected RDR00/TDR00 → RDR11/TDR11
68	I/O Map PFR01 to PFR10	Corrected the foot note number from 4 → 5
89, 90	Recommended Settings 15.1 PLL and Clockgear settings, 15.2 Clock Modulator settings	Added “Please refer to Absolute maximum ratings...”
97	Electrical Characteristics 16.1 Absolute maximum ratings Permitted operating frequency CY91F469QA, CY91F469QAH	Added these parameters, depending on device, T_A and regulator setting
98	Electrical Characteristics 16.1 Absolute maximum ratings Permitted power consumption *7	Added these parameters, depending on device and T_A , added the attached footnotes on next page.
99	Electrical Characteristics 16.2 Recommended operating conditions Operating temperature	Changed maximum from +105°C → $T_{A(max)}$ and added remark
99	Electrical Characteristics 16.2 Recommended operating conditions Lock-up time PLL (4 MHz ->16 ...100MHz)	Corrected “Look-up time PLL” → “Lock-up time PLL”
100, 103, 107, 109,	Electrical Characteristics 16.3 DC characteristics, 16.4 A/D converter characteristics, 16.5 Alarm comparator characteristics, 16.7 AC characteristics	Changed the condition on top of the tables from T_A = −40°C to +105°C → T_A = −40°C to $T_{A(max)}$ Changed the symbol of ambient temperature from "Ta" → "T_A"
101, 102	Electrical Characteristics 16.3 DC characteristics Input leakage current, Analog input leakage current	Changed the condition from T_A = 105°C → T_A = $T_{A(max)}$
102	Electrical Characteristics 16.3 DC characteristics Power supply current CY91 F469QA, CY91 F469QAH	Added CY91F469QAH, added the IccH parameters for T_A = 125°C
103	Electrical Characteristics 16.4 A/D converter characteristics Compare time	Changed Tcomp max from 16,500 µs → "t.b.d." because this parameter is under re-evaluation.
109	Electrical Characteristics 16.7 AC characteristics 16.7.2 Reset input ratings	INITX input time (at power-on): Changed t_{INTL} minimum from 8 ms → 10 ms (same as the main oscillator stabilization time).
145	Ordering Information	Added table column defining the maximum ambient temperature $T_{A(max)}$

Document History

Document Title: CY91460Q Series FR60 32-bit Microcontroller Document Number: 002-04617				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	06/09/2009	Migrated to Cypress and assigned document number 002-04617. No change to document contents or format.
*A	5218659	AKIH	04/13/2016	Updated to Cypress format.
*B	6503390	SHUS	03/12/2019	Changed marketing part numbers from prefix MB to prefix CY. Modified package description to JEDEC description. Updated the ordering information For details, see 20. Major Changes.
*C	6599730	DOBE	06/20/2019	For detail of change, see Rev. *C of “Major Changes” on page 149

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