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MB91460M series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART, CAN controllers, MediaLB(512Fs)*, and I²S.

*: This product is licensed by SMSC Europe in conditions where it is used in the MediaLB system compliant with the MediaLB specification of the SMSC Europe.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
 - Signed 32-bit multiplication: 5 cycles
 - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal peripheral resources

- General-purpose ports : Maximum 175 ports
- DMAC (DMA Controller)
 - Maximum of 5 channels able to operate simultaneously. (External to external : 1 channel)
 - 3 transfer sources (external pin/internal peripheral/software)
 - Activation source can be selected using software.
 - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
 - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
 - Fly-by transfer support (between external I/O and memory)
 - Transfer data size selectable from 8/16/32-bit
 - Multi-byte transfer enabled (by software)
 - DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
 - 10-bit resolution: 12 channels
 - Conversion time: minimum 3 μs
- External interrupt inputs : 16 channels
 - 4 channels shared with CAN RX or I²C pins

- Bit search module (for REALOS)
 - Function to search from the MSB (most significant bit) for the position of the first "0", "1", or changed bit in a word
- LIN-USART (full duplex double buffer): 9 channels
 - Clock synchronous/asynchronous selectable
 - Sync-break detection
 - Internal dedicated baud rate generator
 - 4 channel is equipped with 16 stages of transmission and reception FIFO buffers.
- I²C bus interface (supports 400 kbps): 8 channels
 - Master/slave transmission and reception
 - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 2 channels
 - Maximum transfer speed: 1 Mbps
 - 32 transmission/reception message buffers
- MediaLB
 - Supports 512Fs
 - 15 channels
 - Contains local channel buffers: 32 bit × 2 k.
 - Contains a 32 bit × 2 k FIFO buffer for between MediaLB and I²S.
- I²S : 10 channels
- 16-bit PPG timer : 8 channels
- 16-bit reload timer: 5 channels
- 16-bit free-run timer: 4 channels (1 channel each for ICU and OCU)
- Input capture: 4 channels (operates in conjunction with the free-run timer)
- Output compare: 4 channels (operates in conjunction with the free-run timer)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit
- Clock modulator
- Sub-clock calibration
 - Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator

- Main oscillator stabilization timer
 - Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
 - Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

Package and technology

- Package : QFP-216
- CMOS 0.18 μm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between -40°C and $+105^{\circ}\text{C}$

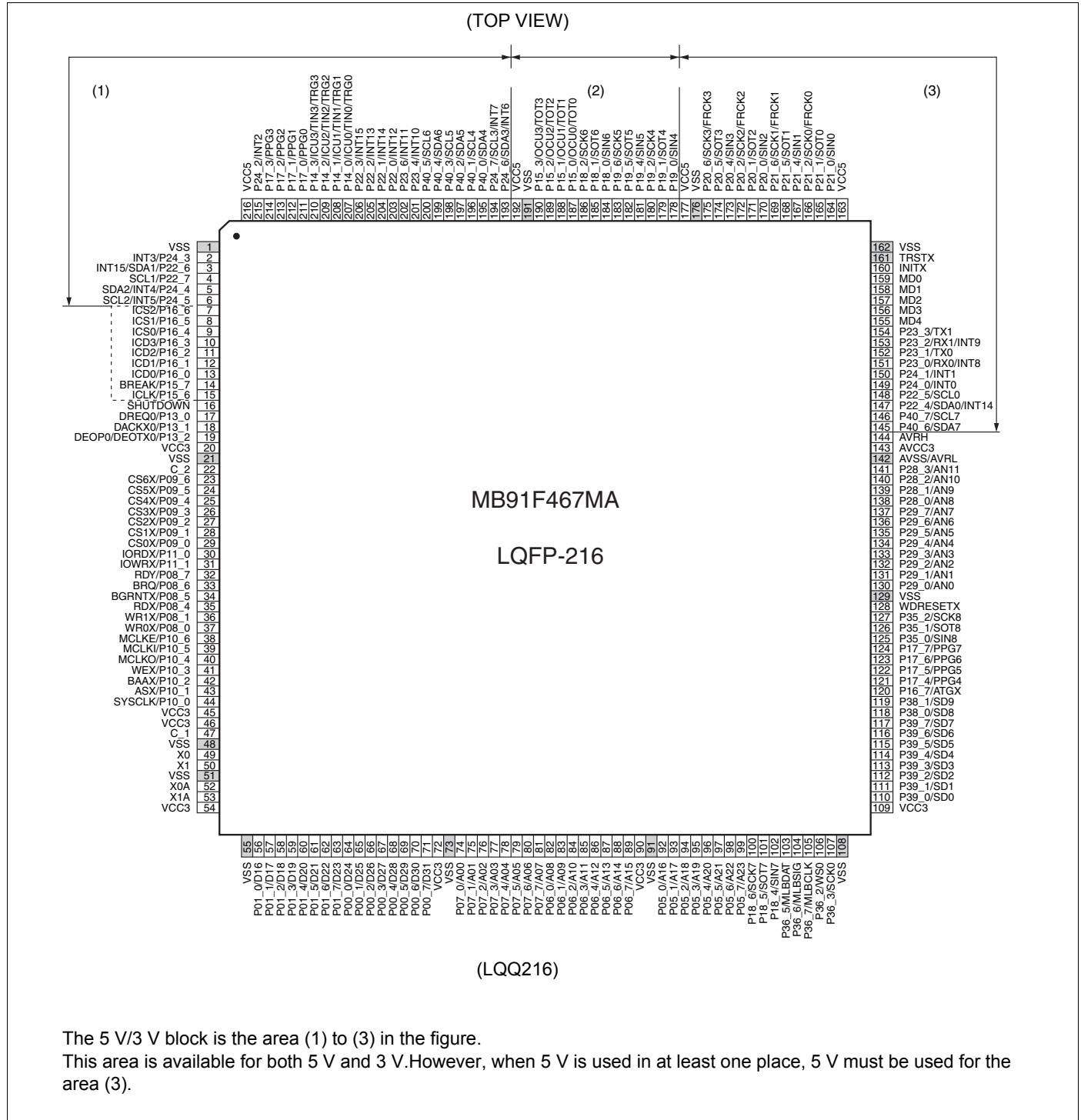
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1. Product Lineup

Feature	MB91F467MA	MB91V460 (Reference)
Core frequency	80 MHz	80 MHz
Resource frequency	20 MHz	40 MHz
External bus frequency	40 MHz	40 MHz
Watchdog timer	Yes	Yes
Bit Search	Yes	Yes
Reset input pin	Yes	Yes
Low power consumption mode	Yes	Yes
DMA	5 channels	5 channels
Flash	1 Mbyte	SRAM
Flash security	Yes	No
D-RAM	48 Kbytes	64 Kbytes
I/D-RAM	16 Kbytes	64 Kbytes
Direct map cache	8 Kbytes	16 Kbytes
I-Cache	4 Kbytes	4 Kbytes
Boot-ROM	4 Kbytes	4 Kbytes
RTC	1 channel	1 channel
Free-run timer	4 channels	8 channels
ICU	4 channels	8 channels
OCU	4 channels	8 channels
Reload timer	5 channels	8 channels
PPG	8 channels	16 channels
C_CAN	2 channels (32 msg + 64 msg)	6 channels (128 msg)
LIN-USART	5 channels + 4 channels FIFO	4 channels + 4 channels FIFO + 8 channels
I ² C	8 channels	4 channels
MediaLB	512Fs	No
I ² S	10 channels	No
External bus	24 bit address / 16 bit data	32 bit address / 32 bit data
External Interrupts	16 channels	16 channels
A/D converter	12 channels	32 channels
DSU4	Yes	Yes
EDSU	Yes	Yes

2. Pin Assignment



3. Pin Description

Pin no.	Pin name	I/O	I/O circuit type*	Function
2	P24_3	I/O	D	General-purpose input/output ports
	INT3			Request input pin of external interrupt ch.3.
3	P22_6	I/O	C	General-purpose input/output ports
	SDA1			Serial data input/output pin of I ² C 1.
	INT15			Request input pin of external interrupt ch.15. Exclusive from P22_3.
4	P22_7	I/O	C	General-purpose input/output ports
	SCL1			Serial clock input/output pin of I ² C 1.
5	P24_4	I/O	C	General-purpose input/output ports
	INT4			Request input pin of external interrupt ch.4.
	SDA2			Serial data input/output pin of I ² C 2.
6	P24_5	I/O	C	General-purpose input/output ports
	INT5			Request input pin of external interrupt ch.5.
	SCL2			Serial clock input/output pin of I ² C 2.
7	P16_6	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	ICS2			Status output pin of DSU4. Enabled when MD4 = "1".
8	P16_5	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	ICS1			Status output pin of DSU4. Enabled when MD4 = "1".
9	P16_4	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	ICS0			Status output pin of DSU4. Enabled when MD4 = "1".
10	P16_3	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	ICD3			Data input/output pin of DSU4. Enabled when MD4 = "1".
11	P16_2	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	ICD2			Data input/output pin of DSU4. Enabled when MD4 = "1".
12	P16_1	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	ICD1			Data input/output pin of DSU4. Enabled when MD4 = "1".
13	P16_0	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	ICD0			Data input/output pin of DSU4. Enabled when MD4 = "1".
14	P15_7	I/O	H	General-purpose input/output ports. Enabled when MD4 = "0".
	BREAK			BREAK input pin of DSU4. Enabled when MD4 = "1".
15	P15_6	I/O	I	General-purpose input/output ports. Enabled when MD4 = "0".
	ICLK			Clock output pin of DSU4. Enabled when MD4 = "1".
16	SHUTDOWN	O	J	Shutdown output, H active.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
17	P13_0	I/O	H	General-purpose input/output ports.
	DREQ0			Input pin for DMA transfer request.
18	P13_1	I/O	H	General-purpose input/output ports.
	DACKX0			Output pin for DMA transfer request acknowledge.
19	P13_2	I/O	H	General-purpose input/output ports.
	DEOTX0			Input pin for DMA transfer stop request.
	DEOP0			Output pin for DMA transfer end.
23	P09_6	I/O	H	General-purpose input/output ports.
	CS6X			Output pin of external bus chip select area 6.
24	P09_5	I/O	H	General-purpose input/output ports.
	CS5X			Output pin of external bus chip select area 5.
25	P09_4	I/O	H	General-purpose input/output ports.
	CS4X			Output pin of external bus chip select area 4.
26	P09_3	I/O	H	General-purpose input/output ports.
	CS3X			Output pin of external bus chip select area 3.
27	P09_2	I/O	H	General-purpose input/output ports.
	CS2X			Output pin of external bus chip select area 2.
28	P09_1	I/O	H	General-purpose input/output ports.
	CS1X			Output pin of external bus chip select area 1.
29	P09_0	I/O	H	General-purpose input/output ports.
	CS0X			Output pin of external bus chip select area 0.
30	P11_0	I/O	H	General-purpose input/output ports.
	IORDX			Output pin for DMA fly-by transfer from I/O to memory.
31	P11_1	I/O	H	General-purpose input/output ports.
	IOWRX			Output pin for DMA fly-by transfer from memory to I/O.
32	P08_7	I/O	H	General-purpose input/output ports.
	RDY			External bus ready input pin (when RDY is enabled to a corresponding CS area).

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
33	P08_6	I/O	H	General-purpose input/output ports.
	BRQ			External bus open request input pin (when sharing is enabled to a corresponding CS area) .
34	P08_5	I/O	H	General-purpose input/output ports.
	BGRNTX			External bus release acceptance output pin (when sharing is enabled to a corresponding CS area)
35	P08_4	I/O	H	General-purpose input/output ports.
	RDX			Output pin for external bus read strobe.
36	P08_1	I/O	H	General-purpose input/output ports.
	WR1X			Output pin for external bus write strobe.
37	P08_0	I/O	H	General-purpose input/output ports.
	WR0X			Output pin for external bus write strobe.
38	P10_6	I/O	H	General-purpose input/output ports.
	MCLKE			Output pin for external bus memory clock enabled.
39	P10_5	I/O	H	General-purpose input/output ports.
	MCLKI			Input pin for external bus memory clock.
40	P10_4	I/O	H	General-purpose input/output ports.
	MCLKO			Output pin for external bus memory clock.
41	P10_3	I/O	H	General-purpose input/output ports.
	WEX			Output pin for external bus write strobe.
42	P10_2	I/O	H	General-purpose input/output ports.
	BAAX			Output pin for external bus burst access.
43	P10_1	I/O	H	General-purpose input/output ports.
	ASX			Output pin for external bus address strobe.
44	P10_0	I/O	H	General-purpose input/output ports.
	SYSCLK			Output pin for external bus clock.
49	X0	—	G	Main oscillation pin
50	X1	—	G	Main oscillation pin
52	X0A	—	G	Sub oscillation pin
53	X1A	—	G	Sub oscillation pin
56	P01_0	I/O	H	General-purpose input/output ports.
	D16			I/O pin for 16-bit external data bus.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
57	P01_1	I/O	H	General-purpose input/output ports.
	D17			I/O pin for 17-bit external data bus.
58	P01_2	I/O	H	General-purpose input/output ports.
	D18			I/O pin for 18-bit external data bus.
59	P01_3	I/O	H	General-purpose input/output ports.
	D19			I/O pin for 19-bit external data bus.
60	P01_4	I/O	H	General-purpose input/output ports.
	D20			I/O pin for 20-bit external data bus.
61	P01_5	I/O	H	General-purpose input/output ports.
	D21			I/O pin for 21-bit external data bus.
62	P01_6	I/O	H	General-purpose input/output ports.
	D22			I/O pin for 22-bit external data bus.
63	P01_7	I/O	H	General-purpose input/output ports.
	D23			I/O pin for 23-bit external data bus.
64	P00_0	I/O	H	General-purpose input/output ports.
	D24			I/O pin for 24-bit external data bus.
65	P00_1	I/O	H	General-purpose input/output ports.
	D25			I/O pin for 25-bit external data bus.
66	P00_2	I/O	H	General-purpose input/output ports.
	D26			I/O pin for 26-bit external data bus.
67	P00_3	I/O	H	General-purpose input/output ports.
	D27			I/O pin for 27-bit external data bus.
68	P00_4	I/O	H	General-purpose input/output ports.
	D28			I/O pin for 28-bit external data bus.
69	P00_5	I/O	H	General-purpose input/output ports.
	D29			I/O pin for 29-bit external data bus.
70	P00_6	I/O	H	General-purpose input/output ports.
	D30			I/O pin for 30-bit external data bus.
71	P00_7	I/O	H	General-purpose input/output ports.
	D31			I/O pin for 31-bit external data bus.
74	P07_0	I/O	H	General-purpose input/output ports.
	A00			I/O pin for 0-bit external address bus.
75	P07_1	I/O	H	General-purpose input/output ports.
	A01			I/O pin for 1-bit external address bus.

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Pin no.	Pin name	I/O	I/O circuit type*	Function
76	P07_2	I/O	H	General-purpose input/output ports.
	A02			I/O pin for 2-bit external address bus.
77	P07_3	I/O	H	General-purpose input/output ports.
	A03			I/O pin for 3-bit external address bus.
78	P07_4	I/O	H	General-purpose input/output ports.
	A04			I/O pin for 4-bit external address bus.
79	P07_5	I/O	H	General-purpose input/output ports.
	A05			I/O pin for 5-bit external address bus.
80	P07_6	I/O	H	General-purpose input/output ports.
	A06			I/O pin for 6-bit external address bus.
81	P07_7	I/O	H	General-purpose input/output ports.
	A07			I/O pin for 7-bit external address bus.
82	P06_0	I/O	H	General-purpose input/output ports.
	A08			I/O pin for 8-bit external address bus.
83	P06_1	I/O	H	General-purpose input/output ports.
	A09			I/O pin for 9-bit external address bus.
84	P06_2	I/O	H	General-purpose input/output ports.
	A10			I/O pin for 10-bit external address bus.
85	P06_3	I/O	H	General-purpose input/output ports.
	A11			I/O pin for 11-bit external address bus.
86	P06_4	I/O	H	General-purpose input/output ports.
	A12			I/O pin for 12-bit external address bus.
87	P06_5	I/O	H	General-purpose input/output ports.
	A13			I/O pin for 13-bit external address bus.
88	P06_6	I/O	H	General-purpose input/output ports.
	A14			I/O pin for 14-bit external address bus.
89	P06_7	I/O	H	General-purpose input/output ports.
	A15			I/O pin for 15-bit external address bus.
92	P05_0	I/O	H	General-purpose input/output ports.
	A16			I/O pin for 16-bit external address bus.
93	P05_1	I/O	H	General-purpose input/output ports.
	A17			I/O pin for 17-bit external address bus.
94	P05_2	I/O	H	General-purpose input/output ports.
	A18			I/O pin for 18-bit external address bus.

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Pin no.	Pin name	I/O	I/O circuit type*	Function
95	P05_3	I/O	H	General-purpose input/output ports.
	A19			I/O pin for 19-bit external address bus.
96	P05_4	I/O	H	General-purpose input/output ports.
	A20			I/O pin for 20-bit external address bus.
97	P05_5	I/O	H	General-purpose input/output ports.
	A21			I/O pin for 21-bit external address bus.
98	P05_6	I/O	H	General-purpose input/output ports.
	A22			I/O pin for 22-bit external address bus.
99	P05_7	I/O	H	General-purpose input/output ports.
	A23			I/O pin for 23-bit external address bus.
100	P18_6	I/O	H	General-purpose input/output ports.
	SCK7			Clock input/output pin of LIN-USART 7.
101	P18_5	I/O	H	General-purpose input/output ports.
	SOT7			Serial data output pin of LIN-USART 7
102	P18_4	I/O	H	General-purpose input/output ports.
	SIN7			Serial data input pin of LIN-USART 7
103	P36_5	I/O	L	General-purpose input/output ports.
	MLBDAT			Data input/output pin for MediaLB.
104	P36_6	I/O	L	General-purpose input/output ports.
	MLBSIG			Data input/output pin for MediaLB.
105	P36_7	I/O	L	General-purpose input/output ports.
	MLBCLK			Clock input pin for MediaLB.
106	P36_2	I/O	H	General-purpose input/output ports.
	WS0			Input/output pin of L/R judgement signal for I ² S.
107	P36_3	I/O	H	General-purpose input/output ports.
	SCK0			Clock input/output pin for I ² S.
110	P39_0	I/O	H	General-purpose input/output ports.
	SD0			Sound data input/output pin for I ² S ch.0.
111	P39_1	I/O	H	General-purpose input/output ports.
	SD1			Sound data input/output pin for I ² S ch.1.
112	P39_2	I/O	H	General-purpose input/output ports.
	SD2			Sound data input/output pin for I ² S ch.2.
113	P39_3	I/O	H	General-purpose input/output ports.
	SD3			Sound data input/output pin for I ² S ch.3.

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Pin no.	Pin name	I/O	I/O circuit type*	Function
114	P39_4	I/O	H	General-purpose input/output ports.
	SD4			Sound data input/output pin for I ² S ch.4.
115	P39_5	I/O	H	General-purpose input/output ports.
	SD5			Sound data input/output pin for I ² S ch.5.
116	P39_6	I/O	H	General-purpose input/output ports.
	SD6			Sound data input/output pin for I ² S ch.6.
117	P39_7	I/O	H	General-purpose input/output ports.
	SD7			Sound data input/output pin for I ² S ch.7.
118	P38_0	I/O	H	General-purpose input/output ports.
	SD8			Sound data input/output pin for I ² S ch.8.
119	P38_1	I/O	H	General-purpose input/output ports.
	SD9			Sound data input/output pin for I ² S ch.9.
120	P16_7	I/O	H	General-purpose input/output ports.
	ATGX			A/D converter external trigger input.
121	P17_4	I/O	H	General-purpose input/output ports.
	PPG4			Waveform output pin of programmable pulse generator PPG 4.
122	P17_5	I/O	H	General-purpose input/output ports.
	PPG5			Waveform output pin of programmable pulse generator PPG 5.
123	P17_6	I/O	H	General-purpose input/output ports.
	PPG6			Waveform output pin of programmable pulse generator PPG 6.
124	P17_7	I/O	H	General-purpose input/output ports.
	PPG7			Waveform output pin of programmable pulse generator PPG 7.
125	P35_0	I/O	H	General-purpose input/output ports.
	SIN8			Serial data input of LIN-USART 8.
126	P35_1	I/O	H	General-purpose input/output ports.
	SOT8			Serial data output of LIN-USART 8.
127	P35_2	I/O	H	General-purpose input/output ports.
	SCK8			Clock input/output of LIN-USART 8.
128	WDRESETX	O	J	Watchdog reset output, L Active.
130	P29_0	I/O	F	General-purpose input/output ports.
	AN0			Analog input ch.0 for A/D converter.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
131	P29_1	I/O	F	General-purpose input/output ports.
	AN1			Analog input ch.1 for A/D converter.
132	P29_2	I/O	F	General-purpose input/output ports.
	AN2			Analog input ch.2 for A/D converter.
133	P29_3	I/O	F	General-purpose input/output ports.
	AN3			Analog input ch.3 for A/D converter.
134	P29_4	I/O	F	General-purpose input/output ports.
	AN4			Analog input ch.4 for A/D converter.
135	P29_5	I/O	F	General-purpose input/output ports.
	AN5			Analog input ch.5 for A/D converter.
136	P29_6	I/O	F	General-purpose input/output ports.
	AN6			Analog input ch.6 for A/D converter.
137	P29_7	I/O	F	General-purpose input/output ports.
	AN7			Analog input ch.7 for A/D converter.
138	P28_0	I/O	F	General-purpose input/output ports.
	AN8			Analog input ch.8 for A/D converter.
139	P28_1	I/O	F	General-purpose input/output ports.
	AN9			Analog input ch.9 for A/D converter.
140	P28_2	I/O	F	General-purpose input/output ports.
	AN10			Analog input ch.10 for A/D converter.
141	P28_3	I/O	F	General-purpose input/output ports.
	AN11			Analog input ch.11 for A/D converter.
145	P40_6	I/O	C	General-purpose input/output ports.
	SDA7			Serial data input/output pin of I ² C 7.
146	P40_7	I/O	C	General-purpose input/output ports.
	SCL7			Serial clock input/output pin of I ² C 7.
147	P22_4	I/O	C	General-purpose input/output ports.
	SDA0			Serial data input/output pin of I ² C 0.
	INT14			Request input pin of external interrupt ch.14. Exclusive from P22_1.
148	P22_5	I/O	C	General-purpose input/output ports.
	SCL0			Serial clock input/output pin of I ² C 0.
149	P24_0	I/O	D	General-purpose input/output ports.
	INT0			Request input pin of external interrupt ch.0.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
150	P24_1	I/O	D	General-purpose input/output ports.
	INT1			Request input pin of external interrupt ch.1.
151	P23_0	I/O	D	General-purpose input/output ports.
	RX0			Reception input pin of CAN 0.
	INT8			Request input pin of external interrupt ch.8.
152	P23_1	I/O	D	General-purpose input/output ports.
	TX0			Transmission output pin of CAN 0.
153	P23_2	I/O	D	General-purpose input/output ports.
	RX1			Reception input pin of CAN 1.
	INT9			Request input pin of external interrupt ch.9.
154	P23_3	I/O	D	General-purpose input/output ports.
	TX1			Transmission output pin of CAN 1.
155	MD4	I	A	Mode pin 4
156	MD3	I	A	Mode pin 3
157	MD2	I	K	Mode pin 2
158	MD1	I	K	Mode pin 1
159	MD0	I	K	Mode pin 0
160	INITX	I	B	MCU reset input pin, L active doesn't change.
161	TRSTX	I	E	Tool reset input pin, L active doesn't change.
164	P21_0	I/O	D	General-purpose input/output ports.
	SIN0			Serial data input pin of LIN-USART 0.
165	P21_1	I/O	D	General-purpose input/output ports.
	SOT0			Serial data output pin of LIN-USART 0.
166	P21_2	I/O	D	General-purpose input/output ports.
	SCK0			Clock input/output pin of LIN-USART 0.
	FRCK0			Clock input pin of Free-run timer FRT0.
167	P21_4	I/O	D	General-purpose input/output ports.
	SIN1			Serial data input pin of LIN-USART 1 .
168	P21_5	I/O	D	General-purpose input/output ports.
	SOT1			Serial data output pin of LIN-USART 1.
169	P21_6	I/O	D	General-purpose input/output ports.
	SCK1			Clock input/output pin of LIN-USART 1.
	FRCK1			Clock input pin of Free-run timer FRT1.
170	P20_0	I/O	D	General-purpose input/output ports.
	SIN2			Serial data input pin of LIN-USART 2 .

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
171	P20_1	I/O	D	General-purpose input/output ports.
	SOT2			Serial data output pin of LIN-USART 2.
172	P20_2	I/O	D	General-purpose input/output ports.
	SCK2			Clock input/output pin of LIN-USART 2.
	FRCK2			Clock input pin of Free-run timer FRT2.
173	P20_4	I/O	D	General-purpose input/output ports.
	SIN3			Serial data input pin of LIN-USART 3 .
174	P20_5	I/O	D	General-purpose input/output ports.
	SOT3			Serial data output pin of LIN-USART 3.
175	P20_6	I/O	D	General-purpose input/output ports.
	SCK3			Clock input/output pin of LIN-USART 3.
	FRCK3			Clock input pin of Free-run timer FRT3.
178	P19_0	I/O	D	General-purpose input/output ports.
	SIN4			Serial data input pin of LIN-USART 4 .
179	P19_1	I/O	D	General-purpose input/output ports.
	SOT4			Serial data output pin of LIN-USART 4.
180	P19_2	I/O	D	General-purpose input/output ports.
	SCK4			Clock input/output pin of LIN-USART 4.
181	P19_4	I/O	D	General-purpose input/output ports.
	SIN5			Serial data input pin of LIN-USART 5 .
182	P19_5	I/O	D	General-purpose input/output ports.
	SOT5			Serial data output pin of LIN-USART 5.
183	P19_6	I/O	D	General-purpose input/output ports.
	SCK5			Clock input/output pin of LIN-USART 5.
184	P18_0	I/O	D	General-purpose input/output ports.
	SIN6			Serial data input pin of LIN-USART 6 .
185	P18_1	I/O	D	General-purpose input/output ports.
	SOT6			Serial data output pin of LIN-USART 6.
186	P18_2	I/O	D	General-purpose input/output ports.
	SCK6			Clock input/output pin of LIN-USART 6.
187	P15_0	I/O	D	General-purpose input/output ports.
	OCU0			Waveform output pin of output compare OCU 0.
	TOT0			Output pin of reload timer RLT 0.

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
188	P15_1	I/O	D	General-purpose input/output ports.
	OCU1			Waveform output pin of output compare OCU 1.
	TOT1			Output pin of reload timer RLT 1.
189	P15_2	I/O	D	General-purpose input/output ports.
	OCU2			Waveform output pin of output compare OCU 2.
	TOT2			Output pin of reload timer RLT 2.
190	P15_3	I/O	D	General-purpose input/output ports.
	OCU3			Waveform output pin of output compare OCU 3.
	TOT3			Output pin of reload timer RLT 3.
193	P24_6	I/O	D	General-purpose input/output ports.
	INT6			Request input pin of external interrupt ch.6.
	SDA3			Serial data input/output pin of I ² C 3.
194	P24_7	I/O	D	General-purpose input/output ports.
	INT7			Request input pin of external interrupt ch.7.
	SCL3			Serial clock input/output pin of I ² C 3.
195	P40_0	I/O	C	General-purpose input/output ports.
	SDA4			Serial data input/output pin of I ² C 4.
196	P40_1	I/O	C	General-purpose input/output ports.
	SCL4			Serial clock input/output pin of I ² C 4.
197	P40_2	I/O	C	General-purpose input/output ports.
	SDA5			Serial data input/output pin of I ² C 5.
198	P40_3	I/O	C	General-purpose input/output ports.
	SCL5			Serial clock input/output pin of I ² C 5.
199	P40_4	I/O	C	General-purpose input/output ports.
	SDA6			Serial data input/output pin of I ² C 6.
200	P40_5	I/O	C	General-purpose input/output ports.
	SCL6			Serial clock input/output pin of I ² C 6.
201	P23_4	I/O	D	General-purpose input/output ports.
	INT10			Request input pin of external interrupt ch.10.
202	P23_6	I/O	D	General-purpose input/output ports.
	INT11			Request input pin of external interrupt ch.11.
203	P22_0	I/O	D	General-purpose input/output ports.
	INT12			Request input pin of external interrupt ch.12.
204	P22_1	I/O	D	General-purpose input/output ports.
	INT14			Request input pin of external interrupt ch.14. Exclusive from P22_4.

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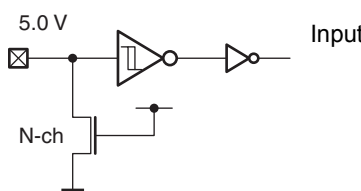
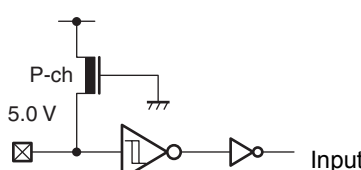
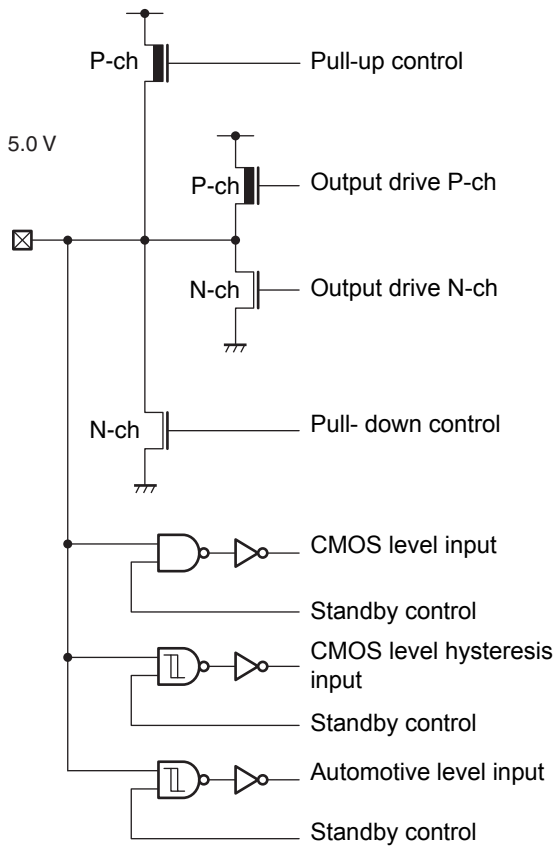
Pin no.	Pin name	I/O	I/O circuit type*	Function
205	P22_2	I/O	D	General-purpose input/output ports.
	INT13			Request input pin of external interrupt ch.13.
206	P22_3	I/O	D	General-purpose input/output ports.
	INT15			Request input pin of external interrupt ch.15. Exclusive from P22_6.
207	P14_0	I/O	D	General-purpose input/output ports.
	ICU0			Data sample input pin of Input capture ICU 0.
	TIN0			Event input pin of reload timer RLT 0.
	TRG0			Event input pin of programmable pulse generator PPG 0.
208	P14_1	I/O	D	General-purpose input/output ports.
	ICU1			Data sample input pin of Input capture ICU 1.
	TIN1			Event input pin of reload timer RLT 1.
	TRG1			Event input pin of programmable pulse generator PPG 1.
209	P14_2	I/O	D	General-purpose input/output ports.
	ICU2			Data sample input pin of input capture ICU 2.
	TIN2			Event input pin of reload timer RLT 2.
	TRG2			Event input pin of programmable pulse generator PPG 2.
210	P14_3	I/O	D	General-purpose input/output ports.
	ICU3			Data sample input pin of input capture ICU 3.
	TIN3			Event input pin of reload timer RLT 3.
	TRG3			Event input pin of programmable pulse generator PPG 3.
211	P17_0	I/O	D	General-purpose input/output ports.
	PPG0			Waveform output pin of programmable pulse generator PPG 0.
212	P17_1	I/O	D	General-purpose input/output ports.
	PPG1			Waveform output pin of programmable pulse generator PPG 1.
213	P17_2	I/O	D	General-purpose input/output ports.
	PPG2			Waveform output pin of programmable pulse generator PPG 2.
214	P17_3	I/O	D	General-purpose input/output ports.
	PPG3			Waveform output pin of programmable pulse generator PPG 3.
215	P24_2	I/O	D	General-purpose input/output ports.
	INT2			Request input pin of external interrupt ch.2.

* : For information about the I/O circuit type, refer to “4. I/O Circuit Types”.

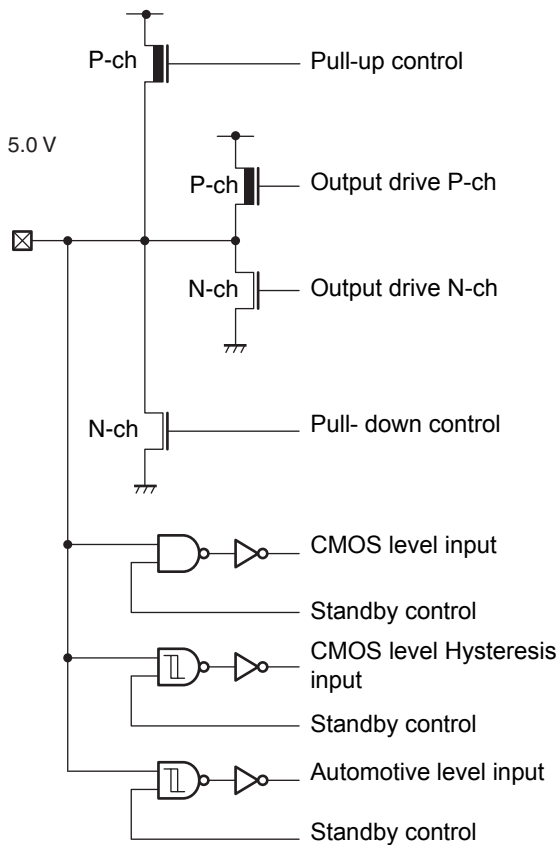
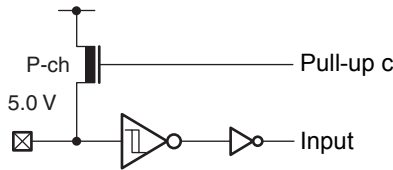
[Power supply/Ground pins]

Pin no.	Pin name	I/O	Function
1, 21, 48, 51, 55, 73, 91, 108, 129, 162, 176, 191	VSS	Supply	Ground pins
20, 45, 46, 54, 72, 90, 109	VCC3		Power supply pins for external data bus and internal regulator.
163, 177, 192, 216	VCC5		Power supply pins
143	AVCC3		Power supply pin for A/D converter
142	AVSS/AVRL		Analog ground pin, reference power supply pin for A/D converter.
144	AVRH		Reference power supply pin for A/D converter
47	C_1		Capacitor connection pin for internal regulator.
22	C_2		Capacitor connection pin for internal regulator.

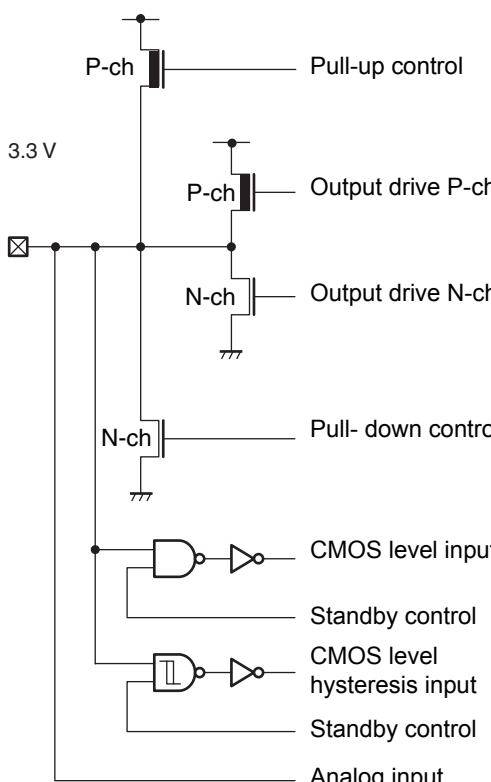
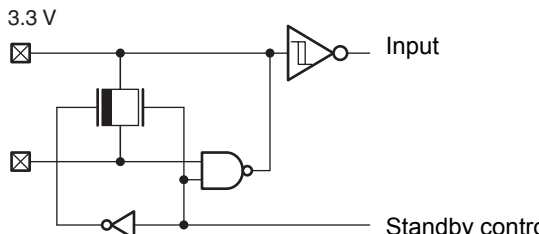
4. I/O Circuit Types

Type	Circuit	Remarks
A		• 5.0 V CMOS level hysteresis input • With Pull-down
B		• 5.0 V CMOS level hysteresis input • With Pull-up
C		• 5.0 V CMOS level output $I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$ • 5.0 V CMOS level input • 5.0 V CMOS level hysteresis input • 5.0 V Automotive level input With standby control With Pull-up/down control • Pseudo open drain when using I²C

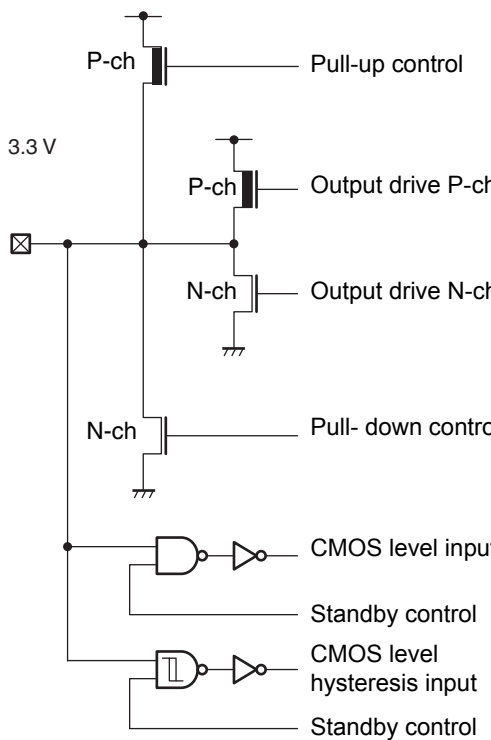
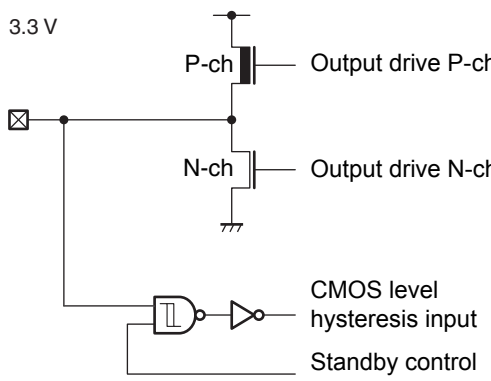
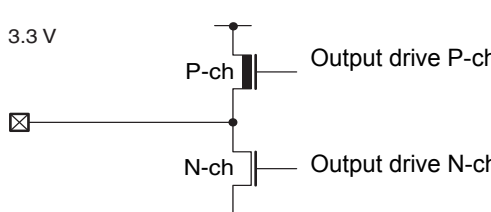
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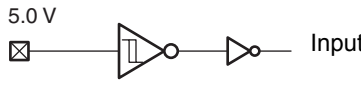
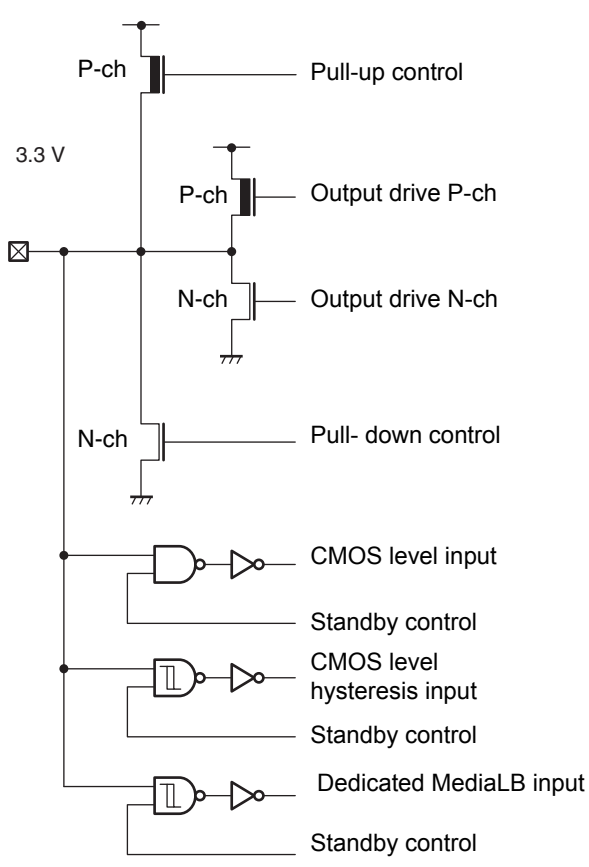
Type	Circuit	Remarks
D	 5.0 V P-ch Pull-up control P-ch Output drive P-ch N-ch Output drive N-ch N-ch Pull-down control CMOS level input Standby control CMOS level Hysteresis input Standby control Automotive level input Standby control	• 5.0 V CMOS level output $I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$ • 5.0 V CMOS level input • 5.0 V CMOS level hysteresis input • 5.0 V Automotive level input - With standby control - With Pull-up/down control
E	 5.0 V P-ch Pull-up control Input	3.3 V CMOS level hysteresis input Withstand voltage 5 V 5.0 V pull-up function (When DSU4 is unused)

(Continued)

Type	Circuit	Remarks
F	 Pull-up control Output drive P-ch Output drive N-ch Pull- down control CMOS level input Standby control CMOS level hysteresis input Standby control Analog input	• 3.3 V CMOS level output $I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$ • 3.3 V CMOS level input • 3.3 V CMOS level hysteresis input With standby control • Analog input for A/D converter
G	 Input Standby control	3.3 V Oscillation cell Feedback resistor 1 MΩ With standby control

(Continued)

Type	Circuit	Remarks
H	 3.3 V P-ch Pull-up control P-ch Output drive P-ch N-ch Output drive N-ch N-ch Pull-down control CMOS level input Standby control CMOS level hysteresis input Standby control	• 3.3 V CMOS level output $I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$ • 3.3 V CMOS level input • 3.3 V CMOS level hysteresis input With standby control With Pull-up/down control
I	 3.3 V P-ch Output drive P-ch N-ch Output drive N-ch CMOS level hysteresis input Standby control	• 3.3 V CMOS level output $I_{OL} = 8 \text{ mA}$, $I_{OH} = -8 \text{ mA}$ • 3.3 V CMOS level hysteresis input With standby control
J	 3.3 V P-ch Output drive P-ch N-ch Output drive N-ch	3.3 V CMOS level output $I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$

Type	Circuit	Remarks
K		5.0 V CMOS level hysteresis input
L		• 3.3 V CMOS level output $I_{OL} = 6 \text{ mA}$, $I_{OH} = -6 \text{ mA}$ • 3.3 V CMOS level input • 3.3 V CMOS level hysteresis input • 3.3 V MediaLB level hysteresis input - With standby control - With Pull-up/down control

5. Handling Devices

Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than V_{CC} or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rating is applied between VCC and VSS pins.

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2 K Ω or more) or enable internal pull up or pull down resistors before setting the global port enable bit.

Unused input and output pins need to leave open at the output state, or treat the same as for the input pin when they are at the input state.

Power supply pins

The MB91460M series has multiple of VCC and VSS pins.

The device is designed such that pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. However, all of these pins must be connected externally to the power supply or ground in order to minimize undesired electromagnetic radiation, prevent strobe signal malfunctions due to the rise in ground level, and conform to the total output current rating.

Moreover, connect the current supply source with the VCC and VSS pins of this device at the low impedance.

It is also recommended that a ceramic capacitor of around 0.1 μ F be connected as a bypass capacitor between the VCC and VSS pins at a location close to the device.

This series has a built-in regulator. Connect a bypass capacitor of 4.7 μ F to C_1 and C_2 pins for the regulator.

Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator (or ceramic oscillator), as well as bypass capacitors connected to ground, are placed as close together as possible. When the signal wires for transmitting from X0 and X1 pins are pulled along, use the circuit with them shielded on board. Be careful especially when a pin next to X0 pin is used.

It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation. Sub clock is also needed when dual clock product is used as single clock product.

Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

Treatment of NC and OPEN pins

Pins marked as NC and OPEN must be left open-circuit.

Mode pins (MD0 to MD4)

These pins should be connected directly to Vcc or Vss. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and Vcc or Vss on the printed circuit board as possible and connect them with low impedance.

Especially, MD3 must be directly connected to Vss with 0 Ω .

Operation at Start-up

Be sure to execute the setting initialized reset (INIT) with INITX pin immediately after start-up.

Hold the "L" level input to the INITX pin during the stabilization wait time immediately after the power on to ensure the stabilization wait time as required by the oscillator circuit (the stabilization wait time is initialized to the minimum value when INIT is asserted to reset using the INITX pin).

Note on oscillator input at power-on

At power-on, ensure that the clock is input until the oscillator stabilization wait time has elapsed.

Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

Notes on using external clock

When using an external clock, simultaneously supply the clock signal to the X1 (X1A) pin and a clock signal with the reverse phase to X0(X0A).

However, the external clock must not be used while the microcontroller is in stop mode (oscillator stop mode). The X1 pin outputs the H level and stops in STOP mode.

Setting external bus

This model guarantees the maximum frequency of 40 MHz for the external clock operation.

Setting the base clock frequency to the maximum operation frequency without changing the initial value of DIVR1 (external bus base clock division setting register) sets the external bus frequency that is not guaranteed.

Before changing the base clock frequency, set SYSCLK not to exceed the maximum guaranteed frequency.

The AC ratings cannot be guaranteed if a pull-up resistor is connected to the pin serving as an external bus pin.

Clock control

Input the "L" signal to INIT to assure the clock oscillation stabilization wait time.

Immediately after power-on or when returning from shutdown by INITX input, keep the "L" level input to the INITX pin for oscillation stabilization wait time (8ms) in order to secure stabilization wait for the built-in regulator or oscillation stabilization wait time for the oscillation circuit.

Switching multiplexed ports

Use PFR (port function register) to switch between the use as a PORT and the multiplexed port.

Low power consumption mode

■ For the standby mode, enable the synchronous standby mode (TBCR.SYNCS="1") to use and be sure to follow the sequence below.

```
LDI    #value_of_standby, R0      ; value_of_standby is write data of STCR.
LDI    #_STCR, R12                ; _STCR is address (481H) of STCR.
STB    R0, @R12                  ; Write to standby control register (STCR)
LDUB   @12, R0                    ; Read STCR for synchronous standby
LDUB   @12, R0                    ; Dummy re-read of STCR
NOP    ; NOP x 5 for arrangement of timing
NOP
NOP
NOP
NOP
NOP
```

In addition, set I flag, ILM and ICR to diverge to the interruption handler which triggers the return after returning to the standby mode.

■ Do not do the following when the monitor debugger is used.

- Break point setting for the above instruction lines
- Step execution for above instruction lines

Power-on sequence for dual-power-supply model

Notes on the power-on and power-off sequences

Power-on sequence : (1) V_{CC5} (2) V_{CC3} (3) AVR_H, AV_{CC}

Power-off sequence : (1) AVR_H, AV_{CC} (2) V_{CC3} (3) V_{CC5}

Follow the above sequence.

Turn on V_{CC3} before applying power supply to the analog power supply AV_{CC3} and AVR_H, or the analog signal.

AVR_H must not exceed voltage of AV_{CC3}.

Multiplexed pin for analog input

Input voltage must not exceed AV_{CC3} when the multiplexed pin serving for the analog input is used as a general-purpose port.

Recommended operating condition

V_{CC3} = AV_{CC3} = AVR_H : Recommended condition

Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling described below may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

- The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:
 - a user interrupt is accepted;
 - single-step execution is performed;
 - or execution breaks due to a data event or from the emulator menu.
 1. D0 and D1 flags are updated in advance.
 2. An EIT handling routine (user interrupt or emulator) is executed.
 3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).
- The following behavior occurs when an ORCCR, STILM, MOV Ri or PS instruction is executed to enable a user interrupt while that interrupt is in the active state.
 4. The PS register is updated in advance.
 5. An EIT handling routine (user interrupt) is executed.
 6. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 4.

Watchdog timer

The watchdog timer built in this model monitors a program and resets the CPU if the reset defer function is not executed within a certain period of time or the program runs out of control. Once the function of the watchdog timer is enabled, the watchdog timer keeps on operating program until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops executing the program. For those conditions to which this exception applies, see “Chapter 20 Watch dog timer in Hardware manual”.

Frequency fluctuation

This chip which contains PLL can switch divide-by-two external clock to PLL output fast clock. The clock gear function which is built in this model prevents consumption power from increasing rapidly at this time.

Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

Write to registers which include a status flag (1)

Be careful not to accidentally clear a status flag, when writing into registers which include a status flag (especially the interrupt request flag).

Take notice that a flag of a status bit is not cleared and the control bit is set to the expected value at writing.

When overwriting the control bit structured by multiple bits simultaneously, it is not possible to use the bit manipulation instruction. As a result, it is necessary to access data with usual byte/half word/word when writing to both a control bit and a status flag simultaneously. At this time, be careful not to accidentally clear other bits (bits in a status flag).

Almost all registers shown below include multiple control bits and status flags.

- TBCR
- OSCR
- TCCS0, TCCS1
- ICS01
- TMCSR0, TMCSR1, TMCSR2, TMCSR3
- PCN0, PCN1, PCN2, PCN3, PCN4, PCN5
- ADCSL0, ADCSL1

Note: It is not necessary to take special care when overwriting a single bit by the bit manipulation instruction.

Write to registers which include a status flag (2)

Take notice that actual access will be delayed when writing into registers which include a status flag (especially the interrupt request flag).

This is because data is written via multiple busses.

For example, when the program exits the interrupt routine after clearing the interrupt request flag, the interrupt flag may be cleared after accepting the RETI instructions. In this case, the interrupts may be accepted again because some of the interrupt requests are left at the time of returning from the interrupt routine.

To adjust any discord between this register address and instruction execution, read synchronous registers (RBSYNC, CBSYNC0/1, and MBSYNC) along with the area where written registers exist.

Adjustment at every writing makes a bus data band width narrow. Therefore, we recommend to adjust only if necessary. For example, when continuous writing is executed, adjustment at the last writing will be enough.

The table below shows the correspondence between a target area and a synchronous register.

Register name	Target area
RBSYNC	0x0000-0x01FF, 0x0280-0x037D, 0x0400-0x063F, 0x0C00-0x0FFF (Peripheral function on R-bus)
CBSYNC0/1	0xC000-0xFFFF (CAN on D-bus)
MBSYNC	0x6000-0x6FFF (MediaLB, I ² S and FIFO buffer on F-bus)

6. Notes On Debugger

Execution of the RETI Command

If an interrupt occurs frequently during step execution, the corresponding interrupt handling routine is executed repeatedly after step execution. As the result of that, the main routine and low-interrupt-level programs will not be executed.

Do not perform the step execution of RETI instruction to prevent this issue.

Disable the corresponding interrupt and execute debugger when the corresponding interrupt routine no longer needs debugging.

Operand break

Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

Flash security

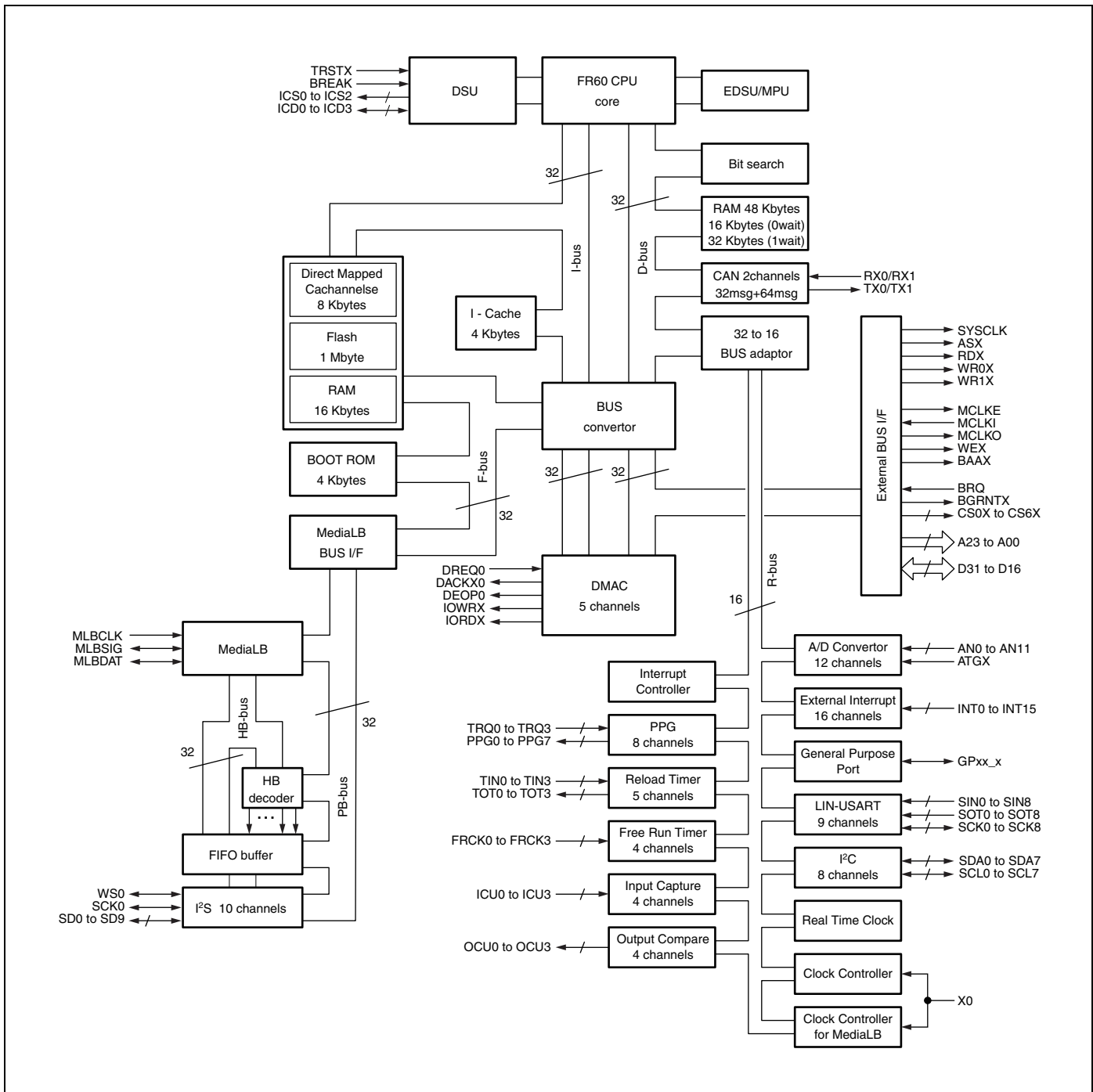
DSU4 will not be available due to security issues when Flash security is used.

Shutdown mode

It is impossible to execute debugger in the shutdown mode.

7. Block Diagram

MB91F467MA



■ CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

7.1 Features

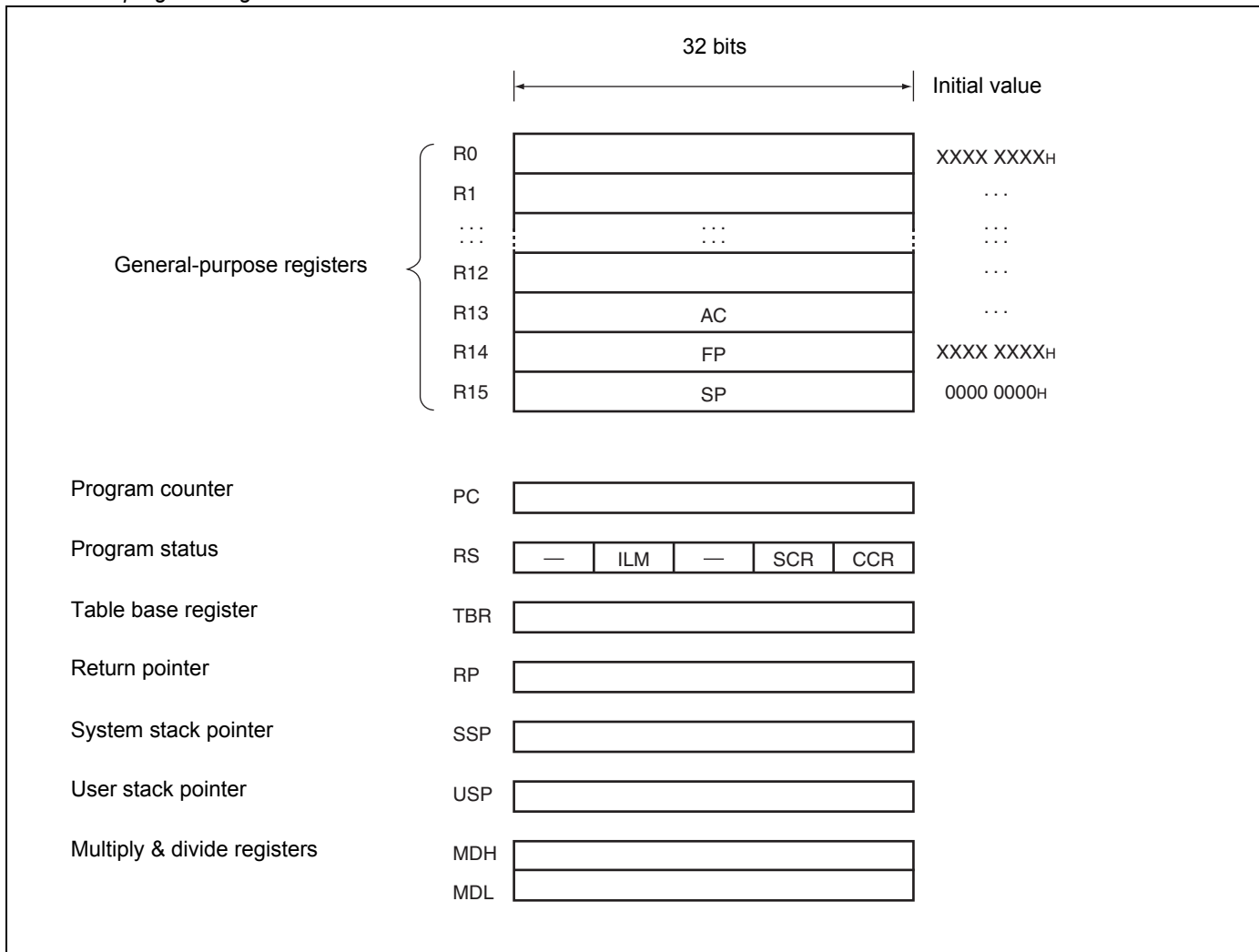
- Adoption of RISC architecture
Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
32-bit × 32-bit multiplication: 5 cycles
16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
Quick response speed (6 cycles)
Multiple-interrupt support
Level mask function (16 levels)
- Enhanced instructions for I/O operation
Memory-to-memory transfer instruction
Bit processing instruction
Basic instruction word length: 16 bits
- Low-power consumption
Sleep mode/stop mode

7.2 Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

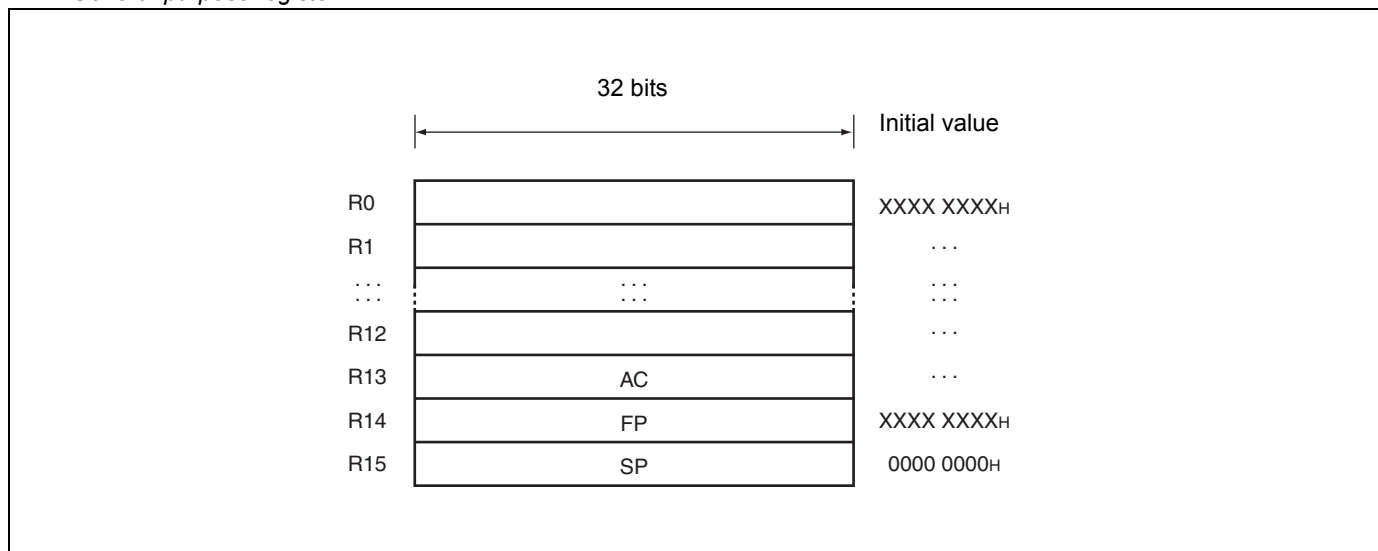
7.3 Programming model

7.3.1 Basic programming model



7.4 Registers

7.4.1 General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

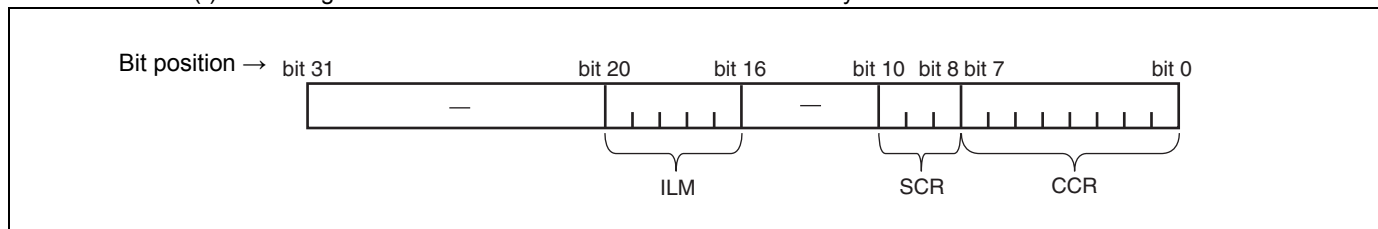
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

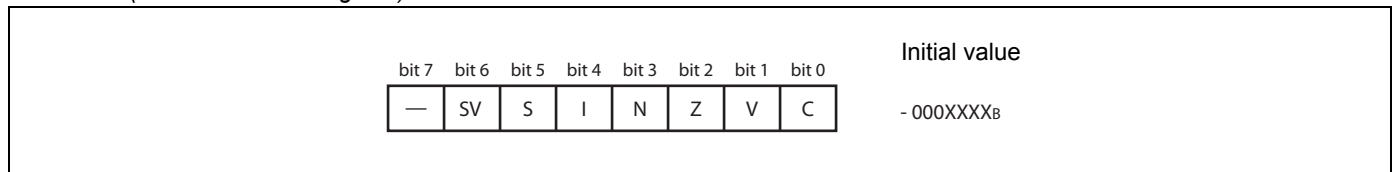
7.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.



7.4.3 CCR (Condition Code Register)



SV : Supervisor flag

S : Stack flag

I : Interrupt enable flag

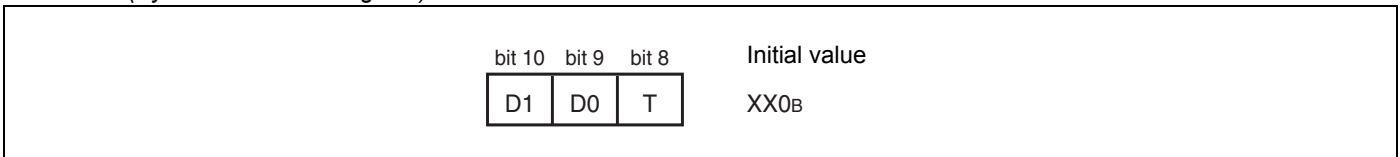
N : Negative enable flag

Z : Zero flag

V : Overflow flag

C : Carry flag

7.4.4 SCR (System Condition Register)



Flag for step division (D1, D0)

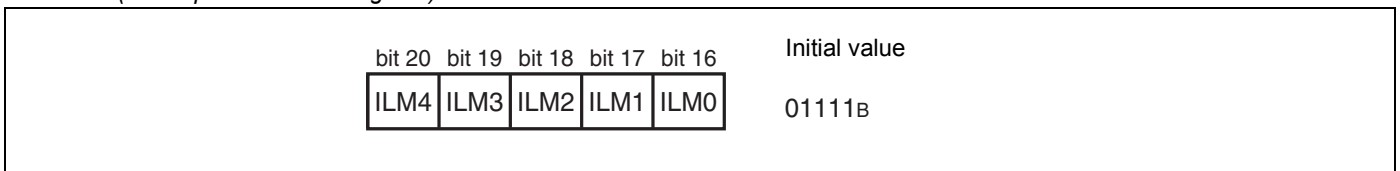
This flag stores interim data during execution of step division.

Step trace trap flag (T)

This flag indicates whether the step trace trap is enabled or disabled.

The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

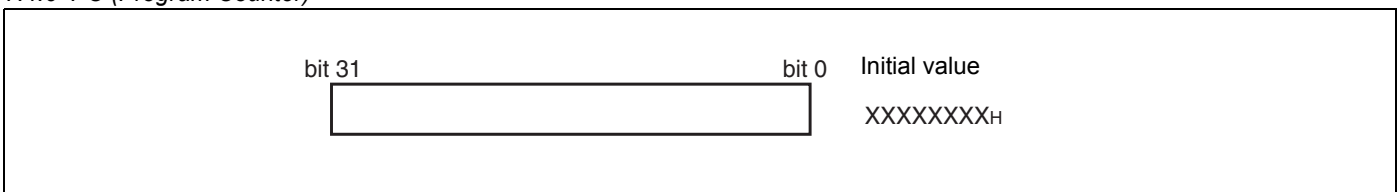
7.4.5 ILM (Interrupt Level Mask register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value "01111_B" at reset.

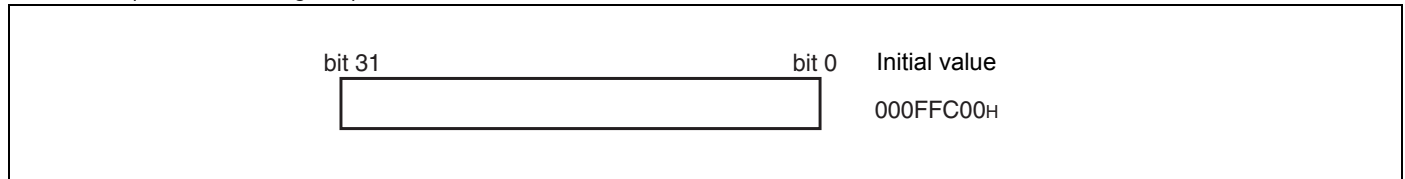
7.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

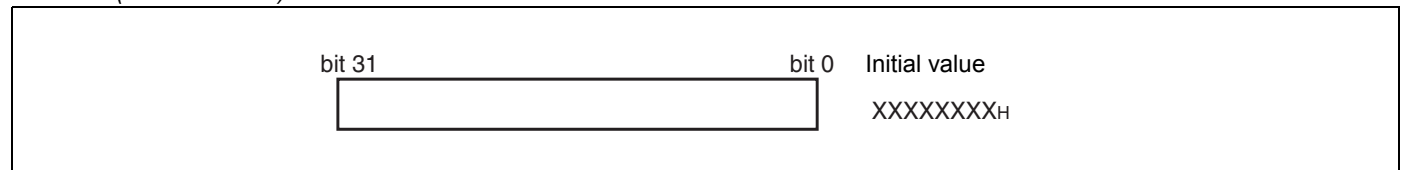
The initial value at reset is undefined.

7.4.7 TBR (Table Base Register)



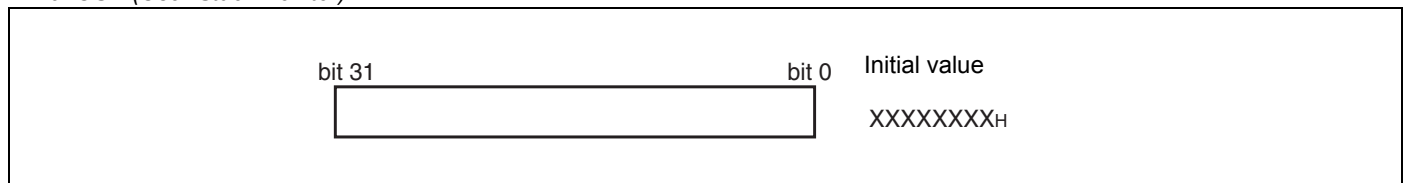
The table base register stores the starting address of the vector table used in EIT processing.
The initial value at reset is 000FFC00_H.

7.4.8 RP (Return Pointer)



The return pointer stores the address for return from subroutines.
During execution of a CALL instruction, the PC value is transferred to this RP register.
During execution of a RET instruction, the contents of the RP register are transferred to PC.
The initial value at reset is undefined.

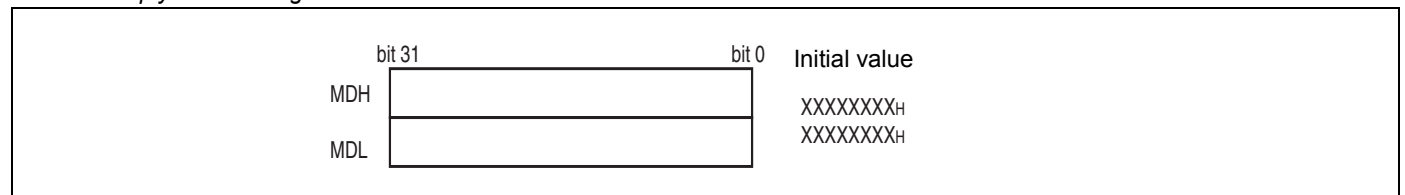
7.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is "1", this register functions as the R15 register.

- The USP register can also be explicitly specified.
The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

7.4.10 Multiply & divide registers



These registers are for multiplication and division, and are 32 bits each in length.
The initial value at reset is undefined.

8. Embedded Program/Data Memory (Flash)

8.1 Flash features

- MB91F467MA: 1088 Kbytes (16×64 Kbytes + 8×8 Kbytes = 8.7 Mbits)
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0014:8000_H to 0014:800F_H
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

8.2 Operation modes

1. 64-bit CPU mode
 - CPU reads and executes programs in word (32-bit) length units.
 - Flash writing is not possible.
 - Actual Flash Memory access is performed in d-word (64-bit) length units.
2. 32-bit CPU mode :
 - Actual Flash Memory access is performed in word (32-bit) length units.
3. 16-bit CPU mode :
 - CPU reads and writes in half-word (16-bit) length units.
 - Program execution from the Flash is not possible.
 - Actual Flash Memory access is performed in half-word (16-bit) length units.

8.3 Flash access in CPU mode

8.3.1 Flash configuration

Flash memory map MB91F467MA

Address									
0014:FFFF _H 0014:C000 _H	SA6 (8kB)				SA7 (8kB)				ROMS7
0014:BFFF _H 0014:8000 _H	SA4 (8kB)				SA5 (8kB)				
0014:7FFF _H 0014:4000 _H	SA2 (8kB)				SA3 (8kB)				
0014:3FFF _H 0014:0000 _H	SA0 (8kB)				SA1 (8kB)				
0013:FFFF _H 0012:0000 _H	SA22 (64kB)				SA23 (64kB)				ROMS6
0011:FFFF _H 0010:0000 _H	SA20 (64kB)				SA21 (64kB)				
000F:FFFF _H 000E:0000 _H	SA18 (64kB)				SA19 (64kB)				ROMS5
000D:FFFF _H 000C:0000 _H	SA16 (64kB)				SA17 (64kB)				ROMS4
000B:FFFF _H 000A:0000 _H	SA14 (64kB)				SA15 (64kB)				ROMS3
0009:FFFF _H 0008:0000 _H	SA12 (64kB)				SA13 (64kB)				ROMS2
0007:FFFF _H 0006:0000 _H	SA10 (64kB)				SA11 (64kB)				ROMS1
0005:FFFF _H 0004:0000 _H	SA8 (64kB)				SA9 (64kB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

8.3.2 Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 80 MHz	1	1	3	-	4	

Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	-	-	0	4	
to 48 MHz	1	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 80 MHz	1	-	-	0	7	

8.3.3 Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

Notes: • Address mapping MB91F467MA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:0000 _H to 14:FFFF _H	addr[2]=0	SA0, SA2, SA4, SA6 (8 Kbyte)	$FA = \text{addr} - \text{addr}\%00:4000_{\text{H}} + (\text{addr}\%00:4000_{\text{H}})/2 - (\text{addr}/2)\%4 + \text{addr}\%4 - 05:0000_{\text{H}}$
14:0000 _H to 14:FFFF _H	addr[2]=1	SA1, SA3, SA5, SA7 (8 Kbyte)	$FA = \text{addr} - \text{addr}\%00:4000_{\text{H}} + (\text{addr}\%00:4000_{\text{H}})/2 - (\text{addr}/2)\%4 + \text{addr}\%4 - 05:0000_{\text{H}} + 00:2000_{\text{H}}$
04:0000 _H to 13:FFFF _H	addr[2]=0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	$FA = \text{addr} - \text{addr}\%02:0000_{\text{H}} + (\text{addr}\%02:0000_{\text{H}})/2 - (\text{addr}/2)\%4 + \text{addr}\%4 + 0C:0000_{\text{H}}$
04:0000 _H to 13:FFFF _H	addr[2]=1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	$FA = \text{addr} - \text{addr}\%02:0000_{\text{H}} + (\text{addr}\%02:0000_{\text{H}})/2 - (\text{addr}/2)\%4 + \text{addr}\%4 + 0C:0000_{\text{H}} + 01:0000_{\text{H}}$

Notes: • FA result is without 20:0000_H offset for parallel Flash programming.

Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

- addr[2] is the value of the third lower bit when CPU address (addr) is described by binary numbers.
- FA[21] is the value of the twenty second lower bit when the flash address (FA) is described by binary numbers.
- “%” represents remainder. For example, “addr%00:4000_H” is the remainder after addr is divided by 4000_H.

8.4 Parallel Flash programming mode

8.4.1 Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F467MA

FA[21:0]	
003F:FFFF _H 003F:0000 _H	SA23 (64kB)
003E:FFFF _H 003E:0000 _H	SA22 (64kB)
003D:FFFF _H 003D:0000 _H	SA21 (64kB)
003C:FFFF _H 003C:0000 _H	SA20 (64kB)
003B:FFFF _H 003B:0000 _H	SA19 (64kB)
003A:FFFF _H 003A:0000 _H	SA18 (64kB)
0039:FFFF _H 0039:0000 _H	SA17 (64kB)
0038:FFFF _H 0038:0000 _H	SA16 (64kB)
0037:FFFF _H 0037:0000 _H	SA15 (64kB)
0036:FFFF _H 0036:0000 _H	SA14 (64kB)
0035:FFFF _H 0035:0000 _H	SA13 (64kB)
0034:FFFF _H 0034:0000 _H	SA12 (64kB)
0033:FFFF _H 0033:0000 _H	SA11 (64kB)
0032:FFFF _H 0032:0000 _H	SA10 (64kB)
0031:FFFF _H 0031:0000 _H	SA9 (64kB)
0030:FFFF _H 0030:0000 _H	SA8 (64kB)
002F:FFFF _H 002F:E000 _H	SA7 (8kB)
002F:DFFF _H 002F:C000 _H	SA6 (8kB)
002F:BFFF _H 002F:A000 _H	SA5 (8kB)
002F:9FFF _H 002F:8000 _H	SA4 (8kB)
002F:7FFF _H 002F:6000 _H	SA3 (8kB)
002F:5FFF _H 002F:4000 _H	SA2 (8kB)
002F:3FFF _H 002F:2000 _H	SA1 (8kB)
002F:1FFF _H 002F:0000 _H	SA0 (8kB)
	FA[1:0]=00
	FA[1:0]=10
16bit write mode	DQ[15:0]
	DQ[15:0]

Note: Always keep FA[0] = 0 and FA[21] = 1.

8.4.2 Pin connections in parallel programming mode

Resetting after setting the MD[4:0] pins to [00111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to general purpose ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	CPU mode	Flash memory mode	Normal function	Pin number
—	INITX	—	INITX	160
RESET	—	FRSTX	P13_2	19
—	—	MD2	MD2	157
—	—	MD1	MD1	156
—	—	MD0	MD0	155
RY/BY	FMCS:RDY	RY/BYX	P09_4	25
BYTE	"H"fixed	BYTEX	P13_1	18
WE	Internal bus control	WEX	P09_3	26
OE		OEX	P09_2	27
CE		CEX	P09_1	28
A-1	Internal address	FA0	P17_4	121
A0 to A7		FA1 to FA8	P17_5 to P17_7 P29_0 to P29_4	122 to 124 130 to 134
A8 to A15		FA9 to FA16	P29_5 to P29_7 P28_0 to P28_3 P16_3	135 to 141 10
A16 to A19		FA17 to FA21	P16_4 to P16_6 P22_4, P22_5	9 to 7 147, 148
DQ0 to DQ7	Internal data	DQ0 to DQ7	P36_2, P36_3 P39_0 to P39_5	106, 107 110 to 115
DQ8 to DQ15		DQ8 to DQ15	P39_6, P39_7 P38_0, P38_1 P16_7 P35_0 to P35_2	116 to 120 125 to 127

9. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : 000_H to 0FF_H

Half word access : 000_H to 1FF_H

Word data access : 000_H to 3FF_H

10. Memory Map

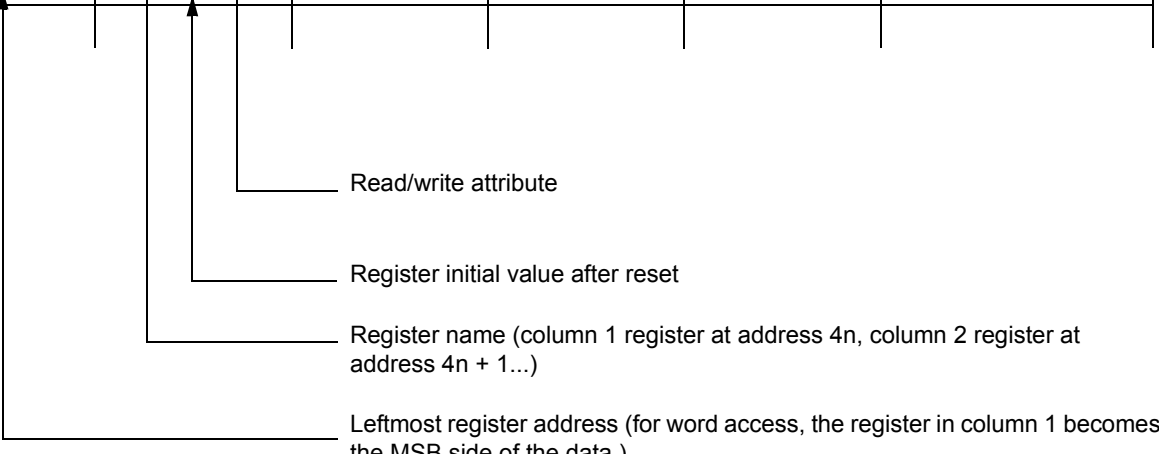
MB91F467M

MB91F467M	
0000:0000 _H	I/O (byte)
0000:00FF _H 0000:0100 _H	I/O (Half Word)
0000:01FF _H 0000:0200 _H	I/O (Word)
0000:03FF _H 0000:0400 _H	I/O
0000:0FFF _H 0000:1000 _H	DMA
0000:10FF _H 0000:1100 _H	reserved
0000:1FFF _H 0000:2000 _H	reserved
0000:3FFF _H 0000:4000 _H	I-cache or I-RAM (8 Kbytes)
0000:5FFF _H 0000:6000 _H	MediaLB & I ² S
0000:6FFF _H 0000:7000 _H	Flash control Flash I-cache
0000:70FF _H 0000:7100 _H	reserved
0000:AFFF _H 0000:B000 _H	Boot ROM (4 Kbytes)
0000:BFFF _H 0000:C000 _H	CAN
0000:CFFF _H 0000:D000 _H	reserved
0000:FFFF _H 0001:0000 _H	ExtBUS I-cache or I-RAM (4 Kbytes)
0001:FFFF _H 0002:0000 _H	reserved
0002:3FFF _H 0002:4000 _H	D-RAM (1wait) (32 Kbytes)
0002:BFFF _H 0002:C000 _H	D-RAM (No wait) (16 Kbytes)
0002:FFFF _H 0003:0000 _H	I/D-RAM (16 Kbytes)
0003:3FFF _H 0003:4000 _H	reserved
0003:FFFF _H 0004:0000 _H	Flash (1088 Kbytes) or External BUS (depends on ROMA/ROMS)
0014:FFFF _H 0015:0000 _H	External BUS
FFFF:FFFF _H	

11. I/O Map

1. MB91F467M

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:

“ 1 ” : Initial value “ 1 ”

“ 0 ” : Initial value “ 0 ”

“ X ” : Initial value “ undefined ”

“ - ” : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved		Port Data Register [R-bus]
000004 _H	Reserved	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008 _H	PDR08 [R/W] XXXX--XX	PDR09 [R/W] -XXXXXXXX	PDR10 [R/W] -XXXXXXXX	PDR11 [R/W] -----XX	
00000C _H	Reserved	PDR13 [R/W] -----XXX	PDR14 [R/W] ----XXXX	PDR15 [R/W] XX--XXXX	
000010 _H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] -XXX-XXX	PDR19 [R/W] -XXX-XXX	
000014 _H	PDR20 [R/W] -XXX-XXX	PDR21 [R/W] -XXX-XXX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] -X-XXXXX	
000018 _H	PDR24 [R/W] XXXXXXXX	Reserved			
00001C _H	PDR28 [R/W] ----XXXX	PDR29 [R/W] XXXXXXXX	Reserved		
000020 _H	Reserved			PDR35 [R/W] -----XXX	
000024 _H	PDR36 [R/W] XXX-XX--	Reserved	PDR38 [R/W] -----XX	PDR39 [R/W] XXXXXXXX	
000028 _H	PDR40 [R/W] XXXXXXXX	Reserved			
00002C _H	Reserved				Reserved
000030 _H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt
000034 _H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		
000038 _H	DICR [R/W] -----0	HRCL [R/W] 0--11111	RBSYNC [R] XXXXXXXX XXXXXXXX		Delay Interrupt I-unit
00003C _H	Reserved				Reserved
000040 _H	SCR00 [R/W, W] 00000000	SMR00 [R/W, W] 00000000	SSR00 [R/W, R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044 _H	ESCR00 [R/W] 00000X00	ECCR00 [R/W, R, W] -00000XX	Reserved		
000048 _H	SCR01 [R/W, W] 00000000	SMR01 [R/W, W] 00000000	SSR01 [R/W, R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
00004C _H	ESCR01 [R/W] 00000X00	ECCR01 [R/W, R, W] -00000XX	Reserved		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000050 _H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054 _H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	Reserved		
000058 _H	SCR03 [R/W, W] 00000000	SMR03 [R/W, W] 00000000	SSR03 [R/W, R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
00005C _H	ESCR03 [R/W] 00000X00	ECCR03 [R/W, R, W] -00000XX	Reserved		
000060 _H	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064 _H	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [R] ---00000	FCR04 [R/W] 0001-000	
000068 _H	SCR05 [R/W, W] 00000000	SMR05 [R/W, W] 00000000	SSR05 [R/W, R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
00006C _H	ESCR05 [R/W] 00000X00	ECCR05 [R/W, R, W] -00000XX	FSR05 [R] ---00000	FCR05 [R/W] 0001-000	
000070 _H	SCR06 [R/W, W] 00000000	SMR06 [R/W, W] 00000000	SSR06 [R/W, R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074 _H	ESCR06 [R/W] 00000X00	ECCR06 [R/W, R, W] -00000XX	FSR06 [R] ---00000	FCR06 [R/W] 0001-000	
000078 _H	SCR07 [R/W, W] 00000000	SMR07 [R/W, W] 00000000	SSR07 [R/W, R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
00007C _H	ESCR07 [R/W] 00000X00	ECCR07 [R/W, R, W] -00000XX	FSR07 [R] ---00000	FCR07 [R/W] 0001-000	
000080 _H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baud rate Generator LIN-USART 0 to 7
000084 _H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088 _H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
00008C _H	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000090 _H to 0000CC _H	Reserved				Reserved
0000D0 _H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] -----00	ITBAL0 [R/W] 00000000	I ² C 0
0000D4 _H	ITMKH0 [R/W] 00----11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] -0000000	
0000D8 _H	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] -0011111	Reserved	
0000DC _H	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] -----00	ITBAL1 [R/W] 00000000	I ² C 1
0000E0 _H	ITMKH1 [R/W] 00----11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] -0000000	
0000E4 _H	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] -0011111	Reserved	
0000E8 _H to 0000FC _H	Reserved				Reserved
000100 _H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] ----0000	PPG Control 0-3
000104 _H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] ----0000	PPG Control 4-7
000108 _H , 00010C _H	Reserved				Reserved
000110 _H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114 _H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000-	PCNL00 [R/W] 000000-0	
000118 _H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
00011C _H	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000-	PCNL01 [R/W] 000000-0	
000120 _H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124 _H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000-	PCNL02 [R/W] 000000-0	
000128 _H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
00012C _H	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000-	PCNL03 [R/W] 000000-0	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000130 _H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134 _H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000-	PCNL04 [R/W] 000000-0	
000138 _H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013C _H	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000-	PCNL05 [R/W] 000000-0	
000140 _H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144 _H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000-	PCNL06 [R/W] 000000-0	
000148 _H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014C _H	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000-	PCNL07 [R/W] 000000-0	
000150 _H to 00017C _H	Reserved				Reserved
000180 _H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184 _H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188 _H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
00018C _H	OCS01 [R/W] ---0--00 0000--00		OCS23 [R/W] ---0--00 0000--00		Input Capture 0 to 3
000190 _H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194 _H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198 _H , 00019C _H	Reserved				Reserved
0001A0 _H	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4 _H	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8 _H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] ---00000	ADECH [R/W] ---00000	
0001AC _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001B0 _H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG0, PPG1)
0001B4 _H	Reserved		TMCSRH0 [R/W] ---00000	TMCSRL0 [R/W] 0-000000	
0001B8 _H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG2, PPG3)
0001BC _H	Reserved		TMCSRH1 [R/W] ---00000	TMCSRL1 [R/W] 0-000000	
0001C0 _H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG4, PPG5)
0001C4 _H	Reserved		TMCSRH2 [R/W] ---00000	TMCSRL2 [R/W] 0-000000	
0001C8 _H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG6, PPG7)
0001CC _H	Reserved		TMCSRH3 [R/W] ---00000	TMCSRL3 [R/W] 0-000000	
0001D0 _H to 0001E4 _H	Reserved				Reserved
0001E8 _H	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (A/D Converter)
0001EC _H	Reserved		TMCSRH7 [R/W] ---00000	TMCSRL7 [R/W] 0-000000	
0001F0 _H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free-run Timer 0 (ICU0, ICU1)
0001F4 _H	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free-run Timer 1 (ICU2, ICU3)
0001F8 _H	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free-run Timer 2 (OCU0, OCU1)
0001FC _H	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free-run Timer 3 (OCU2, OCU3)
000200 _H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208 _H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C _H	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000210 _H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000214 _H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 _H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220 _H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224 _H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228 _H to 00023C _H	Reserved				
000240 _H	DMACR [R/W] 0--00000	Reserved			Reserved
000244 _H to 00027C _H	Reserved				
000280 _H	SCR08 [R/W, W] 00000000	SMR08 [R/W, W] 00000000	SSR08 [R/W, R] 00001000	RDR08/TDR08 [R/W] 00000000	
000284 _H	ESCR08 [R/W] 00000X00	ECCR08 [R/W, R, W] 000000XX	Reserved		
000288 _H to 0002BC _H	Reserved				Reserved
0002C0 _H	BGR108 [R/W] 00000000	BGR008 [R/W] 00000000	Reserved		Baud rate Generator LIN-USART8
0002C4 _H to 000364 _H	Reserved				Reserved
000368 _H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] -----00	ITBAL2 [R/W] 00000000	I ² C 2
00036C _H	ITMKH2 [R/W] 00----11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] -0000000	
000370 _H	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] -0011111	Reserved	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000374 _H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] -----00	ITBAL3 [R/W] 00000000	I ² C 3
000378 _H	ITMKH3 [R/W] 00----11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] -00000000	
00037C _H	Reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] -00111111	Reserved	
000380 _H	IBCR4 [R/W] 00000000	IBSR4 [R] 00000000	ITBAH4 [R/W] -----00	ITBAL4 [R/W] 00000000	I ² C 4
000384 _H	ITMKH4 [R/W] 00----11	ITMKL4 [R/W] 11111111	ISMK4 [R/W] 01111111	ISBA4 [R/W] -00000000	
000388 _H	Reserved	IDAR4 [R/W] 00000000	ICCR4 [R/W] -00111111	Reserved	
00038C _H	Reserved				Reserved
000390 _H	ROMS [R] 11111111 00000000		Reserved		ROM Select Register
000394 _H	IBCR5 [R/W] 00000000	IBSR5 [R] 00000000	ITBAH5 [R/W] -----00	ITBAL5 [R/W] 00000000	I ² C 5
000398 _H	ITMKH5 [R/W] 00----11	ITMKL5 [R/W] 11111111	ISMK5 [R/W] 01111111	ISBA5 [R/W] -00000000	
00039C _H	Reserved	IDAR5 [R/W] 00000000	ICCR5 [R/W] -00111111	Reserved	
0003A0 _H	IBCR6 [R/W] 00000000	IBSR6 [R] 00000000	ITBAH6 [R/W] -----00	ITBAL6 [R/W] 00000000	I ² C 6
0003A4 _H	ITMKH6 [R/W] 00----11	ITMKL6 [R/W] 11111111	ISMK6 [R/W] 01111111	ISBA6 [R/W] -00000000	
0003A8 _H	Reserved	IDAR6 [R/W] 00000000	ICCR6 [R/W] -00111111	Reserved	
0003AC _H	IBCR7 [R/W] 00000000	IBSR7 [R] 00000000	ITBAH7 [R/W] -----00	ITBAL7 [R/W] 00000000	I ² C 7
0003B0 _H	ITMKH7 [R/W] 00----11	ITMKL7 [R/W] 11111111	ISMK7 [R/W] 01111111	ISBA7 [R/W] -00000000	
0003B4 _H	Reserved	IDAR7 [R/W] 00000000	ICCR7 [R/W] -00111111	Reserved	
0003B8 _H to 0003C0 _H	Reserved				Reserved
0003C4 _H	Reserved			ISIZE [R/W] -----10	I-Cache

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0003C8 _H to 0003E0 _H	Reserved				Reserved
0003E4 _H	Reserved			ICHCR [R/W] 0-000000	I-Cache
0003E8 _H , 0003EC _H	Reserved				Reserved
0003F0 _H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search
0003F4 _H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H to 00043C _H	Reserved				Reserved
000440 _H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444 _H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448 _H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	Reserved	ICR11 [R/W] ---11111	
00044C _H	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	Reserved		
000450 _H	ICR16 [R/W] ---11111	Reserved		ICR19 [R/W] ---11111	
000454 _H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458 _H	Reserved	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045C _H	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460 _H	Reserved	ICR33 [R/W] ---11111	Reserved		
000464 _H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000468 _H	Reserved		ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	Interrupt Control Unit
00046C _H	Reserved				
000470 _H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474 _H	Reserved				
000478 _H	Reserved		ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
00047C _H	Reserved	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480 _H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX-00	CTBR [W] XXXXXXXXXX	Clock Control Unit
000484 _H	CLKR [R/W] ----0000	WPR [W] XXXXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488 _H	Reserved				
00048C _H	PLLDIVM [R/W] ----0000	PLLDIVN [R/W] --000000	PLLDIVG [R/W] ----0000	PLLMULG [R/W] 00000000	PLL Clock Gear Unit
000490 _H	PLLCTRL [R/W] ----0000	Reserved			
000494 _H	Reserved				Reserved
000498 _H	PORTEN [R/W] -----00	Reserved			Port Input Enable Control
00049C _H	Reserved				Reserved
0004A0 _H	Reserved	WTCER [R/W] -----00	WTCR [R/W] 00000000 000-00-X		Real Time Clock (Watch Timer)
0004A4 _H	Reserved	WTBR [R/W] ---XXXXX XXXXXXXXXX XXXXXXXXX			
0004A8 _H	WTHR [R/W] ---00000	WTMR [R/W] --000000	WTSR [R/W] --000000	Reserved	
0004AC _H	Reserved		CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock Monitor
0004B0 _H	CUCR [R/W] ----- 0--00		CUTD [R/W] 10000000 00000000		Sub-Oscillation Calibration Unit
0004B4 _H	CUTR1 [R] ----- 00000000		CUTR2 [R] 00000000 00000000		
0004B8 _H	CMPR [R/W] --000010 11111101		Reserved	CMCR [R/W] -001--00	Clock Modulator
0004BC _H	CMT1 [R/W] 00000000 1---0000		CMT2 [R/W] --000000 --000000		
0004C0 _H	CANPRE [R/W] 00000000	Reserved			CAN Clock Control

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0004C4 _H	Reserved		HWWDE [R/W] -----00	HWWD [R/W] 00011000	Hardware-Watchdog
0004C8 _H	OSCRH [R/W] 000--001	Reserved	WPCRH [R/W] 000--001	Reserved	Main-/Sub-Oscillation Stabilization Timer
0004CC _H	OSCCR [R/W] -----00	Reserved			Main- Oscillation Standby Control
0004D0 _H	Reserved				
0004D4 _H	SHDE [R/W] 0-----	Reserved	EXTE [R/W] 00000000	EXTF [R/W] 00000000	Shutdown control
0004D8 _H	EXTLV [R/W] 00000000 00000000		Reserved		
0004DC _H to 0004E4 _H	Reserved				Reserved
0004E8 _H	Reserved		MLBCNT [R/W] 000----0	MLBPRES [R/W] --000000	MediaLB Clock Control
0004EC _H , 0004F0 _H	Reserved				Reserved
0004F4 _H	MPLLDIVM [R/W] ----0000	MPLLDIVN [R/W] --000000	MPLLDIVG [R/W] ----0000	MPLLMULG [R/W] 00000000	MediaLB PLL Clock Gear Unit
0004F8 _H	MPLLCTRL [R/W] ----0000	Reserved			
0004FC _H to 00063C _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000640 _H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000*1		External bus Unit
000644 _H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648 _H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064C _H	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650 _H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654 _H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658 _H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065C _H	Reserved				
000660 _H	AWR0 [R/W] 01001111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664 _H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668 _H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066C _H	AWR6 [R/W] XXXXXXXX XXXXXXXX		Reserved		
000670 _H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674 _H	Reserved				
000678 _H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
00067C _H	Reserved				
000680 _H	CSER [R/W] -0000001	CHER [R/W] -1111111	Reserved	TCR [R/W] 0000**** *2	
000684 _H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688 _H to 0007F8 _H	Reserved				
0007FC _H	Reserved	MODR [W] XXXXXXXX	Reserved		Mode register
000800 _H to 000CFC _H	Reserved				Reserved

*1 : ACR0 [11:10] depends on the mode vector fetch information of bus width.

*2 : TCR [3:0] INIT value = 0000, and keeps the value after RST.

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D00 _H	PDRD00 [R] XXXXXXXXXX	PDRD01 [R] XXXXXXXXXX	Reserved		Port Data Direct Read Register [R-bus]
000D04 _H	Reserved	PDRD05 [R] XXXXXXXXXX	PDRD06 [R] XXXXXXXXXX	PDRD07 [R] XXXXXXXXXX	
000D08 _H	PDRD08 [R] XXXX--XX	PDRD09 [R] -XXXXXXXXX	PDRD10 [R] -XXXXXXXXX	PDRD11 [R] -----XX	
000D0C _H	Reserved	PDRD13 [R] ----XXX	PDRD14 [R] ----XXXX	PDRD15 [R] XX--XXXX	
000D10 _H	PDRD16 [R] XXXXXXXXXX	PDRD17 [R] XXXXXXXXXX	PDRD18 [R] -XXX-XXX	PDRD19 [R] -XXX-XXX	
000D14 _H	PDRD20 [R] -XXX-XXX	PDRD21 [R] -XXX-XXX	PDRD22 [R] XXXXXXXXXX	PDRD23 [R] -X-XXXXX	
000D18 _H	PDRD24 [R] XXXXXXXXXX	Reserved			
000D1C _H	PDRD28 [R] ----XXXX	PDRD29 [R] XXXXXXXXXX	Reserved		
000D20 _H	Reserved			PDRD35 [R] ----XXX	
000D24 _H	PDRD36 [R] XXX-XX--	Reserved	PDRD38 [R] -----XX	PDRD39 [R] XXXXXXXXXX	
000D28 _H	PDRD40 [R] XXXXXXXXXX	Reserved			
000D2C _H to 000D3C _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D40 _H	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		Port Direction Register [R-bus]
000D44 _H	Reserved	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48 _H	DDR08 [R/W] 0000--00	DDR09 [R/W] -0000000	DDR10 [R/W] -0000000	DDR11 [R/W] -----00	
000D4C _H	Reserved	DDR13 [R/W] -----000	DDR14 [R/W] ----0000	DDR15 [R/W] 00--0000	
000D50 _H	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] -000-000	DDR19 [R/W] -000-000	
000D54 _H	DDR20 [R/W] -000-000	DDR21 [R/W] -000-000	DDR22 [R/W] 00000000	DDR23 [R/W] -0-00000	
000D58 _H	DDR24 [R/W] 00000000	Reserved			
000D5C _H	DDR28 [R/W] ----0000	DDR29 [R/W] 00000000	Reserved		
000D60 _H	Reserved			DDR35 [R/W] -----000	
000D64 _H	DDR36 [R/W] 000-00--	Reserved	DDR38 [R/W] -----00	DDR39 [R/W] 00000000	
000D68 _H	DDR40 [R/W] 00000000	Reserved			
000D6C _H to 000D7C _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D80 _H	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		Port Function Register [R-bus]
000D84 _H	Reserved	PFR05 [R/W] 11111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
000D88 _H	PFR08 [R/W] 1111--11	PFR09 [R/W] -1111111	PFR10 [R/W] -1111111	PFR11 [R/W] -----00	
000D8C _H	Reserved	PFR13 [R/W] ----000	PFR14 [R/W] ----0000	PFR15 [R/W] 00--0000	
000D90 _H	PFR16 [R/W] 0-----	PFR17 [R/W] 00000000	PFR18 [R/W] -000-000	PFR19 [R/W] -000-000	
000D94 _H	PFR20 [R/W] -000-000	PFR21 [R/W] -000-000	PFR22 [R/W] 00000000	PFR23 [R/W] -0-00000	
000D98 _H	PFR24 [R/W] 00000000	Reserved			
000D9C _H	PFR28 [R/W] ---0000	PFR29 [R/W] 00000000	Reserved		
000DA0 _H	Reserved			PFR35 [R/W] ----000	
000DA4 _H	PFR36 [R/W] 000-00--	Reserved	PFR38 [R/W] -----00	PFR39 [R/W] 00000000	
000DA8 _H	PFR40 [R/W] 00000000	Reserved			
000DAC _H to 000DBC _H	Reserved				Reserved
000DC0 _H , 000DC4 _H	Reserved				Port Expansion Function Register [R-bus]
000DC8 _H	Reserved		EPFR10 [R/W] --00---0	Reserved	
000DCC _H	Reserved	EPFR13 [R/W] ----0--	EPFR14 [R/W] ----0000	EPFR15 [R/W] ----0000	
000DD0 _H	EPFR16 [R/W] 0-----	Reserved	EPFR18 [R/W] -00--00-	EPFR19 [R/W] -0--0--	
000DD4 _H	EPFR20 [R/W] -0---0--	EPFR21 [R/W] -0---0--	EPFR22 [R/W] ----0-0-	Reserved	
000DD8 _H , 000DDC _H	Reserved				
000DE0 _H	Reserved			EPFR35 [R/W] ----000	
000DE4 _H to 000DFC _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E00 _H to 000E3C _H	Reserved				Reserved
000E40 _H	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		Port Input Level Select Register [R-bus]
000E44 _H	Reserved	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48 _H	PILR08 [R/W] 0000--00	PILR09 [R/W] -0000000	PILR10 [R/W] -0000000	PILR11 [R/W] -----00	
000E4C _H	Reserved	PILR13 [R/W] ----000	PILR14 [R/W] ----0000	PILR15 [R/W] 00--0000	
000E50 _H	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] -000-000	PILR19 [R/W] -000-000	
000E54 _H	PILR20 [R/W] -000-000	PILR21 [R/W] -000-000	PILR22 [R/W] 00000000	PILR23 [R/W] -0-00000	
000E58 _H	PILR24 [R/W] 00000000	Reserved			
000E5C _H	PILR28 [R/W] ----0000	PILR29 [R/W] 00000000	Reserved		
000E60 _H	Reserved			PILR35 [R/W] ----000	
000E64 _H	PILR36 [R/W] 000-00--	Reserved	PILR38 [R/W] -----00	PILR39 [R/W] 00000000	
000E68 _H	PILR40 [R/W] 00000000	Reserved			
000E6C _H to 000E7C _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E80 _H to 000E88 _H	Reserved				Port Expansion Input Level Select Register [R-bus]
000E8C _H	Reserved		EPILR14 [R/W] ---0000	EPILR15 [R/W] ----0000	
000E90 _H	Reserved	EPILR17 [R/W] ----0000	EPILR18 [R/W] -----000	EPILR19 [R/W] -000-000	
000E94 _H	EPILR20 [R/W] -000-000	EPILR21 [R/W] -000-000	EPILR22 [R/W] 00000000	EPILR23 [R/W] -0-00000	
000E98 _H	EPILR24 [R/W] 00000000	Reserved			
000E9C _H , 000EA0 _H	Reserved				
000EA4 _H	EPILR36 [R/W] 000-----	Reserved			
000EA8 _H	EPILR40 [R/W] 00000000	Reserved			
000EAC _H to 000EBC _H	Reserved				Reserved
000EC0 _H	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		Port Pull-Up/Down Enable Register [R-bus]
000EC4 _H	Reserved	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
000EC8 _H	PPER08 [R/W] 0000--00	PPER09 [R/W] -0000000	PPER10 [R/W] -0000000	PPER11 [R/W] -----00	
000ECC _H	Reserved	PPER13 [R/W] -----000	PPER14 [R/W] ----0000	PPER15 [R/W] 0---0000	
000ED0 _H	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] -000-000	PPER19 [R/W] -000-000	
000ED4 _H	PPER20 [R/W] -000-000	PPER21 [R/W] -000-000	PPER22 [R/W] 00000000	PPER23 [R/W] -0-00000	
000ED8 _H	PPER24 [R/W] 00000000	Reserved			
000EDC _H	PPER28 [R/W] ---0000	PPER29 [R/W] 00000000	Reserved		
000EE0 _H	Reserved			PPER35 [R/W] -----000	
000EE4 _H	PPER36 [R/W] 000-00--	Reserved	PPER38 [R/W] -----00	PPER39 [R/W] 00000000	
000EE8 _H	PPER40 [R/W] 00000000	Reserved			

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000EEC _H to 000EFC _H	Reserved				Reserved
000F00 _H	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		Port Pull-Up/Down Control Register [R-bus]
000F04 _H	Reserved	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
000F08 _H	PPCR08 [R/W] 1111--11	PPCR09 [R/W] -1111111	PPCR10 [R/W] -1111111	PPCR11 [R/W] -----11	
000F0C _H	Reserved	PPCR13 [R/W] ----111	PPCR14 [R/W] ----1111	PPCR15 [R/W] 1---1111	
000F10 _H	PPCR16 [R/W] 11111111	PPCR17 [R/W] 11111111	PPCR18 [R/W] -111-111	PPCR19 [R/W] -111-111	
000F14 _H	PPCR20 [R/W] -111-111	PPCR21 [R/W] -111-111	PPCR22 [R/W] 11111111	PPCR23 [R/W] -1-11111	
000F18 _H	PPCR24 [R/W] 11111111	Reserved			
000F1C _H	PPCR28 [R/W] ----1111	PPCR29 [R/W] 11111111	Reserved		
000F20 _H	Reserved			PPCR35 [R/W] ----111	
000F24 _H	PPCR36 [R/W] 111-11--	Reserved	PPCR38 [R/W] -----11	PPCR39 [R/W] 11111111	
000F28 _H	PPCR40 [R/W] 11111111	Reserved			
000F20 _H to 000FFC _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001000 _H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004 _H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008 _H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100C _H	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010 _H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014 _H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018 _H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101C _H	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020 _H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024 _H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028 _H to 005FFC _H	Reserved				Reserved
006000 _H	DCCR [R/W] 00000000 0----- 00000000				MediaLB
006004 _H	SSCR [R/W] ----- 00000000				
006008 _H	SDCR [R/W] 00000000 00000000 00000000 00000000				
00600C _H	SMCR [R/W] ----- -1100000				
006010 _H to 006018 _H	Reserved				
00601C _H	VCCR [R] ----- 00000001 00000010 00000010				
006020 _H to 00602C _H	Reserved				
006030 _H	CICR [R/W] ----- -0000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006034 _H to 00603C _H	Reserved				MediaLB
006040 _H	CECR0 [R/W] 0000000- 00000000 00000000 00000000				
006044 _H	CSCR0 [R/W] 10----- ----0000 00000000 00000000				
006048 _H	CCBCR0 [R] 00000000 00000000 00000000 00000000				
00604C _H	CNBCR0 [R/W] 00000000 00000000 00000000 00000000				
006050 _H	CECR1 [R/W] 0000000- 00000000 00000000 00000000				
006054 _H	CSCR1 [R/W] 10----- ----0000 00000000 00000000				
006058 _H	CCBCR1 [R] 00000000 00000000 00000000 00000000				
00605C _H	CNBCR1 [R/W] 00000000 00000000 00000000 00000000				
006060 _H	CECR2 [R/W] 0000000- 00000000 00000000 00000000				
006064 _H	CSCR2 [R/W] 10----- ----0000 00000000 00000000				
006068 _H	CCBCR2 [R] 00000000 00000000 00000000 00000000				
00606C _H	CNBCR2 [R/W] 00000000 00000000 00000000 00000000				
006070 _H	CECR3 [R/W] 0000000- 00000000 00000000 00000000				
006074 _H	CSCR3 [R/W] 10----- ----0000 00000000 00000000				
006078 _H	CCBCR3 [R] 00000000 00000000 00000000 00000000				
00607C _H	CNBCR3 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006080 _H	CECR4 [R/W] 0000000- 00000000 00000000 00000000				MediaLB
006084 _H	CSCR4 [R/W] 10----- ----0000 00000000 00000000				
006088 _H	CCBCR4 [R] 00000000 00000000 00000000 00000000				
00608C _H	CNBCR4 [R/W] 00000000 00000000 00000000 00000000				
006090 _H	CECR5 [R/W] 0000000- 00000000 00000000 00000000				
006094 _H	CSCR5 [R/W] 10----- ----0000 00000000 00000000				
006098 _H	CCBCR5 [R] 00000000 00000000 00000000 00000000				
00609C _H	CNBCR5 [R/W] 00000000 00000000 00000000 00000000				
0060A0 _H	CECR6 [R/W] 0000000- 00000000 00000000 00000000				
0060A4 _H	CSCR6 [R/W] 10----- ----0000 00000000 00000000				
0060A8 _H	CCBCR6 [R] 00000000 00000000 00000000 00000000				
0060AC _H	CNBCR6 [R/W] 00000000 00000000 00000000 00000000				
0060B0 _H	CECR7 [R/W] 0000000- 00000000 00000000 00000000				
0060B4 _H	CSCR7 [R/W] 10----- ----0000 00000000 00000000				
0060B8 _H	CCBCR7 [R] 00000000 00000000 00000000 00000000				
0060BC _H	CNBCR7 [R/W] 00000000 00000000 00000000 00000000				

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0060C0 _H	CECR8 [R/W] 0000000- 00000000 00000000 00000000				MediaLB
0060C4 _H	CSCR8 [R/W] 10----- ----0000 00000000 00000000				
0060C8 _H	CCBCR8 [R] 00000000 00000000 00000000 00000000				
0060CC _H	CNBCR8 [R/W] 00000000 00000000 00000000 00000000				
0060D0 _H	CECR9 [R/W] 0000000- 00000000 00000000 00000000				
0060D4 _H	CSCR9 [R/W] 10----- ----0000 00000000 00000000				
0060D8 _H	CCBCR9 [R] 00000000 00000000 00000000 00000000				
0060DC _H	CNBCR9 [R/W] 00000000 00000000 00000000 00000000				
0060E0 _H	CECR10 [R/W] 0000000- 00000000 00000000 00000000				
0060E4 _H	CSCR10 [R/W] 10----- ----0000 00000000 00000000				
0060E8 _H	CCBCR10 [R] 00000000 00000000 00000000 00000000				
0060EC _H	CNBCR10 [R/W] 00000000 00000000 00000000 00000000				
0060F0 _H	CECR11 [R/W] 0000000- 00000000 00000000 00000000				
0060F4 _H	CSCR11 [R/W] 10----- ----0000 00000000 00000000				
0060F8 _H	CCBCR11 [R] 00000000 00000000 00000000 00000000				
0060FC _H	CNBCR11 [R/W] 00000000 00000000 00000000 00000000				

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006100 _H	CECR12 [R/W] 0000000- 00000000 00000000 00000000				MediaLB
006104 _H	CSCR12 [R/W] 10----- ----0000 00000000 00000000				
006108 _H	CCBCR12 [R] 00000000 00000000 00000000 00000000				
00610C _H	CNBCR12 [R/W] 00000000 00000000 00000000 00000000				
006110 _H	CECR13 [R/W] 0000000- 00000000 00000000 00000000				
006114 _H	CSCR13 [R/W] 10----- ----0000 00000000 00000000				
006118 _H	CCBCR13 [R] 00000000 00000000 00000000 00000000				
00611C _H	CNBCR13 [R/W] 00000000 00000000 00000000 00000000				
006120 _H	CECR14 [R/W] 0000000- 00000000 00000000 00000000				
006124 _H	CSCR14 [R/W] 10----- ----0000 00000000 00000000				
006128 _H	CCBCR14 [R] 00000000 00000000 00000000 00000000				
00612C _H	CNBCR14 [R/W] 00000000 00000000 00000000 00000000				
006130 _H to 00627F _H	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006280 _H	LCBCR0 [R/W] 00000000 01000000 00000000 00000000				MediaLB
006284 _H	LCBCR1 [R/W] 00000000 01000000 00000000 00000001				
006288 _H	LCBCR2 [R/W] 00000000 01000000 00000000 00000010				
00628C _H	LCBCR3 [R/W] 00000000 01000000 00000000 00000011				
006290 _H	LCBCR4 [R/W] 00000000 01000000 00000000 00000100				
006294 _H	LCBCR5 [R/W] 00000000 01000000 00000000 00000101				
006298 _H	LCBCR6 [R/W] 00000000 01000000 00000000 00000110				
00629C _H	LCBCR7 [R/W] 00000000 01000000 00000000 00000111				
0062A0 _H	LCBCR8 [R/W] 00000000 01000000 00000000 00001000				
0062A4 _H	LCBCR9 [R/W] 00000000 01000000 00000000 00001001				
0062A8 _H	LCBCR10 [R/W] 00000000 01000000 00000000 00001010				
0062AC _H	LCBCR11 [R/W] 00000000 01000000 00000000 00001011				
0062B0 _H	LCBCR12 [R/W] 00000000 01000000 00000000 00001100				
0062B4 _H	LCBCR13 [R/W] 00000000 01000000 00000000 00001101				
0062B8 _H	LCBCR14 [R/W] 00000000 01000000 00000000 00001110				
0062BC _H to 00630F _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006310 _H	I2SSCR [R/W] 00100000 0----000		I2SRSR [R/W] ----- 00000000		I ² S 0 to 9
006314 _H	Reserved				
006318 _H	I2SSCR0 [R/W] ----0000 0--00000		I2SBT0 [R] ----0000	I2SBCR0 [R/W] ---00000	I ² S 0
00631C _H	LTDT0 [R/W] 00000000 00000000		RTDT0 [R/W] 00000000 00000000		
006320 _H	I2SSCR1 [R/W] ----0000 0--00000		I2SBT1 [R] ----0000	I2SBCR1 [R/W] ---00000	I ² S 1
006324 _H	LTDT1 [R/W] 00000000 00000000		RTDT1 [R/W] 00000000 00000000		
006328 _H	I2SSCR2 [R/W] ----0000 0--00000		I2SBT2 [R] ----0000	I2SBCR2 [R/W] ---00000	I ² S 2
00632C _H	LTDT2 [R/W] 00000000 00000000		RTDT2 [R/W] 00000000 00000000		
006330 _H	I2SSCR3 [R/W] ----0000 0--00000		I2SBT3 [R] ----0000	I2SBCR3 [R/W] ---00000	I ² S 3
006334 _H	LTDT3 [R/W] 00000000 00000000		RTDT3 [R/W] 00000000 00000000		
006338 _H	I2SSCR4 [R/W] ----0000 0--00000		I2SBT4 [R] ----0000	I2SBCR4 [R/W] ---00000	I ² S 4
00633C _H	LTDT4 [R/W] 00000000 00000000		RTDT4 [R/W] 00000000 00000000		
006340 _H	I2SSCR5 [R/W] ----0000 0--00000		I2SBT5 [R] ----0000	I2SBCR5 [R/W] ---00000	I ² S 5
006344 _H	LTDT5 [R/W] 00000000 00000000		RTDT5 [R/W] 00000000 00000000		
006348 _H	I2SSCR6 [R/W] ----0000 0--00000		I2SBT6 [R] ----0000	I2SBCR6 [R/W] ---00000	I ² S 6
00634C _H	LTDT6 [R/W] 00000000 00000000		RTDT6 [R/W] 00000000 00000000		
006350 _H	I2SSCR7 [R/W] ----0000 0--00000		I2SBT7 [R] ----0000	I2SBCR7 [R/W] ---00000	I ² S 7
006354 _H	LTDT7 [R/W] 00000000 00000000		RTDT7 [R/W] 00000000 00000000		
006358 _H	I2SSCR8 [R/W] ----0000 0--00000		I2SBT8 [R] ----0000	I2SBCR8 [R/W] ---00000	I ² S 8
00635C _H	LTDT8 [R/W] 00000000 00000000		RTDT8 [R/W] 00000000 00000000		
006360 _H	I2SSCR9 [R/W] ----0000 0--00000		I2SBT9 [R] ----0000	I2SBCR9 [R/W] ---00000	I ² S 9
006364 _H	LTDT9 [R/W] 00000000 00000000		RTDT9 [R/W] 00000000 00000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006368 _H to 00640C _H	Reserved				Reserved
006410 _H	BUFAR0 [R/W] 00000000 00000000 00000000 00000000				MediaLB
006414 _H	BUFAR1 [R/W] 00000000 00000000 00000000 00000000				
006418 _H	BUFAR2 [R/W] 00000000 00000000 00000000 00000000				
00641C _H	BUFAR3 [R/W] 00000000 00000000 00000000 00000000				
006420 _H	BUFAR4 [R/W] 00000000 00000000 00000000 00000000				
006424 _H	BUFAR5 [R/W] 00000000 00000000 00000000 00000000				
006428 _H	BUFAR6 [R/W] 00000000 00000000 00000000 00000000				
00642C _H	BUFAR7 [R/W] 00000000 00000000 00000000 00000000				
006430 _H	MSTD [R/W] -00000000 00000000		MBSYNC [R] XXXXXXXX XXXXXXXX		
006434 _H	BUFAR8 [R/W] 00000000 00000000 00000000 00000000				
006438 _H	BUFAR9 [R/W] 00000000 00000000 00000000 00000000				
00643C _H	BUFAR10 [R/W] 00000000 00000000 00000000 00000000				
006440 _H	BUFAR11 [R/W] 00000000 00000000 00000000 00000000				
006444 _H	BUFAR12 [R/W] 00000000 00000000 00000000 00000000				
006448 _H	BUFAR13 [R/W] 00000000 00000000 00000000 00000000				
00644C _H	BUFAR14 [R/W] 00000000 00000000 00000000 00000000				
006450 _H to 00649C _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0064A0 _H	ASLR [R/W] 00000000 00000000 00000000 00000000				FIFO buffer
0064A4 _H	BUFDCR [R/W] 00000000 00000000 00000000 00000000				
0064A8 _H	BUFIER [R/W] 00000000 00000000 -00000000 00000000				
0064AC _H	BUFSR [R/W] 00000000 00000000 -00000000 00000000				
0064B0 _H	BUFER [R/W] 00000000 00000000 -00000000 00000000				
0064B4 _H	BUFRST [R/W] 00000000 00000000 -00000000 00000000				
0064B8 _H , 0064BC _H	Reserved				
0064C0 _H	BUFCT0 [R/W] ----0000 00000000 ----0000 00000000				
0064C4 _H	BUFCT1 [R/W] ----0000 00000000 ----0000 00000000				
0064C8 _H	BUFCT2 [R/W] ----0000 00000000 ----0000 00000000				
0064CC _H	BUFCT3 [R/W] ----0000 00000000 ----0000 00000000				
0064D0 _H	BUFCT4 [R/W] ----0000 00000000 ----0000 00000000				
0064D4 _H	BUFCT5 [R/W] ----0000 00000000 ----0000 00000000				
0064D8 _H	BUFCT6 [R/W] ----0000 00000000 ----0000 00000000				
0064DC _H	BUFCT7 [R/W] ----0000 00000000 ----0000 00000000				
0064E0 _H to 0064FC _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006500 _H	BUF0CR [R/W] 00000000 00000000 000----0 00000000				FIFO buffer
006504 _H	BUF1CR [R/W] 00000000 00000000 000----0 00000000				
006508 _H	BUF2CR [R/W] 00000000 00000000 000----0 00000000				
00650C _H	BUF3CR [R/W] 00000000 00000000 000----0 00000000				
006510 _H	BUF4CR [R/W] 00000000 00000000 000----0 00000000				
006514 _H	BUF5CR [R/W] 00000000 00000000 000----0 00000000				
006518 _H	BUF6CR [R/W] 00000000 00000000 000----0 00000000				
00651C _H	BUF7CR [R/W] 00000000 00000000 000----0 00000000				
006520 _H	BUF8CR [R/W] 00000000 00000000 000----0 00000000				
006524 _H	BUF9CR [R/W] 00000000 00000000 000----0 00000000				
006528 _H	BUF10CR [R/W] 00000000 00000000 000----0 00000000				
00652C _H	BUF11CR [R/W] 00000000 00000000 000----0 00000000				
006530 _H	BUF12CR [R/W] 00000000 00000000 000----0 00000000				
006534 _H	BUF13CR [R/W] 00000000 00000000 000----0 00000000				
006538 _H	BUF14CR [R/W] 00000000 00000000 000----0 00000000				
00653C _H to 00657C _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006580 _H	BUF0DTR [R/W] 00000000 00000000 00000000 00000000				FIFO buffer
006584 _H	BUF1DTR [R/W] 00000000 00000000 00000000 00000000				
006588 _H	BUF2DTR [R/W] 00000000 00000000 00000000 00000000				
00658C _H	BUF3DTR [R/W] 00000000 00000000 00000000 00000000				
006590 _H	BUF4DTR [R/W] 00000000 00000000 00000000 00000000				
006594 _H	BUF5DTR [R/W] 00000000 00000000 00000000 00000000				
006598 _H	BUF6DTR [R/W] 00000000 00000000 00000000 00000000				
00659C _H	BUF7DTR [R/W] 00000000 00000000 00000000 00000000				
0065A0 _H	BUF8DTR [R/W] 00000000 00000000 00000000 00000000				
0065A4 _H	BUF9DTR [R/W] 00000000 00000000 00000000 00000000				
0065A8 _H	BUF10DTR [R/W] 00000000 00000000 00000000 00000000				
0065AC _H	BUF11DTR [R/W] 00000000 00000000 00000000 00000000				
0065B0 _H	BUF12DTR [R/W] 00000000 00000000 00000000 00000000				
0065B4 _H	BUF13DTR [R/W] 00000000 00000000 00000000 00000000				
0065B8 _H	BUF14DTR [R/W] 00000000 00000000 00000000 00000000				
0065BC _H	Reserved				Reserved
006600 _H	MLBINTR [R] -0000-00 00000000 -----00 00000000				MediaLB I ² S FIFO buffer Interrupt
006604 _H	BUFINTCH [R] 0---0000		Reserved		
006608 _H	BUFPRI0001 [R/W] 11101101	BUFPRI0203 [R/W] 11001011	BUFPRI0405 [R/W] 10101001	BUFPRI0607 [R/W] 10000111	
00660C _H	BUFPRI0809 [R/W] 01100101	BUFPRI1011 [R/W] 01000011	BUFPRI1213 [R/W] 00100001	BUFPRI14 [R/W] 0000----	
006610 _H to 0067FC _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007000 _H	FMCS [R/W] 01101000	FMCR [R/W] ---00000	FCHCR [R/W] -----00 10000011		Flash Memory/ Cache Control Register
007004 _H	FMWT [R/W] 11111111 01011101		FMWT2 [R/W] -101----	FMPs [R/W] -----000	
007008 _H	FMAC [R] 00000000 00000000 00000000 00000000				
00700C _H	FCHA0 [R/W] ----- -00000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010 _H	FCHA1 [R/W] ----- -00000000 00000000 00000000				
007014 _H to 00AFFC _H	Reserved				Reserved
00B000 _H to 00BFFC _H	Boot ROM area				Boot ROM 4Kbytes
00C000 _H	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN0 Control Register
00C004 _H	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
00C008 _H	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
00C00C _H	BRPE0 [R/W] 00000000 00000000		CBSYNCO [R] XXXXXXXX XXXXXXXXX		
00C010 _H	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN0 IF 1 Register
00C014 _H	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
00C018 _H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
00C01C _H	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
00C020 _H	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
00C024 _H	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
00C028 _H , 00C02C _H	Reserved				
00C030 _H	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
00C034 _H	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
00C038 _H , 00C03C _H	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C040 _H	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN0 IF 2 Register
00C044 _H	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
00C048 _H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
00C04C _H	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
00C050 _H	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
00C054 _H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
00C058 _H , 00C05C _H	Reserved				
00C060 _H	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
00C064 _H	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
00C068 _H to 00C07C _H	Reserved				
00C080 _H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN0 Status Flags
00C084 _H to 00C08C _H	Reserved				
00C090 _H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
00C094 _H to 00C09C _H	Reserved				
00C0A0 _H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
00C0A4 _H to 00C0AC _H	Reserved				
00C0B0 _H	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
00C0B4 _H to 00C0FC _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C100 _H	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN1 Control Register
00C104 _H	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
00C108 _H	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
00C10C _H	BRPE1 [R/W] 00000000 00000000		CBSYNC1 [R] XXXXXXXX XXXXXXXXX		
00C110 _H	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN1 IF 1 Register
00C114 _H	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
00C118 _H	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
00C11C _H	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
00C120 _H	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
00C124 _H	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
00C128 _H , 00C12C _H	Reserved				
00C130 _H	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
00C134 _H	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
00C138 _H , 00C13C _H	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C140 _H	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN1 IF 2 Register
00C144 _H	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
00C148 _H	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
00C14C _H	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
00C150 _H	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
00C154 _H	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
00C158 _H , 00C15C _H	Reserved				
00C160 _H	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
00C164 _H	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
00C168 _H to 00C17C _H	Reserved				
00C180 _H	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN1 Status Flags
00C184 _H	TREQR41 [R] 00000000 00000000		TREQR31 [R] 00000000 00000000		
00C188 _H , 00C18C _H	Reserved				
00C190 _H	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
00C194 _H	NEWDT41 [R] 00000000 00000000		NEWDT31 [R] 00000000 00000000		
00C198 _H , 00C19C _H	Reserved				
00C1A0 _H	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
00C1A4 _H	INTPND41 [R] 00000000 00000000		INTPND31 [R] 00000000 00000000		
00C1A8 _H , 00C1AC _H	Reserved				
00C1B0 _H	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
00C1B4 _H	MSGVAL41 [R] 00000000 00000000		MSGVAL31 [R] 00000000 00000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C1B8 _H to 00C1FC _H	Reserved				CAN1 Status Flags
00C200 _H to 00EFFC _H	Reserved				Reserved
00F000 _H	BCTRL [R/W] ----- 11111100 00000000				EDSU / MPU
00F004 _H	BSTAT [R/W] ----- 000 00000000 10--0000				
00F008 _H	BIAC [R] ----- 00000000 00000000				
00F00C _H	BOAC [R] ----- 00000000 00000000				
00F010 _H	BIRQ [R/W] ----- 00000000 00000000				
00F014 _H to 00F01C _H	Reserved				
00F020 _H	BCR0 [R/W] ----- 00000000 00000000 00000000				
00F024 _H	BCR1 [R/W] ----- 00000000 00000000 00000000				
00F028 _H	BCR2 [R/W] ----- 00000000 00000000 00000000				
00F02C _H	BCR3 [R/W] ----- 00000000 00000000 00000000				
00F030 _H to 00F07C _H	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00F080 _H	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F084 _H	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F088 _H	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F08C _H	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F090 _H	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F094 _H	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F098 _H	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F09C _H	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A0 _H	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A4 _H	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A8 _H	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0AC _H	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0 _H	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4 _H	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8 _H	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BC _H	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0 _H to 00FFFC _H	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00010000 _H to 000107FC _H	TAG RAM (way1)				
00010800 _H to 00013FFC _H	Reserved				Reserved
00014000 _H to 000147FC _H	TAG RAM (way2)				
00014800 _H to 00017FFC _H	Reserved				Reserved
00018000 _H to 000187FC _H	CACHE RAM (way1) / I-RAM (2 Kbytes)				
00018800 _H to 0001BFFC _H	Reserved				Reserved
0001C000 _H to 0001C7FC _H	CACHE RAM (way2) / I-RAM (2 Kbytes)				
0001C800 _H to 0001FFFC _H	Reserved				Reserved
020000 _H to 027FFC _H	Reserved				RAM (64 Kbytes)
024000 _H to 02BFFC _H	D-RAM area (32 Kbytes) (It is not possible to use instruction access, data access is 1 wait cycle)				
02C000 _H to 02FFFC _H	D-RAM area (16 Kbytes) (It is not possible to use instruction access, data access is 0 wait cycle)				
030000 _H to 033FFC _H	I/D-RAM area (16 Kbytes) (instruction access is 0 wait cycles, data access is 1 wait cycle)				
034000 _H to 03FFFC _H	Reserved				

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
040000 _H to 05FFFC _H	ROMS00 area (128 Kbytes)				Flash (1088 Kbytes)
060000 _H to 07FFFC _H	ROMS01 area (128 Kbytes)				
080000 _H to 09FFFC _H	ROMS02 area (128 Kbytes)				
0A0000 _H to 0BFFFC _H	ROMS03 area (128 Kbytes)				
0C0000 _H to 0DFFFC _H	ROMS04 area (128 Kbytes)				
0E0000 _H to 0FFFFC _H	ROMS05 area (128 Kbytes) Mode Vector:0FFFF8 _H Reset Vector:0FFFFC _H				
100000 _H to 13FFFC _H	ROMS06 area (256 Kbytes)				
140000 _H to 14FFFC _H	ROMS07 area (64 Kbytes)				
150000 _H to 17FFFC _H	Reserved				

Note: It is not allowed to write into 0FFFF8_H and 0FFFFC_H. When these addresses are read, values shown above will be read.

12. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level* ¹		Interrupt vector* ²		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	0 _H	—	—	3FC _H	000FFFFC _H	
Mode vector	1	1 _H	—	—	3F8 _H	000FFFF8 _H	
System reserved	2	2 _H	—	—	3F4 _H	000FFFF4 _H	
System reserved	3	3 _H	—	—	3F0 _H	000FFFF0 _H	
System reserved	4	4 _H	—	—	3EC _H	000FFFE _C	
CPU supervisor mode (INT #5 instruction)* ⁶	5	5 _H	—	—	3E8 _H	000FFFE8 _H	
Memory Protection exception	6	6 _H	—	—	3E4 _H	000FFFE4 _H	
Co-processor fault trap* ⁵	7	7 _H	—	—	3E0 _H	000FFFE0 _H	
Co-processor error trap* ⁵	8	8 _H	—	—	3DC _H	000FFFD _C	
INTE instruction* ⁵	9	9 _H	—	—	3D8 _{HH}	000FFFD8 _H	
Instruction break exception* ⁵	10	0A _H	—	—	3D4 _H	000FFFD4 _H	
Operand break trap* ⁵	11	0B _H	—	—	3D0 _H	000FFFD0 _H	
Step trace trap* ⁵	12	0C _H	—	—	3CC _H	000FFFC _C	
NMI request (tool) * ⁵	13	0D _H	—	—	3C8 _H	000FFFC8 _H	
Undefined instruction exception	14	0E _H	—	—	3C4 _H	000FFFC4 _H	
NMI request	15	0F _H	F _H fixed		3C0 _H	000FFFC0 _H	
External Interrupt 0	16	10 _H	ICR00	440 _H	3BC _H	000FFFB _C	0, 16
External Interrupt 1	17	11 _H			3B8 _H	000FFFB8 _H	1, 17
External Interrupt 2	18	12 _H	ICR01	441 _H	3B4 _H	000FFFB4 _H	2, 18
External Interrupt 3	19	13 _H			3B0 _H	000FFFB0 _H	3, 19
External Interrupt 4	20	14 _H	ICR02	442 _H	3AC _H	000FFFA _C	20
External Interrupt 5	21	15 _H			3A8 _H	000FFFA8 _H	21
External Interrupt 6	22	16 _H	ICR03	443 _H	3A4 _H	000FFFA4 _H	22
External Interrupt 7	23	17 _H			3A0 _H	000FFFA0 _H	23
External Interrupt 8	24	18 _H	ICR04	444 _H	39C _H	000FFF9 _C	
External Interrupt 9	25	19 _H			398 _H	000FFF98 _H	
External Interrupt 10	26	1A _H	ICR05	445 _H	394 _H	000FFF94 _H	
External Interrupt 11	27	1B _H			390 _H	000FFF90 _H	
External Interrupt 12	28	1C _H	ICR06	446 _H	38C _H	000FFF8 _C	
External Interrupt 13	29	1D _H			388 _H	000FFF88 _H	
External Interrupt 14	30	1E _H	ICR07	447 _H	384 _H	000FFF84 _H	
External Interrupt 15	31	1F _H			380 _H	000FFF80 _H	

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 0	32	20 _H	ICR08	448 _H	37C _H	000FFF7C _H	4, 32
Reload Timer 1	33	21 _H			378 _H	000FFF78 _H	5, 33
Reload Timer 2	34	22 _H	ICR09	449 _H	374 _H	000FFF74 _H	34
Reload Timer 3	35	23 _H			370 _H	000FFF70 _H	35
Reserved	36	24 _H	ICR10	44A _H	36C _H	000FFF6C _H	
Reserved	37	25 _H			368 _H	000FFF68 _H	
Reserved	38	26 _H	ICR11	44B _H	364 _H	000FFF64 _H	
Reload Timer 7	39	27 _H			360 _H	000FFF60 _H	
Free Run Timer 0	40	28 _H	ICR12	44C _H	35C _H	000FFF5C _H	40
Free Run Timer 1	41	29 _H			358 _H	000FFF58 _H	41
Free Run Timer 2	42	2A _H	ICR13	44D _H	354 _H	000FFF54 _H	42
Free Run Timer 3	43	2B _H			350 _H	000FFF50 _H	43
Reserved	44	2C _H	ICR14	44E _H	34C _H	000FFF4C _H	
Reserved	45	2D _H			348 _H	000FFF48 _H	
Reserved	46	2E _H	ICR15	44F _H	344 _H	000FFF44 _H	
Reserved	47	2F _H			340 _H	000FFF40 _H	
CAN 0	48	30 _H	ICR16	450 _H	33C _H	000FFF3C _H	
CAN 1	49	31 _H			338 _H	000FFF38 _H	
Reserved	50	32 _H	ICR17	451 _H	334 _H	000FFF34 _H	
Reserved	51	33 _H			330 _H	000FFF30 _H	
Reserved	52	34 _H	ICR18	452 _H	32C _H	000FFF2C _H	
Reserved	53	35 _H			328 _H	000FFF28 _H	
LIN-USART0 RX	54	36 _H	ICR19	453 _H	324 _H	000FFF24 _H	6, 48
LIN-USART0 TX	55	37 _H			320 _H	000FFF20 _H	7, 49
LIN-USART1 RX	56	38 _H	ICR20	454 _H	31C _H	000FFF1C _H	8, 50
LIN-USART1 TX	57	39 _H			318 _H	000FFF18 _H	9, 51
LIN-USART2 RX	58	3A _H	ICR21	455 _H	314 _H	000FFF14 _H	52
LIN-USART2 TX	59	3B _H			310 _H	000FFF10 _H	53
LIN-USART3 RX	60	3C _H	ICR22	456 _H	30C _H	000FFF0C _H	54
LIN-USART3 TX	61	3D _H			308 _H	000FFF08 _H	55
System reserved	62	3E _H	ICR23*4	457 _H	304 _H	000FFF04 _H	
Delayed Interrupt	63	3F _H			300 _H	000FFF00 _H	

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved *3	64	40 _H	(ICR24)	(458 _H)	2FC _H	000FFEFC _H	
System reserved *3	65	41 _H			2F8 _H	000FFEF8 _H	
LIN-USART (FIFO) 4 RX	66	42 _H	ICR25	459 _H	2F4 _H	000FFEF4 _H	10, 56
LIN-USART (FIFO) 4 TX	67	43 _H			2F0 _H	000FFEF0 _H	11, 57
LIN-USART (FIFO) 5 RX	68	44 _H	ICR26	45A _H	2EC _H	000FFEEC _H	12, 58
LIN-USART (FIFO) 5 TX	69	45 _H			2E8 _H	000FFEE8 _H	13, 59
LIN-USART (FIFO) 6 RX	70	46 _H	ICR27	45B _H	2E4 _H	000FFEE4 _H	60
LIN-USART (FIFO) 6 TX	71	47 _H			2E0 _H	000FFEE0 _H	61
LIN-USART (FIFO) 7 RX	72	48 _H	ICR28	45C _H	2DC _H	000FFEDC _H	62
LIN-USART (FIFO) 7 TX	73	49 _H			2D8 _H	000FFED8 _H	63
I ² C 0 / I ² C 2	74	4A _H	ICR29	45D _H	2D4 _H	000FFED4 _H	
I ² C 1 / I ² C 3	75	4B _H			2D0 _H	000FFED0 _H	
LIN-USART (LIN) 8 RX	76	4C _H	ICR30	45E _H	2CC _H	000FFEC _H	64
LIN-USART (LIN) 8 TX	77	4D _H			2C8 _H	000FFEC8 _H	65
I ² C 4 / I ² C 6	78	4E _H	ICR31	45F _H	2C4 _H	000FFEC4 _H	
I ² C 5 / I ² C 7	79	4F _H			2C0 _H	000FFEC0 _H	
Reserved	80	50 _H	ICR32	460 _H	2BC _H	000FFEB _H	
Reserved	81	51 _H			2B8 _H	000FFEB8 _H	
FIFO buffer	82	52 _H	ICR33	461 _H	2B4 _H	000FFEB4 _H	
Reserved	83	53 _H			2B0 _H	000FFEB0 _H	
Reserved	84	54 _H	ICR34	462 _H	2AC _H	000FFEAC _H	
Reserved	85	55 _H			2A8 _H	000FFEA8 _H	
Reserved	86	56 _H	ICR35	463 _H	2A4 _H	000FFEA4 _H	
Reserved	87	57 _H			2A0 _H	000FFEA0 _H	
MediaLB	88	58 _H	ICR36	464 _H	29C _H	000FFE9C _H	
I ² S ERROR	89	59 _H			298 _H	000FFE98 _H	
I ² S EVEN	90	5A _H	ICR37	465 _H	294 _H	000FFE94 _H	125
I ² S ODD	91	5B _H			290 _H	000FFE90 _H	126
Input Capture 0	92	5C _H	ICR38	466 _H	28C _H	000FFE8C _H	80
Input Capture 1	93	5D _H			288 _H	000FFE88 _H	81
Input Capture 2	94	5E _H	ICR39	467 _H	284 _H	000FFE84 _H	82
Input Capture 3	95	5F _H			280 _H	000FFE80 _H	83

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	96	60 _H	ICR40	468 _H	27C _H	000FFE7C _H	
Reserved	97	61 _H			278 _H	000FFE78 _H	
Reserved	98	62 _H	ICR41	469 _H	274 _H	000FFE74 _H	
Reserved	99	63 _H			270 _H	000FFE70 _H	
Output Compare 0	100	64 _H	ICR42	46A _H	26C _H	000FFE6C _H	88
Output Compare 1	101	65 _H			268 _H	000FFE68 _H	89
Output Compare 2	102	66 _H	ICR43	46B _H	264 _H	000FFE64 _H	90
Output Compare 3	103	67 _H			260 _H	000FFE60 _H	91
Reserved	104	68 _H	ICR44	46C _H	25C _H	000FFE5C _H	
Reserved	105	69 _H			258 _H	000FFE58 _H	
Reserved	106	6A _H	ICR45	46D _H	254 _H	000FFE54 _H	
Reserved	107	6B _H			250 _H	000FFE50 _H	
Reserved	108	6C _H	ICR46	46E _H	24C _H	000FFE4C _H	
Reserved	109	6D _H			248 _H	000FFE48 _H	
Reserved	110	6E _H	ICR47*4	46F _H	244 _H	000FFE44 _H	
Reserved	111	6F _H			240 _H	000FFE40 _H	
PPG0	112	70 _H	ICR48	470 _H	23C _H	000FFE3C _H	15, 96
PPG1	113	71 _H			238 _H	000FFE38 _H	97
PPG2	114	72 _H	ICR49	471 _H	234 _H	000FFE34 _H	98
PPG3	115	73 _H			230 _H	000FFE30 _H	99
PPG4	116	74 _H	ICR50	472 _H	22C _H	000FFE2C _H	100
PPG5	117	75 _H			228 _H	000FFE28 _H	101
PPG6	118	76 _H	ICR51	473 _H	224 _H	000FFE24 _H	102
PPG7	119	77 _H			220 _H	000FFE20 _H	103
Reserved	120	78 _H	ICR52	474 _H	21C _H	000FFE1C _H	
Reserved	121	79 _H			218 _H	000FFE18 _H	
Reserved	122	7A _H	ICR53	475 _H	214 _H	000FFE14 _H	
Reserved	123	7B _H			210 _H	000FFE10 _H	
Reserved	124	7C _H	ICR54	476 _H	20C _H	000FFE0C _H	
Reserved	125	7D _H			208 _H	000FFE08 _H	
Reserved	126	7E _H	ICR55	477 _H	204 _H	000FFE04 _H	
Reserved	127	7F _H			200 _H	000FFE00 _H	
Reserved	128	80 _H	ICR56	478 _H	1FC _H	000FFDFC _H	
Reserved	129	81 _H			1F8 _H	000FFDF8 _H	

(Continued)

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	130	82 _H	ICR57	479 _H	1F4 _H	000FFDF4 _H	
Reserved	131	83 _H			1F0 _H	000FFDF0 _H	
Real Time Clock	132	84 _H	ICR58	47A _H	1EC _H	000FFDEC _H	
Calibration Unit	133	85 _H			1E8 _H	000FFDE8 _H	
A/D Converter 0	134	86 _H	ICR59	47B _H	1E4 _H	000FFDE4 _H	14, 112
Reserved	135	87 _H			1E0 _H	000FFDE0 _H	
Reserved	136	88 _H	ICR60	47C _H	1DC _H	000FFDDC _H	
Reserved	137	89 _H			1D8 _H	000FFDD8 _H	
Low Voltage Detection	138	8A _H	ICR61	47D _H	1D4 _H	000FFDD4 _H	
Reserved	139	8B _H			1D0 _H	000FFDD0 _H	
Timebase Overflow	140	8C _H	ICR62	47E _H	1CC _H	000FFDCC _H	
PLL Clock Gear	141	8D _H			1C8 _H	000FFDC8 _H	
DMA Controller	142	8E _H	ICR63	47F _H	1C4 _H	000FFDC4 _H	
Main/Sub OSC stability wait	143	8F _H			1C0 _H	000FFDC0 _H	
Reserved	144	90 _H	—	—	1BC _H	000FFDBC _H	
Used by the INT instruction.	145 to 255	91 _H to FF _H	—	—	1B8 _H to 000 _H	000FFDB8 _H to 000FFC00 _H	

*1 : The ICRs set the interrupt level for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset.

*3 : Used by REALOS.

*4 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0xC03 : IOS[0])

*5 : System reserved.

*6 : Memory Protection Unit (MPU) support.

13. Recommended Settings

13.1 PLL and Clockgear settings

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

13.2 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a center clock frequency range from 32MHz up to 80 MHz. The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to center clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F _H	72	65.5	79.9	
1	3	026F _H	68	62	75.3	
1	3	026F _H	64	58.5	70.7	
1	5	02AE _H	64	55.3	75.9	
2	3	046E _H	64	55.3	75.9	
1	3	026F _H	60	54.9	66.1	
1	5	02AE _H	60	51.9	71	
1	7	02ED _H	60	49.3	76.7	
2	3	046E _H	60	51.9	71	
3	3	066D _H	60	49.3	76.7	
1	3	026F _H	56	51.4	61.6	
1	5	02AE _H	56	48.6	66.1	
1	7	02ED _H	56	46.1	71.4	
1	9	032C _H	56	43.8	77.6	
2	3	046E _H	56	48.6	66.1	
2	5	04AC _H	56	43.8	77.6	
3	3	066D _H	56	46.1	71.4	
4	3	086C _H	56	43.8	77.6	
1	3	026F _H	52	47.8	57	
1	5	02AE _H	52	45.2	61.2	
1	7	02ED _H	52	42.9	66.1	
1	9	032C _H	52	40.8	71.8	
1	11	036B _H	52	38.8	78.6	
2	3	046E _H	52	45.2	61.2	
2	5	04AC _H	52	40.8	71.8	
3	3	066D _H	52	42.9	66.1	
4	3	086C _H	52	40.8	71.8	
5	3	0A6B _H	52	38.8	78.6	
1	3	026F _H	48	44.2	52.5	
1	5	02AE _H	48	41.8	56.4	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	7	02ED _H	48	39.6	60.9	
1	9	032C _H	48	37.7	66.1	
1	11	036B _H	48	35.9	72.3	
1	13	03AA _H	48	34.3	79.9	
2	3	046E _H	48	41.8	56.4	
2	5	04AC _H	48	37.7	66.1	
2	7	04EA _H	48	34.3	79.9	
3	3	066D _H	48	39.6	60.9	
3	5	06AA _H	48	34.3	79.9	
4	3	086C _H	48	37.7	66.1	
5	3	0A6B _H	48	35.9	72.3	
6	3	0C6A _H	48	34.3	79.9	
1	3	026F _H	44	40.6	48.1	
1	5	02AE _H	44	38.4	51.6	
1	7	02ED _H	44	36.4	55.7	
1	9	032C _H	44	34.6	60.4	
1	11	036B _H	44	33	66.1	
1	13	03AA _H	44	31.5	73	
2	3	046E _H	44	38.4	51.6	
2	5	04AC _H	44	34.6	60.4	
2	7	04EA _H	44	31.5	73	
3	3	066D _H	44	36.4	55.7	
3	5	06AA _H	44	31.5	73	
4	3	086C _H	44	34.6	60.4	
5	3	0A6B _H	44	33	66.1	
6	3	0C6A _H	44	31.5	73	
1	3	026F _H	40	37	43.6	
1	5	02AE _H	40	34.9	46.8	
1	7	02ED _H	40	33.1	50.5	
1	9	032C _H	40	31.5	54.8	
1	11	036B _H	40	30	59.9	
1	13	03AA _H	40	28.7	66.1	
1	15	03E9 _H	40	27.4	73.7	
2	3	046E _H	40	34.9	46.8	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	5	04AC _H	40	31.5	54.8	
2	7	04EA _H	40	28.7	66.1	
3	3	066D _H	40	33.1	50.5	
3	5	06AA _H	40	28.7	66.1	
4	3	086C _H	40	31.5	54.8	
5	3	0A6B _H	40	30	59.9	
6	3	0C6A _H	40	28.7	66.1	
7	3	0E69 _H	40	27.4	73.7	
1	3	026F _H	36	33.3	39.2	
1	5	02AE _H	36	31.5	42	
1	7	02ED _H	36	29.9	45.3	
1	9	032C _H	36	28.4	49.2	
1	11	036B _H	36	27.1	53.8	
1	13	03AA _H	36	25.8	59.3	
1	15	03E9 _H	36	24.7	66.1	
2	3	046E _H	36	31.5	42	
2	5	04AC _H	36	28.4	49.2	
2	7	04EA _H	36	25.8	59.3	
2	9	0528 _H	36	23.7	74.7	
3	3	066D _H	36	29.9	45.3	
3	5	06AA _H	36	25.8	59.3	
4	3	086C _H	36	28.4	49.2	
4	5	08A8 _H	36	23.7	74.7	
5	3	0A6B _H	36	27.1	53.8	
6	3	0C6A _H	36	25.8	59.3	
7	3	0E69 _H	36	24.7	66.1	
8	3	1068 _H	36	23.7	74.7	
1	3	026F _H	32	29.7	34.7	
1	5	02AE _H	32	28	37.3	
1	7	02ED _H	32	26.6	40.2	
1	9	032C _H	32	25.3	43.6	
1	11	036B _H	32	24.1	47.7	
1	13	03AA _H	32	23	52.5	

(Continued)

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Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	03E9 _H	32	22	58.6	
2	3	046E _H	32	28	37.3	
2	5	04AC _H	32	25.3	43.6	
2	7	04EA _H	32	23	52.5	
2	9	0528 _H	32	21.1	66.1	
3	3	066D _H	32	26.6	40.2	
3	5	06AA _H	32	23	52.5	
3	7	06E7 _H	32	20.3	75.9	
4	3	086C _H	32	25.3	43.6	
4	5	08A8 _H	32	21.1	66.1	
5	3	0A6B _H	32	24.1	47.7	
6	3	0C6A _H	32	23	52.5	
7	3	0E69 _H	32	22	58.6	
8	3	1068 _H	32	21.1	66.1	
9	3	1267 _H	32	20.3	75.9	

14. Electrical Characteristics

14.1 Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{CC3}	V _{SS} - 0.5	V _{SS} + 4.0	V	V _{CC5} ≥ V _{CC3}
	V _{CC5}	V _{SS} - 0.5	V _{SS} + 6.0	V	V _{CC5} ≥ V _{CC3}
	AV _{CC3}	V _{SS} - 0.5	V _{SS} + 4.0	V	V _{CC3} ≥ AV _{CC3} ≥ AVRH
	AVRH	V _{SS} - 0.5	V _{SS} + 4.0	V	V _{CC3} ≥ AVRH
Input voltage 1*1	V _{I1}	V _{SS} - 0.3	V _{CC3} + 0.3	V	3 V pin group
Input voltage 2*1	V _{I2}	V _{SS} - 0.3	V _{CC5} + 0.3	V	5 V pin group
Analog pin input voltage	V _{IA}	V _{SS} - 0.3	AV _{CC3} + 0.3	V	
Output voltage 1*1	V _{O1}	V _{SS} - 0.3	V _{CC3} + 0.3	V	3 V pin group
Output voltage 2*1	V _{O2}	V _{SS} - 0.3	V _{CC5} + 0.3	V	5 V pin group
Maximum clamp current (+B input)	I _{CLAMP}	-2	2	mA	*2
Total maximum clamp current (+B input)	ΣI _{CLAMP}	-20	20	mA	*2
"L" level maximum output current	I _{OL}	—	10	mA	*3
"L" level average output current	I _{OLAV}	—	8	mA	*4
"L" level total maximum output current	ΣI _{OL}	—	100	mA	
"L" level total average output current	ΣI _{OLAV}	—	50	mA	*5
"H" level maximum output current	I _{OH}	—	-10	mA	*3
"H" level average output current	I _{OHAV}	—	-4	mA	*4
"H" level total maximum output current	ΣI _{OH}	—	-50	mA	
"H" level total average output current	ΣI _{OHAV}	—	-20	mA	*5
Power consumption	P _D	—	500	mW	
Operating temperature	T _A	-40	+ 105	°C	
Storage temperature	T _{stg}	-55	+ 150	°C	

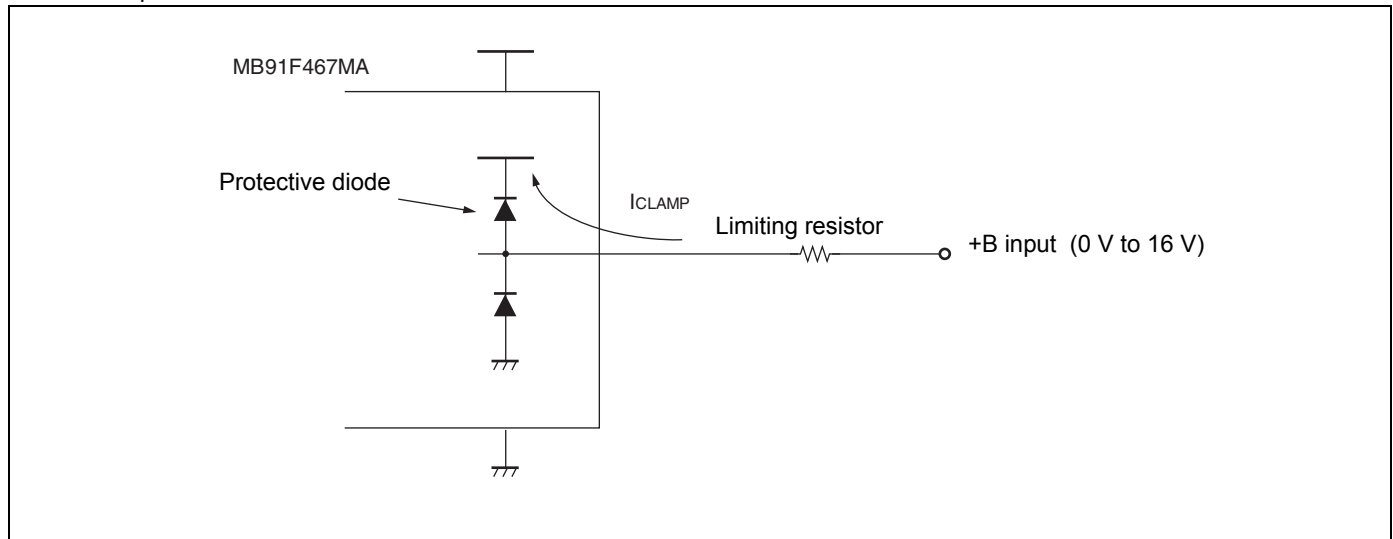
*1 : This parameter is based on V_{SS} = AV_{SS} = 0.0 V

- *2 : • This is a 5 V pin which works as a port or serves with a port.
 • Use within recommended operating conditions.
 • Use with DC voltage (current).
 • The standard value of +B input is defined as the power supply flowing through any one of the corresponding pins.
 • +B signals are input signals that exceed the V_{CC5} voltage.
 Connect limiting resistor between the +B signal and the microcontroller.
 • The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.
 • Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin V_{CC5}, V_{CC3} via a protective diode, possibly affecting other devices.

(Continued)

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- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit:



- *3 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
- *4 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period. The average value is the operation current × the operation ratio.
- *5 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period. The average value is the operation current × the operation ratio.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended operating conditions

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC5}	3.0	5.5	V	5 V operation guarantee range
	V_{CC3}	3.0	3.6	V	3 V operation guarantee range
	AV_{CC3}	3.0	3.6	V	Analog operation guarantee range
Smoothing capacitor at C_1, C_2 pin	C_S	4.7 (accuracy within $\pm 50\%$)		μF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC5, VCC3 pins.
Power supply slew rate	—	1	50	V/ms	
Operating temperature	T_A	-40	+ 105	°C	
Main oscillation stabilization time	—	8	—	ms	
Look-up time PLL (4 MHz→16 ...80 MHz)	—	—	0.6	ms	
ESD Protection (Human body model)	Vsurge	2	—	kV	$R_{\text{discharge}} = 1.5\text{ k}\Omega$ $C_{\text{discharge}} = 100\text{ pF}$
RC Oscillator	fRC100kHz	50	200	kHz	
	fRC2MHz	1	4	MHz	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

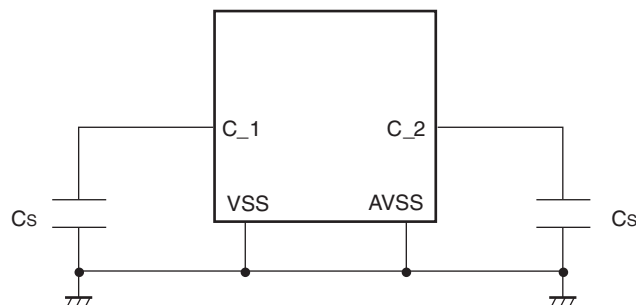
Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.

Users considering application outside the listed conditions are advised to contact their representatives beforehand.

C Pin Connection Diagram



14.3 DC characteristics
 $(T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{CC5} = 5.0\text{ V} \pm 10\%, V_{CC3} = 3.3\text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0\text{ V})$

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	CMOS-hys	—	$0.8 V_{CC5/3}$	—	$V_{CC5/3} + 0.3$	V	CMOS hysteresis input pin
	V_{IH2}	CMOS-hys	—	$0.7 V_{CC5/3}$	—	$V_{CC5/3} + 0.3$	V	CMOS hysteresis input pin
	V_{IH3}	CMOS	—	$0.7 V_{CC5}$	—	$V_{CC5} + 0.3$	V	CMOS input pin
	V_{IH4}	Automotive	—	$0.8 V_{CC5}$	—	$V_{CC5} + 0.3$	V	Automotive input pin
	V_{IH5}	MediaLB	—	1.7	—	$V_{CC3} + 0.3$	V	MediaLB input pin
	V_{IHM}	MD4 to MD0	—	$V_{CC5} - 0.3$	—	$V_{CC5} + 0.3$	V	
	V_{IHX5}	INITX	—	$0.8 V_{CC5}$	—	$V_{CC5} + 0.3$	V	
	V_{IHX3}	X0, X1, X0A, X1A, TRSTX	—	$0.8 V_{CC3}$	—	$V_{CC3} + 0.3$	V	TRSTX can withstand 5 V.
"L" level input voltage	V_{IL1}	CMOS-hys	—	$V_{SS} - 0.3$	—	$0.2 V_{CC5/3}$	V	CMOS hysteresis input pin
	V_{IL2}	CMOS-hys	—	$V_{SS} - 0.3$	—	$0.3 V_{CC5/3}$	V	CMOS hysteresis input pin
	V_{IL3}	CMOS	—	$V_{SS} - 0.3$	—	$0.3 V_{CC5/3}$	V	CMOS input pin
	V_{IL4}	Automotive	—	$V_{SS} - 0.3$	—	$0.5 V_{CC5}$	V	Automotive input pin
	V_{IL5}	MediaLB	—	$V_{SS} - 0.3$	—	0.7	V	MediaLB input pin
	V_{ILM}	MD4 to MD0	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD pin
	V_{ILX5}	INITX	—	$V_{SS} - 0.3$	—	$0.2 V_{CC5}$	V	
	V_{ILX3}	X0, X1, X0A, X1A, TRSTX	—	$V_{SS} - 0.3$	—	$0.2 V_{CC3}$	V	

(Continued)

$(T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{CC5} = 5.0\text{ V} \pm 10\%, V_{CC3} = 3.3\text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0\text{ V})$

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	VCC3	At Main RUN	—	110	140	mA	Core : 80 MHz Peripheral : 20 MHz External bus : 40 MHz CAN : 20 MHz MediaLB : 28 MHz (No load on the external bus)
	I_{CCS}	VCC3	At Main SLEEP	—	30	55	mA	Core : 80 MHz Peripheral : 20 MHz External bus : 40 MHz CAN : 20 MHz MediaLB : 28 MHz (No load on the external bus)
	I_{CCH}	VCC5, VCC3	$T_A = +25^{\circ}\text{C}$, $V_{CC5} = 5\text{ V}$, $V_{CC3} = 3.3\text{ V}$, At STOP mode	—	0.1	1	mA	Main oscillation/PLL stop Sub oscillation stop Main regulator stop Low voltage detector stop
	I_{CCHS}	VCC5, VCC3	$T_A = +25^{\circ}\text{C}$, $V_{CC5} = 5\text{ V}$, $V_{CC3} = 3.3\text{ V}$, At shutdown	—	10	50	μA	Shutdown mode Low voltage detector stop
	I_{CCL}	VCC3	Operation frequency $F_{CP} = 32\text{ kHz}$, $T_A = +25^{\circ}\text{C}$, $V_{CC3} = 3.3\text{ V}$, At Sub RUN	—	1	2	mA	Main oscillation/PLL stop Low voltage detector stop
	I_{CTS4M1}	VCC3	Main clock frequency = 4 MHz, $T_A = +25^{\circ}\text{C}$, $V_{CC3} = 3.3\text{ V}$, At stop (Real Time Clock Operation)	—	500	1000	μA	PLL/Sub oscillation stop Low voltage detector stop
	$I_{CTS32K1}$	VCC3	Sub clock frequency = 32 kHz, $T_A = +25^{\circ}\text{C}$, $V_{CC3} = 3.3\text{ V}$ At stop (Real Time Clock Operation)	—	200	700	μA	Main oscillation/PLL stop Low voltage detector stop
	I_{CTS4M2}	VCC3	Main clock frequency = 4 MHz, $T_A = +25^{\circ}\text{C}$, $V_{CC3} = 3.3\text{ V}$, At stop (Real Time Clock Operation)	—	650	1150	μA	PLL/Sub oscillation stop
	$I_{CTS32K2}$	VCC3	Sub clock frequency = 32 kHz, $T_A = +25^{\circ}\text{C}$, $V_{CC3} = 3.3\text{ V}$ At stop (Real Time Clock Operation)	—	350	850	μA	Main oscillation/PLL stop

* : Power supply current is obtained when an external clock is supplied from X1/X1A pins.

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($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC5} = 5.0\text{ V} \pm 10\%$, $V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	$V_{CC5} = 5\text{ V}$ $V_{CC3} = AV_{CC3} = 3.3\text{ V}$ $V_{SS} < V_I < V_{CC5}/3$	-5	—	+ 5	μA	
Input capacitance 1	C_{IN}	Other than V_{CC5} , V_{CC3} , V_{SS} , AV_{CC3} , AV_{SS} , AV_{RH} , $C_{_1}$, $C_{_2}$	—	—	5	15	pF	
Pull-up resistance	R_{UP}	INITX, Pins with pull-up resistance	—	25	50	100	k Ω	
Pull-down resistance	R_{DOWN}	Pins with pull-down resistance	—	25	50	100	k Ω	
Output “H” voltage	V_{OH1}	5/3 V pin	$V_{CC5} = 5.0\text{ V}$, $I_{OH} = -5.0\text{ mA}$ $V_{CC5} = 3.3\text{ V}$, $I_{OH} = -2.0\text{ mA}$	$V_{CC5} - 0.5$	—	—	V	
	V_{OH2}	3 V pin	$V_{CC3} = 3.3\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC3} - 0.5$	—	—	V	
	V_{OH3}	MediaLB pin	$V_{CC3} = 3.3\text{ V}$, $I_{OH} = -6.0\text{ mA}$	2.0	—	—	V	
Output “L” voltage	V_{OL1}	5/3 Vpin	$V_{CC5} = 5.0\text{ V}$, $I_{OL} = 5.0\text{ mA}$ $V_{CC5} = 3.3\text{ V}$, $I_{OL} = 2.0\text{ mA}$	—	—	0.4	V	
	V_{OL2}	3 Vpin	$V_{CC3} = 3.3\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	V_{OL3}	MediaLB pin	$V_{CC3} = 3.3\text{ V}$, $I_{OL} = 6.0\text{ mA}$	—	—	0.4	V	

14.4 A/D converter characteristics

14.4.1 Electrical Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC3} = AV_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	Bit	
Total error	—	—	—	—	± 3	LSB	$AV_{CC3} = 3.3\text{ V}$ $AVRH = 3.3\text{ V}$
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential linearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN11	$AV_{SS} - 1.5\text{LSB}$	$AV_{SS} + 0.5\text{LSB}$	$AV_{SS} + 2.5\text{LSB}$	V	
Full scale transition voltage	V_{FST}	AN0 to AN11	$AVRH - 3.5\text{LSB}$	$AVRH - 1.5\text{LSB}$	$AVRH + 0.5\text{LSB}$	V	
Sampling time	t_{SMP}	—	1000	—	—	ns	At $R_{EXT} < 4.2\text{ k}\Omega$ *1
Compare time	t_{CMP}	—	2200	—	—	ns	
A/D conversion time	t_{CNV}	—	3	—	1000	μs	$t_{SMP} + t_{CMP}$
Analog port input current	I_{AIN}	AN0 to AN11	—	—	10	μA	$AV_{CC3} \geq V_{AIN} \geq AV_{SS}$
Analog input voltage	V_{AIN}	AN0 to AN11	AV_{SS}	—	$AVRH$	V	
Reference voltage	$AVR +$	$AVRH$	AV_{SS}	—	AV_{CC3}	V	
Power supply current	I_A	$AVCC3$	—	1.9	3.7	mA	
	I_{AH}		—	—	5	μA	*2
Reference voltage current	I_R	$AVRH$	—	500	900	μA	$AVRH = 3.3\text{ V}$
	I_{RH}	$AVRH$	—	—	5	μA	*2
Analog input equivalent capacitance	C_{SH}	AN0 to AN11	—	—	8.5	pF	
Analog input equivalent resistance	R_{IN}	AN0 to AN11	—	—	12.1	k Ω	
Offset between input channels	—	AN0 to AN11	—	—	5	LSB	

*1 : Assuming that output impedance at external analog signal source is 4.2 k Ω or less. If output impedance is more than 4.2 k Ω , it is necessary to take a long sampling time.

Set $t_{CNV} \leq t_{SMP} + t_{CMP}$ for actual use.

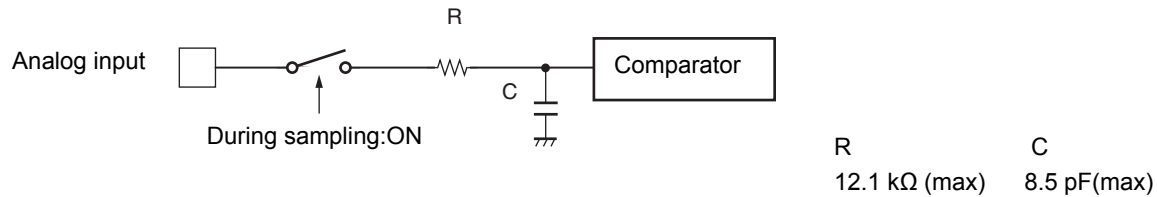
*2 : Assuming that A/D converter is inactive and power supply current is in CPU stop mode ($V_{CC3} = AV_{CC3} = AVRH = 3.3\text{ V}$)

Note:

< About the external impedance of analog input and its sampling time >

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model



Note: The values are reference values.

To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

<Countermeasure for noise which generates on reference power supply>

We recommend to put some μF of bypass capacitor into the reference power supply (AVRH pin).

<About errors>

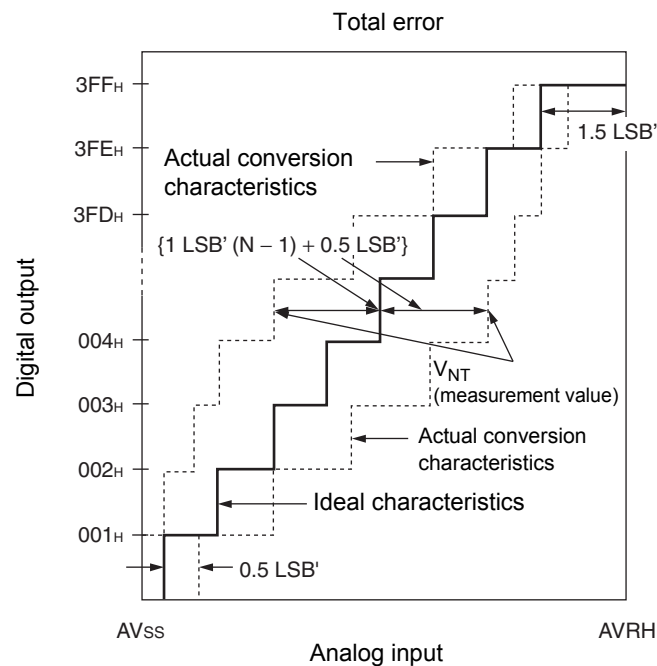
As $|\text{AVRH}-\text{AV}_{\text{SS}}|$ becomes smaller, values of relative errors grow larger.

<Other>

- When inserting a capacitor for blocking direct current between an external circuit and an input pin, set the capacitance value to approximately some thousand times of C_{SH} in order to suppress any influence by the voltage divided depending on chip's internal sampling capacitance C_{SH} .

Definition of A/D converter terms

- Resolution
Analog variation that is recognizable by the A/D converter.
- Nonlinearity error
Deviation between actual conversion characteristics and a straight line connecting the zero transition point (00 0000 0000_B ↔ 00 0000 0001_B) and the full scale transition point (11 1111 1110_B ↔ 11 1111 1111_B).
- Differential nonlinearity error
Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error
This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



$$1\text{LSB}' (\text{ideal value}) = \frac{\text{AVRH} - \text{AVSS}}{1024} \text{ [V]}$$

$$\text{Total error of digital output } N = \frac{V_{\text{NT}} - \{1\text{LSB}' \times (N - 1) + 0.5\text{LSB}'\}}{1\text{LSB}'}$$

N : A/D converter digital output value

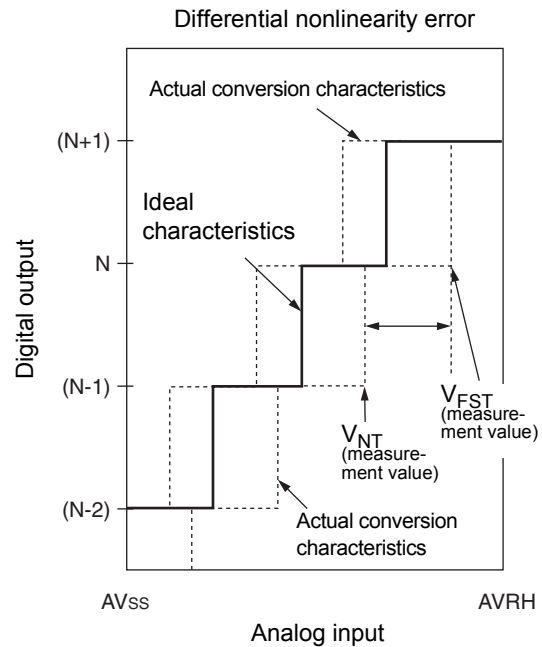
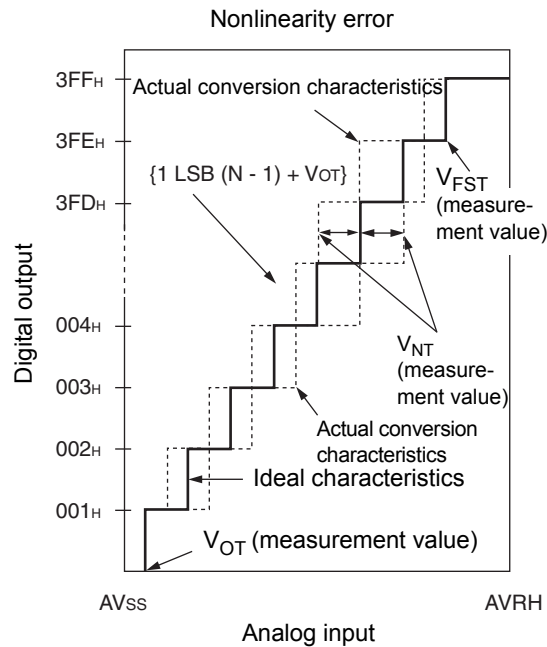
V_{OT}' (ideal value) = AV_{SS} + 0.5 LSB' [V]

V_{FST}' (ideal value) = AV_{RH} - 1.5 LSB' [V]

V_{NT} : Voltage at which the digital output changes from (N + 1) to N

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$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{ [LSB]}$$

$$1\text{LSB} = \frac{V_{EST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.

V_{FST} : Voltage at which the digital output changes from 3FE_H to 3FF_H.

14.5 FLASH memory program/erase characteristics

(T_A = + 25°C, V_{CC5} = 5.0 V, V_{CC3} = 3.3 V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.5	—	s	Erasure programming time not included
Chip erase time	—	n*0.5	—	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	—	6	—	μs	System overhead time not included
Programme/Erase cycle	10000	—	—	cycle	
Flash data retention time	10	—	—	year	*

*: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at + 85°C).

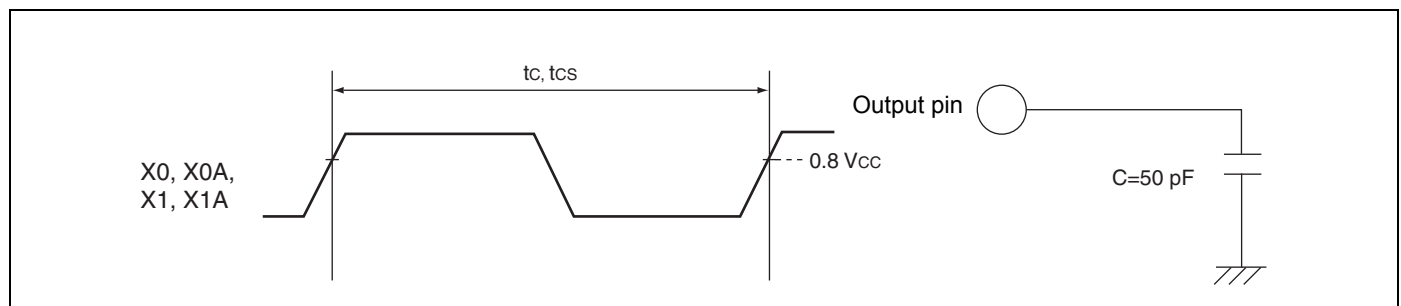
14.6 AC characteristics

14.6.1 Clock timing

($V_{CC5} = 5.0 \text{ V} \pm 10\%$, $V_{CC3} = 3.3 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.4	—	4.2	MHz	Main clock
Clock cycle time	t_C	X0 X1	238	—	294	ns	
Clock frequency	f_{CS}	X0A X1A	32	—	100	kHz	Sub clock
Clock cycle time	t_{CS}	X0A X1A	10	—	31.25	μs	
Internal operation clock frequency	f_{CP}	—	0.032	—	80	MHz	CPU
	f_{CPP}		0.032	—	20	MHz	Peripheral
	f_{CPT}		0.032	—	40	MHz	External bus
	f_{CAN}		—	—	20	MHz	Clock after division by CAN prescaler
	f_{MLB}		—	—	26	MHz	MediaLB
Internal operation clock cycle time	t_{CP}	—	12.5	—	31250	ns	CPU
	t_{CPP}		50	—	31250	ns	Peripheral
	t_{CPT}		25	—	31250	ns	External bus
	t_{CAN}		50	—	—	ns	Clock after division by CAN prescaler
	t_{MLB}		38.5	—	—	ns	MediaLB

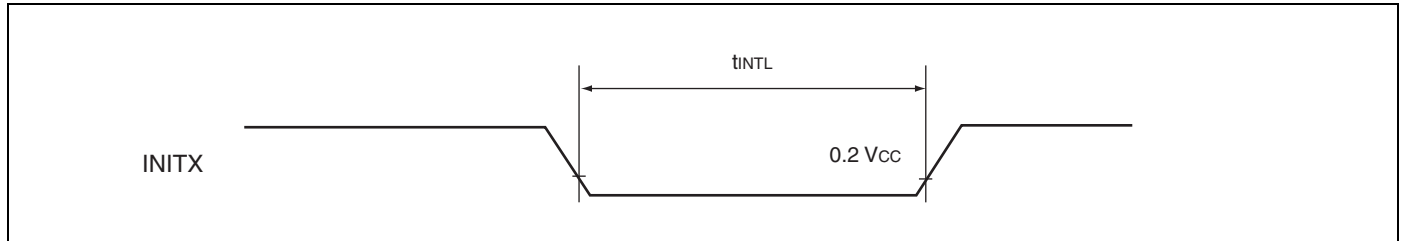
Clock timing condition



14.6.2 Reset input ratings

($V_{CC5} = 5.0 \text{ V} \pm 10\%$, $V_{CC3} = 3.3 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on, when returning from shutdown)	t_{INTL}	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	μs



14.6.3 Interrupt characteristics for recover from shutdown

($V_{CC5} = 5.0 \text{ V} \pm 10\%$, $V_{CC3} = 3.3 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Condition	Value		Unit
		Min	Max	
Interrupt input time (If using level interrupt during recover from shutdown)	—	500	—	μs

14.6.4 LIN-USART

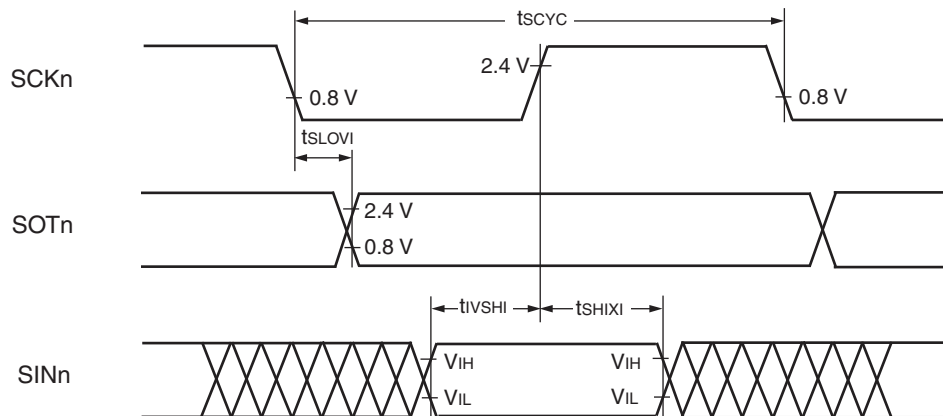
Bit setting : ESCR : SCES = 0, ECCR : SCDE = 0

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC5} = 5.0\text{ V} \pm 10\%$, $V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

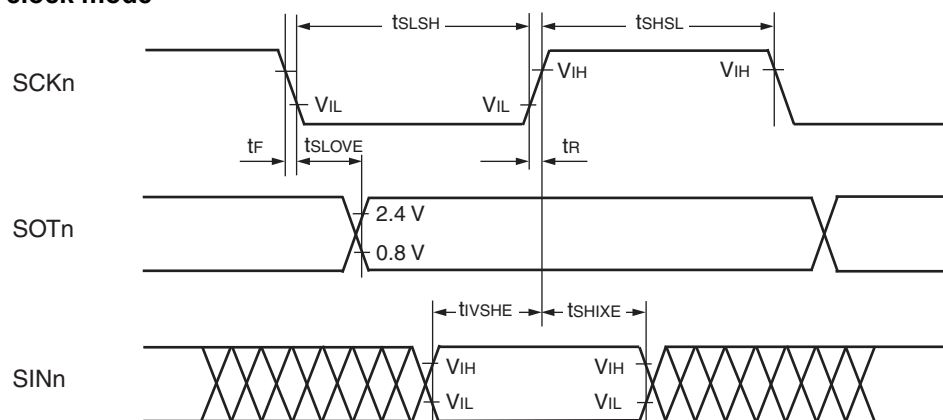
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{CP}$	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		$t_{CP} + 80$	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	ns
Serial clock "L" pulse width	t_{SHSL}	SCKn	External shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	t_{SLSH}	SCKn		$t_{CP} + 10$	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	$2 t_{CP} + 60$	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		$t_{CP} + 30$	—	ns
SCK rising time	t_F	SCKn		—	10	ns
SCK falling time	t_R	SCKn		—	10	ns

- Notes:
- AC characteristic in CLK synchronized mode.
 - C_L is the load capacity of a pin during testing.
 - t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).

Internal shift clock mode



External shift clock mode



Bit setting : ESCR : SCES = 1, ECCR : SCDE = 0

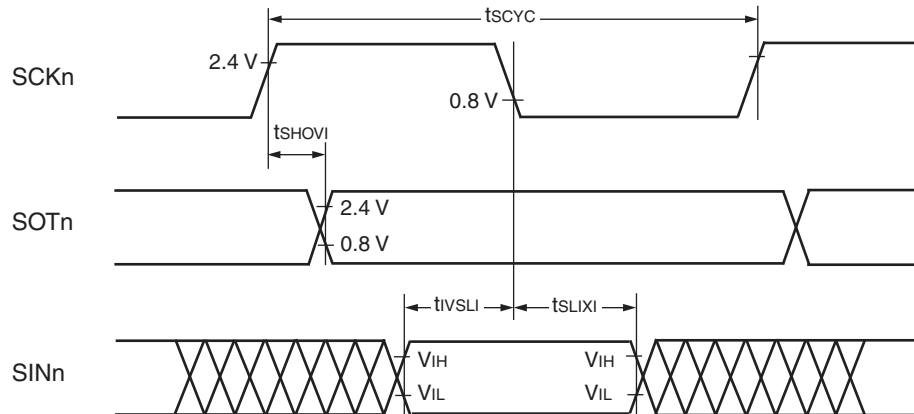
($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC5} = 5.0\text{ V} \pm 10\%$, $V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCKn, SOTn		- 50	+ 50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLI}	SCKn, SINn		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCKn, SINn		0	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn	External shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$	$3 t_{CP} - t_R$	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn		$t_{CP} + 10$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVE}	SCKn, SOTn		—	$2 t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLE}	SCKn, SINn		30	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXE}	SCKn, SINn		$t_{CP} + 30$	—	ns
SCK rise	t_F	SCKn		—	10	ns
SCK fall	t_R	SCKn		—	10	ns

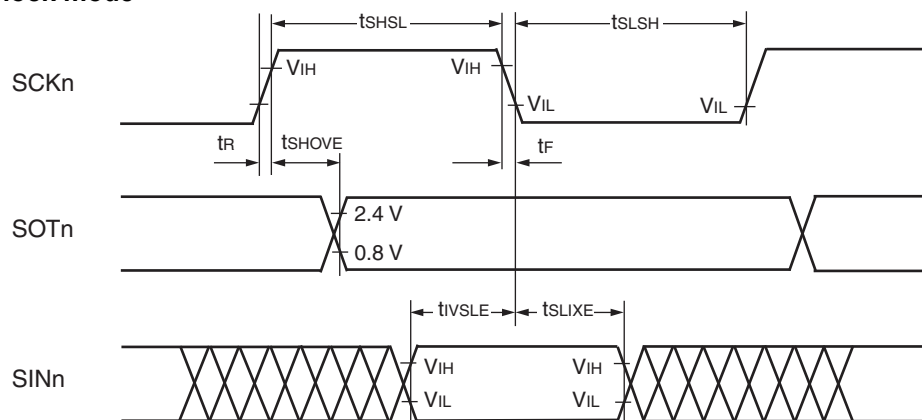
Notes: • C_L is the load capacity of a pin during testing.

• t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).

Internal shift clock mode



External shift clock mode

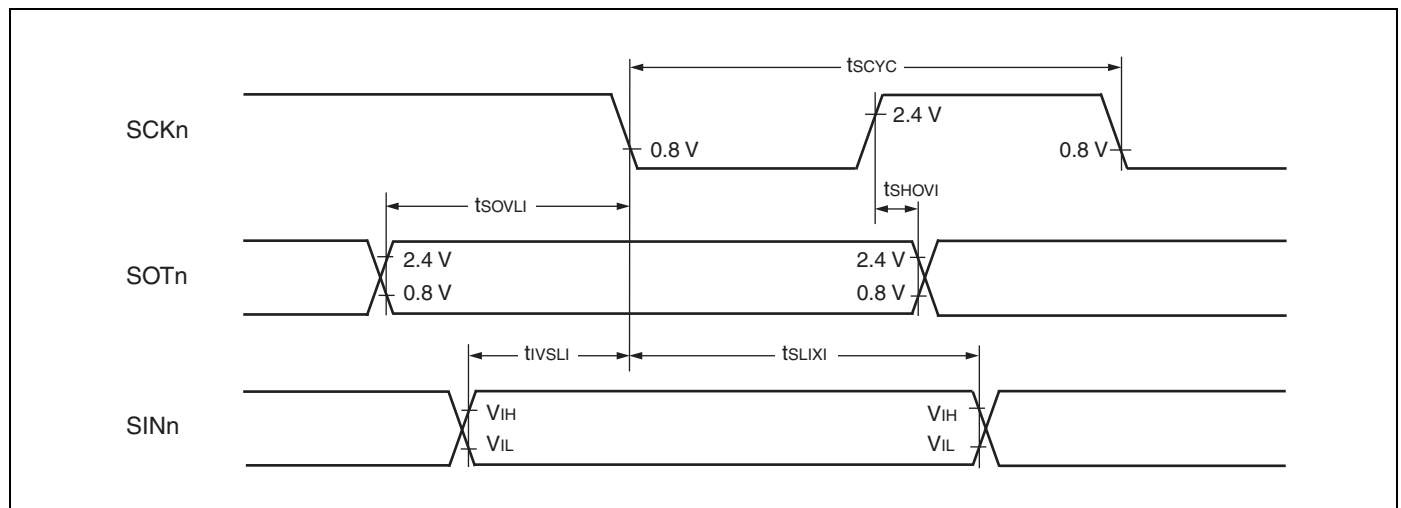


Bit setting:ESCR:SCES = 0, ECCR:SCDE = 1

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC5} = 5.0\text{ V} \pm 10\%$, $V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCKn, SOTn		- 50	+ 50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLI}	SCKn, SINn		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCKn, SINn		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	t_{SOVLI}	SCKn, SOTn		$3 t_{CP} - 70$	—	ns

- Notes:
- C_L is the load capacity of a pin during testing.
 - t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).



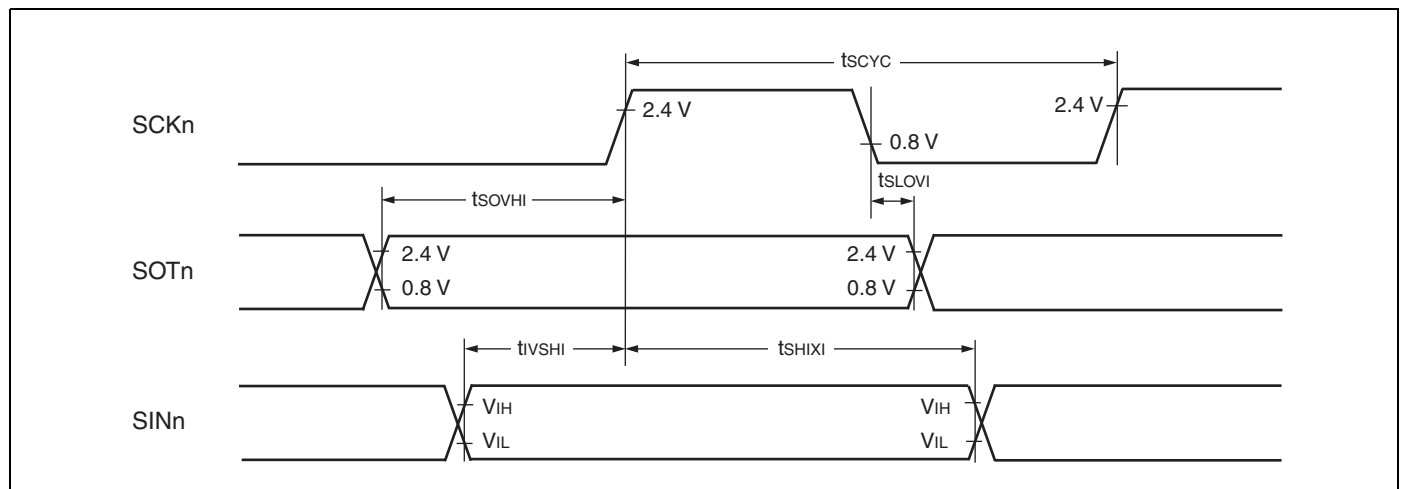
Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC5} = 5.0\text{ V} \pm 10\%$, $V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCKn, SOTn		- 50	+ 50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCKn, SINn		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN delay time	t_{SHIXI}	SCKn, SINn		0	—	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	t_{SOVHI}	SCKn, SOTn		$3 t_{CP} - 70$	—	ns

Notes: • C_L is the load capacity of a pin during testing.

• t_{CP} indicates the peripheral clock (CLKP) cycle time (Unit : ns).

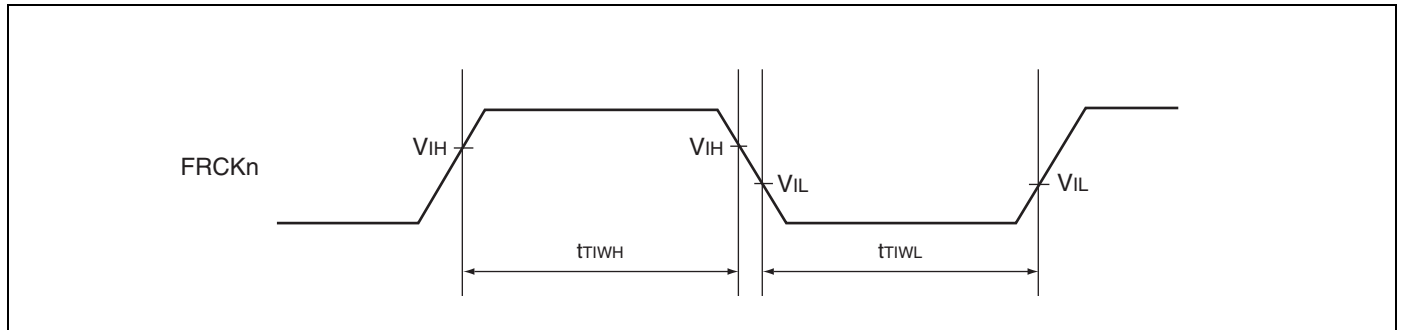


14.6.5 Free-run timer clock

($V_{CC5} = 5.0\text{ V} \pm 10\%$, $V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	FRCKn	—	$4t_{CLKP}$	—	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.

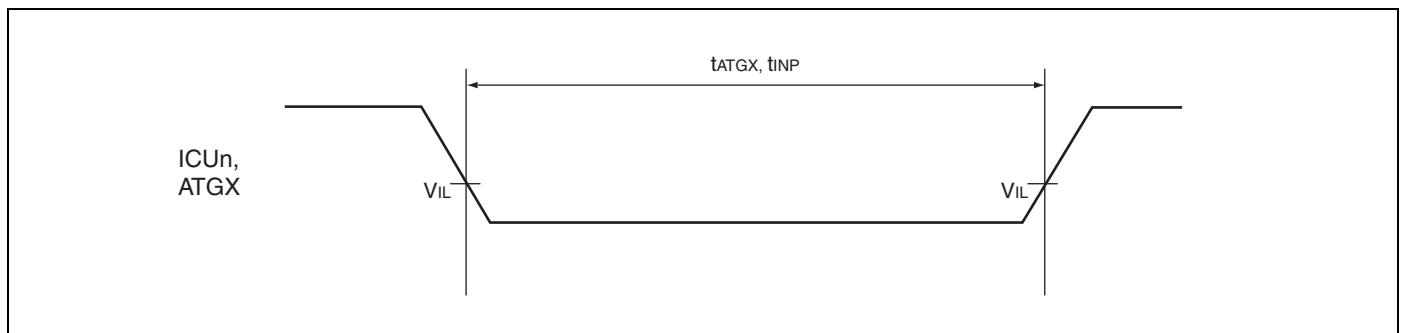


14.6.6 Trigger input timing

($V_{CC5} = 5.0\text{ V} \pm 10\%$, $V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

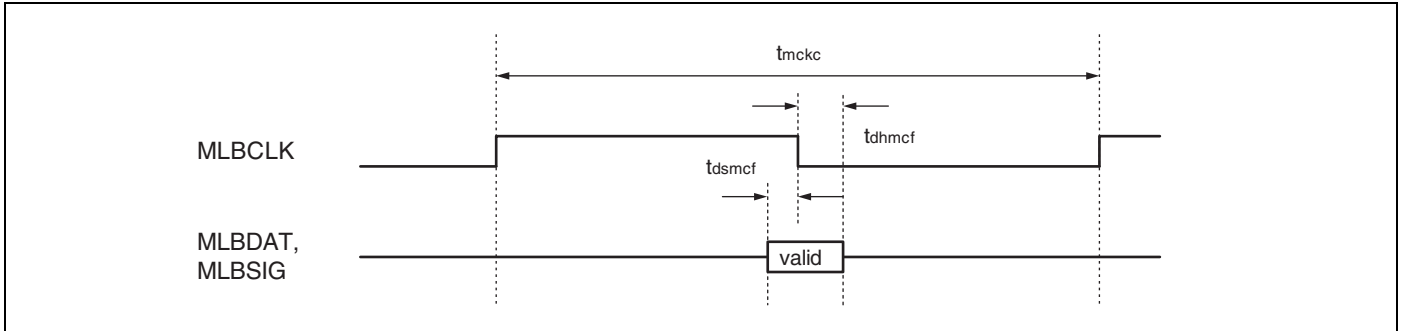
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.



MediaLB AC characteristics

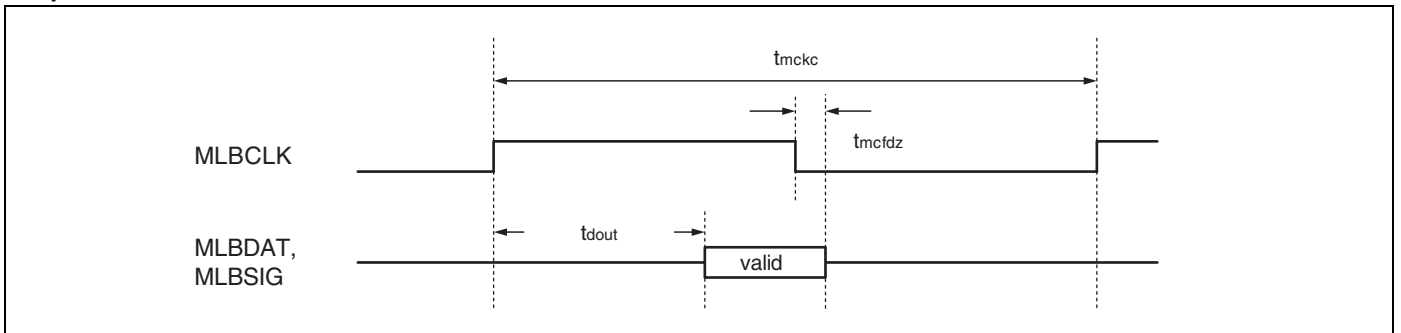
Input



($V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	—	—	40	—	ns	
MLBSIG, MLBDAT input setup	t_{dsmcf}	MLBSIG MLBDAT	—	1	—	—	ns	
MLBSIG, MLBDAT input hold	t_{dhmcf}	MLBSIG MLBDAT	—	4	—	—	ns	

Output



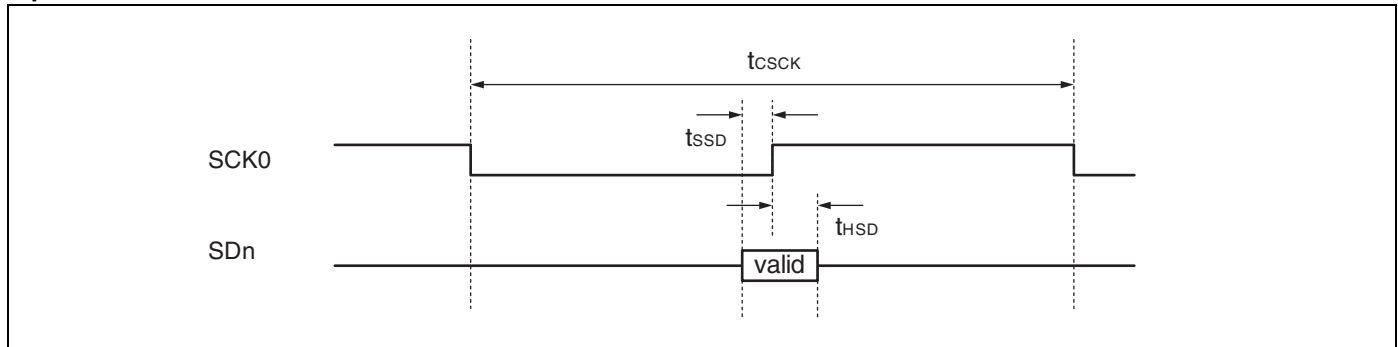
($V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	—	—	40	—	ns	
MLBSIG, MLBDAT output stop	t_{mcfdz}	MLBSIG MLBDAT	—	0	—	—	ns	
MLBSIG, MLBDAT output delay	t_{dout}	MLBSIG MLBDAT	—	—	—	11	ns	

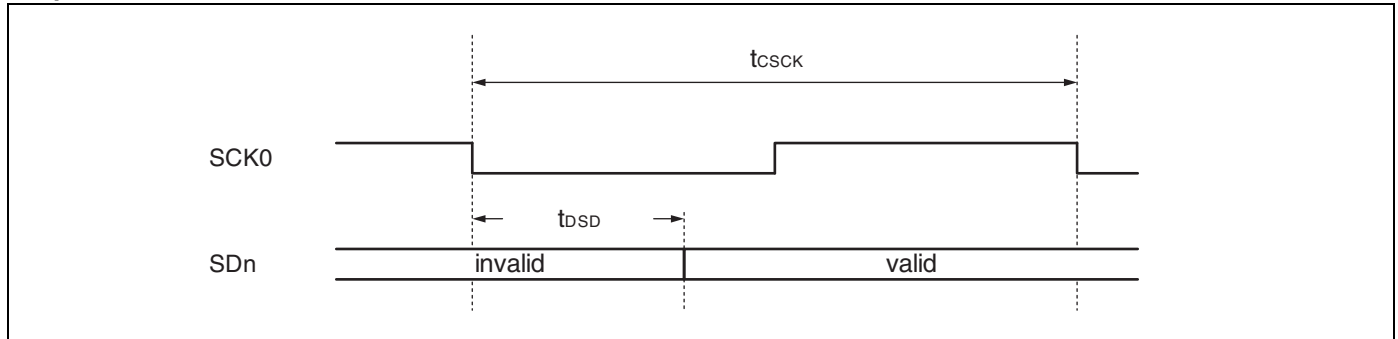
Note: Addition capacity 50 pF

I²S AC characteristics

Input



Output



($V_{CC3} = 3.3 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
SCK cycle	t_{CSSK}	SCK0	—	651	—	—	ns	
SD input setup	t_{SSD}	SDn	—	50	—	—	ns	
SD input hold	t_{HSD}	SDn	—	50	—	—	ns	
SD output delay	t_{DSD}	SDn	—	—	—	50	ns	

Note: Addition capacity 50 pF

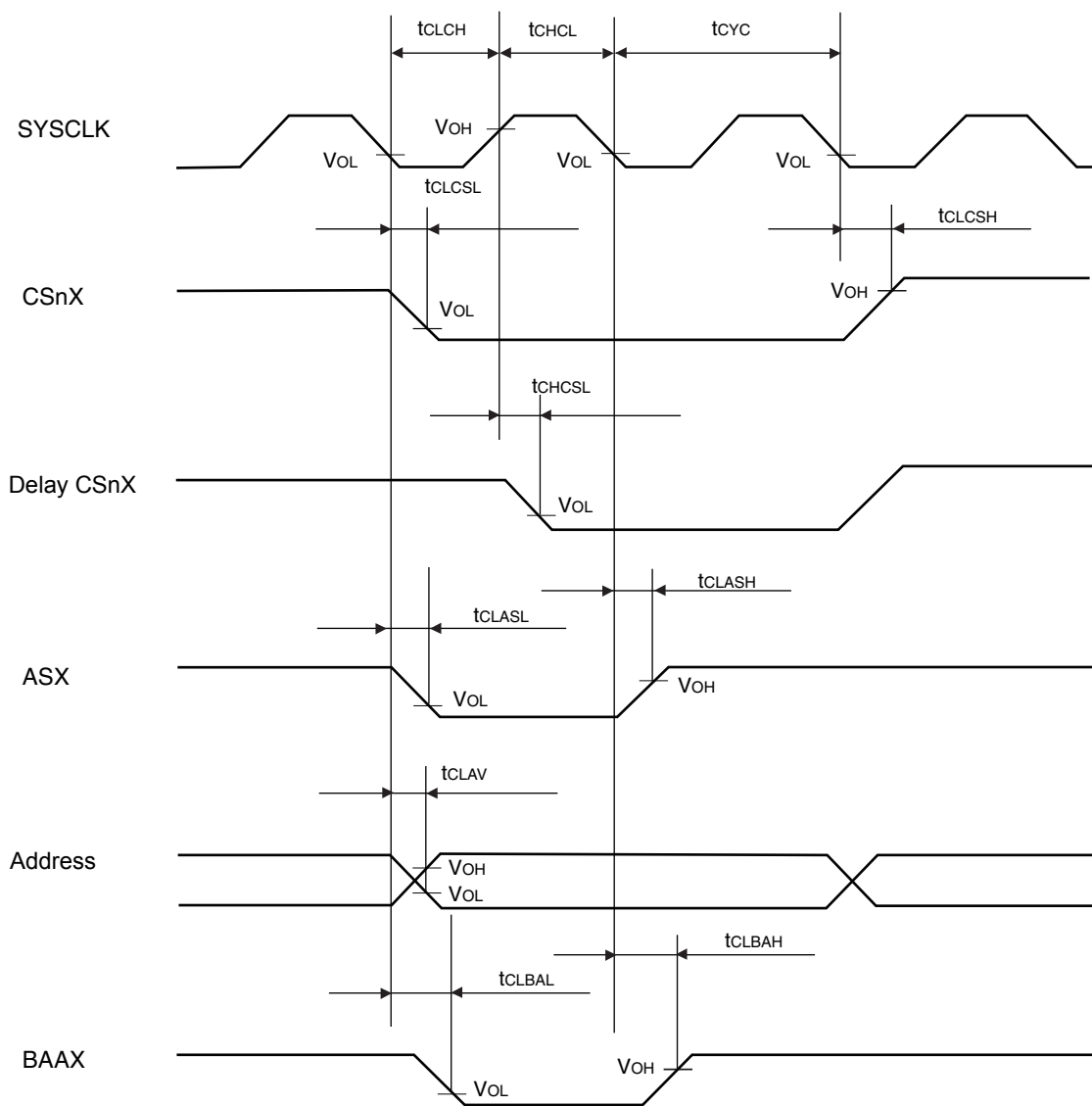
14.6.7 External Bus AC Timings

Basic Timing

(Vcc3 = 3.3 V ± 10%, Vss = 0.0 V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK	t _{CLCH}	SYSCLK	—	—	t _{CLKT} / 2	—	ns
	t _{CHCL}			—	t _{CLKT} / 2	—	
SYSCLK ↓ →CSnX delay	t _{CLCSL}	SYSCLK CSnX		− 6	—	+ 6	
	t _{CLCSH}			− 6	—	+ 6	
SYSCLK ↑ →CSnX delay when using CS delay function	t _{CHCSL}			− 6	—	+ 6	
SYSCLK ↓ →ASX delay	t _{CLASL}	SYSCLK ASX		− 6	—	+ 6	
	t _{CLASH}			− 6	—	+ 6	
SYSCLK ↓ →BAAX delay	t _{CLBAL}	SYSCLK BAAX		− 6	—	+ 6	
	t _{CLBAH}			− 6	—	+ 6	
SYSCLK ↓ →address output delay	t _{CLAV}	SYSCLK A23 to A00		− 6	—	+ 6	

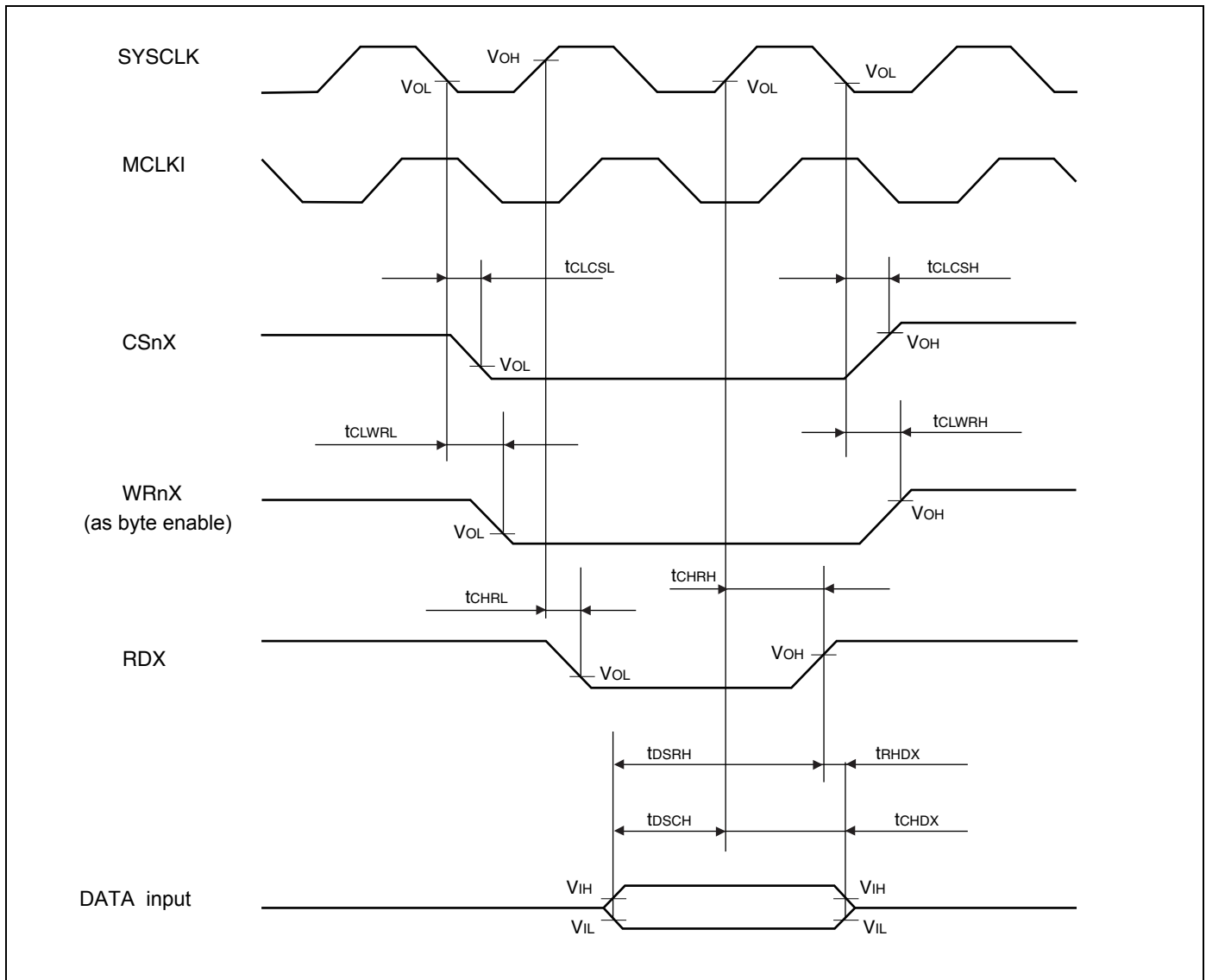
Note: t_{CLKT} is the cycle time of the external bus clock.



Read access

(V_{CC3} = 3.3 V ±10%, V_{SS} = 0.0 V, T_A = -40°C to +105°C)

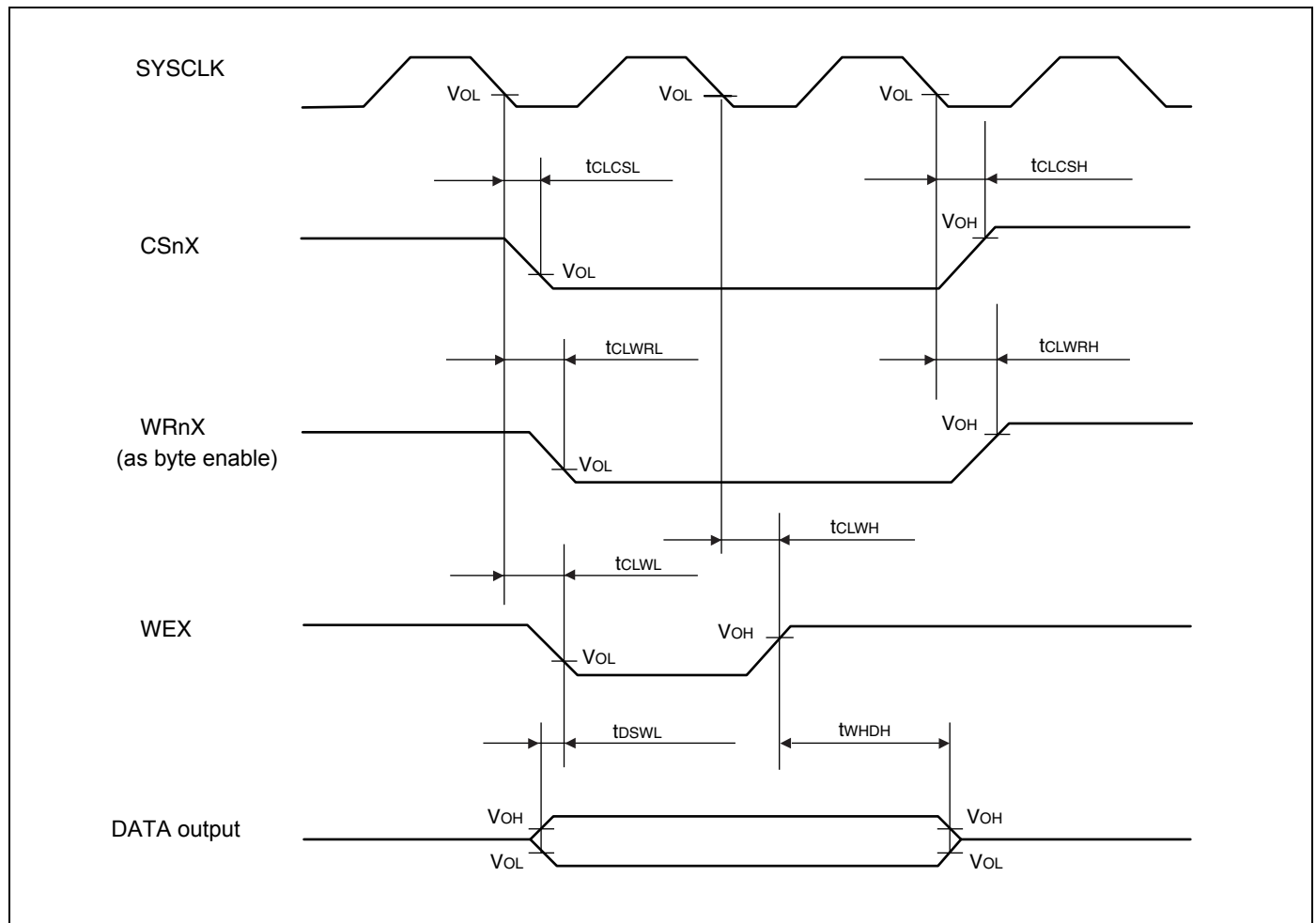
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↑ → RDX delay	t _{CHRL}	SYSCLK RDX	—	− 6	—	+ 6	ns
	t _{CHRH}			− 6	—	+ 6	
Data Valid → RDX ↑ setup	t _{DSRH}	RDX D31 to D16		30	—	—	
RDX ↑ → Valid data hold	t _{RHDX}	RDX D31 to D16		0	—	—	
Data Valid → SYSCLK ↑ setup	t _{DSCH}	MCLKI D31 to D16		6	—	—	
SYSCLK ↑ → Valid data hold	t _{CHDX}	MCLKI D31 to D16		6	—	—	
SYSCLK ↓ → WRnX delay (as byte enable)	t _{CLWRL}	MCLKO WRnX		—	3	—	
	t _{CLWRH}			—	3	—	
SYSCLK ↓ → CSnX delay	t _{CLCSL}	MCLKO CSnX		− 6	—	+ 6	
	t _{CLCSH}			− 6	—	+ 6	



Synchronous write access – Byte control type

($V_{CC3} = 3.3 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

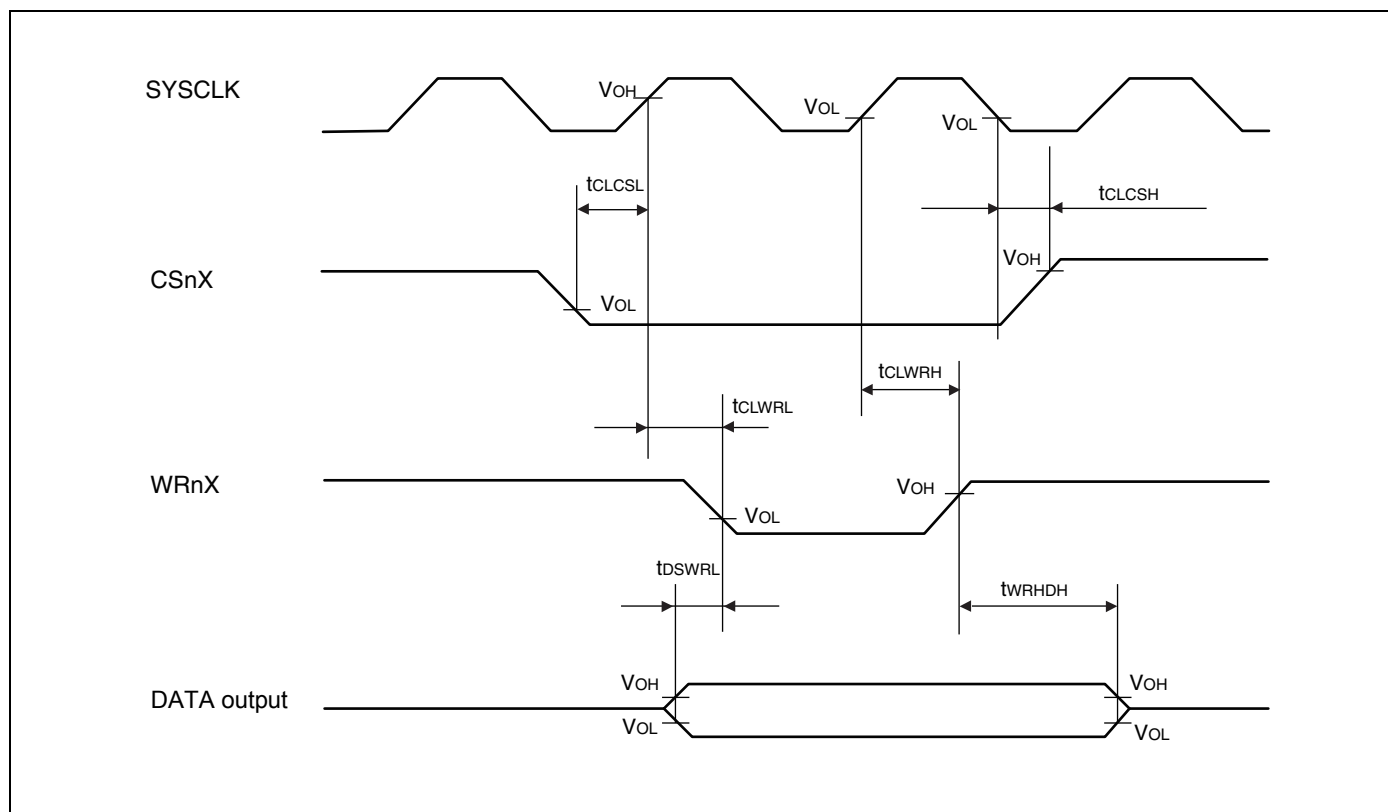
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK $\downarrow \rightarrow$ WEX delay	t_{CLWL}	SYSCLK	—	- 6	—	+ 6	ns
	t_{CLWH}	WEX		- 6	—	+ 6	
Data Valid $\rightarrow$ WEX $\downarrow$ setup	t_{DSWL}	WEX D31 to D16		—	0	—	
WEX $\uparrow \rightarrow$ Valid data hold	t_{WHDH}	WEX D31 to D16		—	t_{CLKT}	—	
SYSCLK $\downarrow \rightarrow$ WRnX delay (as byte enable)	t_{CLWRL}	SYSCLK		—	3	—	
	t_{CLWRH}	WRnX		—	3	—	
SYSCLK $\downarrow \rightarrow$ CSnX delay	t_{CLCSL}	SYSCLK		- 6	—	+ 6	
	t_{CLCSH}	CSnX		- 6	—	+ 6	



Synchronous write access – Non-byte control type

(V_{cc3} = 3.3 V ±10%, V_{ss} = 0.0 V, T_A = –40°C to +105°C)

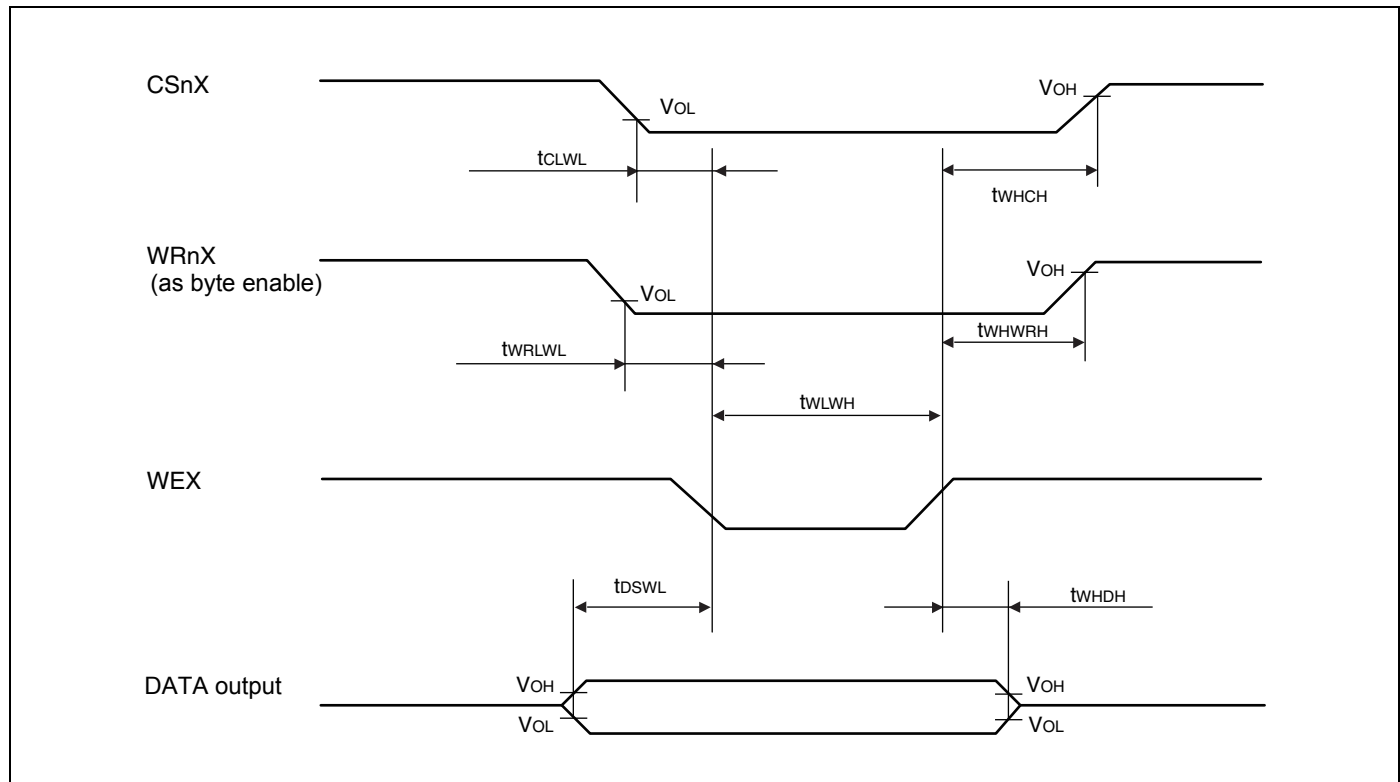
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↑ → WRnX delay	t _{CLWRL}	SYSCLK WEX	—	– 6	—	+ 6	ns
	t _{CLWRH}			– 6	—	+ 6	
Data Valid → WRnX ↓ setup	t _{DSWRL}	WEX D31 to D16		—	0	—	
WRnX ↑ → Valid data hold	t _{WRHDH}	WEX D31 to D16		—	t _{CLKT}	—	
SYSCLK ↓ → CSnX delay	t _{CLCSL}	SYSCLK CSnX		– 6	—	+ 6	
	t _{CLCSH}			– 6	—	+ 6	



Asynchronous write access – Byte control type

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = –40°C to +105°C)

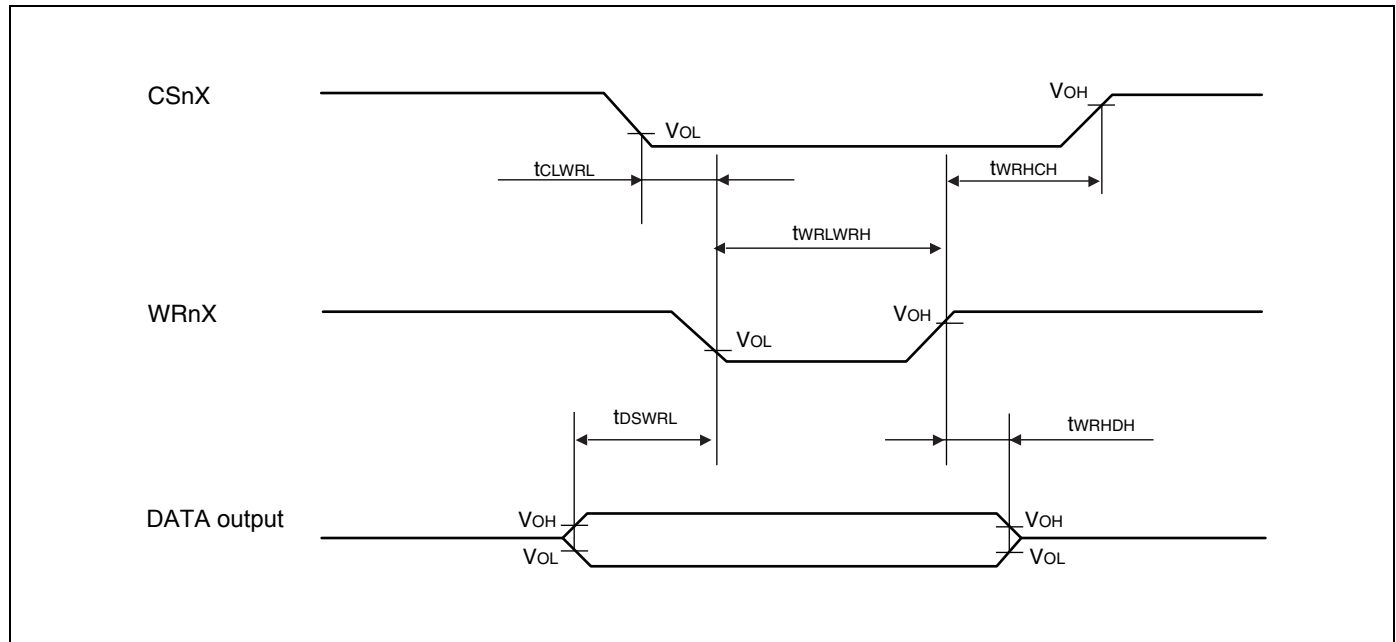
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
WEX ↓ → WEX ↑ pulse width	t _{WLWH}	WEX	—	—	t _{CLKT}	—	ns
Data Valid → WEX ↓ setup	t _{DSWL}	WEX D31 to D16		—	t _{CLKT} / 2	—	
WEX ↑ → Valid data hold	t _{WHDH}	WEX D31 to D16		—	t _{CLKT} / 2	—	
WEX → WRnX delay	t _{WRLWL}	WEX WRnX		—	t _{CLKT} / 2	—	
	t _{WHWRH}	WRnX		—	t _{CLKT} / 2	—	
WEX → CSnX delay	t _{CLWL}	WEX CSnX		—	t _{CLKT} / 2	—	
	t _{WHCH}	CSnX		—	t _{CLKT} / 2	—	



Asynchronous write access – Non-byte control type

(V_{CC3} = 3.3 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +105°C)

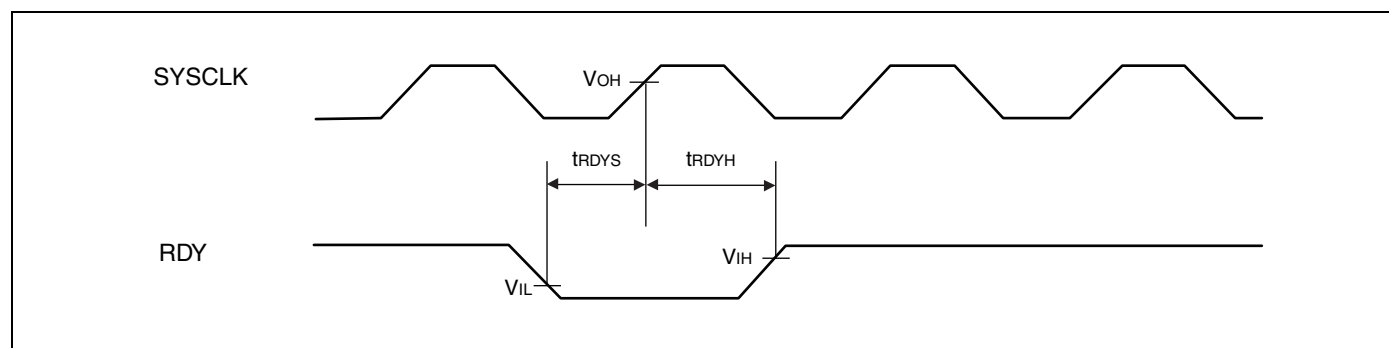
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
WRnX ↓ →WRnX ↑ pulse width	t _{WRLWRH}	WRnX	—	—	t _{CLKT}	—	ns
Data Valid →WRnX ↓ setup	t _{DSWRL}	WRnX D31 to D16		—	t _{CLKT} / 2	—	
WRnX ↑ →Valid data hold	t _{WRHCH}	WRnX D31 to D16		—	t _{CLKT} / 2	—	
WRnX→CSnX delay	t _{CLWRL}	WRnX CSnX		—	t _{CLKT} / 2	—	
	t _{WRHCH}			—	t _{CLKT} / 2	—	



RDY wait cycle insertion

($V_{CC3} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	t_{RDYS}	SYSCLK RDY	40	—	ns
RDY hold time	t_{RDYH}	SYSCLK RDY	0	—	ns



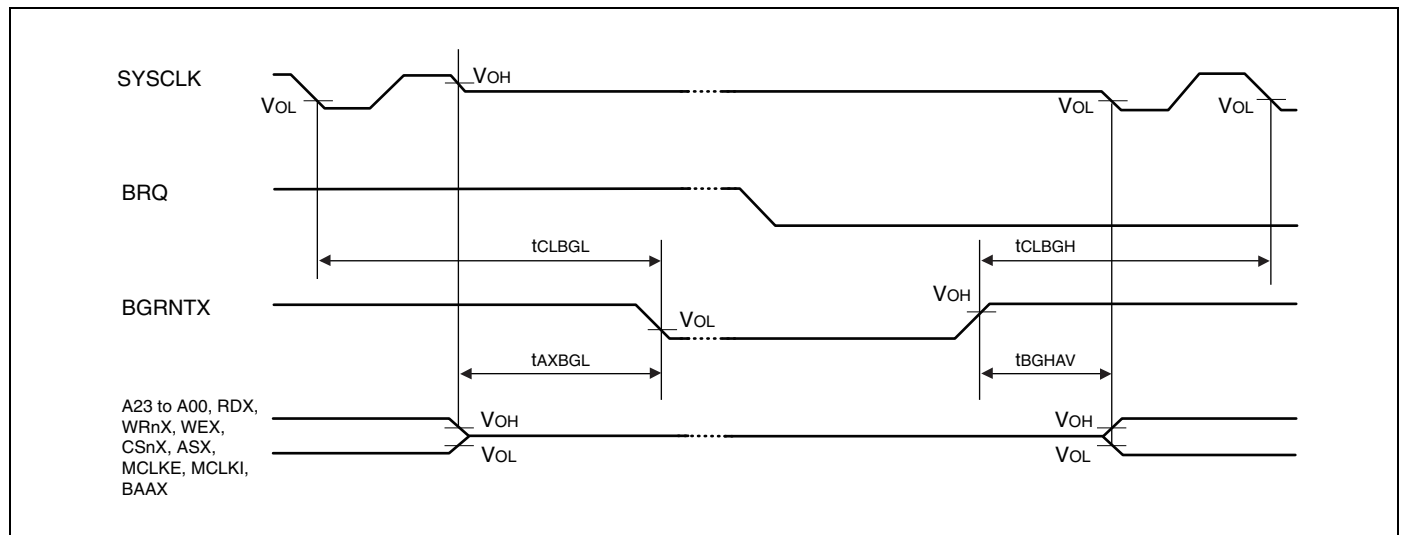
Bus hold timing

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = -40°C to +105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↓ →BGRNTX delay	t _{CLBGL}	SYSCLK BGRNTX	—	—	2 × t _{CLKT}	—	ns
	t _{CLBGH}				2 × t _{CLKT}		
Bus High-Z→BGRNTX ↓	t _{AXBGL}	BGRNTX MCLKE, MCLKI		—	t _{CLKT}	—	
	t _{BGHAV}	A23 to A00 RDX, ASX WRnX, WEX CSnX, BAAX		—	t _{CLKT}		

Note: Keep BRQ high until bus is enabled (recognized by the falling edge of BGRNTX). Keep BRQ high during the bus retention period.

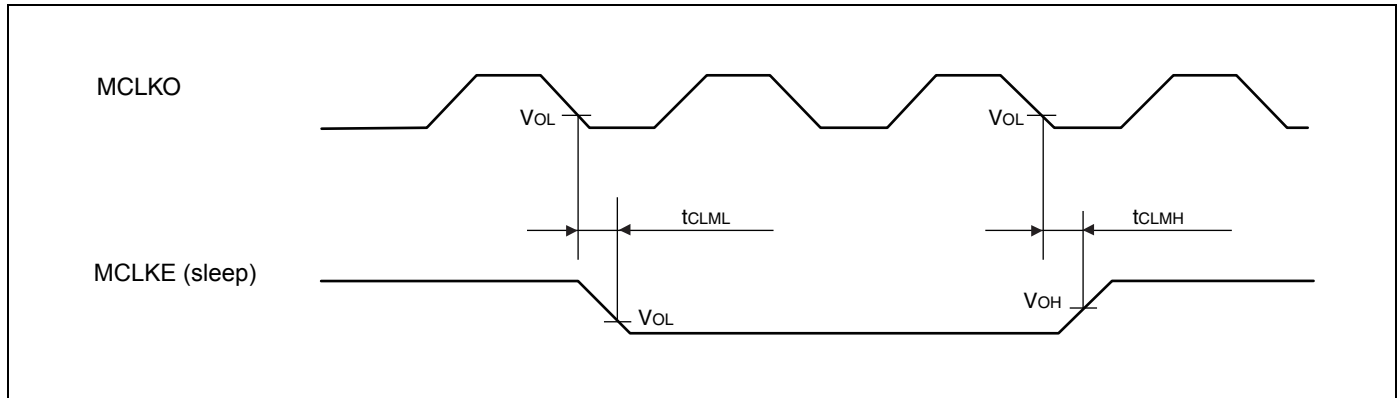
The rising edge of BGRNTX recognizes whether bus is enabled after releasing the bus (setting BRQ to Low).



Correlation of clock

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = -40°C to +105°C)

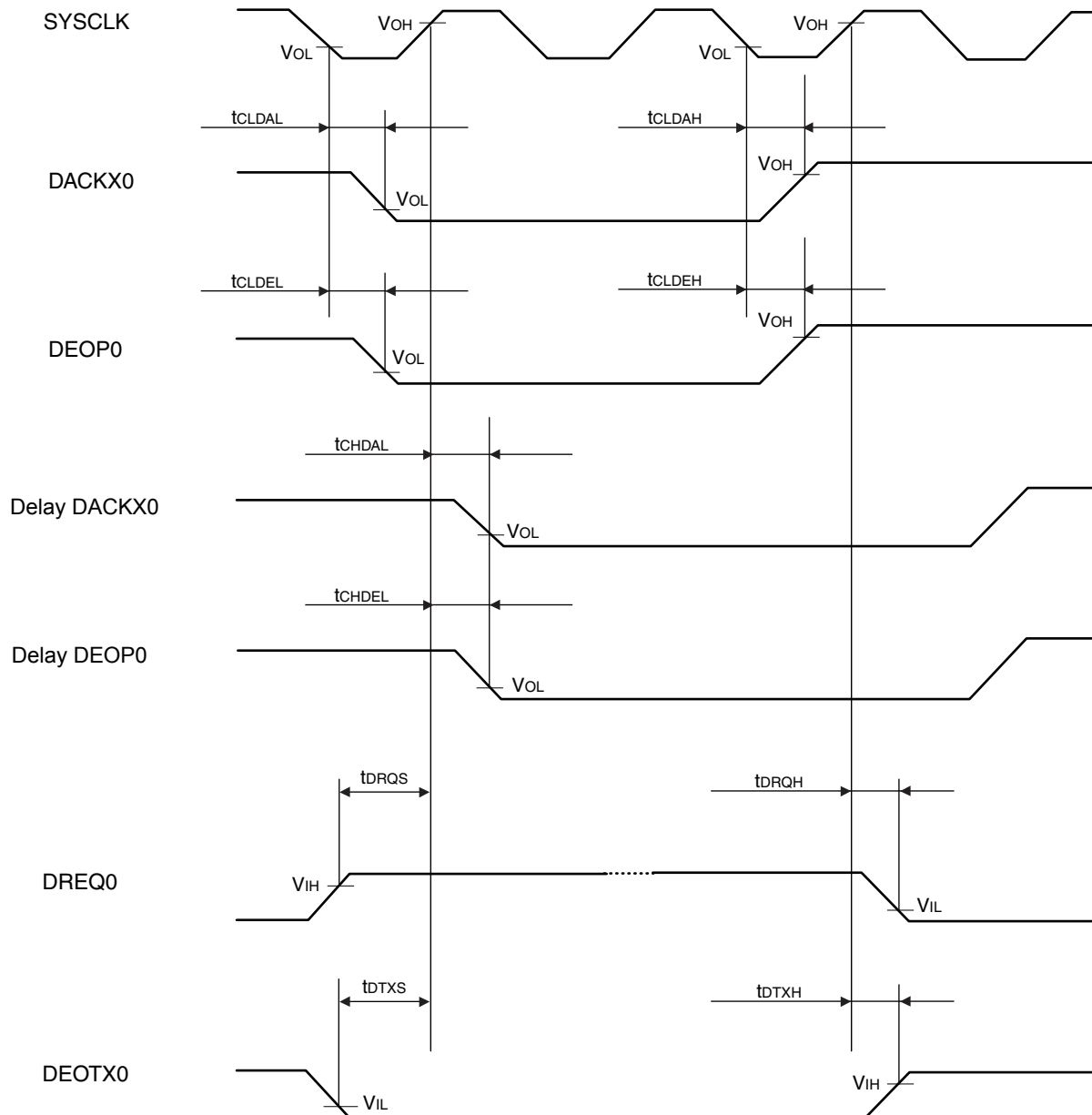
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
MCLKO ↓ → MCLKE (sleep mode)	t _{CLML}	MCLKO	—	—	3	—	ns
	t _{CLMH}	MCLKE		—	3	—	



DMA transfer

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = -40°C to +105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↓ → DACKX0 delay	t _{CLDAL}	SYSCLK	—	—	3	—	ns
	t _{CLDAH}	DACKX0		—	3	—	
SYSCLK ↓ → DEOP0 delay	t _{CLDEL}	SYSCLK		—	3	—	
	t _{CLDEH}	DEOP0		—	3	—	
SYSCLK ↑ → DACKX0 delay (when using CS delay function)	t _{CHDAL}	SYSCLK		—	3	—	
SYSCLK ↑ → DEOP0 delay (when using CS delay function)	t _{CHDEL}	SYSCLK		—	3	—	
DREQ0 SETUP	t _{DRQS}	SYSCLK		—	40	—	
DREQ0 hold	t _{DRQH}	SYSCLK		—	0	—	
DEOTX0 SETUP	t _{DTXS}	SYSCLK	—	—	40	—	ns
DEOTX0 hold	t _{DTXH}	DEOTX0		—	0	—	

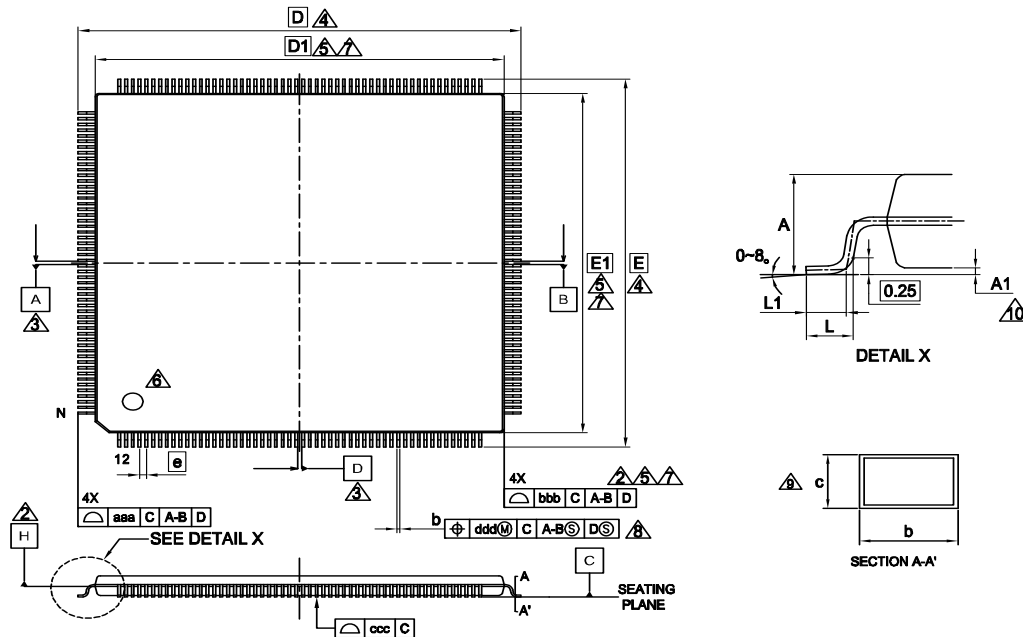


15. Ordering Information

Part number	Package	Remarks
MB91F467MAPMC-GSE2 MB91F467MAPMC-GSE1	216-pin plastic QFP (LQQ216)	Lead-free package

16. Package Dimension

LQQ216 , 216 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQQ216		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.13	0.18	0.23
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.40 BSC.		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.07
N	216		

NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

17. Main Changes

Spansion Publication Number: DS07-16613-3E

Page	Section	Change Results
83	Interrupt Vector Table	Corrected the column of interrupt and RN in interrupt number 89 to 91 as follows; Interrupt: I ² S EVEN → I ² S ERROR / RN: 125 → None Interrupt: I ² S ODD → I ² S EVEN / RN: 126 → 125 Interrupt: I ² S error → I ² S ODD / RN: None → 126

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB91460M Series FR60 32-bit Microcontroller Document Number: 002-04615				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	05/18/2010	Migrated to Cypress and assigned document number 002-04615. No change to document contents or format.
*A	5210835	AKIH	05/18/2016	Updated to Cypress format.

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