

## CY8CPROTO-062S3-4343W PSoC 62S3 Wi-Fi BT Prototyping Kit Baseboard

CONTENTS	
PAGE	DESCRIPTION
01	Title Page
02	Block Diagram
03	Power Supply (1)
04	Power Supply (2)
05	KitProg3
06	Carrier Module Power
07	Carrier Module Signals
08	Interfaces and Peripherals
09	Peripherals and Accessories
10	Revision History

### Drawing Numbers

PCBA	121-60562-01
PCB	600-60562-01
FAB DRW	610-60562-01
ASSY DRW	620-60562-01
SCH DRW	630-60562-01



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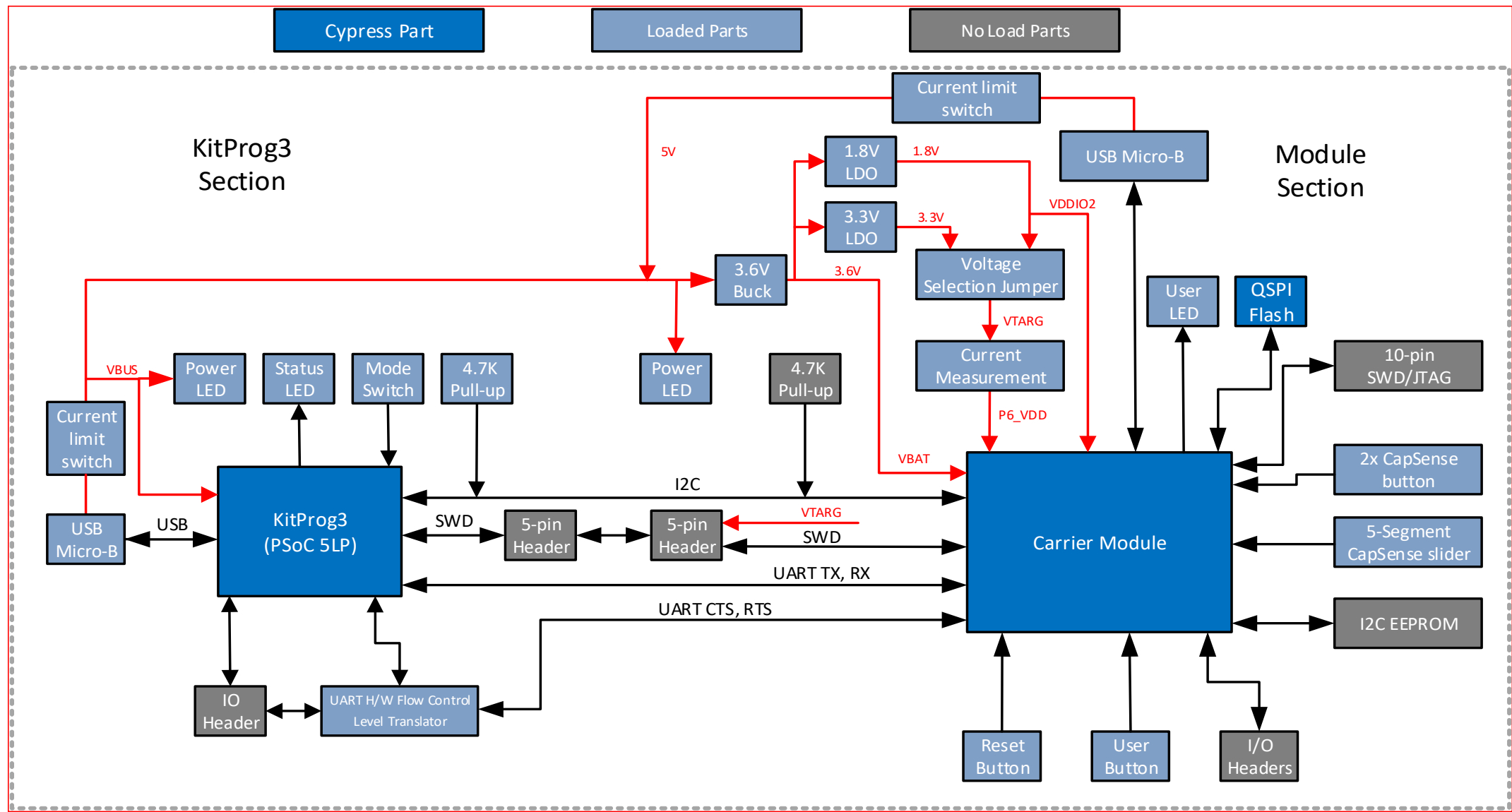
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**SCH Title : PSoC 62S3 Wi-Fi BT Prototyping Baseboard**

**Page Title : Title Page**

Size A4	Document Number <b>630-60562-01</b>	Drawn By <b>TARE</b>	Approved By <b>RKAD</b>	Rev <b>03</b>
Date:	Thursday, September 19, 2019		Sheet	1 of 10



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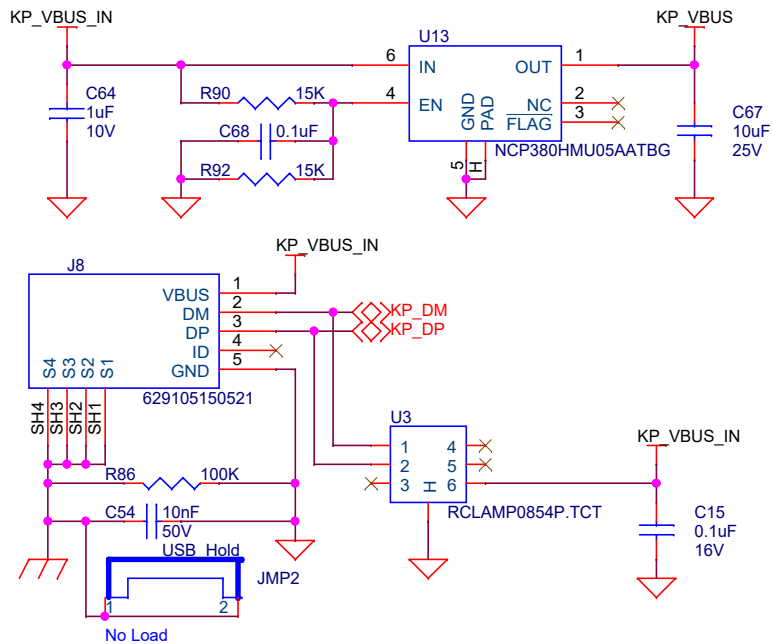
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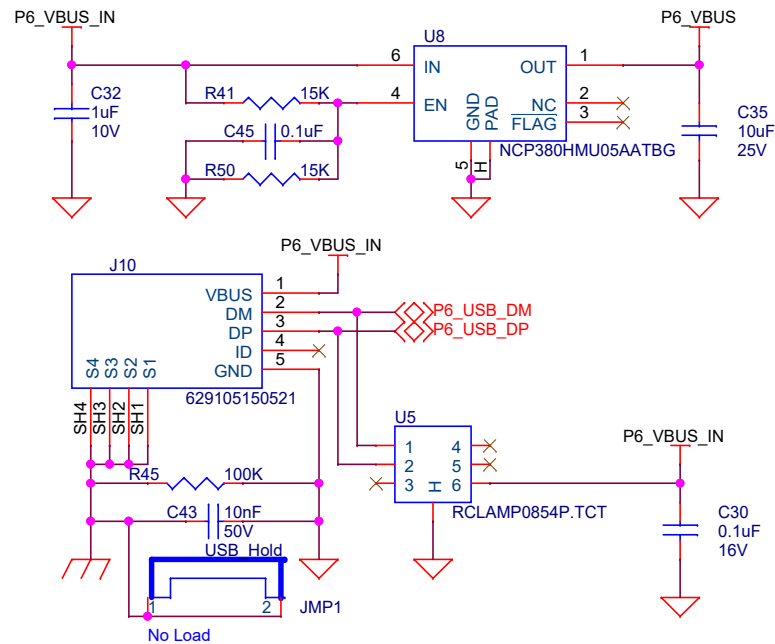
**Page Title : Block Diagram**

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Date:	Thursday, September 19, 2019		Sheet	2 of 10

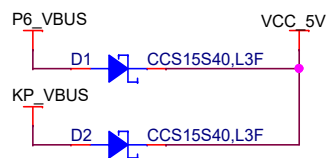
### KitProg3 USB Micro-B connector



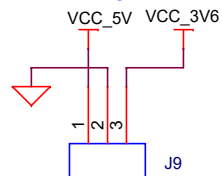
### PSoC 6 MCU USB Device Micro-B connector



### Input Supply

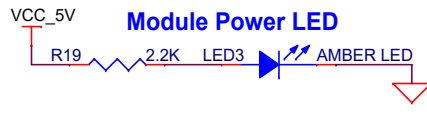


### Input Supply Header

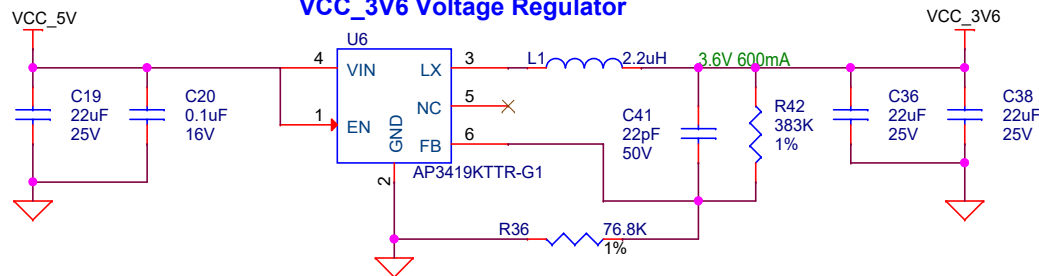


Note: Remove L1 to disable on-board supply.

### Module Power LED



### VCC\_3V6 Voltage Regulator



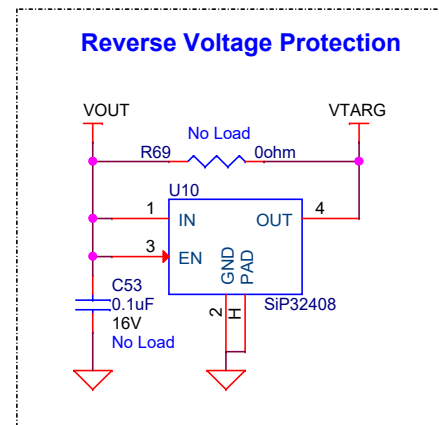
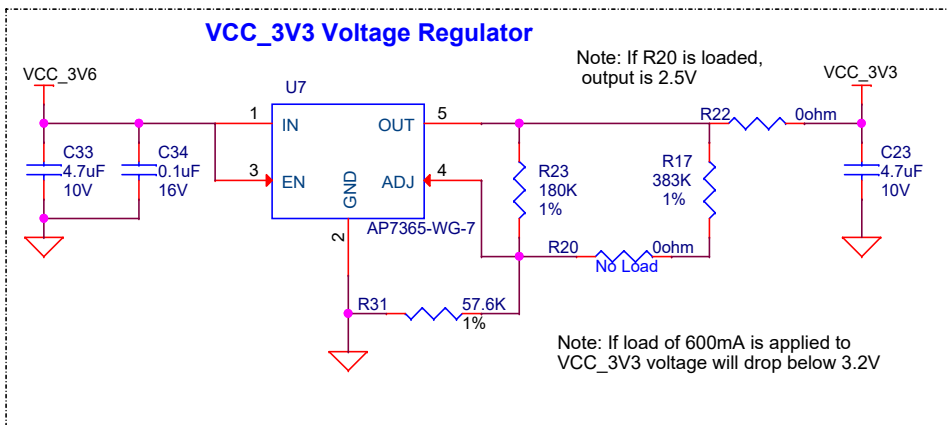
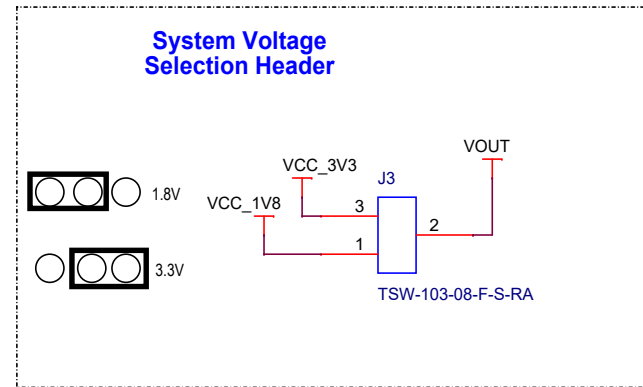
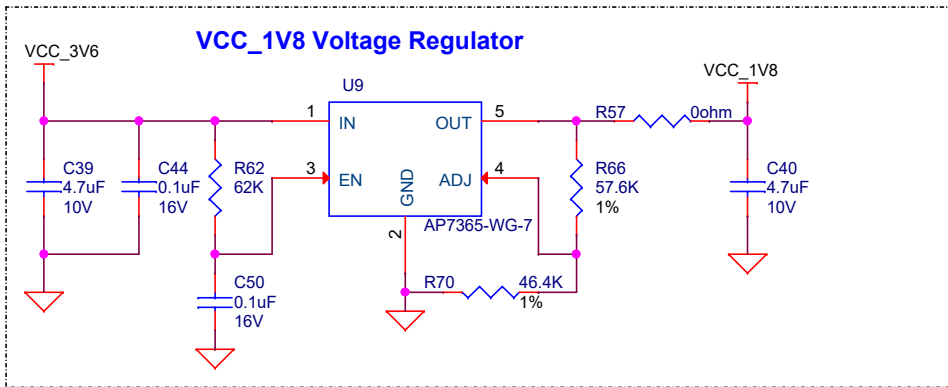
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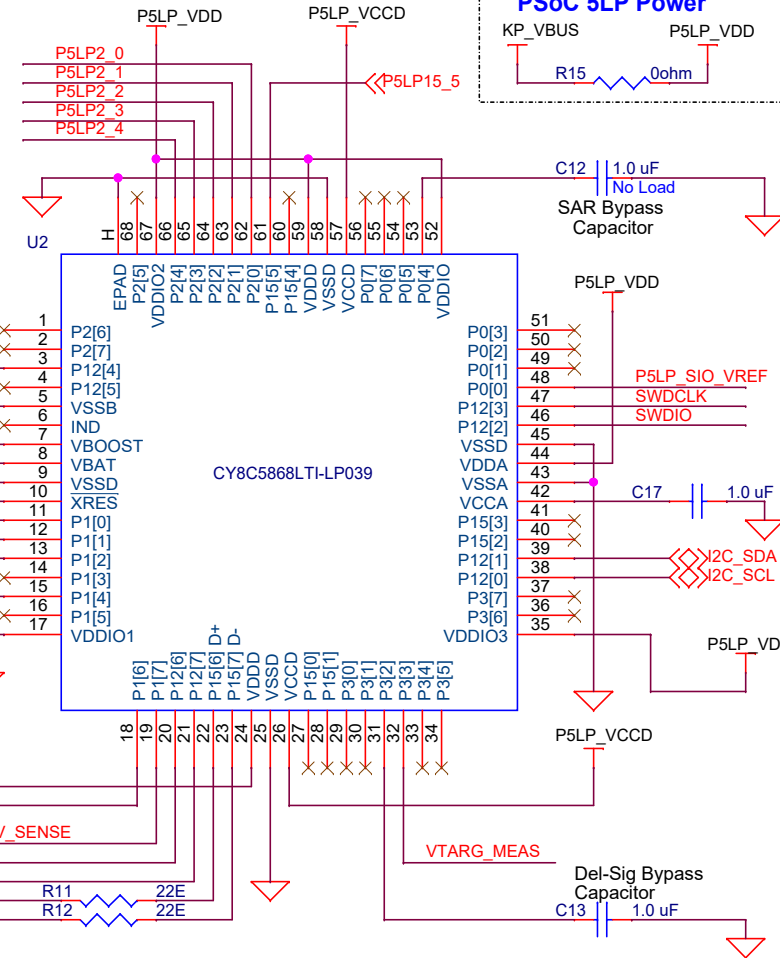
**SCH Title : PSoC 62S3 Wi-Fi BT Prototyping Baseboard**

**Page Title : Power Supply (1)**

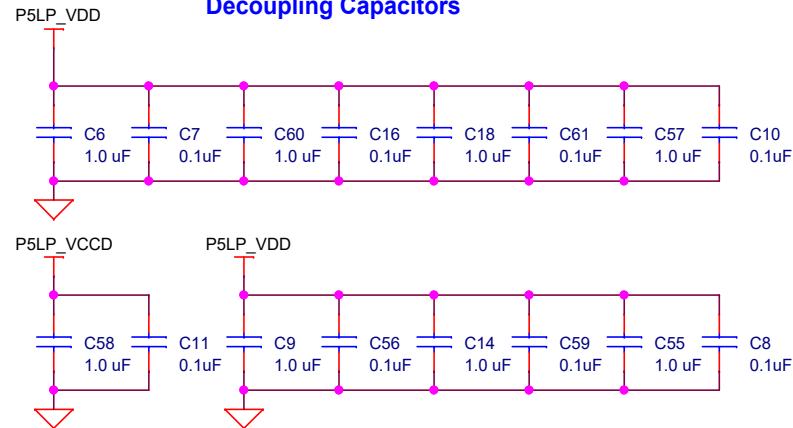
Size A4	Document Number <b>630-60562-01</b>	Drawn By <b>TARE</b>	Approved By <b>RKAD</b>	Rev <b>03</b>
Date:	Thursday, September 19, 2019		Sheet	3 of 10



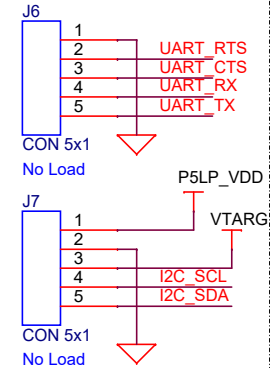
## PSoC 5LP based KitProg3



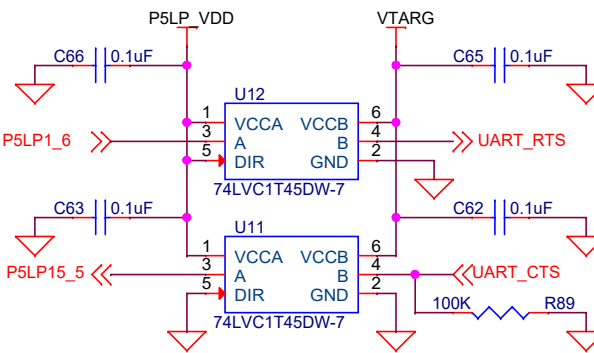
## Decoupling Capacitors



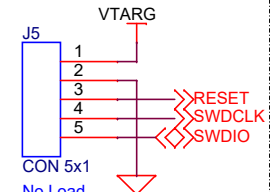
## KitProg3 I/O Connectors



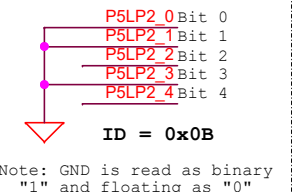
## UART H/W Flow Control Level Translator



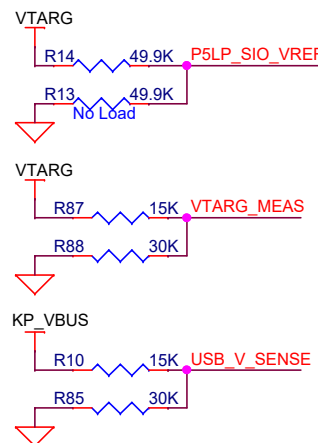
## Target Program/Debug Connector



## KitProg3 H/W ID



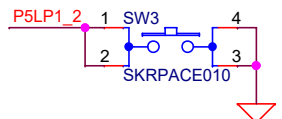
## Voltage Monitoring



## I2C Pull-ups



## Mode Switch



## KitProg3 Power LED



## KitProg3 Status LED



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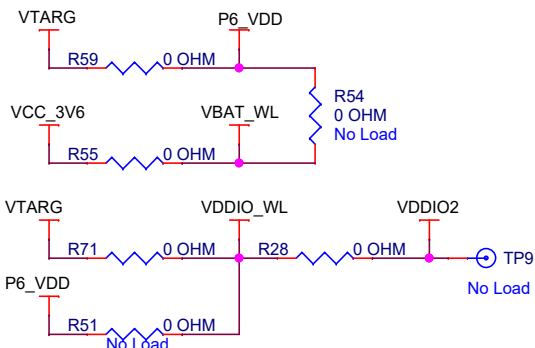
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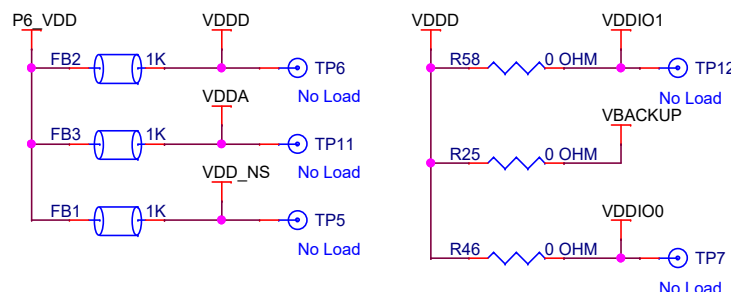
**Page Title : KitProg3**

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A4	630-60562-01	TARE	RKAD	03
Date:	Thursday, September 19, 2019		Sheet	5 of 10

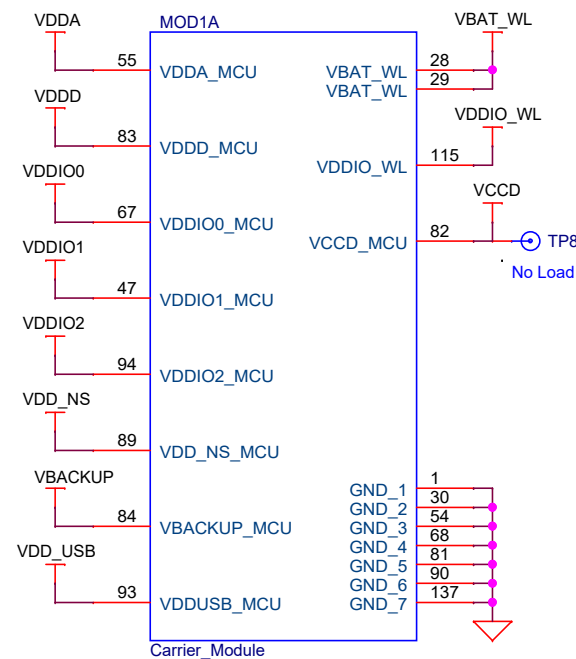
## Current Measurement



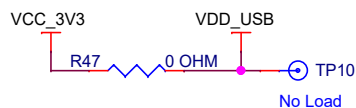
Note: Load R54, R51 and remove R55, R71 to measure combined current ( VBAT, VDDIO\_WL and P6\_VDD) . It is recommended to supply external power in this scenario



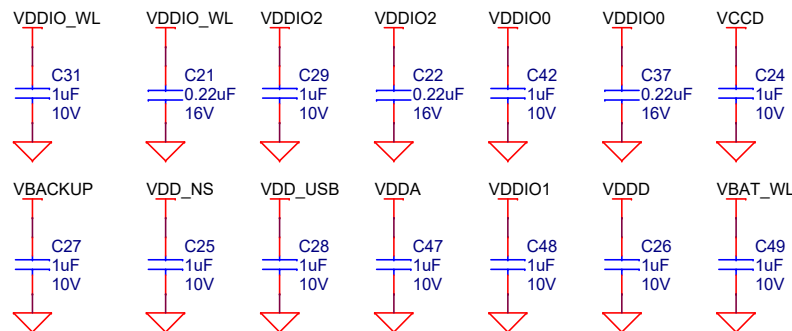
## Module Power



## MCU USB Voltage



## Decoupling Capacitors



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**Page Title : Carrier Module Power**

Size A4	Document Number <b>630-60562-01</b>	Drawn By <b>TARE</b>	Approved By <b>RKAD</b>	Rev <b>03</b>
Date:	Thursday, September 19, 2019		Sheet	6 of 10

**Carrier Module Signals**

VREF

MOD1B

MCU\_I2C\_SCL 136 I2C\_SCL

MCU\_I2C\_SDA 133 I2C\_SDA

ARD\_AREF 53

ARD\_A0 52 ARD\_A0

ARD\_A1 60 ARD\_A1

ARD\_A2 59 ARD\_A2

ARD\_A3 58 ARD\_A3

ARD\_A4 62 ARD\_A4

ARD\_A5 63 ARD\_A5

ARD\_A6 61 ARD\_A6

ARD\_A7 64 ARD\_A7

ETM\_CLK 44

ARD\_A8 46 ARD\_A8

ARD\_A9 48 ARD\_A9

ARD\_A10 49 ARD\_A10

ARD\_A11 45 ARD\_A11

ARD\_A12 50 ARD\_A12

ARD\_A13 56 ARD\_A13

ARD\_A14 57 ARD\_A14

ARD\_A15 51 ARD\_A15

ARD\_D0 2 ARD\_D0

ARD\_D1 3 ARD\_D1

ARD\_D2 4 ARD\_D2

ARD\_D3 6 ARD\_D3

ARD\_D4 5 ARD\_D4

ARD\_D5 9 ARD\_D5

ARD\_D6 7 ARD\_D6

ARD\_D7 8 ARD\_D7

ARD\_D8 23 ARD\_D8

ARD\_D9 25 ARD\_D9

ARD\_D10 78 ARD\_D10

ARD\_D11 76 ARD\_D11

ARD\_D12 75 ARD\_D12

ARD\_D13 77 ARD\_D13

USER\_BTN\_1 130 BUTTON\_1

125 BUTTON\_2

XRES\_L\_MCU 39 MCU\_XRES\_L

TDO\_SWO 40 MCU\_TDO

TDI 43 MCU\_TDI

TMS\_SWDIO 41 MCU\_TMS\_SWDIO

TCLK\_SWCLK 42 MCU\_TCLK\_SWCLK

CSX\_TX 124 CS\_TX\_RX

CSB\_0 33 CS\_BTN\_0

CSB\_1 31 CS\_BTN\_1

CSS\_0 36 CS\_SLD\_0

CSS\_1 34 CS\_SLD\_1

CSS\_2 32 CS\_SLD\_2

CSS\_3 38 CS\_SLD\_3

CSS\_4 37 CS\_SLD\_4

CSD\_SHIELD 98 CS\_CAP\_SH

FRAM\_SS\_L 71 FRAM\_SS\_L

FLASH\_SS\_L 72 FLASH\_SS\_L

QSPI\_CLK 66 R5 22E QSPI\_SCK

QSPI\_DATA0 70 R3 22E QSPI\_IO0

QSPI\_DATA1 74 R1 22E QSPI\_IO1

QSPI\_DATA2 65 R7 22E QSPI\_IO2

QSPI\_DATA3 73 R2 22E QSPI\_IO3

SD\_CMD 79

SD\_CLK 80

SD\_DATA0 88

SD\_DATA1 86

SD\_DATA2 85

SD\_DATA3 87

SD\_CD\_L 97

MCU\_USBDP 92 P6\_USB\_DP

MCU\_USBDM 91 P6\_USB\_DM

USB\_VBUS\_DET 134

USB\_INT 135

USB\_HOST\_EN 127

RGB\_R 123

RGB\_G 132

RGB\_B 26

LED\_1 126 R\_LED\_L

LED\_2 69

MCU\_IO\_0 129

MCU\_IO\_1 131

MCU\_IO\_2 128

MCU\_IO\_3 24

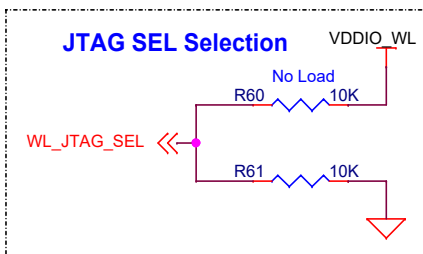
MCU\_IO\_4 35

MCU\_IO\_5 95

MCU\_IO\_6 96

Note: Not all nets connected to Carrier\_Module are actually connected to a Pin. Please refer module schematic for pinout details

Carrier\_Module



Note: Not all nets connected to Carrier\_Module are actually connected to a Pin. Please refer module schematic for pinout details

### Carrier Module Signals

MOD1C

Pin	Signal	Direction	Notes
100	WL_SDIO_DATA0	Out	
101	WL_SDIO_DATA1	Out	
102	WL_SDIO_DATA2	Out	
104	WL_SDIO_DATA3	Out	
103	WL_SDIO_CMD	Out	
99	WL_SDIO_CLK	Out	
14	WL_HOST_WAKE	In	
15	WL_DEV_WAKE	In	
16	WL_REG_ON	In	
11	WL_UART_TX	Out	
12	WL_UART_RX	In	
13	WL_IO_1	In	
10	WL_IO_2	In	
20	WL_JTAG_TCK	In	
19	WL_JTAG_TMS	In	
18	WL_JTAG_TRST_L	In	
17	WL_JTAG_TDI	In	
16	WL_JTAG_TDO	In	
22	WL_JTAG_SEL	In	
108	BT_UART_TXD	Out	
106	BT_UART_RXD	In	
107	BT_UART_CTS	In	
109	BT_UART_RTS	Out	
122	BT_HOST_WAKE	In	No Load
120	BT_DEV_WAKE	In	No Load
121	BT_REG_ON	In	No Load
112	BT_I2S_CLK	Out	
111	BT_I2S_WS	Out	
114	BT_I2S_DO	Out	
113	BT_I2S_DI	In	
116	BT_GPIO_2	In	
117	BT_GPIO_3	In	
119	BT_GPIO_4	In	
118	BT_GPIO_5	In	
27	RFU_1	In	
105	RFU_2	In	
110	LPO_IN	In	

Carrier\_Module



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<b>Date:</b> Thursday, September 19, 2019		<b>Sheet</b> 7 <b>of</b> 10		

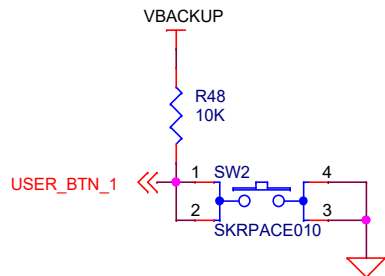
SCH Title : PSoC 62S3 Wi-Fi BT Prototyping Baseboard

Page Title : Carrie Module Signals

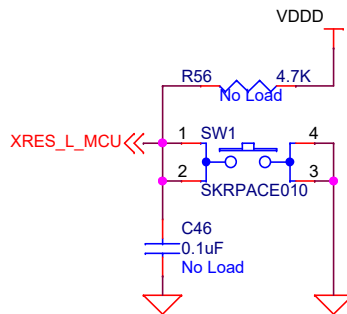
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Date:	Thursday, September 19, 2019	Sheet	7	of	10
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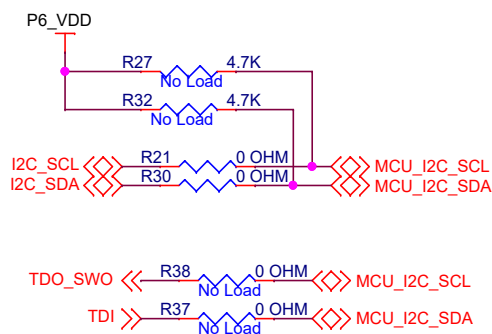
### User Button / Hibernate Wakeup



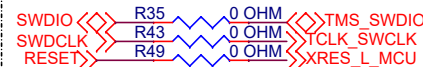
### MCU Reset Button



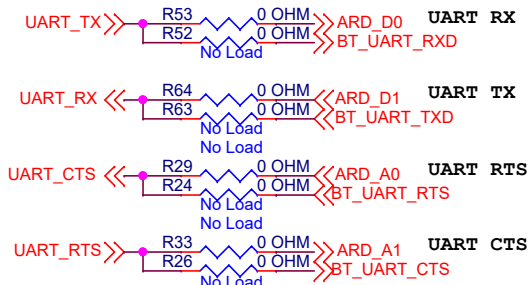
### KitProg3 MCU I2C



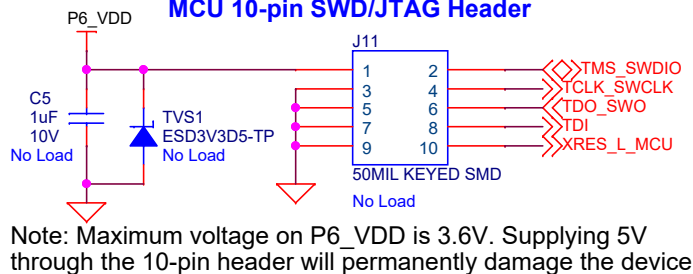
### KitProg3 MCU SWD



### KitProg3 MCU UART with H/W Flow Control



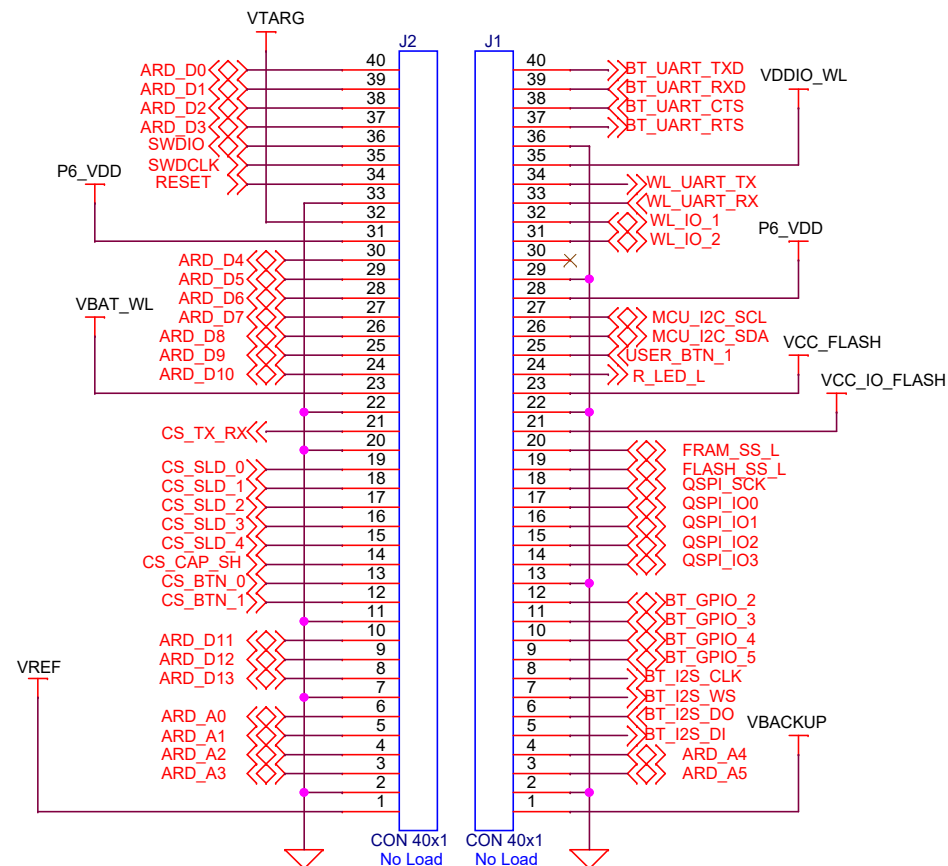
### MCU 10-pin SWD/JTAG Header



### User LED



### I/O Headers



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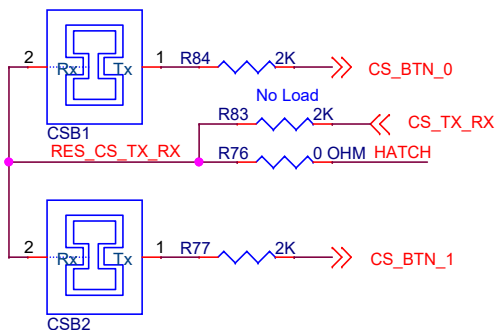
**Page Title : Interfaces and Peripherals**

Size	Document Number	Drawn By	Approved By	Rev
A4	<b>630-60562-01</b>	<b>TARE</b>	<b>RKAD</b>	<b>03</b>

Date:	Thursday, September 19, 2019	Sheet	8	of	10
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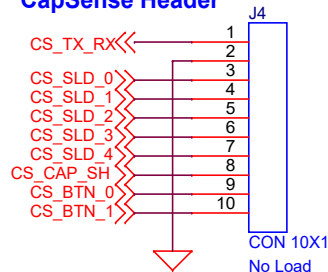


## CapSense Buttons

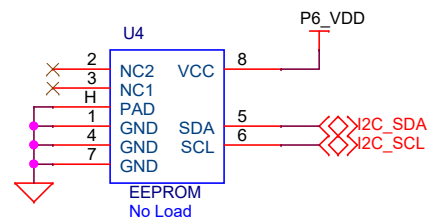


Note: CSX Mode is not supported in this kit, but is used for future compatibility

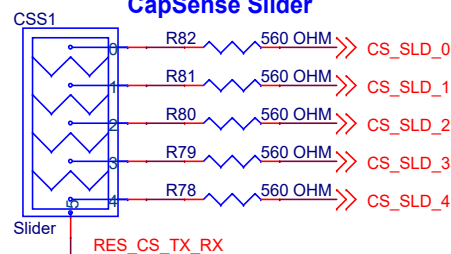
## CapSense Header



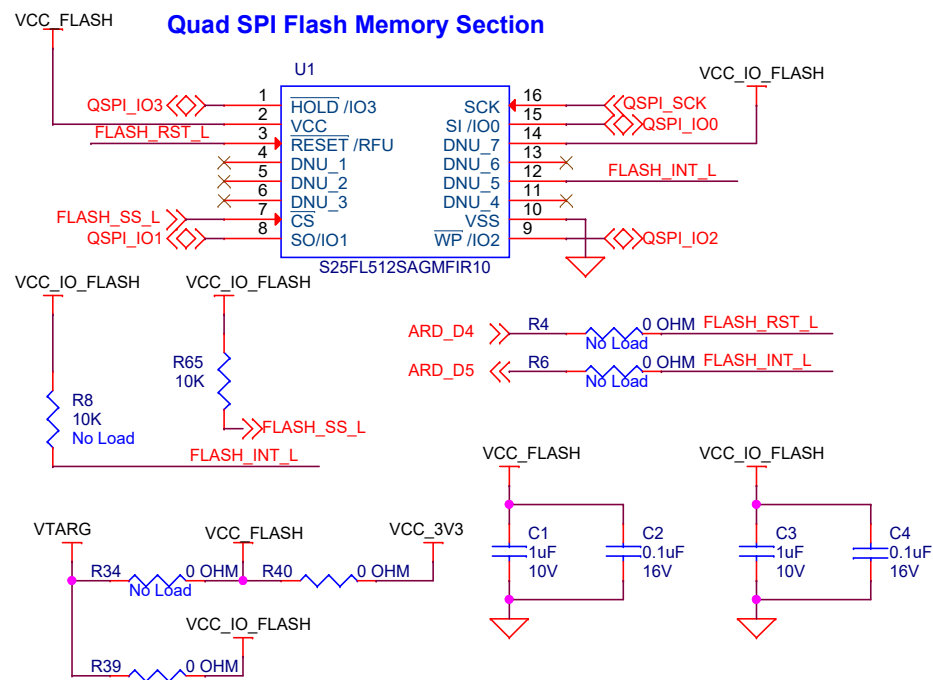
## I2C EEPROM



## CapSense Slider



## Quad SPI Flash Memory Section



## Accessories

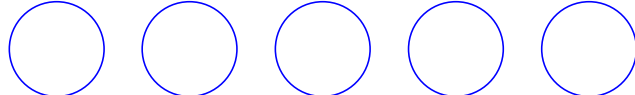
### PCBA label

LBL PCA Label



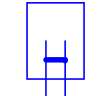
### Bumper

RBS-27 RBS-27 RBS-27 RBS-27 RBS-27



### Jumper Shunt

SPC02SYAN

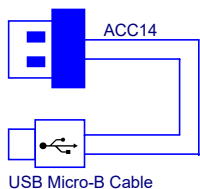


### Acrylic Overlay

Acrylic Overlay

Color: Clear, Transparent  
Finish: Matt

L = 89.66mm  
W = 25.63mm  
Thickness = 1mm



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**Page Title : Peripherals and Accessories**

Size	Document Number	Drawn By	Approved By	Rev
A4	<b>630-60562-01</b>	<b>TARE</b>	<b>RKAD</b>	<b>03</b>

Date: Thursday, September 19, 2019 Sheet 9 of 10

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Internal Release	2019/07/27
02	Internal Release	2019/08/08
03	Initial Release	2019/09/19



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Page Title : Revision History

Size A4	Document Number <b>630-60562-01</b>	Drawn By <b>TARE</b>	Approved By <b>RKAD</b>	Rev <b>03</b>
Date:	Thursday, September 19, 2019	Sheet	10 of 10	