CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit

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Drawing	Numbers
PCBA	121-60537-01
PCB	600-60537-01
FAB DRW	610-60537-01
ASSY DRW	620-60537-01
SCH DRW	630-60537-01

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SCH Title : PSoC 6 Wi-Fi BT Prototyping Kit

Page Title : Title Page

Size	Document Number	Drawn By	Approved By	Rev
A4	630-60537-01	TARE	RKAD	02

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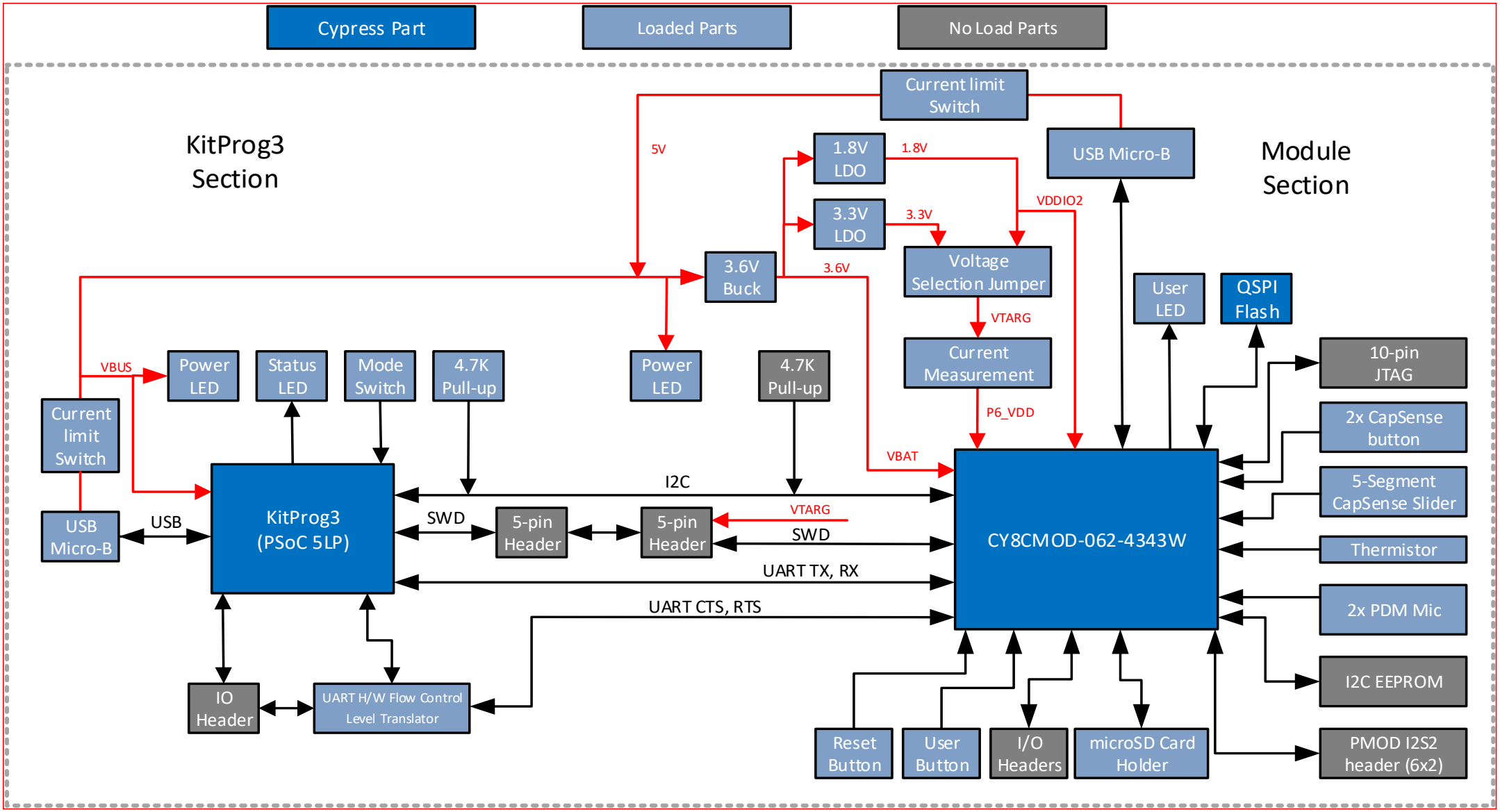

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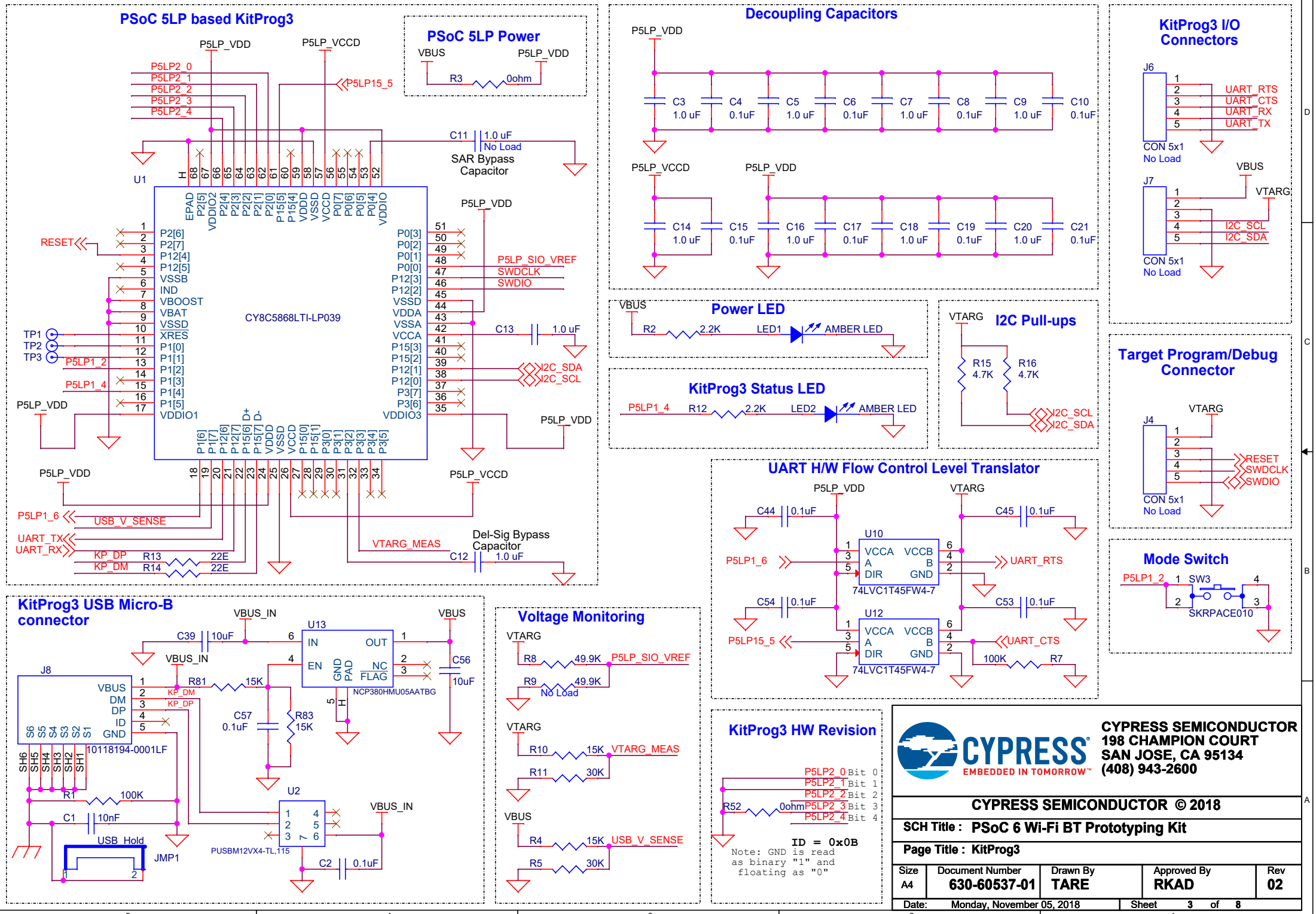
PSoC 5LP based KitProg3
U1
CY8C5868LTI-LP039
P5LP_VDD
P5LP_VCCD
P5LP2_0
P5LP2_1
P5LP2_2
P5LP2_3
P5LP2_4
P5LP15_5
RESET
TP1
TP2
TP3
P5LP1_2
P5LP1_4
P5LP1_6
USB_V_SENSE
UART_TX
UART_RX
KP_DP
KP_DM
R13 22E
R14 22E
VTARG_MEAS
C11 1.0 uF
No Load
SAR Bypass Capacitor
C13 1.0 uF
P5LP_SIO_VREF
SWDCLK
SWDIO
I2C_SDA
I2C_SCL
Del-Sig Bypass Capacitor
C12 1.0 uF
PSoC 5LP Power
VBUS
R3 0ohm
Decoupling Capacitors
C3 1.0 uF
C4 0.1uF
C5 1.0 uF
C6 0.1uF
C7 1.0 uF
C8 0.1uF
C9 1.0 uF
C10 0.1uF
C14 1.0 uF
C15 0.1uF
C16 1.0 uF
C17 0.1uF
C18 1.0 uF
C19 0.1uF
C20 1.0 uF
C21 0.1uF
Power LED
R2 2.2K
LED1
AMBER LED
KitProg3 Status LED
R12 2.2K
LED2
AMBER LED
I2C Pull-ups
VTARG
R15 4.7K
R16 4.7K
KitProg3 I/O Connectors
J6
CON 5x1
No Load
UART_RTS
UART_CTS
UART_RX
UART_TX
J7
VBUS
VTARG
I2C_SCL
I2C_SDA
Target Program/Debug Connector
J4
RESET
SWDCLK
SWDIO
Mode Switch
P5LP1_2
SW3
SKRPACE010
UART H/W Flow Control Level Translator
U10
U12
VCCA
VCCB
A
B
DIR
GND
74LVC1T45FW4-7
C44 0.1uF
C45 0.1uF
C54 0.1uF
C53 0.1uF
P5LP1_6
P5LP15_5
UART_RTS
UART_CTS
100K R7
KitProg3 USB Micro-B connector
J8
VBUS
DM
DP
ID
GND
10118194-0001LF
VBUS_IN
C39 10uF
U13
IN
OUT
EN
NC
FLAG
NCP380HMU05AATBG
C56 10uF
R81 15K
C57 0.1uF
R83 15K
R1 100K
C1 10nF
USB_Hold
JMP1
U2
PUSBM12VX4-TL,115
C2 0.1uF
Voltage Monitoring
R8 49.9K
R9 49.9K
No Load
R10 15K
R11 30K
R4 15K
R5 30K
USB_V_SENSE
KitProg3 HW Revision
R52 0ohm
P5LP2_0 Bit 0
P5LP2_1 Bit 1
P5LP2_2 Bit 2
P5LP2_3 Bit 3
P5LP2_4 Bit 4
ID = 0x0B
Note: GND is read as binary "1" and floating as "0"
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Page Title : KitProg3
Size A4
Document Number 630-60537-01
Drawn By TARE
Approved By RKAD
Rev 02
Date: Monday, November 05, 2018
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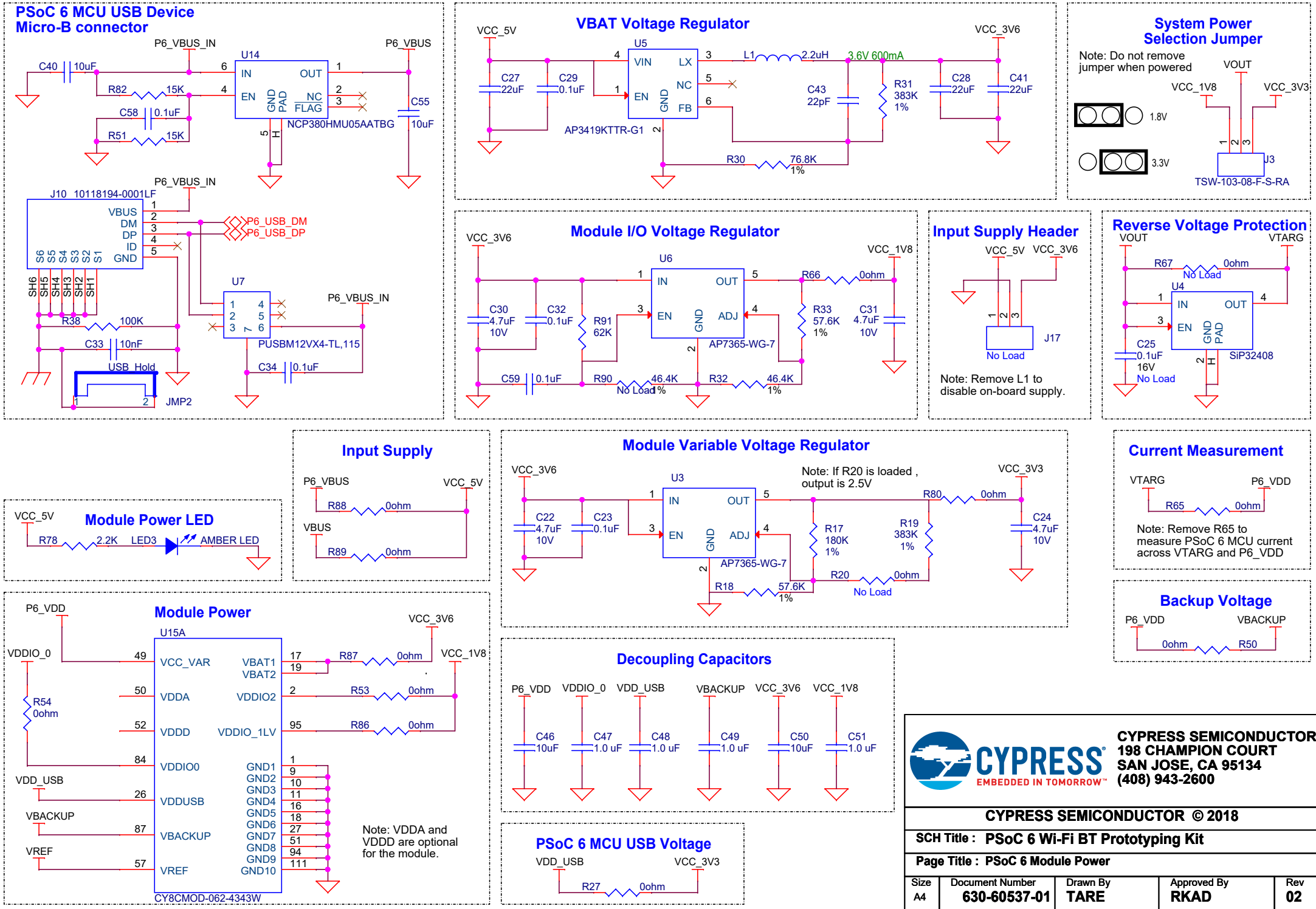
PSoC 6 MCU USB Device
Micro-B connector
P6_VBUS_IN
P6_VBUS
U14
IN
OUT
EN
GND PAD
NC
FLAG
NCP380HMU05AATBG
C40 10uF
R82 15K
C58 0.1uF
R51 15K
C55 10uF
J10 10118194-0001LF
VBUS
DM
DP
ID
GND
S6 S5 S4 S3 S2 S1
SH6 SH5 SH4 SH3 SH2 SH1
P6_USB_DM
P6_USB_DP
U7
PUSBM12VX4-TL,115
R38 100K
C33 10nF
C34 0.1uF
USB_Hold
JMP2
VBAT Voltage Regulator
VCC_5V
VCC_3V6
U5
VIN
LX
EN
GND
NC
FB
AP3419KTTR-G1
L1 2.2uH
3.6V 600mA
C27 22uF
C29 0.1uF
C43 22pF
R31 383K 1%
C28 22uF
C41 22uF
R30 76.8K 1%
System Power
Selection Jumper
Note: Do not remove
jumper when powered
VOUT
VCC_1V8
VCC_3V3
1.8V
3.3V
U3
TSW-103-08-F-S-RA
Module I/O Voltage Regulator
VCC_3V6
VCC_1V8
U6
IN
OUT
EN
GND
ADJ
AP7365-WG-7
R66 0ohm
C30 4.7uF 10V
C32 0.1uF
R91 62K
R33 57.6K 1%
C31 4.7uF 10V
C59 0.1uF
R90 46.4K 1%
No Load
R32 46.4K 1%
Input Supply Header
VCC_5V
VCC_3V6
J17
No Load
Note: Remove L1 to
disable on-board supply.
Reverse Voltage Protection
VOUT
VTARG
R67 0ohm
No Load
U4
IN
OUT
EN
GND PAD
SiP32408
C25 0.1uF 16V
No Load
Input Supply
P6_VBUS
VCC_5V
R88 0ohm
VBUS
R89 0ohm
Module Variable Voltage Regulator
VCC_3V6
VCC_3V3
U3
IN
OUT
EN
GND
ADJ
AP7365-WG-7
Note: If R20 is loaded ,
output is 2.5V
C22 4.7uF 10V
C23 0.1uF
R17 180K 1%
R19 383K 1%
R80 0ohm
C24 4.7uF 10V
R20 0ohm
No Load
R18 57.6K 1%
Current Measurement
VTARG
P6_VDD
R65 0ohm
Note: Remove R65 to
measure PSoC 6 MCU current
across VTARG and P6_VDD
Module Power LED
VCC_5V
R78 2.2K
LED3
AMBER LED
Backup Voltage
P6_VDD
VBACKUP
0ohm
R50
Module Power
P6_VDD
U15A
VCC_3V6
VCC_1V8
VDDIO_0
VCC_VAR
VBAT1
VBAT2
VDDA
VDDIO2
VDDD
VDDIO_1LV
VDDIO0
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
VDDUSB
VBACKUP
VREF
R87 0ohm
R53 0ohm
R86 0ohm
R54 0ohm
VDD_USB
VBACKUP
VREF
CY8CMOD-062-4343W
Note: VDDA and
VDDD are optional
for the module.
Decoupling Capacitors
P6_VDD
VDDIO_0
VDD_USB
VBACKUP
VCC_3V6
VCC_1V8
C46 10uF
C47 1.0 uF
C48 1.0 uF
C49 1.0 uF
C50 10uF
C51 1.0 uF
PSoC 6 MCU USB Voltage
VDD_USB
VCC_3V3
R27 0ohm
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Size A4
Document Number 630-60537-01
Drawn By TARE
Approved By RKAD
Rev 02
Date: Monday, November 12, 2018
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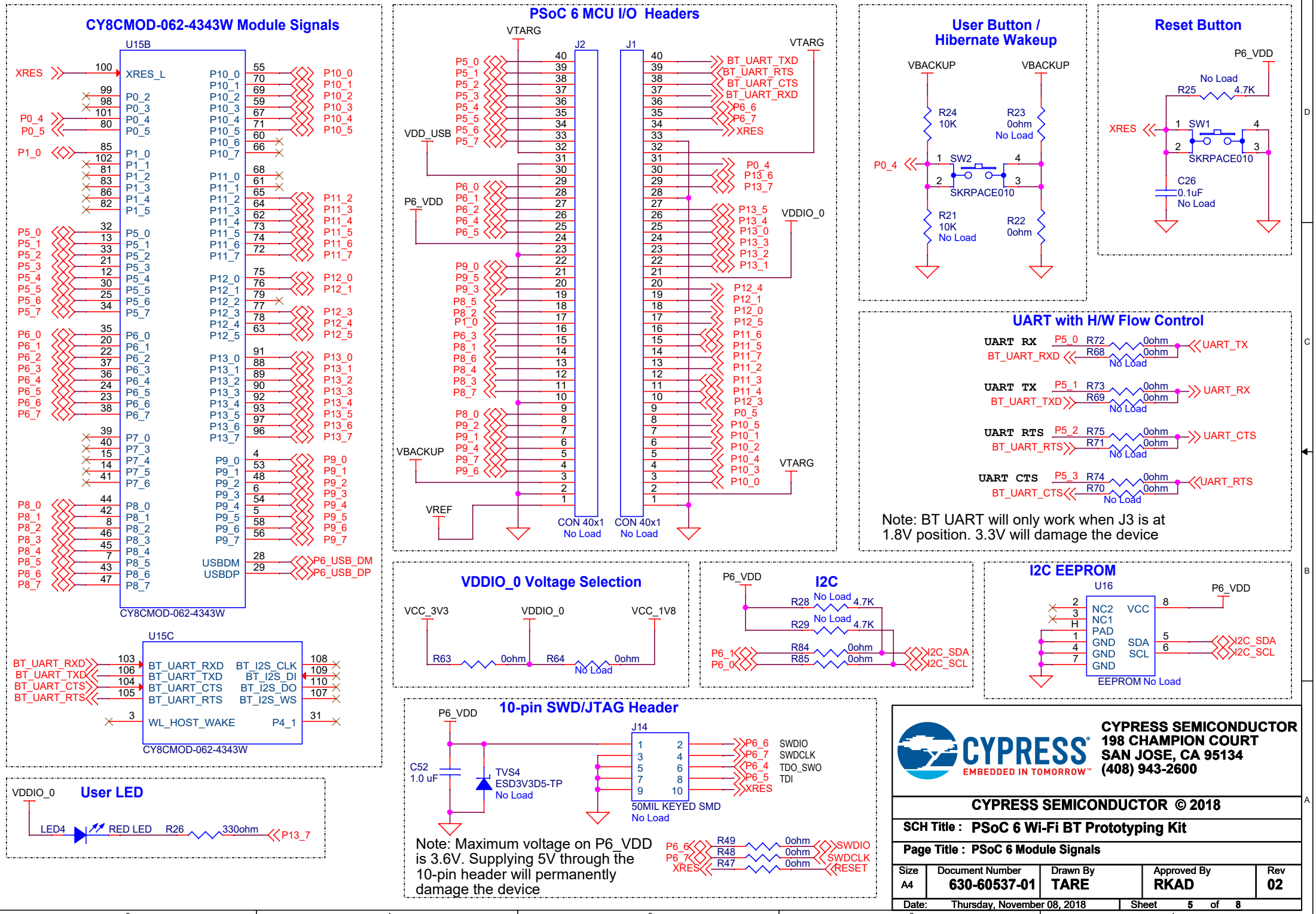
CY8CMOD-062-4343W Module Signals
U15B
XRES_L
CY8CMOD-062-4343W
U15C
WL_HOST_WAKE
P4_1
BT_UART_RXD
BT_UART_TXD
BT_UART_CTS
BT_UART_RTS
BT_I2S_CLK
BT_I2S_DI
BT_I2S_DO
BT_I2S_WS
USBDM
USBDP
P6_USB_DM
P6_USB_DP
User LED
VDDIO_0
LED4
RED LED
R26
330ohm
P13_7
PSoC 6 MCU I/O Headers
VTARG
J2
J1
VDD_USB
P6_VDD
VDDIO_0
VBACKUP
VREF
CON 40x1
No Load
BT_UART_TXD
BT_UART_RTS
BT_UART_CTS
BT_UART_RXD
XRES
VDDIO_0 Voltage Selection
VCC_3V3
VCC_1V8
R63
0ohm
R64
I2C
R28
R29
4.7K
R84
R85
I2C_SDA
I2C_SCL
10-pin SWD/JTAG Header
J14
C52
1.0 uF
TVS4
ESD3V3D5-TP
50MIL KEYED SMD
SWDIO
SWDCLK
TDO_SWO
TDI
R49
R48
R47
RESET
User Button / Hibernate Wakeup
VBACKUP
R24
10K
R23
SW2
SKRPACE010
R21
R22
Reset Button
P6_VDD
R25
SW1
C26
0.1uF
UART with H/W Flow Control
UART RX
UART TX
UART RTS
UART CTS
R72
R68
R73
R69
R75
R71
R74
R70
UART_TX
UART_RX
UART_CTS
UART_RTS
Note: BT UART will only work when J3 is at 1.8V position. 3.3V will damage the device
I2C EEPROM
U16
NC2
NC1
PAD
GND
VCC
SDA
SCL
EEPROM No Load
Note: Maximum voltage on P6_VDD is 3.6V. Supplying 5V through the 10-pin header will permanently damage the device
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Approved By RKAD
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Thermistor and PDM Mic Section

THERM_OUT R36 0ohm P10_1

THERM_OUT R37 0ohm P10_2

Header

J11 — CON 8x1 — No Load

VTARG

Pin	Net	Function
1	P10_5	PDM_DATA
2	P10_1	THERM_OUT
3	P10_2	THERM_OUT
4	P10_4	PDM_CLK
5	P10_3	THERM_VDD
6	P10_0	THERM_GND
7		
8		

Thermistor

P10_3 THERM_VDD

C38 10nF 50V No Load

RT1 NCP18XH103F03RB

THERM_OUT

C37 10nF 50V No Load

R39 10K 1%

P10_0 THERM_GND

PDM Mic

VTARG

C36 0.1uF

SPK0838HT4H-B — U9

SEL CLK DAT

P10_4 P10_5

U8 — SPK0838HT4H-B

C35 0.1uF

Quad SPI Flash Memory and microSD Card Section

Quad SPI Flash (SMIF)

VDDIO_0

R77 0ohm

U11 — S25FL512SAGMFI010

Pin	Net	Pin	Net
1	HOLD /IO3	16	SCK
2	VCC	15	SI /IO0
3	RESET /RFU	14	DNU_7
4	DNU_1	13	DNU_6
5	DNU_2	12	DNU_5
6	DNU_3	11	DNU_4
7	CS	10	VSS
8	SO/IO1	9	WP /IO2

P11_3 P11_2 P11_5 P11_7 P11_6 P11_4

C42 1.0 uF

R6 10K

Header

VDDIO_0

J13 — CON 18x1 — No Load

Net	Pin
P13_5	2
P13_4	3
P13_0	4
P13_3	5
P13_2	6
P13_1	7
	8
P12_4	9
P12_1	10
P12_0	11
P12_5	12
P11_6	13
P11_5	14
P11_7	15
P11_2	16
P11_3	17
P11_4	18

SD_IO0 SD_IO3 SD_IO2 SD_IO1 SD_CMD SD_CLK SPI_IO_0 SPI_IO_1 SPI_CLK SPI_SEL SPI_IO_3 SPI_IO_2

microSD Card

VDDIO_0

R60 49.9K
R59 49.9K
R58 49.9K
R57 49.9K
R56 49.9K

J9 — MICROSD CARD SOCKET

Net	Pin	Function
SD_CMD P12_4	3	CMD
SD_CLK P12_5	5	CLK
SD_IO0 P13_0	7	DAT0
SD_IO1 P13_1	8	DAT1
SD_IO2 P13_2	1	DAT2
SD_IO3 P13_3	2	DAT3
	4	VDD
	9A	CD1
	9B	CD2
	10A	CD_COM1
	10B	CD_COM2
	6	VSS

CD_L

R46 49.9K

Card Detect Multiplexing

P13_5 R61 10K CD_L

P12_1 R62 10K No Load

CapSense Section

Shield

CAP_SH P6_3 R55 0ohm No Load

CAP_SH1 — HATCH SH

R76 0ohm

Header

J12 — CON 12X1 — No Load

Net	Pin
SLD_TX P9_3	1
SLD2 P8_5	2
BTN1 P8_2	3
BTN_TX P1_0	4
CAP_SH P6_3	5
BTN0 P8_1	6
SLD3 P8_6	7
SLD1 P8_4	8
SLD0 P8_3	9
SLD4 P8_7	10
	11
	12

CapSense Buttons

CSB1 — Tx Rx

BTN0 — 1 2 R34 2k P8_1

BTN_TX — R35 2k P1_0

CSB2 — Tx Rx

BTN1 — 1 2 R45 2k P8_2

CapSense Slider

CSS1 — Slider

Pin	Resistor	Net	Function
0	R40 560ohm	P8_3	SLD0
1	R41 560ohm	P8_4	SLD1
2	R42 560ohm	P8_5	SLD2
3	R43 560ohm	P8_6	SLD3
4	R44 560ohm	P8_7	SLD4

R79 2k P9_3 SLD_TX

Pmod Header Section

Pmod SPI

VTARG

J16 — CON 6x1 — No Load

Net	Pin
SPI_SEL P5_7	1
SPI_MOSI P5_0	2
SPI_MISO P5_1	3
SPI_CLK P5_2	4
	5
	6

Pmod I2S2

VTARG

J15 — CON 6x2 — No Load

Net	Pin	Pin	Net
MCLK P5_0	1	7	P5_0 MCLK
TX_WS P5_2	2	8	P5_5 RX_WS
TX_SCK P5_1	3	9	P5_4 RX_SCK
TX_SDO P5_3	4	10	P5_6 RX_SDO
	5	11	
	6	12	

J5

VTARG

J5 — CON 10X1 — No Load

Net	Pin
P5_0	1
P5_1	2
P5_2	3
P5_3	4
P5_4	5
P5_5	6
P5_6	7
P5_7	8
	9
	10

Note: Pmod I2S2 will only work when VTARG is 3.3V

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Accessories

PCBA label

LBL PCA Label

Bumper

RBS-27 RBS-27 RBS-27 RBS-27 RBS-27

Jumper Shunt

SPC02SYAN

Acrylic Overlay

Acrylic Overlay

Color: Clear, Transparent
Finish: Matt

L = 89.26mm
W = 20.62mm
Thickness = 1mm

ACC14

USB Micro-B Cable

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A4	630-60537-01	TARE	RKAD	02

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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Internal release	2018/08/13
02	Initial release	2018/08/21

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Size	Document Number	Drawn By	Approved By	Rev
A4	630-60537-01	TARE	RKAD	02

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