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CY8CKIT-062S2-43012

PSoC 62S2 Wi-Fi BT Pioneer Kit Guide

Doc. # 002-28109 Rev. *G

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Safety and Regulatory Compliance Information



Regulatory Compliance Information

Contains Transmitter Module FCC ID: VPYLBEE59B1LV and IC: 772C-LBEE59B1LV

This kit is intended to use for ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY and is not considered by Cypress Semiconductor to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

The kit contains [Murata's Type 1LV \(LBEE59B1LV\)](#) certified module. Due to change in the antenna pattern/type used in CY8CKIT-062S2-43012 PSoC® 62S2 Wi-Fi BT Pioneer Kit, class II permissive changes are required to recertify this kit. The radiated emission tests must be performed again to obtain a new FCC ID for this host kit. Most conducted RF test results may still be reused. Customer also needs to take their product through other FCC/ISED testing such as unintentional radiators (FCC sub part 15B) and any other required regional product certifications including but not limited to EU directives. Refer [FCC Regulatory Certification Guide](#) by Murata on information on pre-certified and reference certified module concepts and information on what additional test are required for FCC certification. Customer should consult a Telecommunication Certification Body (TCB) lab for guidance on other requirements for the device certification.

For more details on Murata Type 1LV module refer <https://wireless.murata.com/type-1lv.html>.



PSoC 62S2 Wi-Fi BT Pioneer Boards contain electrostatic discharge (ESD)- sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, which can cause a discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused PSoC 62S2 Wi-Fi BT Pioneer Boards in the protective shipping package.



End-of-Life/Product Recycling

The end-of-life cycle for this kit is five years from the date of manufacture mentioned on the back of the box. Contact your nearest recycler to discard the kit.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If an ESD workstation is unavailable, use appropriate ESD protection by wearing an anti-static wrist strap attached to a grounded metal object.

Handling Boards

CY8CKIT-062S2-43012 PSoC 62S2 Wi-Fi BT Pioneer Kit is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad, if available. Do not slide the board over any surface.

1. Introduction



Thank you for your interest in the CY8CKIT-062S2-43012 PSoC 62S2 Wi-Fi BT Pioneer Kit. The PSoC 62S2 Wi-Fi BT Pioneer Kit enables you to evaluate and develop your applications using the [PSoC 62 Series MCU](#) (hereafter called “PSoC 6 MCU”) and CYW43012 WICED Wi-Fi/BT combo device.

PSoC 6 MCU is Cypress’ latest, ultra-low-power PSoC specifically designed for wearables and IoT products. PSoC 6 MCU is a true programmable embedded system-on-chip, integrating a 150-MHz Arm® Cortex®-M4 as the primary application processor, a 100-MHz Arm Cortex-M0+ that supports low-power operations, up to 2 MB Flash and 1 MB SRAM, Secure Digital Host Controller (SDHC) supporting SD/SDIO/eMMC interfaces, CapSense® touch-sensing, and programmable analog and digital peripherals that allow higher flexibility, in-field tuning of the design, and faster time-to-market.

The PSoC 6 BLE Pioneer Board offers compatibility with Arduino™ shields. The board features a PSoC 6 MCU, and a CYW43012 Wi-Fi/Bluetooth combo module. Cypress CYW43012 is a 28-nm, ultra-low-power device that supports single-stream, dual-band IEEE 802.11n-compliant Wi-Fi MAC/baseband/radio and Bluetooth 5.0 BR/EDR/LE. The WLAN section supports SDIO interface to the host MCU (PSoC 6 MCU), and the Bluetooth section supports high-speed 4-wire UART interface to the host MCU. In addition, the board features an onboard programmer/debugger (KitProg3), a 512-Mbit Quad SPI NOR flash, a 4-Mbit Quad SPI F-RAM, a micro-B connector for USB device interface, a 5-segment CapSense slider, two CapSense buttons, a microSD card holder, an RGB LED, two user LEDs, one potentiometer, and two push buttons. The board supports operating voltages from 1.8 V to 3.3 V for PSoC 6 MCU.

You can use ModusToolbox™ to develop and debug your PSoC 6 MCU projects. [ModusToolbox software](#) is a set of tools that enable you to integrate Cypress devices into your existing development methodology.

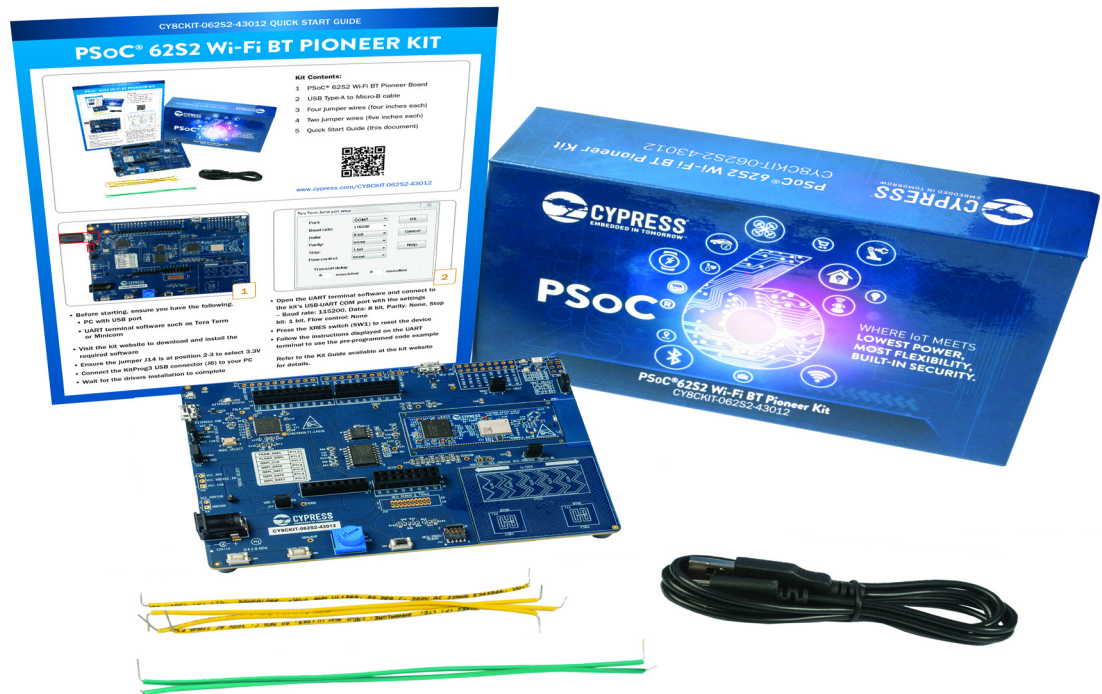
If you are new to PSoC 6 MCU and ModusToolbox IDE, refer to the application note [AN221774 - Getting Started with PSoC 6 MCU](#) to help you familiarize with the PSoC 6 MCU and help you create your own design using the ModusToolbox IDE.

1.1 Kit Contents

The CY8CKIT-062S2-43012 PSoC 62S2 Wi-Fi BT Pioneer Kit has the following contents, as shown in Figure 1-1.

- PSoC 62S2 Wi-Fi BT Pioneer Board
- USB Type-A to Micro-B cable
- Four jumper wires (4 inches each)
- Two jumper wires (5 inches each)
- Quick Start Guide

Figure 1-1. Kit Contents



Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help: www.cypress.com/support.

1.2 Getting Started

This guide will help you get acquainted with the PSoC 62S2 Wi-Fi BT Pioneer Kit:

- The [Kit Operation chapter on page 18](#) describes the major features of the PSoC 62S2 Wi-Fi BT Pioneer Kit and functionalities such as programming, debugging, and the USB-UART and USB-I²C bridges.
- The [Hardware chapter on page 29](#) provides a detailed hardware description, methods to use the onboard NOR flash, kit schematics, and the bill of materials (BOM).
- Application development using PSoC 62S2 Wi-Fi BT Pioneer Kit is supported in various development ecosystems such as ModusToolbox and Mbed OS. For the latest software support for this development kit including the different development ecosystems, refer to the [kit webpage](#).
 - ModusToolbox software is a free development ecosystem that includes the ModusToolbox IDE. Using ModusToolbox IDE, you can enable and configure device resources, middleware libraries, and program and debug the device. You can download the software from the [ModusToolbox home page](#). See the ModusToolbox User Guide for additional information.
 - Mbed OS: Visit [Cypress' Mbed OS page](#) on instructions to develop applications on Cypress' target board on the Mbed OS platform.
- There are wide range of code examples to evaluate the PSoC 62S2 Wi-Fi BT Pioneer board. These examples help you familiarize PSoC 6 MCU and create your own design. These examples are available in various development ecosystems such as ModusToolbox IDE and Mbed OS. Visit Cypress' code example page to access examples for the following development ecosystems:
 - [ModusToolbox based examples](#)
 - [Mbed OS based examples](#)

1.3 Board Details

The PSoC 62S2 Wi-Fi BT Pioneer Board that has the following features:

- CY8CMOD-062S2-43012 carrier module that contains
 - PSoC 6 MCU (CY8C624ABZI-S2D44)
 - Murata 1LV ultra-small 2.4/5.0-GHz WLAN and Bluetooth functionality module based on CYW43012
- 512-Mbit external Quad SPI NOR Flash that provides a fast, expandable memory for data and code
- 4-Mbit Quad SPI ferroelectric random-access memory (F-RAM)
- KitProg3 onboard SWD programmer/debugger with USB-UART and USB-I²C bridge functionality
- CapSense touch-sensing slider (5 elements), two buttons, based on self-capacitance (CSD) and mutual-capacitance (CSX) sensing
- A micro-B connector for USB device interface for PSoC 6 MCU
- 1.8 V and 3.3 V operation of PSoC 6 MCU is supported
- Two user LEDs, an RGB LED, two user buttons, and a reset button for PSoC 6 MCU
- A potentiometer
- One Mode selection button and one Status LED for KitProg3
- A microSD Card holder

Figure 1-2. Pioneer Board Pinout



CY8CKIT-062S2-43012 PSoC 62S2 Wi-Fi BT Pioneer Kit Guide, Doc. # 002-28109 Rev. *G

Table 1-1. Pioneer Board Pinout (*continued*)

Pin	Primary On-board Function	Secondary On-board Function	Connection details
P1[0]	CapSense RX for buttons and CapSense TX for sliders	GPIO on non-Arduino header IO7 (J22.8)	Remove R33 to disconnect from CapSense. Populate R145 to connect to GPIO on non-Arduino header.
P1[1]	RGB red LED (LED5)	GPIO on non-Arduino header (J24.1)	–
P1[2]	USB Host Enable	–	–
P1[3]	GPIO on non-Arduino header J22.3	–	–
P1[4]	User button with Hibernate wakeup capability	GPIO on non-Arduino header (J21.10)	–
P1[5]	Orange user LED (LED8)	GPIO on non-Arduino header (J24.2)	–
P5[0]	UART_RX	Arduino D0 (J4.1)	Remove R21 to disconnect from KitProg3.
P5[1]	UART_TX	Arduino D1 (J4.2)	Remove R61 to disconnect from KitProg3.
P5[2]	UART_RTS	Arduino D2 (J4.3)	Remove R19 to disconnect from KitProg3.
P5[3]	UART_CTS	Arduino D3 (J4.4)	Remove R18 to disconnect from KitProg3.
P5[4]	Arduino D4 (J4.5)	–	–
P5[5]	Arduino D5 (J4.6)	–	–
P5[6]	Arduino D6 (J4.7)	–	–
P5[7]	Arduino D7 (J4.8)	–	–
P6[0]	I2C SCL	Arduino (J3.10)	Remove R58 to disconnect from KitProg3.
P6[1]	I2C SDA	Arduino (J3.9)	Remove R59 to disconnect from KitProg3.
P6[2]	USB VBUS Detect	–	–
P6[3]	USB Interrupt	–	–
P6[4]	PSoC 6 MCU JTAG TDO/SWD SWO	–	–
P6[5]	PSoC 6 MCU JTAG TDI	–	–
P6[6]	PSoC 6 MCU JTAG TMS/SWD SWDIO	–	–
P6[7]	PSoC 6 MCU JTAG TCK/SWD SWCLK	–	–
P7[0]	ETM Clock	–	–
P7[1]	CapSense CINTA	–	–
P7[2]	CapSense CINTB	–	–
P7[3]	RGB blue LED (LED5)	GPIO on non-Arduino header (J24.5)	–

Table 1-1. Pioneer Board Pinout (*continued*)

Pin	Primary On-board Function	Secondary On-board Function	Connection details
P7[4]	GPIO on non-Arduino header IO15 (J21.8)	CapSense Shield	Remove R155 to disconnect from IO15 (J21.8). Populate R38 to connect to CapSense Shield.
P7[5]	Arduino D8 (J3.1)	–	–
P7[6]	Arduino D9 (J3.2)	–	–
P7[7]	CapSense CMOD	–	–
P8[0]	GPIO on non-Arduino header (J22.5)	–	–
P8[1]	CapSense Button0 TX	GPIO on non-Arduino header IO8 (J21.1)	Remove R24 to disconnect from CapSense. Populate R144 to connect to GPIO on non-Arduino header.
P8[2]	CapSense Button1 TX	GPIO on non-Arduino header IO9 (J21.2)	Remove R25 to disconnect from CapSense. Populate R143 to connect to GPIO on non-Arduino header.
P8[3]	CapSense Slider0 RX	GPIO on non-Arduino header IO10 (J21.3)	Remove R28 to disconnect from CapSense. Populate R142 to connect to GPIO on non-Arduino header.
P8[4]	CapSense Slider1 RX	GPIO on non-Arduino header IO11 (J21.4)	Remove R29 to disconnect from CapSense. Populate R152 to connect to GPIO on non-Arduino header.
P8[5]	CapSense Slider2 RX	GPIO on non-Arduino header IO12 (J21.5)	Remove R30 to disconnect from CapSense. Populate R153 to connect to GPIO on non-Arduino header.
P8[6]	CapSense Slider3 RX	GPIO on non-Arduino header IO13 (J21.6)	Remove R31 to disconnect from CapSense. Populate R151 to connect to GPIO on non-Arduino header.
P8[7]	CapSense Slider4 RX	GPIO on non-Arduino header IO14 (J21.7)	Remove R32 to disconnect from CapSense. Populate R149 to connect to GPIO on non-Arduino header.
P9[0]	Extended Arduino A8 (J2.2)	ETM TRACEDATA[3]	Remove R125 to disconnect from J2 header. Populate R126 to connect to ETM Trace header.
P9[1]	Extended Arduino A9 (J2.4)	ETM TRACEDATA[2]	Remove R124 to disconnect from J2 header. Populate R127 to connect to ETM Trace header.
P9[2]	Extended Arduino A10 (J2.6)	ETM TRACEDATA[1]	Remove R123 to disconnect from J2 header. Populate R128 to connect to ETM Trace header.

Table 1-1. Pioneer Board Pinout (*continued*)

Pin	Primary On-board Function	Secondary On-board Function	Connection details
P9[3]	Extended Arduino A11 (J2.8)	ETM TRACEDATA[0]	Remove R117 to disconnect from J2 header. Populate R129 to connect to ETM Trace header.
P9[4]	Extended Arduino A12 (J2.10)	—	—
P9[5]	Extended Arduino A13 (J2.12)	—	—
P9[6]	Extended Arduino A14 (J2.14)	—	—
P9[7]	Extended Arduino A15 (J2.16)	—	—
P10[0]	Arduino A0 (J2.1)	—	—
P10[1]	Arduino A1 (J2.3)	—	—
P10[2]	Arduino A2 (J2.5)	—	—
P10[3]	Arduino A3 (J2.7)	—	—
P10[4]	Arduino A4 (J2.9)	—	—
P10[5]	Arduino A5 (J2.11)	—	—
P10[6]	Potentiometer output	Extended Arduino A6 (J2.13)	Remove R51 to disconnect from potentiometer.
P10[7]	Extended Arduino A7 (J2.15)	—	—
P11[0]	QSPI F-RAM CS	—	—
P11[1]	Red user LED (LED9)	GPIO on non-Arduino header (J24.4)	—
P11[2]	QSPI Flash CS	—	—
P11[3:6]	QSPI Flash IO[3:0]	—	—
P11[7]	QSPI Flash CLK	—	—
P12[0]	Arduino header D11 (J3.4)	—	—
P12[1]	Arduino header D12 (J3.5)	—	—
P12[2]	Arduino header D13 (J3.6)	—	—
P12[3]	Arduino header D10 (J3.3)	—	—
P12[4]	microSD card CMD	—	Remove R168 to disconnect from microSD card connector.
P12[5]	microSD card CLK	—	Remove R166 to disconnect from microSD card connector.
P12[6]	ECO Crystal XIN	—	—
P12[7]	ECO Crystal XOUT	—	—

Table 1-1. Pioneer Board Pinout (*continued*)

Pin	Primary On-board Function	Secondary On-board Function	Connection details
P13[0]	microSD card DAT0	microSD card MOSI	Remove R164 to disconnect from microSD port (J20.7). Populate R169 to connect to microSD (J20.3).
P13[1]	microSD card DAT1	microSD card MISO	Remove R163 to disconnect from microSD port (J20.8). Populate R165 to connect to microSD (J20.7).
P13[2]	microSD card DAT2	microSD card SPI CLK	Remove R162 to disconnect from microSD port (J20.1) Populate R167 to connect to microSD (J20.5)
P13[3]	microSD card DAT3	microSD card SPI SSEL	–
P13[4]	GPIO on non-Arduino header IO5 (J22.6)	–	–
P13[5]	GPIO on non-Arduino header IO6 (J22.7)	–	–
P13[6]	GPIO on non-Arduino header IO3 (J22.4)	–	–
P13[7]	microSD card chip detect	GPIO on non-Arduino header IO16 (J24.6)	Remove R161 to disconnect from microSD card detect Populate R160 to connect to IO16 (J24.6)
CYW43012 Pins			
BT_UART_TXD	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_UART_RXD	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_UART_CTS	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_UART_RTS	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_I2S_CLK	I2S serial clock	–	–
BT_I2S_WS	I2S serial word select	–	–
BT_I2S_DO	I2S serial data out	–	–
BT_I2S_DI	I2S serial data in	–	–
BT_IO_2	Bluetooth general-purpose I/Os	–	–
BT_IO_3	Bluetooth general-purpose I/Os	–	–

Table 1-1. Pioneer Board Pinout (*continued*)

Pin	Primary On-board Function	Secondary On-board Function	Connection details
BT_IO_4	Bluetooth general-purpose I/Os	–	–
BT_IO_5	Bluetooth general-purpose I/Os	–	–
WL_UART_RX	Wi-Fi debug UART Rx pin	–	–
WL_UART_TX	Wi-Fi debug UART Tx Pin	–	–
WL_GPIO_1	Programable GPIO	–	–
WL_GPIO_2	Programable GPIO	–	–

1.4 Additional Learning Resources

Cypress provides a wealth of data at www.cypress.com/psoc6 to help you to select the right PSoC device for your design and to help you to quickly and effectively integrate the device into your design.

1.5 Technical Support

For assistance, visit Cypress Support or contact customer support at +1(800) 541-4736 Ext. 3 (in the USA) or +1 (408) 943-2600 Ext. 3 (International).

You can also use the following support resources if you need quick assistance:

- [Self-help \(Technical Documents\)](#)
- [Local Sales Office Locations](#)

1.6 Documentation Conventions

Table 1-2. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\...cd\icc\
<i>Italics</i>	Displays file names and reference documentation: Read about the <i>sourcefile.hex</i> file in the <i>PSoC Creator User Guide</i> .
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the File icon and then click Open .
Times New Roman	Displays an equation: $2 + 2 = 4$
Text in gray boxes	Describes cautions or unique functionality of the product.

1.7 Acronyms

Table 1-3. Acronyms Used in this Document

Acronym	Definition
ADC	Analog-to-Digital Converter
BLE	Bluetooth Low Energy
BOM	Bill of Materials
BT	Bluetooth
CINT	Integration Capacitor
CMOD	Modulator Capacitor
CPU	Central Processing Unit
CSD	CapSense Sigma Delta
CSX	CapSense Crosspoint
DC	Direct Current
Del-Sig	Delta-Sigma
DMA	Direct Memory Access
ECO	External Crystal Oscillator
ESD	Electrostatic Discharge
GPIO	General-Purpose Input/Output
HID	Human Interface Device
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Integrated Circuit
IDE	Integrated Development Environment
IoT	Internet of Things
LED	Light-emitting Diode
LPO	Low Power Oscillator
PC	Personal Computer
PDM	Pulse Density Modulation
PSoC	Programmable System-on-Chip
PWM	Pulse Width Modulation
QSPI	Quad Serial Peripheral Interface
SAR	Successive Approximation Register
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input Output
SMIF	Serial Memory Interface
SPI	Serial Peripheral Interface
SRAM	Serial Random Access Memory

Table 1-3. Acronyms Used in this Document (*continued*)

Acronym	Definition
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WCO	Watch Crystal Oscillator

2. Kit Operation



This chapter introduces you to various features of the PSoC 62S2 Wi-Fi BT Pioneer Board, including the theory of operation and the onboard KitProg3 programming and debugging functionality, USB-UART and USB-I2C bridges.

2.1 Theory of Operation

The PSoC 62S2 Wi-Fi BT Pioneer Board is built around a PSoC 6 MCU. [Figure 2-1](#) shows the block diagram of the PSoC 6 MCU device used on the board. For details of device features, see the [device datasheet](#).

[Figure 2-2](#) shows the block diagram of the CYW9-BASE-01 Pioneer Board (modified for CY8CKIT-062S2-43012).

Figure 2-1. PSoC 6 MCU Block Diagram

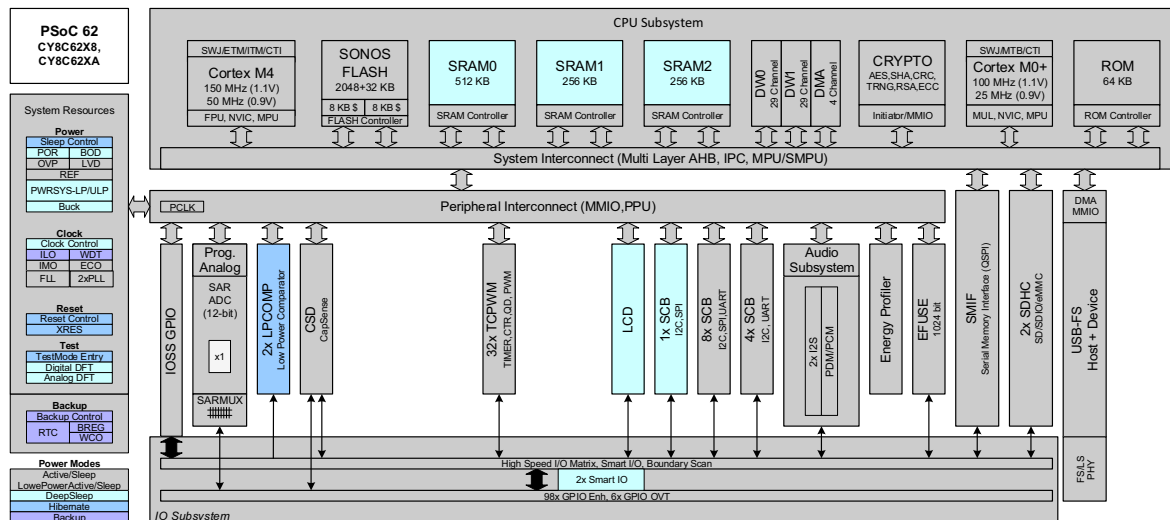
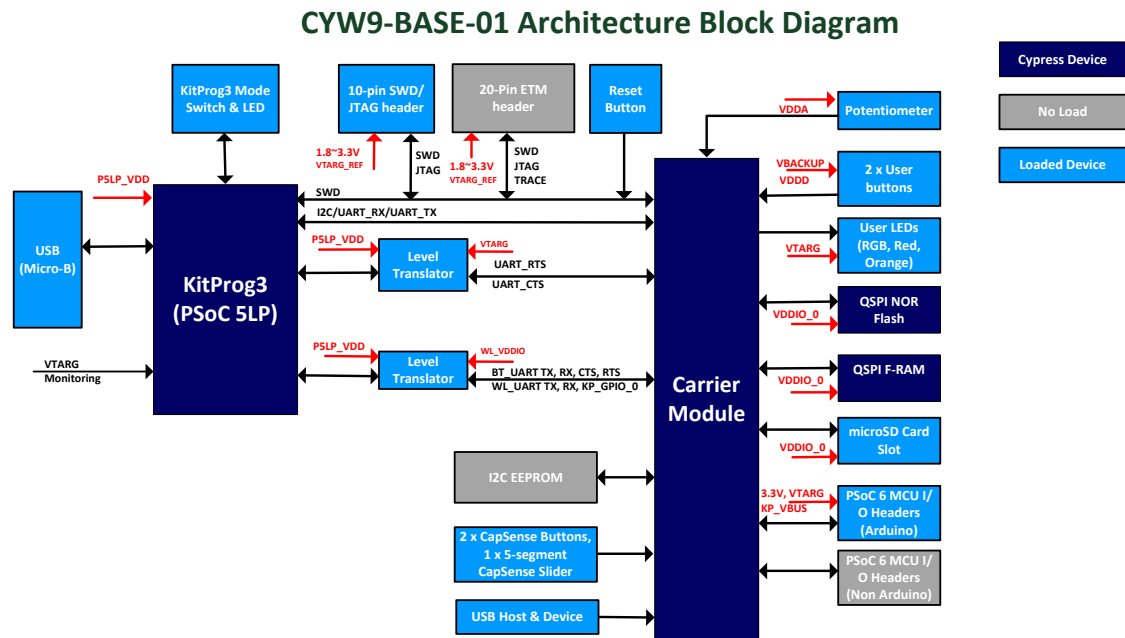


Figure 2-2. Block Diagram of Pioneer Board



The PSoC 62S2 Wi-Fi BT Pioneer Kit comes with the PSoC 62S2 Wi-Fi BT Pioneer Board. [Figure 2-3](#) and [Figure 2-4](#) show the markup of the Pioneer Board.

Figure 2-3. PSoC 62S2 Wi-Fi BT Pioneer Board - Top View

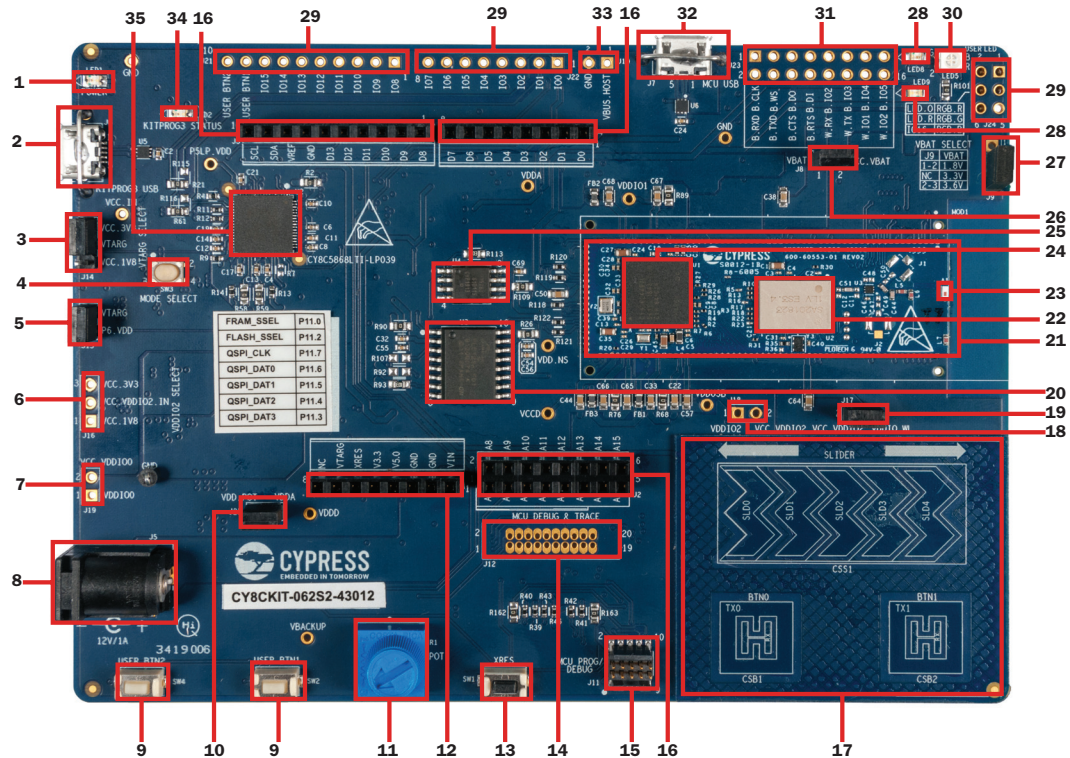
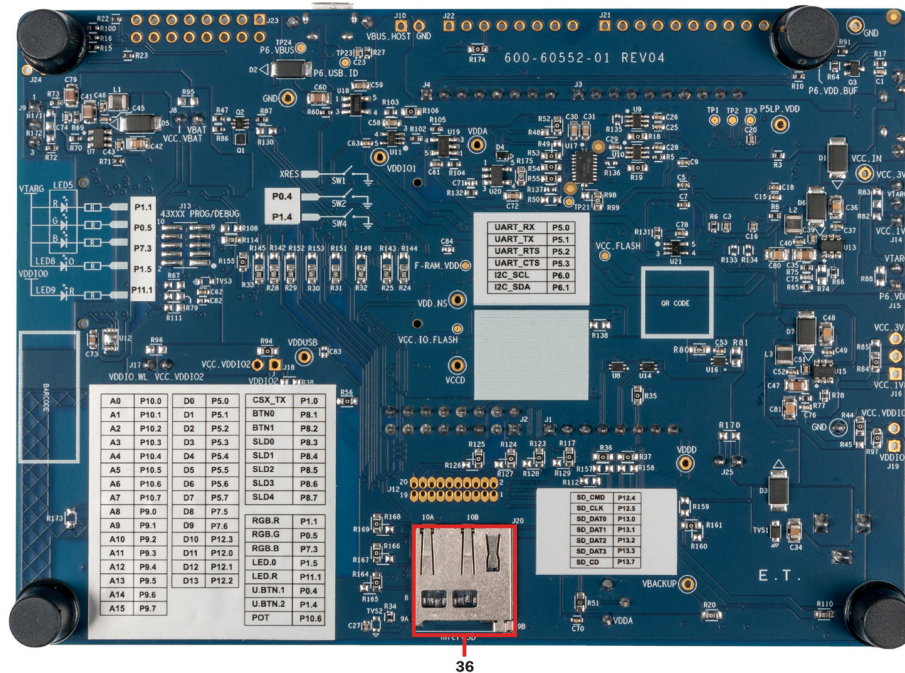


Figure 2-4. PSoC 62S2 Wi-Fi BT Pioneer Board - Bottom View



The PSoC 62S2 Wi-Fi BT Pioneer Board has the following peripherals:

1. **Power LED (LED1):** This Yellow LED indicates the status of power supplied to board.
2. **KitProg3 USB connector (J6):** The USB cable provided along with the PSoC 62S2 Wi-Fi BT Pioneer Board connects between this USB connector and the PC to use the KitProg3 onboard programmer and debugger and to provide power to the board.
3. **PSoC 6 MCU VDD power selection jumper (J14):** This jumper is used to select the PSoC 6 MCU VDD supply voltage between 1.8 V and 3.3 V.
4. **KitProg3 programming mode selection button (SW3):** This button can be used to switch between various modes of operation of KitProg3 (CMSIS-DAP BULK, CMSIS-DAP HID or DAPLink modes). For more details, see the [KitProg3 User Guide](#).
5. **PSoC 6 MCU VDD current measurement jumper (J15):** An ammeter can be connected to this jumper to measure the current consumed by the PSoC 6 MCU VDD power domain.
6. **PSoC 6 MCU VDDIO2 and CYW43012 VDDIO power selection jumper (J16):** This jumper is used to select the PSoC 6 MCU VDDIO2 and CYW43012 VDDIO supply voltage between 1.8 V and 3.3 V. This is not loaded by default.
7. **PSoC 6 MCU VDDIO0 current measurement jumper (J19):** An ammeter can be connected to this jumper to measure the current consumed by the PSoC 6 MCU VDDIO0 power domain. This is not loaded by default.
8. **External power supply VIN connector (J5):** This connector connects an external DC power supply input to the onboard regulators.
9. **PSoC 6 MCU user buttons (SW2 and SW4):** These buttons can be used to provide an input to PSoC 6 MCU. Note that by default these buttons connect the PSoC 6 MCU pin to ground when pressed, so you need to configure the PSoC 6 MCU pin as a digital input with resistive pull-up for detecting the button press. These buttons also provides a wake-up source from low-power modes of the device. In addition, this button can be used to activate the regulator control output from PSoC 6 MCU.

10. **Potentiometer connection jumper (J25):** This jumper connects the PSoC 6 MCU VDDA to potentiometer.
11. **Potentiometer (R1):** This is a 10k Ohm potentiometer connected to PSoC 6 MCU pin P10[6]. It can be used to simulate a sensor output to PSoC 6 MCU.
12. **Arduino-compatible power header (J1):** This header powers the Arduino shields. It also has a provision to power the kit through the VIN input.
13. **PSoC 6 MCU reset button (SW1):** This button is used to reset PSoC 6 MCU. It connects the PSoC 6 MCU reset (XRES) pin to ground.
14. **PSoC 6 MCU debug and trace header (J12):** This header can be connected to an Embedded Trace Macrocell (ETM)-compatible programmer/debugger. This is not loaded by default.
15. **PSoC 6 MCU program and debug header (J11):** This 10-pin header allows you to program and debug the PSoC 6 MCU using an external programmer such as [MiniProg4](#).
16. **Arduino Uno R3-compatible I/O headers (J2, J3, and J4):** These I/O headers bring out pins from PSoC 6 MCU to interface with the Arduino shields. Some of these pins are multiplexed with onboard peripherals and are not connected to PSoC 6 MCU by default. For a detailed information on how to rework the kit to access these pins, see [Table 1-1 on page 10](#).
17. **CapSense slider (SLIDER) and buttons (BTN0 and BTN1):** The CapSense touch-sensing slider and two buttons, all of which are capable of both self-capacitance (CSD) and mutual-capacitance (CSX) operation, allow you to evaluate Cypress' fourth-generation CapSense technology. The slider and buttons have a 1-mm acrylic overlay for smooth touch sensing.
18. **PSoC 6 MCU VDDIO2 current measurement jumper (J18):** An ammeter can be connected to this jumper to measure the current consumed by the PSoC 6 MCU VDDIO2 power domain. This is not loaded by default.
19. **CYW43012 VDDIO current measurement jumper(J17):** An ammeter can be connected to this jumper to measure the current consumed by the CYW43012 VDDIO power domain.
20. **Cypress serial NOR flash memory (S25FL512S, U3):** The S25HL512S NOR flash of 512-Mbit capacity is connected to the Quad SPI interface of the PSoC 6 MCU. The NOR device can be used for both data and code memory with execute-in-place (XIP) supports and encryption.
21. **Cypress PSoC 6 (2M) with CYW43012 Carrier Module (CY8CMOD-062S2-43012, MOD1):** This kit is designed to highlight the features of the PSoC 6 MCU on the CY8CMOD-062S2-43012. For details, see [CY8CMOD-062S2-43012 \(MOD1\) on page 29](#).
22. **CYW43012 based Murata Type 1LV module:** The Type 1LV module is an ultra-small module that includes 2.4 GHz and 5 GHz dual-band WLAN and Bluetooth functionality. Based on Cypress CYW43012, the module provides high-efficiency RF front end circuits. To ease Wi-Fi certification, the Type 1LV module complies with IEEE 802.11a/b/g/n and Bluetooth Version 5.0 plus EDR, Power Class 1 + BLE.
23. **Wi-Fi/BT antenna:** This is the onboard antenna connected to the Wi-Fi and Bluetooth module.
24. **PSoC 6 MCU:** This kit is designed to highlight the features of the PSoC 6 MCU. For details on PSoC 6 MCU pin mapping, refer to [Table 1-1 on page 10](#).
25. **Cypress serial Ferroelectric RAM (CY15B104QSN, U4):** The CY15B104QSN is a 4-Mbit non-volatile memory employing an advanced ferroelectric process. F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years and is connected to the Quad SPI interface of the PSoC 6 MCU.
26. **CYW43012 VBAT current measurement jumper (J8):** An ammeter can be connected to this jumper to measure the current consumed by the CYW43012 VBAT power domain.
27. **CYW43012 VBAT power selection jumper (J9):** This jumper is used to select the CYW43012 VBAT supply voltage between 1.8 V, 3.3 V and 3.6 V.

28. **PSoC 6 MCU user LEDs (LED8 and LED9):** These two user LEDs can operate at the entire operating voltage range of PSoC 6 MCU. The LED is active LOW, so the pins must be driven to ground to turn ON the LED.
29. **PSoC 6 I/O header (J21, J22, J24):** These headers provide connectivity to PSoC 6 MCU GPIOs that are not connected to the Arduino compatible headers. Some of these I/Os are also connected to on-board peripherals see [Table 1-1 on page 10](#) for pin mapping.
30. **RGB LED (LED5):** This onboard RGB LED can be controlled by the PSoC 6 MCU. The LEDs are active LOW, so the pins must be driven to ground to turn ON the LEDs.
31. **Wi-Fi/BT GPIO header (J23):** This header brings out few IOs of the CYW43012 for general purpose applications.
32. **PSoC 6 USB device connector (J7):** The USB cable provided with the PSoC 62S2 Wi-Fi BT Pioneer Kit can also be connected between this USB connector and the PC to use the PSoC 6 MCU USB device applications.
33. **Optional USB Host power supply header (J10):** This header provides an option to supply external power to the PSoC 6 USB when used as a USB Host.
34. **KitProg3 status LED (LED2):** This Yellow LED indicates the status of KitProg3. For details on the KitProg3 status, see the [KitProg3 User Guide](#).
35. **KitProg3 (PSoC 5LP) programmer and debugger (CY8C5868LTI-LP039, U2):** The PSoC 5LP device (CY8C5868LTI-LP039) serving as KitProg3, is a multi-functional system, which includes a SWD programmer, debugger, USB-I2C bridge and USB-UART bridge. For more details, see the [KitProg3 User Guide](#).
36. **microSD Card holder (J20):** Provide SDHC interface with microSD cards with the option to detect the presence of the card.

See [Hardware Functional Description on page 29](#) for details on various hardware blocks.

2.2 KitProg3: On-Board Programmer/Debugger

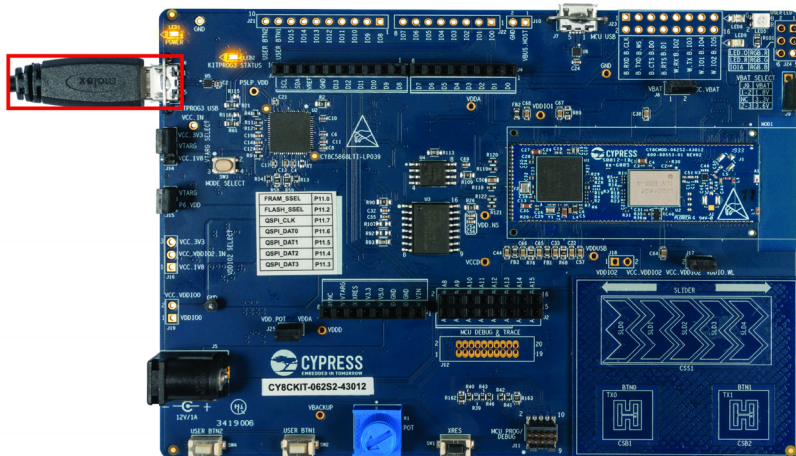
The PSoC 62S2 Wi-Fi BT Pioneer Board can be programmed and debugged using the onboard KitProg3. KitProg3 is an onboard programmer/debugger with USB-UART and USB-I2C functionality. A Cypress PSoC 5LP device is used to implement KitProg3 functionality. For more details on the KitProg3 functionality, see the [KitProg3 User Guide](#).

2.2.1 Programming and Debugging using ModusToolbox

This section presents a quick overview of programming and debugging using ModusToolbox. For detailed instructions, see **Help > ModusToolbox IDE Documentation > User Guide**.

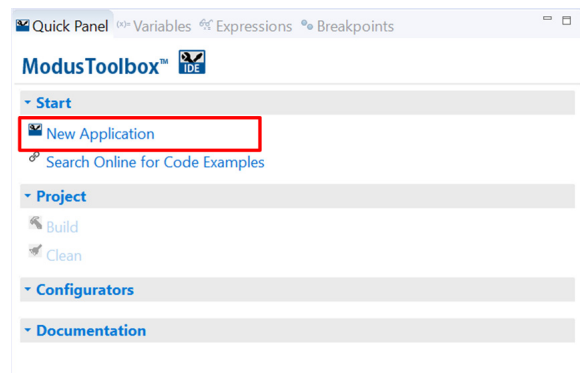
1. Connect the board to the PC using the USB cable, as shown in [Figure 2-5](#). It enumerates as a USB Composite Device if you are connecting it to your PC for the first time. KitProg3 can operate either in CMSIS-DAP Bulk mode (default), CMSIS-DAP HID mode or DAPLink mode (DAPLink mode is required for programing using Mbed CLI). KitProg3 also supports CMSIS-DAP Bulk with two UARTs. Programming is faster with the Bulk mode. The status LED (Yellow) is always ON in Bulk mode, ramping at 1 Hz rate in HID mode, and ramping at 2 Hz rate in DAPLink mode. Press and release the Mode select button (SW3) to switch between these modes. If you do not see the desired LED status, see the KitProg3 User Guide for details on the KitProg3 status and troubleshooting instructions.

Figure 2-5. Connect USB Cable to USB Connector on the Board



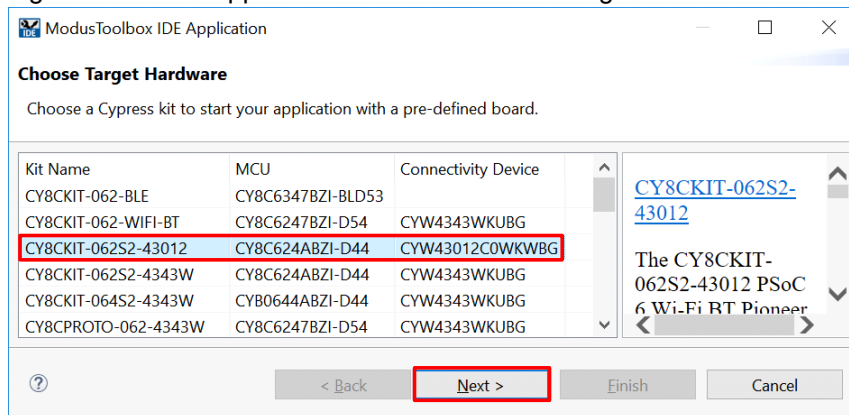
2. In the ModusToolbox IDE, import the desired code example (application) into a new workspace.
 - a. Click on **New Application** from **Quick Panel**.

Figure 2-6. Create New Application



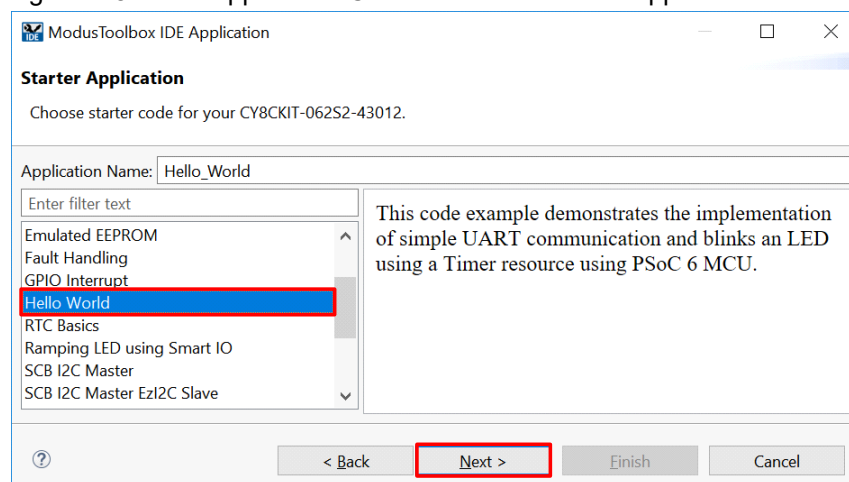
- b. Select the CY8CKIT-062S2-43012 in the **Choose Hardware Target** window and click **Next**, as shown in Figure 2-7.

Figure 2-7. New Application Creation: Choose Target Hardware



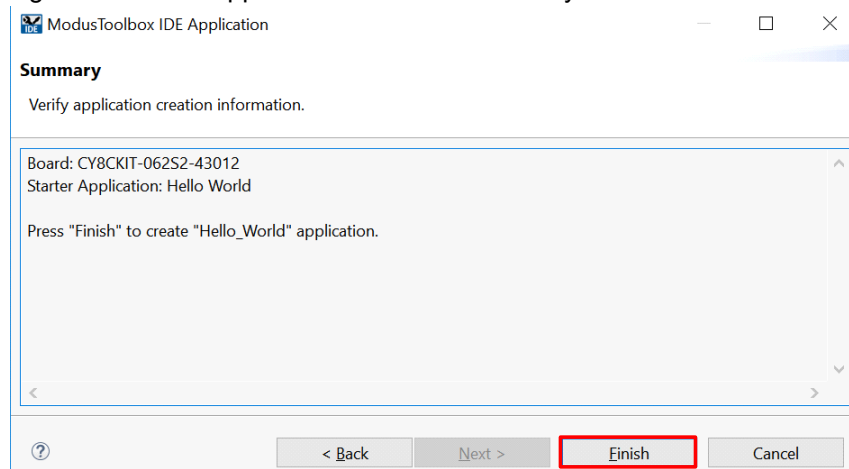
- c. Select the application in **Starter Application** window and click **Next**, as shown in Figure 2-8.

Figure 2-8. New Application Creation: Select Starter Application



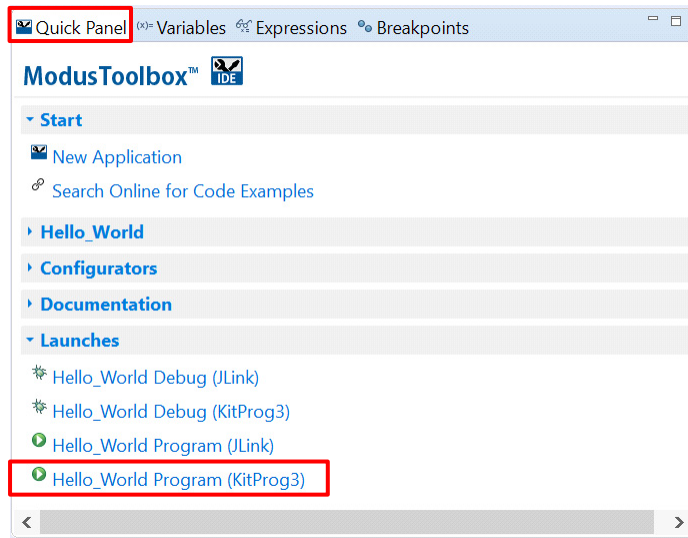
- d. Click **Finish** in **Summary** window, as shown in Figure 2-9.

Figure 2-9. New Application Creation: Summary



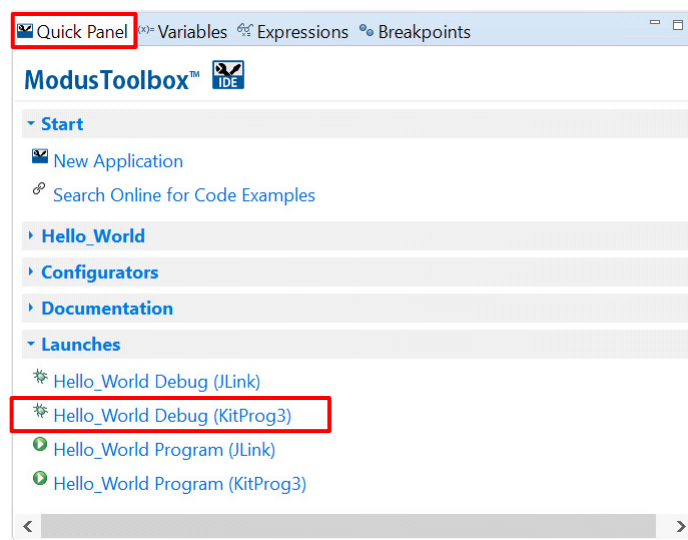
- To build and program a PSoC 6 MCU application, in the Project Explorer, select **<App_Name>** project. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Program (KitProg3)** configuration as shown in [Figure 2-10](#).

Figure 2-10. Programming in ModusToolbox



- ModusToolbox has an integrated debugger. To debug a PSoC 6 MCU application, in the Project Explorer, select **<App_Name>** project. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Debug (KitProg3)** configuration as shown in [Figure 2-11](#). For a detailed explanation on how to debug using ModusToolbox, see [KBA224621](#).

Figure 2-11. Debugging in ModusToolbox



2.2.1.1 Using the OOB Example – PSoC 6 MCU: Hello World

The PSoC 62S2 Wi-Fi BT Pioneer Board is by default programmed with the code example: PSoC 6 MCU: Hello World. The steps below describe on how to use the example. For a detailed description of the project refer to the example's readme file in the [GitHub repository](#).

Note: At any point of time, if you overwrite the OOB example, you can restore it back by programming the PSoC 6 MCU: Hello World. Refer [Programming and Debugging using ModusToolbox on page 23](#) for programming the board.

1. Connect the board to your PC using the provided USB cable through the KitProg3 USB connector.
2. Open a terminal program and select the KitProg3 COM port. Set the serial port parameters to 8N1 and 115200 baud.
3. Press the reset button (SW1) on the board and confirm that terminal application displays code example title and other text [Figure 2-12](#).

Figure 2-12. Hello World in Terminal

```
***** PSoC 6 MCU: Hello World! Example *****
Hello World!!!
For more PSoC 6 MCU projects, visit our code examples repositories:
1. ModusToolbox Examples:
  https://github.com/cypresssemiconductorco/Code-Examples-for-ModusToolbox-Software
2. Mbed OS Examples:
  https://os.mbed.com/teams/Cypress/
Press 'Enter' key to pause or resume blinking the user LED
```

4. Confirm that the kit LED blinks at 1 Hz.
5. Press the Enter key. Confirm that the kit LED stops blinking. The terminal displays the message "LED blinking paused".
6. Press the Enter key again. Confirm that the kit LED resumes blinking at 1 Hz. The message displayed on the terminal is updated to "LED blinking resumed".

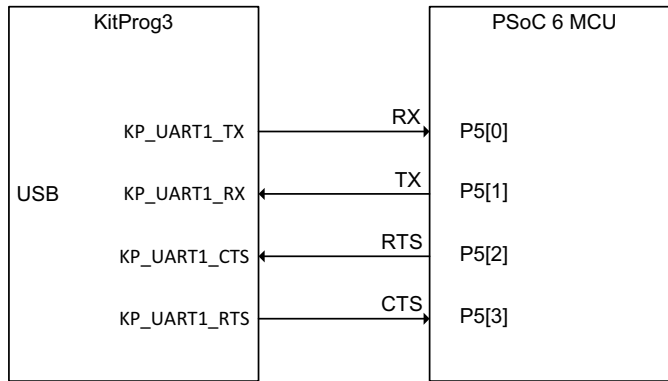
You can repeat steps 5 and 6 indefinitely.

2.2.2 USB-UART Bridge

The KitProg3 on the PSoC 62S2 Wi-Fi BT Pioneer Board can act as a USB-UART bridge.

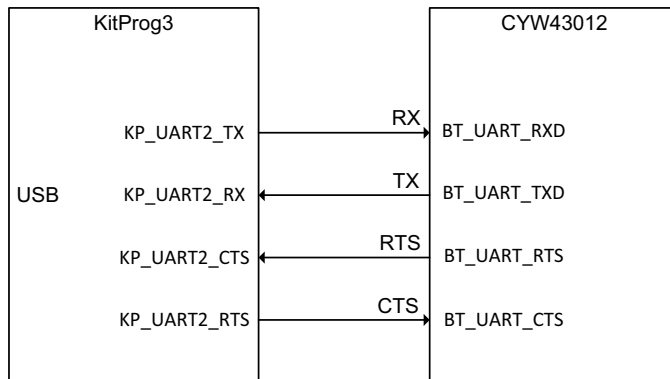
The primary UART and flow-control lines between the PSoC 6 MCU and the KitProg3 are hard-wired on the board, as [Figure 2-13](#) shows.

Figure 2-13. UART Connection between KitProg3 and PSoC 6



The secondary UART and flow-control lines between the CYW43012 and the KitProg3 are hard-wired on the board, as [Figure 2-14](#) shows.

Figure 2-14. UART Connection between KitProg3 and CYW43012

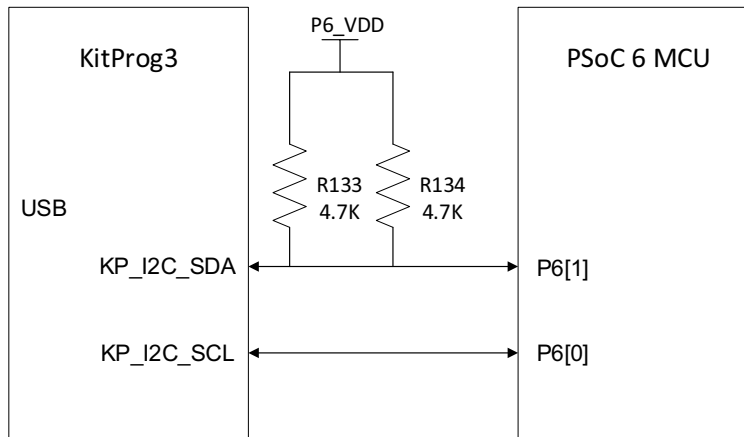


For more details on the KitProg3 USB-UART functionality, see the [KitProg3 User Guide](#).

2.2.3 USB-I2C Bridge

The KitProg3 can function as a USB-I2C bridge and can communicate with the Bridge Control Panel (BCP) software which acts as an I2C master. The I2C lines on the PSoC 6 MCU are hard-wired on the board to the I2C lines of the KitProg3, with onboard pull-up resistors as [Figure 2-15](#) shows. The USB-I2C supports I2C speeds of 50 kHz, 100 kHz, 400 kHz, and 1 MHz. For more details on the KitProg3 USB-I2C functionality, see the [KitProg3 User Guide](#).

Figure 2-15. I2C Connection between KitProg3 and PSoC 6 MCU



3. Hardware



3.1 Schematics

Refer to the schematic files available in the [kit webpage](#).

3.2 Hardware Functional Description

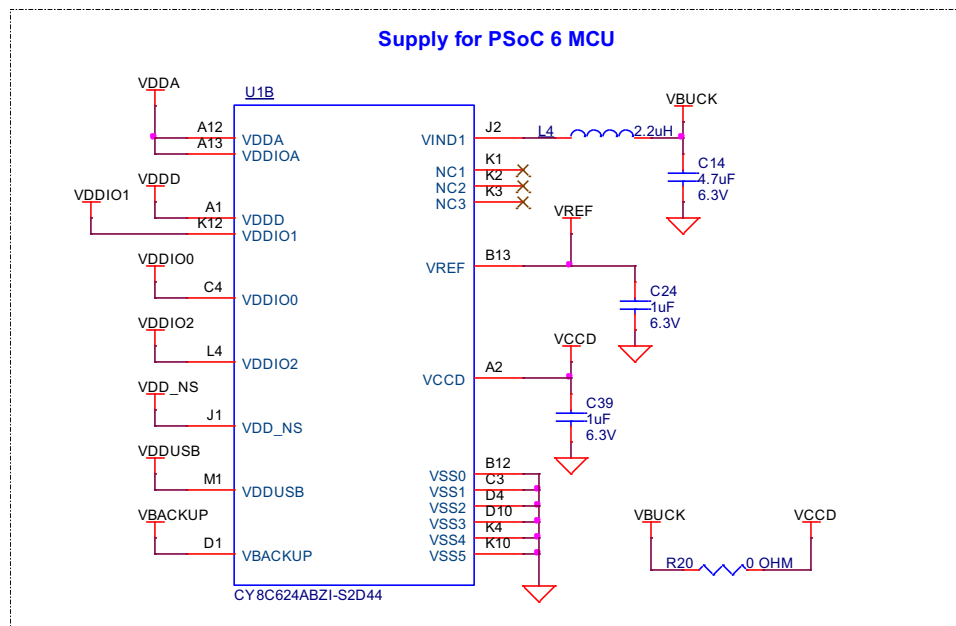
This section explains in detail the individual hardware blocks.

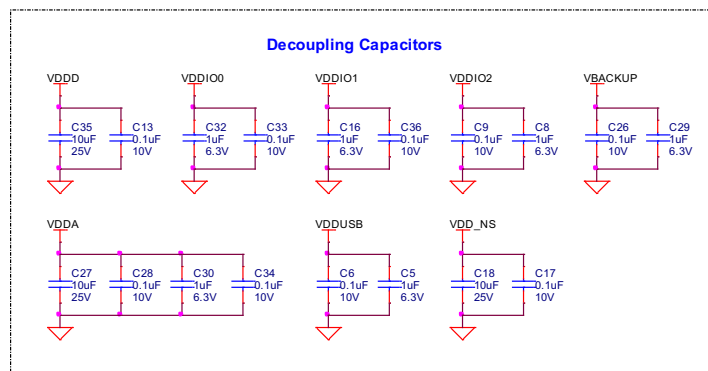
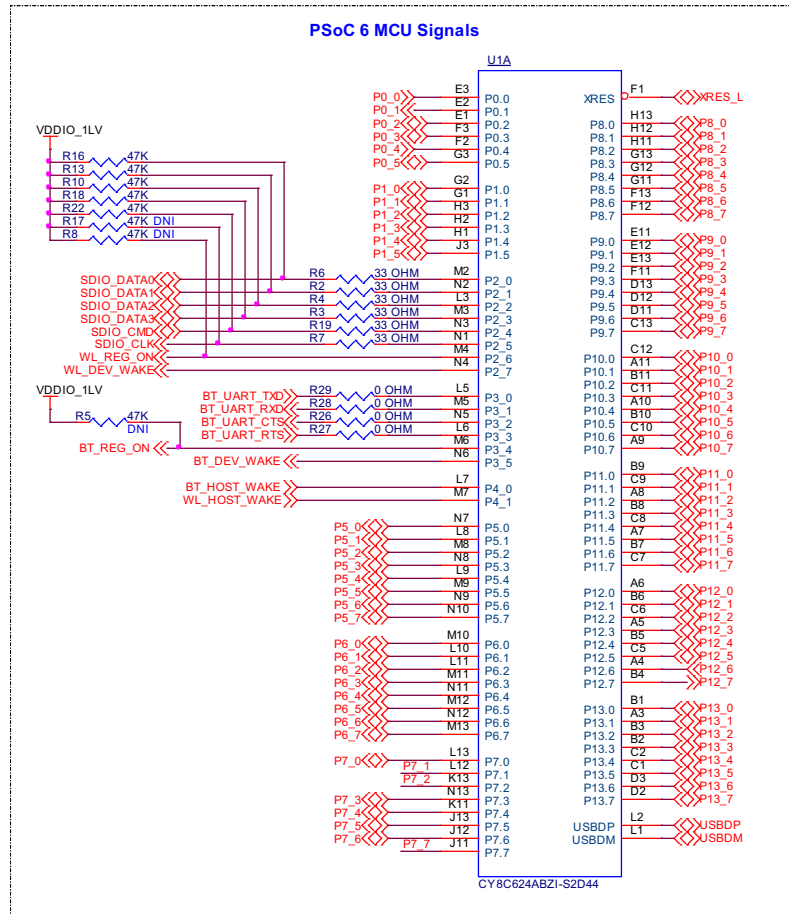
3.2.1 CY8CMOD-062S2-43012 (MOD1)

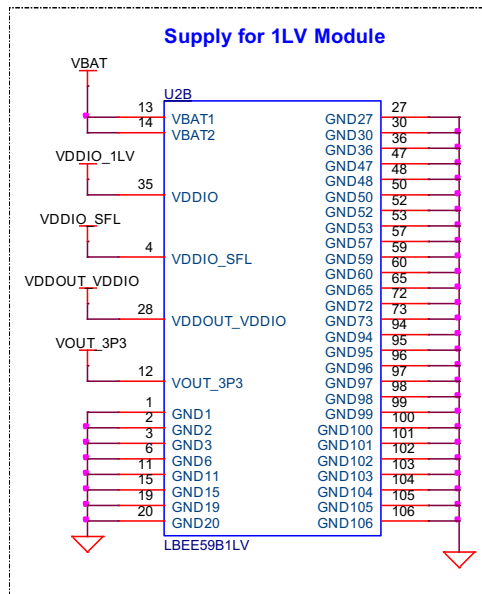
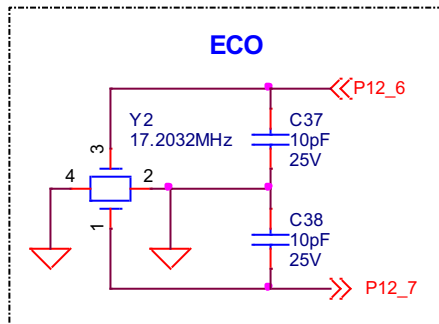
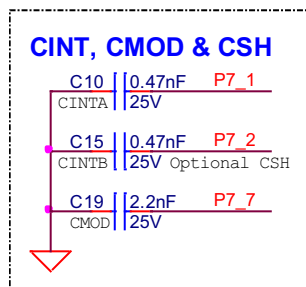
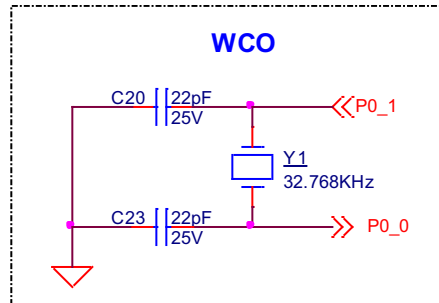
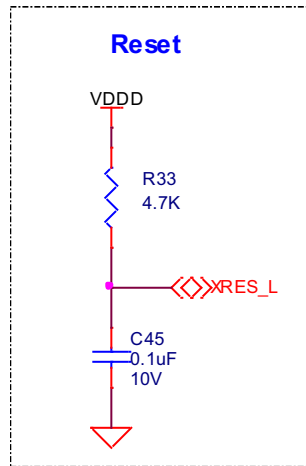
CY8CMOD-062S2-43012 PSoC 6 (2M) with CYW43012 Carrier Module is a castellated PCB module which consists mainly of PSoC 6 MCU and CYW43012 devices. The module also houses a 2.45-GHz/5-GHz dual-band chip antenna, RF switch for antenna diversity, Low Power Oscillator (LPO) for CYW43012, crystal oscillators for PSoC 6 MCU, modulation and integration capacitors to support CapSense and other passive components required for the proper working of PSoC 6 MCU and CYW43012. Pre-certified Type 1LV module with CYW43012 from Murata, LBEE59B1LV, is used for the ease of development. The antenna used is 2450AD14A5500 Dual Band 2.45GHz/5GHz Mini Chip Antenna from Johanson. The castellated PCB module has 137 castellated pads, which are used for different voltage rails and I/O signals of PSoC 6 MCU and CYW43012.

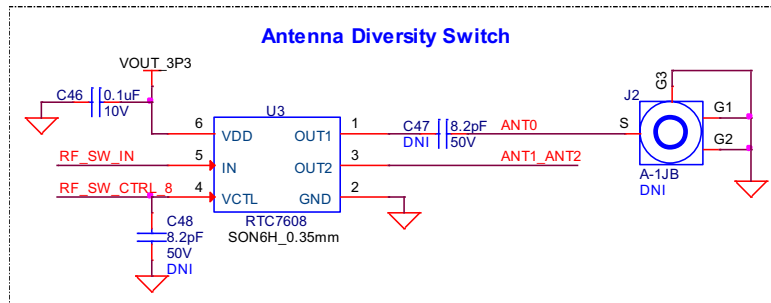
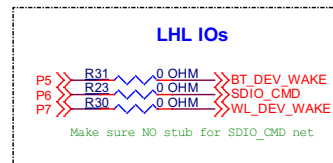
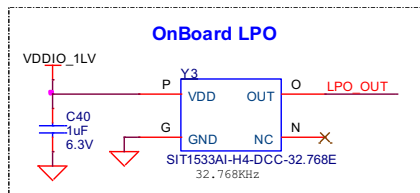
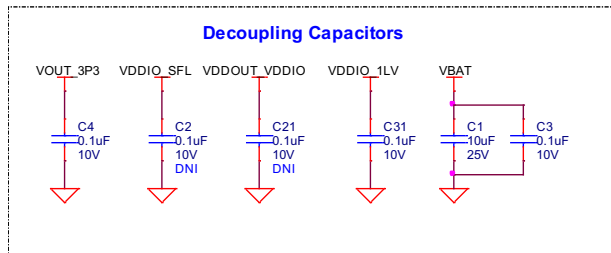
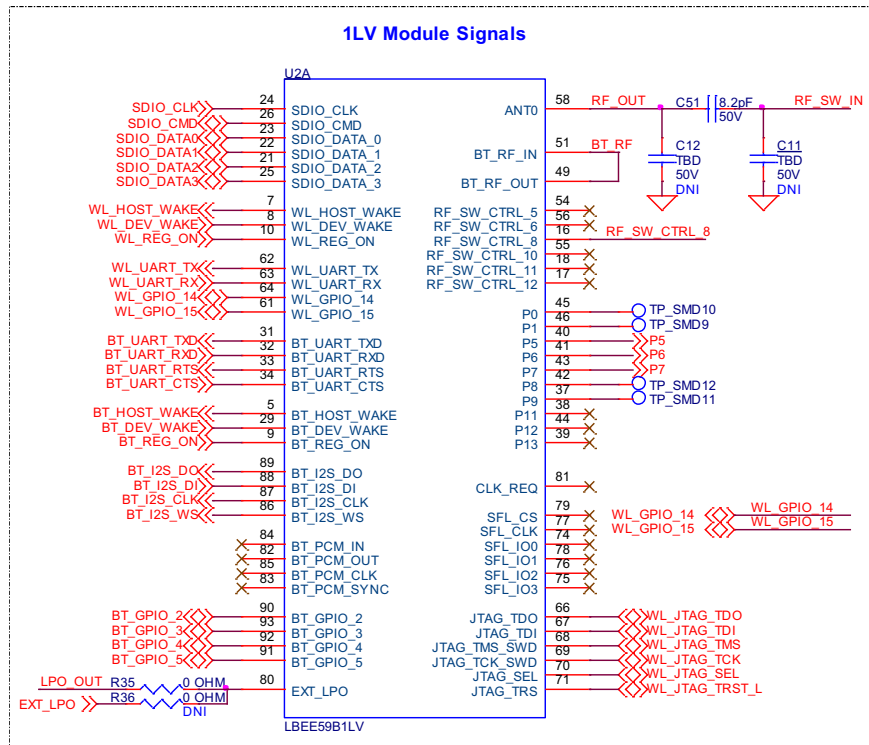
For more information, see the [PSoC 6 MCU webpage](#), [Murata Type 1LV webpage](#) and the [datasheet](#).

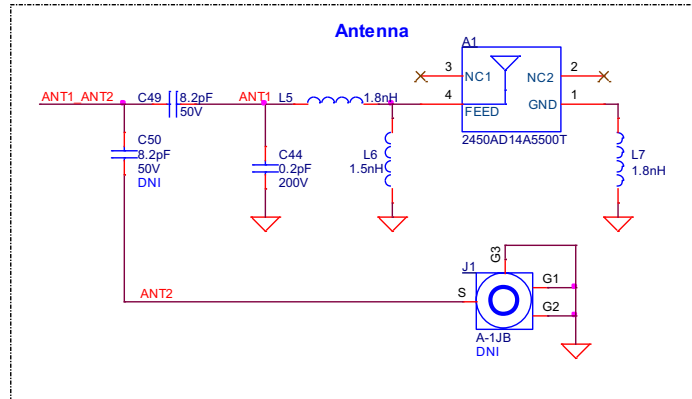
Figure 3-1. Schematics of CY8CMOD-062S2-43012



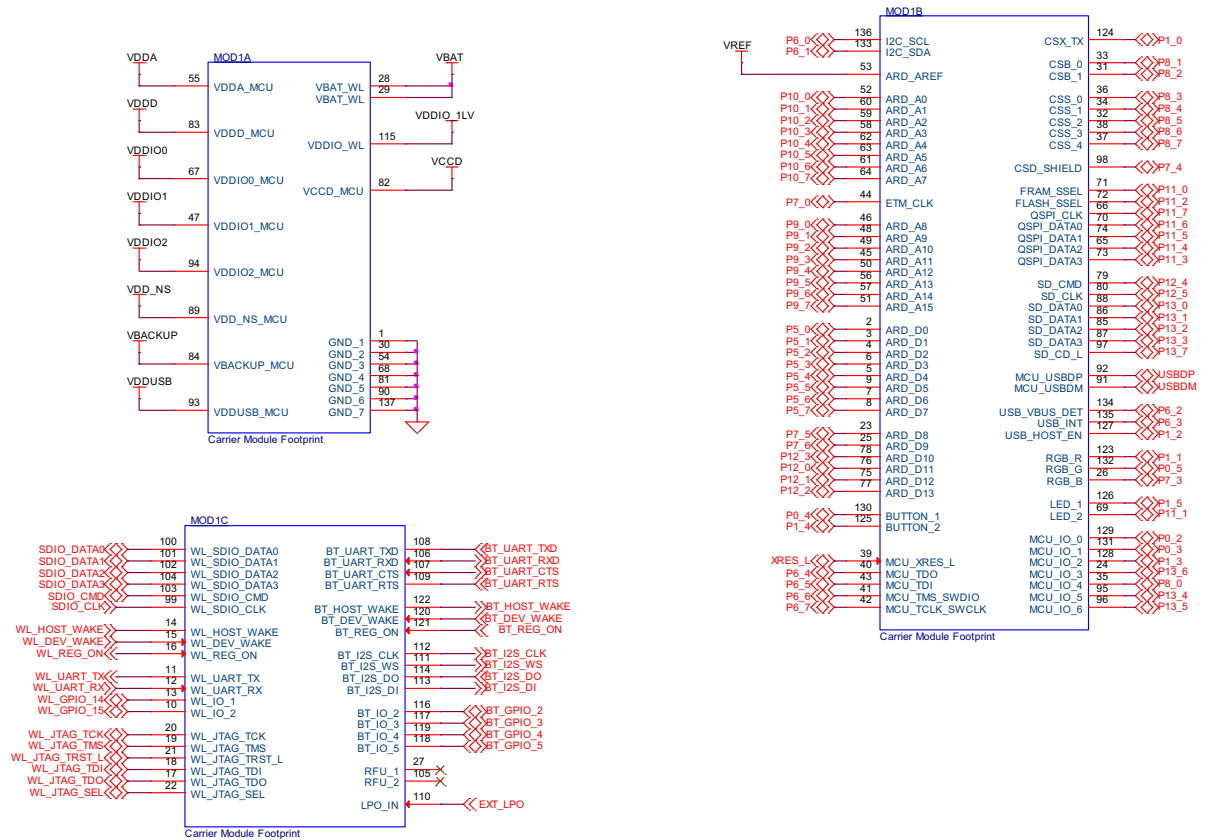








Carrier Module Footprint

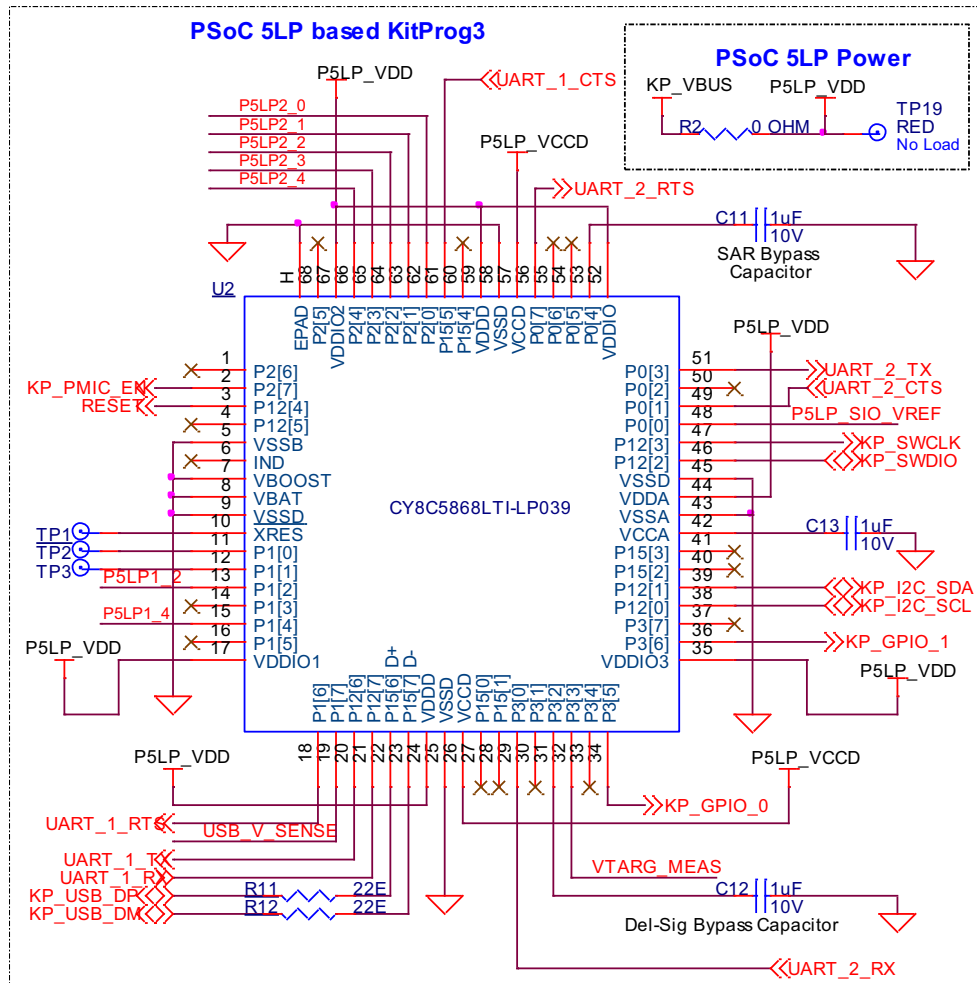


3.2.2 PSoC 5LP-based KitProg3 (U2)

An onboard PSoC 5LP (CY8C5868LTI-LP039) device is used as KitProg3 to program and debug PSoC 6 MCU. The PSoC 5LP device connects to the USB port of a PC through a USB connector and to the SWD and other communication interfaces of PSoC 6 MCU.

The PSoC 5LP device is a true system-level solution providing MCU, memory, analog, and digital peripheral functions in a single chip. For more information, visit the [PSoC 5LP web page](#). Also, see the [CY8C58LPxx Family datasheet](#).

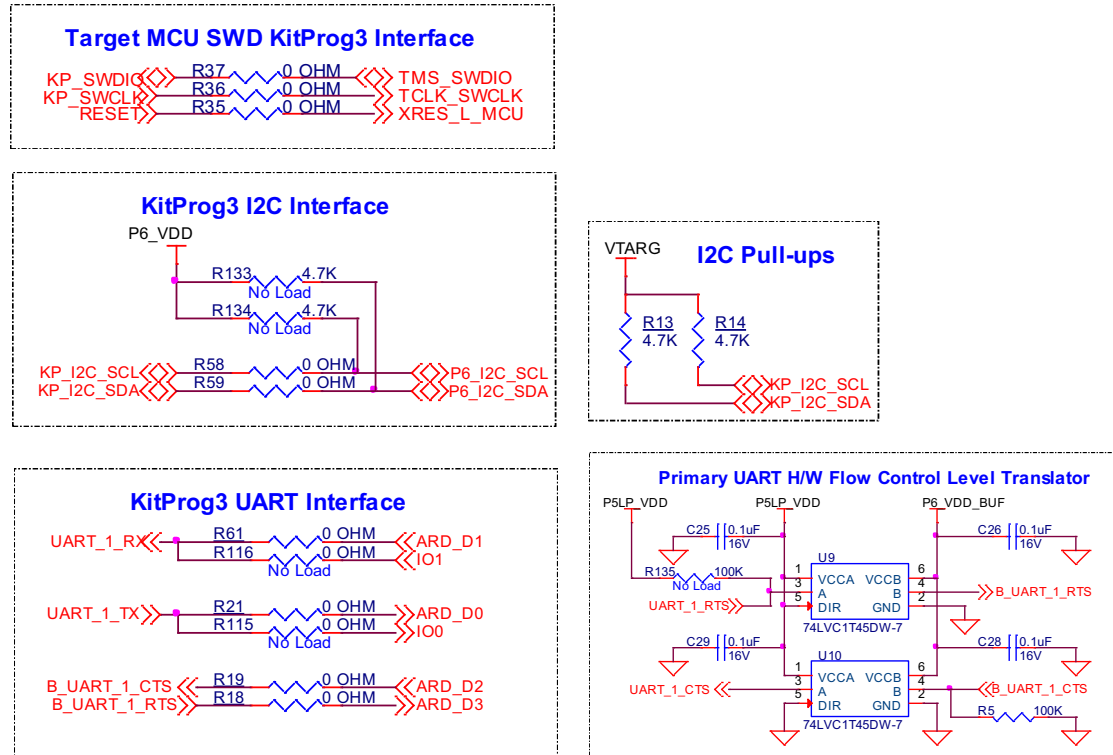
Figure 3-2. Schematics of PSoC 5LP based KitProg3



3.2.3 Serial Interconnection between PSoC 5LP and PSoC 6 MCU

In addition to the use as an onboard programmer, the PSoC 5LP device functions as an interface for the USB-UART and USB-I2C bridges, as shown in [Figure 3-3](#). The USB-Serial pins of the PSoC 5LP device are hard-wired to the I2C/UART pins of the PSoC 6 MCU. These pins are also available on the Arduino-compatible I/O headers.

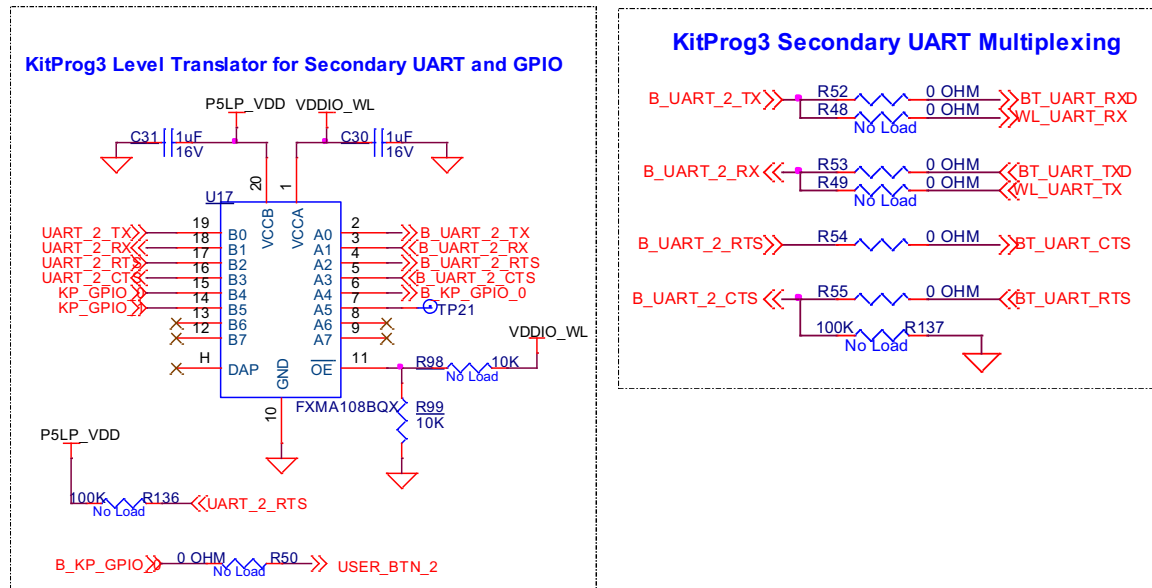
Figure 3-3. Schematics of Programming and Serial Interface Connections



3.2.4 Serial Interconnection Between PSoC 5LP and CYW43012

The PSoC 5LP device also has a secondary UART that is connected to the BT_UART of CYW43012 (Murata Type 1LV).

Figure 3-4. Serial Interconnection Between PSoC 5LP and CYW43012

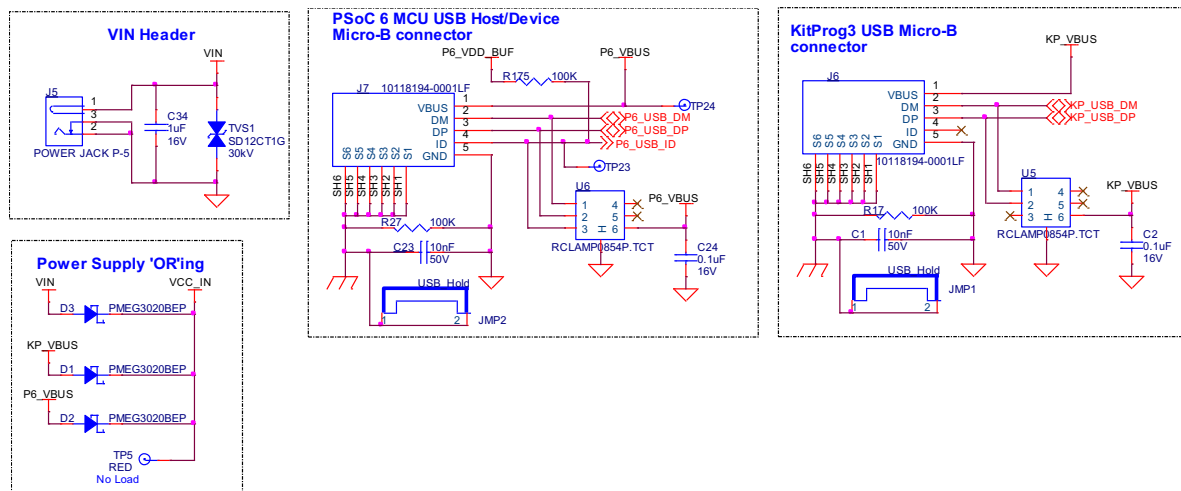


3.2.5 Power Supply System

The power supply system on this board is versatile, allowing the input supply to come from the following sources:

- 5V from the onboard USB Micro-B connectors (**J6** and **J7**)
- 7V–12V from external power supply through the VIN barrel jack (**J5**) or from an Arduino shield

Figure 3-5. Schematics of Power Supply Input and OR'ing



3.2.5.1 Voltage regulators

The power supply system is designed for the voltage configurations listed in [Table 3-1](#). Some configurations achievable on this kit are outside the operating range for the device. However, it is not possible to achieve all applicable configurations by changing jumper positions but rather requires re-work of respective 0-ohm resistors.

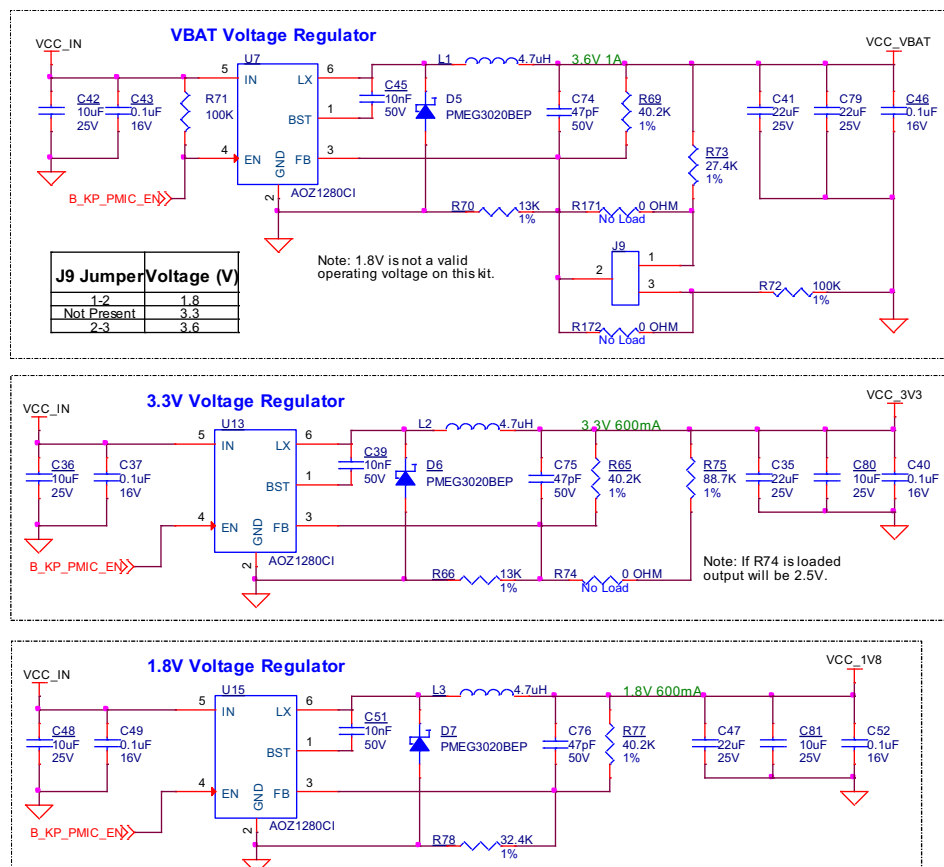
VDDIO_WL and VDDIO2_MCU must be at the same voltage since they power the SDIO interface between PSoC 6 MCU and CYW43012. Hence both are supplied by the VCC_VDDIO2_IN domain.

Three buck regulators **U15**, **U13** and **U7** are used to achieve 1.8 V, 3.3 V and 3.6 V outputs respectively. [Figure 3-6](#) shows the schematics of the voltage regulator circuits.

Table 3-1. Operating voltage ranges of domains

Voltage Domain	Carrier Module (MOD1) Power Pins powered by the domain	Operating Voltage		Voltage Configuration applicable in kit	Voltage Selection Header
		Min (V)	Max (V)		
VCC_VBAT	VBAT_WL	3.2	4.4	3.6V, 3.3V	J9
VCC_VDDIO2_IN	VDDIO2_MCU, VDDIO_WL	1.62	1.98	1.8V	J16 (not loaded)
VTARG	VDDD_MCU, VDDIO1_MCU, VDDA_MCU, VDD_NS_MCU, VBACKUP_MCU	1.7	3.6	1.8, 3.3V	J14
VCC_VDDIO0	VDDIO0_MCU	1.7	3.6	1.8, 3.3V	None (uses 0 Ohms)

Figure 3-6. Voltage Regulators



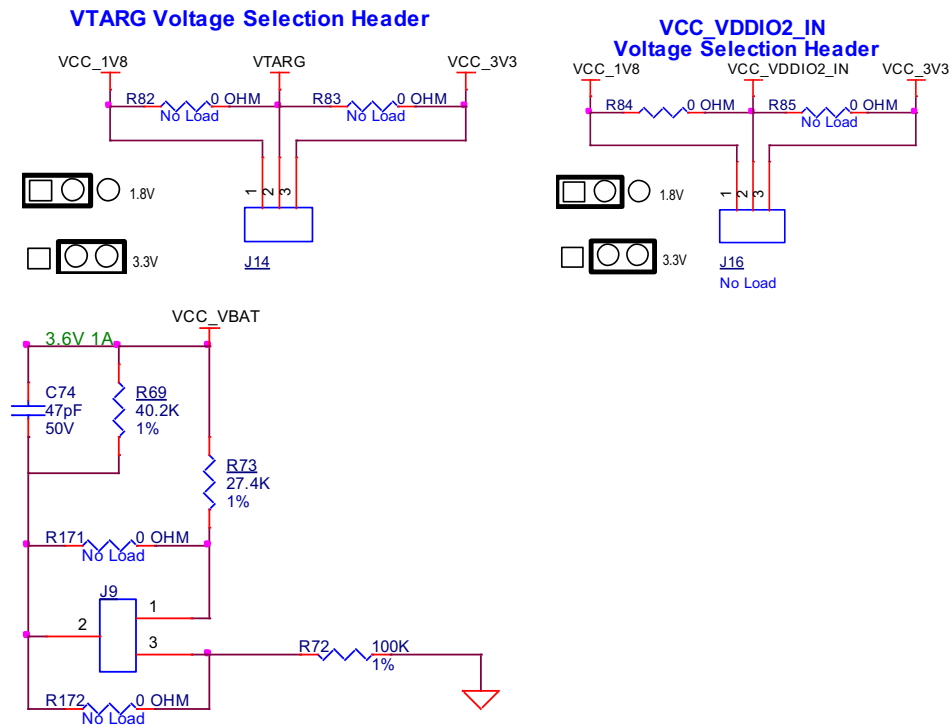
3.2.5.2 Voltage Selection

VCC_VBAT has a dedicated regulator that changes voltage by varying the feedback voltage through the resistor network at **J9**.

VTARG and VCC_VDDIO2_IN have dedicated 3-pin voltage selection headers **J14** and **J16** respectively that select between VCC_3V3 or VCC_1V8 voltages. [Figure 3-7](#) shows the schematics of the power selection circuits.

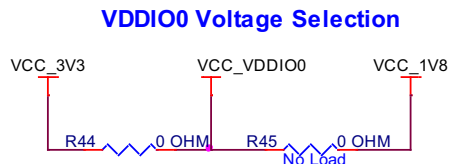
Note: In this kit, CYW43012 only works with VCC_VDDIO2_IN at VCC_1V8 configuration and hence by default, **R84** is loaded and **J16** is not loaded.

Figure 3-7. Voltage Selection Headers



VCC_VDDIO0 voltage can be selected between VCC_3V3 and VCC_1V8 using zero-ohm resistors. It is connected to VCC_3V3 by default as microSD card (powered by VCC_VDDIO0) works only at 3.3V. [Figure 3-8](#) shows the schematics of the voltage selection circuits.

Figure 3-8. Voltage Selection



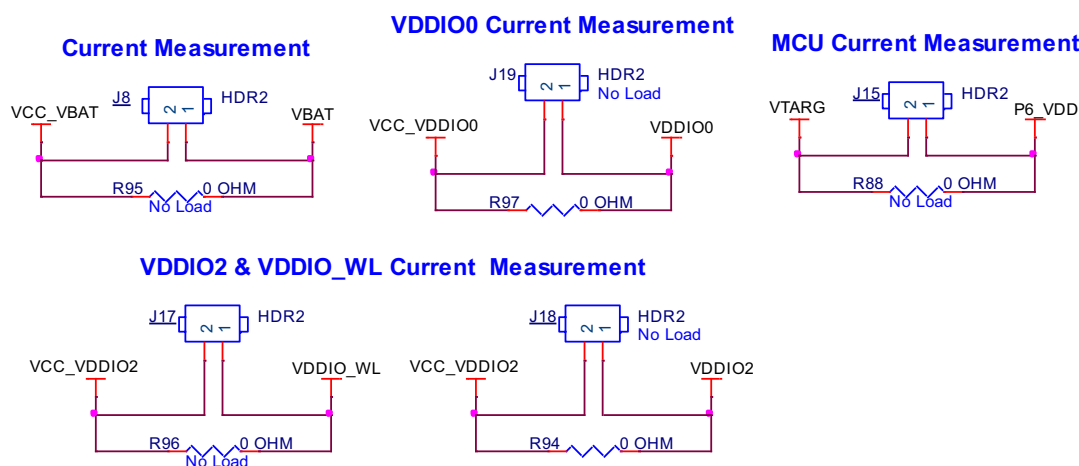
3.2.5.3 Current Measurement Headers

The current of the following domains have dedicated 2-pin headers to facilitate easy current measurement using an ammeter across the pins.

Table 3-2. Current Measurement Headers

Domain Name	Header Reference Designator	Loaded by default
VBAT	J8	Y
P6_VDD	J15	Y
VDDIO_WL	J17	Y
VDDIO2	J18	N
VDDIO0	J19	N

Figure 3-9. Current Measurement Headers



Note: When measuring P6_VDD current, make sure that the J25 jumper is removed. This will disconnect the potentiometer from VDDA and removes the leakage caused by it.

3.2.6 I/O Headers

3.2.6.1 Arduino-compatible Headers (J1, J2, J3, J4)

The board has four Arduino-compatible headers: **J1**, **J2**, **J3**, and **J4**. You can connect 3.3 V Arduino-compatible shields to develop applications based on the shield's hardware.

Note: 5-V shields are not supported and connecting a 5-V shield may permanently damage the board.

Note: All Arduino header pins are not connected to the same voltage reference. ARD_D[10:13] are powered by VDDIO0 whereas rest are powered by domains connected to VTARG. Hence arduino shields particularly that use ARD_D[10:13] must no be used when VTARG is 1.8V.

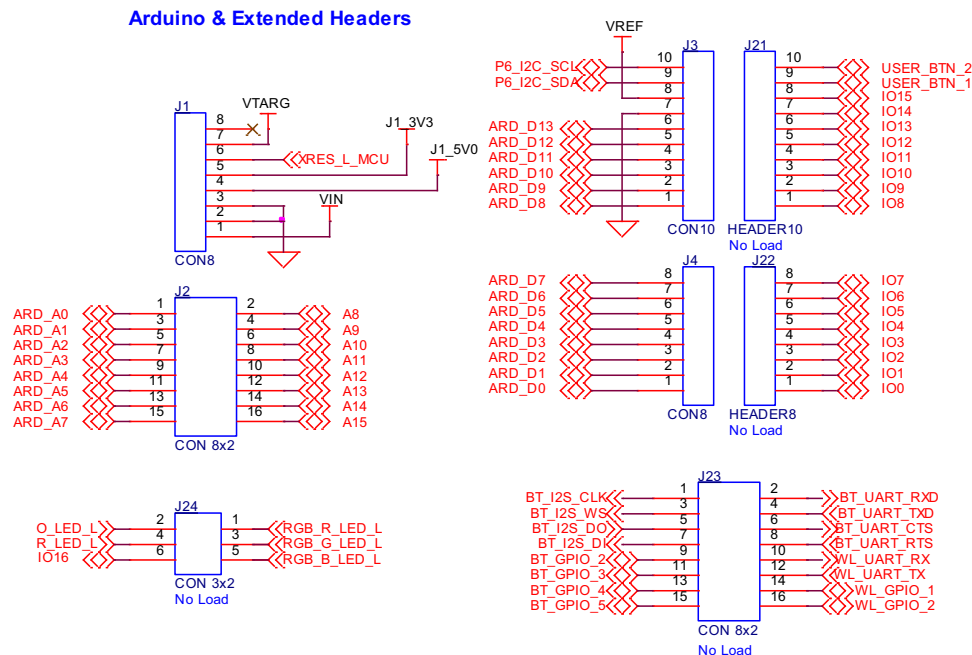
3.2.6.2 PSoC 6 MCU I/O Headers (J21, J22, and J24)

These headers provide connectivity to PSoC 6 MCU GPIOs that are not connected to the Arduino-compatible headers. Majority of these pins are multiplexed with onboard peripherals and are not connected to PSoC 6 MCU by default.

3.2.6.3 WL/BT I/O Headers (J23)

These headers provide connectivity to a few of the CYW43012 GPIOs that are available at the castellated pads. All these I/O work at VDDIO_WL voltage (1.8 V by default).

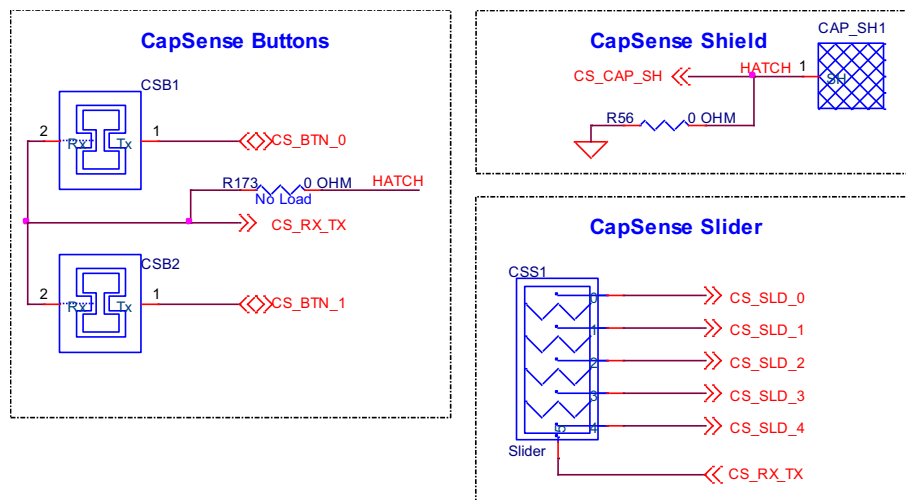
Figure 3-10. I/O Headers



3.2.7 CapSense Circuit

A CapSense slider and two buttons, all supporting both self-capacitance (CSD) and mutual-capacitance (CSX) sensing are connected to PSoC 6 MCU as Figure 3-11 shows. Three external capacitors - CMOD for CSD, CINTA and CINTB for CSX - are present on the CY8CMOD-062S2-43012. Note that CINTA can be reused as CSH. For details on using CapSense including design guidelines, see the [Getting Started with CapSense Design Guide](#).

Figure 3-11. Schematics of CapSense Circuit



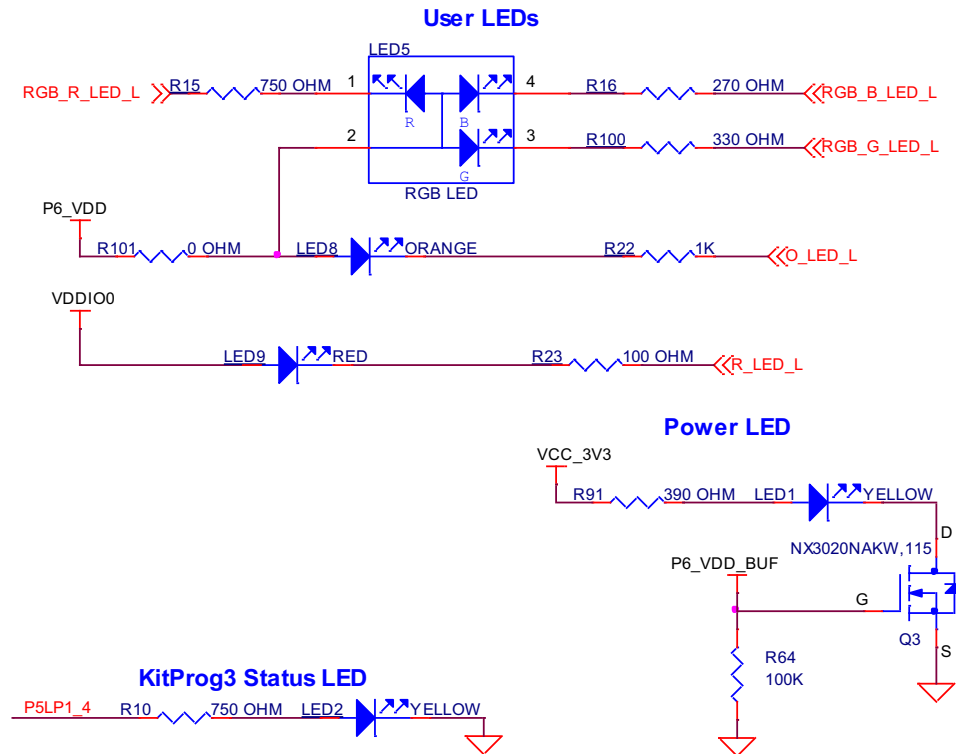
Simultaneous GPIO switching with unrestricted drive strengths and frequency can affect CapSense and ADC performance. For more details, see the Errata section of the corresponding device datasheet.

3.2.8 LEDs

LED2 (Yellow) indicates the status of KitProg3 (See the [KitProg3 User Guide](#) for details). **LED1** (Yellow) indicates the status of the power supplied to the board.

The board also has two user-controllable LEDs (**LED8** and **LED9**) and an RGB LED (**LED5**) connected to PSoC 6 MCU pins for user applications.

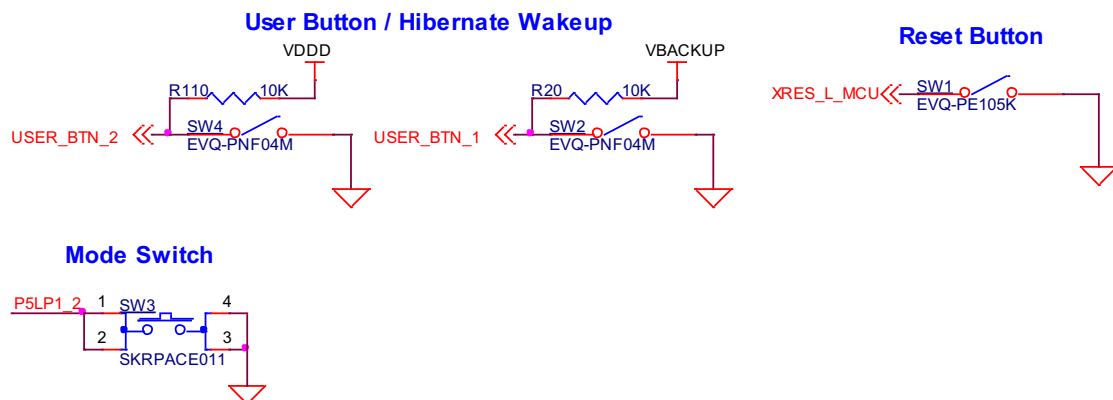
Figure 3-12. LEDs



3.2.9 Push Buttons

The board has a reset button, two user-controllable buttons and a KitProg3 Mode selection button. The reset button (**SW1**) is connected to the XRES pin of the PSoC 6 MCU and is used to reset the device. Two user buttons (**SW2** and **SW4**) are connected to pin P0[4] and P1[4] of the PSoC 6 MCU respectively. In addition, the Mode selection button (**SW3**) is connected to the PSoC 5LP device for programming mode selection (Refer to the [KitProg3 User Guide](#) for details). All buttons are active LOW configuration and short to GND when pressed. The CY8CMOD-062S2-43012 has a pull-up on the PSoC 6 MCU XRES line.

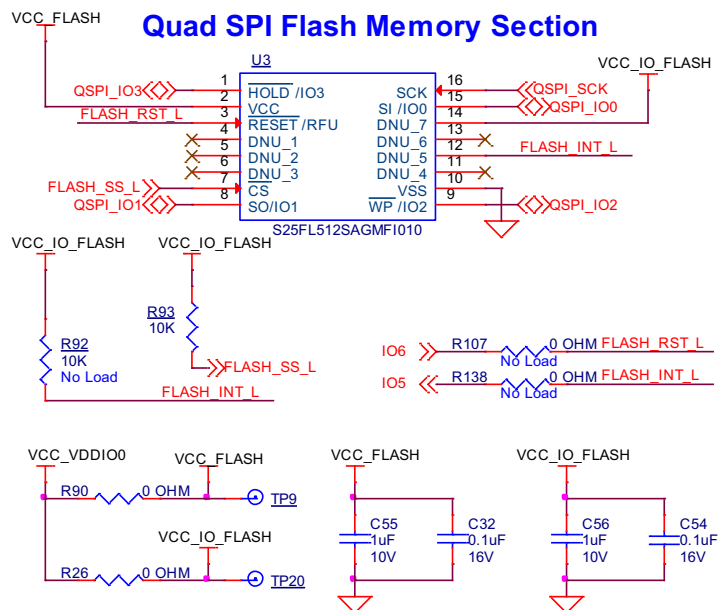
Figure 3-13. Schematics of Push Buttons



3.2.10 Cypress Quad SPI NOR Flash

The PSoC 62S2 Pioneer Board has a Cypress NOR flash memory (S25FL512SAGMFI010) of 512Mb capacity. The NOR flash is connected to the Quad SPI interface of the PSoC 6 MCU device. The NOR flash device can be used for both data and code with execute-in-place (XIP) support and encryption.

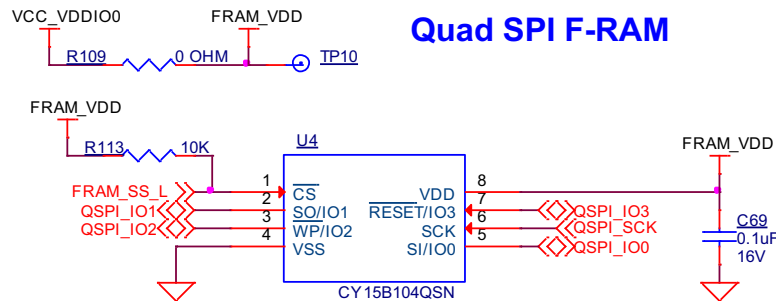
Figure 3-14. Schematics of QSPI Flash



3.2.11 Cypress Quad SPI F-RAM

The PSoC 62S2 Pioneer Board contains the CY15B104QSN Excelon™ F-RAM device, which can be accessed through Quad SPI interface. The F-RAM is 4-Mbit (512K × 8) and is capable of Quad SPI speed up to 108 MHz but PSoC 6 MCU is limited to 80 MHz.

Figure 3-15. Schematics of Quad SPI F-RAM

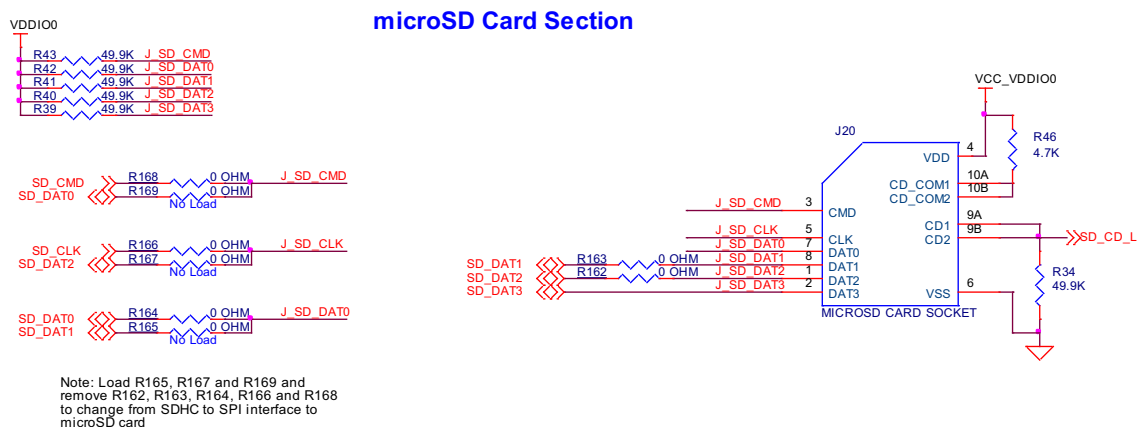


3.2.12 microSD card section

The PSoC 62S2 Pioneer Board contains a bottom-mounted microSD card holder with card detect pin that is connected to PSoC 6 MCU. It is powered by VDD_VDDIO0 (connected to VCC_3V3 by default). The PSoC 6 MCU is capable of UHS-I but is limited to High-Speed mode (50 MHz clock) in this kit.

By default, the PSoC 6 MCU device is connected using an SDHC interface but optionally can be connected using SPI by re-working a few zero-ohm resistors.

Figure 3-16. Schematics of microSD Card Section

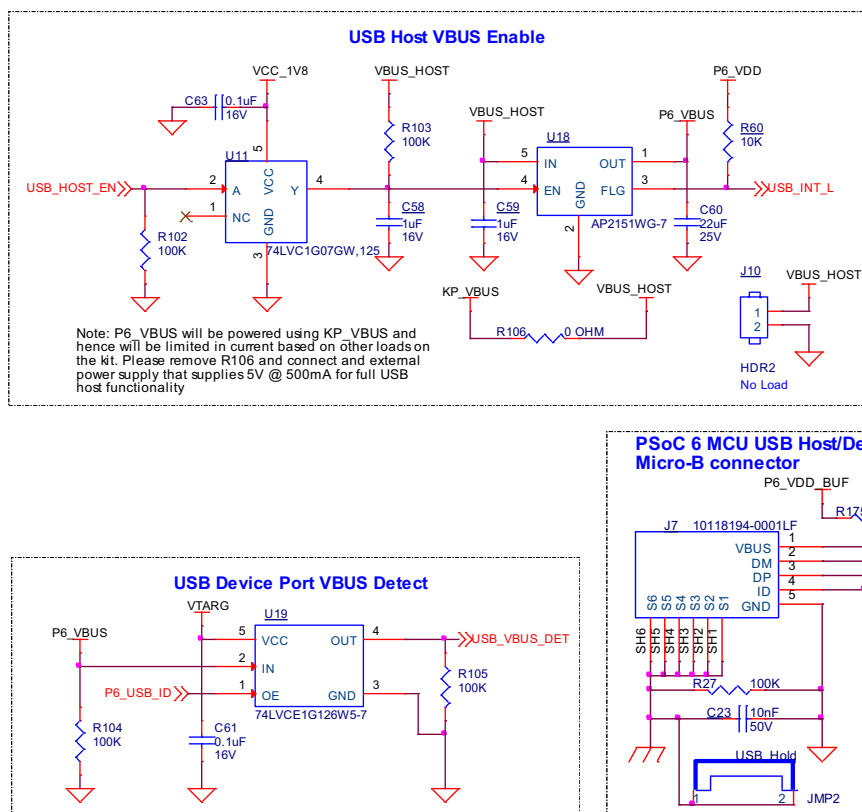


3.2.13 PSoC 6 USB Section

The board contains a micro-B USB connector for PSoC 6 MCU. It is capable of both device and host functionality. Although PSoC 6 MCU does not support USB-OTG, the hardware is compliant with it. By default, the PSoC 6 MCU device will work as a USB device; when an OTG cable (all such cables have ID pin connected to GND) is connected, it will work as USB Host.

As a USB Host, the board must provide power to a USB device that is connected to it. This power is provided by VBUS_HOST which is controlled by PSoC 6 MCU using a load switch. By default, VBUS_HOST is powered using KP_VBUS and optionally can be powered using external sources through J10.

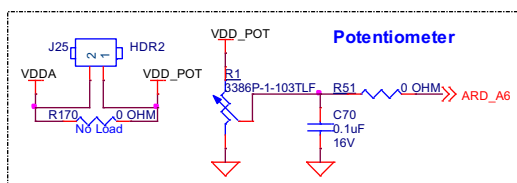
Figure 3-17. PSoC 6 USB



3.2.14 Potentiometer Section

The board contains a 10K potentiometer connected to A6 (P10[6]) pin of Arduino-header (J2). The fixed ends are connected to VDDA (VDD_POT through J25) and GND and hence may contribute to leakage current on the P6_VDD. Remove jumper J25 to disconnect power from the potentiometer when measuring P6_VDD current.

Figure 3-18. Schematics of Potentiometer



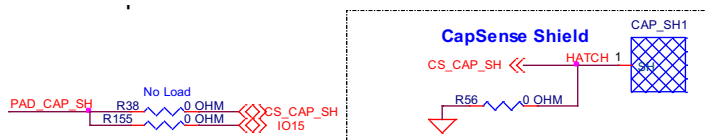
3.3 PSoC 62S2 Wi-Fi BT Pioneer Kit Rework

3.3.1 CapSense Shield

The hatched pattern around the CapSense buttons and slider are connected to ground. In case liquid tolerance is required, this pattern needs to be connected to a shield pin. This pattern can be connected to P7[4] by populating R38 and removing R56. Pin P7[4] needs to be configured as a shield pin in the firmware. CINTB (C15 on MOD1) connected to P7[2] must be configured as CSH in firmware when using CapSense Shield.

Connecting the hatched pattern to shield instead of ground will also reduce the parasitic capacitance of the sensors.

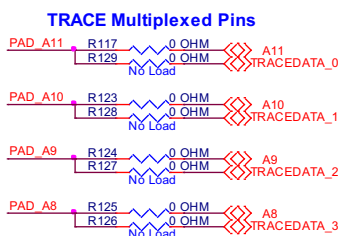
Figure 3-19. Schematics of CapSense Shield



3.3.2 ETM Trace Header

The 20-pin ETM trace header J12 is not loaded by default and the lines to the header are used as I/Os on header J2. To connect the PSoC 6 MCU to trace header, populate the resistors R126–R129 and remove resistors R117, R123–R125.

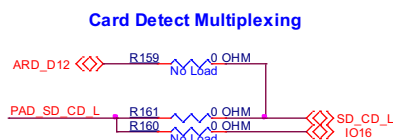
Figure 3-20. ETM Trace Header



3.3.3 microSD Card Detect Multiplexing

On the PSoC 6 MCU, the default card detect pin for the SHDC block is P12[1]. However, on this kit, P13[7] is connected to the card detect pin on the microSD card slot. Therefore, the firmware must be modified to use P13[7] as the card detect pin. In order to instead use the default PSoC 6 MCU card detect pin, remove R161 and load R159. In this case, P13[7] can optionally be used as a GPIO by loading R160 which connects it to an I/O header.

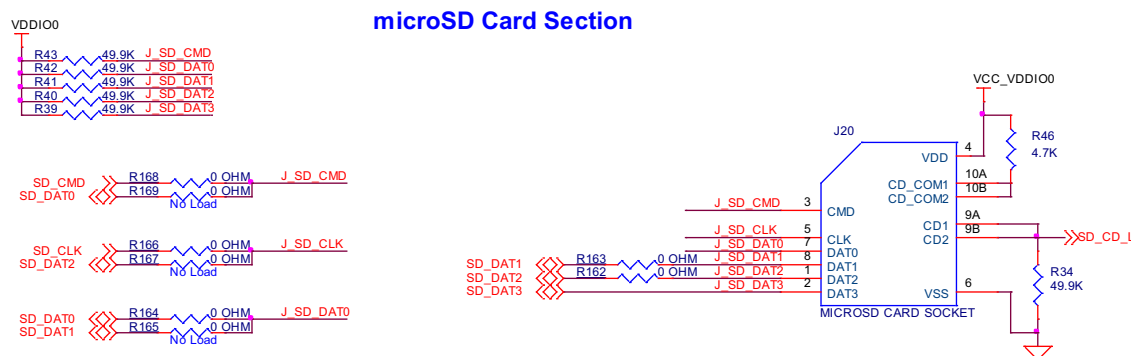
Figure 3-21. microSD Card Detect Multiplexing



3.3.4 microSD Card SPI Multiplexing

The microSD card is connected by a 6-pin SDHC interface by default i.e., CLK, CMD and DAT[0:3]. There is an optional provision to connect it over a 4-pin SPI interface i.e., CLK, MOSI, MISO and SSEL. To do this, load R165, R167, and R169 and remove R162, R163, R164, R166, and R168.

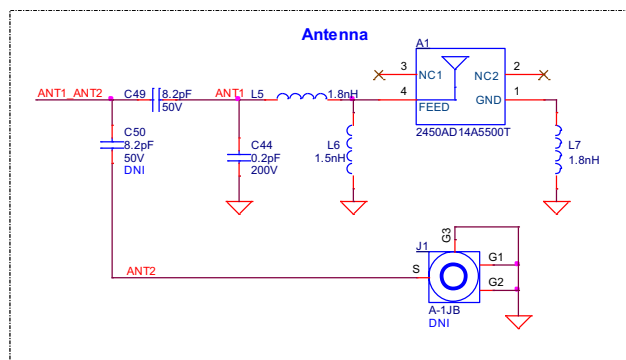
Figure 3-22. microSD Card SPI Multiplexing



3.3.5 U.FL (UMCC) Connector for External Antenna

The RF output of CYW43012 is connected to the chip antenna by default. To disconnect the chip antenna and connect an external antenna, remove C49 and populate C50, J1 on CY8CMOD-062S2-43012.

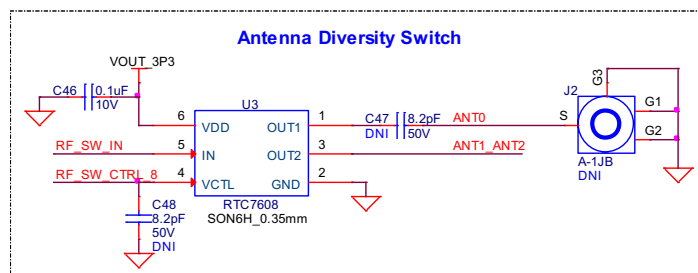
Figure 3-23. U.FL (UMCC) Connector for External Antenna



3.3.6 U.FL (UMCC) Connector for Antenna Diversity

To evaluate antenna diversity, an external antenna can be connected to the output of antenna diversity RF switch by populating C47 and J2 on CY8CMOD-062S2-43012.

Figure 3-24. U.FL (UMCC) Connector for Antenna Diversity



3.4 Bill of Materials

Refer to the BOM files in the [kit webpage](#).

3.5 Frequently Asked Questions

1. How does CY8CKIT-062S2-43012 handle a voltage connection when multiple power sources are plugged in?

There are three different options to power the baseboard; KitProg3 Micro-B USB connector (**J6**), PSoC 6 Micro-B USB connector (**J7**), and External DC supply via VIN connector (**J5**). The voltage from each of the sources is passed through ORing diodes that supply VCC_IN.

2. What are the input voltage tolerances? Is there any overvoltage protection on this kit?

Input voltage levels are as follows:

Table 3-3. Input voltage levels

Supply	Typical I/P Voltage	Absolute max
USB Micro-B connector (J6 , J7)	4.5 V to 5.5 V	5.5 V
VIN connector (J5)	7 V to 12 V	18 V

There is no overvoltage protection on this kit.

3. Why is the voltage of the kit restricted to 3.3 V? Can't it drive external 5-V interfaces?

PSoC 6 MCU is not meant to be operated at voltages greater than 3.6 V. Powering PSoC 6 to more than 4 V will damage the chip. It is recommended to power PSoC 6 MCU at 3.3 V.

4. I am unable to program the target device.

- a. Check **J15** to ensure that jumper shunt is placed.
- b. Make sure that no external devices are connected to the external programming header J11.
- c. Update your KitProg3 version to the latest one using the steps mentioned in the [KitProg3 User Guide](#).

5. What additional overlays can be used with the CapSense?

Any kind of overlays (up to 5-mm thickness) like wood, acrylic, and glass can be used with CapSense. Note that additional tuning may be required when the overlay is changed.

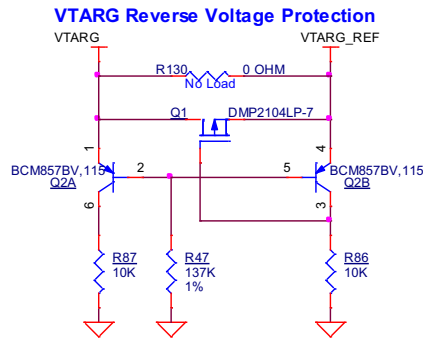
6. Can I power the kit using external program/debug headers J11 and J12?

No, this is not possible by default in this board. The target MCU is powered by on-board regulators only and hence one of the 3 main sources (**J5**, **J6** and **J7**) must be present.

There is a protection circuit that prevents reverse voltage from VTARG_REF to VTARG. Hence the board can't be powered through **J11** and **J12**. However this can be by-passed by loading R130.

Note: This modification is not recommended as the target MCU will have no protection and will be permanently damaged if 5V is supplied.

Figure 3-25. VTARG Reverse Voltage Protection



Note: VTARG_REF is only output voltage sense line for external debuggers. PSoC 6 can't be powered using external debugging headers J11 and J12

Note: If R130 is loaded and external power is used, make sure to remove jumper shunt from J14 to prevent reverse voltage to on-board regulator

Revision History



Document Revision History

Document Title: CY8CKIT-062S2-43012 PSoC 62S2 Wi-Fi BT Pioneer Kit Guide			
Document Number: 002-28109			
Revision	ECN Number	Issue Date	Description of Change
**	6664175	09/19/2019	New kit guide.
*A	6703552	10/17/2019	Updated Introduction chapter on page 7: Updated "Kit Contents" on page 8: Updated Figure 1-1 . Updated "Board Details" on page 9: Updated Table 1-1 . Updated Kit Operation chapter on page 18: Updated "Theory of Operation" on page 18: Updated description. Updated "KitProg3: On-Board Programmer/Debugger" on page 23: Updated "Programming and Debugging using ModusToolbox" on page 23: Added "Using the OOB Example – PSoC 6 MCU: Hello World" on page 26. Updated "USB-I2C Bridge" on page 28: Updated Figure 2-15 .
*B	6713283	10/25/2019	Updated Safety and Regulatory Compliance Information chapter on page 5: Updated description. Updated "General Safety Instructions" on page 6: Updated "Handling Boards" on page 6: Updated description. Updated Introduction chapter on page 7: Updated "Board Details" on page 9: Updated Table 1-1 . Updated Kit Operation chapter on page 18: Updated "Theory of Operation" on page 18: Updated description. Updated "KitProg3: On-Board Programmer/Debugger" on page 23: Updated "Programming and Debugging using ModusToolbox" on page 23: Updated "Using the OOB Example – PSoC 6 MCU: Hello World" on page 26: Updated description.

Document Revision History (*continued*)

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Document Number: 002-28109			
Revision	ECN Number	Issue Date	Description of Change
*C	6754704	12/17/2019	Updated Introduction chapter on page 7 : Updated "Board Details" on page 9: Updated Figure 1-2 . Updated Kit Operation chapter on page 18 : Updated "Theory of Operation" on page 18: Updated Figure 2-3 . Updated "KitProg3: On-Board Programmer/Debugger" on page 23: Updated "Programming and Debugging using ModusToolbox" on page 23: Updated Figure 2-5 . Updated Hardware chapter on page 29 : Updated "Hardware Functional Description" on page 29: Updated "Power Supply System" on page 36: Updated "Voltage regulators" on page 37: Updated Figure 3-6 .
*D	6792835	01/30/2020	Updated Introduction chapter on page 7 : Updated "Board Details" on page 9: Updated description. Updated Hardware chapter on page 29 : Updated "Hardware Functional Description" on page 29: Updated "CY8CMOD-062S2-43012 (MOD1)" on page 29: Updated Figure 3-1 .
*E	6795725	02/11/2020	Updated Hardware chapter on page 29 : Updated "Hardware Functional Description" on page 29: Updated "CY8CMOD-062S2-43012 (MOD1)" on page 29: Updated hyperlinks. Updated Figure 3-1 .
*F	7062647	02/02/2021	Updated Safety and Regulatory Compliance Information chapter on page 5 : Removed description. Updated "Regulatory Compliance Information" on page 5: Updated description. Removed "Regulatory Statements and Product Labeling". Updated to new template.
*G	7111681	03/26/2021	Updated Safety and Regulatory Compliance Information chapter on page 5 : Updated "Regulatory Compliance Information" on page 5: Updated description.