CY8CKIT-029 PSoC® LCD Segment Drive Expansion Board Kit Guide

Doc. # 001-55415 Rev. *K

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Contents

Safety Information

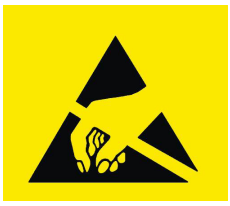
Regulatory Compliance

The CY8CKIT-029 is intended for use as a development platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure. This may cause interference to other electrical or electronic devices in close proximity.

In a domestic environment, this product may cause radio interference. In this case, the user may be required to take adequate prevention measures. Also, the board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

The CY8CKIT-029 as shipped from the factory has been verified to meet with requirements of CE as a Class A product.



The CY8CKIT-029 contains electrostatic discharge (ESD) sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY8CKIT-029 boards in the protective shipping package.

End-of-Life / Product Recycling

This Kit has end-of life after 5 years of date of manufactured mentioned on the back side of the Box. Please contact your nearest recycler for dispositioning the kit.

General Safety Instructions

Electrostatic Discharge (ESD) Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If one is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to chassis ground (any unpainted metal surface) on your board when handling parts.

Handling Boards

CY8CKIT-029 boards are sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static free surface. Use a conductive foam pad if available. Do not slide board over any surface.

1. Introduction

The CY8CKIT-029 PSoC® LCD Segment Drive Expansion Board Kit (EBK) is an expansion board used with either CY8CKIT-001 PSoC Development Kit or CY8CKIT-030 PSoC 3 Development Kit or CY8CKIT-050 PSoC 5LP Development Kit. It allows you to evaluate PSoC's LCD drive capability by designing your own projects with the easy-to-use LCD segment component in Cypress's PSoC Creator™ or altering the code examples provided with this kit.

The CY8CKIT-029 PSoC LCD Segment Drive EBK is based on the PSoC family of devices. PSoC is a programmable system-on-chip platform for 8-, 16-, and 32-bit applications. With PSoC, you can create the exact combination of peripherals and integrated proprietary IP to meet the needs of your applications.

The included example projects support PSoC 3 (8051) and PSoC 5LP (ARM Cortex-M3).

1.1 Kit Contents

This kit contains:

- PSoC LCD Segment Drive Expansion Board
- Quick Start Guide
- Kit CD

Inspect the contents of the kit; if you do not find any part, contact your nearest Cypress sales office for help.

1.2 PSoC Creator

Cypress's PSoC Creator software is a state-of-the-art, easy-to-use software development Integrated Development Environment (IDE). It introduces a hardware and software co-design environment based on classic schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Create and share user defined, custom peripherals using hierarchical schematic design.
- Automatically place and route select components and integrate simple glue logic normally residing in discrete muxes.
- Trade off hardware and software design considerations allowing you to focus on what matters and get to market faster.

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support PSoC 3, PSoC 4 and PSoC 5LP.

1.3 Getting Started

To get started, see the Kit Operation chapter on page 13 to learn how to program the PSoC 3/5LP device. A code example is used to explain how to use the PSoC LCD segment drive expansion board with the CY8CKIT-001 DVK / CY8CKIT-030 PSoC 3 DVK / CY8CKIT-050 PSoC 5LP DVK. Hardware chapter on page 21 provides details of the hardware. Code Examples chapter on page 29 guides you to create simple code examples. The Appendix on page 49 provides the schematics and bill of materials (BOM) associated with the expansion board.

1.4 Additional Learning Resources

Visit http://www.cypress.com for additional learning resources in the form of datasheets, technical reference manual, and application notes.

1.4.1 Beginner Resources

AN54181 - Getting Started with PSoC® 3

AN77759 - Getting Started with PSoC 5LP

PSoC Creator Training

1.4.2 Engineers Looking for More

AN54460 - PSoC® 3, PSoC 4 and PSoC 5LP Interrupts

AN52705 - PSoC® 3 and PSoC 5LP - Getting Started with DMA

AN52701 - PSoC® 3 and PSoC 5LP - Getting Started with Controller Area Network (CAN)

AN54439 - PSoC® 3 and PSoC 5LP External Crystal Oscillators

AN52927 - PSoC® 3 and PSoC 5LP - Segment LCD Direct Drive

Cypress continually strives to provide the best support. Click here to view a growing list of application notes for PSoC 3, PSoC 4 and PSoC 5LP.

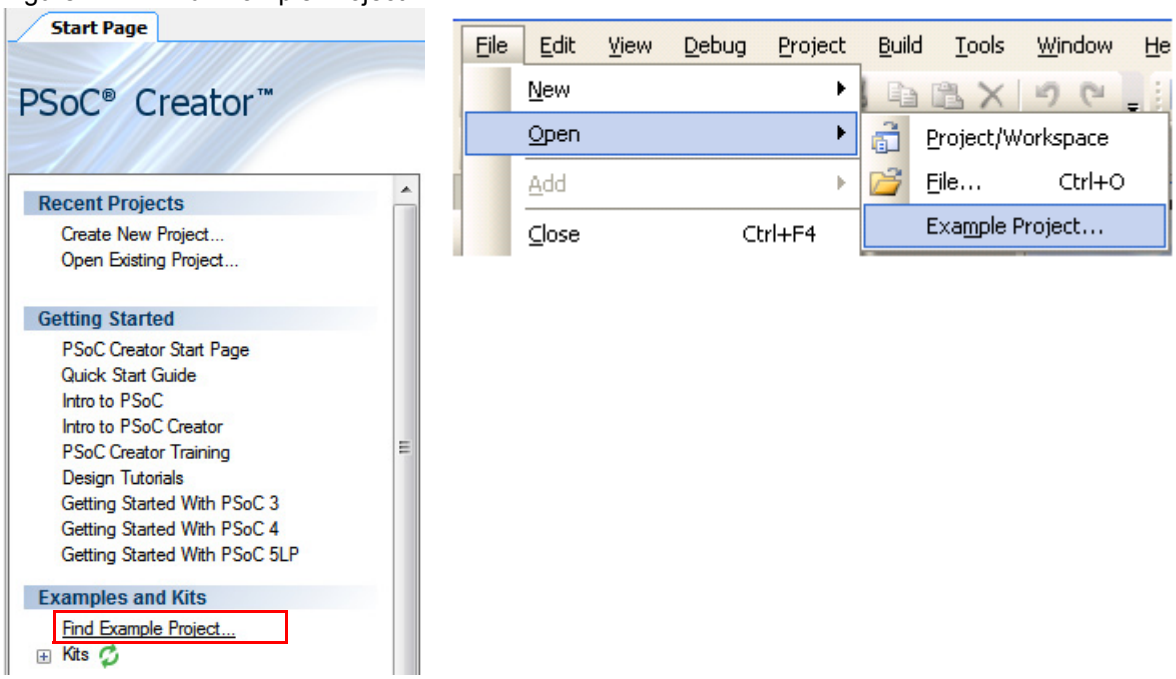
1.4.3 Learning from Peers

Cypress Developer Community Forums

1.4.4 More Code Examples

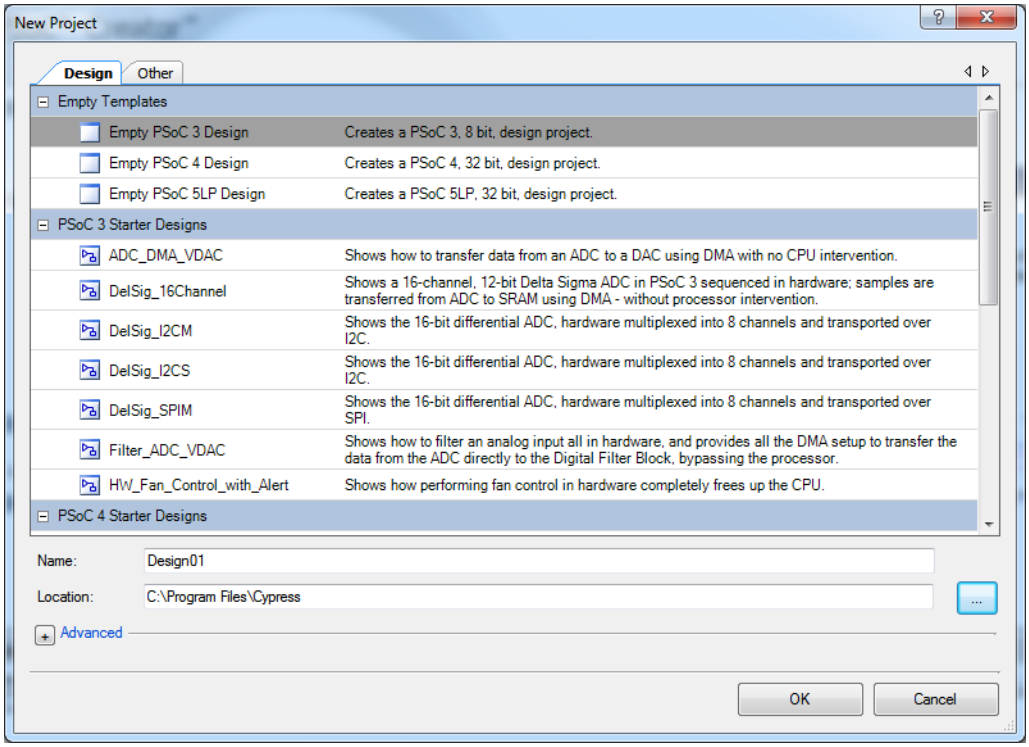
PSoC Creator provides several example projects that make code development fast and easy. To access these example projects, click on **Find Example Project…** under the **Example and Kits** section in the **Start Page** of PSoC Creator or navigate to **File > Open > Example Project…**

Figure 1-1. Find Example Project



The Find Example Project section has various filters that help you locate the most relevant project. PSoC Creator provides several starter designs. These designs highlight features that are unique to PSoC devices. They allow you to create a design with various components, instead of creating an empty design; the code is also provided. To use a starter design for your project, navigate to **File > New > Project** and select the design required.

Figure 1-2. New Project



The example projects and starter designs are designed for the CY8CKIT-001 PSoC Development Kit. However, these projects can be converted for use with the CY8CKIT-030 PSoC 3 Development Kit or CY8CKIT-050 PSoC 5LP Development Kit by following the procedure in the knowledge base article Migrating Project from CY8CKIT-001 to CY8CKIT-030 or CY8CKIT-050 LP.

1.5 Document Conventions

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\ ...cd\icc\
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes Cautions or unique functionality of the product.

2. Installation

2.1 CD Installation

Follow these steps to install the CY8CKIT-029 PSoC LCD Segment Drive EBK software:

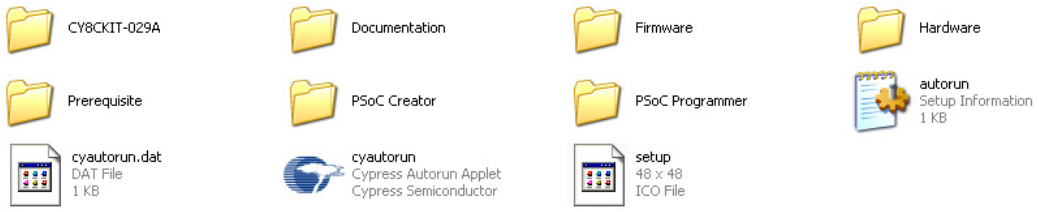
1. Insert the kit CD into the CD drive of your computer. The CD is designed to auto-run and the PSoC LCD Segment Drive EBK menu appears.

Figure 2-1. CY8CKIT-029 Kit Menu

Note If auto-run does not execute, double-click ***cyautorun.exe*** in the root directory of the CD.

2. Use Windows Explorer to browse documents inside the PSoC LCD Segment Drive EBK folder.

Figure 2-2. Kit CD Folder



Note After the installation is complete, the kit contents are found at the following location:

`<Install_Directory>:\CY8CKIT-029A\<version>`

2.2 Install Hardware

No hardware installation is required for this kit.

2.3 Install Software

When installing the PSoC LCD segment drive EBK, the installer checks if the prerequisite software is installed in your system. These include PSoC Creator, PSoC Programmer, Windows Installer, .NET, and KEIL Complier. If these applications are not installed, the installer installs them in your PC before installing the kit. If Acrobat Reader application is not installed in your PC, then the installer provides link to install the same. However, this does not prevent kit installation but Adobe reader is required to view the kit documents.

The following software are provided in the CD:

- PSoC Creator 3.0 or later
- PSoC Programmer 3.19.1 or later
  Note Choose “Typical” type of installation for all installations.

2.4 Verify Kit version

To know the kit revision, look for the white sticker on the back of the kit box. If the revision reads CY8CKIT-029 Rev **, then congratulations, you own the latest version.

You can purchase the latest version of the kit at http://www.cypress.com/go/CY8CKIT-029.

3. Kit Operation

3.1 Introduction

The CY8CKIT-029 PSoC LCD Segment Drive EBK code examples are designed using a display with many segments (8 common lines by 16 segment lines giving 128 segments).

- **Code Example 1: LCD_Seg_Example1_Battery_Meter**

This example demonstrates the battery charge indicator along with the 14-segment display of the LCD glass by implementing a battery meter.

- **Code Example 2: LCD_Seg_Example2_StopWatch**

This example implements a stopwatch using the RTC component in PSoC Creator. The hours, minutes, and seconds (HH:MM:SS) are displayed on the 14-segment LCD display.

See Code Examples on page 29 for more information.

Note The suffix <xxx> in the project name indicates the DVK on which the project works. The suffixes are:

009A - The project with this suffix works on CY8CKIT-009 (CY8C38 Processor Module) using CY8CKIT-001 DVK

010 - The project with this suffix works on CY8CKIT-010 (CY8C58LP Processor Module) using CY8CKIT-001 DVK

030 - The project with this suffix works on CY8CKIT-030 DVK

050 - The project with this suffix works on CY8CKIT-050LP DVK

3.2 Programming the device

3.2.1 Programming a PSoC 3/PSoC 5LP Device (processor module) on a CY8CKIT-001 DVK

The code examples are provided in the documentation section of the kit CD. This section provides details on programming the PSoC 3 device.

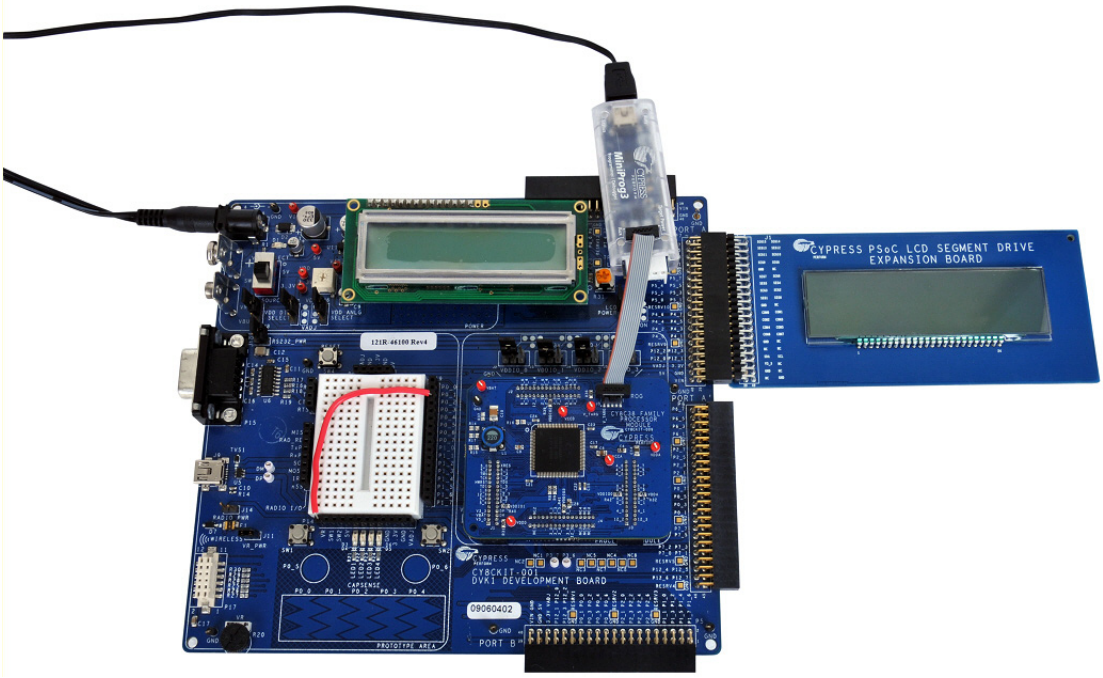
To program the ‘Battery Meter’ example to the PSoC 3 silicon, follow these steps:

1. Place the PSoC 3/PSoC 5LP processor module on the CY8CKIT-001 DVK.
2. Power the DVK using either battery connections or a wall power unit.
3. Connect the MiniProg3 JTAG cable to the JTAG connector, both on MiniProg3 and the PSoC 3 processor module. Connect the MiniProg3 to a host PC USB high-speed port using a USB cable.

The connections for steps 1 to 3 are shown in Figure 3-1.

Note The figures are shown for PSoC 3 processor module. The same connections need to be done if PSoC 5LP processor module is used.

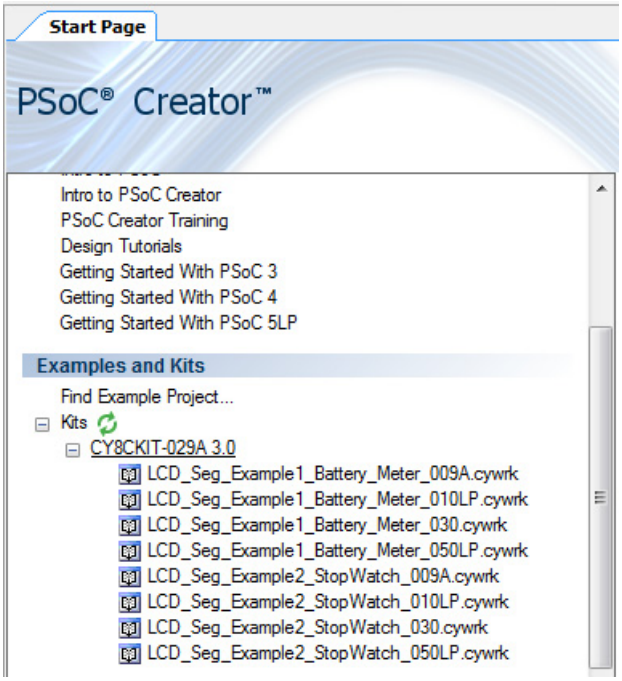
Figure 3-1. PSoC 3 Processor Module, Power, and MiniProg3 Connection with CY8CKIT-001 DVK



Note See the *CY8CKIT-001_PSoC_Development_Kit_Guide in* www.cypress.com/go/cy8ckit-001 for details on connecting and programming PSoC devices.

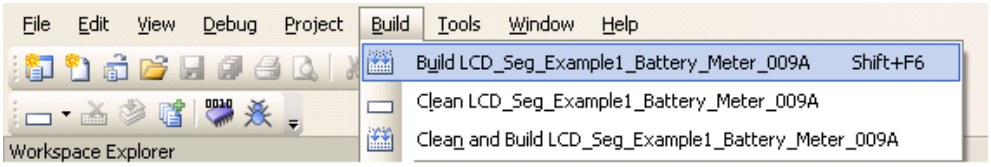
4. Click on the relevant code example i.e., LCD_Seg_Example1_Battery_Meter_009A for PSoC 3 module and LCD_Seg_Example1_Battery_Meter_010LP for PSoC 5LP module, located in **Examples and Kits** on the Start Page of PSoC Creator.

Figure 3-2. Start Page



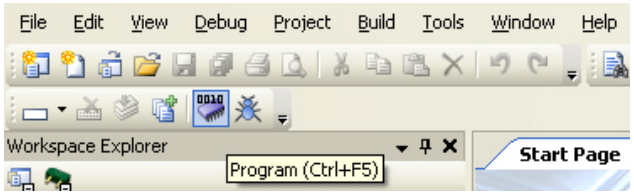
5. Create a folder in the desired location and click **OK**. The project opens in PSoC Creator and is saved in that folder.
6. Build the project by selecting the **Build** option.

Figure 3-3. Build Project



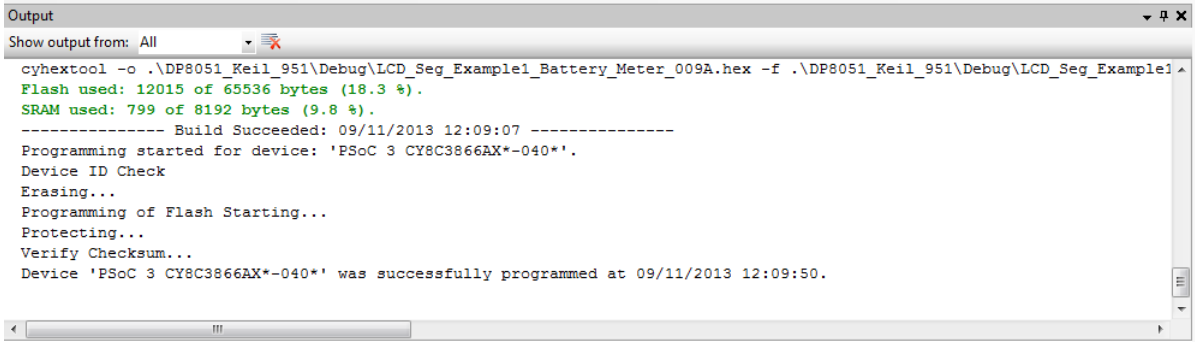
7. Click the **Program** icon.

Figure 3-4. Program Option



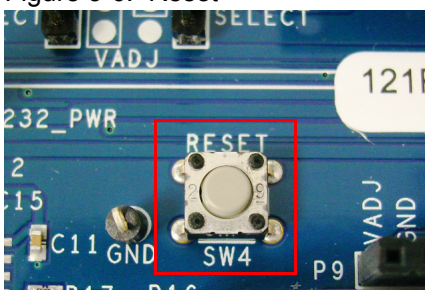
8. The project is programmed successfully, as shown in Figure 3-5.

Figure 3-5. Programming Successful



9. Reset the device by pressing the SW4 switch on the DVK; see Figure 3-6.

Figure 3-6. Reset



3.2.2 Programming a PSoC 3/PSoC 5LP Development Kit

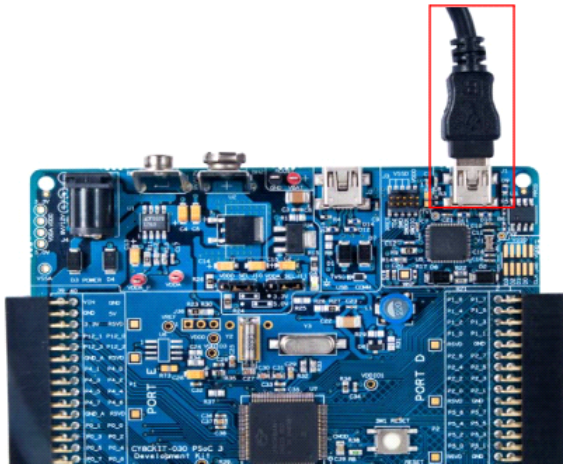
This section provides details on programming the PSoC 3/ PSoC 5LP Development Kit.

The default programming interface for the board is a USB based on-board programming interface.

To program the device, follow the following steps:

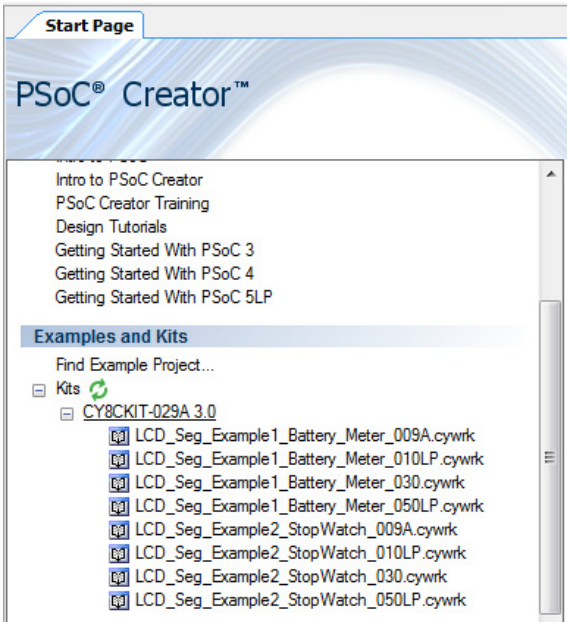
1. Connect the DVK to PC using a USB cable connected at the programming USB connector J1 and wait until the DVK gets enumerated as DVKProg in case of CY8CKIT-030 and DVKProg5 incase of CY8CKIT-050LP, as shown in Figure 3-7.
   Note: The figures are shown for CY8CKIT-030. The same connections need to be done if CY8CKIT-050LP is used.

Figure 3-7. Connect USB Cable to J1



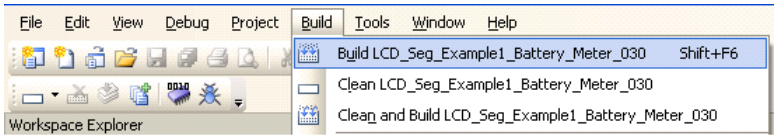
2. Click on the code example, LCD_Seg_Example1_Battery_Meter_030/ LCD_Seg_Example1_Battery_Meter_050LP, located in Examples and Kits on the Start Page of PSoC Creator.

Figure 3-8. Start page



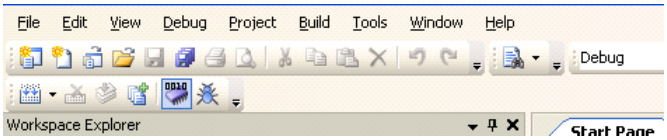
3. Create a folder in the desired location and click OK. The project opens in PSoC Creator and is saved in that folder.
4. Build the project by selecting the Build option.

Figure 3-9. Build Project



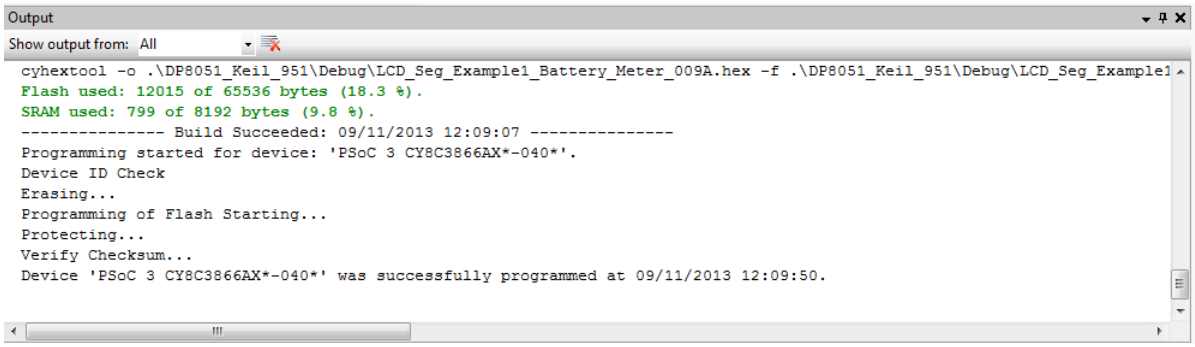
5. Click the Program icon.

Figure 3-10. Program Option



6. The project is programmed successfully, as shown in Figure 3-11.

Figure 3-11. Programming Successful



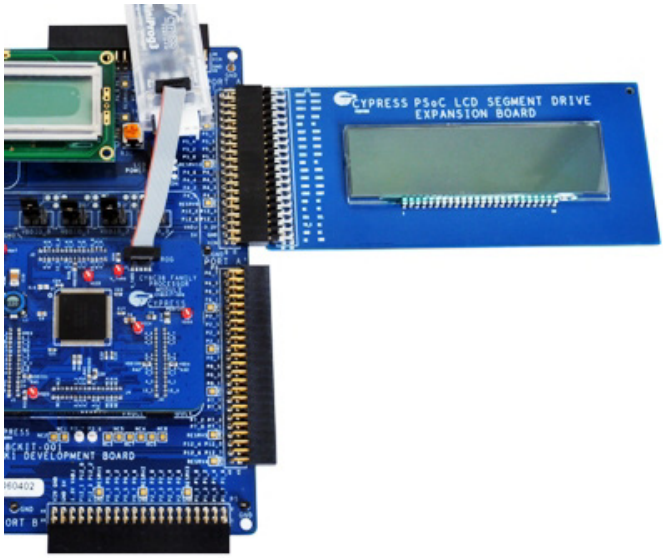
3.3 Hardware Connection

3.3.1 Hardware Connection for CY8CKIT-001 DVK

Note: The Hardware Connection on page 18 and Verify the Output on page 20 describe the Example1_Battery_Metercode example. Please refer Code Example 2: LCD_Seg_Example2_StopWatch on page 37 for details on Example2_StopWatch code example.

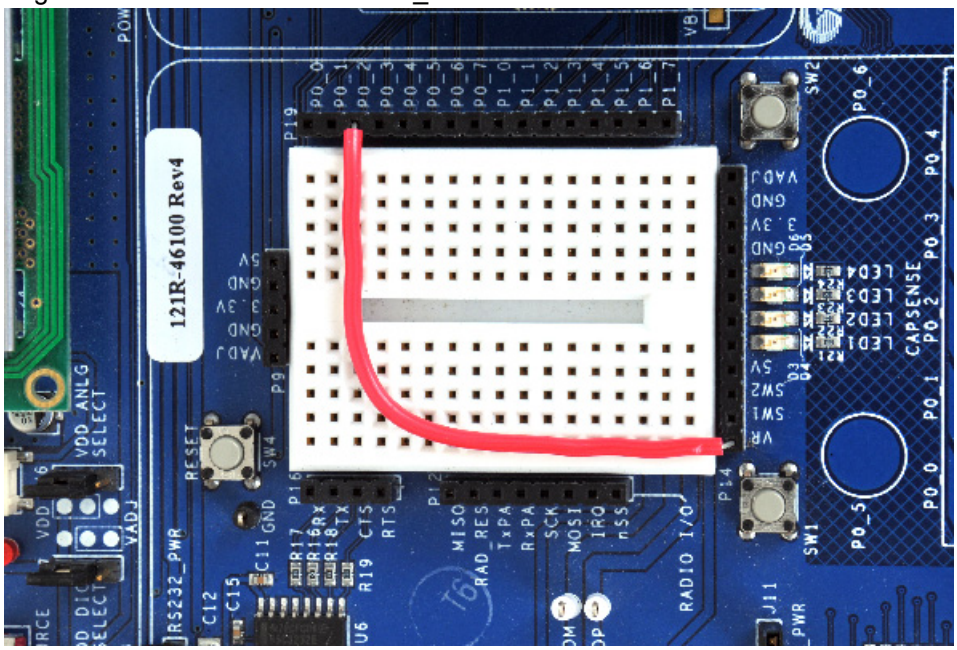
Configure the DVK SW3 to 3.3 V. Connect the PSoC LCD segment drive board to port A of the DVK as shown in Figure 3-12.

Figure 3-12. Board Connected to Port A



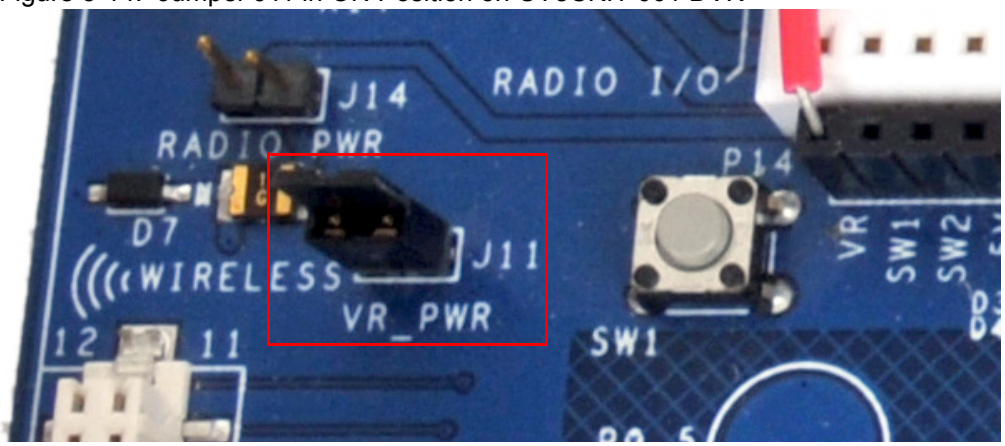
Connect the analog input from the potentiometer (VR slot in CY8CKIT-001 DVK) to P0_2 on the DVK as shown in Figure 3-13.

Figure 3-13. VR Connected to P0_2 on CY8CKIT-001 DVK



Power the VR by setting jumper J11 to the ‘ON’ position.

Figure 3-14. Jumper J11 in ON Position on CY8CKIT-001 DVK



Note: The remaining jumper settings on the DVK have the default state. See the CY8CKIT-001_PSoC_Development_Kit_Guide in www.cypress.com/go/cy8ckit-001 for default setting of the jumpers.

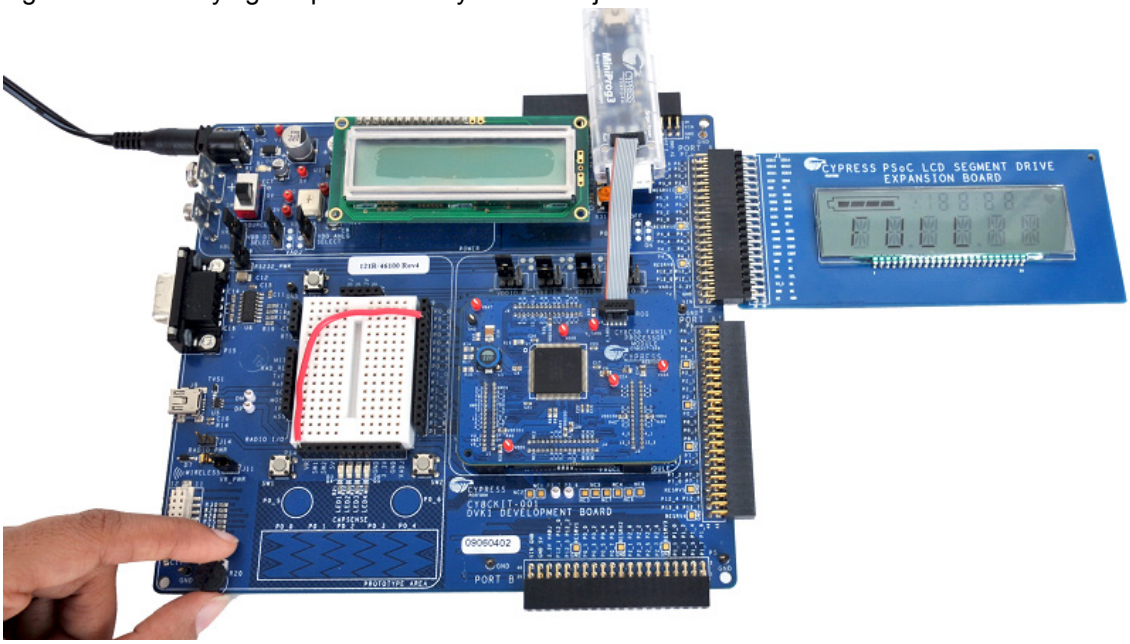
3.3.2 Hardware Connections for PSoC 3/PSoC 5LP Development Kit

1. Remove the USB cable for J1 connector (it was connected for programming the board) on board.
2. Connect the PSoC LCD segment drive board to port D of the CY8CKIT-030/ CY8CKIT-050LP DVK.
3. Remove the Character LCD (if connected) from LCD connector as the Port 2 pins are shared on the LCD connector and Port D.
4. Ensure that the J30 is shorted allowing power to the potentiometer.
5. Ensure that VDD SEL jumpers J10 and J11 are set to 3.3 V position.
6. CY8CKIT-030 and CY8CKIT-050LP do not require any other hardware connections as the potentiometer is hardwired to P6[5] of PSoC.
7. Power the board by connecting a USB cable on USB communications connector J2 or by connecting a 12 V power supply at U1 or by connecting a 12 V battery at the battery connector.

3.4 Verify the Output

Vary the VR (potentiometer) and note the change in status displayed on the LCD.

Figure 3-15. Verifying Output of Battery Meter Project



Note The best viewing angle is from 6 o'clock, according to the LCD glass characteristics.

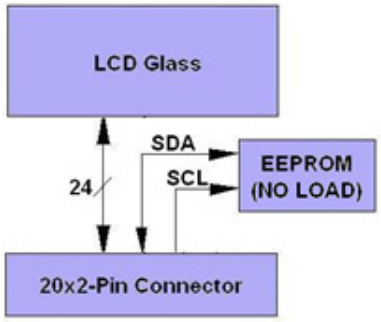
4. Hardware

4.1 System Block Diagram

The PSoC LCD Segment Drive EBK consists of only three blocks.

- LCD glass (Golden View Display LCD, GV13956A-TPP)
- I2C EEPROM (ST, M24C02-W)
- 40-pin (20x2) connector (Sullins Connector Solutions, S2111E-20-ND)

Figure 4-1. System Block Diagram



This board includes a custom LCD glass with maximum 128 segments. The glass has 24 pins (8 common and 16 segments lines) that are routed to the 20 × 2 pin connector and connected to the configured I/O pins of PSoC.

I2C EEPROM is a 'No Load' component on the board. It is used to store information about the EBK board number, so PSoC can recognize the board. ST M24C02-W is the 2-Kbit EEPROM with operating voltage in the range 2.5 V to 5.5 V.

40-pin (20 × 2) connector helps to connect the configured PSoC I/O pins to the LCD glass pins. From the 40 pins available, only 24 are used by the kit. All unused pins are left floating.

4.2 Functional Description

4.2.1 LCD Glass Details

Figure 4-2 shows the image of the LCD glass and Table 4-1 lists the segment details. The LCD glass provides visual feedback.

Figure 4-2. LCD Glass

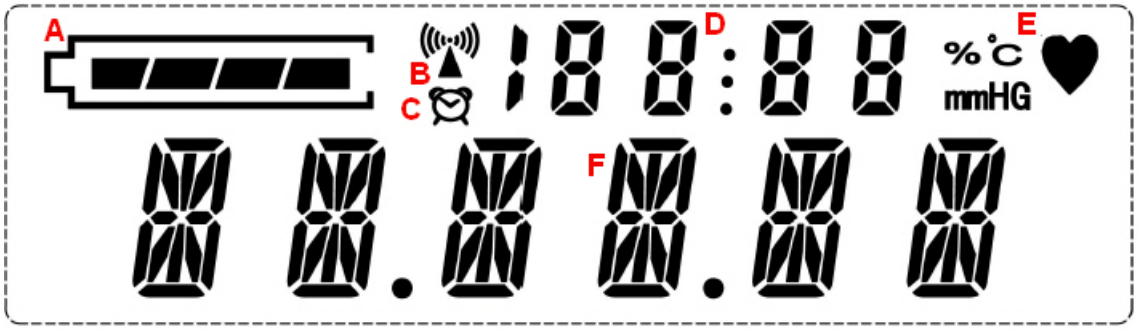


Table 4-1. LCD Glass Segment Details

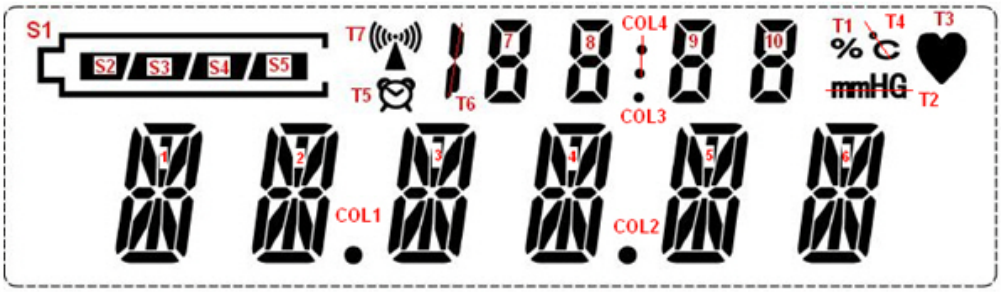
Label	Description
A	Battery charge indicator bars
B	Wireless symbol
C	Alarm display
D	7-segment numeric section
E	Medical symbol
F	14-segment alpha numeric section

4.2.1.1 Pixel Mapping Table

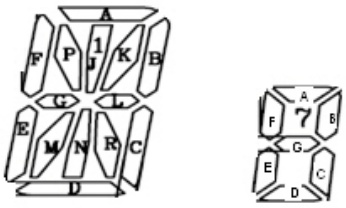
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
COM7	T7	S1	S2	COL1	S3	S4	S5	COL2	T1	T4	T2	T3	COL3	COL4	T5	T6
COM6	1A	1J	2A	2J	3A	3J	4A	4J	5A	5J	6A	6J	10D	9D	8D	7D
COM5	1P	1K	2P	2K	3P	3K	4P	4K	5P	5K	6P	6K	10C	9C	8C	7C
COM4	1F	1B	2F	2B	3F	3B	4F	4B	5F	5B	6F	6B	10E	9E	8E	7E
COM3	1G	1L	2G	2L	3G	3L	4G	4L	5G	5L	6G	6L	10G	9G	8G	7G
COM2	1E	1C	2E	2C	3E	3C	4E	4C	5E	5C	6E	6C	10B	9B	8B	7B
COM1	1M	1R	2M	2R	3M	3R	4M	4R	5M	5R	6M	6R	10F	9F	8F	7F
COM0	1N	1D	2N	2D	3N	3D	4N	4D	5N	5D	6N	6D	10A	9A	8A	7A

The following figure shows the segment lettering information for all LCD segments.

Figure 4-3. Segment Lettering Information



14-Segment and 7–Segment Lettering Information:



Note Pixel mapping table is also available on the back of the CY8CKIT-029 PSoC LCD Segment Drive EBK.

4.2.1.2 *Glass Specification*

- Display type: TN
- Viewing direction: 6 o'clock
- Drive method:1/8 Duty, 1/4 BIAS
- Operating voltage: 3.0 V
- Polarizer mode: Reflective/Positive
- Operating temperature: 0 °C ~ +50 °C.
- Storage temperature: –10 °C ~ +60 °C.

4.3 Port Options with CY8CKIT-001 DVK

The LCD segment drive board connects to the CY8CKIT-001 DVK through the 20 × 2 pin connector. It connects through one of the following ports: port A, port A prime (Port A'), or port B. Table 4-2 shows the pin assignment for all three ports along with the segment LCD pins (common and segments lines) assignment. Figure 3-12 shows the LCD segment board connection to port A of the DVK.

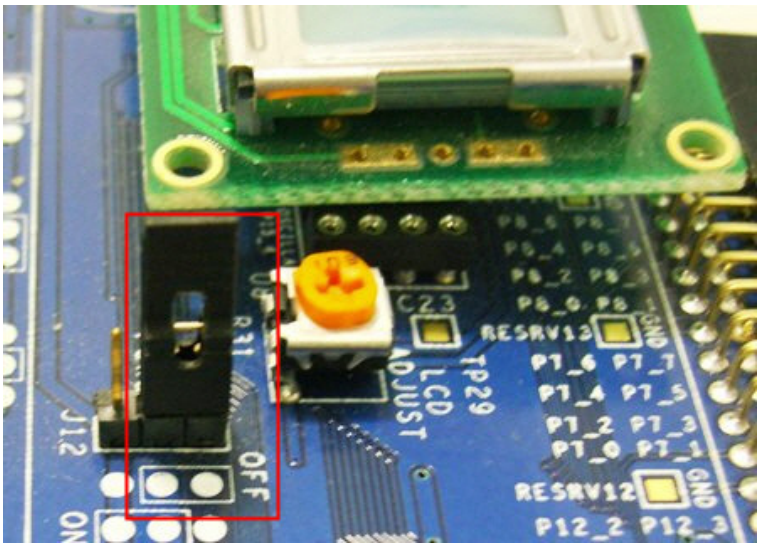
Table 4-2. Port Pin Connections

Pin	Port A	Port A'	Port B	PSoC EBK
1	P3_7	P6_7	P1_7	SEG15
2	P3_6	P6_6	P1_6	SEG14
3	P3_5	P6_5	P1_5	SEG13
4	P3_4	P6_4	P1_4	SEG12
5	P3_3	P6_3	P1_3	SEG11
6	P3_2	P6_2	P1_2	SEG10
7	P3_1	P6_1	P1_1	SEG9
8	P3_0	P6_0	P1_0	SEG8
9	GND	GND	GND	GND
10	RESRV 11	RESRV 8	RESRV 3	NC
11	P5_7	P2_7	P2_7	SEG7
12	P5_6	P2_6	P2_6	SEG6
13	P5_5	P2_5	P2_5	SEG5
14	P5_4	P2_4	P2_4	SEG4
15	P5_3	P2_3	P2_3	SEG3
16	P5_2	P2_2	P2_2	SEG2
17	P5_1	P2_1	P2_1	SEG1
18	P5_0	P2_0	P2_0	SEG0
19	GND	GND	GND	GND
20	RESRV 10	RESRV 7	RESRV 2	NC
21	P4_7	P0_7	P0_7	COM0
22	P4_6	P0_6	P0_6	COM1
23	P4_5	P0_5	P0_5	COM2
24	P4_4	P0_4	P0_4	COM3
25	P4_3	P0_3	P0_3	COM4
26	P4_2	P0_2	P0_2	COM5
27	P4_1	P0_1	P0_1	COM6
28	P4_0	P0_0	P0_0	COM7
29	GND	GND	GND	GND
30	RESRV 9	RESRV 6	RESRV 1	NC
31	P12_3	P7_7	P12_3	NC
32	P12_2	P7_6	P12_2	NC
33	P12_1	P7_5	P12_1	SDA
34	P12_0	P7_4	P12_0	SCL
35	V3_3	P7_3	V3_3	V3_3
36	VADJ	P7_2	VADJ	NC
37	GND	P7_1	GND	GND
38	V5_0	P7_0	V5_0	NC
39	VIN	GND	VIN	NC
40	GND	RESRV 5	GND	GND

Jumper Settings of CY8CKIT-001 DVK to Use Port A' and Port B:

Both port A' and port B uses the port 2 pins for segment lines. Switch the jumper J12 to the 'OFF' position; this switches off power to the character LCD, which is connected to port 2 of the CY8CKIT-001 DVK.

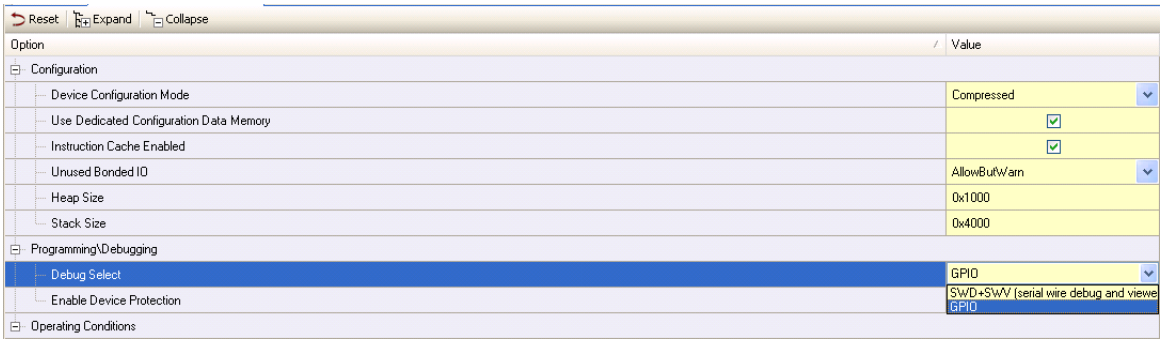
Figure 4-4. J12 Jumper in OFF Position



PSoC provides serial wire debugging (SWD) with SWD on GPIO pins option. The port pins used for SWD are P1_0 (SWDIO) and P1_1 (SWDCK). Port B uses the P1_0 and P1_1 for Seg9 and Seg8 signals, respectively. Therefore, by default, these 2 pins are not available for pin assignment in the 'Pins' tab of DWR file. To enable these 2 pins for GPIO purposes, follow these steps:

1. Open the design wide resource file (with extension '.cydwr').
2. Click the **System** tab.
3. In the Programming\Debugging section, select GPIO in the Debug Select option. Setting to GPIO frees the pins for use as GPIOs but does not completely disable the debug interface for flash protection purposes.

Figure 4-5. Enabling P1[0] and P1[1] as GPIO



4.4 Port Options with CY8CKIT-030/CY8CKIT-050LP DVK

The code examples provided with the kit uses Port D of CY8CKIT-030 and CY8CKIT-050LP. The code examples can be converted to use Port E of the kit by changing the pin connection in the DWR file of the project. The pin assignment table for Port D and Port E of DVK is as follows:

Table 4-3. Pin Assignment Table

Pin	Port D	Port E	PSoC LCD EBK
1	P1_7	P3_7	SEG15
2	P1_6	P3_6	SEG14
3	P1_5	P3_5	SEG13
4	P1_4	P3_4	SEG12
5	P1_3	P3_3	SEG11
6	P1_2	P3_2	SEG10
7	P1_1	P3_1	SEG9
8	P1_0	P3_0	SEG8
9	GND	GND_A	GND
10	RSVD	RSVD	NC
11	P2_7	P0_7	SEG7
12	P2_6	P0_6	SEG6
13	P2_5	P0_5	SEG5
14	P2_4	P0_4	SEG4
15	P2_3	P0_3	SEG3
16	P2_2	P0_2	SEG2
17	P2_1	P0_1	SEG1
18	P2_0	P0_0	SEG0
19	GND	GND_A	GND
20	RSVD	RSVD	NC
21	P5_7	P4_7	COM0
22	P5_6	P4_6	COM1
23	P5_5	P4_5	COM2
24	P5_4	P4_4	COM3
25	P5_3	P4_3	COM4
26	P5_2	P4_2	COM5
27	P5_1	P4_1	COM6
28	P5_0	P4_0	COM7
29	GND	GND_A	GND
30	RSVD	RSVD	NC
31	P12_3	P12_3	NC
32	P12_2	P12_2	NC
33	P12_1	P12_1	SDA
34	P12_0	P12_0	SCL
35	3.3 V	3.3 V	V3_3
36	RSVD	RSVD	NC

Table 4-3. Pin Assignment Table *(continued)*

Pin	Port D	Port E	PSoC LCD EBK
37	GND	GND	GND
38	5 V	5 V	NC
39	VIN	VIN	NC
40	GND	GND	GND

Port D uses Port 2 for segment lines. So, the Character LCD should be removed from LCD port while using Port D.

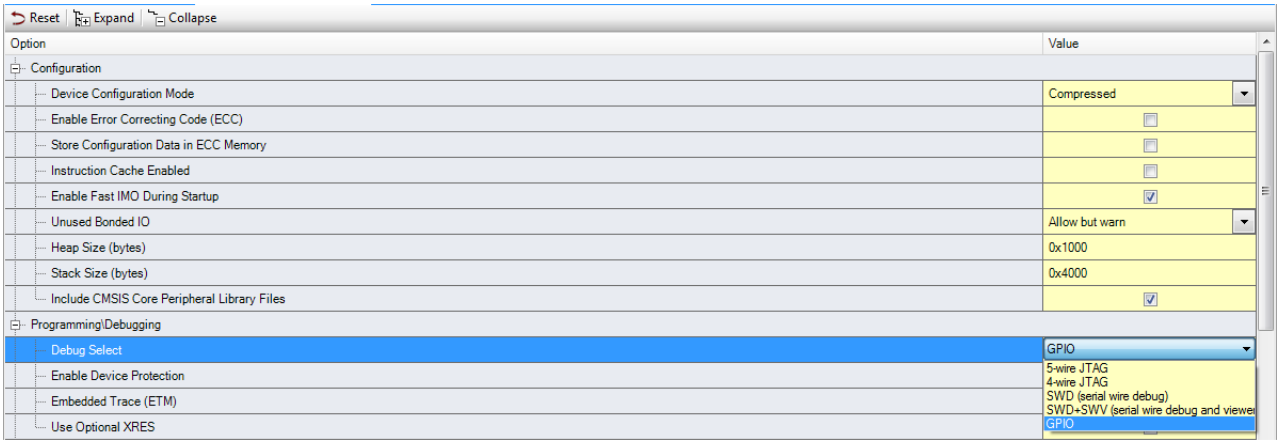
PSoC provides serial wire debugging (SWD) with SWD on GPIO pins option. The port pins used for SWD are P1_0 (SWDIO) and P1_1 (SWDCK). Port D uses the P1_0 and P1_1 for Seg9 and Seg8 signals, respectively. Therefore, by default, these 2 pins are not available for pin assignment in the 'Pins' tab of DWR file. To enable these 2 pins for GPIO purposes, follow these steps:

1. Open the design wide resource file (with extension '.cydwr').

2. Click the System tab.

3. In the Programming\Debugging section, select GPIO in the Debug Select option. Setting to GPIO frees the pins for use as GPIOs but does not completely disable the debug interface for flash protection purposes.

Figure 4-6. Enabling P1[0] and P1[1] as GPIO



4.5 Power Supply

The kit is powered from the DVK through the 40-pin (2×20) connector.

5. Code Examples

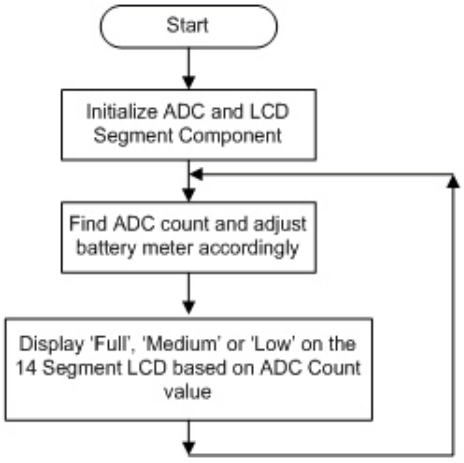
5.1 Code Example 1: LCD_Seg_Example1_Battery_Meter

This code example demonstrates the battery charge indicator along with the 14-segment display of the LCD glass by implementing a battery meter. The battery meter is used to graphically display the battery charge level; the 14-segment display is used to relay messages related to the battery charge (full, medium, and low).

5.1.1 Project Description

The potentiometer on the DVK is used to increase and decrease the battery meter on the segment LCD. The four segments in Figure 4-3 (S2, S3, S4, and S5) have four voltage levels (1.25 V, 2.50 V, 3.75 V, and 5 V) to define the switching on/off of the battery meter. This is accomplished using count values from the Delta-Sigma ADC available on PSoC 3. Based on the battery meter, 'Full', 'Medium', and 'Low' are displayed on the 14-segment LCD display.

Figure 5-1. Battery Meter Firmware Flowchart



5.1.2 Running the Code Example

Follow the steps described in Programming a PSoC 3/PSoC 5LP Device (processor module) on a CY8CKIT-001 DVK on page 13 to program the PSoC 3 device with the Battery Meter code example.

Follow the steps described in Programming a PSoC 3/PSoC 5LP Development Kit on page 16 to program the PSoC 3/PSoC 5LP DVK with the Battery Meter code example.

5.1.3 Hardware Connections

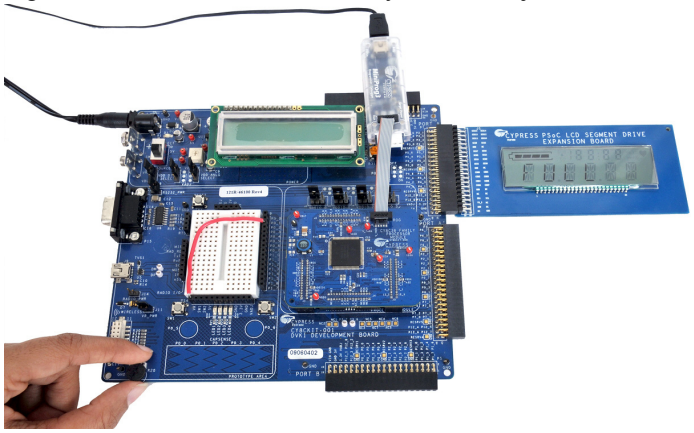
See Hardware Connection for CY8CKIT-001 DVK on page 18 for details on hardware connections on CY8CKIT-001 DVK.

See Hardware Connections for PSoC 3/PSoC 5LP Development Kit on page 19 for details on hardware connections on CY8CKIT-030/CY8CKIT-050LP.

5.1.4 Verifying Output

Vary the VR (potentiometer) and note the status changes displayed on the LCD.

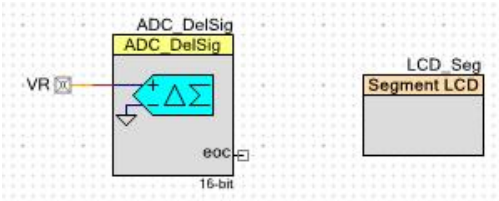
Figure 5-2. Verification of Battery Meter Project



5.1.5 PSoC Creator Project Details

PSoC Creator offers a flexible software tool to create and configure the programmable peripherals.

Figure 5-3. PSoC Creator Top Level Design For Battery Meter Project



5.1.5.1 LCD_Seg

The LCD_Seg is the core component in this code example. A single segment LCD component is selected to handle all displays on the LCD glass panel. This component defines all segment assignments for the glass. The component presents a grid containing an entry for each addressable element in the glass. An element can be a pixel in the matrix characters, a segment of one of the segment displays, or a specific icon (symbol) built into the display. Each element is considered a pixel and is individually addressed at its mapped location and turned on or off using the component pixel handling API calls.

Helper functions are also available; each helper is specifically designed to allow handling of the different types of characters in the display. Thus, segments of a segment character are grouped and addressed collectively by a single helper. Each helper has a set of component API calls that are placed in the code to write digits or characters to the target display areas.

Each icon is turned on or off using a write pixel API call. The matrix display characters are set using a write string API call. The segment displays are written one character at a time using a write character or write digit API call.

In the basic configuration, the bias voltage is selected to set the contrast level. The contrast level can also be adjusted dynamically, by using the API call provided by the segment LCD component. The higher the bias level set in the call to the API, the higher the contrast. The API allows a selection

between 0 and 127 with 127 corresponding to the maximum contrast level. The frame rate is selected to be the maximum rate before the characters in the display begin to reduce in contrast.

The segment LCD component in this code example is used to control the switching on/off of the segments of battery charge indicator (S1, S2, S3, S4, and S5) and also the 14-segment display message. The component provides all analog and digital signals necessary to drive 128 segments liquid crystal display using eight common lines and sixteen segment drive lines.

Figure 5-4. Segment LCD Configuration: Basic Tab

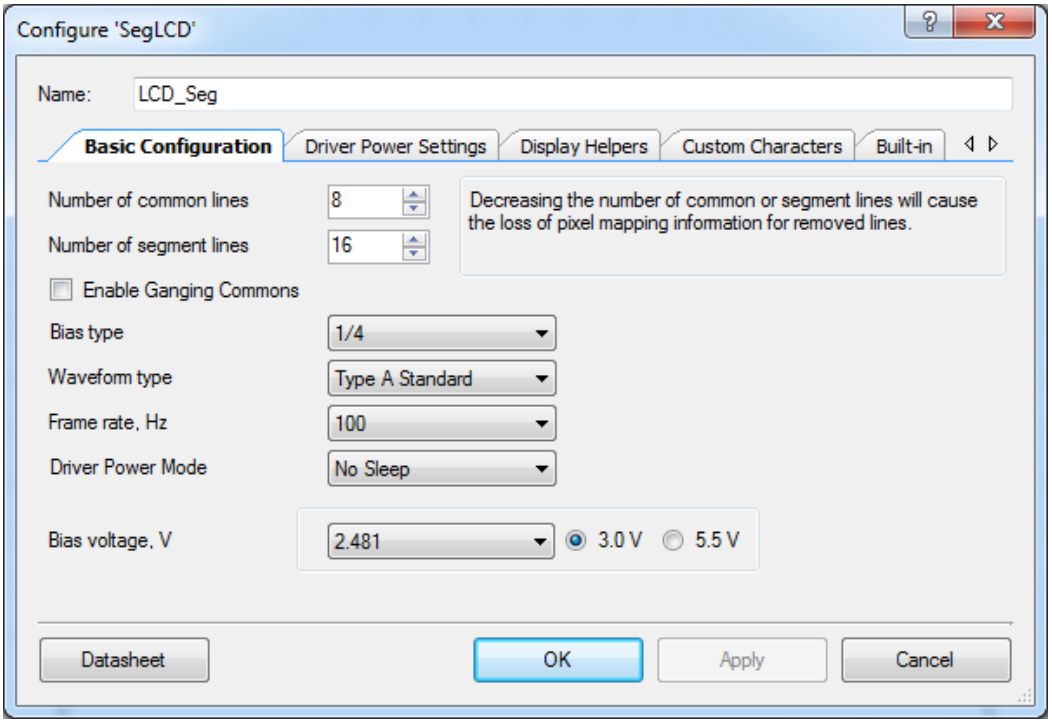


Figure 5-5. Segment LCD Configuration: Driver Power Settings

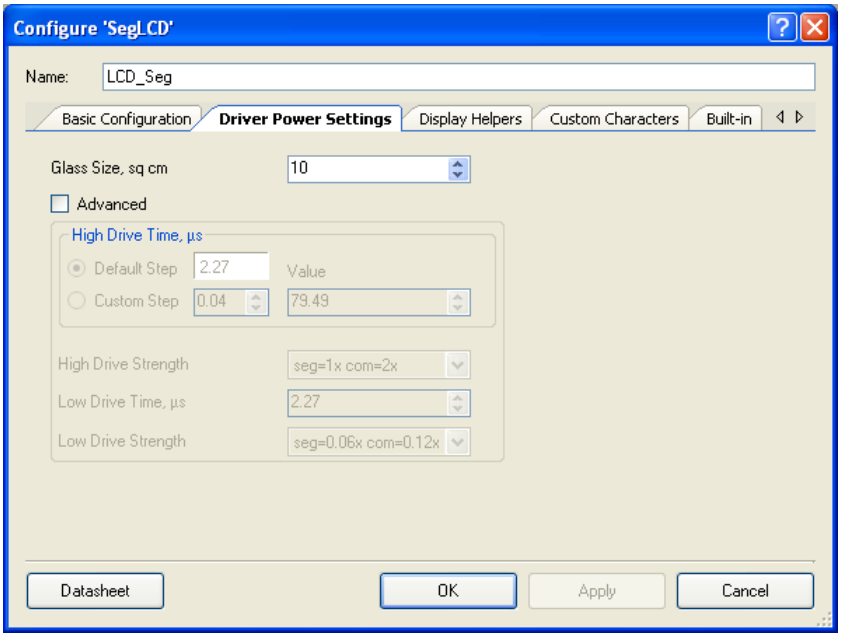
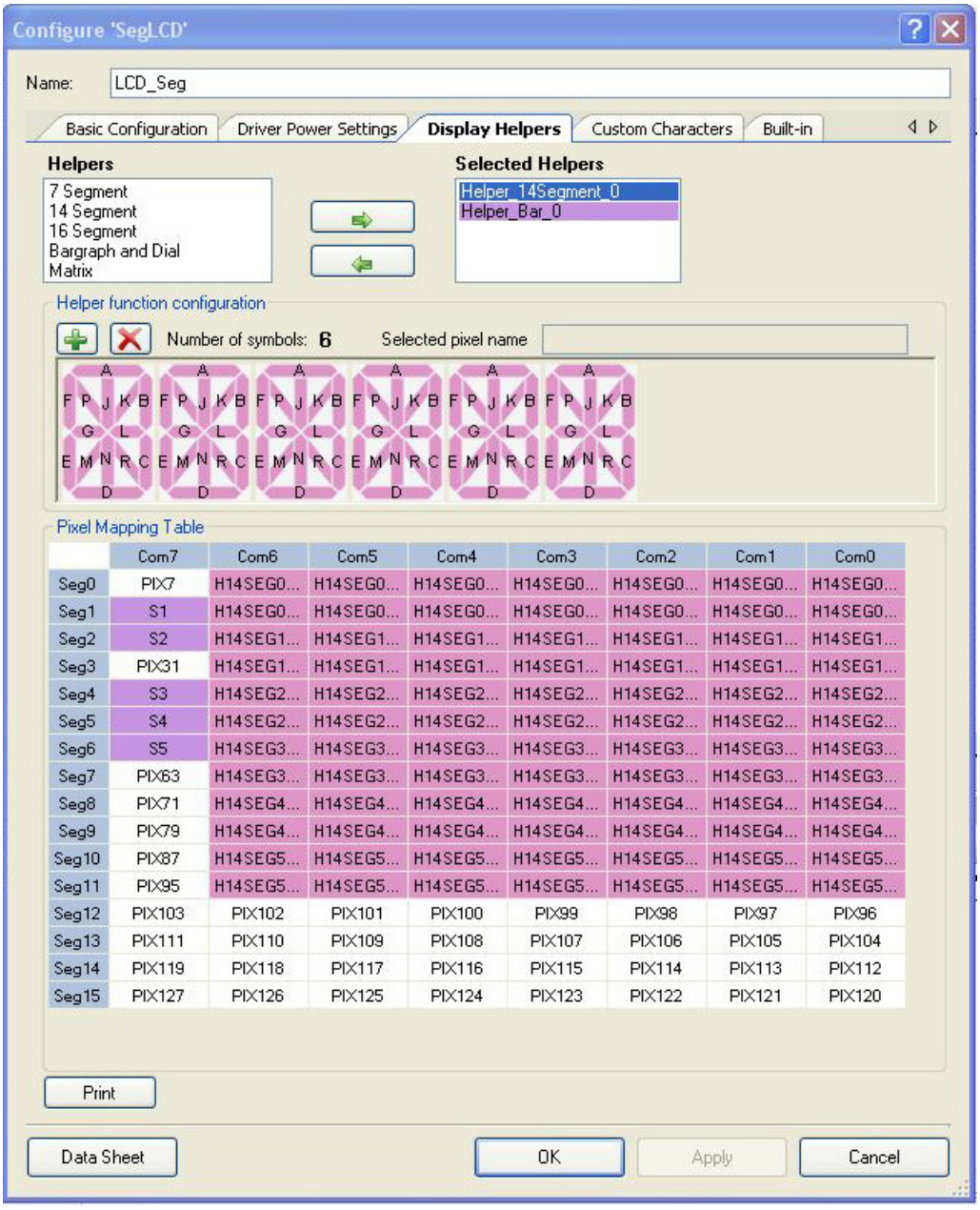
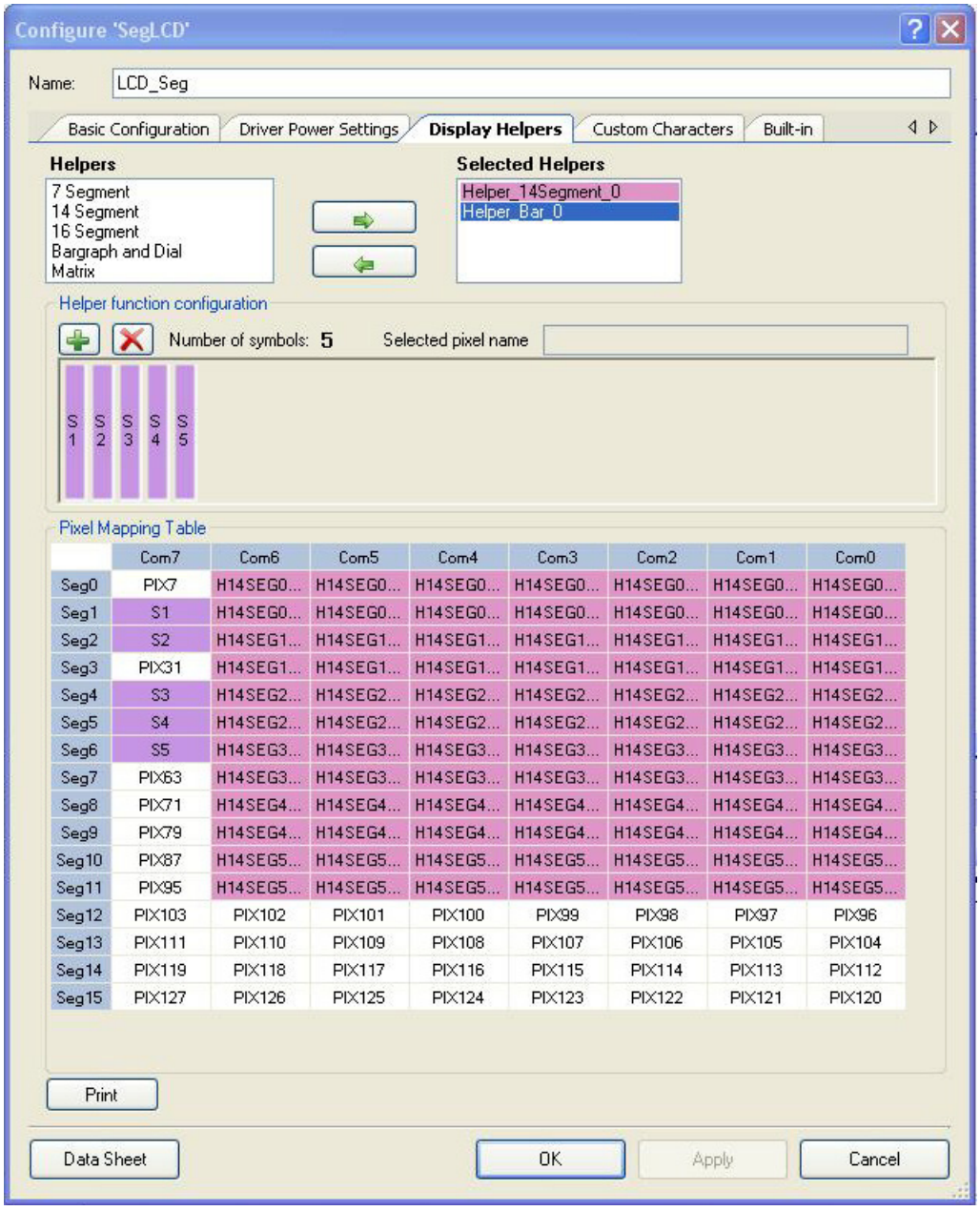


Figure 5-6. Six Character Helper for 16-Segment Display



	Com7	Com6	Com5	Com4	Com3	Com2	Com1	Com0
Seg0	PIX7	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...
Seg1	S1	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...	H14SEG0...
Seg2	S2	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...
Seg3	PIX31	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...	H14SEG1...
Seg4	S3	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...
Seg5	S4	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...	H14SEG2...
Seg6	S5	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...
Seg7	PIX63	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...	H14SEG3...
Seg8	PIX71	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...
Seg9	PIX79	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...	H14SEG4...
Seg10	PIX87	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...
Seg11	PIX95	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...	H14SEG5...
Seg12	PIX103	PIX102	PIX101	PIX100	PIX99	PIX98	PIX97	PIX96
Seg13	PIX111	PIX110	PIX109	PIX108	PIX107	PIX106	PIX105	PIX104
Seg14	PIX119	PIX118	PIX117	PIX116	PIX115	PIX114	PIX113	PIX112
Seg15	PIX127	PIX126	PIX125	PIX124	PIX123	PIX122	PIX121	PIX120

Figure 5-7. Bar Graph Helper for 5 Battery Indicator Segments



Notes

- For details of parameters see the component datasheets.
- The figure only shows the tabs within the component that need to be changed. Other tabs, such as the Built In tab, have the default setting. This is valid for all components of both code examples.

The segment naming in the LCD glass (Golden View Display LCD, GV13956A-TPP) and SegLCD component in PSoC Creator are different.

Table 5-1. Segment Naming in LCD

No.	Segment in Golden View Display LCD, GV13956A-TPP	SegLCD Component in PSoC Creator
1	A	A
2	B	B
3	C	C
4	D	D
5	E	E
6	F	F
7	G	G
8	P	H
9	J	I
10	K	J
11	L	K
12	R	L
13	N	M
14	M	N

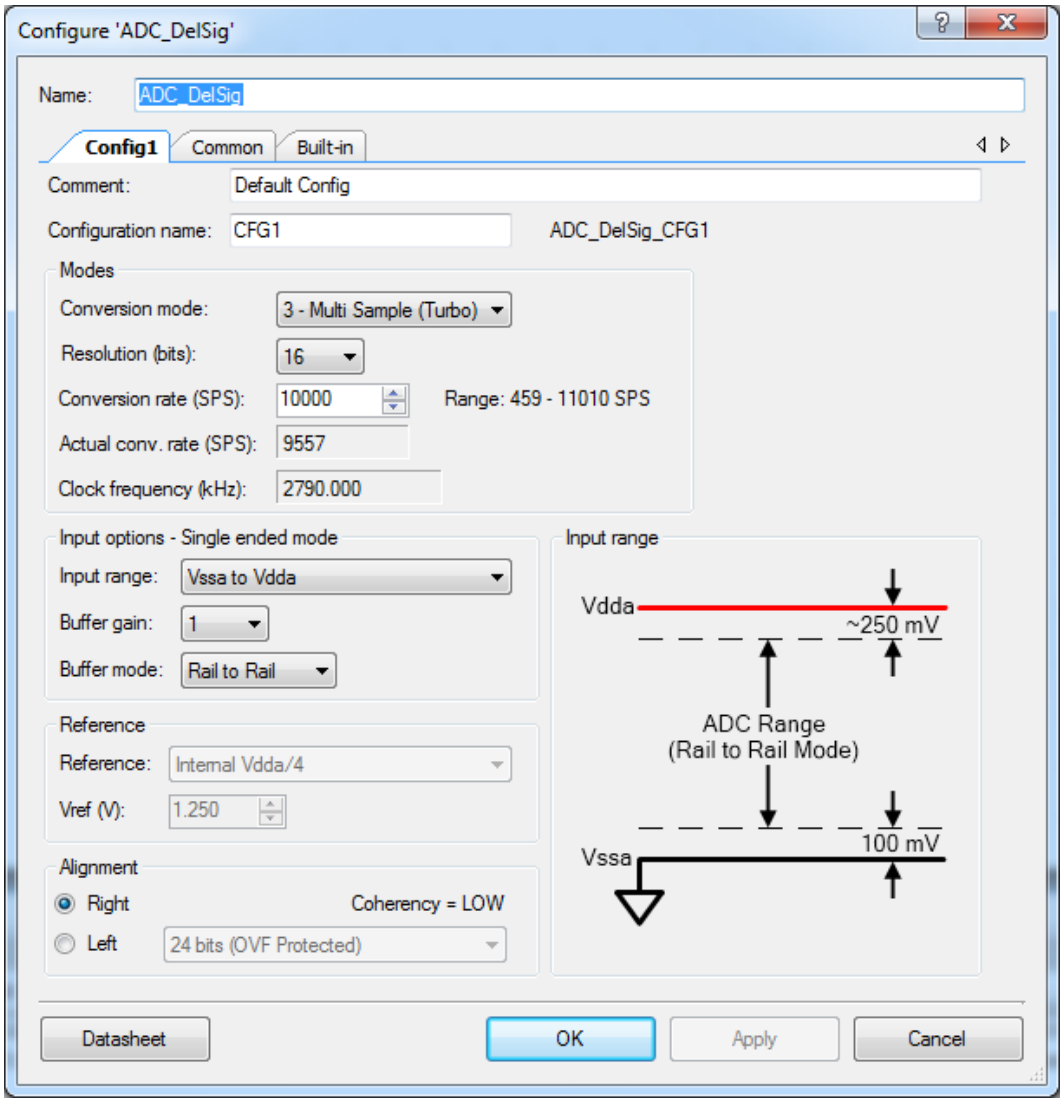
The same is depicted symbolically in Figure 5-8

Figure 5-8. Segment Naming in LCD

5.1.5.2 *ADC_DelSig*

The ADC is used to sample an input voltage, take the voltage from the potentiometer, and control the battery charge indication on the LCD segments.

Figure 5-9. ADC_DelSig Component Configuration: Configure Tab



5.1.5.3 VR

The VR pin is used to read the analog value from the potentiometer. The Pin Drive mode is configured as High-Z, which is the default value. Figure 5-10 and Figure 5-11 show the port pin setting.

Figure 5-10. VR Configuration: Type Tab

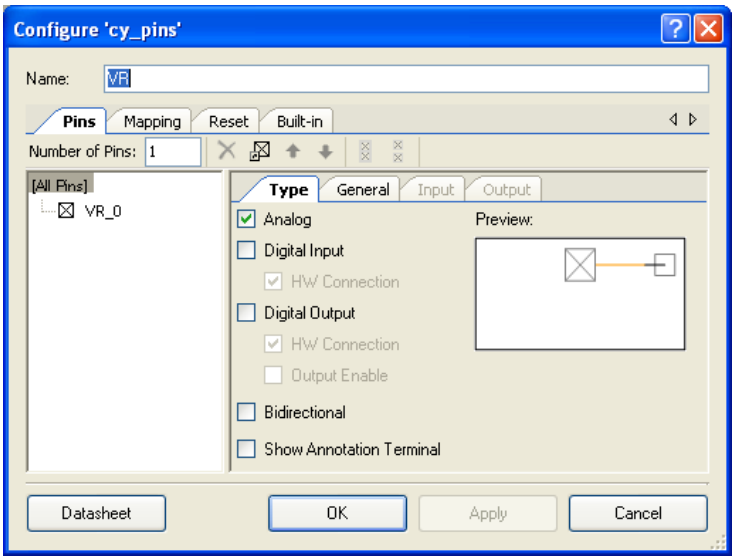
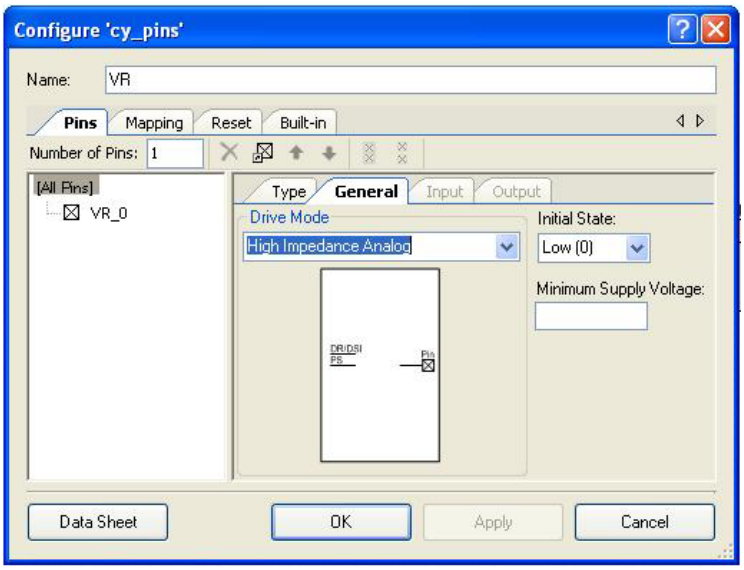


Figure 5-11. VR Configuration: General Tab

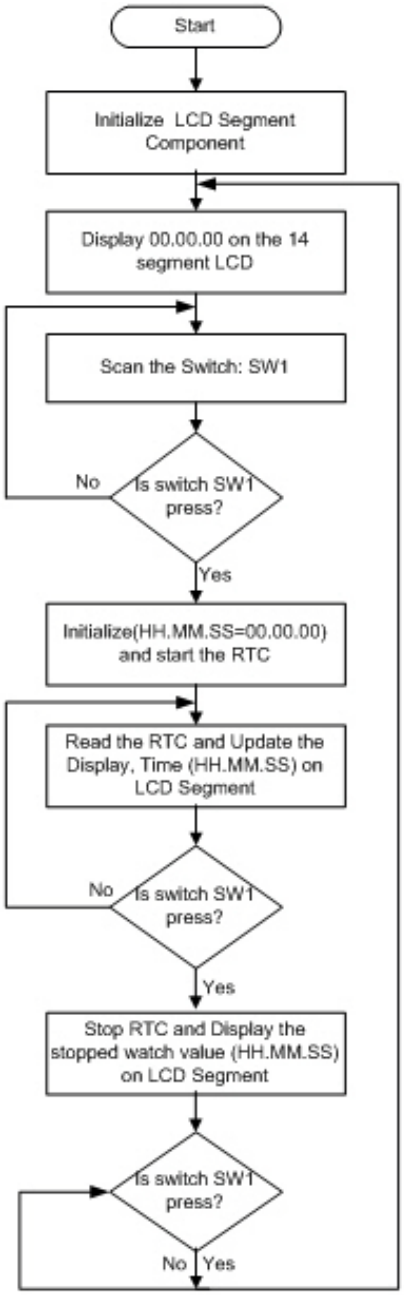


5.2 Code Example 2: LCD_Seg_Example2_StopWatch

5.2.1 Project Description

This code example implements a stopwatch using the RTC component in PSoC Creator. The values hours, minutes, and seconds (HH:MM:SS) are displayed on the 14-segment display of the LCD.

Figure 5-12. StopWatch Project Flowchart



5.2.2 Running the Code Example

To program the PSoC 3/PSoC 5LP device with the stopwatch code example,

1. Follow steps 1 to 3 in Programming a PSoC 3/PSoC 5LP Device (processor module) on a CY8CKIT-001 DVK on page 13.
2. Click the code example, LCD_Seg_Example2_StopWatch_009A for PSoC 3 processor module and LCD_Seg_Example2_StopWatch_010 for PSoC 5LP processor module, from **Examples and Kits** in the **Start Page** of PSoC Creator.
3. Follow the steps 5 to 10 in Programming a PSoC 3/PSoC 5LP Device (processor module) on a CY8CKIT-001 DVK on page 13 to complete programming.

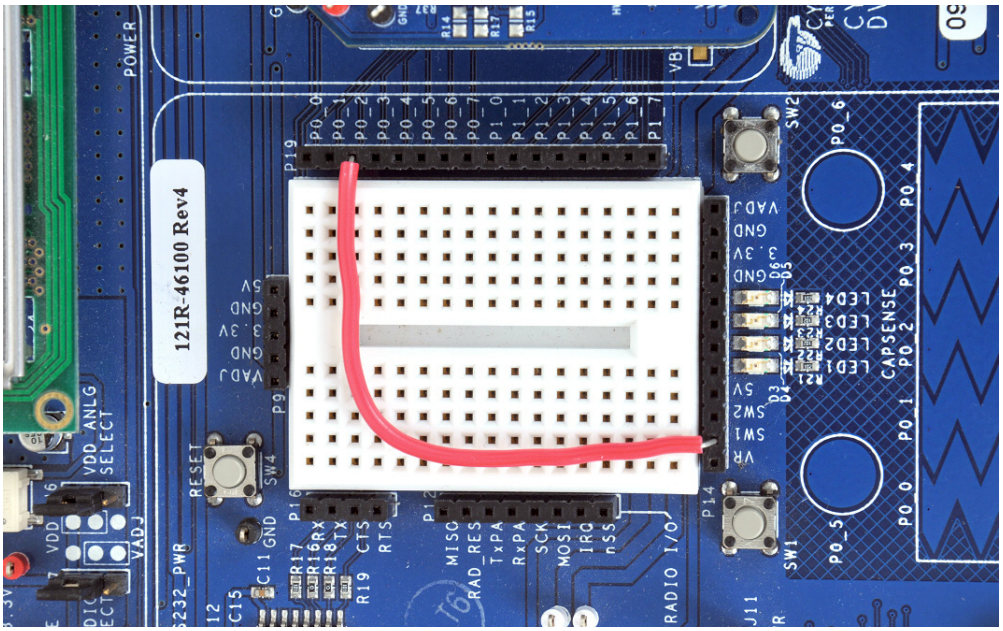
To program the PSoC 3/PSoC 5LP DVK with the stopwatch code example,

1. Follow steps 1 to 3 in Programming a PSoC 3/PSoC 5LP DVK.
2. Click the code example, LCD_Seg_Example2_StopWatch_030 for CY8CKIT-030 and LCD_Seg_Example2_StopWatch_050 for CY8CKIT-050LP, from Examples and Kits in the Start Page of PSoC Creator.
3. Follow the steps 5 to 10 in Programming a PSoC 3/PSoC 5LP Development Kit on page 16 to complete programming.

5.2.3 Hardware Connections for CY8CKIT-001 DVK

1. Connect the LCD segment drive board to port A of the DVK, as shown in Figure 3-12.
2. Connect the input from the mechanical switch SW1 of the DVK to port pin P0_2 on the DVK, as shown in Figure 5-13.

Figure 5-13. Connect Switch SW1 to P0_2 on CY8CKIT-001 DVK



Note The remaining jumper settings on the DVK have the default state. See the *CY8CKIT-001_PSoC_Development_Kit_Guide in www.cypress.com/go/cy8ckit-001* for default setting of the jumpers.

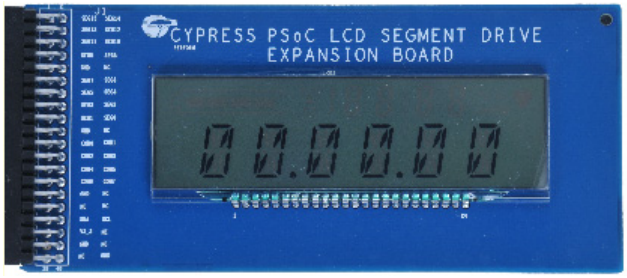
5.2.4 Hardware Connections for CY8CKIT-030/CY8CKIT-050LP DVK

1. Connect the LCD segment drive board to port D of the DVK.
2. Ensure that Character LCD is removed from LCD port as the Port 2 pins are used for Segment lines on Port D
3. After programming the DVK, power the board by connecting the USB cable on USB communications connector J2 or by connecting an external power supply or by 12 V battery.
4. CY8CKIT-030 and CY8CKIT-050LP do not require any more hardware connections as the SW2 is hard wired to P6[1] of PSoC.

5.2.5 Verifying the Output

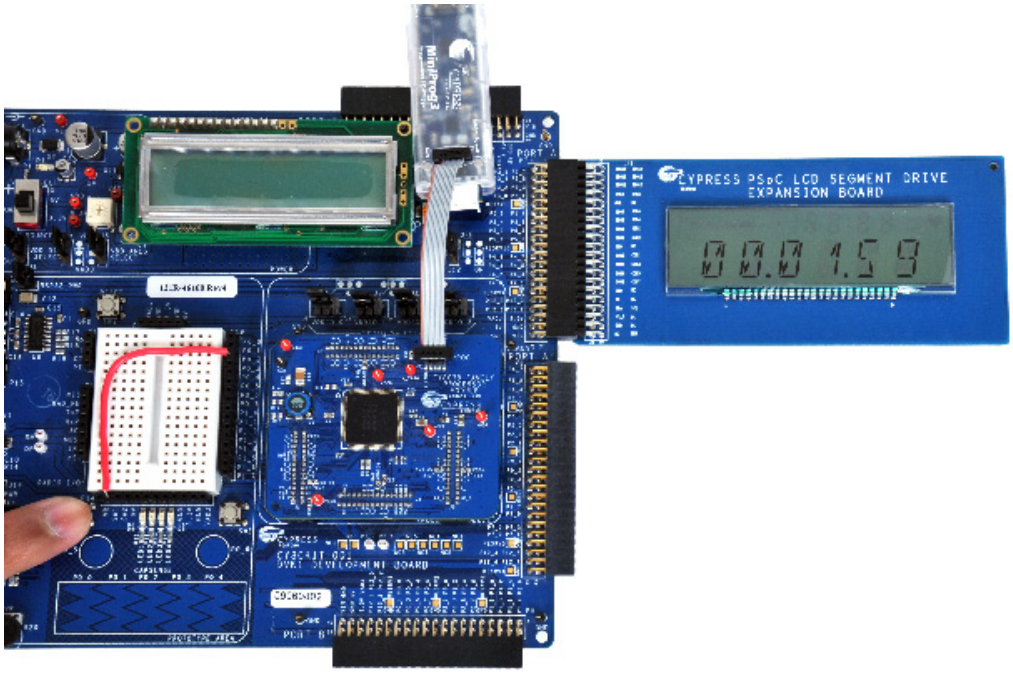
On power up, the LCD segment displays HH.MM.SS as 00.00.00 on the 14-segment display of the LCD.

Figure 5-14. LCD Display



The mechanical switch SW1 on the CY8CKIT-001 or SW2 on CY8CKIT-030/CY8CKIT-050LP is used to start, stop, and reset the stopwatch. The switch sequence is shown Figure 5-15.

Figure 5-15. Switch SW1 Starts RTC

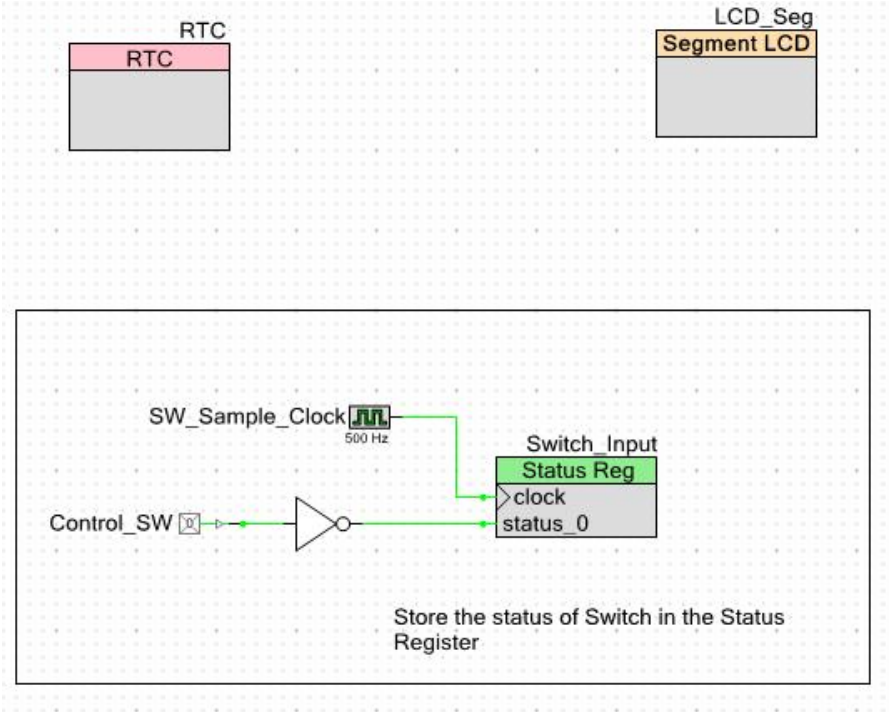


Pressing SW1 on CY8CKIT-001 or SW2 on CY8CKIT-030/CY8CKIT-050LP the first time starts the stopwatch and the values HH.MM.SS from the RTC are displayed on the LCD. The stopwatch

increments every second. The second press stops the stopwatch and the value at which the watch stopped (HH.MM.SS) is displayed on the LCD. The third press of the switch resets the display to 00.00.00 (HH.MM.SS).

5.2.6 PSoC Creator Project Details

Figure 5-16. PSoC Creator Top Level Design for StopWatch Project



5.2.6.1 LCD_Seg

The LCD_Seg is the core component used in this project. It displays the time (HH:MM:SS) on the 14-segment display section. The component provides all analog and digital signals necessary to drive 128 segments LCD using eight common lines and sixteen segment drive lines.

Figure 5-17. Segment LCD Configuration: Basic Tab

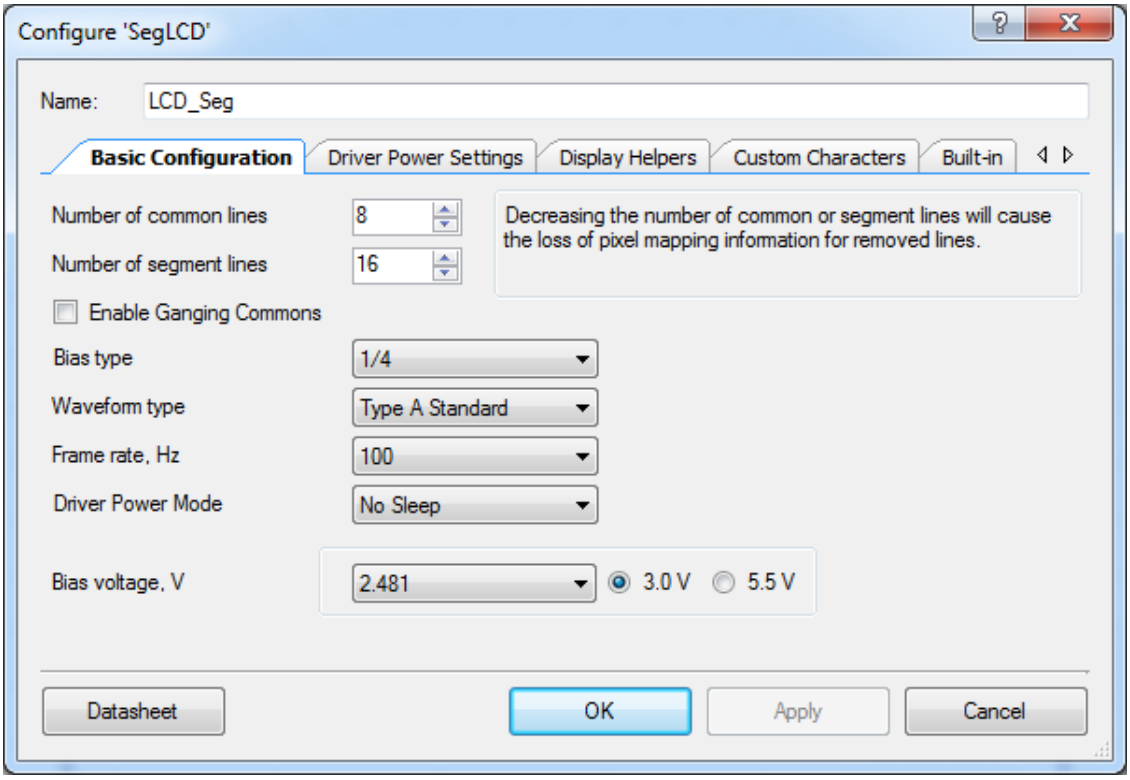


Figure 5-18. Segment LCD Configuration: Driver Power Settings

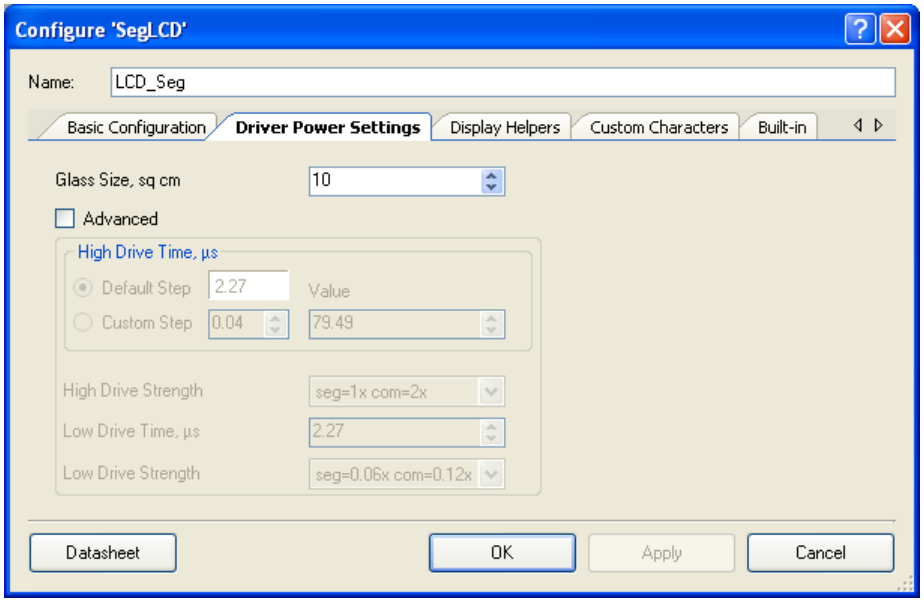
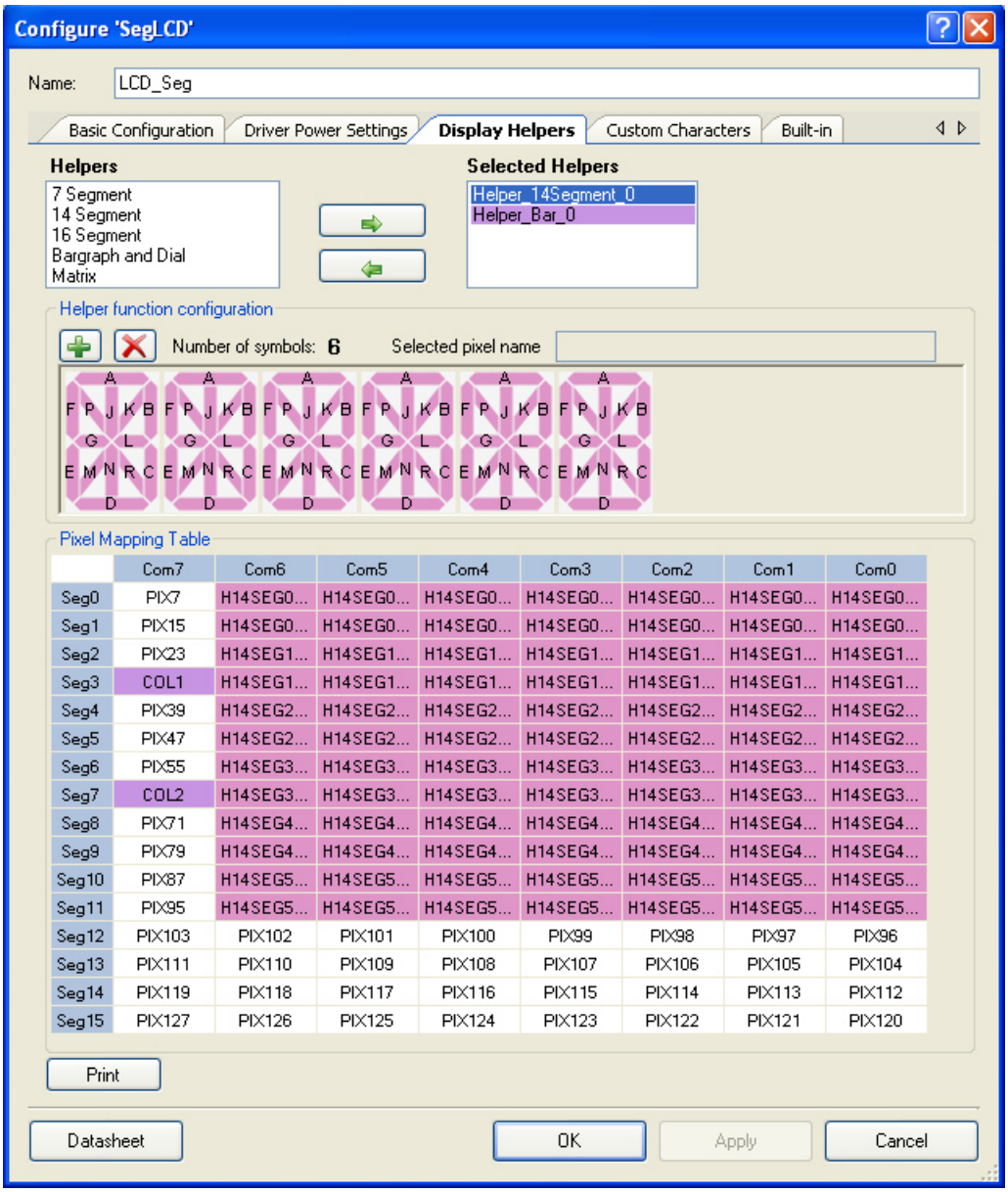


Figure 5-19. Six Character Helper for 16-Segment Display



The segment naming in the LCD glass (Golden View Display LCD, GV13956A-TPP) and SegLCD component in PSoC Creator are different.

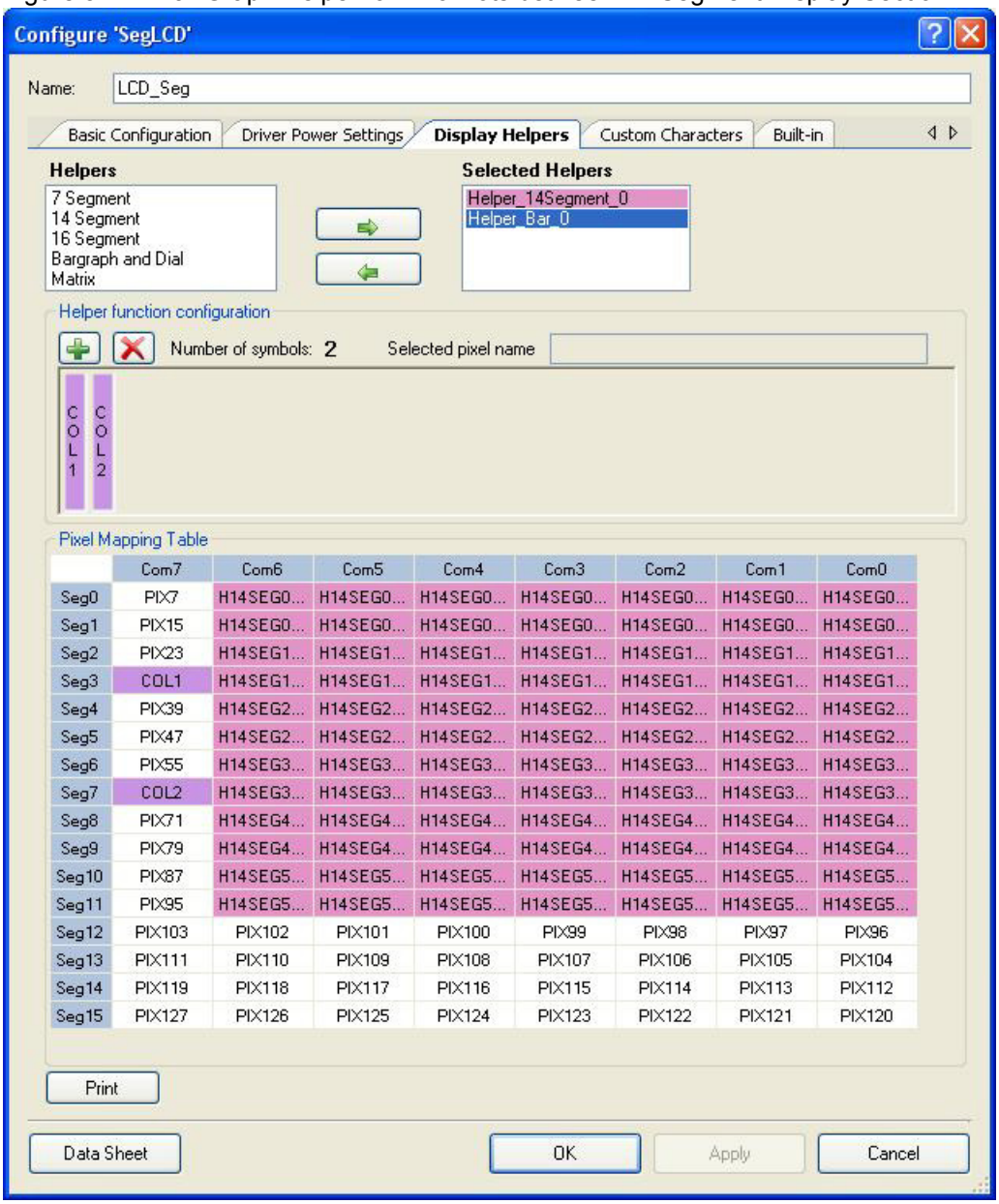
Table 5-2. Segment Naming in LCD

No.	Segment in Golden View Display LCD, GV13956A-TPP	SegLCD component in PSoC Creator
1	A	A
2	B	B
3	C	C
4	D	D
5	E	E
6	F	F
7	G	G
8	P	H
9	J	I
10	K	J
11	L	K
12	R	L
13	N	M
14	M	N

The same is depicted symbolically in Figure 5-20

Figure 5-20. Segment Naming in LCD

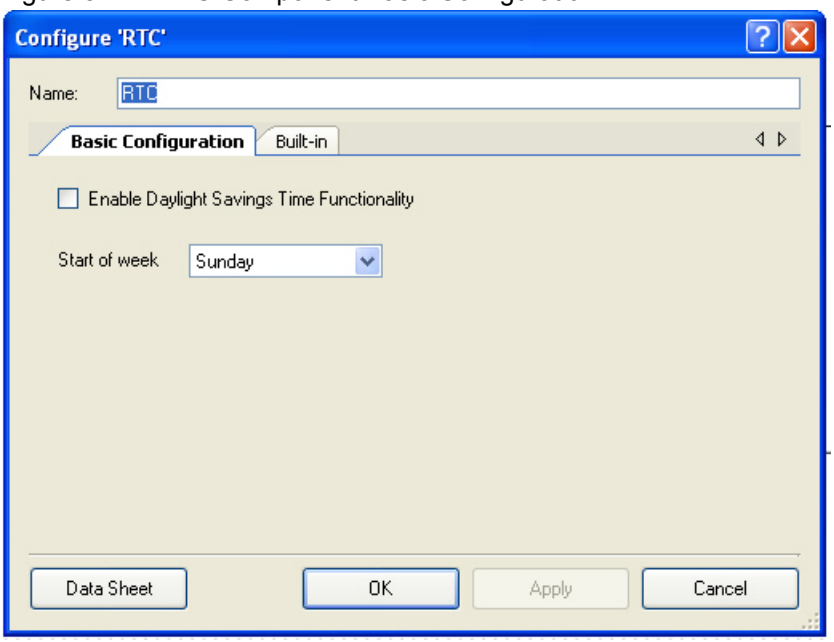
Figure 5-21. Bar Graph Helper for Two Dots between 14-Segment Display Section



5.2.6.2 *Real Time Clock (RTC)*

The RTC is minimally configured to use Sunday as the start of the week. The firmware enables the RTC with hours, minutes, and seconds set to zero. When you press SW1, the RTC starts incrementing the time every second, SS from 0 to 59, then MM to 0 to 59, and hours from 0 to 24; thereafter it resets. If you press SW1 again, the RTC stops; on the third press, the RTC is reset to initial condition of hours, minutes, and seconds set to zero.

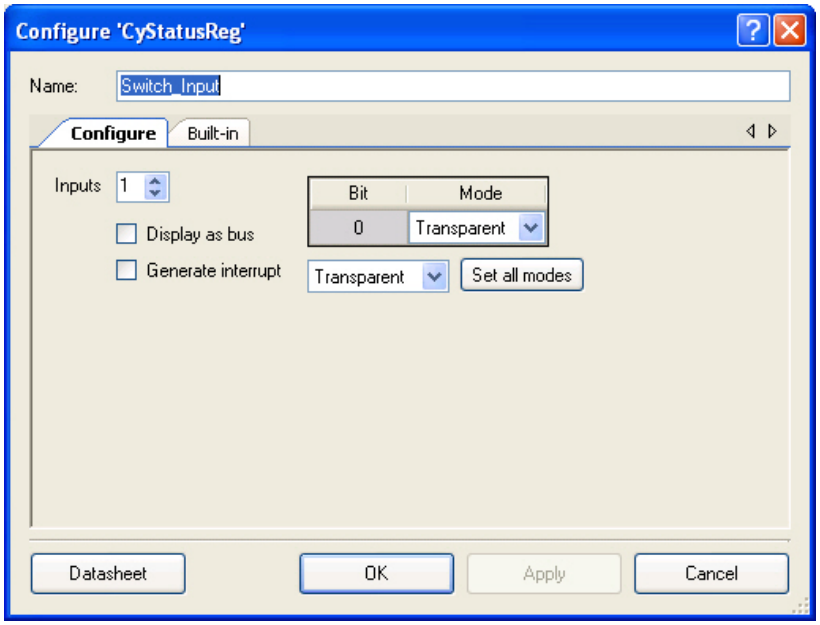
Figure 5-22. RTC Component Basic Configuration



5.2.6.3 *Status Register*

Status register is used to store the status of the switch that is read in the firmware.

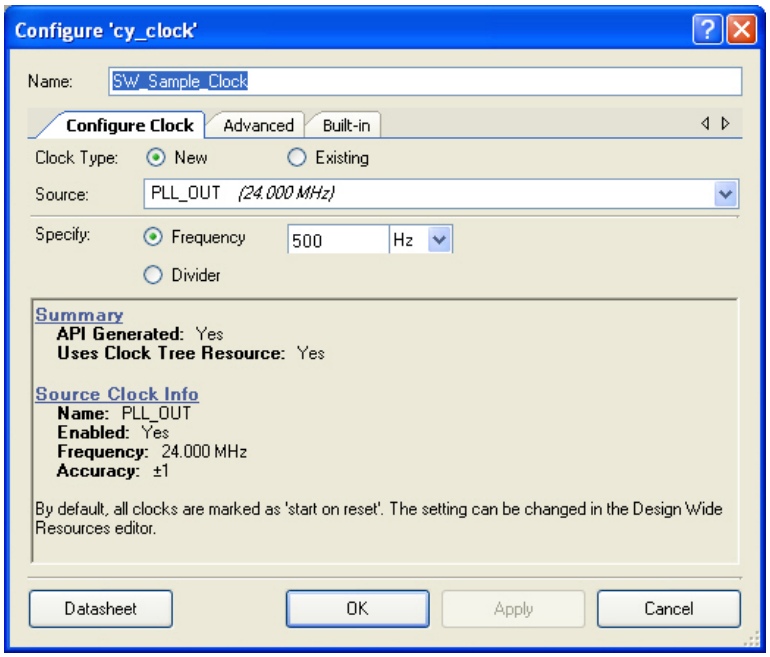
Figure 5-23. Status Register Configuration: Configure Tab



5.2.6.4 *Sw_Sample_Clock*

The clock component of PSoC Creator is used to sample the switch at the frequency of 500 Hz.

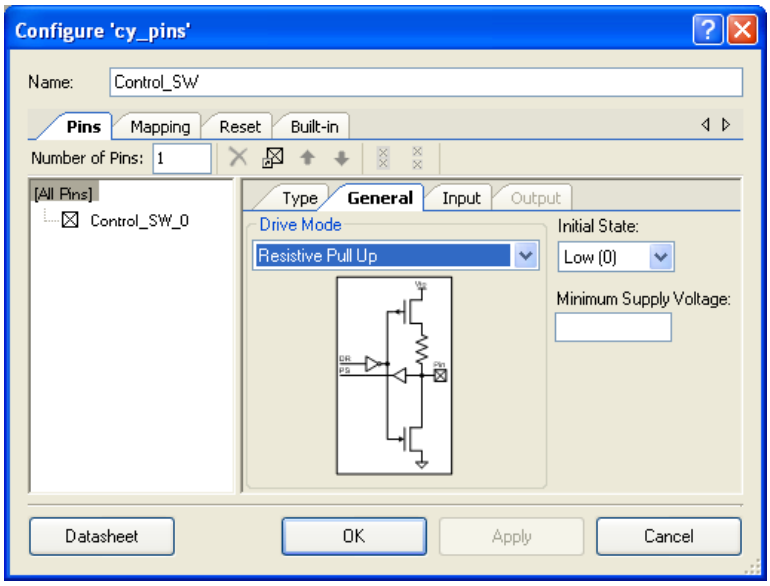
Figure 5-24. Clock Component Configuration: Configure Clock Tab



5.2.6.5 *Clock_SW*

This is a digital port component used to read the pin status. It is configured as "Input" port. The drive mode of the pin is configured to Resistive Pull Up mode because the switch input is a Active High input.

Figure 5-25. Switch Pin Configuration: General Tab

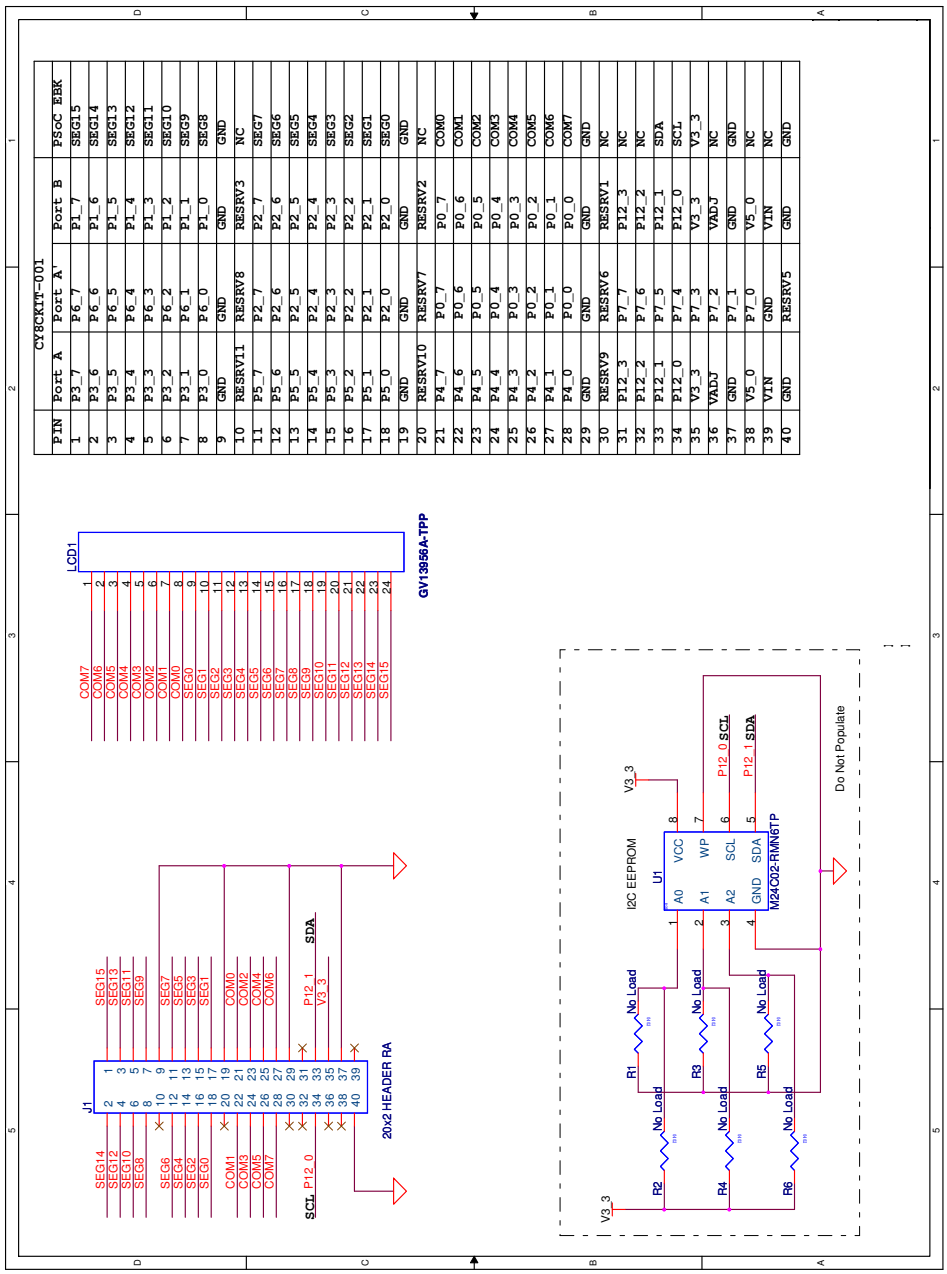


Note Pin assignment in both code examples is according to port A of the DVK. Open the code example and change the pin assignment in PSoC Creator (.cydwr file) for port A' or port B according to Table 4-2.

Note The pins for VR and SW1 must be reassigned to any other free GPIO when using port A' and port B. This is because P0_2 pin used in both code examples for VR and SW1, is used for common lines.

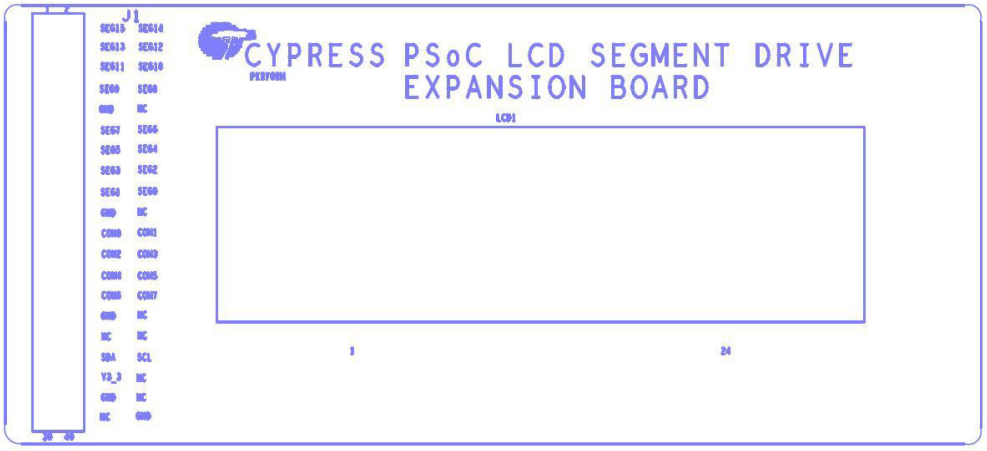
A. Appendix

A.1 Schematic

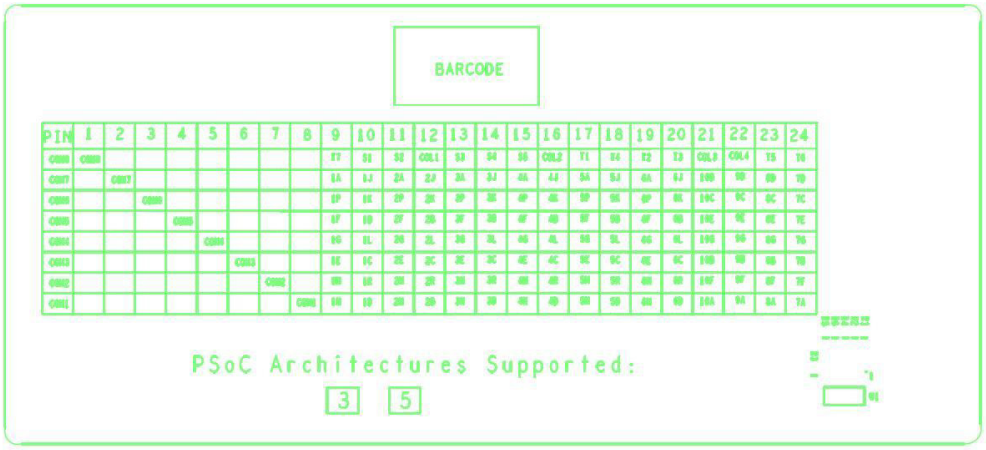


A.2 Board Layout

A.2.1 PDCR-09571 Top View



A.2.2 PDCR-09571 Bottom View



Note See the Hardware folder in the kit CD for schematic and layout PDF files.

A.3 BOM

Item	Qty.	Reference	Description	Manufacturer Name	Manufacturing Part Number
1			PCB	Cypress	PDCR-09571
2	1	LCD1	LCD Glass	Golden View Display	GV13956A-TPP
3	1	J1	CONN HEADER.100 DUAL R/A 40POS	Sullins Connector Solutions	S2111E-20-ND
No load					
4	6	R1, R2, R3, R4, R5, R6	RES 10 KΩ 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ103X
5	1	U1	IC SRL EEPROM I2C 2 KBIT SO-8	STMicroelectronics	M24C02-RMN6TP
Install at the bottom of PCB as close to the corners as possible					
6	4	N/A	BUMPER WHITE.500X.23 SQUARE	Richco Plastic Co	RBS-3R

A.4 Regulatory Compliance Information

CY8CKIT-029 has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations.

- CISPR 22 - Emissions
- EN 55022 Class A - Immunity (Europe)

Revision History

Document Revision History

Document Title: CY8CKIT-029 PSoC® LCD Segment Drive Expansion Board Kit Guide Document Number: 001-55415				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	2779772	09/02/2009	XKJ	Initial version of the guide
*A	2786580	10/13/2009	XKJ	CDT Updates
*B	2799298	11/02/2009	XKJ	Updated Schematic in Appendix
*C	2823587	12/08/2009	RKAD	Updated Figure 5-3, Figure 5-15, and Note in section 5.2.5.5 Clock_SW
*D	3236679	02/16/2011	RKAD	Updated Figures as per the latest software
*E	3281381	05/24/2011	RKAD	Fixed template styles
*F	3347294	08/17/2011	RKAD	Updated Figures 5-4, Figure 5-5, Figure 5-9, Figure 5-17, Figure 5-18.
*G	3455166	12/02/2011	RKAD	Updated kit installation location in section 2.1
*H	3596461	04/23/2012	RKAD	Updated the Additional Resources section.
*I	3704765	07/19/2012	RKAD	Added Safety Information chapter on page 5. Updated Kit Operation chapter on page 13: Updated “Programming the device” on page 13 (Updated “Programming a PSoC 3/PSoC 5LP Device (processor module) on a CY8CKIT-001 DVK” on page 13 (Updated the Note below the Figure 3-1 on page 14)). Updated “Hardware Connection” on page 18 (Updated “Hardware Connection for CY8CKIT-001 DVK” on page 18 (Updated description)). Updated Code Examples chapter on page 29: Updated “Code Example 2: LCD_Seg_Example2_StopWatch” on page 37 (Updated the Note below the Figure 5-13 on page 38, updated Figure 5-23 on page 45). Updated Appendix chapter on page 49: Added “Regulatory Compliance Information” on page 51.
*J	4178232	12/09/2013	SASH	Updated Introduction chapter on page 7: Updated description. Updated “PSoC Creator” on page 7: Updated description. Updated “Getting Started” on page 8: Updated description. Updated “Additional Learning Resources” on page 8: Updated “Beginner Resources” on page 8: Updated titles of all application notes. Updated “Engineers Looking for More” on page 8: Updated titles of all application notes. Added “More Code Examples” on page 8. Updated Installation chapter on page 11: Updated “CD Installation” on page 11: Updated Figure 2-1. Updated “Install Software” on page 12: Updated description.

Document Revision History *(continued)*

Document Title: CY8CKIT-029 PSoC® LCD Segment Drive Expansion Board Kit Guide Document Number: 001-55415				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
*J (cont.)	4178232	12/09/2013	SASH	Updated Kit Operation chapter on page 13: Updated "Introduction" on page 13: Updated description. Updated "Programming the device" on page 13: Updated "Programming a PSoC 3/PSoC 5LP Device (processor module) on a CY8CKIT-001 DVK" on page 13: Updated description. Updated Figure 3-2. Updated Figure 3-5. Updated "Programming a PSoC 3/PSoC 5LP Development Kit" on page 16: Updated description. Updated Figure 3-8. Updated Figure 3-11. Updated "Hardware Connection" on page 18: Updated "Hardware Connection for CY8CKIT-001 DVK" on page 18: Updated description. Updated Hardware chapter on page 21: Updated "System Block Diagram" on page 21: Updated description. Updated "Port Options with CY8CKIT-001 DVK" on page 23: Updated description. Updated "Port Options with CY8CKIT-030/CY8CKIT-050LP DVK" on page 26: Updated Figure 4-6. Updated Code Examples chapter on page 29: Updated "Code Example 1: LCD_Seg_Example1_Battery_Meter" on page 29: Updated "PSoC Creator Project Details" on page 30: Updated "LCD_Seg" on page 30: Updated Figure 5-4. Updated "ADC_DelSig" on page 35: Updated Figure 5-9. Updated "Code Example 2: LCD_Seg_Example2_StopWatch" on page 37: Updated "PSoC Creator Project Details" on page 40: Updated "LCD_Seg" on page 40: Updated Figure 5-17. Updated "Clock_SW" on page 46: Removed Figure "Pin Connection Mapping for Port A'". Replaced all instances of PSoC 5 with PSoC 5LP across the document. Replaced all instances of "CY8CKIT-050 DVK" to "CY8CKIT-050LP DVK" across the document. Updated to new template.
*K	4911948	09/08/2015	SRVS	No technical updates. Completing Sunset Review.
Distribution: External **Posting**: None				