CY8CKIT-015

PSoC® 1 Power Supervision Kit Guide

Doc. # 001-81218 Rev. **

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intnl): 408.943.2600
http://www.cypress.com

Copyrights

Flash Code Protection

Cypress products meet the specifications contained in their particular Cypress PSoC Data Sheets. Cypress believes that its family of PSoC products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as 'unbreakable'.

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

Contents

1. Introduction

1.1 Overview

Thank you for your interest in the CY8CKIT-015 PSoC® 1 Power Supervision Kit. This kit is part of the PSoC development kit ecosystem and is designed to work with the CY8CKIT-001 PSoC Development Kit (DVK) and CY8CKIT-035 Power Supervision Expansion Board Kit (EBK). It enables you to evaluate the system power supervision functions and capabilities of PSoC 1 devices. You can alter the example project, which is provided with the kit and described in this guide.

In general terms, power supervision is a combination of sequencing, monitoring, and control of multiple regulators or point-of-load DC power converters in a system. Typical solutions for power supervision include multiple devices, such as CPLDs, mixed-signal ASICs, and limited-functionality and inflexible discrete devices. Power supervision solutions require:

- Fault detection capabilities for high-availability systems
- Accurate and reliable power rail sequencing of the power converters during power-on and power-off events
- Voltage and current measurement of the power converters to optimize power consumption and for data logging
- Closed-loop control of the power converters through trimming and, for development and margining of voltage rails (for manufacturing test purposes)

The PSoC 1 Power Supervision Kit is used with the PSoC family of devices and is specifically designed and packaged for use with the PSoC 1 device family. PSoC 1 is a programmable system-on-chip platform that combines programmable analog and digital logic with a proprietary M8C processor. With the flexibility of the PSoC 1 architecture, you can easily create your own custom power supervision solution on a chip with the exact functionality you need.

1.2 Prerequisites

- CY8CKIT-001 PSoC Development Kit
- CY8CKIT-035 PSoC Power Supervision EBK

1.3 Features

The CY8CKIT-015 Power Supervision Kit demonstrates how to develop PSoC 1 based power system solutions with an example project, which describes a variety of functions including:

- Voltage sequencing
- Voltage and current measurement
- Voltage trimming and margining
- Over-voltage (OV) and under-voltage (UV) fault detection

1.4 Kit Contents

You can download the *CY8CKIT-015 Kit Setup* executable file from http://www.cypress.com/go/CY8CKIT-015. If you already have PSoC Designer and PSoC Programmer installed, download *CY8CKIT-015 Kit Only*.

The executable file includes the following:

- PSoC Designer™ 5.2 SP1 or later
- PSoC Programmer 3.14 or later
- Example firmware for the CY8C28645 PSoC 1 device (CY8CKIT_015_Example Project)
- Kit guide (this document)
- Quick start guide
- Release notes
- Application Note AN78646: Integrated Power Manager using PSoC 1

1.5 Development Kit Compatibility

This kit contains only downloadable materials from http://www.cypress.com/go/CY8CKIT-015 for development purposes and requires Cypress development kit platforms to use it. This kit is compatible with the CY8CKIT-001 PSoC DVK that hosts the CY8CKIT-020 processor module (CY8C28xxx Family processor module) and CY8CKIT-035 PSoC Power Supervision Expansion Board Kit (EBK).

1.6 Document History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	08/22/2012	KERI	Initial version of the kit user guide

1.7 Documentation Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes cautions or unique functionality of the product.

2. Getting Started

This chapter provides details on how to set up the hardware for demonstration.

2.1 Software Installation

1. Download the executable file, as described in 1.4 Kit Contents and run the file to install the PSoC 1 Power Supervision Kit software.

Figure 2-1. Kit Installer Menu

After the installation is complete, the kit contents are available in the following location:
`C:\Program Files\Cypress\PSoC 1 Power Supervision Kit\1.0`

When installing the kit software, the installer checks if your system has the required software. This includes PSoC Designer, PSoC Programmer, Windows Installer, .NET framework, Adobe Acrobat Reader, and Keil Compiler. If these applications are not installed, then the installer prompts you to install all prerequisite software, which is also available in the *CY8CKIT-015 ISO* file at http://www.cypress.com/go/CY8CKIT-015.

The software can be uninstalled using one of the following methods:

- Go to **Start > Control Panel > Add or Remove Programs**; select the appropriate software package and click the **Remove** button.

- Go to **Start > All Programs > Cypress > Cypress Update Manager > Cypress Update Manager**; select the **Uninstall** button for the appropriate software package.
- Run the executable file and click **Install CY8CKIT-015** button. In the CyInstaller for the PSoC 1 Power Supervision Kit 1.0 window, select **Remove** from the **Installation Type** drop-down menu. Follow the instructions to uninstall.

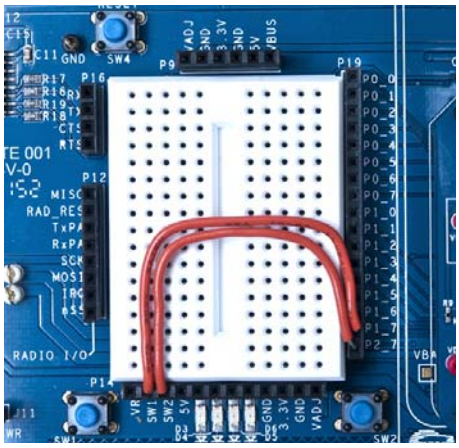
  Note This method will only uninstall the kit software and not all the other software that may have been installed along with the kit software.

2.2 Hardware Setup

The kit includes an example project for the CY8CKIT-001 PSoC DVK hardware platform to be used with the CY8CKIT-020 (CY8C28 Family processor module). CY8CKIT-015 does not include any hardware; it reuses Cypress CY8CKIT-035 PSoC Power Supervision EBK for demonstration. The following sections describe how to set up the hardware to run the example project.

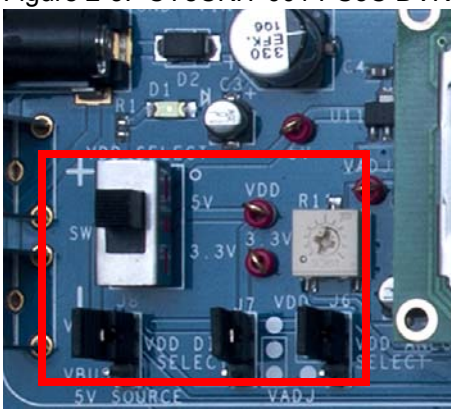
1. In the pin header or breadboard area of the PSoC DVK base board, use jumper wires to make the following connections:
   a. SW1 to P1_7
   b. SW2 to P2_7

Figure 2-2. CY8CKIT-001 PSoC DVK Breadboard



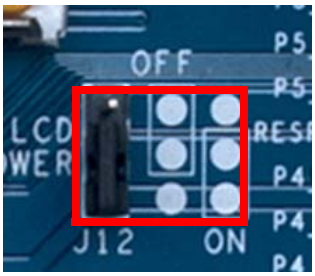
2. Set the system to run at 5 V using SW3 and set J6 VDD ANLG and J7 VDD DIG to VDD = 5 V using J6 and J7, as shown in Figure 2-3.

Figure 2-3. CY8CKIT-001 PSoC DVK Power Jumpers



3. Ensure that the LCD included with the PSoC DVK is attached and the LCD power jumper (J12) is in the ON position.

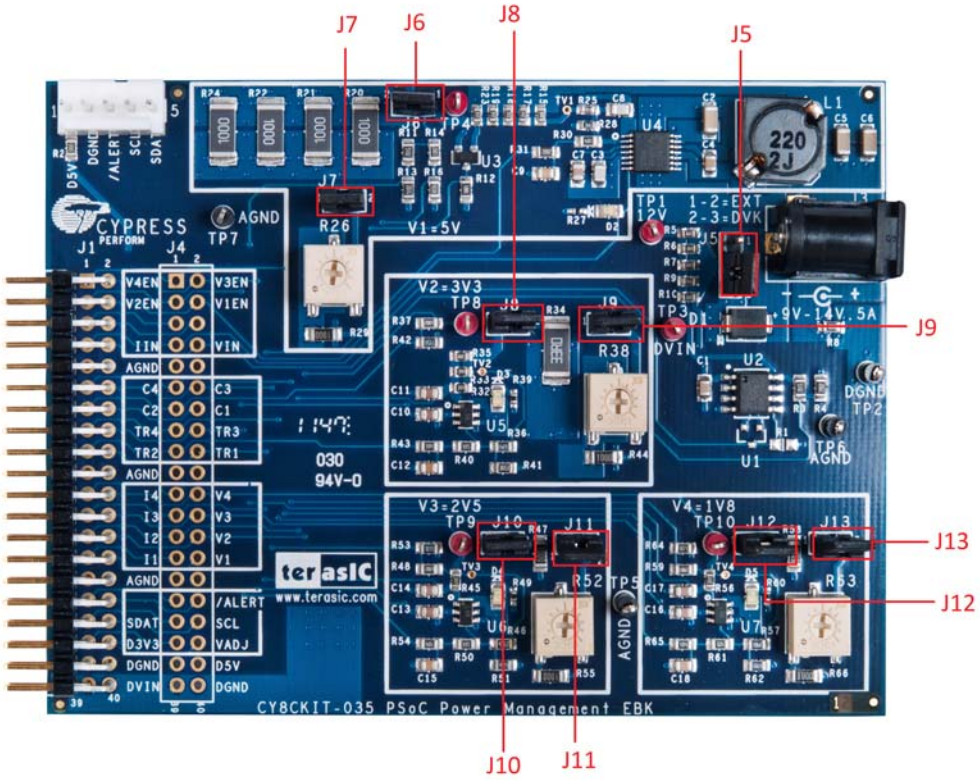
Figure 2-4. CY8CKIT-001 PSoC DVK LCD Power Jumper



4. Set jumpers on the CY8CKIT-035 as follows.

Jumper	Name	Setting
J5	12V_Source	12V_DVK (2-3)

Figure 2-5. J6 to J13 Jumpers Placed (default position)



CAUTION Do not attach the CY8CKIT-035 EBK to the PSoC DVK until you have programmed the PSoC 1 with the example project. The GPIOs routed to the EBK connect to the power regulator circuits. They may be damaged if firmware previously programmed into PSoC drives those pins. When the PSoC 1 has been programmed, attach the EBK to port A of the PSoC DVK.

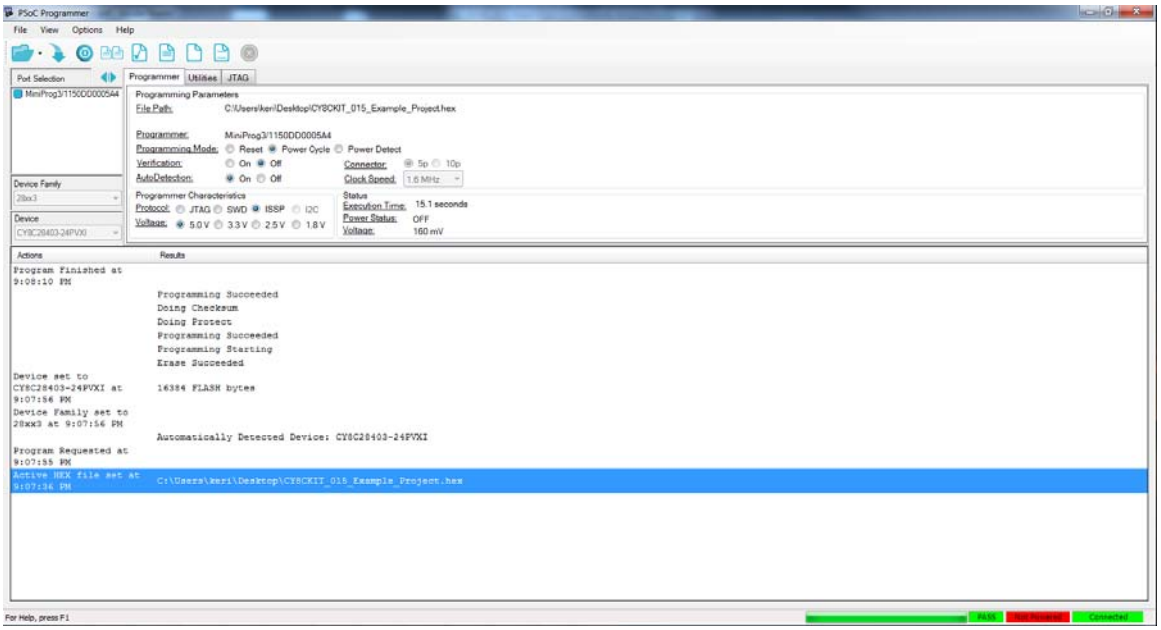
3. Example Project

The PSoC 1 Power Supervision Kit includes the CY8CKIT_015_Example_Project. This section provides instructions to run the example project.

3.1 Running the Example Firmware

1. Make sure the hardware is configured according to Hardware Setup on page 8.
2. If this is the first time that the example project firmware is being programmed into PSoC 1, make sure the EBK is not connected to the PSoC DVK.
3. Connect the MiniProg3 first to a USB port on the PC and then to the PROG port on the CY8CKIT-020 (CY8C28 Family processor module).
4. Open PSoC Programmer; connect to the MiniProg3 by clicking on the MiniProg3 device ID that appears in the Port Selection tab.
5. Browse to the hex file located in the firmware section of the CD contents; load the file using the **File Load** option; turn on **AutoDetection**; and select **Power Cycle** programming mode.
6. Select **ISSP** programming protocol and **5.0 V** programming voltage.

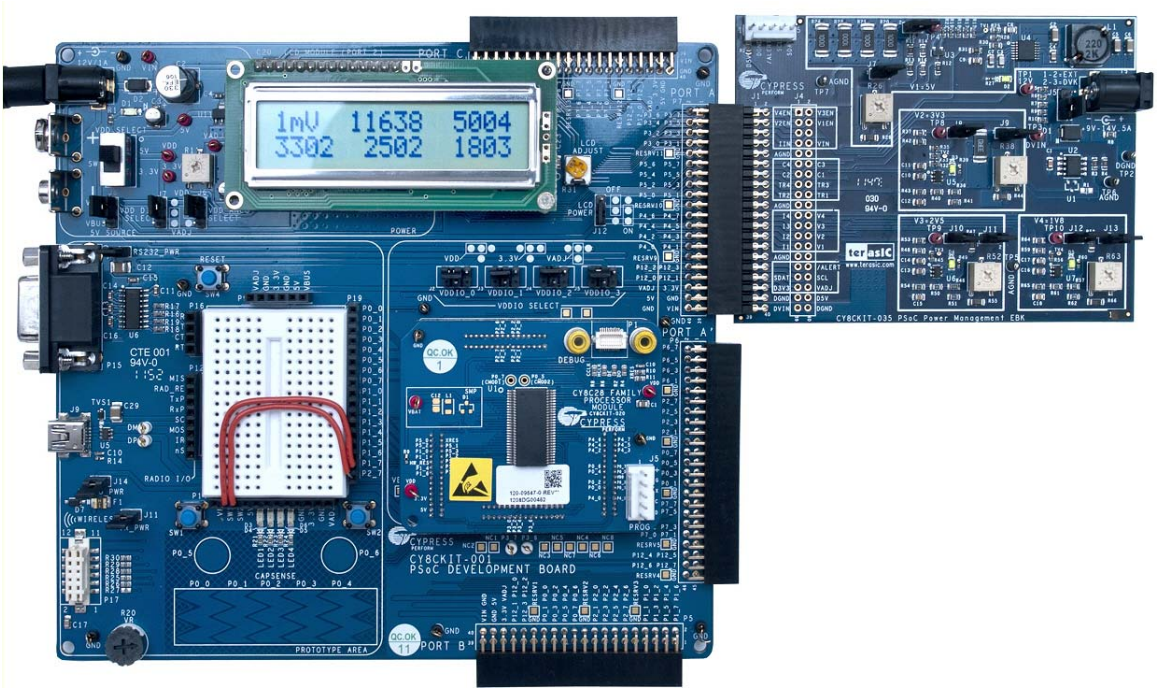
Figure 3-1. PSoC Programmer



7. Click on the **Program** tab to start programming.
8. Remove MiniProg3 from the DVK and attach the EBK to port A of the DVK.
9. On the EBK, make sure the power jumper (J5) is set to **DVK** (default setting).

10. Apply 12-VDC power to the PSoC DVK.
11. If the EBK cannot be detected by PSoC 1, an error message will be displayed on the LCD. If this happens, check if all the jumpers are positioned as mentioned in Hardware Setup on page 8.
12. If PSoC 1 detects the EBK, it automatically sequences the four rails on the EBK and displays the 4+1 voltages on the LCD, as shown in Figure 3-2.

Figure 3-2. CY8CKIT-001 PSoC DVK with CY8CKIT-035 EBK



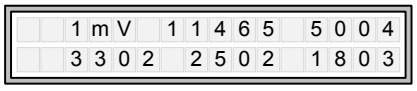
3.2 Example Project - Overview

This example demonstrates the following features:

- Voltage sequencing
- Under-voltage (UV) and over-voltage (OV) monitoring using the window comparator
- Voltage and current measurement accurate to better than 1%
- Trimming and margining accurate to better than 1%

If the project is running correctly, all four green LEDs on the EBK should be turned on and the debug LCD should display the voltages similar to Figure 3-3.

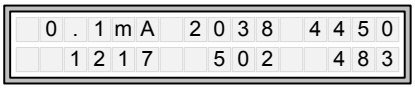
Figure 3-3. LCD Display - Voltages



The *1mV* display in the top left corner indicates the units of the 4+1 power supply voltage measurements. The next two numbers on the first line indicate the measured 12-V primary input voltage value and the measured 5-V rail value. The second line of the display indicates the measured 3.3-V, 2.5-V, and 1.8-V rail values. Note that regulator trimming is performed by PSoC 1 automatically to regulate the four secondary voltages to the nominal output. The primary 12-V input supply cannot be controlled by PSoC 1 so the voltage displayed may not be nominal.

Pressing and releasing SW1 on the CY8CKIT-001 PSoC DVK displays the supply currents measured on the EBK by PSoC 1 (see Figure 3-4).

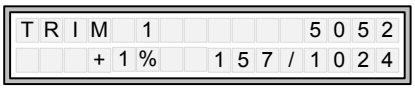
Figure 3-4. LCD Display - Currents



The *0.1mA* reading in the top left corner indicates the units of the 4+1 power supply current measurements. The next two numbers on the first line indicate the measured 12-V primary input load current value and the measured 5-V rail load current value. The second line of the display indicates the measured 3.3-V, 2.5-V, and 1.8-V rail load current values. Loads can be adjusted on EBK using the potentiometers. The load currents measured by PSoC's ADC converter can be compared with a digital multimeter (DMM) by removing the appropriate jumper and connecting the DMM configured to measure current.

Pressing and releasing SW1 on the CY8CKIT-001 PSoC DVK toggles the display between voltage and current measurements. Pressing and holding the SW1 on the CY8CKIT-001 PSoC DVK for a longer period will enable manual trimming control. The following example shows the manual trimming display for rail 1 (+5 V nominal); see Figure 3-5.

Figure 3-5. LCD Display - Trimming



The top line displays the actual voltage of the rail currently measured by PSoC 1. The left side of the second line shows the deviation from the nominal 5 V as a percentage. The right side of the second line shows the current PWM duty cycle used by the trimming hardware to achieve the currently selected voltage. In this mode, pressing and releasing SW1 on the CY8CKIT-001 PSoC DVK will trim the rail up in steps of approximately 2%. Pressing and releasing the SW2 on the CY8CKIT-001 PSoC DVK will trim the rail down in steps of approximately 2%. The actual voltages and PWM duty cycles will update in response to switch presses.

Trimming below or above the nominal voltage by more than 6% will cause the UV or OV window comparator fault detection circuit to trip; this turns off all regulators. The green LEDs on the EBK will be turned off in that case and the LCD will display "Power Fail, Press SW1". To restart the regulators, press SW1 on the CY8CKIT-001 PSoC DVK. The regulators will be powered up again, indicated by the green LEDs on EBK turning on. Note that all the regulators will turn on simultaneously and come back to the same trim menu where the rail fail happened.

When the trimming menu is displayed, pressing and holding SW1 on the CY8CKIT-001 PSoC DVK for a longer period will enable manual trimming control for the next secondary regulator. To return to the main voltage display menu, cycle through all four manual trim menus by pressing and holding SW1 on the CY8CKIT-001 PSoC DVK for a longer period.

When displaying voltages or currents on LCD, if you remove jumper J6 on the EBK, it cuts the power to regulators 2 through 4. This causes an UV fault on rails 2 through 4 and the display appears as shown in Figure 3-6.

Figure 3-6. LCD Display - Under Voltage

Note also that the PSoC 1 is programmed to shut down all rails on any fault condition. Therefore, all four green LEDs on the EBK should turn off when jumper J6 is removed. To power the sequencer again, replace J6 and press and hold the retry switch (SW1 on the CY8CKIT-001 PSoC DVK).

Note Apart from the signals intended for the expansion board kit, other internal analog and digital signals from PSoC 1 are also routed to the GPIOs. Because of this, touching the port pins on the development kit may cause undesirable change in the functionality of the project. If this happens, reset the PSoC 1 device to restart by pressing the SW4 Reset switch on the CY8CKIT-001 PSoC DVK.

3.3 PSoC 1 Power Supervisor Solution

The CY8CKIT-035 PSoC Power Supervision Expansion Board Kit (EBK) contains four DC voltage regulator circuits. They all have enable inputs to allow PSoC 1 to control the power-up and power-down sequencing of the regulators. They also have the necessary passive components to enable PSoC 1 to measure their output voltage and load currents using its in-built analog-to-digital converter (ADC). The regulators have a feedback option that allows PSoC 1 to trim (margin) their output voltage.

The EBK has the necessary passive components to enable PSoC 1 to detect under-voltage (UV) and over-voltage (OV) fault conditions using its internal window comparator hardware.

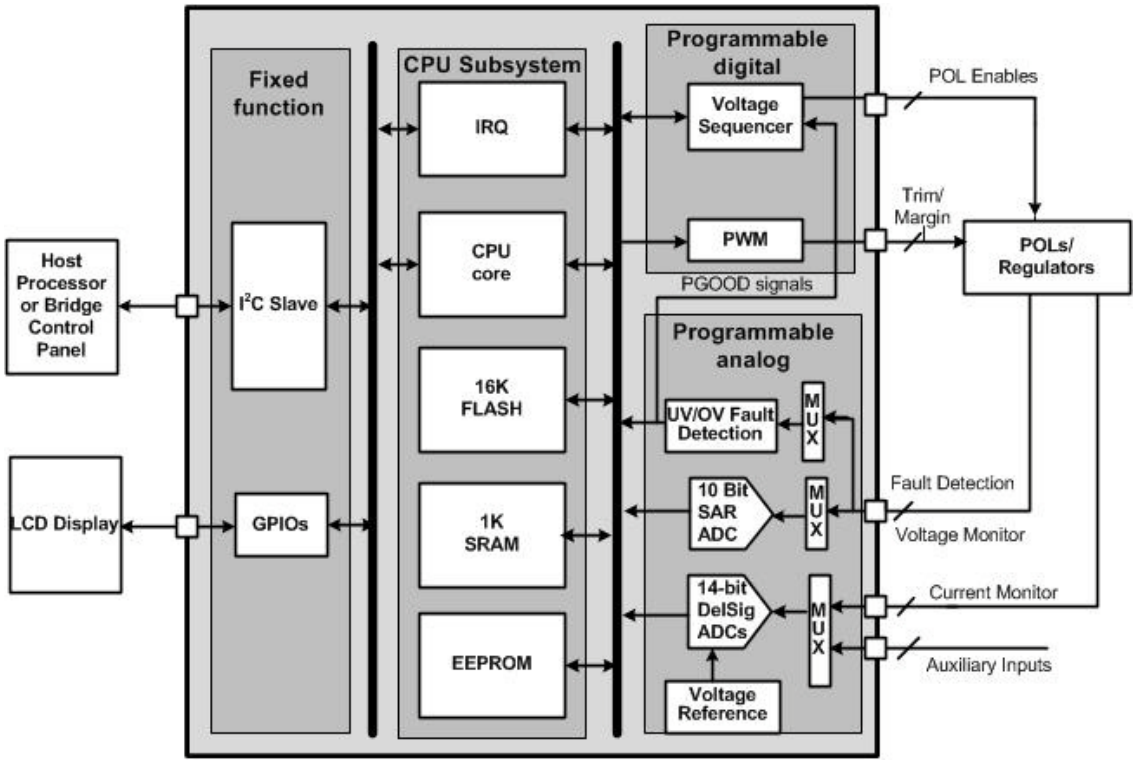
The CY8CKIT-035 EBK also provides an I2C/SMBus/PMBus compatible header to support systems that need to communicate with a host controller.

All of this functionality is implemented on a single PSoC. The EBK routes all the input/output signals for power supervision to a PSoC 1 (CY8C28xxx processor module) mounted on a development kit platform such as the CY8CKIT-001 PSoC Development Kit. PSoC 1 is not mounted on the EBK itself.

Figure 3-7 shows a high-level overview of the 4+1 power supervision solution, which can be implemented using the EBK. Up to four secondary regulators can be sequenced through the logic-level enable outputs (labeled as EN[4]). The four secondary voltage rails along with one primary input power rail (labeled as V[4+1]) are multiplexed into a 10-bit, SAR ADC configured for a single-ended input range of 0 mV to 4160 mV at 150 ksps with a 1.5% accurate internal reference. For load current measurements of 3.3-V, 2.5-V, and 1.8-V rails across a series shunt resistor (labeled as I[4+1]), a 14-bit delta-sigma ADC is used along with an instrumentation amplifier with an input range of 0 mV to 520 mV at 7.8 ksps. For load current measurements of supply rail and 5.0-V rail, a Current Sense Amplifier (CSA) is used in the EBK. Another 14-bit delta-sigma ADC along with a PGA is used for the current measurements of these two rails.

The measured voltages are used to increase or decrease the duty cycles of the pulse-width-modulator (PWM) outputs for regulator trimming and margining. The trim or margin PWM outputs from PSoC 1 (labeled as TR[4]) are filtered with a single RC filter stage on the EBK and fed into the voltage feedback input of the regulators. A single time-multiplexed window comparator is implemented in PSoC 1 using two voltage digital-to-analog converters (DAC) (to set the UV and OV limits for each rail), two comparators, and two programmable glitch filters. This window comparator loops through each channel that it monitors (labeled as V[4+1]).

Figure 3-7. PSoC 1 Power Supervision Functional Diagram



Note that the EBK hardware supports up to four secondary regulator circuits. The PSoC 1 Power Supervisor solution can be easily extended to support up to eight secondary regulator circuits.

3.4 Technical Details

3.4.1 Voltage Sequencing

Voltage sequencing is a major function of any power supervisor IC. The supply voltages to different sub-systems of a complex system are required to be sequenced depending on operating conditions, such as power up, power down, and fault conditions to ensure proper operation of all the devices. As the system becomes more complex, the number of different supply voltages in a single system increases. Therefore, an accurate and reliable power sequencing solution is required.

When powering up the system, each of the voltage regulators needs to be powered one after the other in a sequence with programmable delays between each of them. During sequencing, the controller enables the voltage regulator, monitors its rail for the voltage level, and proceeds to the next rail only if the voltage level is within the user-defined UV/OV range. If a power rail does not reach the expected voltage level, the controller must indicate a sequencing fail.

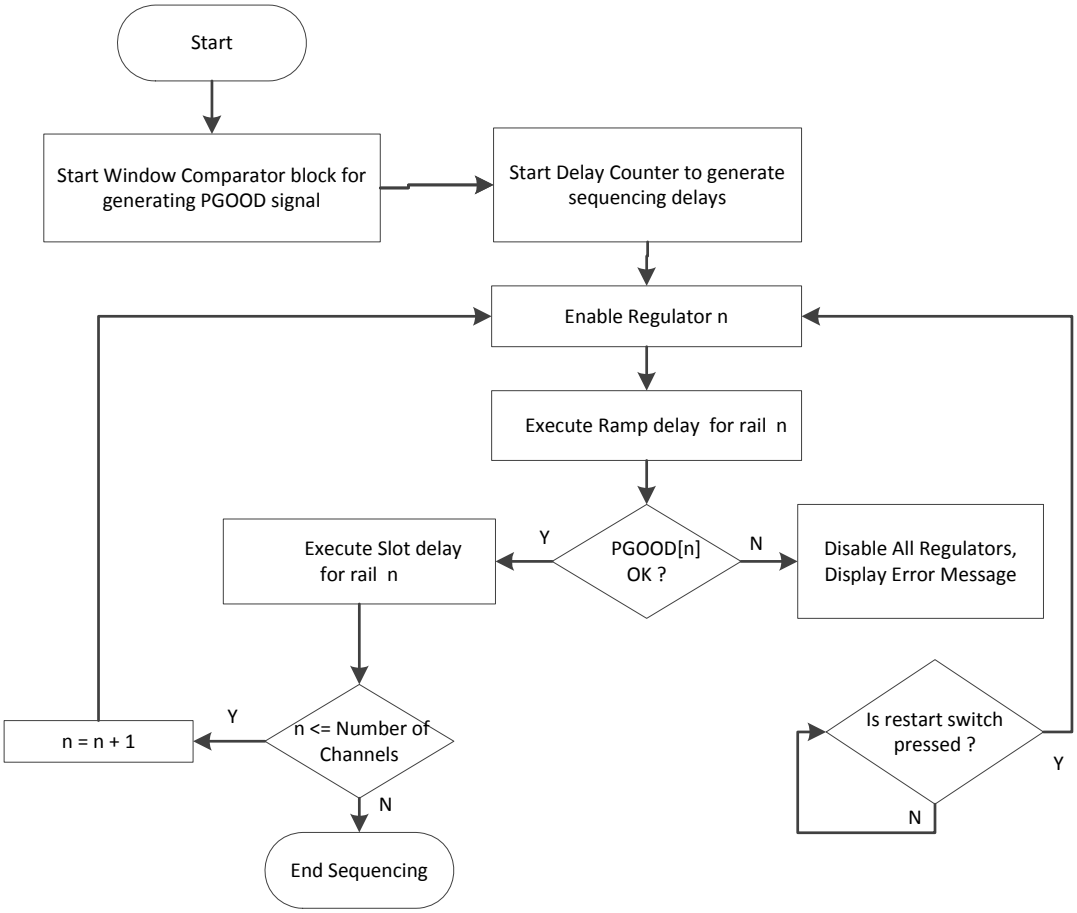
This implementation uses the following resources:

- A 16-bit counter for generating user-defined delays. Two digital blocks of PSoC 1 are used to create a 16-bit counter with a 50-kHz internally generated clock as the time base, which gives the maximum counting time interval of 1.31 seconds before overflowing. The API provided can be used to generate a time delay from 1 to 1.31 seconds in steps of 1 msec.
- Four GPIOs to enable or disable four voltage regulators on the CY8CKIT-035 board.

- A Power Good (PGOOD) signal that indicates the correctness of the voltage on a particular rail. The PGOOD signal can be generated by either the regulator or the controller. Currently, it is generated by PSoC 1 using a window comparator. The window comparator is explained in detail in the next section.

When a sequencing fails, all the regulators will be disabled simultaneously. An error message along with the rail number that is faulty is displayed on the LCD. With some modifications to the firmware, you can easily implement power-down sequencing in different orders when a power fail occurs.

Figure 3-8. Voltage Sequencer Flowchart



The voltage sequencing algorithm works depending on the following parameters:

- Sequencing Mode: This indicates the sequencing order in which the four rails must be powered up. Six different modes are available.
- Ramp Delay: This indicates the time that the sequencer must wait before monitoring the rail for its goodness (checking the PGOOD) after the regulator is enabled.
- Slot Delay: This indicates the time that the sequencer must wait before sequencing the next rail after the current rail is verified with the correct voltage (PGOOD = 1).

To change the behavior of the voltage sequencer, change the parameters for the sequencer. To do this, open the *configuration.h* file of the project in PSoC Designer 5.2 SP1. Change the definition of DEFAULT_SEQUENCING_MODE by choosing any of the defined sequencing modes from

SEQUENCING_MODE_1 to SEQUENCING_MODE_6. This changes the sequencing order of the rails.

```
/* Definitions for Sequencing modes */
#define SEQUENCING_MODE_1 1          /* CHANNEL 1 -> CHANNEL 2 -> CHANNEL 3 -> CHANNEL 4 */
#define SEQUENCING_MODE_2 2          /* CHANNEL 1 -> CHANNEL 2 -> CHANNEL 4 -> CHANNEL 3 */
#define SEQUENCING_MODE_3 3          /* CHANNEL 1 -> CHANNEL 3 -> CHANNEL 2 -> CHANNEL 4 */
#define SEQUENCING_MODE_4 4          /* CHANNEL 1 -> CHANNEL 3 -> CHANNEL 4 -> CHANNEL 2 */
#define SEQUENCING_MODE_5 5          /* CHANNEL 1 -> CHANNEL 4 -> CHANNEL 2 -> CHANNEL 3 */
#define SEQUENCING_MODE_6 6          /* CHANNEL 1 -> CHANNEL 4 -> CHANNEL 3 -> CHANNEL 2 */

#define DEFAULT_SEQUENCING_MODE SEQUENCING_MODE_1
```

Similarly, you can change the ramp delays and slot delays to be used for sequencing by changing the default delays in the same header file. The entered delay must be in msec. from 1 to 1300.

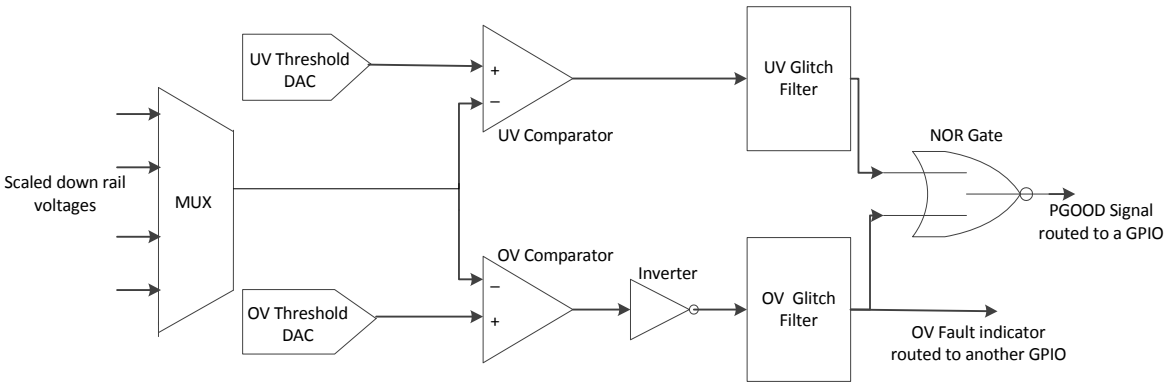
```
/*Default Slot Delays for each channel in msec */
#define SLOT_1_DELAY 500
#define SLOT_2_DELAY 500
#define SLOT_3_DELAY 500
#define SLOT_4_DELAY 500

/* Default Ramp Delays for each channel in msec */
#define RAMP_1_DELAY 10
#define RAMP_2_DELAY 10
#define RAMP_3_DELAY 10
#define RAMP_4_DELAY 10
```

3.4.2 UV and OV Monitoring using Window Comparator

To support under-voltage (UV) and over-voltage (OV) fault detection on the four secondary power supply rails, eight comparators and eight programmable DACs are required. As the number of regulators in the systems expands, the number of comparators and DACs required becomes excessive. To make more efficient use of analog hardware resources, an alternative implementation is provided.

As shown in Figure 3-9, a single window comparator and glitch filter are time-multiplexed across all the rails requiring monitoring. The voltage regulator output for rail[n] (signal V[n]) of the power rail is compared against the OV and UV thresholds using two hardware comparators. If the voltage level is not within these thresholds, the appropriate comparator generates the fault signal.

Figure 3-9. Time Multiplexed OV and UV Fault Detection Hardware



The UV comparator checks for under-voltage fault; output will be high if there is a fault. The OV comparator checks for over-voltage fault; output (after the inverter) will be high if there is a fault. Eight-bit DACs are used to generate the user-defined UV and OV thresholds.

When the inputs to the comparator become nearly equal, the comparator's output may contain glitches leading to unstable fault detection output. To fairly detect the fault, you must ignore the rare glitches (transitions from 0 to 1 and 1 to 0) in the comparator's output. To do this, glitch filters are implemented at the output of the comparators. The glitch filter will indicate a fault only when the comparator indicates a fault for a sufficient amount of time. The time required to get an accurate PGOOD signal is determined by trial and error. This time depends on the glitch filter's clock; for this reason, it is programmable. In the current implementation, the glitch filter waits for four updates of the comparator output. If all four updates indicate a fault, the glitch filter asserts fault. This way, you can eliminate any glitches from the comparator whose time period is less than four updates.

The PGOOD signal indicates whether the voltage is within the UV/OV range. This is a NOR'ed signal of the OV and UV comparator outputs. If any fault exists, PGOOD becomes 0 to indicate the fault. This is routed to a GPIO, and its falling edge interrupt is enabled. Whenever a fault occurs, the CPU will be interrupted. After the PGOOD interrupt occurs, the OV fault indicator (which is routed to another GPIO) is checked to find out whether the fault was UV or OV. Within the ISR, all rails are monitored and checked for their PGOOD status to capture all faulty rails.

Note that on the EBK, the four secondary regulator output voltages are scaled down to normalized value and routed out as signals C[4:1]. These are provided especially for rapid fault detection to have an independent multiplexing loop apart from the voltage measurement loop. This provides the best possible fault detection time. In this example project, those signals are not used because of the I/O limitation on Port A of the DVK. The signals V[4:1] are used for both fault detection and voltage monitoring. However, AN78646 - Integrated Power Manager Using PSoC 1, implements rapid fault detection by using C[4:1] signals through a custom cable. Detailed user module (UM) and register-level implementation of comparators, glitch filters, and other finer details regarding the window comparator are discussed in the Appendix section of the application note.

The fault detection feature works based on the following parameters:

- UV threshold percentage: This indicates the under-voltage threshold for the power rails in terms of –ve percentage of deviation from nominal voltage.
- OV threshold percentage: This indicates the over voltage threshold for the power rails in terms of +ve percentage of deviation from nominal voltage.

Example:

If UV threshold = 5%, then the UV threshold voltage = Nominal voltage × 95%.

If OV threshold = 5%, then the OV threshold voltage = Nominal voltage × 105%.

These voltages are generated by the DAC. The window comparator detects the fault when the input voltage crosses these two threshold voltages.

These UV/OV percentages can be changed for each rail by changing the definitions in the project's *configuration.h* file. The default values are 6%, as shown here.

```
/* Default Fault threshold percentages */
#define UV_THRESHOLD_1 6        /* For Rail 1 */
#define OV_THRESHOLD_1 6
#define UV_THRESHOLD_2 6        /* For Rail 2 */
#define OV_THRESHOLD_2 6
#define UV_THRESHOLD_3 6        /* For Rail 3 */
#define OV_THRESHOLD_3 6
#define UV_THRESHOLD_4 6        /* For Rail 4 */
#define OV_THRESHOLD_4 6
```

3.4.3 Voltage and Current Measurements

Voltage monitoring in a power supervision system is measuring all of the rail voltages. The measured rail voltages can be used for trimming and to regulate the power consumption based on the load connected to the rail. Also, the voltages can be communicated to the host so that it can log the information.

A dedicated 10-bit SAR ADC is used to measure voltages of four rails on the CY8CKIT-035. The four rail voltages from EBK are multiplexed to the same SAR ADC. The reference for ADC is derived from the on-chip reference generator multiplex (RefMux) and the conversion range is selected as 0 V to 4.16 V. Both the 5-V rail and 12-V power rail are scaled down to within the ADC range. Because the measured voltage is used for trimming, the voltage measurement and trimming are inter-related and occur sequentially.

4+1 current monitoring uses two 14-bit delta-sigma ADCs. The currents delivered by 12-V and 5-V rail are measured by one of those ADCs in a single-ended mode along with a unity gain buffer. Both these rails have an high-side current sense amplifier each on the EBK to provide single-ended signal for current measurement. The currents delivered by 3.3-V, 2.5-V, and 1.8-V rails are measured using the other delta-sigma ADC along with an instrumentation amplifier. These rails have series sense resistors on high sides on EBK. The instrumentation amplifier converts the differential signal across the sense resistor to single-ended signal. The two ADCs are used because of the different input ranges, which cannot be accommodated with a single ADC. The delta-sigma ADCs works with the same reference voltage as that of SAR ADC.

At the time of multiplexing, after the input to the ADC is changed, three samples of digital data must be discarded. This is required because the delta-sigma ADC works by oversampling the input and decimating the single-bit results. Because all output data is dependent on analog input over a period of time, the conversions that happen after changing the input will be invalid.

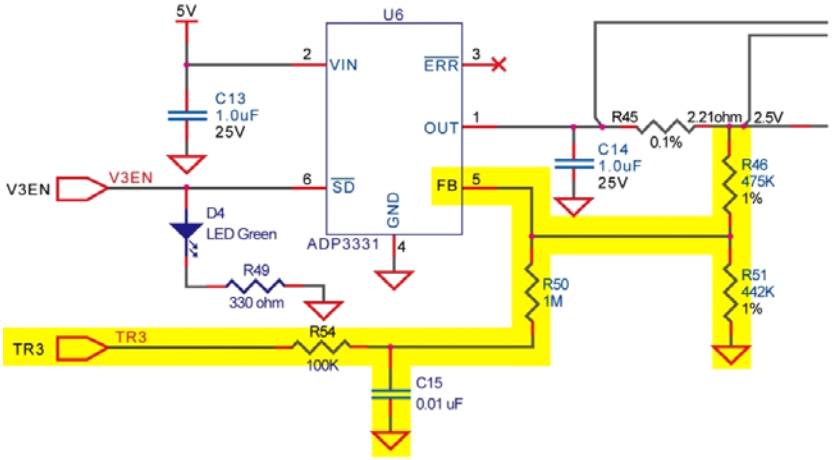
3.4.4 Regulator Trimming and Margining

To trim (fine tune) each regulator output, apply a controlled analog voltage to the "feedback" (VFB) or "adjust" (VADJ) analog control pin on the regulators. To support trimming on the four secondary power supply rails, four additional DACs to the ones already being used are required for the UV or OV window comparator circuit. As the number of regulators in the system expands, the number of DACs required for trimming and margining becomes excessive. To make more efficient use of analog hardware resources, an alternative implementation is developed based on PWM blocks with external RC filter networks to achieve the equivalent result. Because PSoC can measure the analog voltage of each rail, a closed loop control system can be implemented to fine tune each regulator output beyond the accuracy specifications of the regulators themselves.

The circuit in Figure 3-10 shows the detail of the trimming and margining circuit for the V3=2.5-V rail. The output scaling network of R46 and R51 are the recommended values provided by the regulator manufacturer to ensure that the regulator can sense its own output voltage and regulate it as the load varies. The TR3 pin is a PWM output signal from PSoC that is filtered by R54/C15; that voltage is summed into the FB pin of the regulator through R50.

If the PWM duty cycle controlled by PSoC 1 is reduced, the voltage applied to the FB will reduce and the regulator will respond by increasing its output voltage. Conversely, if the PWM duty cycle is increased, the voltage applied to the FB pin will increase and the regulator will respond by decreasing its output voltage. Typical power supplies respond in this manner; for others that do not, this circuit both internal to PSoC 1 and external can be customized for the specific power supply chosen (for example, inverting the PWM output such that a decrease in PWM duty cycle decreases the regulator output voltage).

Figure 3-10. Margin and Trim Circuit for the V3=2.5-V Rail



Margining is similar to trimming but is used for manufacturing test purposes. In this case, the rails are intentionally set to their upper or lower limits to enable system designers to verify that their systems work at both extremes of the voltage rail tolerances. For example, if a 5-V rail is used in the system and specified to have an accuracy of ± 5%, margining will set the rail to 5 V –5% to enable system verification. Then the rail can be margined to the high side of 5 V +5% and the system verified again. This capability exists on all four rails controlled by PSoC 1 in this example project.

The trimming feature works based on the 'Trim Percentage' parameter. This configurable parameter indicates the amount to which the rail voltage must be trimmed in terms of percentage of nominal voltage of that rail. Each of the rails can have a different trim percentage. By default, the trim percentages is set to '0' to get the expected rail voltages. However, there will be trimming error of at least 4 mV because of ADC measurement resolution of 4 mV. To change the trim percentages, the definitions must be changed in the *configuration.h* file of the project, as shown here.

```
/* Default Trim Percentages for each channel */
#define TRIM_PERCENTAGE_CHANNEL_1 0
#define TRIM_PERCENTAGE_CHANNEL_2 0
#define TRIM_PERCENTAGE_CHANNEL_3 0
#define TRIM_PERCENTAGE_CHANNEL_4 0
```

3.4.5 Other Features

- I2C/SMBus/PMBus interface to a host CPU (available on the white 5-pin header on the EBK).
- EEPROM for calibration/configuration parameters, fault logging, and so on.

Detailed description of how to make use of those features is not currently covered by this document. Example projects covering these topics in more detail will be added in the future.

3.4.6 Firmware Flowchart

The firmware has the following initialization steps:

1. Display the introductory message and initialize the system parameters
2. Check for EBK connectivity and wait until it is connected
3. Initialize PWM trim/margin hardware
4. Initialize fault detection hardware

When the initialization is complete, all the rails will be sequenced according to the specified order. The main loop runs the following functions:

1. Measure supply voltage
2. Measure supply current
3. Measure all other secondary rail voltages
4. Trim each regulator
5. Measure all secondary rail currents
6. Display the voltages/currents on LCD
7. Handle user interface

In addition to the main loop flow, there is an additional thread that runs autonomously and asynchronously from the main loop. This is the fault interrupt service routine (ISR) thread (see Figure 3-12). After the sequencing is complete, the fault detection ISR will be enabled; it generates an interrupt if any fault occurs on any rail. That interrupt routine will find out the rails that have faults and shuts down all the rails.

Figure 3-11. Example Firmware Main Loop Flowchart

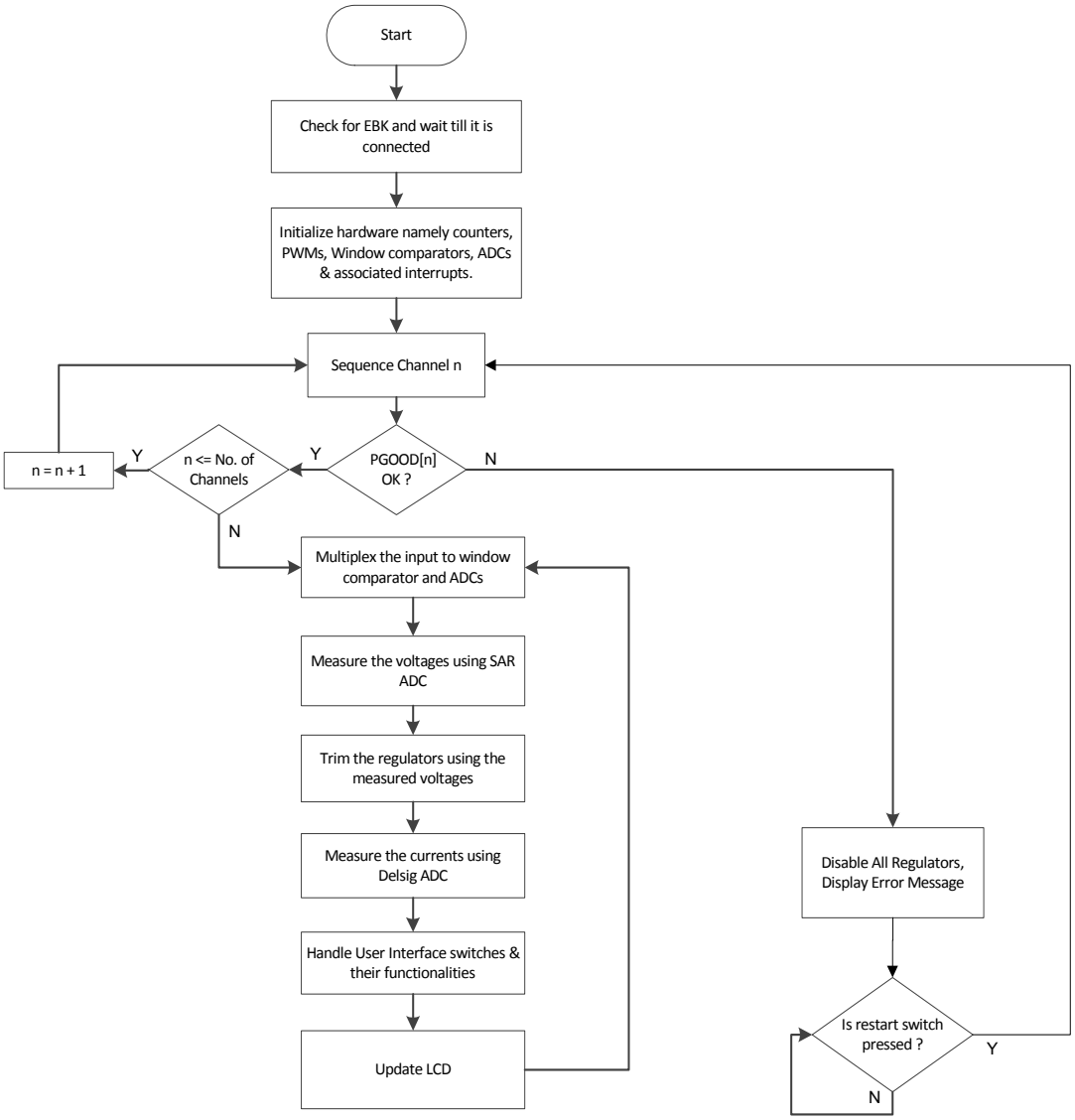
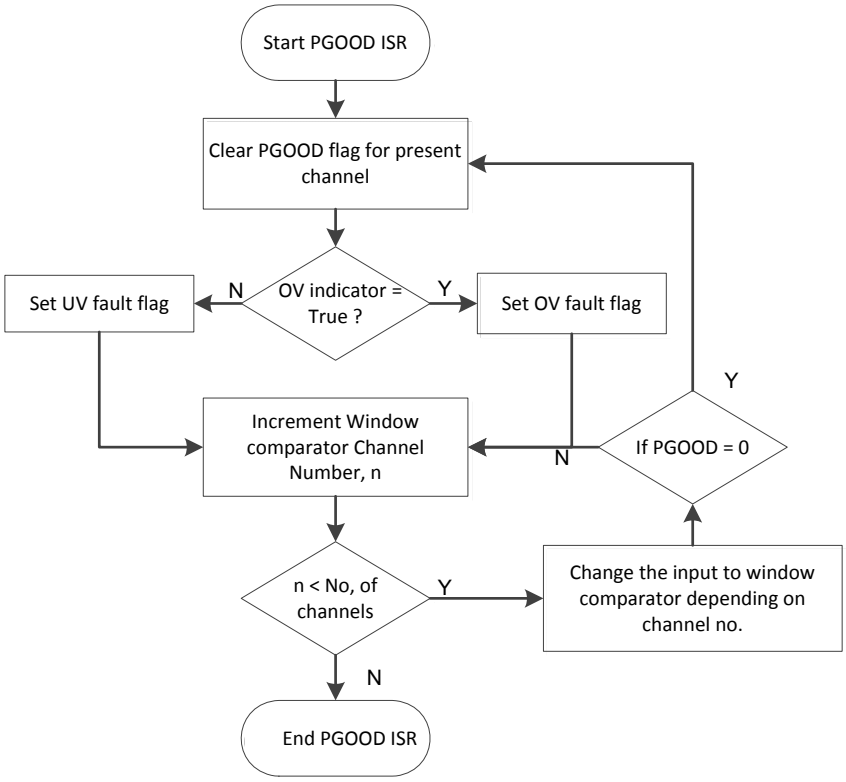


Figure 3-12. PGOOD ISR Flowchart



3.4.7 PSoC 1 Resource Usage Details

The following table lists the resources used inside PSoC 1.

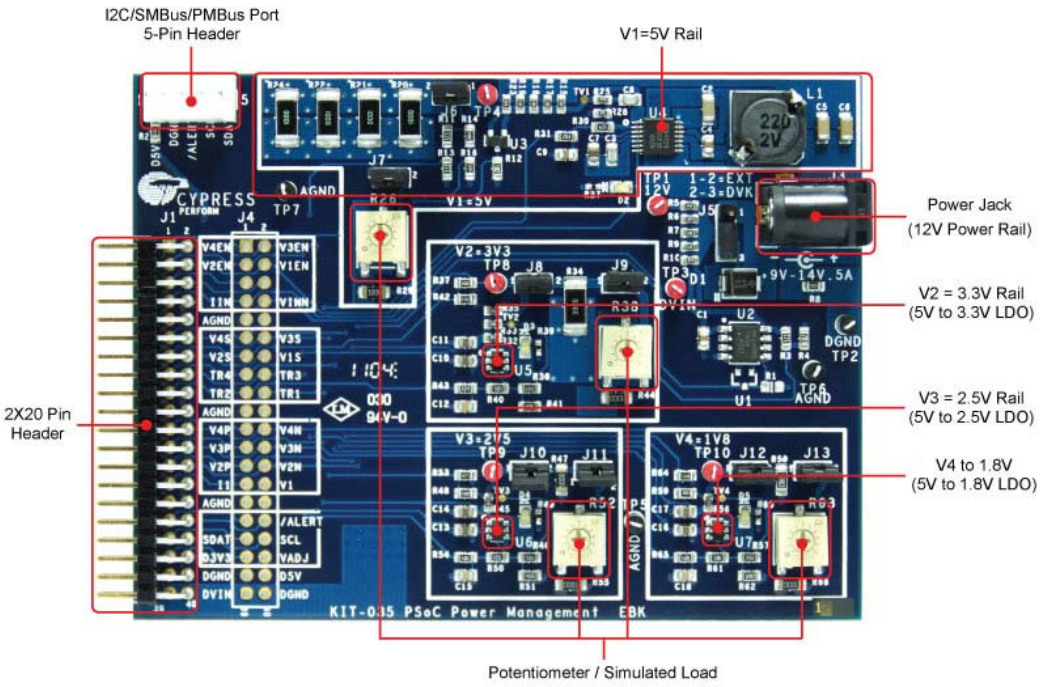
Table 3-1. Resource Usage

IP	Functions	Digital Blocks	Analog Blocks	Pins
Voltage Sequencer	16-bit counter	2	0	4
Voltage Measurement ADC	10-bit SAR ADC	0	0	5
Current Measurement ADC	2 14-bit Del-Sig ADCs, PGA, and instrumentation amplifier	0	7	8
Window Comparator with Glitch Filter	2 comparators, 2 DACs, and 2 PRS as glitch filters	2	6	4
PWM Trim/Margin	4 16-bit PWM blocks	8	0	4

A. Appendix

A.1 PSoC Power Supervision EBK Hardware Overview

Figure 0-1. EBK Hardware Components



The Power Supervision EBK board consists of a 12-V primary input power source and four secondary voltage rails: V1 = 5 V, V2 = 3.3 V, V3 = 2.5 V, and V4 = 1.8 V. Voltage rail V1 feeds power to the other three rails V2, V3, and V4. Therefore, disabling V1 will disable V2 to V4. Each secondary rail consists of a regulator with enable input, circuitry that enables PSoC 1 to apply a DC control voltage to the regulator feedback or adjust pin, as well as fixed and adjustable (potentiometer) load elements. Two jumpers are provided for each rail to disconnect all loads or disconnect only the adjustable load.

The EBK provides an I2C/SMBus/PMBus connector. A 40-pin (2×20) header J1 is provided to connect this board with the host PSoC 1 on a development kit platform, such as the CY8CKIT-001 PSoC DVK. The header carries voltage enables, regulator voltage, regulator load currents, and trim/margin control signals for each regulator on the EBK. The I2C physical layer signals (SDA/SCL) from the PSoC 1 are also routed across this header to allow connection to an external host or management processor that supports standard I2C, SMBus, or PMBus protocol interfaces.

A.1.1 2x20 Pin Interface Header

The following table outlines the definition of the 40-pin J1 header interface.

Table A-1. 2x20 Header (J1) Pin Definition

Description	Signal	Pin	Pin	Signal	Description
Voltage Regulator 4, Enable	V4EN	1	2	V3EN	Voltage Regulator 3, Enable
Voltage Regulator 2, Enable	V2EN	3	4	V1EN	Voltage Regulator 1, Enable
–	NC	5	6	NC	–
Power Rail Current (measured as single-ended voltage)	IIN	7	8	VIN	Power Rail Sensing Voltage
Analog Ground	AGND	9	10	NC	–
Voltage Regulator 4, Fault Sensing Voltage (Not Used)	C4	11	12	C3	Voltage Regulator 3, Fault Sensing Voltage (Not Used)
Voltage Regulator 2, Fault Sensing Voltage (Not Used)	C2	13	14	C1	Voltage Regulator 1, Fault Sensing Voltage (Not Used)
Voltage Regulator 4, Trim	TR4	15	16	TR3	Voltage Regulator 3, Trim
Voltage Regulator 2, Trim	TR2	17	18	TR1	Voltage Regulator 1, Trim
Analog Ground	AGND	19	20	NC	-
Voltage Regulator 4, Current (Measured as differential voltage)	I4	21	22	V4	Voltage Regulator 4
Voltage Regulator 3, Current (Measured as differential voltage)	I3	23	24	V3	Voltage Regulator 3
Voltage Regulator 2, Current (Measured as differential voltage)	I2	25	26	V2	Voltage Regulator 2
Voltage Regulator 1 Current (Measured as single-ended voltage)	I1	27	28	V1	Voltage Regulator 1
Analog Ground	AGND	29	30	NC	–
–	NC	31	32	/ ALERT	Alert Signal (I2C/SMBus/ PMBus)
Serial Data (I2C/SMBus/PMBus)	SDAT	33	34	SCL	Serial Clock (I2C/SMBus/ PMBus)
unused	D3V3	35	36	VADJ	unused
Digital Ground	DGND	37	38	D5V	unused
Optional 12V Power from DVK	DVIN	39	40	DGND	Digital Ground

A.1.2 EBK Headers and Jumpers

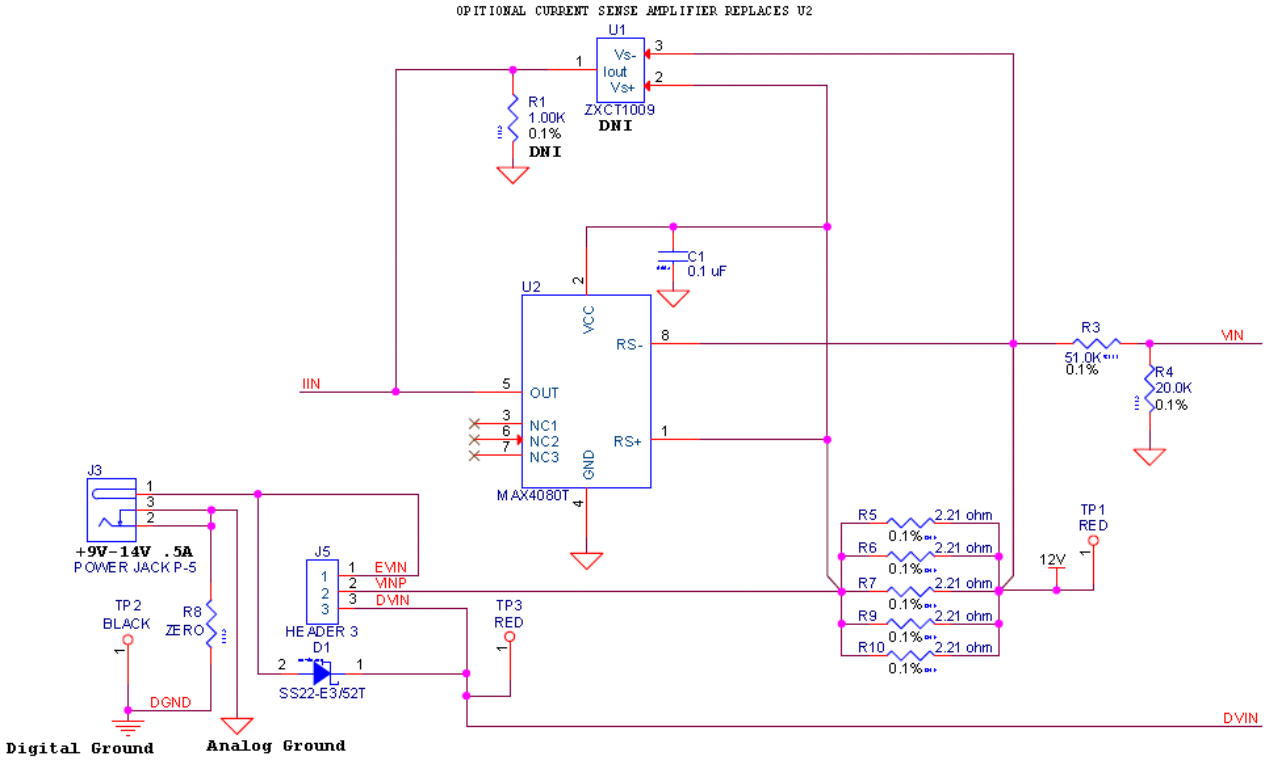
A number of headers and jumpers are provided on the EBK. The following table outlines the function of each item and the default configuration.

Table A-2. EBK Jumper Settings

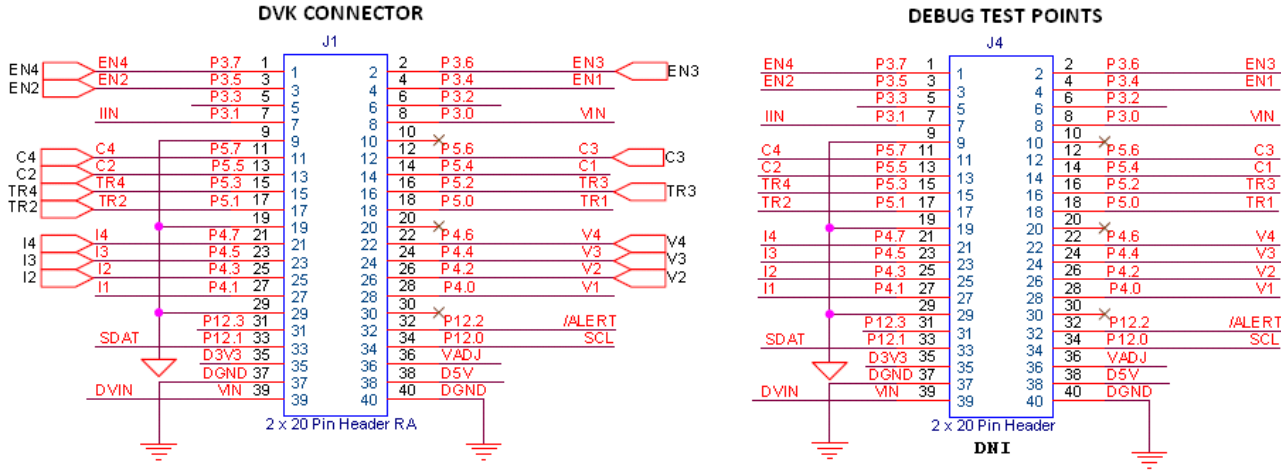
PCB Designator	Description	Factory Default Configuration
J1	2×20 pin header for connecting to PSoC DVK	–
J2	5-pin header for connecting an external host or management processor via I2C/SMBus/PMBus	–
J3	Power jack	–
J4	2×20 pin header that replicates signals on J1 for easy connection to a logic analyzer or oscilloscope	–
J5	3-pin header for primary input power source selection. Place jumper in 1-2 position to source power from the DC power jack J3. Place in 2-3 position to source power from the PSoC platform DVK	2-3 position
J6	2-pin header for connecting all loads on V1=5-V rail (this includes the fixed and adjustable loads on V1 as well as the load presented by the V2, V3, and V4 rails)	Installed
J7	2-pin header for connecting the potentiometer load on V1=5-V rail	Installed
J8	2-pin header for connecting both loads on V2=3.3-V rail (fixed and adjustable)	Installed
J9	2-pin header for connecting potentiometer load on V2=3.3-V rail	Installed
J10	2-pin header for connecting ALL loads on V3=2.5-V rail (fixed and adjustable)	Installed
J11	2-pin header for connecting variable potentiometer on V3=2.5-V rail	Installed
J12	2-pin header for connecting ALL loads on V4=1.8-V rail (fixed and adjustable)	Installed
J13	2-pin header for connecting variable potentiometer on V4=1.8-V rail	Installed

A.2 CY8CKIT-035 Schematics

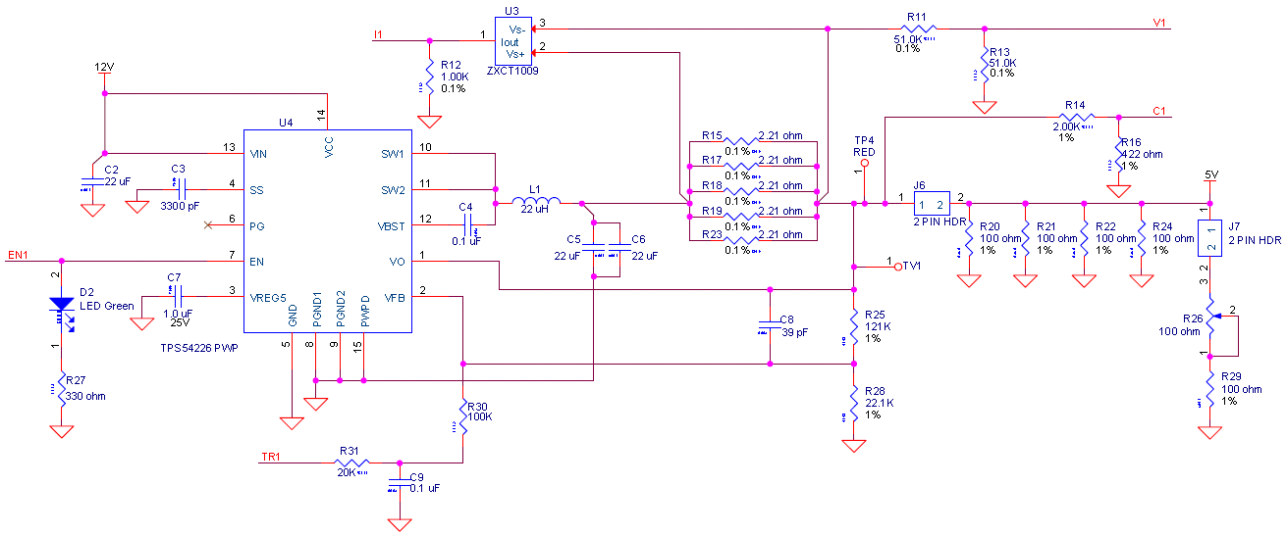
A.2.1 Primary 12-V Power Input



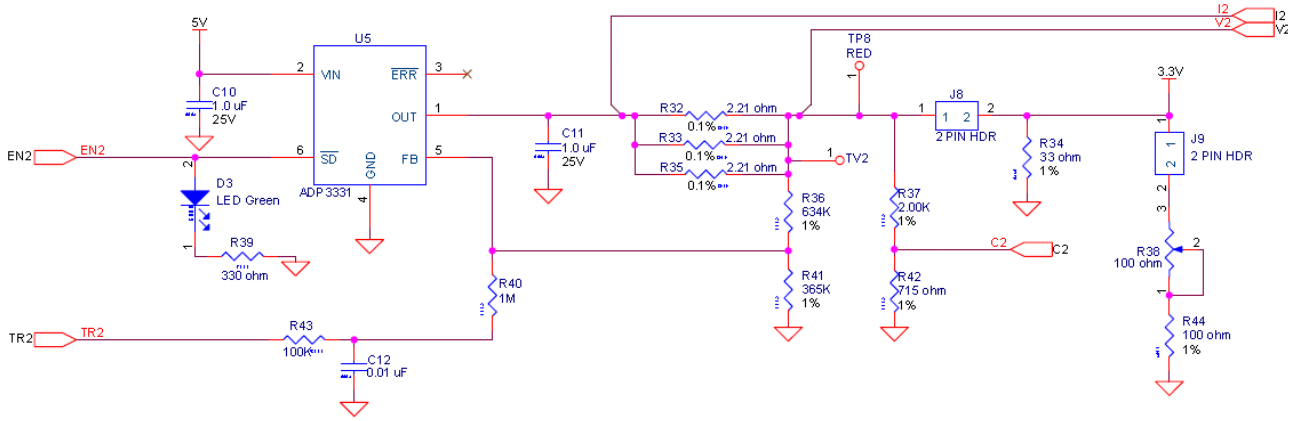
A.2.2 DVK Connector and Debug Test Points



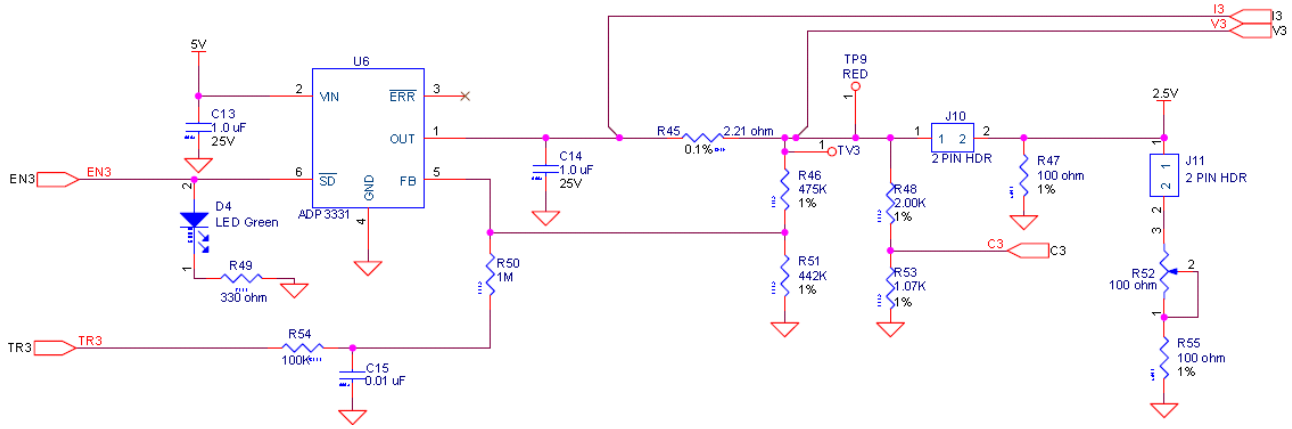
A.2.3 Voltage Regulator V1 = 5 V



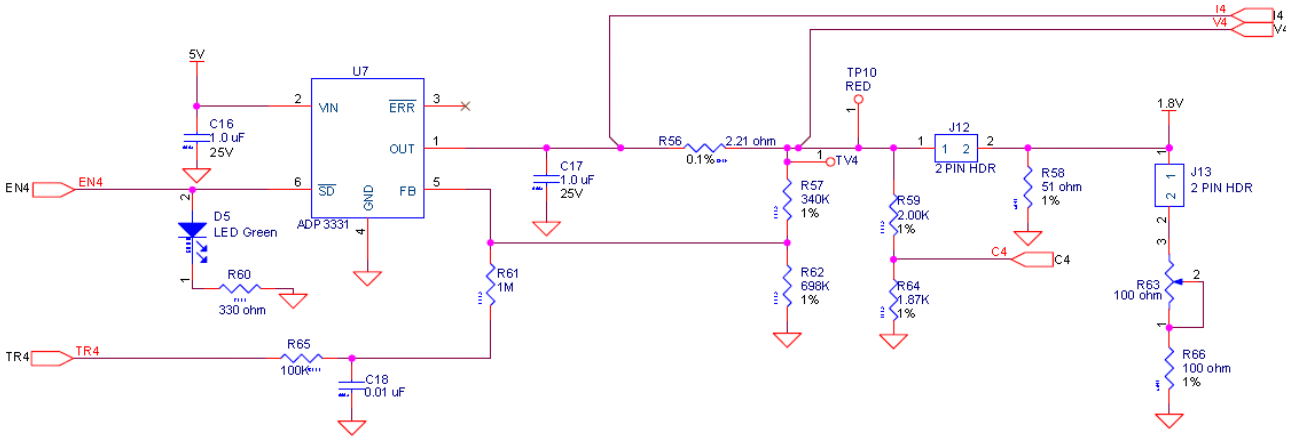
A.2.4 Voltage Regulator V2 = 3.3 V



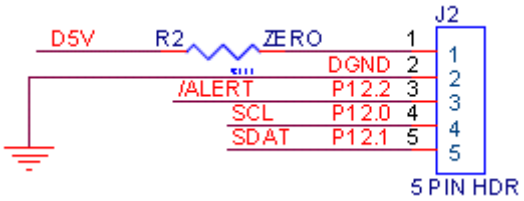
A.2.5 Voltage Regulator V3 = 2.5 V



A.2.6 Voltage Regulator V4 = 1.8 V

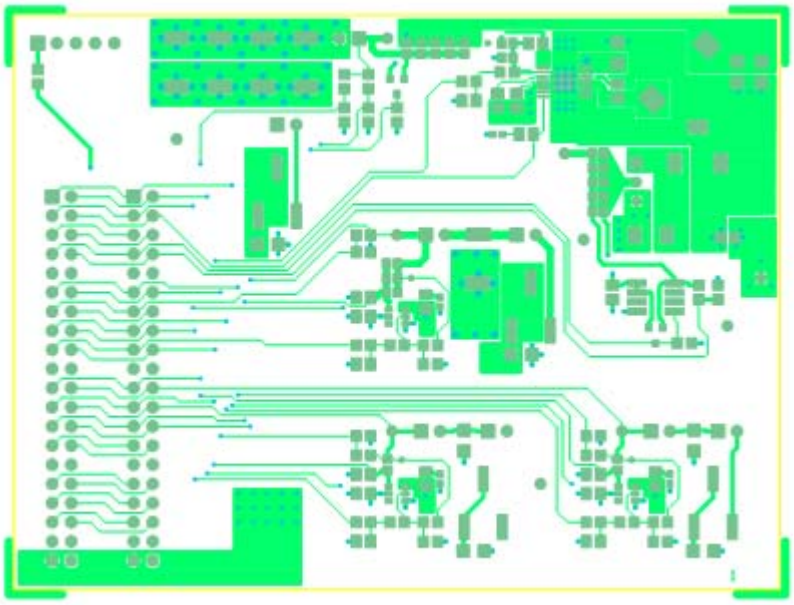


A.2.7 I2C/SMBus/PMBus Interface Connector

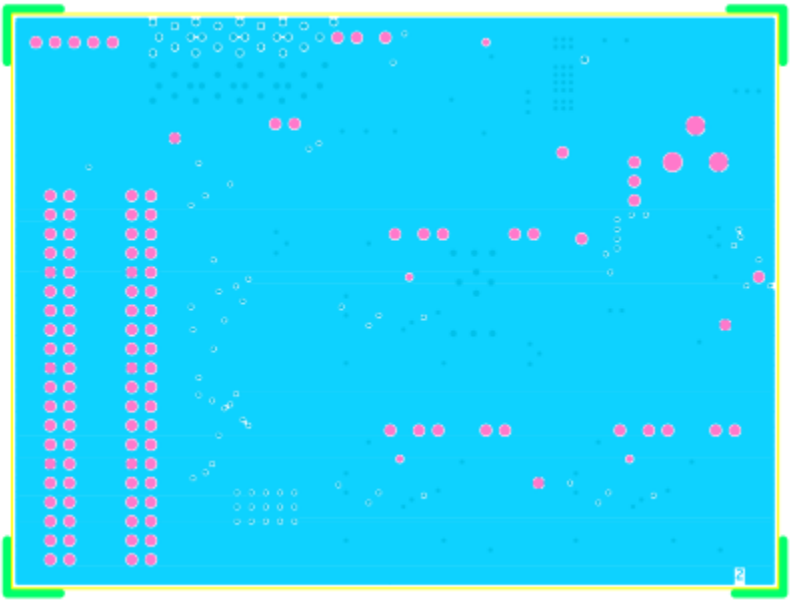


A.3 CY8CKIT-035 Board Layout

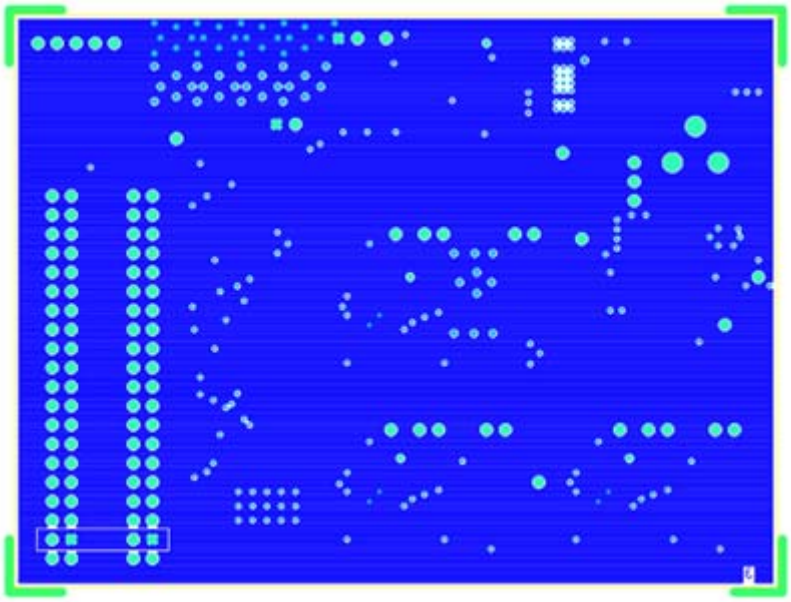
A.3.1 Top layer



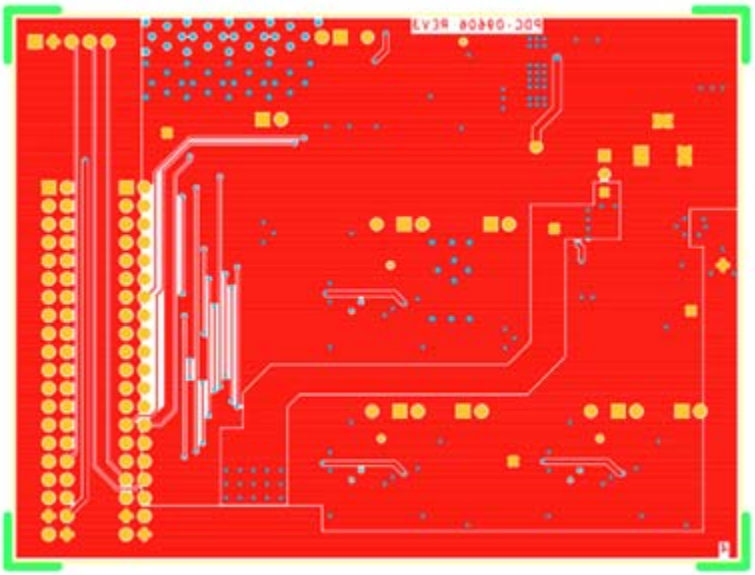
A.3.2 Ground Layer



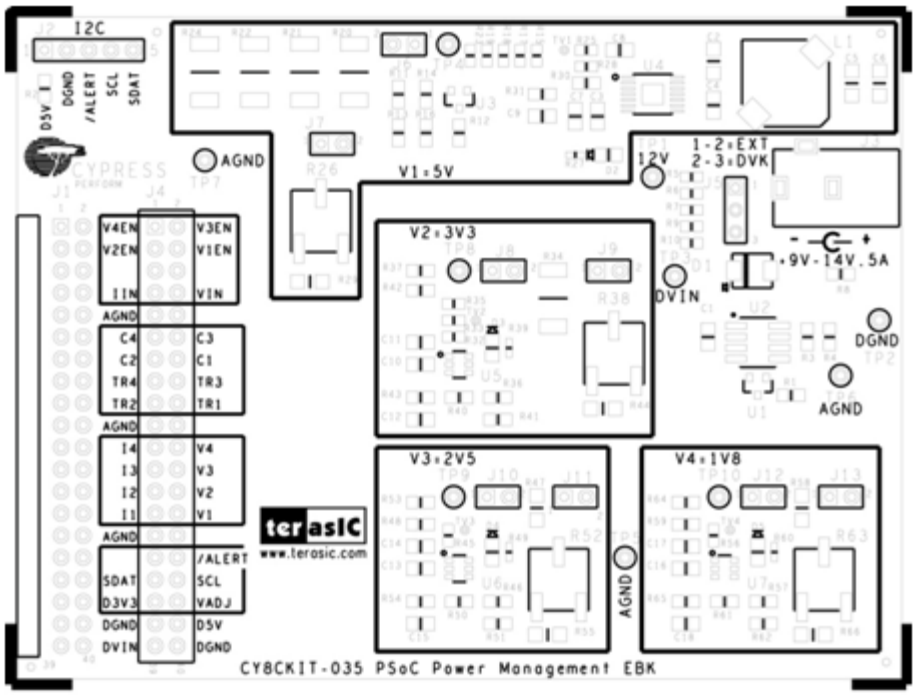
A.3.3 Power Layer



A.3.4 Bottom Layer



A.3.5 Top Silkscreen



PDC-09606 REV ** PRIMARY SILKSCREEN

A.4 CY8CKIT-035 Bill of Materials

Item	Qty.	Designator	Value	Description	Manufacturer	Manufacturer Part No.
1	3	C1,C4,C9	0.1µF, 25V	CAP .1UF 25V CERAMIC X7R 0805	Kemet	C0805C104K3RAC7210
2	3	C2,C5,C6	22µF, 25V	CAP CER 22UF 25V X5R 1206	Murata Electronics North America	GRM31CR61E226KE15L
3	1	C3	3.3nF, 50V	CAP CER 3300PF 50V 5% C0G 0805	Murata Electronics North America	GRM2165C1H332JA01D
4	7	C7,C10,C11,C13 C14,C16,C17	1.0µF, 25V	CAP CER 1.0UF 25V 10% X5R 0805	Murata Electronics North America	GRM216R61E105KA12D
5	1	C8	39pF, 50V	CAP CERM 39PF 5% 50V NP0 0805	AVX Corporation	08055A390JAT2A
6	3	C12,C15,C18	10nF, 50V	CAP CER 10000PF 50V 10% X7R 0805	Murata Electronics North America	GRM216R71H103KA01D
7	1	D1		DIODE SCHOTTKY 2A 20V SMB	Vishay/General Semi-conductor	SS22-E3/52T
8	4	D2,D3,D4,D5		LED GREEN CLEAR 0805 SMD	LITE-ON	LTST-C170GKT
9	1	J1		CONN HEADER R/A DUAL 40POS GOLD	3M	961240-5604-AR
10	1	J2		CONN HEADER 5POS .100 VERT TIN	Molex Inc	22-23-2051
11	1	J3		CONN JACK POWER 2.1mm PCB RA	CUI	PJ-102A
12	1	J5		BERGSTIK II .100" SR STRAIGHT	FCI	68000-403HLF
13	8	J6,J7,J8,J9,J10, J11,J12,J13		CONN HEADER 2 POS .100 VERT TIN	Molex/Waldcom Elec-tronics Corp	22-28-4020
14	1	L1	22µH, 2.2A	COIL PWR CHOKE 22UH 2.2A SMD	Panasonic - ECG	ELL-ATV220M
15	2	R2,R8		RES 0.0 OHM 1/10W 5% 0805 SMD	Panasonic-ECG	ERJ-6GEY0R00V
16	3	R3,R11,R13	51kΩ	RES 51.0K OHM 1/8W 0.1% 0805 SMD	Susumu	RG2012P-513-B-T5
17	1	R4	22kΩ	RES 20.0K OHM 1/8W 0.1% 0805 SMD	Susumu	RG2012P-203-B-T5
18	15	R5,R6,R7,R9, R10,R15,R17, R18,R19,R23, R32,R33, R35,R45,R56	2.21Ω	RES 2.21 OHM 1/16W 0.1% 0603 SMD	Stackpole Electronics Inc	RNCF0603BKC2R21
19	1	R12	1kΩ	RES 1/10W 1K OHM 0.1% 0805	Susumu	RG2012P-102-B-T5
20	4	R14,R37,R48, R59	2kΩ	RES 2.00K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF2001V
21	1	R16	422Ω	RES 422 OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF4220V
22	4	R20,R21,R22, R24	100Ω	RES 100 OHM 2W 1% 2512 SMD	Stackpole Electronics Inc	RHC2512FT100R
23	1	R25	121kΩ	RES 121K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-07121KL
24	4	R26,R38,R52, R63	100Ω	TRIMPOT 100 OHM 6MM SQ SMD	Bourns Inc.	3361P-1-101GLF
25	4	R27,R39,R49, R60	330Ω	RES 330 OHM 1/16W 5% 0402 SMD	Yageo Corporation	RC0402JR-07330RL
26	1	R28	22.1kΩ	RES 22.1K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0722K1L

Item	Qty.	Designator	Value	Description	Manufacturer	Manufacturer Part No.
27	5	R29,R44,R47, R55,R66	100Ω	RES 100 OHM .5W 1% 1206 SMD	Vishay/Dale	CRCW1206100RFKEAHP
28	4	R30,R43,R54, R65	100kΩ	RES 100K OHM 1/8W 5% 0805 SMD	Panasonic - ECG	ERJ-6GEYJ104V
29	1	R31	20kΩ	RES 20K OHM 1/8W 5% 0805 SMD	Panasonic - ECG	ERJ-6GEYJ203V
30	1	R34	33Ω	RES 33 OHM 2W 1% 2512 SMD	Stackpole Electronics Inc	RHC2512FT33R0
31	1	R36	634kΩ	RES 634K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF6343V
32	3	R40,R50,R61	1MΩ	RES 1M OHM 1/10W 5% 0805 SMD	Panasonic - ECG	ERJ-6GEYJ105V
33	1	R41	365kΩ	RES 365K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF3653V
34	1	R42	715Ω	RES 715 OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF7150V
35	1	R46	475kΩ	RES 475K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF4753V
36	1	R51	442kΩ	RES 442K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF4423V
37	1	R53	1.07kΩ	RES 1.07K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF1071V
38	1	R57	340kΩ	RES 340K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF3403V
39	1	R58	51Ω	RES 51.0 OHM 1/4W 1% 1206 SMD	Vishay/Dale	CRCW120651R0FKEA
40	1	R62	698kΩ	RES 698K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF6983V
41	1	R64	1.87kΩ	RES 1.87K OHM 1/8W 1% 0805 SMD	Panasonic - ECG	ERJ-6ENF1871V
42	6	TP1,TP3,TP4, TP8,TP9,TP10		TEST POINT 43 HOLE 65 PLATED RED	Keystone Electronics	5000
43	4	TP2,TP5,TP6, TP7		TEST POINT 43 HOLE 65 PLATED BLACK	Keystone Electronics	5001
44	1	U2		IC AMP CURRENT SENSE 8-SOIC	Maxim Integrated Products	MAX4080TASA+
45	1	U3		HIGH-SIDE CURRENT MONITOR	Zetex	ZXCT1009FTA
46	1	U4		IC CONV STP-DWN SYNC 2A 14HTSSOP	Texas Instruments	TPS54226PWPR
47	3	U5,U6,U7		IC REG LDO ADJ 200MA SOT-23-6	Analog Devices Inc	ADP3331ARTZ-REEL7
48	4	See Assembly Drawing		BUMPER WHITE .500X.23 SQUARE	Richco Plastics Co.	RBS-3R
49	9			SHUNT GOLD W/HAN-DLE, BLACK	Kobiconn	151-8030-E
No Load Components						
50	1	R1	1kΩ	RES 1K 1/10W OHM 0.1% 0805	Stackpole Electronics Inc	RNCF0805BTC1K00
51	1	J4		CONN HEADER VERT DUAL 40POS GOLD	3M	961240-6404-AR
52	1	U1		HIGH-SIDE CURRENT MONITOR	Zetex	ZXCT1009FTA
53	4	TV1,TV2,TV3, TV4		TEST VIA 40 HOLE 20 PLATED	NONE	NA