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Programmable System-on-Chip (PSoC)

General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an ARM® Cortex™-M0+ CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC CY8C4146 FNI-S443 product family is a member of the PSoC 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CapSense) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC CY8C4146 FNI-S443 products will be upward compatible with members of the PSoC 4 platform for new applications and design needs.

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0+ CPU
- Up to 64 KB of flash with Read Accelerator
- Up to 8 KB of SRAM

Programmable Analog

- Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and Comparator modes and ADC input buffering capability. Opamps can operate in Deep Sleep low-power mode.
- 12-bit 1-Msps SAR ADC with differential and single-ended modes, and Channel Sequencer with signal averaging
- Single-slope 10-bit ADC function provided by a capacitance sensing block
- Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- Two low-power comparators that operate in Deep Sleep low-power mode

Programmable Digital

- Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs

Low-Power 1.71-V to 5.5-V Operation

- Deep Sleep mode with operational analog and 2.5-μA digital system current

Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™)

LCD Drive Capability

- LCD segment drive capability on GPIOs

Serial Communication

- Three independent run-time reconfigurable Serial Communication Blocks (SCBs) with re-configurable I²C, SPI, or UART functionality

Timing and Pulse-Width Modulation

- Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

31 Programmable GPIO Pins on the 35-ball WLCSP

- 35-ball WLCSP package
- Any GPIO pin can be CapSense, analog, or digital
- Drive modes, strengths, and slew rates are programmable

PSoC Creator Design Environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API) component for all fixed-function and programmable peripherals

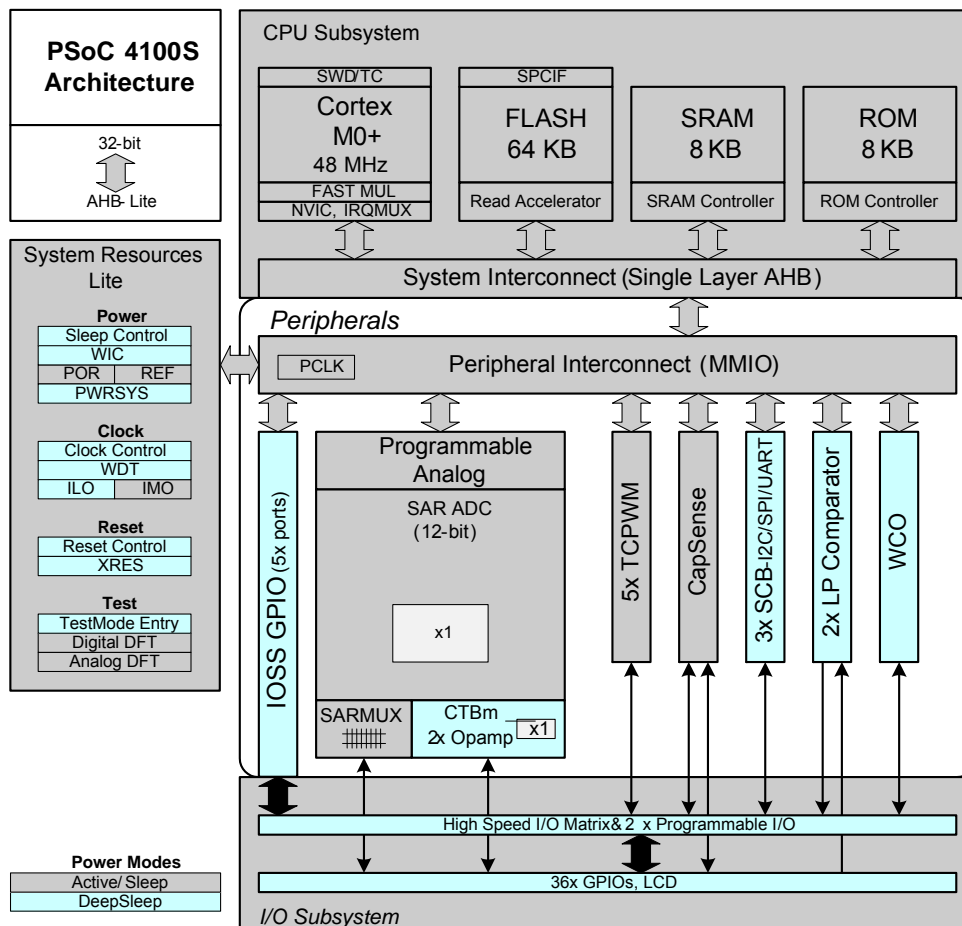
Industry-Standard Tool Compatibility

- After schematic entry, development can be done with ARM-based industry-standard development tools

Contents

Functional Definition	4	Device Level Specifications	12
CPU and Memory Subsystem	4	Analog Peripherals	16
System Resources	4	Digital Peripherals	24
Analog Blocks	5	Memory	27
Fixed Function Digital	5	System Resources	27
GPIO	6	Ordering Information	30
Special Function Peripherals	6	Packaging	31
Pinouts	7	Package Diagram	32
Alternate Pin Functions	8	Acronyms	33
Power	10	Document Conventions	35
Mode 1: 1.8 V to 5.5 V External Supply	10	Units of Measure	35
Mode 2: 1.8 V ±5% External Supply	10	Revision History	36
Development Support	11	Sales, Solutions, and Legal Information	37
Documentation	11	Worldwide Sales and Design Support	37
Online	11	Products	37
Tools	11	PSoC® Solutions	37
Electrical Specifications	12	Cypress Developer Community	37
Absolute Maximum Ratings	12	Technical Support	37

Figure 1. Block Diagram



PSoC CY8C4146 FNI-S443 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC CY8C4146 FNI-S443 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC CY8C4146 FNI-S443 allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC CY8C4146 FNI-S443 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC CY8C4146 FNI-S443 has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC CY8C4146 FNI-S443 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait-state access at 48 MHz.

SRAM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power on page 10](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC CY8C4146 FNI-S443 operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC CY8C4146 FNI-S443 provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

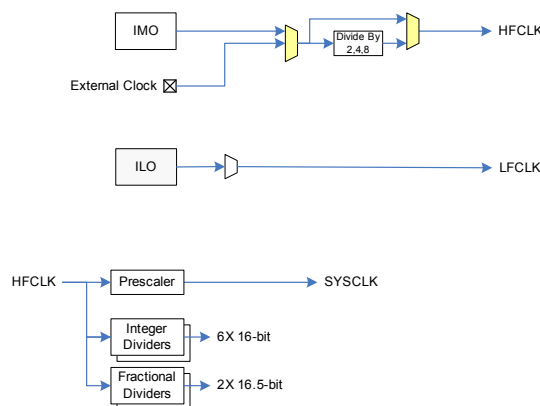
Clock System

The PSoC CY8C4146 FNI-S443 clock system is responsible for providing clocks to all subsystems that require clocks and for

switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC CY8C4146 FNI-S443 consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC CY8C4146 FNI-S443 MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC CY8C4146 FNI-S443; two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is \pm 2%.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC CY8C4146 FNI-S443 clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC CY8C4146 FNI-S443 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

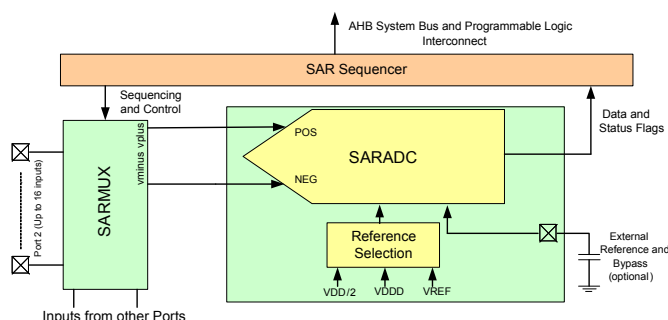
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 3. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

The PSoC CY8C4146 FNI-S443 has two opamps with Comparator modes which allow most common analog functions

to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

The PSoC CY8C4146 FNI-S443 has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

The PSoC CY8C4146 FNI-S443 has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC CY8C4146 FNI-S443 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

The Programmable I/O (PRGIO) will be branded Smart I/O pending legal clearance) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The PRGIO can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC CY8C4146 FNI-S443.

Serial Communication Block (SCB)

The PSoC CY8C4146 FNI-S443 has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI²C that creates a mailbox address range in the memory of the PSoC CY8C4146 FNI-S443 and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC CY8C4146 FNI-S443 is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

The PSoC CY8C4146 FNI-S443 has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC CY8C4146 FNI-S443).

Special Function Peripherals

CapSense

CapSense is supported in the PSoC CY8C4146 FNI-S443 through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

LCD Segment Drive

The PSoC CY8C4146 FNI-S443 has an LCD controller, which can drive up to 4 commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

Pinouts

The following table provides the pin list for PSoC CY8C4146 FNI-S443 for the 35-ball CSP package. All port pins support GPIO.

Table 1. Pin List

35-CSP		35-CSP	
Pin	Name	Pin	Name
C3	P0.0	D5	P1.5
A5	P0.1	D6	P1.6
A4	P0.2	E7	P1.7/VREF
A3	P0.3	D3	P2.2
B3	P0.4	E4	P2.3
A6	P0.5	E5	P2.4
B4	P0.6	E6	P2.5
B5	P0.7	E3	P2.6
B6	XRES	E2	P2.7
A7	VCCD	E1	P3.0
B7	VSS	D2	P3.1
C7	VDD	D1	P3.2
C7	VDD	C1	P3.3
B7	VSS	C2	P3.4
C4	P1.0	B1	P4.0
C5	P1.1	B2	P4.1
C6	P1.2	A2	P4.2
D7	P1.3	A1	P4.3
D4	P1.4		

Descriptions of the Power pins are as follows:

VDDD: Power supply for the chip.

VSSD: Ground pin for the chip.

VCCD: Regulated digital supply. This is an output if the internal regulator is used. If the internal regulator is bypassed (in which case VDDD and VCCD must be shorted together), VCCD must be driven by a 1.8 V $\pm 5\%$ supply.

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

Table 2. WLCSP Balls to Pins Connections

Ball	Port/ Pin	Analog	Alt Function 1	Alt Function 2	Alt Function 3	Deep Sleep 1	Deep Sleep 2	Description
C3	P0.0	lpcomp.in_p[0]	—	—	tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0	Port 0 Pin 0: gpio, lcd, csd, scb0, scb2, comp
A5	P0.1	lpcomp.in_n[0]	—	—	tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0	Port 0 Pin 1: gpio, lcd, csd, scb0, scb2, comp
A4	P0.2	lpcomp.in_p[1]	—	—	—	—	scb[0].spi_select3:0	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
A3	P0.3	lpcomp.in_n[1]	—	—	—	—	scb[2].spi_select0	Port 0 Pin 3: gpio, lcd, csd, scb2, comp
B3	P0.4	wco.wco_in	—	scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1	Port 0 Pin 4: gpio, lcd, csd, scb1, scb2
A6	P0.5	wco.wco_out	—	scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1	Port 0 Pin 5: gpio, lcd, csd, scb1, scb2
B4	P0.6	—	srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1	—	scb[1].spi_clk:1	Port 0 Pin 6: gpio, lcd, csd, scb1, scb2, ext_clk
B5	P0.7	—	tcpwm.line[0]:2	scb[1].uart_rts:0	—	—	scb[1].spi_select0:1	Port 0 Pin 7: gpio, lcd, csd, scb1, tcpwm
B6	XRE S	—	—	—	—	—	—	Chip reset, active low
A7	VCC D	—	—	—	—	—	—	Regulated supply, connect to 1µF cap or 1.8V
B7	VSS	—	—	—	—	—	—	Ground
C7	VDD	—	—	—	—	—	—	Supply, 1.71 - 5.5V
C4	P1.0	ctb0_oa0+	tcpwm.line[2]:1	scb[0].uart_rx:1	—	scb[0].i2c_scl:0	scb[0].spi_mosi:1	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm, scb0
C5	P1.1	ctb0_oa0-	tcpwm.line_comp[2]:1	scb[0].uart_tx:1	—	scb[0].i2c_sda:0	scb[0].spi_miso:1	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm, scb0
C6	P1.2	ctb0_oa0_out	tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm, scb0, scb2
D7	P1.3	ctb0_oa1_out	tcpwm.line_comp[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm, scb0
D4	P1.4	ctb0_oa1-	—	—	—	—	scb[0].spi_select1:1	Port 1 Pin 4: gpio, lcd, csd, ctb, scb0
D5	P1.5	ctb0_oa1+	—	—	—	—	scb[0].spi_select2:1	Port 1 Pin 5: gpio, lcd, csd, ctb, scb0

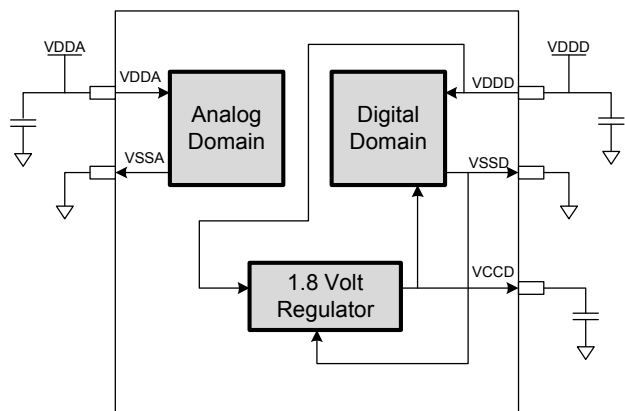
Table 2. WLCSP Balls to Pins Connections *(continued)*

Ball	Port/ Pin	Analog	Alt Function 1	Alt Function 2	Alt Function 3	Deep Sleep 1	Deep Sleep 2	Description
D6	P1.6	ctb0_oa0+	—	—	—	—	scb[0].spi_select3: 1	Port 1 Pin 6: gpio, lcd, csd, scb0
E7	P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1	—	—	—	—	scb[2].spi_clk	Port 1 Pin 7: gpio, lcd, csd, ext_ref, scb2
D3	P2.2	sarmux[2]	—	—	—	—	scb[1].spi_clk:2	Port 2 Pin 2: gpio, lcd, csd, sarmux, scb1
E4	P2.3	sarmux[3]	—	—	—	—	scb[1].spi_select0: 2	Port 2 Pin 3: gpio, lcd, csd, sarmux, scb1
E5	P2.4	sarmux[4]	tcpwm.line[0]:1	—	—	—	scb[1].spi_select1: 1	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm, scb1
E6	P2.5	sarmux[5]	tcpwm.line_compl[0]:1	—	—	—	scb[1].spi_select2: 1	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm, scb1
E3	P2.6	sarmux[6]	tcpwm.line[1]:1	—	—	—	scb[1].spi_select3: 1	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm, scb1
E2	P2.7	sarmux[7]	tcpwm.line_compl[1]:1	—	—	lpcomp.comp[0]:1	scb[2].spi_mosi	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm, scb2
E1	P3.0	—	tcpwm.line[0]:0	scb[1].uart_rx:1	—	scb[1].i2c_scl:2	scb[1].spi_mosi:0	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
D2	P3.1	—	tcpwm.line_compl[0]:0	scb[1].uart_tx:1	—	scb[1].i2c_sda:2	scb[1].spi_miso:0	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
D1	P3.2	—	tcpwm.line[1]:0	scb[1].uart_cts:1	—	cpuss.swd_data	scb[1].spi_clk:0	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
C1	P3.3	—	tcpwm.line_compl[1]:0	scb[1].uart_rts:1	—	cpuss.swd_clk	scb[1].spi_select0: 0	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
C2	P3.4	—	tcpwm.line[2]:0	—	tcpwm.tr_in[6]	—	scb[1].spi_select1: 0	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
B1	P4.0	csd.vref_ext	—	scb[0].uart_rx:0	—	scb[0].i2c_scl:1	scb[0].spi_mosi:0	Port 4 Pin 0: gpio, lcd, csd, scb0
B2	P4.1	csd.cshieldpads	—	scb[0].uart_tx:0	—	scb[0].i2c_sda:1	scb[0].spi_miso:0	Port 4 Pin 1: gpio, lcd, csd, scb0
A2	P4.2	csd.cmodpad	—	scb[0].uart_cts:0	—	lpcomp.comp[0]:0	scb[0].spi_clk:0	Port 4 Pin 2: gpio, lcd, csd, scb0
A1	P4.3	csd.csh_tank	—	scb[0].uart_rts:0	—	lpcomp.comp[1]:0	scb[0].spi_select0: 0	Port 4 Pin 3: gpio, lcd, csd, scb0

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 4. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is 1.8 V \pm 5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC CY8C4146 FNI-S443 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC CY8C4146 FNI-S443 supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 μ F; X5R ceramic or better) and must not be connected to anything else.

Mode 2: 1.8 V \pm 5% External Supply

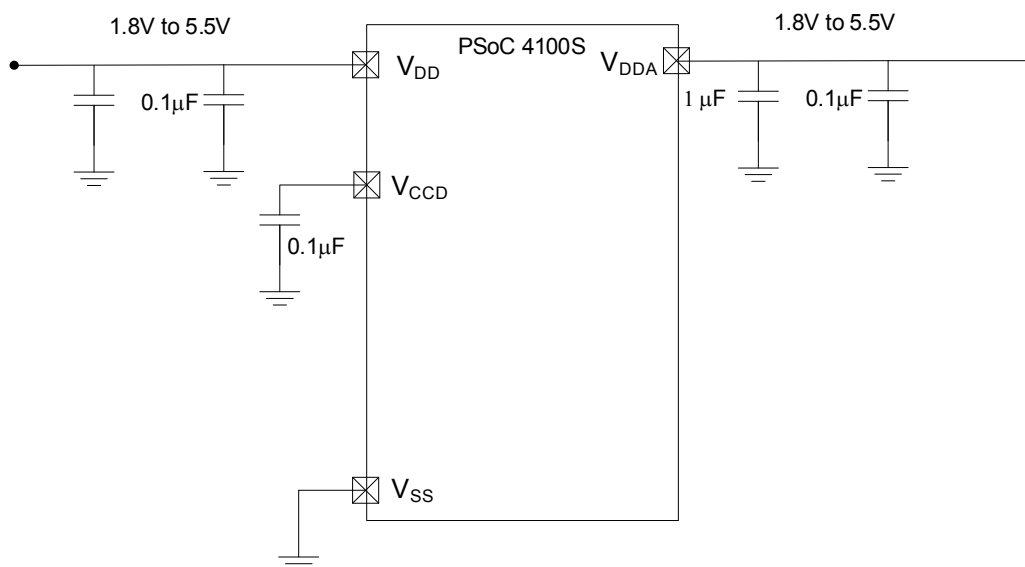
In this mode, the PSoC CY8C4146 FNI-S443 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μ F range, in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 5. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active

Power supply bypass connections example



Development Support

The PSoC CY8C4146 FNI-S443 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC CY8C4146 FNI-S443 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC CY8C4146 FNI-S443 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V _{DDD_ABS}	Digital supply relative to V _{SS}	−0.5	−	6	V	−
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	−0.5	−	1.95		−
SID3	V _{GPIO_ABS}	GPIO voltage	−0.5	−	V _{DD} +0.5		−
SID4	I _{GPIO_ABS}	Maximum current per GPIO	−25	−	25	mA	−
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	−0.5	−	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	−	−	V	−
BID45	ESD_CDM	Electrostatic discharge charged device model	500	−	−		−
BID46	LU	Pin current for latch-up	−140	−	140	mA	−

Device Level Specifications

All specifications are valid for −40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 4. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V _{DD}	Power supply input voltage	1.8	−	5.5	V	Internally regulated supply
SID255	V _{DD}	Power supply input voltage (V _{CCD} = V _{DDD} = V _{DDA})	1.71	−	1.89		Internally unregulated supply
SID54	V _{CCD}	Output voltage (for core logic)	−	1.8	−		−
SID55	C _{EFC}	External regulator voltage bypass	−	0.1	−	μF	X5R ceramic or better
SID56	C _{EXC}	Power supply bypass capacitor	−	1	−		X5R ceramic or better

Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25 °C.

SID10	I _{DD5}	Execute from flash; CPU at 6 MHz	−	1.8	2.7	mA	Max is at 85 °C and 5.5 V
SID16	I _{DD8}	Execute from flash; CPU at 24 MHz	−	3.0	4.75		Max is at 85 °C and 5.5 V
SID19	I _{DD11}	Execute from flash; CPU at 48 MHz	−	5.4	6.85		Max is at 85 °C and 5.5 V

Note

- Usage above the absolute maximum conditions listed in Table 3 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 4. DC Specifications (continued)

Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	IDD17	I ² C wakeup WDT, and Comparators on	–	1.7	2.2	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID25	IDD20	I ² C wakeup, WDT, and Comparators on.	–	2.2	2.5		12 MHZ. Max is at 85 °C and 5.5 V.
Sleep Mode, VDDD = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	IDD23	I ² C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHZ. Max is at 85 °C and 5.5 V.
SID28A	IDD23A	I ² C wakeup, WDT, and Comparators on	–	1	1.2	mA	12 MHZ. Max is at 85 °C and 5.5 V.
Deep Sleep Mode, VDD = 1.8 V to 3.6 V (Regulator on)							
SID31	IDD26	I ² C wakeup and WDT on	–	2.5	75	μA	Max is at 3.6 V and 85 °C.
Deep Sleep Mode, VDD = 3.6 V to 5.5 V (Regulator on)							
SID34	IDD29	I ² C wakeup and WDT on	–	2.5	75	μA	Max is at 5.5 V and 85 °C.
Deep Sleep Mode, VDD = VCCD = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	IDD32	I ² C wakeup and WDT on	–	2.5	75	μA	Max is at 1.89 V and 85 °C.
XRES Current							
SID307	IDD_XR	Supply current while XRES asserted	–	2	5	mA	–

Table 5. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49	T _{SLEEP}	Wakeup from Sleep mode	–	0	–	μs	
SID50 ^[2]	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	35	–		

Note

2. Guaranteed by characterization.

GPIO

Table 6. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		CMOS Input
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} < 2.7$ V	$0.7 \times V_{DD}$	–	–		–
SID242	V_{IL}	LVTTL input, $V_{DD} < 2.7$ V	–	–	$0.3 \times V_{DD}$		–
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} \geq 2.7$ V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, $V_{DD} \geq 2.7$ V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	$V_{DD} - 0.6$	–	–		$I_{OH} = 4$ mA at 3 V V_{DD}
SID60	V_{OH}	Output voltage high level	$V_{DD} - 0.5$	–	–		$I_{OH} = 1$ mA at 1.8 V V_{DD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 4$ mA at 1.8 V V_{DD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 10$ mA at 3 V V_{DD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		$I_{OL} = 3$ mA at 3 V V_{DD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DD} = 3.0$ V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67 ^[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DD} \geq 2.7$ V
SID68 ^[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–		$V_{DD} < 4.5$ V
SID68A ^[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		$V_{DD} > 4.5$ V
SID69 ^[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	–
SID69A ^[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 7. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DD} , Load = 25 pF

Notes

3. V_{IH} must not exceed $V_{DD} + 0.2$ V.
4. Guaranteed by characterization.

Table 7. GPIO AC Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T _{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V _{DD} , Cload = 25 pF
SID74	F _{GPIOOUT1}	GPIO F _{OUT} ; 3.3 V ≤ V _{DD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F _{GPIOOUT2}	GPIO F _{OUT} ; 1.71 V ≤ V _{DD} ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	F _{GPIOOUT3}	GPIO F _{OUT} ; 3.3 V ≤ V _{DD} ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	F _{GPIOOUT4}	GPIO F _{OUT} ; 1.71 V ≤ V _{DD} ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F _{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V _{DD} ≤ 5.5 V	–	–	48		90/10% V _{IO}

XRES

Table 8. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V _{IH}	Input voltage high threshold	0.7 × V _{DD}	–	–	V	CMOS Input
SID78	V _{IL}	Input voltage low threshold	–	–	0.3 × V _{DD}		
SID79	R _{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID80	C _{IN}	Input capacitance	–	–	7	pF	–
SID81 ^[5]	V _{HYSXRES}	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V _{DD} > 4.5 V
SID82	I _{DIODE}	Current through protection diode to V _{DD} /V _{SS}	–	–	100	μA	

Table 9. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 ^[5]	T _{RESETWIDTH}	Reset pulse width	1	–	–	μs	–
BID194 ^[5]	T _{RESETWAKE}	Wake-up time from reset release	–	–	2.2	ms	–

Note

5. Guaranteed by characterization.

Analog Peripherals

Table 10. CTBm Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I _{DD}	Opamp block current, External load					
SID269	I _{DD_HI}	power=hi	–	1100	1850	μA	–
SID270	I _{DD_MED}	power=med	–	550	950		–
SID271	I _{DD_LOW}	power=lo	–	150	350		–
	G _{BW}	Load = 20 pF, 0.1 mA V _{DDA} = 2.7 V					
SID272	G _{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to V _{DDA} -0.2 V
SID273	G _{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to V _{DDA} -0.2 V
SID274	G _{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to V _{DDA} -0.2 V
	I _{OUT_MAX}	V _{DDA} = 2.7 V, 500 mV from rail					
SID275	I _{OUT_MAX_HI}	power=hi	10	–	–	mA	Output is 0.5 V V _{DDA} -0.5 V
SID276	I _{OUT_MAX_MID}	power=mid	10	–	–		Output is 0.5 V V _{DDA} -0.5 V
SID277	I _{OUT_MAX_LO}	power=lo	–	5	–		Output is 0.5 V V _{DDA} -0.5 V
	I _{OUT}	V _{DDA} = 1.71 V, 500 mV from rail					
SID278	I _{OUT_MAX_HI}	power=hi	4	–	–	mA	Output is 0.5 V V _{DDA} -0.5 V
SID279	I _{OUT_MAX_MID}	power=mid	4	–	–		Output is 0.5 V V _{DDA} -0.5 V
SID280	I _{OUT_MAX_LO}	power=lo	–	2	–		Output is 0.5 V V _{DDA} -0.5 V
	I _{DD_Int}	Opamp block current Internal Load					
SID269_I	I _{DD_HI_Int}	power=hi	–	1500	1700	μA	–
SID270_I	I _{DD_MED_Int}	power=med	–	700	900		–
		General opamp specs for both internal and external modes					
SID281	V _{IN}	Charge-pump on, V _{DDA} = 2.7 V	–0.05	–	V _{DDA} -0.2	V	–
SID282	V _{CM}	Charge-pump on, V _{DDA} = 2.7 V	–0.05	–	V _{DDA} -0.2		–

Table 10. CTBm Opamp Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	V _{OUT}	V _{DDA} = 2.7 V					
SID283	V _{OUT_1}	power=hi, Iload=10 mA	0.5	–	V _{DDA} -0.5	V	–
SID284	V _{OUT_2}	power=hi, Iload=1 mA	0.2	–	V _{DDA} -0.2		–
SID285	V _{OUT_3}	power=med, Iload=1 mA	0.2	–	V _{DDA} -0.2		–
SID286	V _{OUT_4}	power=lo, Iload=0.1 mA	0.2	–	V _{DDA} -0.2		–
SID288	V _{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V _{DDA} -0.2 V
SID288A	V _{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V _{DDA} -0.2 V
SID288B	V _{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V _{DDA} -0.2 V
SID290	V _{OS_DR_TR}	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID290A	V _{OS_DR_TR}	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID290B	V _{OS_DR_TR}	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V _{DDA} -0.2 V, Output is 0.2 V to V _{DDA} -0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V _{DDD} = 3.6 V, high-power mode, input is 0.2 V to V _{DDA} -0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power=Hi	–	72	–	nV/rtHz	3
SID295	VN3	Input-referred, 10 kHz, power=Hi	–	28	–		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID296	VN4	Input-referred, 100 kHz, power=Hi	–	15	–		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID297	C _{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V _{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T _{OP_WAKE}	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	Guaranteed by Design
	COMP_MODE	Comparator mode; 50 mV drive, T _{rise} =T _{fall} (approx.)					

Table 10. CTBm Opamp Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to $V_{DDA}-0.2$ V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	μs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	I _{DD_HI_M1}	Mode 1, High current	–	1400	–	μA	25 °C
SID_DS_2	I _{DD_MED_M1}	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	I _{DD_LOW_M1}	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	I _{DD_HI_M2}	Mode 2, High current	–	120	–		25 °C
SID_DS_5	I _{DD_MED_M2}	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	I _{DD_LOW_M2}	Mode 2, Low current	–	15	–		25 °C
SID_DS_7	G _{BW_HI_M1}	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_8	G _{BW_MED_M1}	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_9	G _{BW_LOW_M1}	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_10	G _{BW_HI_M2}	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_11	G _{BW_MED_M2}	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_12	G _{BW_Low_M2}	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V

Table 10. CTBm Opamp Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_13	V _{OS_HI_M1}	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_14	V _{OS_MED_M1}	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_15	V _{OS_LOW_M2}	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_16	V _{OS_HI_M2}	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to V _{DDA} -0.2 V
SID_DS_17	V _{OS_MED_M2}	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_18	V _{OS_LOW_M2}	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to V _{DDA} -0.2 V
SID_DS_19	I _{OUT_HI_M1}	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_20	I _{OUT_MED_M1}	Mode 1, Medium current	–	10	–		Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_21	I _{OUT_LOW_M1}	Mode 1, Low current	–	4	–		Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_22	I _{OUT_HI_M2}	Mode 2, High current	–	1	–		
SID_DS_23	I _{OU_MED_M2}	Mode 2, Medium current	–	1	–		
SID_DS_24	I _{OU_LOW_M2}	Mode 2, Low current	–	0.5	–		

Table 11. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID84	V _{OFFSET1}	Input offset voltage, Factory trim	–	–	±10	mV	
SID85	V _{OFFSET2}	Input offset voltage, Custom trim	–	–	±4		
SID86	V _{HYST}	Hysteresis when enabled	–	10	35		
SID87	V _{ICM1}	Input common mode voltage in normal mode	0	–	V _{DDD} -0.1	V	Modes 1 and 2
SID247	V _{ICM2}	Input common mode voltage in low power mode	0	–	V _{DDD}		
SID247A	V _{ICM3}	Input common mode voltage in ultra low power mode	0	–	V _{DDD} -1.15		V _{DDD} ≥ 2.2 V at –40 °C
SID88	C _{MRR}	Common mode rejection ratio	50	–	–	dB	V _{DDD} ≥ 2.7V
SID88A	C _{MRR}	Common mode rejection ratio	42	–	–		V _{DDD} ≤ 2.7V
SID89	I _{CMP1}	Block current, normal mode	–	–	400	μA	
SID248	I _{CMP2}	Block current, low power mode	–	–	100		
SID259	I _{CMP3}	Block current in ultra low-power mode	–	–	6		V _{DDD} ≥ 2.2 V at –40 °C
SID90	Z _{CMP}	DC Input impedance of comparator	35	–	–	MΩ	

Note

6. Guaranteed by characterization.

Table 12. Comparator AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	μs	$V_{DD} \geq 2.2 \text{ V}$ at -40°C

Table 13. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID93	TSSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 14. SAR Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SAR ADC DC Specifications							
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	
SID102	A_VIND	Input voltage range - differential[V_{SS}	–	V_{DDA}	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	1.2	V	
SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	$F_{IN} = 10 \text{ kHz}$
SID110	A_BW	Input bandwidth without aliasing	–	–	$A_{\text{samp}}/2$	kHz	
SID111	A_INL	Integral non linearity. $V_{DD} = 1.71$ to 5.5 , 1 Msps	–1.7	–	2	LSB	$V_{REF} = 1$ to V_{DD}
SID111A	A_INL	Integral non linearity. $V_{DD} = 1.71$ to 3.6 , 1 Msps	–1.5	–	1.7	LSB	$V_{REF} = 1.71$ to V_{DD}
SID111B	A_INL	Integral non linearity. $V_{DD} = 1.71$ to 5.5 , 500 kps	–1.5	–	1.7	LSB	$V_{REF} = 1$ to V_{DD}
SID112	A_DNL	Differential non linearity. $V_{DD} = 1.71$ to 5.5 , 1 Msps	–1	–	2.2	LSB	$V_{REF} = 1$ to V_{DD}

Table 14. SAR Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID112A	A_DNL	Differential non linearity. $V_{DD} = 1.71$ to 3.6 , 1 Msps	-1	—	2	LSB	$V_{REF} = 1.71$ to V_{DD}
SID112B	A_DNL	Differential non linearity. $V_{DD} = 1.71$ to 5.5 , 500 ksps	-1	—	2.2	LSB	$V_{REF} = 1$ to V_{DD}
SID113	A_THD	Total harmonic distortion	—	—	-65	dB	$F_{in} = 10$ kHz
SID261	FSARINTREF	SAR operating speed without external ref. bypass	—	—	100	ksps	12-bit resolution

Table 15. CSD and IDAC Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	$V_{DD} > 2\text{ V}$ (with ripple), 25 °C T_A , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	$V_{DD} > 1.75\text{ V}$ (with ripple), 25 °C T_A , Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Total block current with comparators and reference
SID.CSD#15	VREF	Voltage reference for CSD and Comparator	0.6	1.2	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.6$ or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		$V_{DDA} - 0.6$	V	$V_{DDA} - 0.6$ or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	µA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.6$ or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5 LSB for $V_{DDA} < 2\text{ V}$
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5 LSB for $V_{DDA} < 2\text{ V}$
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.2-pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4	–	6	µA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	30	–	47	µA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	262	–	368	µA	LSB = 2.4-µA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	11.5	µA	LSB = 37.5-nA typ. 2X output stage
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	65	–	90	µA	LSB = 300-nA typ. 2X output stage
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	522	–	730	µA	LSB = 2.4-µA typ. 2X output stage
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4	–	6	µA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	30	–	45	µA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	260	–	360	µA	LSB = 2.4-µA typ.

Table 15. CSD and IDAC Specifications (continued)

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	11.5	µA	LSB = 37.5-nA typ. 2X output stage
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	65	–	90	µA	LSB = 300-nA typ. 2X output stage
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	520	–	730	µA	LSB = 2.4-µA typ.2X output stage
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	12	µA	LSB = 37.5-nA typ.
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	60	–	94	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	524	–	736	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	10	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	10	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	10	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 16. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±0.1	%	
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	
SIDA100	A_ISAR	Current consumption	–	–	1	mA	
SIDA101	A_VINS	Input voltage range - single ended	VSSA	–	VDDA	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = $F_{clk}/(2^{(N+2)})$. Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.

Table 16. 10-bit CapSense ADC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = $F_{hclk}/(2^{(N+2)})$. Clock frequency = 48 MHz.	–	–	85.3	μs	Does not include acquisition time. Equivalent to 11.6 ksp/s including acquisition time.
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksp/s	–	–	2	LSB	VREF = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksp/s	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 17. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[7]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–		Minimum pulse width between Quadrature phase inputs

²C

Table 18. Fixed I²C DC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	–	1.4		

Table 19. Fixed I²C AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Msp/s	–

Notes

7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
8. Guaranteed by characterization.

Table 20. SPI DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbits/sec	–	–	360	μA	–
SID164	ISPI2	Block current consumption at 4 Mbits/sec	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbits/sec	–	–	600		–

Table 21. SPI AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	SID166
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Scklock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Scklock driving edge	–	–	42 + 3*Tcpu		T _{CPU} = 1/F _{CPU}
SID171A	TDSO_EXT	MISO Valid after Scklock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

Table 22. UART DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I _{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	μA	–
SID161	I _{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	μA	–

Table 23. UART AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F _{UART}	Bit rate	–	–	1	Mbps	–

Table 24. LCD Direct Drive DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current $V_{bias} = 5\text{ V}$	–	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	I_{LCDOP2}	LCD system operating current $V_{bias} = 3.3\text{ V}$	–	2	–		32 × 4 segments. 50 Hz. 25 °C 4 segments. 50 Hz. 25 °C

Table 25. LCD Direct Drive AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note

9. Guaranteed by characterization.

Memory

Table 26. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 27. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE} ^[10]	Row erase time	–	–	13		–
SID176	T _{ROWPROGRAM} ^[10]	Row program time after erase	–	–	7		–
SID178	T _{BULKERASE} ^[10]	Bulk erase time (64 KB)	–	–	35		–
SID180 ^[11]	T _{DEVPROG} ^[10]	Total device program time	–	–	7	Seconds	–
SID181 ^[11]	F _{END}	Flash endurance	100 K	–	–	Cycles	–
SID182 ^[11]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	Years	–
SID182A ^[11]	–	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 28. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[11]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	–
SID186 ^[11]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4		–

Table 29. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[11]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 ^[11]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

11. Guaranteed by characterization.

SWD Interface

Table 30. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7		SWDCLK \leq 1/3 CPU clock frequency
SID215 ^[12]	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	$0.25 \cdot T$	–	–	ns	–
SID216 ^[12]	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	$0.25 \cdot T$	–	–		–
SID217 ^[12]	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	$0.5 \cdot T$		–
SID217A ^[12]	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–		–

Internal Main Oscillator

Table 31. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	–
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	–

Table 32. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	–
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 33. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 ^[12]	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	–

Table 34. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 ^[12]	T _{STARTILO1}	ILO startup time	–	–	2	ms	–
SID236 ^[12]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	–
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	–

Note

12. Guaranteed by characterization.

Table 35. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	μW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	
SID406	IWCO2	Operating Current (low power mode)	–	–	1	uA	

Table 36. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[13]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306 ^[13]	ExtClkDuty	Duty cycle; measured at V _{DD/2}	45	–	55	%	–

Table 37. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[13]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	–

Table 38. PRGIO Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max. delay added by PRGIO in bypass mode	–	–	1.6	ns	PRGIO will be branded Smart I/O pending legal clearance

Note

13. Guaranteed by characterization.

Ordering Information

The marketing part numbers for the PSoC CY8C4146 FNI-S443 family are listed in the following table.

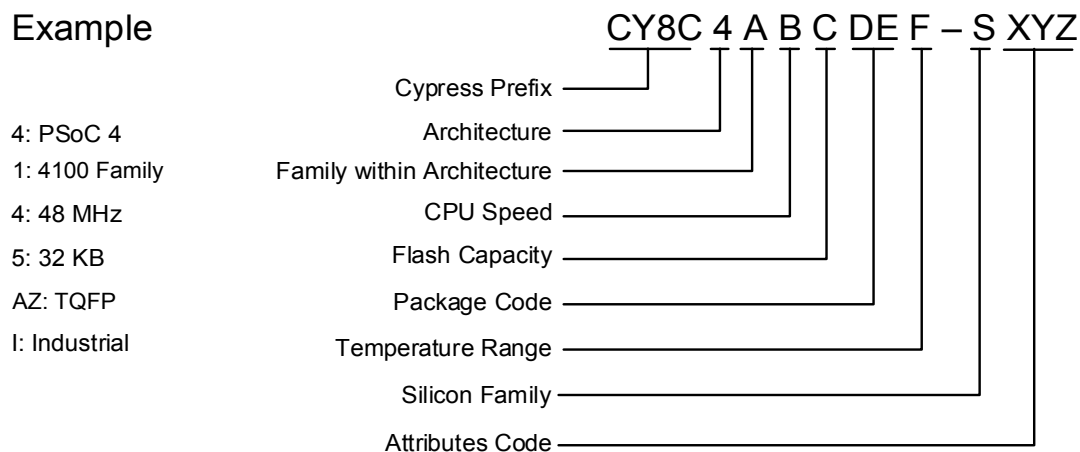
Category	MPN	Features												Package
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Op-amp (CTBm)	CSD	12-bit SAR ADC	ADC Sample Rate	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	35-WLCSP (PSoC 4A Frame)
4146	CY8C4146FNI-S443	48	64	8	2	1	1	1Mpsps	2	5	3	16	31	X

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8mm pitch)
		AZ	TQFP (0.5mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	N/A	PSoC 4A, PSoC 4A-S2
		M	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

Example



Packaging

The PSoC CY8C4146 FNI-S443 will be offered in a 35-ball WLCSP package.

Package dimensions and Cypress drawing numbers are in the following table.

Table 39. Package List

Spec ID#	Package	Description	Package Dwg
BID34G	35-Ball WLCSP	3.2 × 2.1 × 0.55 mm height with 0.4-mm pitch	001-93741

Table 40. Package Thermal Characteristics

Parameter	Description	Package	Min	Typ	Max	Units
T _A	Operating Ambient temperature		−40	25	85	°C
T _J	Operating junction temperature		−40	—	100	°C
T _{JA}	Package θ_{JA}	35-Ball WLCSP	—	28.0	—	°C/Watt
T _{JC}	Package θ_{JC}	35-Ball WLCSP	—	0.4	—	°C/Watt

Table 41. Solder Reflow Peak Temperature

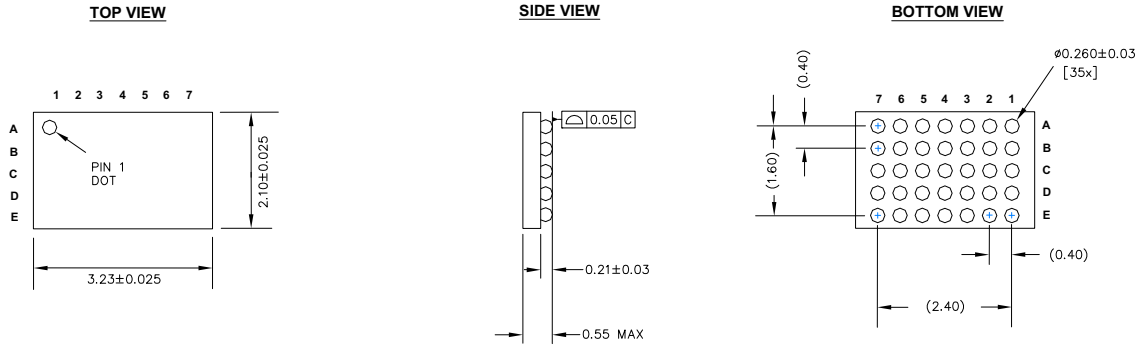
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
35-Ball WLCSP	260 °C	30 seconds

Table 42. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
35-Ball WLCSP	MSL 1

Package Diagram

Figure 6. 35-Ball WLCSP Dimensions



NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 **

Acronyms

Table 43. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 43. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 43. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 43. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 44. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 4: PSoC CY8C4146 FNI -S443 Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-10507				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*B	5314870	WKA	06/30/2016	Release to web.
*C	5561833	WKA	12/23/2016	Updated Figure 3 . Updated DC Specifications . Updated SID95 max value.

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