

### General Physical Specification

For product parameters and availability, refer to the CY7C60123 product datasheets available on the Cypress Semiconductor web site (<http://www.cypress.com/>).

**Table 1. CY7C60123 Die Physical Specification**

<b>Die Technology:</b>	0.35 $\mu\text{m}$ cmos	<b>Wafer Diameter [mm]:</b>	203.2
<b>Metal I:</b>	AlCu 0.6 $\mu\text{m}$	<b>Die Size [<math>\mu\text{m}</math>]:</b>	1722.66 x 2683.14
<b>Metal II:</b>	AlCu 0.8 $\mu\text{m}$	<b>Step Size [<math>\mu\text{m}</math>]:</b>	1808 x 2749
<b>Metal III:</b>	NA	<b>Scribe Size [<math>\mu\text{m}</math>]:</b>	85.34 x 65.86
<b>Die Passivation:</b>	0.6 $\mu\text{m}$ SiO <sub>2</sub> /0.6 $\mu\text{m}$ Si <sub>3</sub> N <sub>4</sub>	<b>Pad Count:</b>	47
<b>Substrate Connection Req.:</b>	Ground	<b>Pad Size [<math>\mu\text{m}</math>]:</b>	69.85 x 69.85

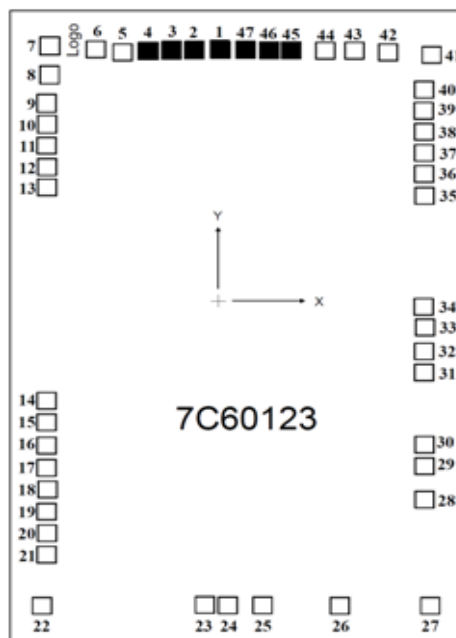
### Product Thickness Guide

**Table 2. Thickness Guide for CY7C60123**

Code	Description	Min	Nom	Max	Unit
X14	Die (14 Mils)	342.5	355	367.5	$\mu\text{m}$
3XWC	Wafer (29 Mils)	710	725	740	$\mu\text{m}$

### Bond Pads

**Figure 1. 7C60123 Bond Pad Locations <sup>[1]</sup>**



**Note**  
1. The bond pad diagram gives the approximate location of the pads. The bond pad co-ordinates table gives the accurate location of the pads on the following page.

**Table 3. Bond Pad Coordinates and Signal Descriptions**

Pad Number <sup>[2]</sup>	Pad Name	Co-ordinates		Description
		X (μm)	Y (μm)	
1	NC	-66.234	1220.457	No Connect
2	NC	-170.436	1220.457	No Connect
3	NC	-264.012	1220.457	No Connect
4	NC	-355.95	1214.64	No Connect
5	VDD1	-455.784	1211.469	Power
6	P41	-565.446	1220.457	GPIO port 4 – configured as a group (nibble)
7	P40	-749.448	1236.9	
8	P27	-749.448	1109.934	GPIO port 2 – configured as a group (byte)
9	P26	-762.678	987.294	
10	P25	-762.678	894.39	
11	P24	-762.678	801.486	
12	P23	-762.678	708.582	
13	P22	-762.678	615.678	
14	P21	-762.678	-315.945	
15	P20	-762.678	-408.849	
16	P07	-762.678	-513.933	GPIO port 0 bit 7 – Configured individually
17	P06_TIO1	-762.678	-606.837	GPIO port 0 bit 6 – Configured individually Alternate function timer capture inputs or timer output TIO1.
18	P05_TIO0	-762.678	-699.741	GPIO port 0 bit 5 – Configured individually Alternate function timer capture inputs or timer output TIO0.
19	P04_INT2	-762.678	-802.053	GPIO port 0 bit 4 – Configured individually Optional rising edge interrupt INT2.
20	P03_INT1	-762.678	-894.957	GPIO port 0 bit 3 – Configured individually Optional rising edge interrupt INT1.
21	P02_INT0	-762.678	-987.861	GPIO port 0 bit 2 – Configured individually Optional rising edge interrupt INT0.
22	P01_CLKOUT	-780.087	-1210.146	GPIO port 0 bit 1 – Configured individually On CY7C601xx, optional Clock Out when external oscillator is disabled or external oscillator output drive when external oscillator is enabled.
23	P00_CLKIN	-127.386	-1210.146	GPIO port 0 bit 0 – Configured individually On CY7C601xx, optional Clock In when external oscillator is disabled or external oscillator input when external oscillator is enabled.
24	Vss	-32.571	-1210.146	Ground
25	P10_DP	104.643	-1210.146	GPIO port 1 bit 0/ISSP-SCLK If this pin is used as a general-purpose output it draws current. It is, therefore, configured as an input to reduce current draw.
26	P11_DM	416.199	-1210.146	GPIO port 1 bit 1/ISSP-SDATA If this pin is used as a general-purpose output it draws current. It is, therefore, configured as an input to reduce current draw.
27	Vdd	777.966	-1210.146	Power
28	P12	752.556	-747.432	GPIO port 1 bit 2

**Note**

2. The pads 1, 2, 3, 4, 45, 46, and 47 should be left unconnected.

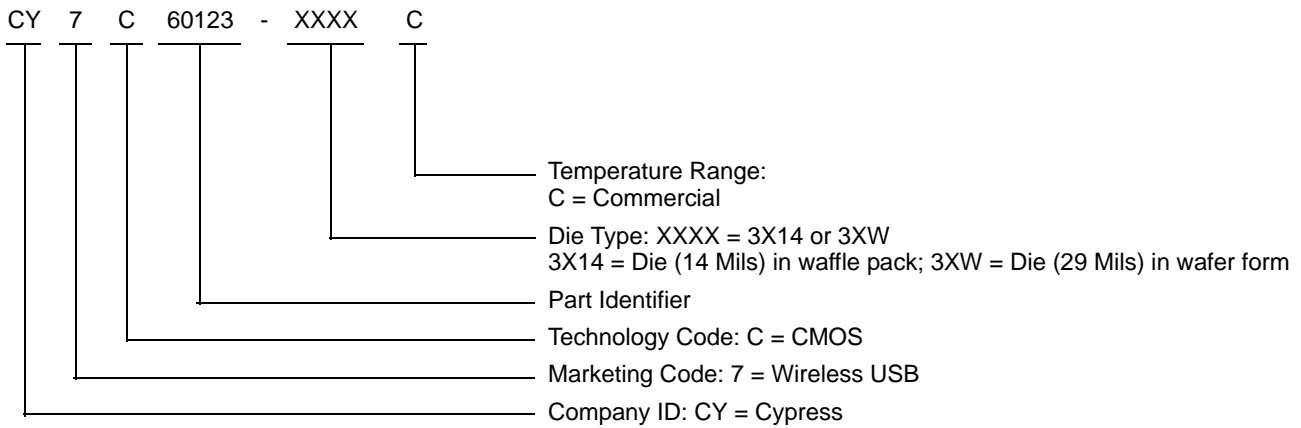
**Table 3. Bond Pad Coordinates and Signal Descriptions** *(continued)*

Pad Number <sup>[2]</sup>	Pad Name	Co-ordinates		Description
		X (μm)	Y (μm)	
29	P13_SSEL	752.556	-598.521	GPIO port 1 bit 3 – Configured individually Alternate function is SSEL signal of the SPI bus.
30	P14_SCLK	752.556	-505.617	GPIO port 1 bit 4 – Configured individually Alternate function is SCLK signal of the SPI bus.
31	P15_SMOSI	752.556	-191.436	GPIO port 1 bit 5 – Configured individually Alternate function is SMOSI signal of the SPI bus.
32	P16_SMISO	752.556	-98.532	GPIO port 1 bit 6 – Configured individually Alternate function is SMISO signal of the SPI bus.
33	P17	752.556	2.877	GPIO port 1 bit 7 – Configured individually TTL voltage threshold.
34	P30	752.556	95.781	GPIO port 3 – configured as a group (byte)
35	P31	752.556	581.931	
36	P32	752.556	674.835	
37	P33	752.556	767.739	
38	P34	752.556	860.643	
39	P35	752.556	953.547	
40	P36	752.556	1046.451	
41	P37	782.25	1198.827	
42	P42	608.622	1209.705	
43	P43	471.219	1220.457	
44	VSS1	353.451	1213.317	Ground
45	NC	219.303	1220.457	No Connect
46	NC	129.297	1220.457	No Connect
47	NC	33.495	1220.457	No Connect

**Die Ordering Information**

Ordering Code	Die Type	Operating Range
CY7C60123-3X14C	Die (14 Mils) in waffle pack	Commercial
CY7C60123-3XWC	Die (29 Mils) in wafer form	Commercial
CG7592AS	Die (14 Mils) in waffle pack	Commercial

**Ordering Code Definitions**



**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
μm	micrometer

**Document History Page**

Document Title: CY7C60123, enCoRe™ II LV Microcontroller Die Document Number: 001-75786				
Revision	ECN	Orig. Change	Submission Date	Description of Change
**	3507375	ANTG	01/31/2012	New datasheet
*A	3705650	SIRK	08/07/2012	Updated title and document information with part number CY7C60123-3XWC.
*B	4426785	SETU	07/01/2014	Updated <a href="#">Die Ordering Information</a> (Updated part numbers). Updated in new template.
*C	4447669	VIKS	07/18/2014	Updated <a href="#">Product Thickness Guide</a> : Updated <a href="#">Table 2</a> : Replaced 27 Mils with 29 Mils in description of 3XWC. Updated minimum, nominal and maximum values of 3XWC. Updated <a href="#">Die Ordering Information</a> : No change in part numbers. Replaced 27 Mils with 29 Mils in "Die Type" column corresponding to Ordering Code "CY7C60123-3XWC". Updated <a href="#">Ordering Code Definitions</a> .
*D	4650356	VIKS	02/04/2015	No technical changes. Sunset ECN.

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