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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY7C1051H Automotive

8-Mbit (512K × 16) Static RAM

Features

- AEC-Q100 qualified
- Temperature ranges
  - Automotive-E: –40 °C to +125 °C
- High speed
  - t_{AA} = 10 ns
- Low active and standby currents
  - I_{CC} = 90 mA typical
  - I_{SB2} = 20 mA typical
- 1.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 44-pin thin small outline package (TSOP) II and 48-ball very fine-pitch ball grid array (VFBGA) package

Functional Description

The CY7C1051H[1] is a high-performance CMOS fast static RAM automotive part with embedded ECC.

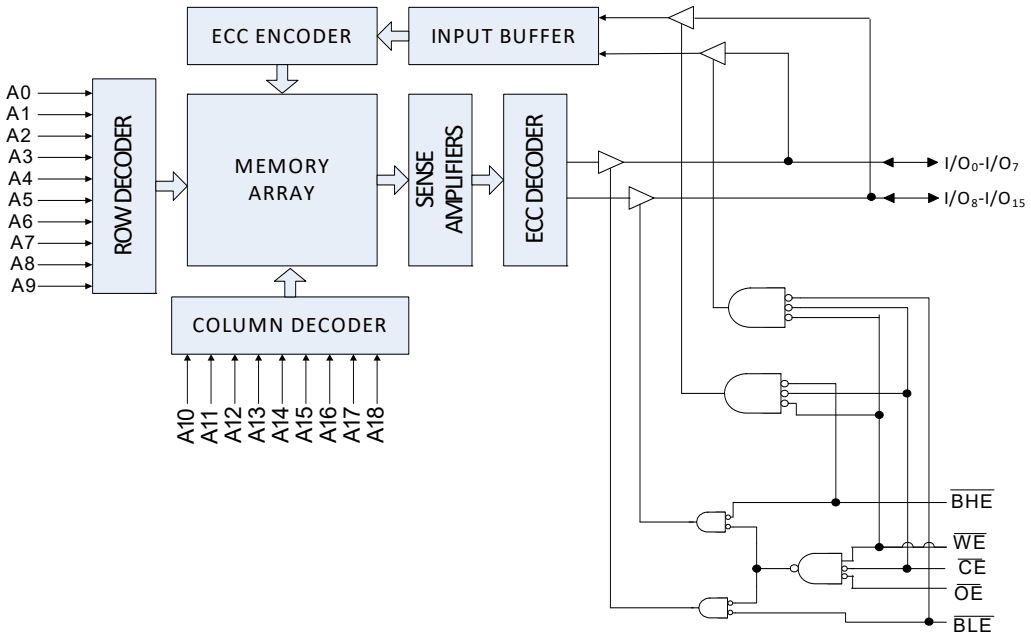
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0–I/O_7), is written into the location specified on the address pins (A_0–A_{18}). If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8–I/O_{15}) is written into the location specified on the address pins (A_0–A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0–I/O_7. If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

The input/output pins (I/O_0–I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW) is in progress.

The CY7C1051H is available in 44-pin TSOP II and 48-ball VFBGA package.

Logic Block Diagram – CY7C1051H



Note
1. This device does not support automatic write-back on error detection.

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Pin Configurations

Figure 1. 48-ball FBGA Pinout (Top View) [2]

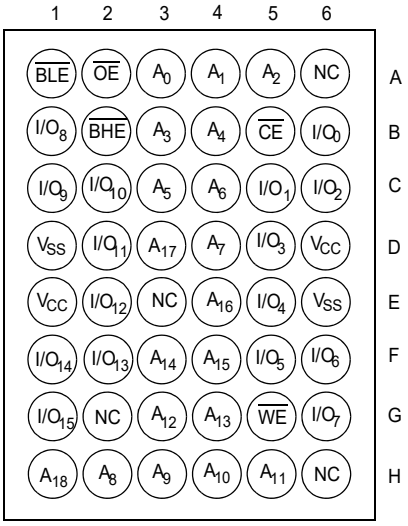
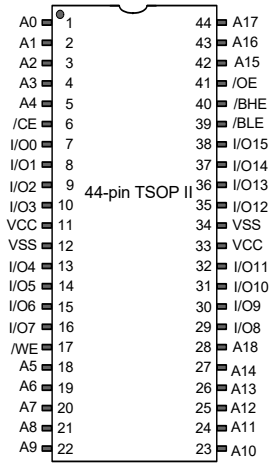


Figure 2. 44-pin TSOP II Pinout



Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
				Typ [3]	Max	Typ [3]	Max
CY7C1051H	Automotive-E	2.2 V–3.6 V	10	90	160	20	50

Notes
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND [4] .....–0.5 V to +4.6 V

DC voltage applied to outputs in high-Z state [4] ..... –0.3 V to V_{CC} + 0.3 V

DC input voltage [4] ..... –0.3 V to V_{CC} + 0.3 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive-E	–40 °C to +125 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions		Automotive-E		Unit
					Min	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2	–	V
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	V
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	0.4	V
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	–		2	V_{CC} + 0.3	V
		2.7 V to 3.6 V	–		2	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage [4]	2.2 V to 2.7 V	–		–0.3	0.6	V
		2.7 V to 3.6 V	–		–0.3	0.8	V
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–5	+5	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–5	+5	µA
I_{CC}	Operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = f_{MAX} = $1/t_{RC}$	–	160	mA
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	60	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	50	mA

Note

4. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.

Capacitance

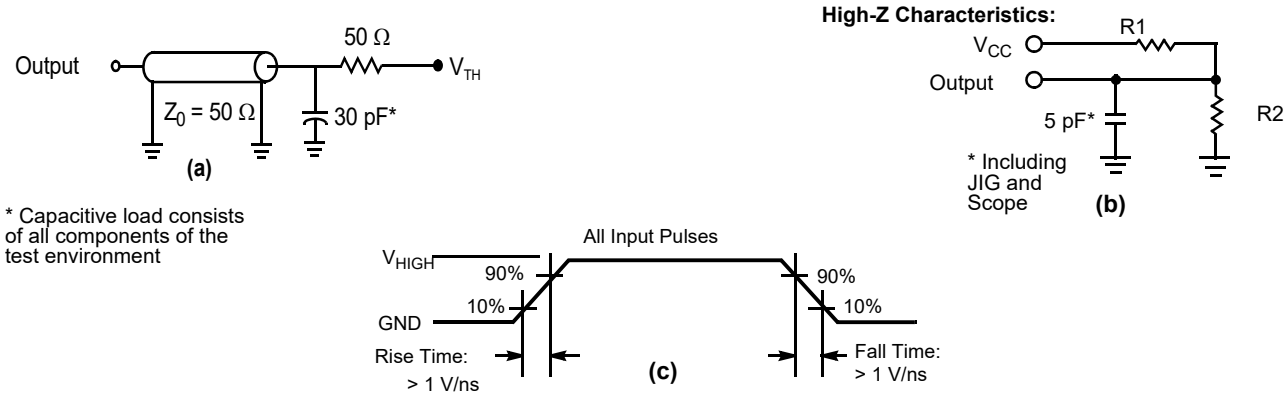
Parameter [5]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	44-pin TSOP II Package	48-ball VFBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	66.96	31.50	°C/W
Θ_{JC}	Thermal resistance (junction to case)		12.66	15.75	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [6]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Notes
5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device AC operation assumes a 100-µs ramp time from 0 to $V_{CC(min)}$ and 100-µs wait time after V_{CC} stabilization.

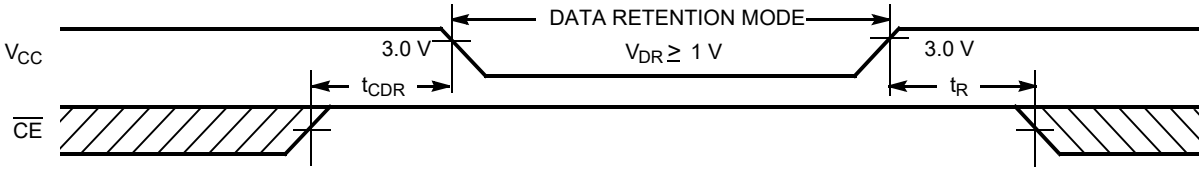
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	50	mA
t_{CDR}[7]	Chip deselect to data retention time	–	0	–	ns
t_R[8]	Operation recovery time	$V_{CC} \geq 2.2$ V	10	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

AC Switching Characteristics

Over the Operating Range

Parameter [9]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{power} [10]	V_{CC}(typical) to the First Access	100	–	µs
t_{RC}	Read Cycle Time	10	–	ns
t_{AA}	Address to Data Valid	–	10	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [11]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [11, 12]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [11]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [11, 12]	–	5	ns
t_{PU}	$\overline{CE}$ LOW to Power Up [13]	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to Power Down [13]	–	10	ns
t_{DBE}	Byte Enable to Data Valid	–	5	ns
t_{LZBE}	Byte Enable to Low Z [11]	0	–	ns
t_{HZBE}	Byte Disable to High Z [11, 12]	–	6	ns
Write Cycle [14, 15]				
t_{WC}	Write Cycle Time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7	–	ns
t_{AW}	Address Setup to Write End	7	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	7	–	ns
t_{SD}	Data Setup to Write End	5	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [11]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [11, 12]	–	5	ns
t_{BW}	Byte Enable to End of Write	7	–	ns

Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
10. t_{POWER} gives the minimum amount of time that the power supply must be at typical V_{CC} values until the first memory access can be performed.
11. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any device.
12. t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 5.Transition is measured when the outputs enter a high impedance state.
13. These parameters are guaranteed by design and are not tested.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must refer to the leading edge of the signal that terminates the write.
15. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 [16, 17]

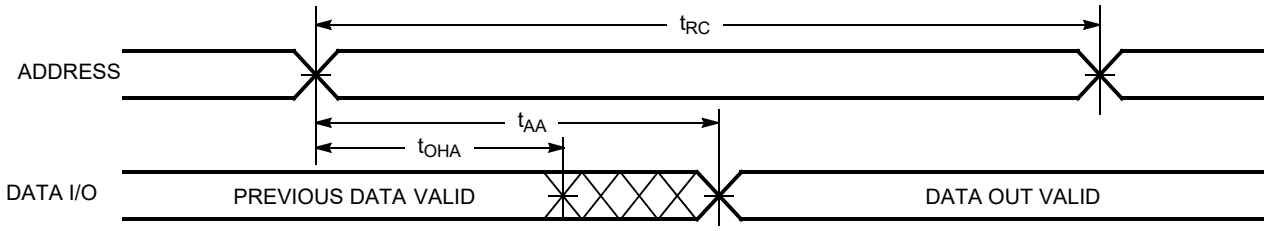
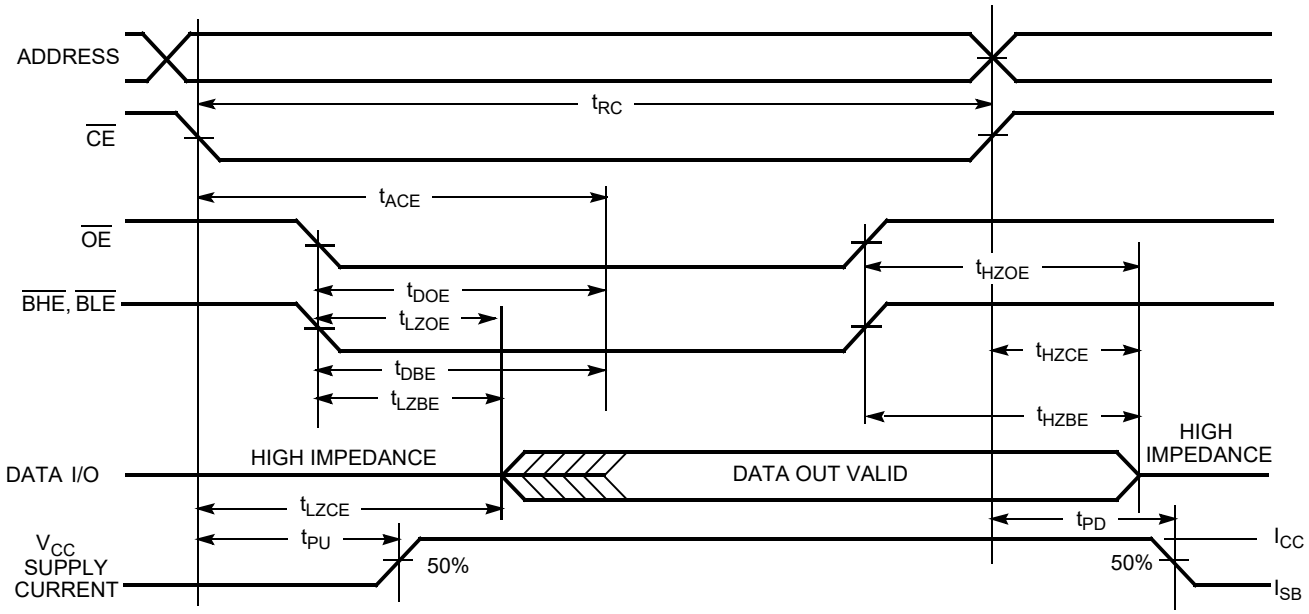


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [17, 18]



Notes
16. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
17. $\overline{WE}$ is HIGH for Read cycle.
18. Address valid before or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms(continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [19, 20, 21]

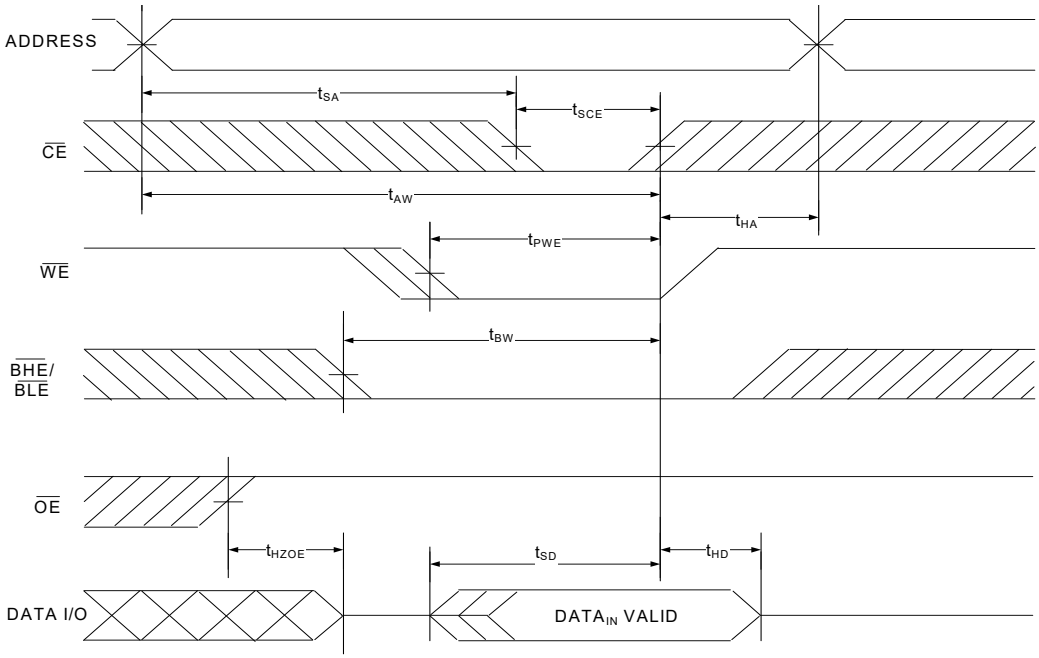
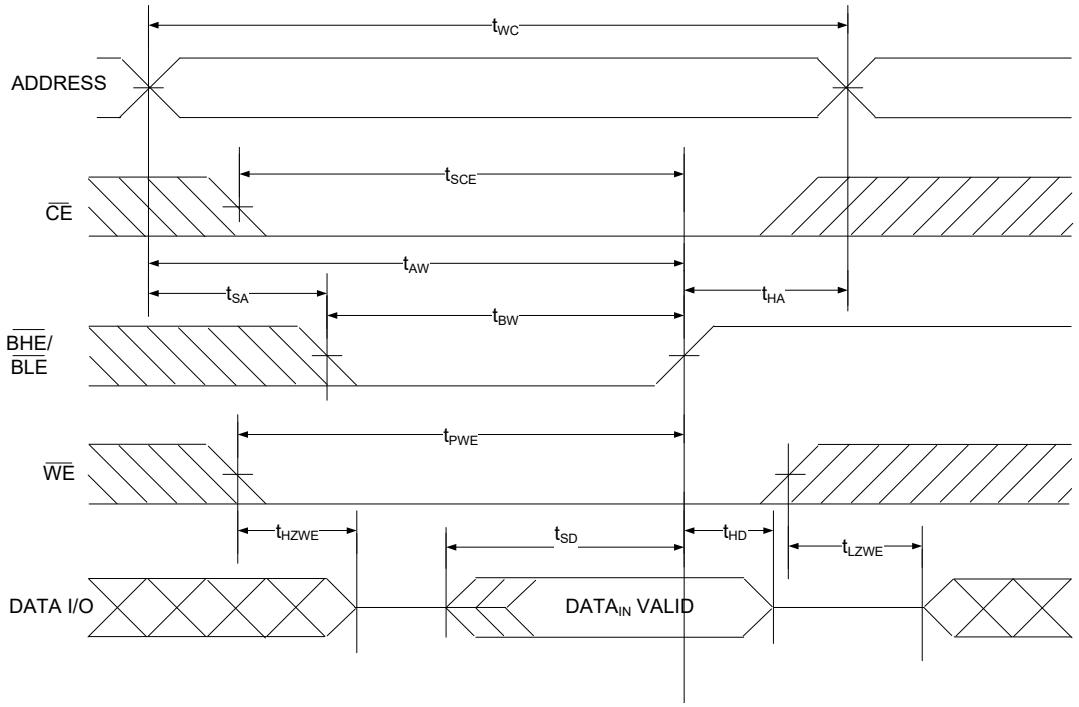


Figure 8. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [19, 20, 21]



Notes

19. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
21. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms(continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [22, 23, 24, 25]

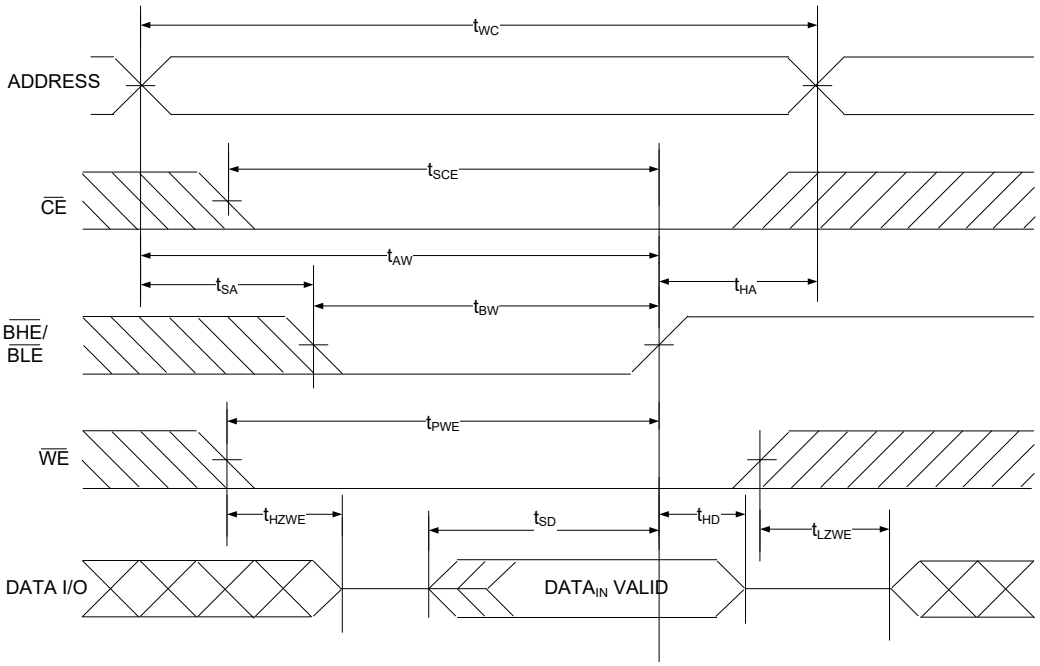
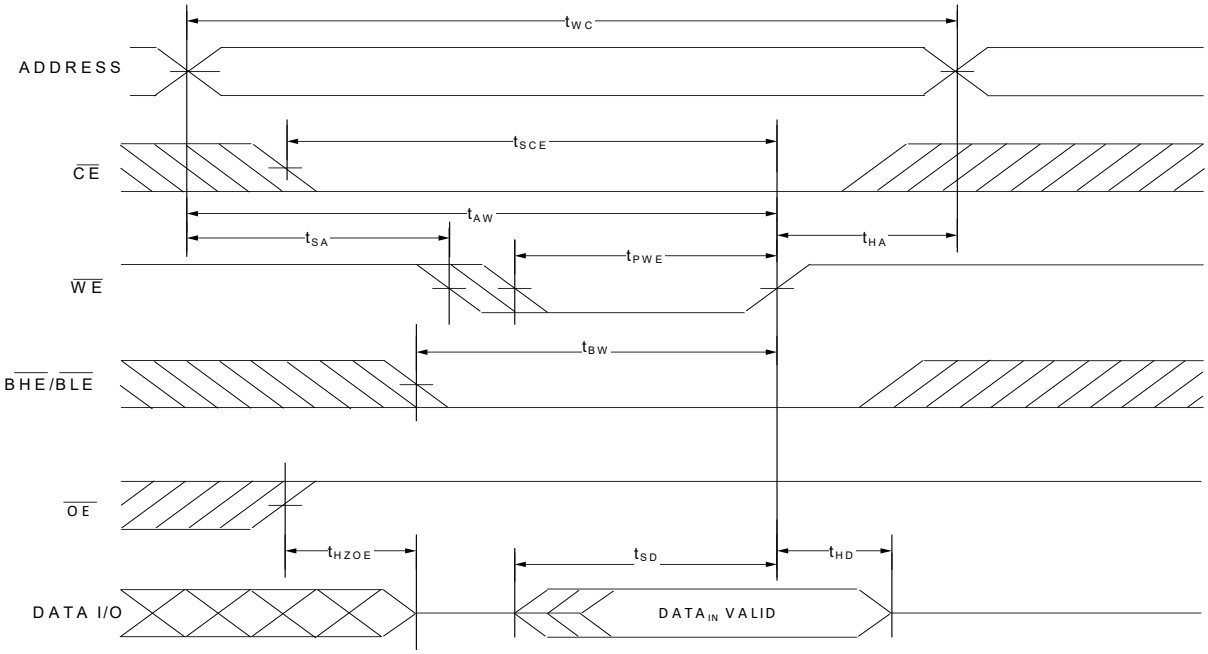


Figure 10. Write Cycle No. 4 ($\overline{WE}$ Controlled) [23, 24]



Notes

22. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.
23. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. Data I/O is in high impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
25. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

The truth table is as follows [26]:

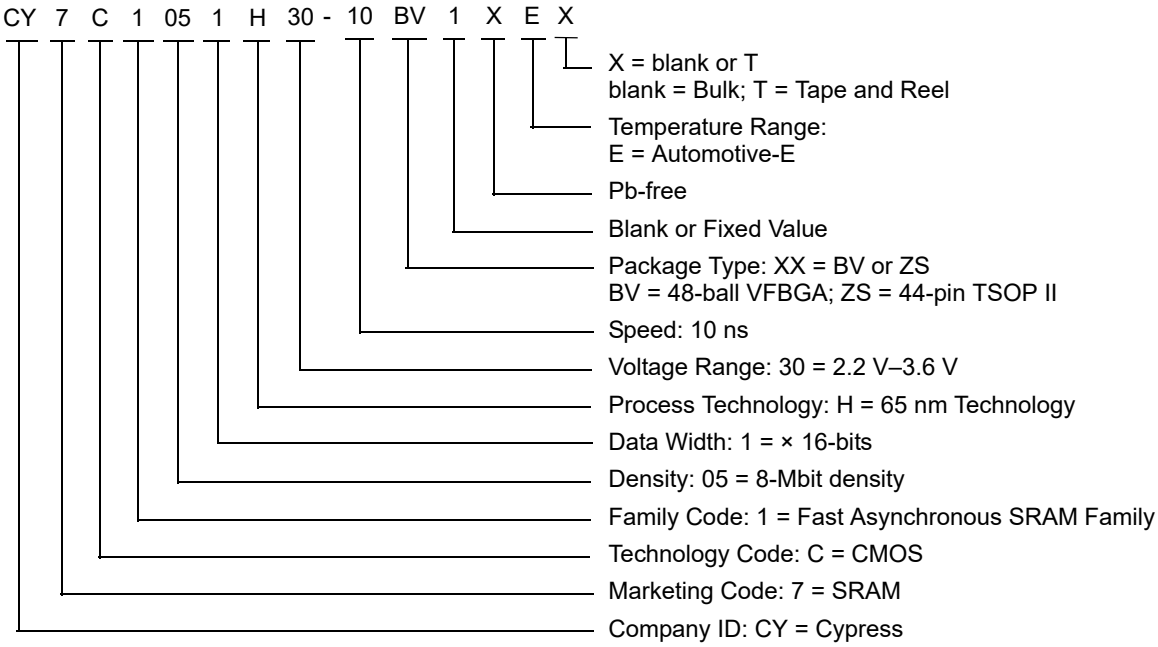
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	BLE	BHE	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Note
26. The input voltage levels on signals with value X should be either at V_{IH} or V_{IL}.

Ordering Information

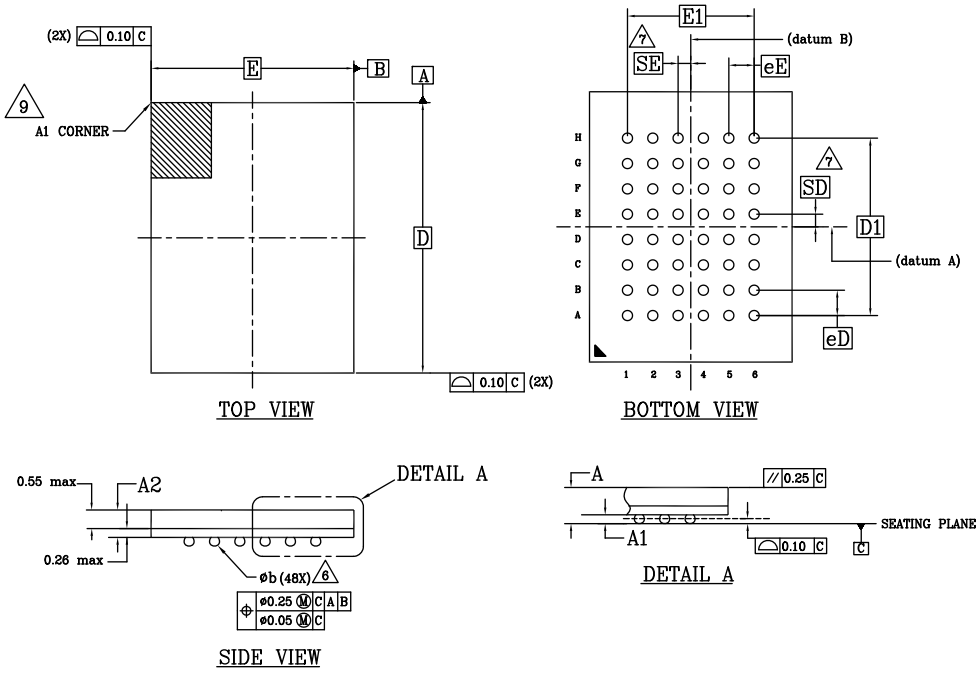
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
10	2.2 V–3.6 V	CY7C1051H30-10BV1XE	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Automotive-E
		CY7C1051H30-10BV1XET			
	2.2 V–3.6 V	CY7C1051H30-10ZSXE	51-85087	44-pin TSOP II (Pb-free)	
		CY7C1051H30-10ZSXET			

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

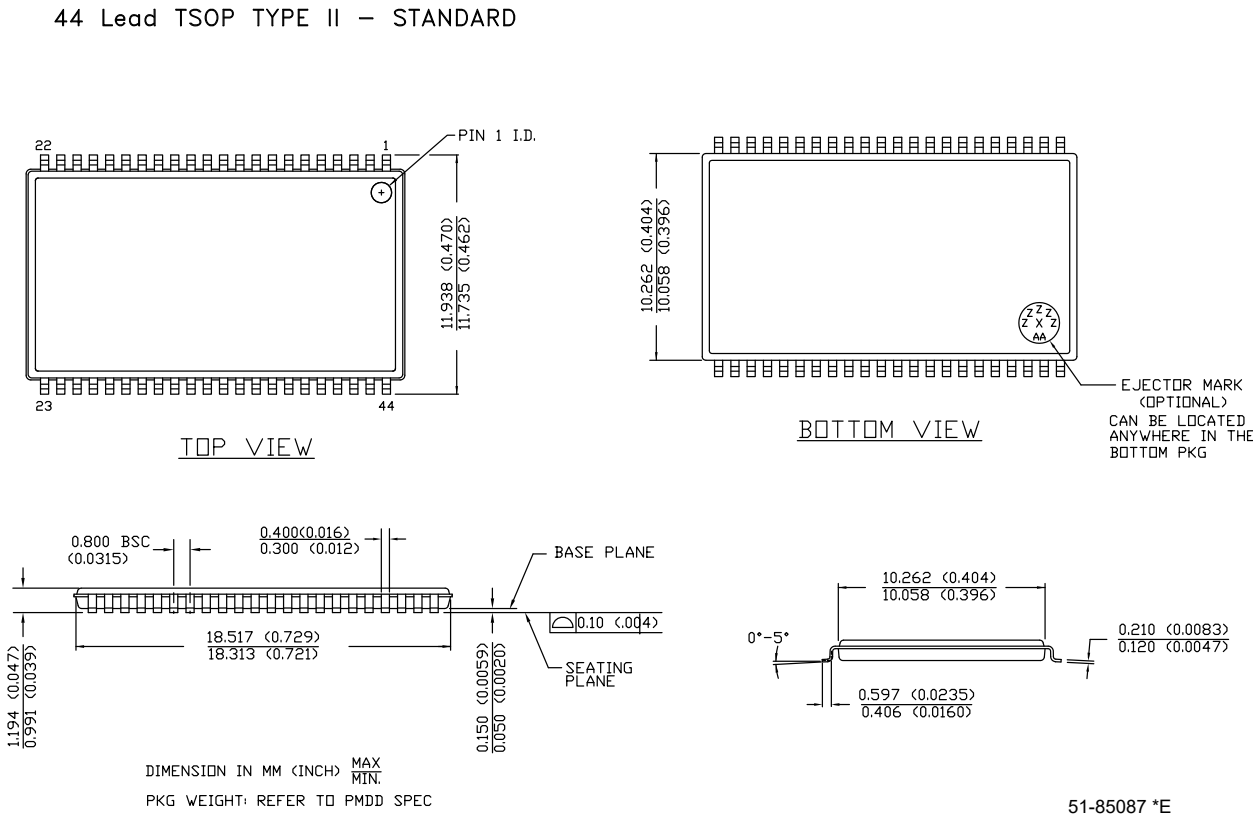
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Package Diagrams(continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1051H Automotive, 8-Mbit (512K × 16) Static RAM Document Number: 001-87624				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C	4961297	NILE	10/13/2015	Changed status from Preliminary to Final.
*D	5303970	VINI	06/10/2016	Added Automotive-A Temperature Range related information in all instances across the document. Added 44-pin TSOP II Package related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Added spec 51-85087 *E. Updated to new template. Completing Sunset Review.
*E	5333780	VINI	07/20/2016	Removed Automotive-A Temperature Range related information in all instances across the document. Removed 44-pin TSOP II Package related information in all instances across the document. Updated Features: Added “AEC-Q100 qualified”. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Removed spec 51-85087 *E.
*F	5435305	VINI	09/13/2016	Updated Maximum Ratings: Updated Note 4 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V_{OH} parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V_{OH} parameter. Updated Ordering Information: Updated part numbers. Updated to new template.
*G	6012091	AESATMP9	01/03/2018	Updated logo and copyright.
*H	6183584	NILE	05/31/2018	Added 44-pin TSOP II Package related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Added spec 51-85087 *E. Completing Sunset Review.
*I	6352307	NILE	10/31/2018	Updated Thermal Resistance: Fixed typo (Replaced “48-pin TSOP II Package” with “44-pin TSOP II Package” in column heading). Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I.

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