

## Features

- Pin-and function-compatible with CY7C1011CV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 90 \text{ mA @ } 10 \text{ ns (Industrial)}$
- Low CMOS standby power
  - $I_{SB2} = 10 \text{ mA}$
- Data Retention at 2.0 V
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 44-pin TSOP II, and 48-ball VFBGA

## Functional Description

The CY7C1011DV33<sup>[1]</sup> is a high-performance CMOS Static RAM organized as 128 K words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

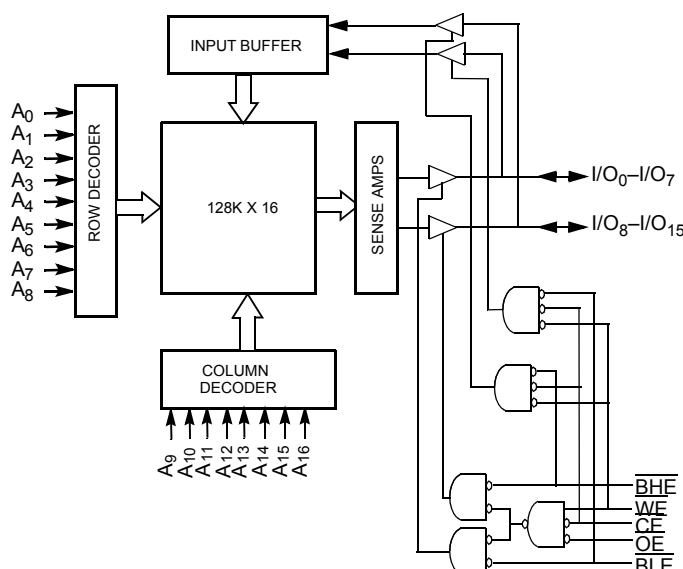
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1011DV33 is available in standard Pb-free 44-pin TSOP II with center power and ground pinout, as well as 48-ball very fine-pitch ball grid array (VFBGA) packages.

For a complete list of related resources, [click here](#).

## Logic Block Diagram



### Note

1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com)

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## Selection Guide

| Description                  | -10 | Unit |
|------------------------------|-----|------|
| Maximum Access Time          | 10  | ns   |
| Maximum Operating Current    | 90  | mA   |
| Maximum CMOS Standby Current | 10  | mA   |

## Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View)

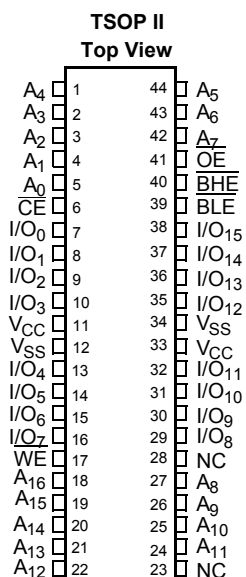
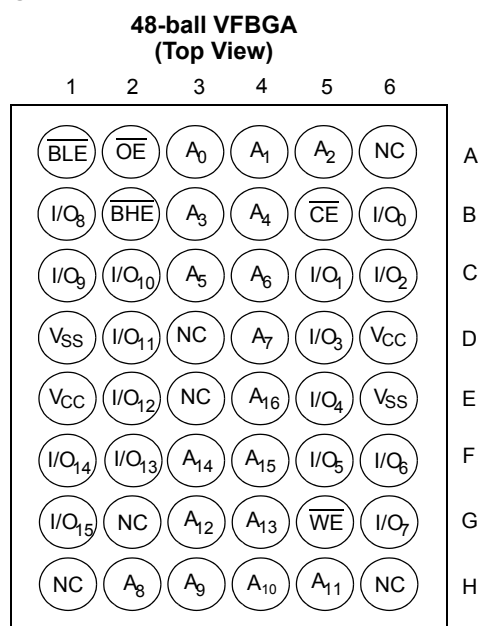


Figure 2. 48-ball VFBGA pinout (Top View)



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND <sup>[2]</sup> ..... -0.3 V to +4.6 V

DC voltage applied to outputs in high Z State <sup>[2]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

DC input voltage <sup>[2]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Range      | Ambient Temperature | $V_{CC}$      |
|------------|---------------------|---------------|
| Industrial | -40 °C to +85 °C    | 3.3 V ± 0.3 V |

## DC Electrical Characteristics

Over the Operating Range

| Parameter        | Description                                   | Test Conditions                                                                                                                                      |         | -10  |                       | Unit |
|------------------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------|-----------------------|------|
|                  |                                               |                                                                                                                                                      |         | Min  | Max                   |      |
| V <sub>OH</sub>  | Output HIGH voltage                           | V <sub>CC</sub> = Min, I <sub>OH</sub> = −4.0 mA                                                                                                     |         | 2.4  | –                     | V    |
| V <sub>OL</sub>  | Output LOW voltage                            | V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA                                                                                                      |         | –    | 0.4                   | V    |
| V <sub>IH</sub>  | Input HIGH voltage                            |                                                                                                                                                      |         | 2.0  | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>  | Input LOW voltage <sup>[3]</sup>              |                                                                                                                                                      |         | −0.3 | 0.8                   | V    |
| I <sub>IX</sub>  | Input leakage current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                               |         | −1   | +1                    | μA   |
| I <sub>OZ</sub>  | Output leakage current                        | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled                                                                                           |         | −1   | +1                    | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> operating supply current      | V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>                                                                                      | 100 MHz | –    | 90                    | mA   |
|                  |                                               |                                                                                                                                                      | 83 MHz  | –    | 80                    |      |
|                  |                                               |                                                                                                                                                      | 66 MHz  | –    | 70                    |      |
|                  |                                               |                                                                                                                                                      | 40 MHz  | –    | 60                    |      |
| I <sub>SB1</sub> | Automatic CE Power-down Current — TTL Inputs  | Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ ,<br>V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> |         | –    | 20                    | mA   |
| I <sub>SB2</sub> | Automatic CE Power-down Current — CMOS Inputs | Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0  |         | –    | 10                    | mA   |

### Notes

2. Tested initially and after any design or process changes that may affect these parameters.
3.  $V_{IL}(\text{min}) = -2.0 \text{ V}$  and  $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V}$  for pulse durations of less than 20 ns.

## Capacitance

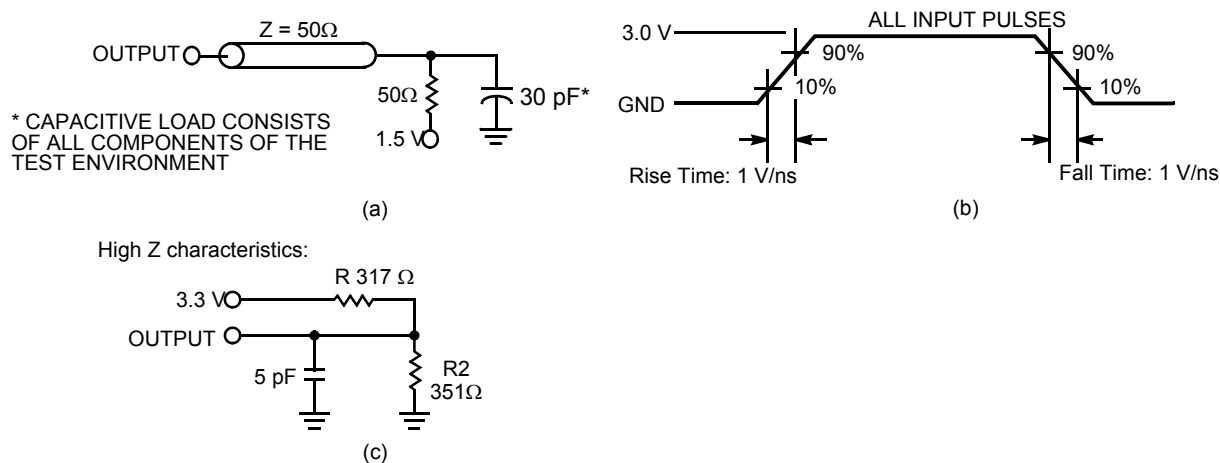
| Parameter <sup>[4]</sup> | Description       | Test Conditions                                                         | Max | Unit |
|--------------------------|-------------------|-------------------------------------------------------------------------|-----|------|
| $C_{IN}$                 | Input capacitance | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$ | 8   | pF   |
| $C_{OUT}$                | I/O capacitance   |                                                                         | 8   | pF   |

## Thermal Resistance

| Parameter <sup>[4]</sup> | Description                              | Test Conditions                                                                | TSOP II | VFBGA | Unit               |
|--------------------------|------------------------------------------|--------------------------------------------------------------------------------|---------|-------|--------------------|
| $\Theta_{JA}$            | Thermal resistance (junction to ambient) | Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board | 50.66   | 27.89 | $^\circ\text{C/W}$ |
| $\Theta_{JC}$            | Thermal resistance (junction to case)    |                                                                                | 17.17   | 14.74 | $^\circ\text{C/W}$ |

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[5]</sup>



### Note

4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except high Z) are tested using the load conditions shown in (a). High Z characteristics are tested for all speeds using the test load shown in (c).

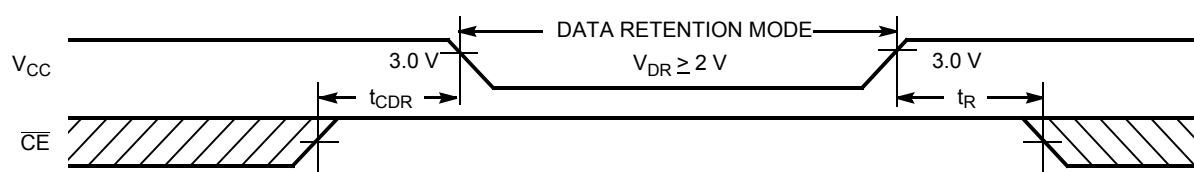
## Data Retention Characteristics

Over the Operating Range

| Parameter       | Description                          | Conditions <sup>[6]</sup>                                                                                                                            | Min      | Max | Unit |
|-----------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----|------|
| $V_{DR}$        | $V_{CC}$ for data retention          |                                                                                                                                                      | 2.0      | –   | V    |
| $I_{CCDR}$      | Data retention current               |                                                                                                                                                      | –        | 10  | mA   |
| $t_{CDR}^{[7]}$ | Chip deselect to data retention time | $V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | 0        | –   | ns   |
| $t_R^{[8]}$     | Operation recovery time              |                                                                                                                                                      | $t_{RC}$ | –   | ns   |

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

6. No input may exceed  $V_{CC} + 0.3\text{ V}$ .
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the Operating Range

| Parameter <sup>[9]</sup>           | Description                                               | -10 |     | Unit |
|------------------------------------|-----------------------------------------------------------|-----|-----|------|
|                                    |                                                           | Min | Max |      |
| Read Cycle                         |                                                           |     |     |      |
| t <sub>power</sub> <sup>[10]</sup> | V <sub>CC</sub> (typical) to the first access             | 100 | –   | μs   |
| t <sub>RC</sub>                    | Read cycle time                                           | 10  | –   | ns   |
| t <sub>AA</sub>                    | Address to data valid                                     | –   | 10  | ns   |
| t <sub>OHA</sub>                   | Data hold from address change                             | 3   | –   | ns   |
| t <sub>ACE</sub>                   | $\overline{\text{CE}}$ LOW to data valid                  | –   | 10  | ns   |
| t <sub>DOE</sub>                   | $\overline{\text{OE}}$ LOW to data valid                  | –   | 5   | ns   |
| t <sub>LZOE</sub>                  | $\overline{\text{OE}}$ LOW to low Z <sup>[11]</sup>       | 0   | –   | ns   |
| t <sub>HZOE</sub>                  | $\overline{\text{OE}}$ HIGH to high Z <sup>[11, 12]</sup> | –   | 5   | ns   |
| t <sub>LZCE</sub>                  | $\overline{\text{CE}}$ LOW to low Z <sup>[11]</sup>       | 3   | –   | ns   |
| t <sub>HZCE</sub>                  | $\overline{\text{CE}}$ HIGH to high Z <sup>[11, 12]</sup> | –   | 5   | ns   |
| t <sub>PU</sub>                    | $\overline{\text{CE}}$ LOW to power-up                    | 0   | –   | ns   |
| t <sub>PD</sub>                    | $\overline{\text{CE}}$ HIGH to power-down                 | –   | 10  | ns   |
| t <sub>DBE</sub>                   | Byte enable to data valid                                 | –   | 5   | ns   |
| t <sub>LZBE</sub>                  | Byte enable to low Z                                      | 0   | –   | ns   |
| t <sub>HZBE</sub>                  | Byte disable to high Z                                    | –   | 6   | ns   |
| Write Cycle <sup>[13, 14]</sup>    |                                                           |     |     |      |
| t <sub>WC</sub>                    | Write cycle time                                          | 10  | –   | ns   |
| t <sub>SCE</sub>                   | $\overline{\text{CE}}$ LOW to write end                   | 7   | –   | ns   |
| t <sub>AW</sub>                    | Address set-up to write end                               | 7   | –   | ns   |
| t <sub>HA</sub>                    | Address hold from write end                               | 0   | –   | ns   |
| t <sub>SA</sub>                    | Address set-up to write start                             | 0   | –   | ns   |
| t <sub>PWE</sub>                   | $\overline{\text{WE}}$ pulse width                        | 7   | –   | ns   |
| t <sub>SD</sub>                    | Data set-up to write end                                  | 5   | –   | ns   |
| t <sub>HD</sub>                    | Data hold from write end                                  | 0   | –   | ns   |
| t <sub>LZWE</sub>                  | $\overline{\text{WE}}$ HIGH to low Z <sup>[11]</sup>      | 3   | –   | ns   |
| t <sub>HZWE</sub>                  | $\overline{\text{WE}}$ LOW to high Z <sup>[11, 12]</sup>  | –   | 5   | ns   |
| t <sub>BW</sub>                    | Byte enable to end of write                               | 7   | –   | ns   |

### Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

10.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access is performed.

11. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ ,  $t_{\text{HZBE}}$  is less than  $t_{\text{LZBE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.

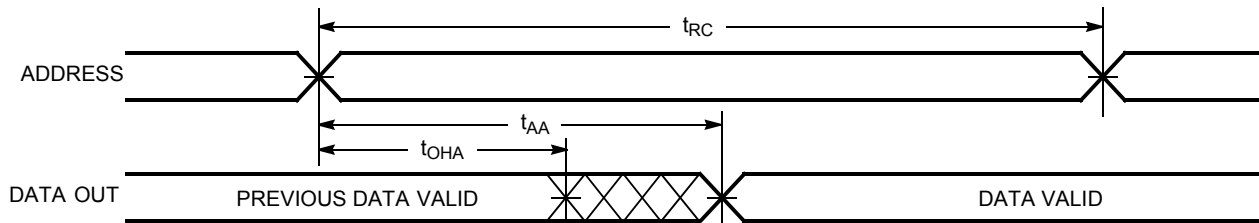
12.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZBE}}$  and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.

13. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

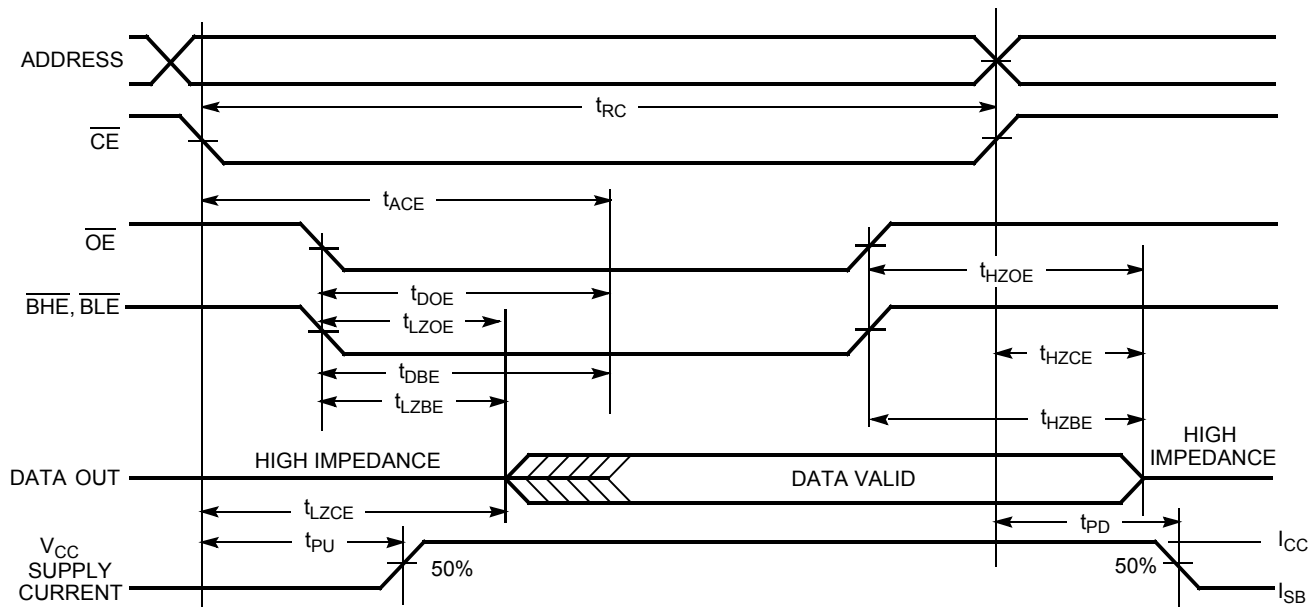
14. The minimum write cycle pulse width for Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be the sum of  $t_{\text{SD}}$  and  $t_{\text{HZWE}}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1** [15, 16]



**Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [16, 17]



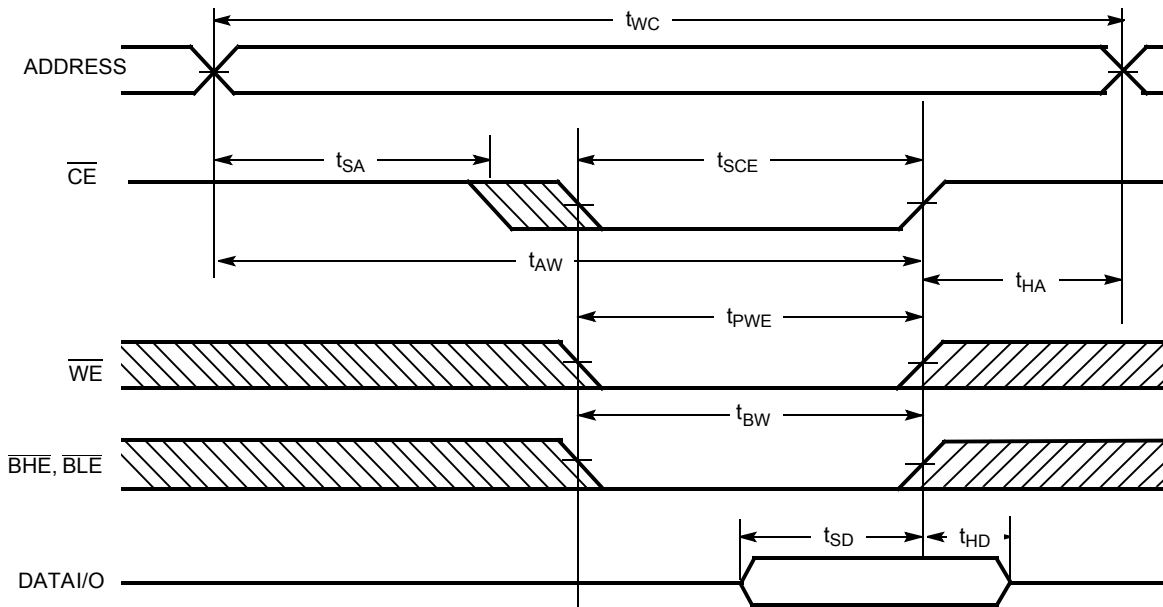
### Notes

15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BHE} = V_{IL}$ .
16.  $\overline{WE}$  is HIGH for read cycle.
17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

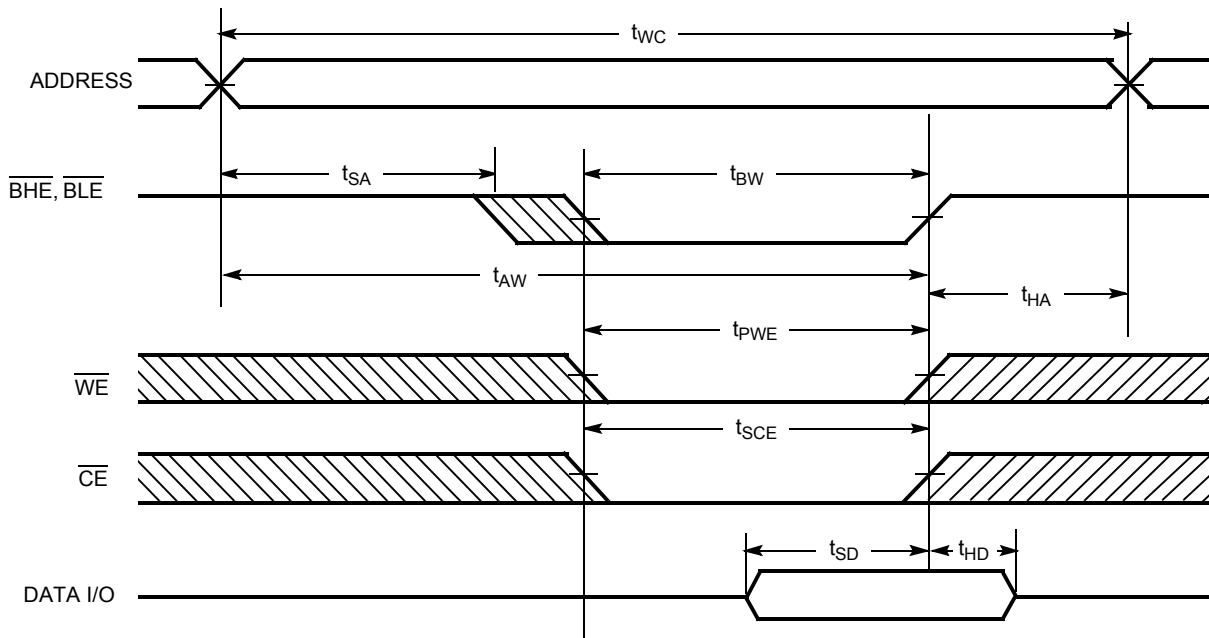


**Switching Waveforms** (continued)

**Figure 7. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [18, 19]



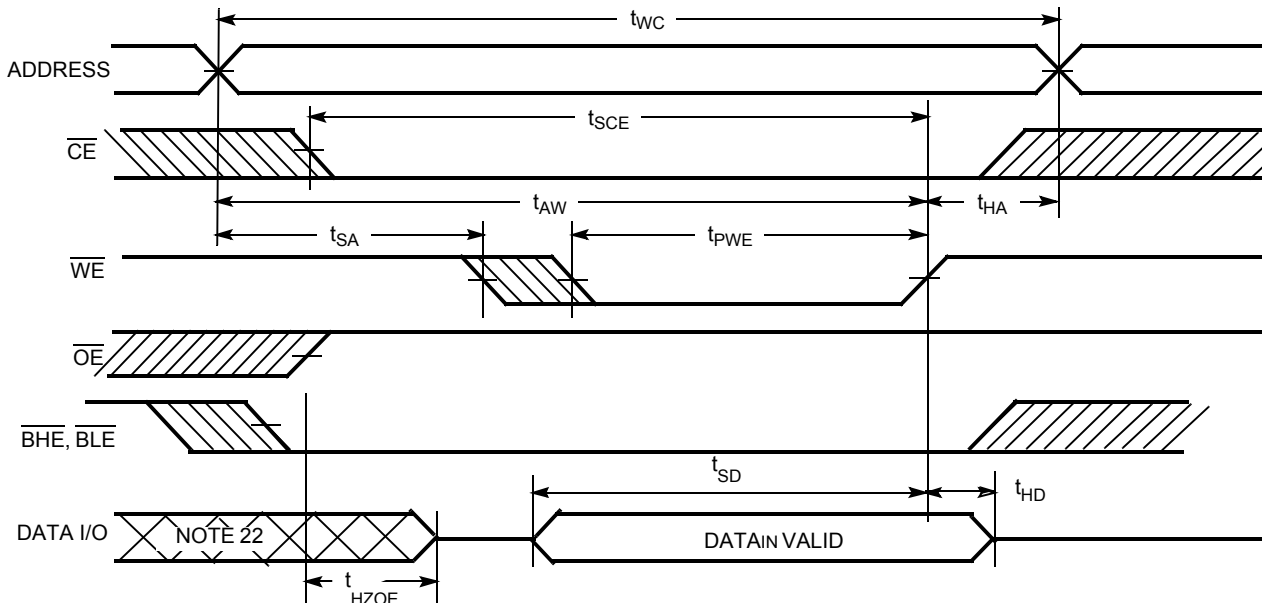
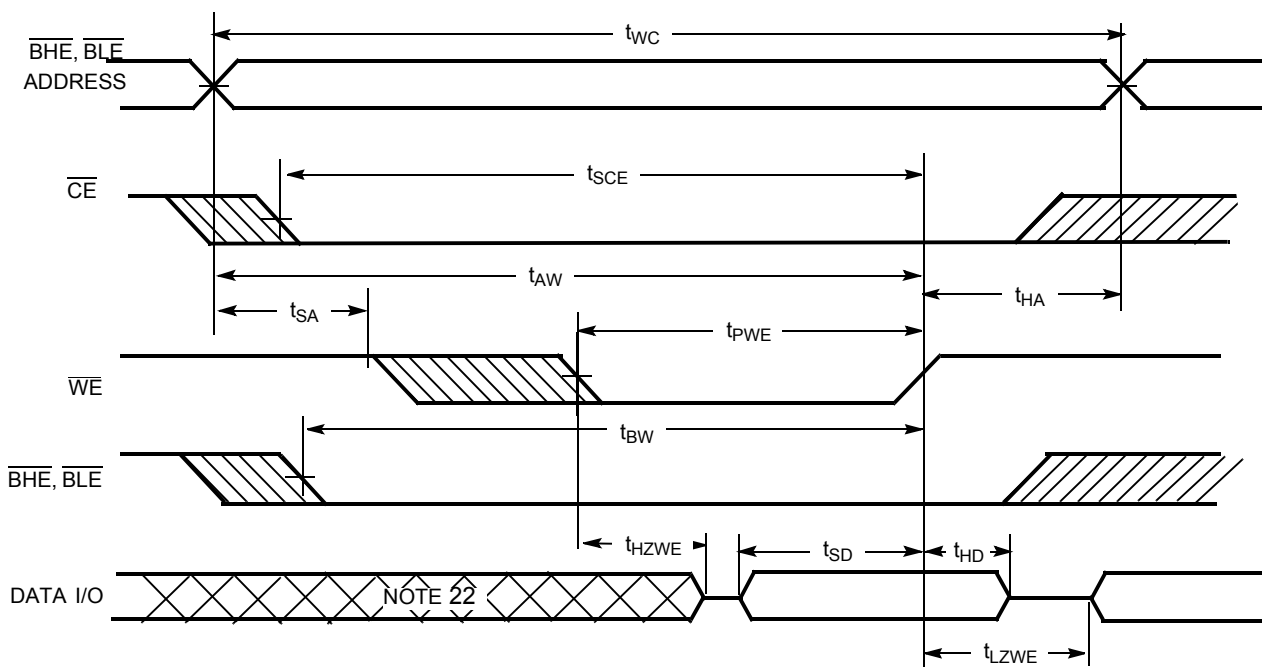
**Figure 8. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**



**Notes**

18. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .  
 19. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Figure 9. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write) [20, 21]**

**Figure 10. Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [23]**

**Notes**

20. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .  
 21. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.  
 22. During this period the I/Os are in the output state and input signals should not be applied.  
 23. The minimum write pulse width for Write Cycle No. 4 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) should be the sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Truth Table**

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{BLE}}$ | $\overline{\text{BHE}}$ | I/O <sub>0</sub> –I/O <sub>7</sub> | I/O <sub>8</sub> –I/O <sub>15</sub> | Mode                       | Power                      |
|------------------------|------------------------|------------------------|-------------------------|-------------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H                      | X                      | X                      | X                       | X                       | High Z                             | High Z                              | Power-down                 | Standby (I <sub>SB</sub> ) |
| L                      | L                      | H                      | L                       | L                       | Data Out                           | Data Out                            | Read all bits              | Active (I <sub>CC</sub> )  |
| L                      | L                      | H                      | L                       | H                       | Data Out                           | High Z                              | Read lower bits only       | Active (I <sub>CC</sub> )  |
| L                      | L                      | H                      | H                       | L                       | High Z                             | Data Out                            | Read upper bits only       | Active (I <sub>CC</sub> )  |
| L                      | X                      | L                      | L                       | L                       | Data In                            | Data In                             | Write all bits             | Active (I <sub>CC</sub> )  |
| L                      | X                      | L                      | L                       | H                       | Data In                            | High Z                              | Write lower bits only      | Active (I <sub>CC</sub> )  |
| L                      | X                      | L                      | H                       | L                       | High Z                             | Data In                             | Write upper bits only      | Active (I <sub>CC</sub> )  |
| L                      | H                      | H                      | X                       | X                       | High Z                             | High Z                              | Selected, outputs disabled | Active (I <sub>CC</sub> )  |

## Ordering Information

| Speed (ns) | Ordering Code       | Package Diagram | Package Type             | Operating Range |
|------------|---------------------|-----------------|--------------------------|-----------------|
| 10         | CY7C1011DV33-10ZSXI | 51-85087        | 44-pin TSOP II (Pb-free) | Industrial      |
|            | CY7C1011DV33-10BVXI | 51-85150        | 48-ball VFBGA (Pb-free)  |                 |

Please contact your local Cypress sales representative for availability of these parts

## Ordering Code Definitions

|    |   |   |   |    |   |   |     |   |    |    |   |   |                                                |
|----|---|---|---|----|---|---|-----|---|----|----|---|---|------------------------------------------------|
| CY | 7 | C | 1 | 01 | 1 | D | V33 | - | 10 | XX | X | I |                                                |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Temperature Range:                             |
|    |   |   |   |    |   |   |     |   |    |    |   |   | I = Industrial                                 |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Pb-free                                        |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Package Type: XX = ZS or BV                    |
|    |   |   |   |    |   |   |     |   |    |    |   |   | ZS = 44-pin TSOP II                            |
|    |   |   |   |    |   |   |     |   |    |    |   |   | BV = 48-ball VFBGA                             |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Speed: 10 ns                                   |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Voltage Range: V33 = 3 V to 3.6 V              |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Process Technology: D = C9, 90 nm Technology   |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Data Width: 1 = × 16-bits                      |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Density: 01 = 2-Mbit                           |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Family Code: 1 = Fast Asynchronous SRAM family |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Technology Code: C = CMOS                      |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Marketing Code: 7 = SRAM                       |
|    |   |   |   |    |   |   |     |   |    |    |   |   | Company ID: CY = Cypress                       |

## Package Diagrams

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087

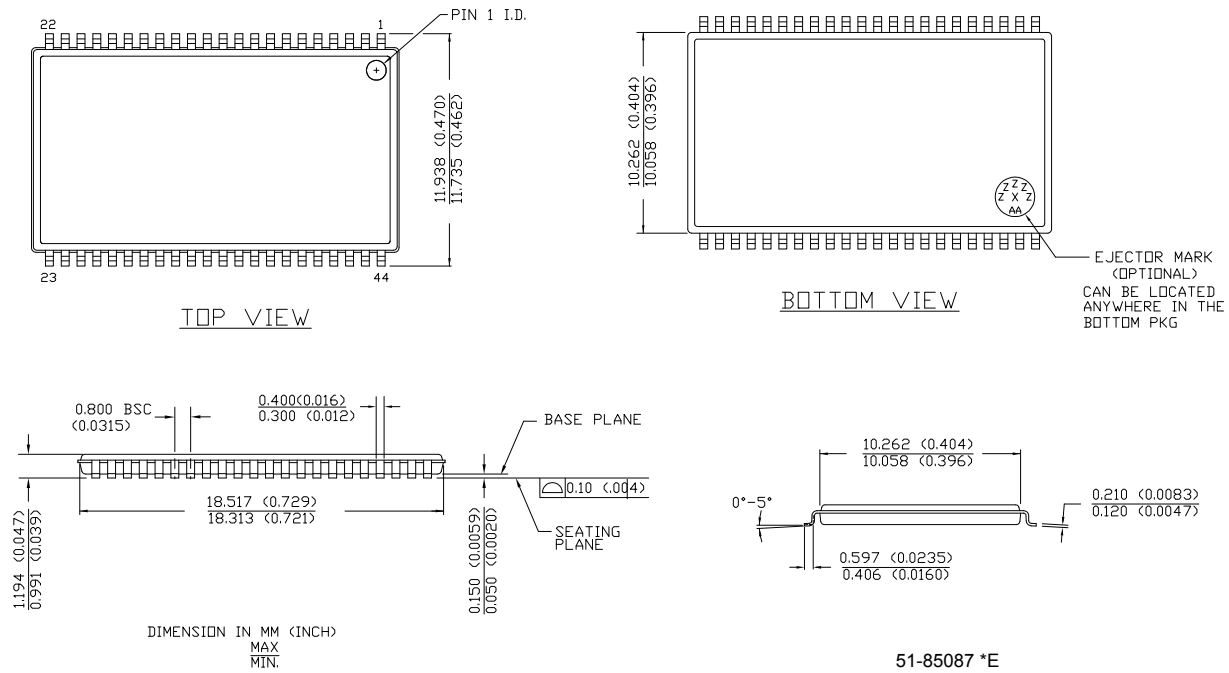
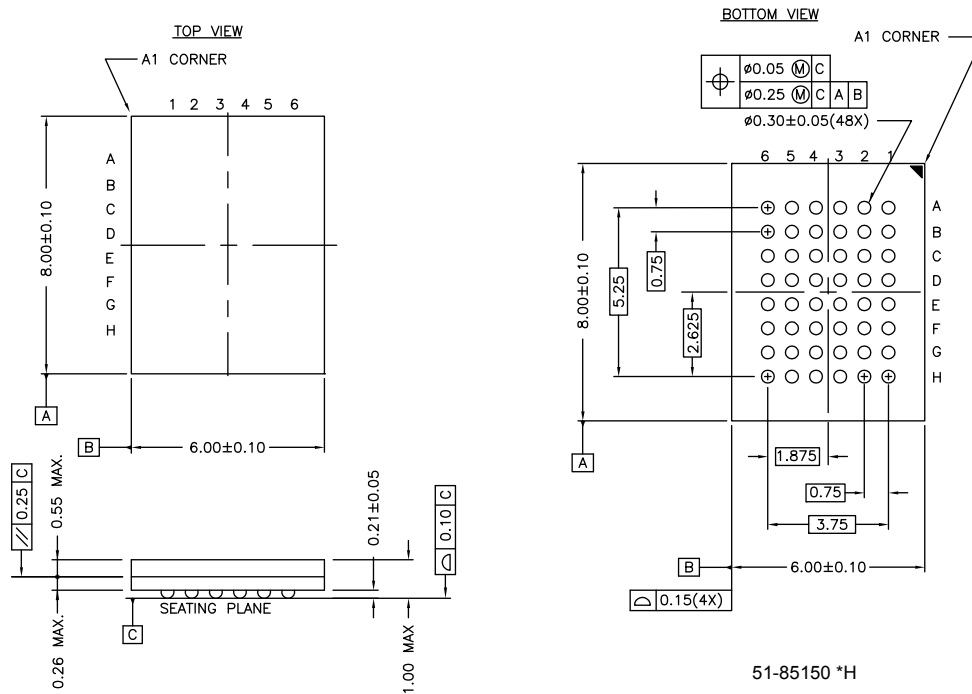


Figure 12. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



## Acronyms

| Acronym                | Description                             |
|------------------------|-----------------------------------------|
| CMOS                   | Complementary Metal Oxide Semiconductor |
| $\overline{\text{CE}}$ | Chip Enable                             |
| I/O                    | Input/Output                            |
| $\overline{\text{OE}}$ | Output Enable                           |
| SRAM                   | Static Random Access Memory             |
| TSOP                   | Thin Small Outline Package              |
| TTL                    | Transistor-Transistor Logic             |
| VFBGA                  | Very Fine-Pitch Ball Grid Array         |
| $\overline{\text{WE}}$ | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μs     | microsecond     |
| μA     | microampere     |
| mA     | milliampere     |
| ns     | nanosecond      |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History

| Document Title: CY7C1011DV33, 2-Mbit (128 K × 16) Static RAM<br>Document Number: 38-05609 |         |            |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                      | ECN No. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| **                                                                                        | 250650  | See ECN    | RKF             | New data sheet.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| *A                                                                                        | 399070  | See ECN    | NXR             | <p>Changed from Advance to Preliminary</p> <p>Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed TQFP Package from product offering</p> <p>Removed –15 speed bin</p> <p>Corrected DC voltage limits in maximum ratings section from –0.5 to –0.3V and <math>V_{CC} + 0.5V</math> to <math>V_{CC} + 0.3V</math></p> <p>Redefined <math>I_{CC}</math> values for Com'l and Ind'l temperature ranges</p> <p><math>I_{CC}</math> (Com'l): Changed from 100, 80 and 70 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively</p> <p><math>I_{CC}</math> (Ind'l): Changed from 80 and 70 mA to 90 and 85 mA for 10 and 12ns speed bins respectively</p> <p>Modified Note# 4 on AC Test Loads</p> <p>Added Static Discharge Voltage and latch-up current spec</p> <p>Added <math>V_{IH(max)}</math> spec in Note# 2</p> <p>Changed reference voltage level for measurement of Hi-Z parameters from <math>\pm 500</math> mV to <math>\pm 200</math> mV</p> <p>Added Data Retention Characteristics Table and footnote on <math>t_R</math></p> <p>Added Write Cycle (WE Controlled, OE HIGH During Write) Timing Diagram</p> <p>Changed package name for 44-pin TSOP II from Z to ZS</p> <p>Added 8 ns parts in the Ordering Information table</p> <p>Shaded Ordering Information Table</p> |
| *B                                                                                        | 459073  | See ECN    | NXR             | <p>Converted Preliminary to Final.</p> <p>Removed –8 and –12 Speed bins</p> <p>Removed Commercial Operating Range from product offering.</p> <p>Changed the description of <math>I_{IX}</math> from "Input Load Current" to "Input Leakage Current"</p> <p>Updated the Thermal Resistance table.</p> <p>Changed <math>t_{HZBE}</math> from 5 ns to 6 ns.</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Added footnote #12.</p> <p>Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| *C                                                                                        | 480177  | See ECN    | VKN             | Added -10BVI product ordering code in the Ordering Information table.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| *D                                                                                        | 3059162 | 10/14/2010 | PRAS            | <p>Added <a href="#">Ordering Code Definitions</a>.</p> <p>Updated <a href="#">Package Diagrams</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *E                                                                                        | 3098812 | 12/01/2010 | PRAS            | <p>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a>.</p> <p>Minor edits and updated in new template.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *F                                                                                        | 3861347 | 01/08/2013 | TAVA            | <p>Updated <a href="#">Ordering Information</a> (Updated part numbers).</p> <p>Updated <a href="#">Package Diagrams</a>:</p> <p>spec 51-85087 – Changed revision from *C to *E.</p> <p>spec 51-85150 – Changed revision from *F to *H.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| *G                                                                                        | 4187715 | 11/10/2013 | MEMJ            | <p>Updated in new template.</p> <p>Completing Sunset Review.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Document History** *(continued)*

| Document Title: CY7C1011DV33, 2-Mbit (128 K × 16) Static RAM<br>Document Number: 38-05609 |         |            |                 |                                                                                                                                                                                                                                                                                                                     |
|-------------------------------------------------------------------------------------------|---------|------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                      | ECN No. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                               |
| *H                                                                                        | 4567909 | 11/12/2014 | MEMJ            | <p>Updated <a href="#">Functional Description</a>:<br/>Added “For a complete list of related resources, <a href="#">click here</a>.” at the end.</p> <p>Updated <a href="#">Switching Waveforms</a>:<br/>Added Note 23 and referred the same note in <a href="#">Figure 10</a>.</p> <p>Competing Sunset Review.</p> |



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