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8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

Features

■ Ultra-low standby current

Typical standby current: 5.5 μA

Maximum standby current: 16 μA

■ High speed: 45 ns

■ Voltage range: 2.2 V to 3.6 V

 \blacksquare Embedded Error-Correcting Code (ECC) for single-bit error

correction

■ 1.0 V data retention

■ Transistor-transistor logic (TTL) compatible inputs and outputs

■ Available in Pb-free 48-ball VFBGA and 48-pin TSOP I

packages

Functional Description

CY62157H is a high-performance CMOS low-power (MoBL) SRAM device with Embedded Error-Correcting Code. ECC logic can detect and correct single bit error in accessed location.

This device is offered in dual chip enable option. Dual chip enable $\underline{\text{dev}}$ ices are accessed by asserting both chip enable inputs – $\overline{\text{CE}}_1$ as LOW and $\overline{\text{CE}}_2$ as HIGH.

 $\overline{\text{Data}}$ writes are performed by asserting the Write Enable input (WE LOW), and providing the data and address on device data (I/O₀ through I/O₁₅) and address (A₀ through A₁₈) pins respectively. The Byte High/Low Enable (BHE, BLE) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O₈ through I/O₁₅ and BLE controls I/O₀ through I/O₇.

Data reads are performed by asserting the Output Enable (\overline{OE}) input and providing the required address on the address lines. Read data is accessible on I/O lines (I/O $_0$ through I/O $_{15}$). Byte accesses can be performed by asserting the required byte enable signal (BHE, BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O₀ through I/O₁₅) are p<u>lace</u>d in a high impedance state when the device is deselected (\overline{CE}_1 HIGH / \overline{CE}_2 LOW for <u>dual chip</u> enable device), or control signals are de-asserted (\overline{OE} , \overline{BLE} , BHE).

These devices also have a unique "Byte Power down" feature, where, if both the Byte Enables (BHE and BLE) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enable(s), thereby saving power.

The CY62157H device is available in a Pb-free 48-ball VFBGA and 48-pin TSOP I packages. The logic block diagram is on page 2.

Product Portfolio

	Features and					Power Di	ssipation			
Dua duat	Options	D	V D (10)	0		I _{CC} , (mA)	Standby, I _{SB2} (µA)			
Product	(see the Pin Configurations	Range	V _{CC} Range (V)	Speed (ns)	f = 1	f _{max}	Stariuby,	, ISB2 (PA)		
	section)	T [1] Mac.	Max	Typ [1]	Max					
CY62157H30	Dual Chip Enable	Industrial	2.2 V-3.6 V	45	29	36	5.5	16		

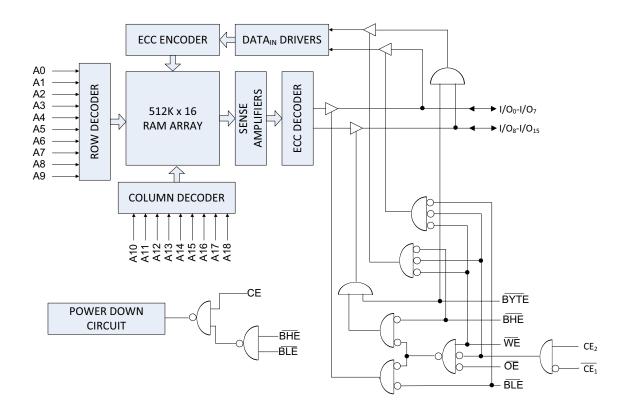
Note

Revised February 8, 2018

^{1.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.



Logic Block Diagram





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Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1mm) pinout [2]

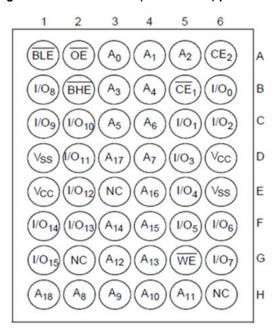
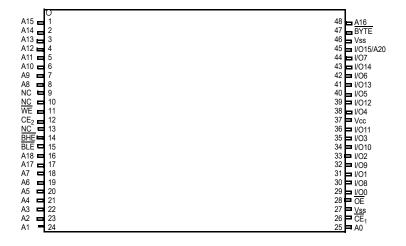


Figure 2. 48-pin TSOP I pinout (Dual Chip Enable) $^{[2,\ 3]}$



Notes

- 2. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- 3. Tie the BYTE pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, Pin 45 is the extra address line A20, while BHE, BLE, and I/O₈ to I/O₁₄ pins are not used and can be left floating.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature-65 °C to + 150 °C Ambient temperature Supply voltage

DC input voltage [4]	–0.2 V to V _{CC} + 0.3 V
Output current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	>2001 V
Latch-up current	>140 mA

Operating Range

Grade	Ambient Temperature	V _{CC}	
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V	

DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

D	D		Took Conditions			11!4		
Parameter	Desc	ription	Test Conditio	ns	Min	Typ ^[5]	Max	Unit
V _{OH}	Output HIGH	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = -0.1 mA	V _{CC} = Min, I _{OH} = -0.1 mA		_	_	V
	voltage	2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = -1.0 mA		2.4	_	_	
V_{OL}	Output LOW	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		_	_	0.4	V
	voltage	2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		_	_	0.4	
V _{IH}	Input HIGH	2.2 V to 2.7 V	_		1.8	_	V _{CC} + 0.3	V
	voltage	2.7 V to 3.6 V	_		2	_	V _{CC} + 0.3	
V_{IL}	Input LOW	2.2 V to 2.7 V	_		-0.3	_	0.6	V
	voltage ^[4]	2.7 V to 3.6 V	-		-0.3	_	0.8	
I _{IX}	Input leakage current		$GND \leq V_{IN} \leq V_{CC}$		-1	_	+1	μΑ
I _{OZ}	Output leakage current		$GND \le V_{OUT} \le V_{CC}$, Output disabled		-1	_	+1	μΑ
I _{CC}	V _{CC} operating s	upply current	$V_{CC} = Max$, $f =$	f _{MAX}	_	29.0	36.0	mA
			I _{OUT} = 0 mA, CMOS levels	1 MHz	_	7.0	9.0	mA
I _{SB1} ^[6]	Automatic power down current – CMOS inputs; V _{CC} = 2.2 to 3.6 V		$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V or CE}_2$ $(\overline{\text{BHE}} \text{ and } \overline{\text{BLE}}) \ge \text{V}_{\text{CC}} - 0.2 \text{ V}$ $\text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V}$, $\text{V}_{\text{IN}} \le 0.2 \text{ V}$ $\text{F} = \text{F}_{\text{max}}$ (address and data of $\text{F} = 0$), $\text{CO} = 0.2 \text{ V}$	1.2 V, 1.2 V, 1.2 V, 1.3 only),	-	5.5	16.0	μА
I _{SB2} ^[6]	Automatic powe current – CMOS V _{CC} = 2.2 to 3.6	S inputs	$\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V or}$ $CE_2 \le 0.2 \text{ V,}$ $(\overline{BHE} \text{ and } \overline{BLE}) \ge V_{CC} - 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V or}$ $V_{IN} \le 0.2 \text{ V,}$ $f = 0, V_{CC} = V_{CC(max)}$	25 °C ^[7] 40 °C ^[7]	-	5.5 6.3 12.0 ^[7]	6.5 8.0 16.0	μА

^{4.} V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 20 ns.
5. Typical values <u>are</u> included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.
6. Chip enables (CE₁ and CE₂) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
7. The I_{SB2} limits at 25 °C, 70 °C, 40 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.



Capacitance

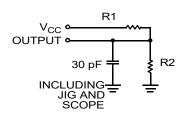
Parameter [8]	Description	Description Test Conditions		Unit
C _{IN}	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output capacitance		10	pF

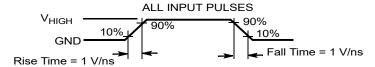
Thermal Resistance

Parame	ter [8] Description	Test Conditions	48-pin TSOP I	48-ball VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	57.99	31.50	°C/W
Θ^{JC}	Thermal resistance (junction to case)		13.42	15.75	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

OUTPUT•——W——• V

Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

^{8.} Tested initially and after any design or process changes that may affect these parameters.



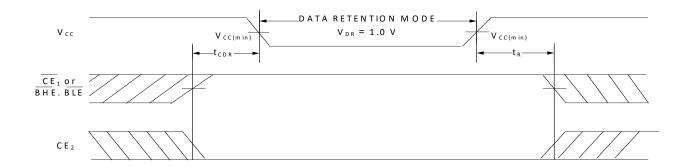
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit
V_{DR}	V _{CC} for data retention		1	_	-	V
I _{CCDR} ^[10, 11]	Data retention current	2.2 V < V _{CC} ≤ 3.6 V,	_	5.5	16.0	μА
		$\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V or } CE_2 \le 0.2 \text{ V},$				
		$(\overline{BHE} \text{ and } \overline{BLE}) \ge V_{CC} - 0.2 \text{ V},$				
		$V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$				
t _{CDR} ^[12]	Chip deselect to data retention time		0	_	-	_
t _R ^[13]	Operation recovery time		45	_	_	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [14]



- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.

 10. Chip enables (CE₁ and CE₂) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

 11. I_{CCDR} is guaranteed only after the device is firs powered up to V_{CC}(min) and then brought down to V_{DR}.

 12. Tested initially and after any design or process changes that may affect these parameters.

- Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.
 BHE BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both BHE and BLE.



Switching Characteristics

Read Cycle	Unit	ns	45	Description	Parameter [15]	
tpC Read cycle time 45 — tpAA Address to data valid — 45 toHA Data hold from address change 10 — tpCE CE1 LOW and CE2 HIGH to data valid — 45 tpDE OE LOW to data valid — 22 tpDE OE LOW to Low Z ^[16] 5 — tpDE OE HIGH to High Z ^[16, 17] — 18 tpDE OE HIGH to Low-Z ^[16] 10 — tpDE CE1 LOW and CE2 HIGH to Low-Z ^[16] 10 — tpDE CE1 HIGH and CE2 LOW to High-Z ^[16, 17] — 18 tpDE CE1 LOW and CE2 HIGH to power-up 0 — tpDE CE1 HIGH and CE2 LOW to power-down — 45 tpDE DE7 HIGH and CE2 LOW to Journal CE2 LOW to	Unit	Max	Min	Description		
tAA Address to data valid - 45 tOHA Data hold from address change 10 - tACE CE1 LOW and CE2 HIGH to data valid - 45 tDOE OE LOW to data valid - 22 tLZOE OE LOW to Low Z ^[16] 5 - tHZOE OE HIGH to High Z ^[16, 17] - 18 tLZCE CE1 LOW and CE2 HIGH to Low-Z ^[16] 10 - tHZCE CE1 HIGH and CE2 LOW to High-Z ^[16, 17] - 18 tpu CE1, LOW and CE2 HIGH to power-up 0 - tpD CE1, HIGH and CE2 LOW to power-down - 45 tpBE BLE / BHE LOW to data valid - 45 t_LZBE BLE / BHE LOW to Low-Z ^[16] 5 - t_HZBE BLE / BHE LOW to Low-Z ^[16] 5 - tHZBE BLE / BHE HIGH to High-Z ^[16, 17] - 18 Write cycle time twc Virte cycle time 35 - tSCE CE1, LOW and CE2 HIGH to write end <td></td> <td></td> <td></td> <td></td> <td>Read Cycle</td>					Read Cycle	
Total Data hold from address change 10 - tACE CE1 LOW and CE2 HIGH to data valid - 45 tDOE OE LOW to data valid - 22 tLZOE OE LOW to Low Z ^[16] 5 - tHZOE OE HIGH to High Z ^[16, 17] - 18 tLZCE CE1 LOW and CE2 HIGH to LOW-Z ^[16] 10 - tHZCE CE1 HIGH and CE2 LOW to High-Z ^[16, 17] - 18 tpu CE1 LOW and CE2 HIGH to power-up 0 - tpD CE1 HIGH and CE2 LOW to power-down - 45 tpD CE1 HIGH and CE2 LOW to data valid - 45 t_LZBE BLE / BHE LOW to Low-Z ^[16] 5 - t_LZBE BLE / BHE HIGH to High-Z ^[16, 17] - 18 Write Cycle [18, 19] 5 - - twc Write cycle time 45 - tsCE CE1 LOW and CE2 HIGH to write end 35 - tpW Address setup to write end 35 -	ns	_	45	Read cycle time	t _{RC}	
tACE CE1 LOW and CE2 HIGH to data valid - 45 tDOE OE LOW to data valid - 22 tLZOE OE LOW to Low Z ^[16] 5 - tHZOE OE HIGH to High Z ^[16, 17] - 18 tLZCE CE1 LOW and CE2 HIGH to LOW-Z ^[16] 10 - tHZCE CE1 HIGH and CE2 LOW to High-Z ^[16, 17] - 18 tpu CE1 LOW and CE2 HIGH to power-up 0 - tpD CE1 HIGH and CE2 LOW to power-down - 45 tDBE BLE / BHE LOW to data valid - 45 tLZBE BLE / BHE LOW to Low-Z ^[16] 5 - tHZBE BLE / BHE HIGH to High-Z ^[16, 17] - 18 Write Cycle [^{18, 19]} - 18 tWC Write cycle time 45 - tSCE CE1 LOW and CE2 HIGH to write end 35 - tAW Address setup to write end 35 - tPWE WE pulse width 35 - tBW BLE / BHE LOW	ns	45	-	Address to data valid	t _{AA}	
tDDE DE LOW to data valid − 22 tLZOE DE LOW to Low Z ^[16] 5 − tHZOE DE HIGH to High Z ^[16, 17] − 18 tLZCE CE₁ LOW and CE₂ HIGH to Low-Z ^[16] 10 − tHZCE CE₁ HIGH and CE₂ LOW to High-Z ^[16, 17] − 18 tpu CE₁ LOW and CE₂ HIGH to power-up 0 − tpD CE₁ HIGH and CE₂ LOW to power-down − 45 tDBE BLE / BHE LOW to data valid − 45 tLZBE BLE / BHE LOW to Low-Z ^[16] 5 − tHZBE BLE / BHE HIGH to High-Z ^[16, 17] − 18 Write Cycle [¹18, ¹19] ± − 18 Write Cycle [¹18, ¹19] ± − 18 Write Cycle [¹18, ¹19] − 18 LyC Write cycle time 45 − tSCE	ns	_	10	Data hold from address change	t _{OHA}	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ns	45	-	CE ₁ LOW and CE ₂ HIGH to data valid	t _{ACE}	
tHZOE OE HIGH to High Z[16, 17] − 18 tLZCE CE₁ LOW and CE₂ HIGH to Low-Z[16] 10 − tHZCE CE₁ HIGH and CE₂ LOW to High-Z[16, 17] − 18 tpU CE₁ LOW and CE₂ HIGH to power-up 0 − tpD CE₁ HIGH and CE₂ LOW to power-down − 45 tDBE BLE / BHE LOW to data valid − 45 tLZBE BLE / BHE LOW to Low-Z[16] 5 − tHZBE BLE / BHE HIGH to High-Z[16, 17] − 18 Write Cycle [18, 19] ± − 45 − tWC Write cycle time 45 − − twc Write cycle time 45 − − t _{AW} Address setup to write end 35 − t _{HA} Address setup to write end 0 − t _{SA} Address setup to write end 35 − t _{BW} BLE / BHE LOW to write end 35 − t _{BD} Data hold from write end 0 −	ns	22	_	OE LOW to data valid	t _{DOE}	
t_ZCE CE1 LOW and CE2 HIGH to Low-Z[16] 10 - t_HZCE CE1 HIGH and CE2 LOW to High-Z[16, 17] - 18 tpu CE1 LOW and CE2 HIGH to power-up 0 - tpD CE1 HIGH and CE2 LOW to power-down - 45 t_DBE BLE / BHE LOW to data valid - 45 t_ZBE BLE / BHE LOW to Low-Z[16] 5 - t_HZBE BLE / BHE HIGH to High-Z[16, 17] - 18 Write Cycle [18, 19] - 18 twc Write cycle time 45 - t_SCE CE1 LOW and CE2 HIGH to write end 35 - t_AW Address setup to write end 35 - t_HA Address setup to write end 0 - t_BW BLE / BHE LOW to write end 35 - t_BW BLE / BHE LOW to write end 25 - t_HD Data hold from write end 0 -	ns	_	5	OE LOW to Low Z ^[16]	t _{LZOE}	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ns	18	_	OE HIGH to High Z ^[16, 17]	t _{HZOE}	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ns	_	10		t _{LZCE}	
tpD CE1 HIGH and CE2 LOW to power-down - 45 tDBE BLE / BHE LOW to data valid - 45 tLZBE BLE / BHE LOW to Low-Z ^[16] 5 - tHZBE BLE / BHE HIGH to High-Z ^[16, 17] - 18 Write Cycle [18, 19] - 18 tWC Write cycle time 45 - tSCE CE1 LOW and CE2 HIGH to write end 35 - tAW Address setup to write end 35 - tHA Address hold from write end 0 - tSA Address setup to write start 0 - tBW BLE / BHE LOW to write end 35 - tBW BLE / BHE LOW to write end 25 - tBD Data hold from write end 0 -	ns	18	_	CE ₁ HIGH and CE ₂ LOW to High-Z ^[16, 17]	t _{HZCE}	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ns	_	0	CE ₁ LOW and CE ₂ HIGH to power-up	t _{PU}	
tLZBE BLE / BHE LOW to Low-Z ^[16] 5 - tHZBE BLE / BHE HIGH to High-Z ^[16, 17] - 18 Write Cycle [18, 19] twc Write cycle time 45 - tSCE CE1 LOW and CE2 HIGH to write end 35 - tAW Address setup to write end 35 - tHA Address hold from write end 0 - tSA Address setup to write start 0 - tPWE WE pulse width 35 - tBW BLE / BHE LOW to write end 35 - tBD Data setup to write end 25 - tHD Data hold from write end 0 -	ns	45	_	CE ₁ HIGH and CE ₂ LOW to power-down	t _{PD}	
t _{HZBE} BLE / BHE HIGH to High-Z ^[16, 17] – 18 Write Cycle [18, 19] t _{WC} Write cycle time 45 – t _{SCE} CE ₁ LOW and CE ₂ HIGH to write end 35 – t _{AW} Address setup to write end 35 – t _{HA} Address hold from write end 0 – t _{SA} Address setup to write start 0 – t _{PWE} WE pulse width 35 – t _{BW} BLE / BHE LOW to write end 35 – t _{SD} Data setup to write end 25 – t _{HD} Data hold from write end 0 –	ns	45	_		t _{DBE}	
Write Cycle [18, 19] t _{WC} Write cycle time 45 — t _{SCE} CE ₁ LOW and CE ₂ HIGH to write end 35 — t _{AW} Address setup to write end 35 — t _{HA} Address hold from write end 0 — t _{SA} Address setup to write start 0 — t _{PWE} WE pulse width 35 — t _{BW} BLE / BHE LOW to write end 35 — t _{SD} Data setup to write end 25 — t _{HD} Data hold from write end 0 —	ns	_	5			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ns	18	_	BLE / BHE HIGH to High-Z ^[16, 17]	t _{HZBE}	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$					Write Cycle [18, 19	
tAW Address setup to write end 35 - tHA Address hold from write end 0 - tSA Address setup to write start 0 - tPWE WE pulse width 35 - tBW BLE / BHE LOW to write end 35 - tSD Data setup to write end 25 - tHD Data hold from write end 0 -	ns	_	45	Write cycle time	t _{WC}	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ns	_	35	CE ₁ LOW and CE ₂ HIGH to write end	t _{SCE}	
tsA Address setup to write start 0 - tpWE WE pulse width 35 - tbW BLE / BHE LOW to write end 35 - tsD Data setup to write end 25 - thD Data hold from write end 0 -	ns	_	35	Address setup to write end	t _{AW}	
tpWE WE pulse width 35 - tBW BLE / BHE LOW to write end 35 - tSD Data setup to write end 25 - tHD Data hold from write end 0 -	ns	_	0	Address hold from write end	t _{HA}	
t _{BW} BLE / BHE LOW to write end 35 - t _{SD} Data setup to write end 25 - t _{HD} Data hold from write end 0 -	ns	_	0	Address setup to write start	t _{SA}	
t _{SD} Data setup to write end 25 – t _{HD} Data hold from write end 0 –	ns	_	35	WE pulse width	t _{PWE}	
t _{HD} Data hold from write end 0 -	ns	_	35	BLE / BHE LOW to write end	t _{BW}	
	ns	_	25	Data setup to write end	t _{SD}	
	ns	_	0	Data hold from write end	t _{HD}	
t_{HZWE} WE LOW to High-Z ^[16, 17] – 18	ns	18	_	WE LOW to High-Z ^[16, 17]	t _{HZWE}	
t _{LZWE} WE HIGH to Low-Z ^[16] 10 –	ns	_	10	WE HIGH to Low-Z ^[16]	t _{LZWE}	

^{15.} Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V_{CC} ≥ 3 V) and V_{CC}/2 (for V_{CC} < 3 V), and input pulse levels of 0 to 3 V (for V_{CC} ≥ 3 V) and 0 to V_{CC} (for V_{CC} < 3V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified

^{16.} At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZDE}, t_{HZDE} is less than t_{LZDE}, and t_{HZWE} is less than t_{LZWE} for any device.

17. t_{HZCE}, t_{HZDE}, t_{HZDE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

18. The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

^{19.} The minimum write cycle pulse width for Write Cycle No. 1 (WE Controlled, OE LOW) should be equal to the sum of t_{HZWE} and t_{SD}.



Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62157H (Address Transition Controlled) [20, 21]

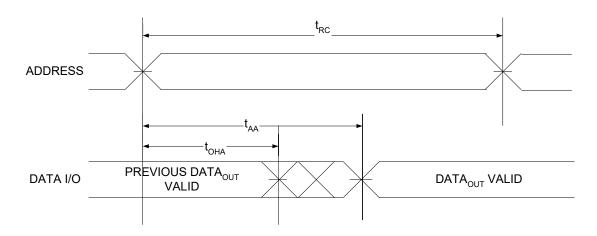
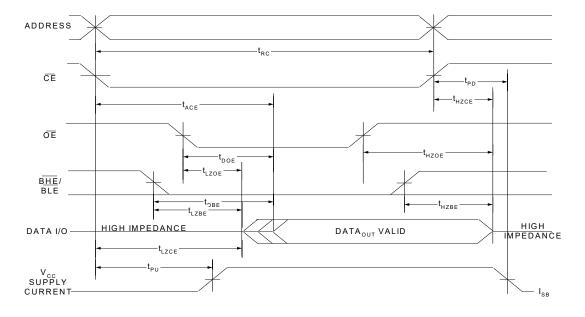


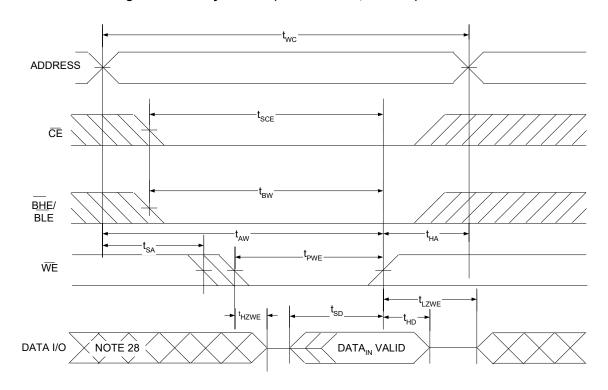
Figure 6. Read Cycle No. 2 (OE Controlled) [21, 22, 23]



- Notes 20. The device is continuously selected. $\overline{OE} = V_{|L}$, $\overline{CE} = V_{|L}$, \overline{BHE} or \overline{BLE} or both = $V_{|L}$.
- 21. WE is HIGH for read cycle.
- 22. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and \overline{CE}_2 . When \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW, \overline{CE} is HIGH.
- 23. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.



Figure 7. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [24, 25, 26, 27]



Notes

^{24.} For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$. When $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or $\overline{\text{CE}}_2$ is LOW, $\overline{\text{CE}}_1$ is HIGH.

^{25.} The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

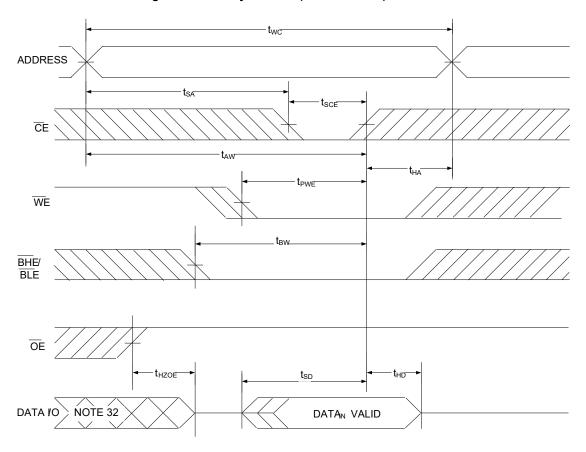
^{26.} Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

^{27.} The minimum write cycle pulse width for Write Cycle No. 1 (WE Controlled, OE LOW) should be equal to the sum of t_{HZWE} and t_{SD}.

^{28.} During this period the I/Os are in output state. Do not apply input signals.



Figure 8. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [29, 30, 31]



^{29. &}lt;u>For</u> all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and \overline{CE}_2 . When \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW, \overline{CE} is HIGH.

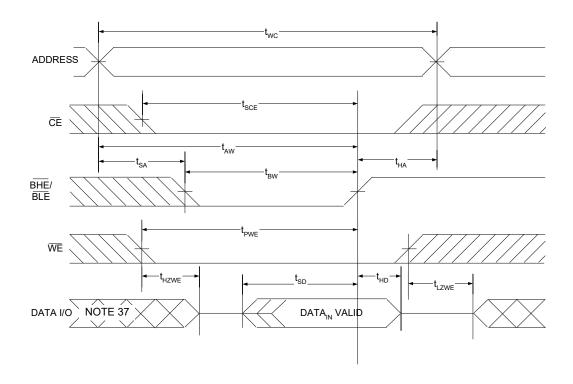
^{30.} The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

^{31.} Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

^{32.} During this period the I/Os are in output state. Do not apply input signals.



Figure 9. Write Cycle No. 3 (BHE/BLE controlled, OE LOW) [33, 34, 35, 36]



^{33.} For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$. When $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or $\overline{\text{CE}}_2$ is LOW, $\overline{\text{CE}}_1$ is HIGH.

^{34.} The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

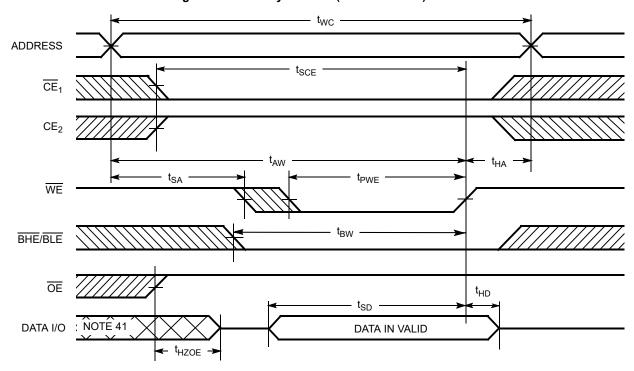
^{35.} Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

36. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

^{37.} During this period the I/Os are in output state. Do not apply input signals.



Figure 10. Write Cycle No. 4 ($\overline{\text{WE}}$ Controlled) $^{[38,\ 39,\ 40]}$



^{38.} The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, BHE or BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

39. Data I/O is high impedance if OE = V_{IH}.

^{40.} If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}}$ = V_{IH} , the output remains in a high impedance state.

^{41.} During this period the I/Os are in output state. Do not apply input signals.



Truth Table - CY62157H

CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	X ^[42]	Х	Х	Х	Х	High-Z	Deselect/Power-down	Standby (I _{SB})
X ^[42]	L	Х	Х	Х	Х	High-Z	Deselect/Power-down	Standby (I _{SB})
X ^[42]	X ^[42]	Х	Х	Н	Н	High-Z	Deselect/Power-down	Standby (I _{SB})
L	Н	Н	L	L	L	Data Out (I/O ₀ -I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	L	Н	L	Data Out (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	L	L	Н	High Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	L	Х	L	L	Data In (I/O ₀ -I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	Н	L	Data In (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	L	Н	High-Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	Н	L	Х	Х	Data Out (I/O ₀ –I/O ₇)	Read	Active (I _{CC})
L	Н	Н	Н	Х	Х	High-Z	Output disabled	Active (I _{CC})
L	Н	L	Х	Х	Х	Data In (I/O ₀ –I/O ₇)	Write	Active (I _{CC})

Note

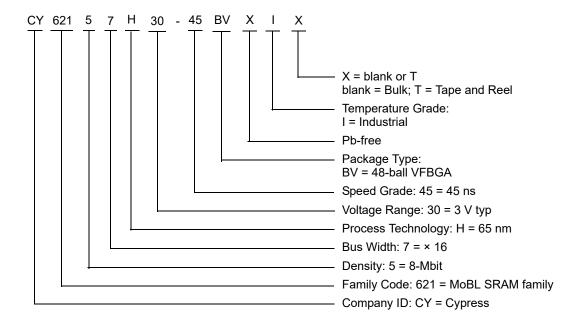
^{42.} The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157H30-45BVXI	51-85150 48-ball VFBGA (6 × 8 × 1 mm) (Pb-free),		Industrial
	CY62157H30-45BVXIT		Package Code: BZ48	

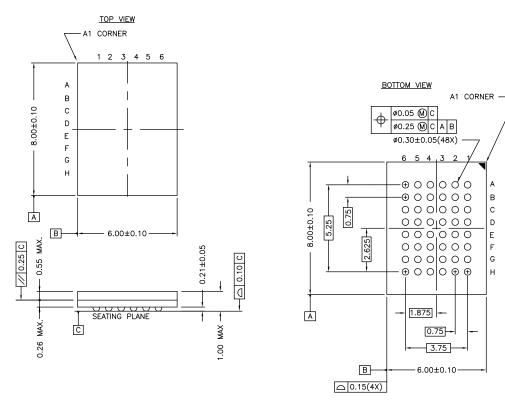
Ordering Code Definitions





Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



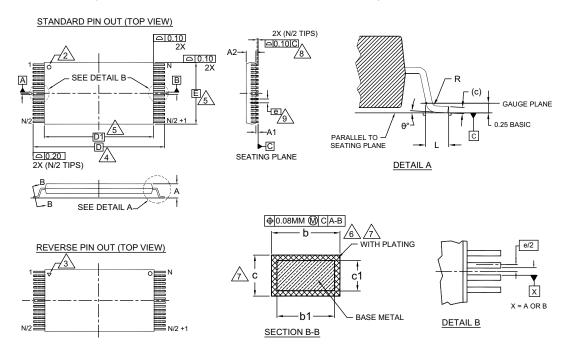
NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
posted on the Cypress web.

51-85150 *H



Package Diagrams (continued)

Figure 12. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
STIVIBOL	MIN.	NOM.	MAX.
А	_	_	1.20
A1	0.05	_	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	-	0.16
С	0.10	_	0.21
D	20.00 BASIC		SIC
D1	18.40 BASIC		C
E	12.00 BASIC		
е	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	_	8
R	0.08	_	0.20
N	48		

NOTES:

DIMENSIONS ARE IN MILLIMETERS (mm).

2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).

PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.

TO BE DETERMINED AT THE SEATING PLANE [-C-]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.

DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.

DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF 6 DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.

THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.

DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F



Acronyms

Acronym	Description		
BHE	byte high enable		
BLE	byte low enable		
CE	chip enable		
CMOS complementary metal oxide semiconductor			
I/O	input/output		
OE	output enable		
SRAM	static random access memory		
VFBGA	very fine-pitch ball grid array		
WE	write enable		

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	Degrees Celsius		
MHz	megahertz		
μΑ	microamperes		
μS	microseconds		
mA	milliamperes		
mm	millimeters		
ns	nanoseconds		
Ω	ohms		
%	percent		
pF	picofarads		
V	volts		
W	watts		



Document History Page

	Document Title: CY62157H MoBL [®] , 8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-88316					
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change		
*B	4983842	NILE	10/23/2015	Changed status from Preliminary to Final.		
*C	5109716	NILE	01/27/2016	Updated DC Electrical Characteristics: Changed minimum value of V_{OH} parameter from 2.2 V to 2.4 V corresponding to V_{CC} Operating Range "2.7 V to 3.6 V" and Test Condition " V_{CC} = Min, I_{OH} = -1.0 mA".		
*D	5427485	VINI	09/06/2016	Updated Maximum Ratings: Updated Note 4 (Replaced "2 ns" with "20 ns"). Updated DC Electrical Characteristics: Changed minimum value of V _{IH} parameter from 2.0 V to 1.8 V corresponding to the Operating Range "2.2 V to 2.7 V". Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.		
*E	6063494	VINI	02/08/2018	Updated Package Diagrams: spec 51-85183 – Changed revision from *D to *F. Updated to new template.		



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