# 8-Mbit (512K × 16) Static RAM

## Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical Standby current: 2 µA
  - Maximum Standby current: 8 µA
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

## Functional Description

The CY62157ESL is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}$ HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input or output pins ($I/O_0$ through $I/O_{15}$) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both the Byte High Enable and the Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during an active write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

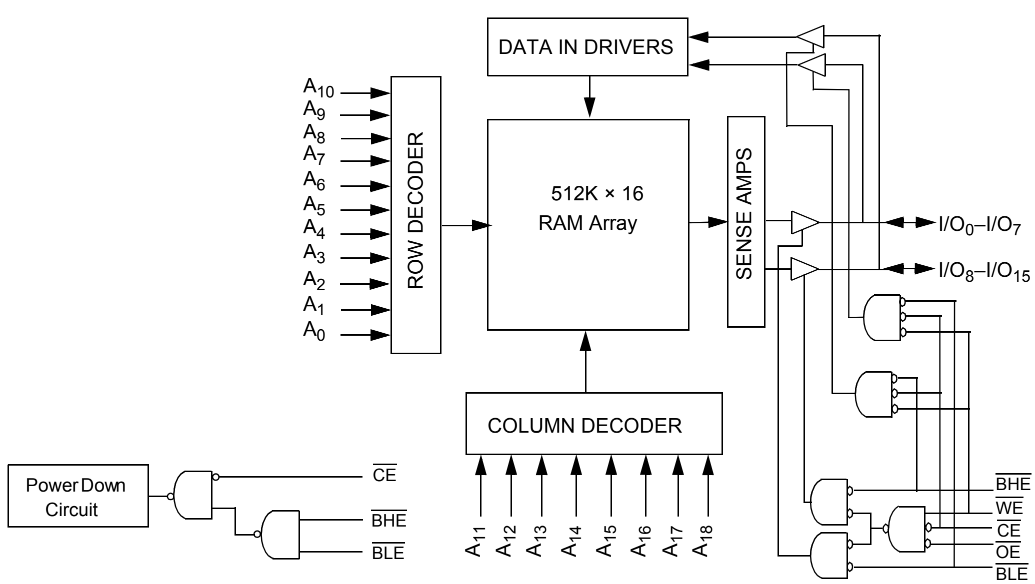
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$) is written into the location specified on the address pins ($A_0$ through $A_{18}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{18}$).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on $I/O_8$ to $I/O_{15}$. See the Truth Table on page 11 for a complete description of read and write modes.

The CY62157ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

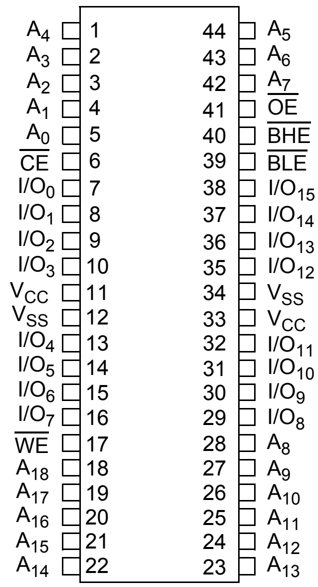
## Logic Block Diagram



## Contents

## Pin Configurations

**Figure 1. 44-pin TSOP II pinout (Top View)**




## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) [1] | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Operating $I_{CC}$, (mA) | | | | Standby, $I_{SB2}$ (µA) | |
| | | | | f = 1MHz | | f = $f_{max}$ | | | |
| | | | | Typ [2] | Max | Typ [2] | Max | Typ [2] | Max |
| CY62157ESL | Industrial | 2.2 V–3.6 V and 4.5 V–5.5 V | 45 | 1.8 | 3 | 18 | 25 | 2 | 8 |

**Notes**
1. Datasheet specifications are not guaranteed for $V_{CC}$ in the range of 3.6 V to 4.5 V.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 3 V, and $V_{CC}$ = 5 V, $T_A$ = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .............................. –65 °C to +150 °C

Ambient Temperature with Power Applied ........................................ –55 °C to +125 °C

Supply Voltage to Ground Potential ...............–0.5 V to 6.0 V

DC Voltage Applied to Outputs in High Z State [3, 4] .......................................–0.5 V to 6.0 V

DC Input Voltage [3, 4] ...................................–0.5 V to 6.0 V

Output Current into Outputs (LOW) ............................ 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ................................. >2001 V

Latch up Current ..................................................... >200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ [5] |
|---|---|---|---|
| CY62157ESL | Industrial | –40 °C to +85 °C | 2.2 V–3.6 V, and 4.5 V–5.5 V |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [6] | Max | |
| $V_{OH}$ | Output high voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OH} = –0.1$ mA | 2.0 | – | – | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OH} = –1.0$ mA | 2.4 | – | – | |
| | | $4.5 \le V_{CC} \le 5.5$ | $I_{OH} = –1.0$ mA | 2.4 | – | – | |
| | | $4.5 \le V_{CC} \le 5.5$ | $I_{OH} = –0.1$ mA | – | – | 3.4 [7] | |
| $V_{OL}$ | Output low voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OL} = 0.1$ mA | – | – | 0.4 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OL} = 2.1$ mA | – | – | 0.4 | |
| | | $4.5 \le V_{CC} \le 5.5$ | $I_{OL} = 2.1$ mA | – | – | 0.4 | |
| $V_{IH}$ | Input high voltage | $2.2 \le V_{CC} \le 2.7$ | | 1.8 | – | $V_{CC} + 0.3$ | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | 2.2 | – | $V_{CC} + 0.3$ | |
| | | $4.5 \le V_{CC} \le 5.5$ | | 2.2 | – | $V_{CC} + 0.5$ | |
| $V_{IL}$ | Input low voltage | $2.2 \le V_{CC} \le 2.7$ | | –0.3 | – | 0.6 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | –0.3 | – | 0.8 | |
| | | $4.5 \le V_{CC} \le 5.5$ | | –0.5 | – | 0.8 | |
| $I_{IX}$ | Input leakage current | $GND \le V_I \le V_{CC}$ | | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | $GND \le V_O \le V_{CC}$, Output Disabled | | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | $f = f_{max} = 1/t_{RC}$ | $V_{CC} = V_{CCmax}$ | – | 18 | 25 | mA |
| | | f = 1 MHz | $I_{OUT} = 0$ mA, CMOS levels | – | 1.8 | 3 | |
| $I_{SB1}$ [8] | Automatic CE power down current – CMOS inputs | $\overline{CE} \ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, $f = f_{max}$ (address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$ | | – | 2 | 8 | µA |
| $I_{SB2}$ [8] | Automatic CE power down current – CMOS inputs | $\overline{CE} \ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$ | | – | 2 | 8 | µA |

**Notes**

3. $V_{IL}$ (min) = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH}$ (max) = $V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to $V_{CC}$ (min) and 200 µs wait time after $V_{CC}$ stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 3 V, and $V_{CC}$ = 5 V, $T_A$ = 25 °C.
7. Please note that the maximum $V_{OH}$ limit does not exceed minimum CMOS $V_{IH}$ of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum $V_{IH}$ of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
8. Chip enable ($\overline{CE}$) needs to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.

## Capacitance

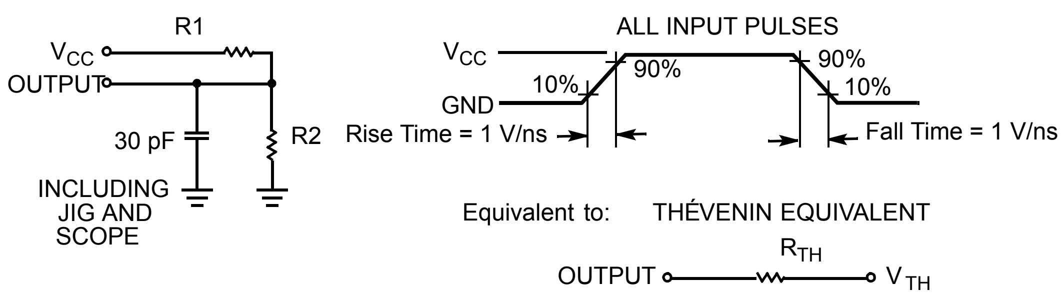
| Parameter [9] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [9] | Description | Test Conditions | TSOP II | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 57.92 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 17.44 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**




| Parameters | 2.5 V | 3.0 V | 5.0 V | Unit |
|---|---|---|---|---|
| R1 | 16667 | 1103 | 1800 | Ω |
| R2 | 15385 | 1554 | 990 | Ω |
| $R_{TH}$ | 8000 | 645 | 639 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | 1.77 | V |

**Note**
9. Tested initially and after any design or process changes that may affect these parameters.

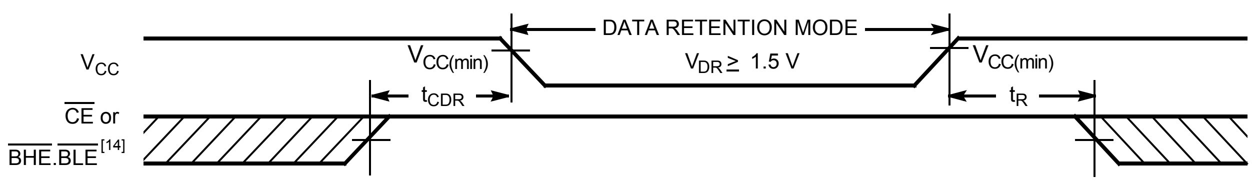
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | | Min | Typ [10] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | | 1.5 | – | – | V |
| $I_{CCDR}$ [11] | Data retention current | $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | $V_{CC}$ = 1.5 V | – | 2 | 5 | µA |
| | | | $V_{CC}$ = 2.0 V | – | 2 | 8 | |
| $t_{CDR}$ [12] | Chip deselect to data retention time | | | 0 | – | – | ns |
| $t_R$ [13] | Operation recovery time | | | 45 | – | – | ns |

## Data Retention Waveform

**Figure 3. Data Retention Waveform**




**Notes**

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 3 V, and $V_{CC}$ = 5 V, $T_A$ = 25 °C.
11. Chip enable ($\overline{CE}$) needs to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the Operating Range

| Parameter [15, 16] | Description | 45 ns | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 45 | – | ns |
| $t_{AA}$ | Address to data valid | – | 45 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [17] | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [17, 18] | – | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z [17] | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z [17, 18] | – | 18 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power down | – | 45 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to data valid | – | 45 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [17, 19] | 5 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to High Z [17, 18] | – | 18 | ns |
| **Write Cycle** [20, 21] | | | | |
| $t_{WC}$ | Write cycle time | 45 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 35 | – | ns |
| $t_{AW}$ | Address setup to write end | 35 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 35 | – | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to write end | 35 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [17, 18] | – | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [17] | 10 | – | ns |

**Notes**

15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified IOL/IOH as shown in the Figure 2 on page 5.
17. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
18. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
19. If both byte enables are toggled together, this value is 10 ns.
20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = $V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width for Write Cycle No. 4 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [22, 23]

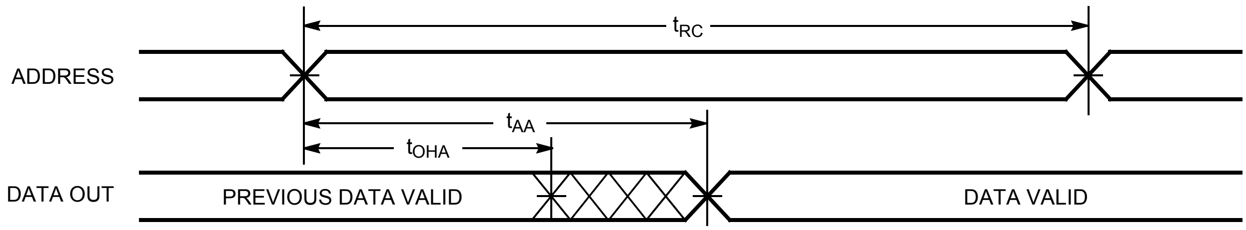
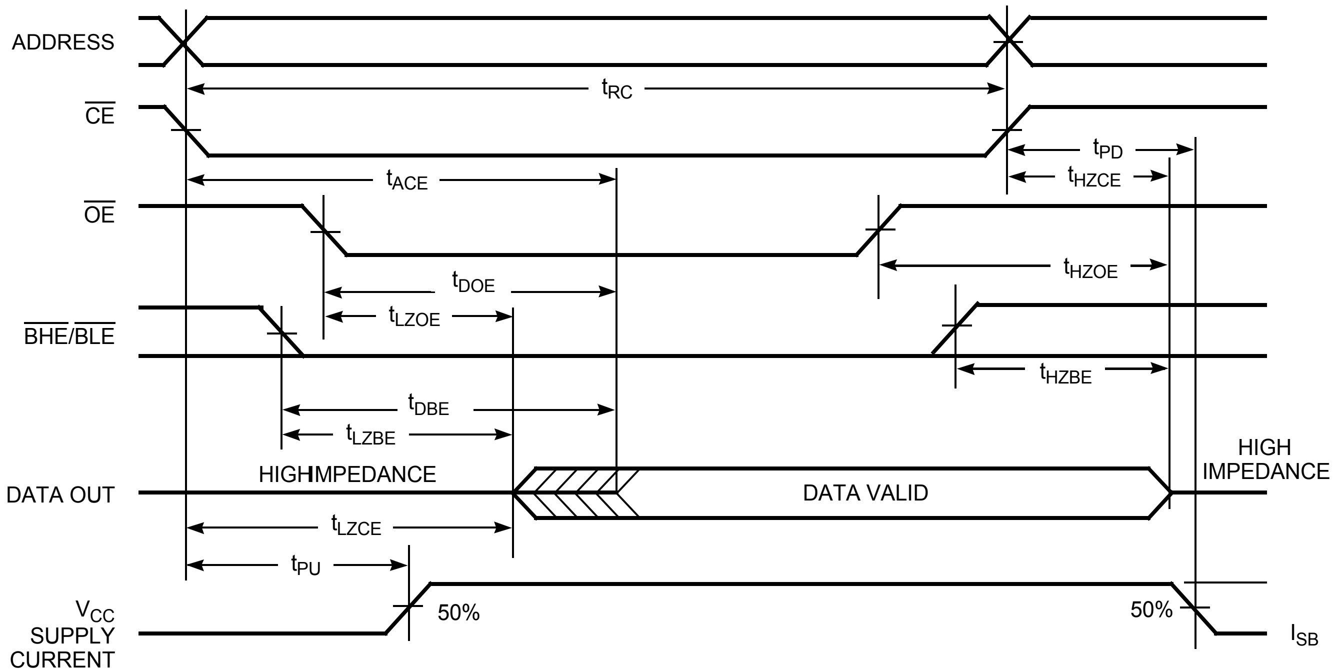



**Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [23, 24]




**Notes**
22. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$.
23. $\overline{WE}$ is HIGH for read cycle.
24. Address valid before or similar to $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled)** [25, 26]

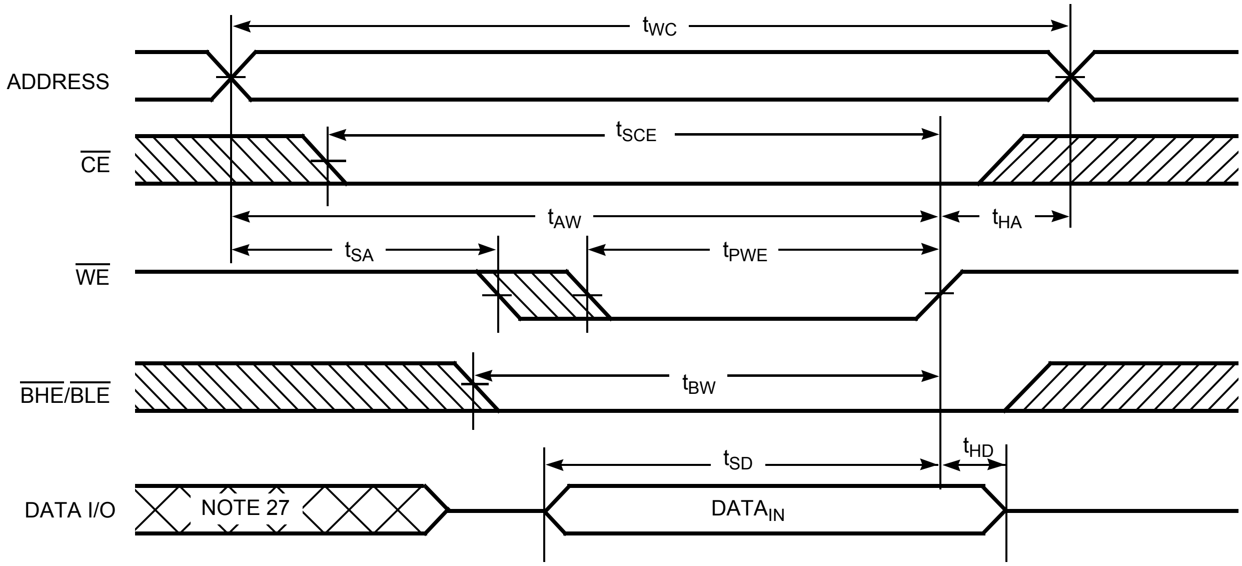
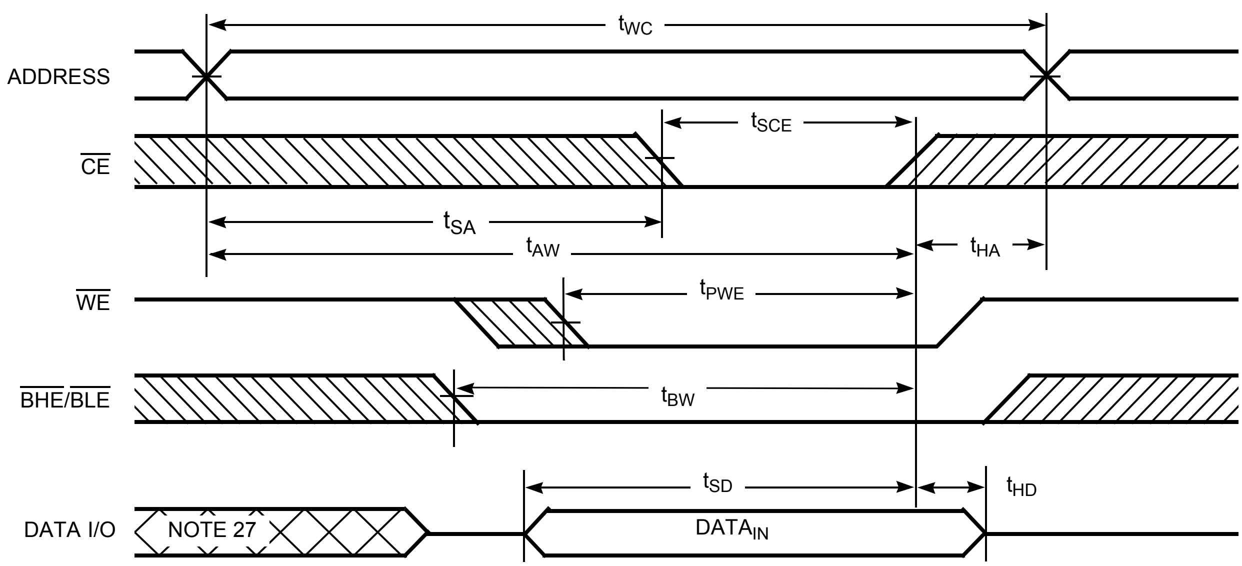



**Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled)** [25, 26]




**Notes**

25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = $V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 ($\overline{BHE}$/$\overline{BLE}$ Controlled) [28, 29]**

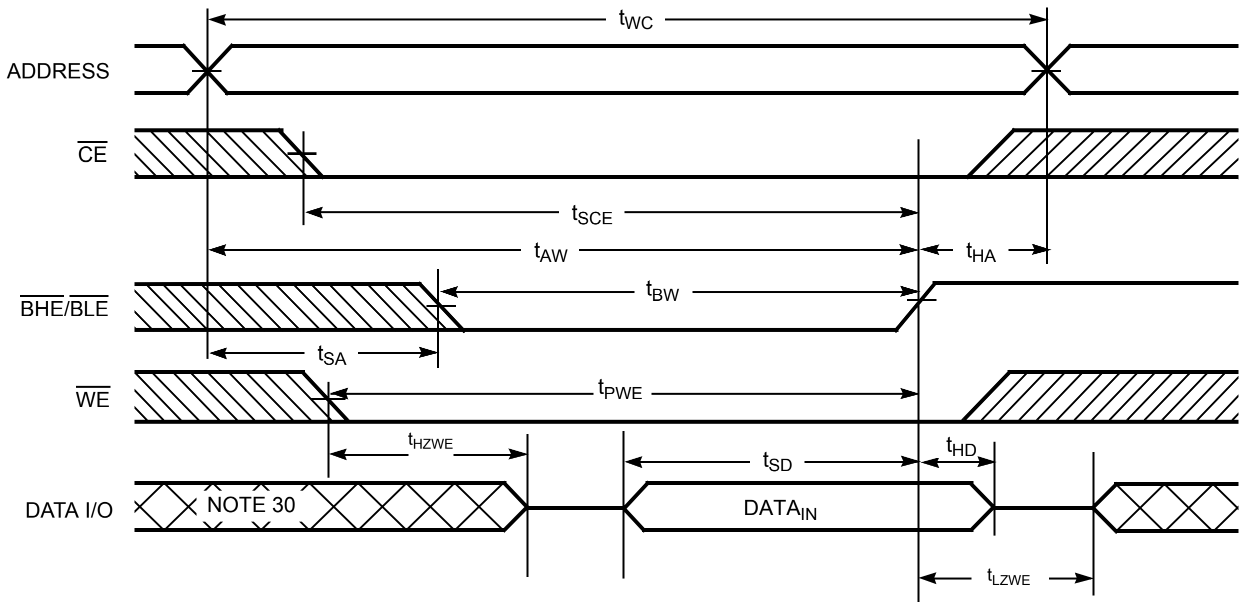
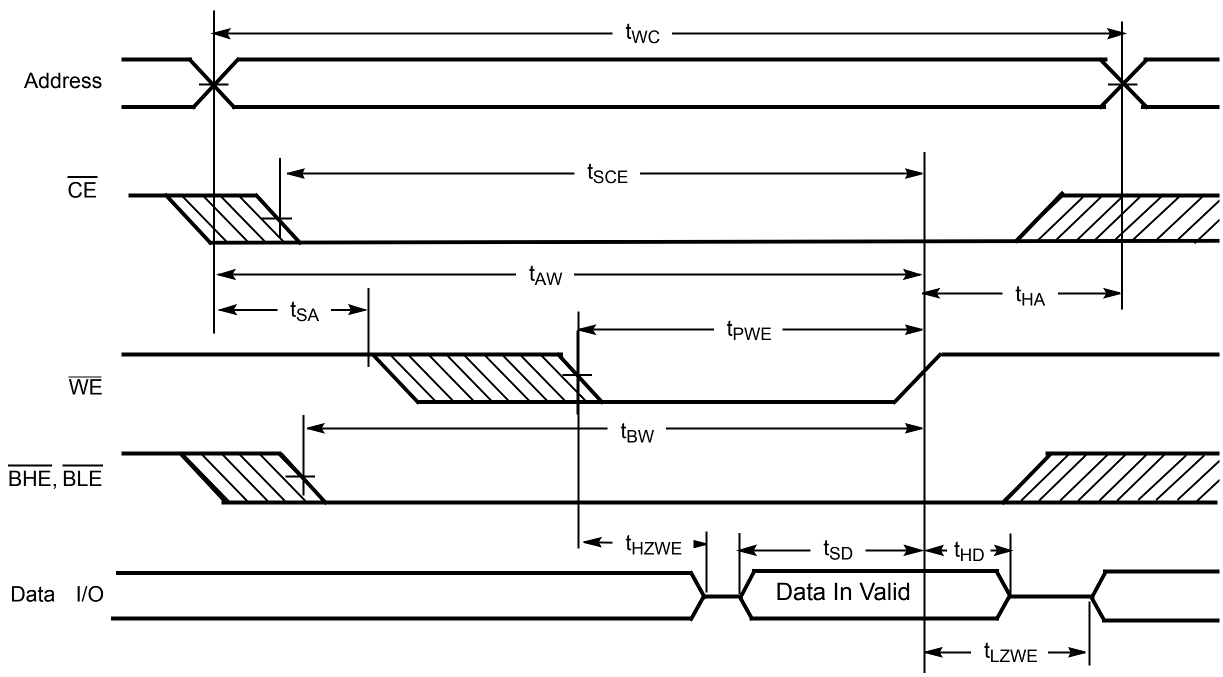



**Figure 9. Write Cycle No. 4 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [28, 29, 31]**




**Notes**

28. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = $V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
29. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
30. During this period, the I/Os are in output state. Do not apply input signals.
31. The minimum write cycle pulse width should be equal to the sum of $t_{SD}$ and $t_{HZWE}$.

## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | Deselect/power down | Standby ($I_{SB}$) |
| X[32] | X | X | H | H | High Z | Deselect/power down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data Out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data Out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High-Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High-Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High-Z | Output disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data In ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data In ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data In ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Write | Active ($I_{CC}$) |

**Note**

32. The ‘X’ (Don’t care) state for the Chip enable in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on this pin is not permitted.

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62157ESL-45ZSXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | Industrial |

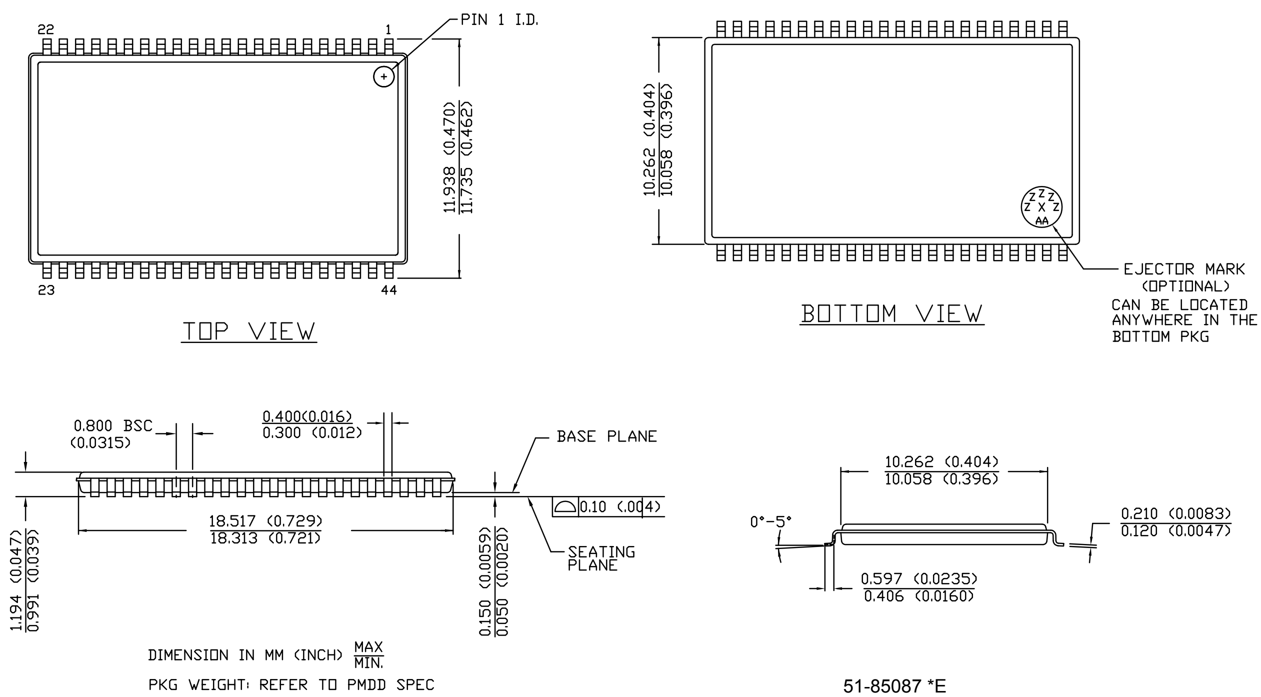
### Ordering Code Definitions

CY 621 5 7 E SL - 45 ZS X I

- Temperature Range: I = Industrial
- Pb-free
- Package Type: ZS = 44-pin TSOP II
- Speed Grade: 45 ns
- Voltage Range: SL = 3 V typical; 5 V typical
- Process Technology: E = 90 nm
- Bus width: 7 = × 16
- Density: 5 = 8-Mbit
- Family Code: MoBL SRAM family
- Company ID: CY = Cypress

## Package Diagram

**Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087**



## Acronyms

| Acronym | Description |
|---|---|
| $\overline{BHE}$ | Byte High Enable |
| $\overline{BLE}$ | Byte Low Enable |
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY62157ESL MoBL®, 8-Mbit (512K × 16) Static RAM<br>Document Number: 001-43141 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 1875228 | See ECN | VKN / AESA | New data sheet. |
| *A | 2943752 | 06/03/2010 | VKN | Added Contents.<br>Updated Electrical Characteristics:<br>Added Note 8 and referred the same note in $I_{SB2}$ parameter.<br>Updated Truth Table:<br>Added Note 32 and referred the same note in $\overline{CE}$ column.<br>Updated Package Diagram.<br>Added Sales, Solutions, and Legal Information. |
| *B | 3109266 | 12/13/2010 | PRAS | Changed Table Footnotes to Footnotes.<br>Added Ordering Code Definitions. |
| *C | 3295175 | 06/29/2011 | RAME | Updated Functional Description:<br>Remove reference to AN1064 SRAM system guidelines.<br>Updated Electrical Characteristics:<br>Updated Note 8 (Added $I_{SB1}$) and referred the same note in $I_{SB1}$ parameter.<br>Updated Capacitance:<br>Added Note 9 and referred the same note in parameter column.<br>Updated Thermal Resistance:<br>Added Note 9 and referred the same note in parameter column.<br>Updated Data Retention Characteristics:<br>Added Note 11 and referred the same note in $I_{CCDR}$ parameter.<br>Updated Ordering Code Definitions.<br>Added Units of Measure. |
| *D | 3904207 | 02/14/2013 | MEMJ | Updated Switching Waveforms:<br>Updated Figure 6 (Removed $\overline{OE}$ signal).<br>Updated Figure 7 (Removed $\overline{OE}$ signal).<br>Removed the Note "Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$." and its reference in Figure 6, Figure 7.<br>Removed the figure "Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW".<br>Updated Figure 8 (Removed "$\overline{OE}$ LOW" in caption only).<br>Removed the Note "Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$." and its reference in Figure 8.<br>Updated Package Diagram:<br>spec 51-85087 – Changed revision from *C to *E. |
| *E | 4019657 | 06/04/2013 | MEMJ | Updated Functional Description:<br>Updated description.<br>Updated Electrical Characteristics:<br>Added one more Test Condition "4.5 ≤ $V_{CC}$ ≤ 5.5, $I_{OH}$ = –0.1 mA" for $V_{OH}$ parameter and added maximum value corresponding to that Test Condition.<br>Added Note 7 and referred the same note in maximum value for $V_{OH}$ parameter corresponding to Test Condition "4.5 ≤ $V_{CC}$ ≤ 5.5, $I_{OH}$ = –0.1 mA". |
| *F | 4100920 | 08/21/2013 | VINI | Updated Switching Characteristics:<br>Added Note 15 and referred the same note in "Parameter" column.<br>Updated to new template. |
| *G | 4576406 | 01/16/2015 | VINI | Updated Functional Description:<br>Added "For a complete list of related documentation, click here." at the end.<br>Updated Switching Characteristics:<br>Added Note 21 and referred the same note in "Write Cycle".<br>Updated Switching Waveforms:<br>Added Figure 9.<br>Added Note 31 and referred the same note in Figure 9. |

## Document History Page (continued)

| Document Title: CY62157ESL MoBL®, 8-Mbit (512K × 16) Static RAM<br>Document Number: 001-43141 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| *H | 5169392 | 03/10/2016 | VINI | Updated Thermal Resistance:<br>Replaced “two-layer” with “four-layer” in “Test Conditions” column.<br>Changed value of $\Theta_{JA}$ parameter from 77 °C/W to 57.92 °C/W.<br>Changed value of $\Theta_{JC}$ parameter from 13 °C/W to 17.44 °C/W.<br>Updated to new template.<br>Completing Sunset Review. |

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