

Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Features

- Higher speed up to 55 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 2.5 μ A
 - Maximum standby current: 7 μ A
- Ultra low active power
 - Typical active current: 3.5 mA at $f = 1$ MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin shrunk thin small outline package (STSOP) package

Functional Description

The CY62148ESL is a high performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

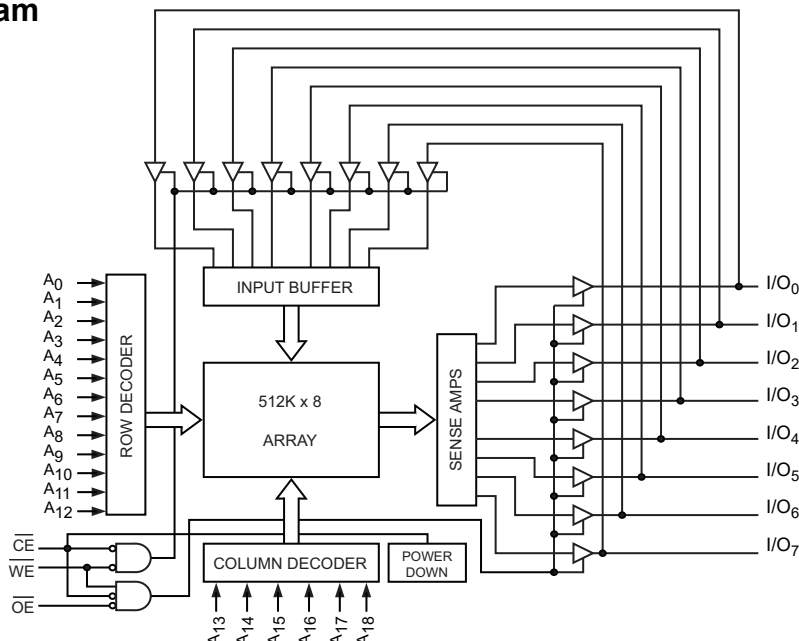
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The CY62148ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related resources, [click here](#).

Logic Block Diagram

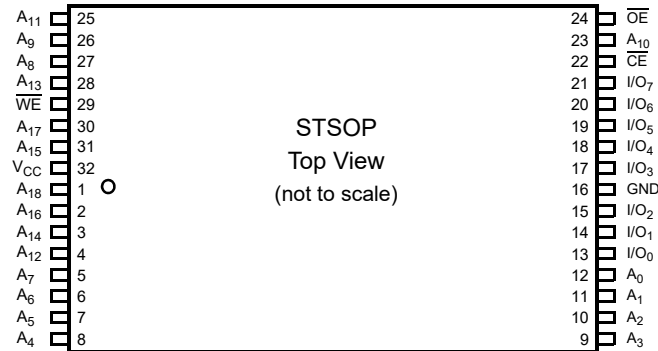


Contents

Pin Configuration	3	Ordering Information	12
Product Portfolio	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagram	13
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	17
Data Retention Characteristics	6	Worldwide Sales and Design Support	17
Data Retention Waveform	6	Products	17
Switching Characteristics	7	PSoC® Solutions	17
Switching Waveforms	8	Cypress Developer Community	17
Truth Table	11	Technical Support	17

Pin Configuration

Figure 1. 32-pin STSOP (Top View) pinout



Product Portfolio

Product	Range	V _{CC} Range (V) ^[1]	Speed (ns)	Power Dissipation					
				Operating I _{CC} , (mA)				Standby, I _{SB2} (μA)	
				f = 1 MHz		f = f _{max}			
				Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62148ESL	Industrial/ Automotive-A	2.2 V to 3.6 V and 4.5 V to 5.5 V	55	3.5	6	15	20	2.5	7

Notes

1. Data sheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied ... 55 °C to +125 °C

Supply voltage to ground potential -0.5 V to 6.0 V

DC voltage applied to outputs

in high Z state ^[3, 4] -0.5 V to 6.0 V

DC input voltage ^[3, 4] -0.5 V to 6.0 V

Output current into outputs (low) 20 mA

Static discharge voltage

(MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[5]
CY62148ESL	Industrial/ Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V, and 4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	55 ns (Industrial/Automotive-A)			Unit
			Min	Typ ^[6]	Max	
V _{OH}	Output HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7 I _{OH} = -0.1 mA	2.0	—	—	V
		2.7 ≤ V _{CC} ≤ 3.6 I _{OH} = -1.0 mA	2.4	—	—	
		4.5 ≤ V _{CC} ≤ 5.5 I _{OH} = -1.0 mA	2.4	—	—	
		4.5 ≤ V _{CC} ≤ 5.5 I _{OH} = -0.1 mA	—	—	3.4 ^[7]	
V _{OL}	Output LOW voltage	2.2 ≤ V _{CC} ≤ 2.7 I _{OL} = 0.1 mA	—	—	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6 I _{OL} = 2.1 mA	—	—	0.4	
		4.5 ≤ V _{CC} ≤ 5.5 I _{OL} = 2.1 mA	—	—	0.4	
V _{IH}	Input HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7	1.8	—	V _{CC} + 0.3	V
		2.7 ≤ V _{CC} ≤ 3.6	2.2	—	V _{CC} + 0.3	
		4.5 ≤ V _{CC} ≤ 5.5	2.2	—	V _{CC} + 0.5	
V _{IL} ^[8]	Input LOW voltage	2.2 ≤ V _{CC} ≤ 2.7	-0.3	—	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6	-0.3	—	0.6	
		4.5 ≤ V _{CC} ≤ 5.5	-0.5	—	0.6	
I _{IX}	Input leakage current	GND ≤ V _{IN} ≤ V _{CC}	-1	—	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-1	—	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC} V _{CC} = V _{CCmax}	—	15	20	mA
		f = 1 MHz I _{OUT} = 0 mA, CMOS levels	—	3.5	6	
I _{SB1} ^[9]	Automatic CE power-down current – CMOS inputs	CE ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE and WE), V _{CC} = V _{CC(max)}	—	2.5	7	μA
			—			
I _{SB2} ^[9]	Automatic CE power-down current – CMOS inputs	CE ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = V _{CC(max)}	—	2.5	7	μA
			—			

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.
- Under DC conditions the device meets a V_{IL} of 0.8 V (for V_{CC} range of 2.7 V to 3.6 V and 4.5 V to 5.5 V) and 0.6 V (for V_{CC} range of 2.2 V to 2.7 V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6 V and 0.4 V for the above ranges.
- Chip enable (CE) must be HIGH at CMOS level to meet the I_{SB1}/I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.

Capacitance

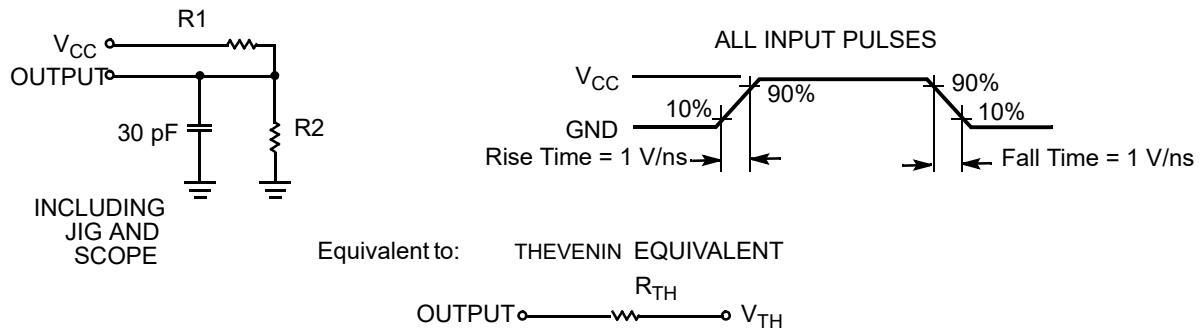
Parameter ^[10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(Typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	32-pin STSOP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, two-layer printed circuit board	49.02	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		14.07	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Note

10. Tested initially and after any design or process changes that may affect these parameters.

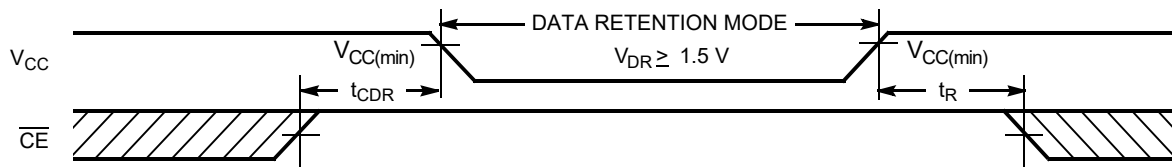
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ ^[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} ^[12]	Data retention current	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $V_{CC} = 1.5 \text{ V}$	–	3	8.8	μA
t_{CDR}	Chip deselect to data retention time		0	–	–	ns
t_R ^[13]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.
12. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu\text{s}$ or stable at $V_{CC(min)} \geq 100 \mu\text{s}$.

Switching Characteristics

Over the operating range

Parameter ^[14, 15]	Description	55 ns (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	55	–	ns
t _{AA}	Address to data valid	–	55	ns
t _{OHA}	Data hold from address change	10	–	ns
t _{ACE}	$\overline{CE}$ LOW to data valid	–	55	ns
t _{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t _{LZOE}	$\overline{OE}$ LOW to low Z ^[16]	5	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to high Z ^[16, 17]	–	20	ns
t _{LZCE}	$\overline{CE}$ LOW to low Z ^[16]	10	–	ns
t _{HZCE}	$\overline{CE}$ HIGH to high Z ^[16, 17]	–	20	ns
t _{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t _{PD}	$\overline{CE}$ HIGH to power-up	–	55	ns
Write Cycle ^[18, 19]				
t _{WC}	Write cycle time	55	–	ns
t _{SCE}	$\overline{CE}$ LOW to write end	40	–	ns
t _{AW}	Address setup to write end	40	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{WE}$ pulse width	40	–	ns
t _{SD}	Data setup to write end	25	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	$\overline{WE}$ LOW to high Z ^[16, 17]	–	20	ns
t _{LZWE}	$\overline{WE}$ HIGH to low Z ^[16]	10	–	ns

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note [AN66311](#). However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in [Figure 2 on page 5](#).
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

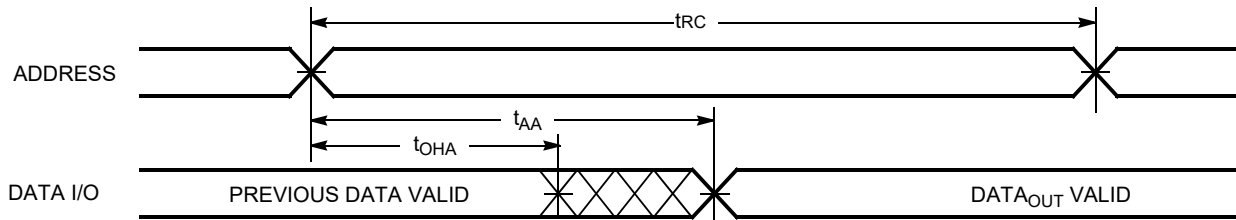
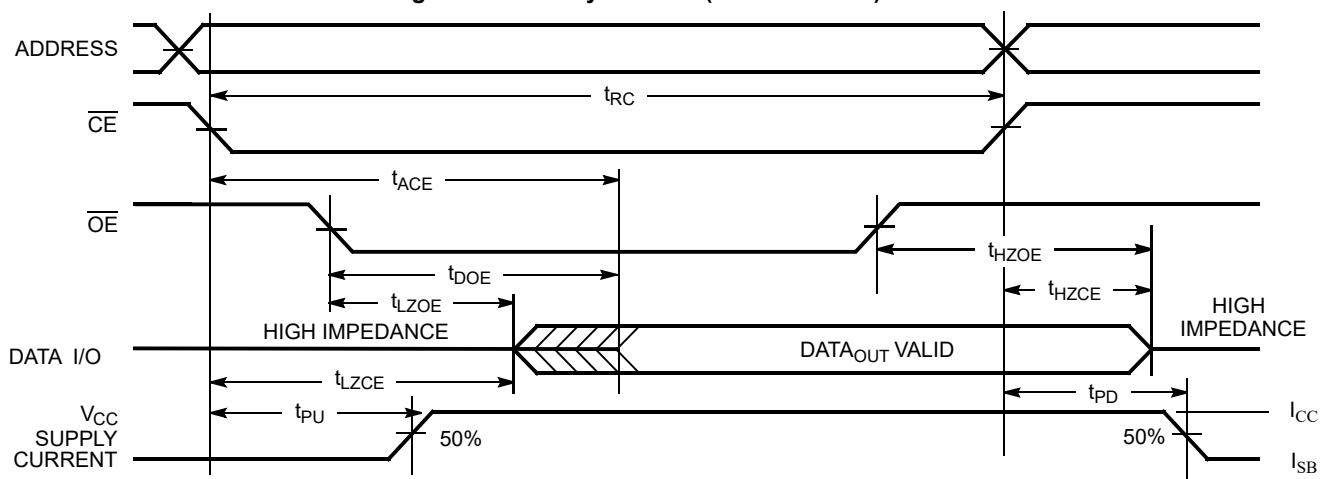
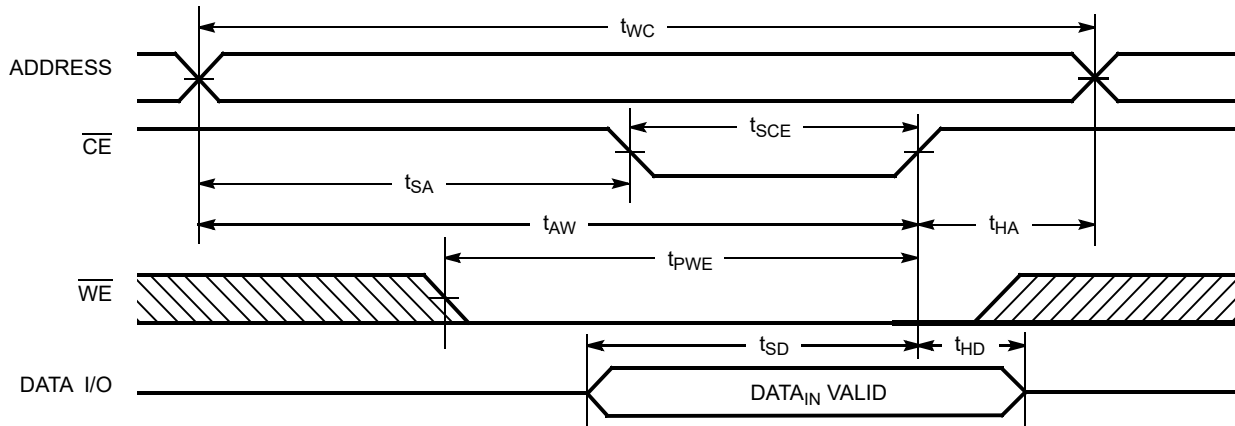
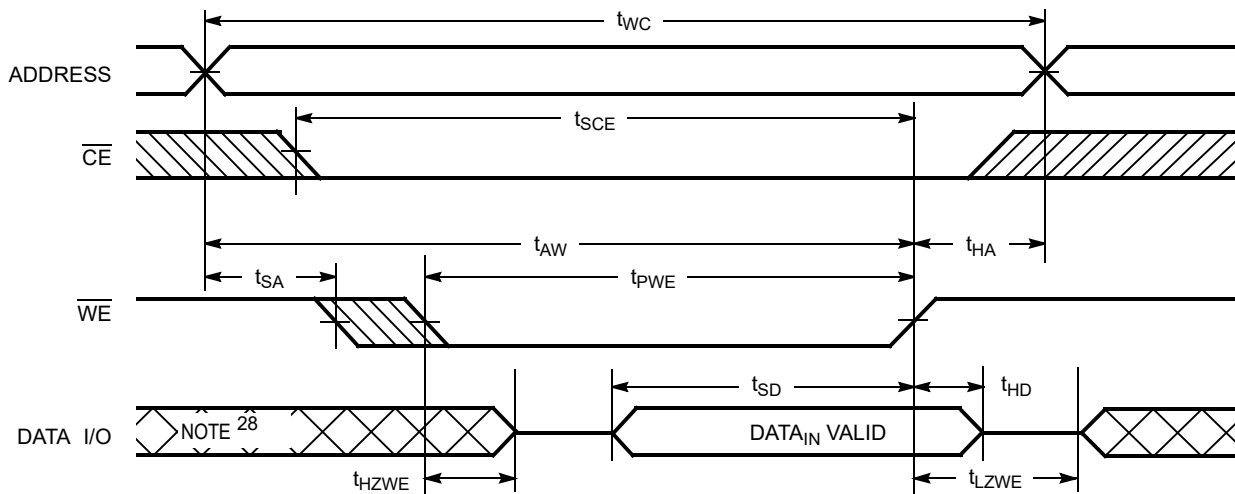


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



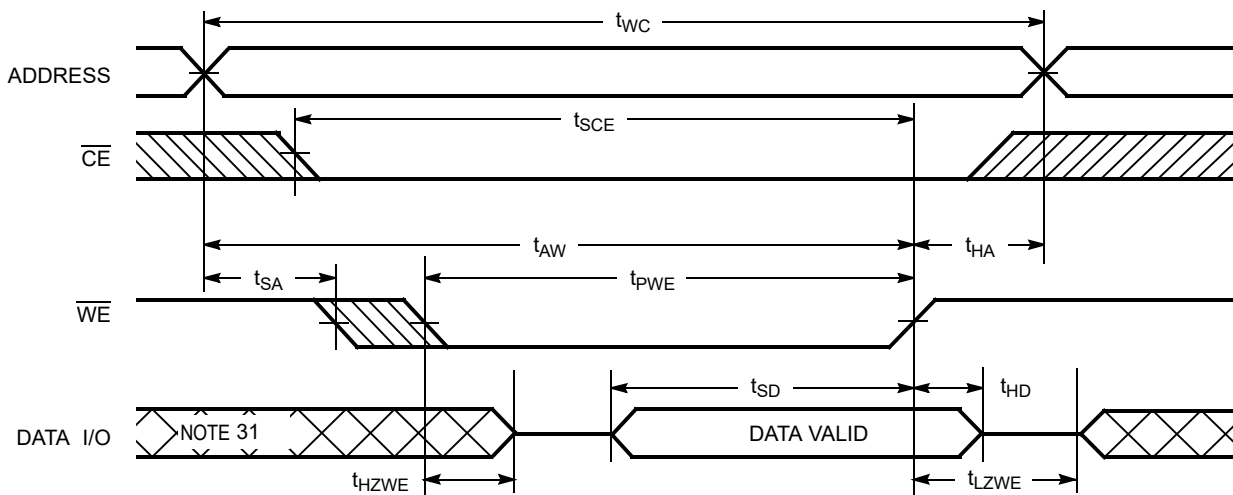
Notes

20. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
21. $\overline{WE}$ is HIGH for read cycles.
22. Address valid before or similar to $\overline{CE}$ transition LOW.
23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)
Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [26, 27]

Figure 7. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled) [27]

Notes

26. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
 27. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in high impedance state.
 28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [29, 30]

Notes

29. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.

30. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .

31. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Mode	Power
H ^[32]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

Note

32. Chip enable ($\overline{\text{CE}}$) must be HIGH at CMOS level to meet the $I_{\text{SB1}} / I_{\text{SB2}} / I_{\text{CCDR}}$ spec. Other inputs can be left floating.

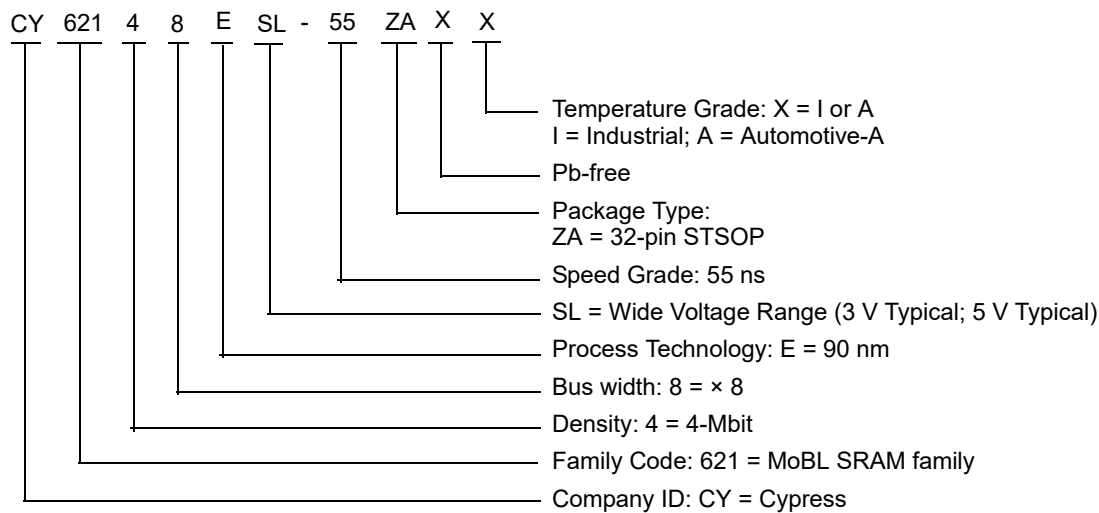
Ordering Information

Table 1 lists the CY62148ESL MoBL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>.

Table 1. Key features and Ordering Information

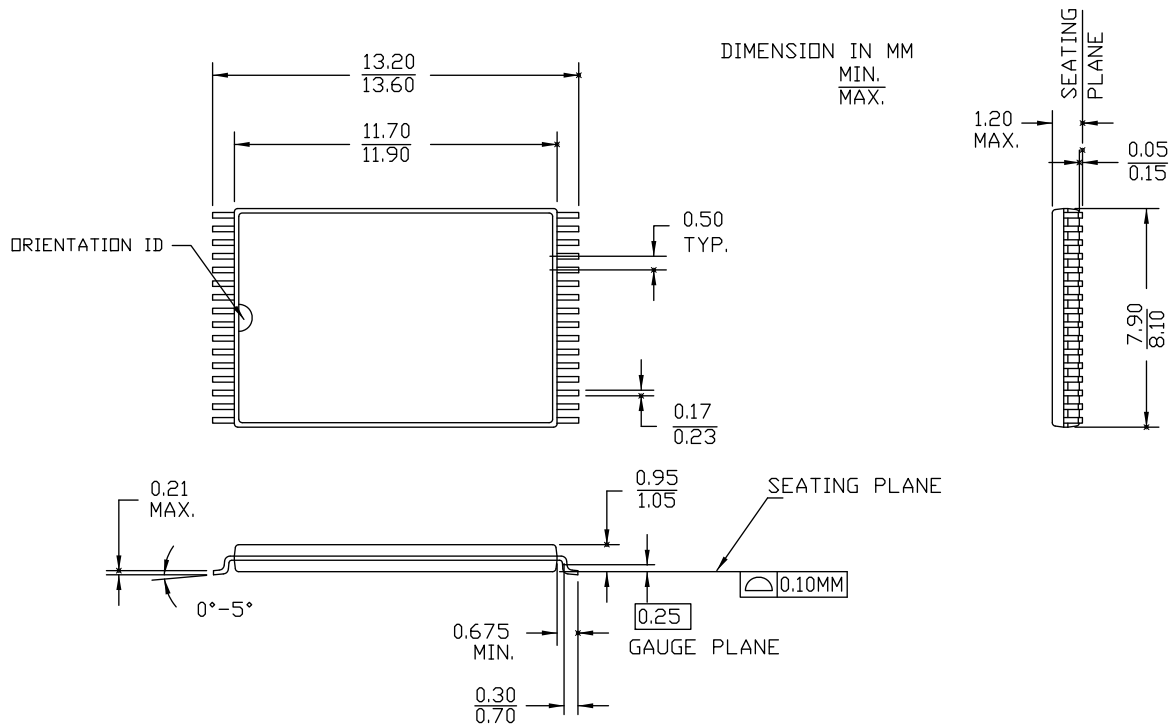
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148ESL-55ZAXI	51-85094	32-pin STSOP (Pb-free)	Industrial
	CY62148ESL-55ZAXA	51-85094	32-pin STSOP (Pb-free)	Automotive-A

Ordering Code Definitions



Package Diagram

Figure 9. 32-pin STSOP (8 × 13.4 × 1.2 mm) ZA32 Package Outline, 51-85094



51-85094 *G

Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148ESL MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 001-50045			
Rev.	ECN	Submission Date	Description of Change
**	2612938	01/21/2009	New data sheet.
*A	2800124	11/06/2009	Updated Product Portfolio (Included Automotive-A information). Updated Operating Range (Included Automotive-A information). Updated Ordering Information : Updated part numbers.
*B	2947039	06/10/2010	Updated Electrical Characteristics : Added Note 9 and referred the same note in I _{SB2} parameter. Updated Truth Table : Added Note 32 and referred the same note in "CE" column. Updated Package Diagram : spec 51-85094 – Changed revision from *D to *E.
*C	3006318	08/23/2010	Updated Electrical Characteristics : Updated Note 9 and referred the same note in I _{SB1} parameter. Updated Data Retention Characteristics : Added Note 12 and referred the same note in I _{CCDR} parameter. Updated Ordering Information : No change in part numbers. Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated to new template.
*D	3296704	06/29/2011	Updated Functional Description : Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines ." at the end. Updated Ordering Information : No change in part numbers. Updated Ordering Code Definitions . Updated Package Diagram : spec 51-85094 – Changed revision from *E to *F.
*E	3515577	02/03/2012	Updated Switching Waveforms : Updated Figure 4 . Updated Figure 5 . Updated Figure 6 . Updated Figure 7 . Updated Figure 8 . Completing Sunset Review.
*F	3548240	03/12/2012	Updated Electrical Characteristics : Updated Note 8 (Removed "Refer to AN13470 for details.>").
*G	3897076	02/06/2013	Updated Switching Waveforms : Removed figure "Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)". Updated Figure 7 (Updated caption only). Completing Sunset Review.
*H	4039358	07/01/2013	Updated Functional Description : Updated description. Updated Electrical Characteristics : Added one more Test Condition "4.5 ≤ V _{CC} ≤ 5.5" for V _{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V _{OH} parameter corresponding to Test Condition "4.5 ≤ V _{CC} ≤ 5.5". Updated to new template.
*I	4099182	08/19/2013	Updated Switching Characteristics : Added Note 14 and referred the same note in "Parameter" column.

Document History Page (continued)

Document Title: CY62148ESL MoBL, 4-Mbit (512K × 8) Static RAM Document Number: 001-50045			
Rev.	ECN	Submission Date	Description of Change
*J	4779516	05/28/2015	Updated Functional Description : Added "For a complete list of related resources, click here ." at the end. Updated AC Test Loads and Waveforms : Updated Figure 2 . Updated Switching Characteristics : Added Note 19 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Figure 8 . Added Note 29, 30, 31 and referred the same note in Figure 8 . Updated Package Diagram : spec 51-85094 – Changed revision from *F to *G. Updated to new template.
*K	6906316	06/26/2020	Updated Features : Changed value of Typical standby current from 1 μ A to 2.5 μ A. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio : Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to "f = 1 MHz". Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to "f = 1 MHz". Changed typical value of Standby, I_{SB2} from 1 μ A to 2.5 μ A. Updated Electrical Characteristics : Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB1} parameter from 1 μ A to 2.5 μ A. Changed typical value of I_{SB2} parameter from 1 μ A to 2.5 μ A. Updated Data Retention Characteristics : Changed typical value of I_{CCDR} parameter from 1 μ A to 3 μ A. Changed maximum value of I_{CCDR} parameter from 7 μ A to 8.8 μ A. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2009–2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.