

## Features

- Very high speed: 45 ns
- Temperature range
  - Automotive-A: -40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA (Automotive-A)
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  Features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package
- Byte power down feature

## Functional Description

The CY621472E30 is a high-performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device

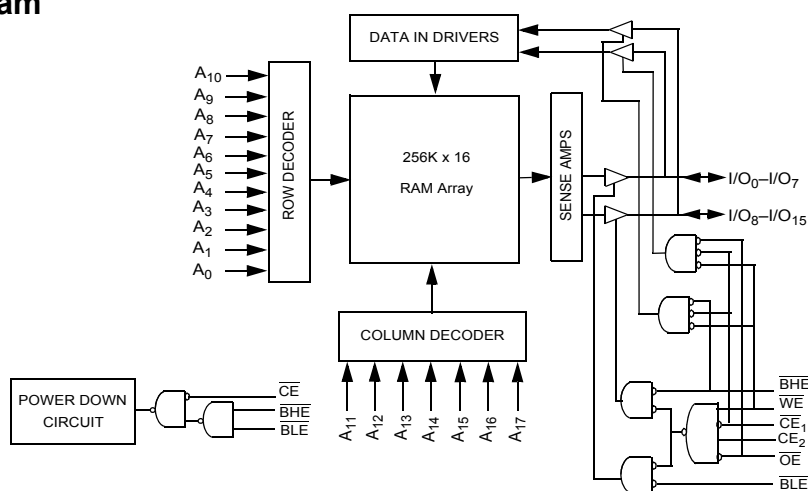
also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both BLE and BHE are HIGH). The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH and  $\overline{WE}$  LOW)

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from the I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data from the I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from the memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See the [Truth Table on page 11](#) for a complete description of read and write modes.

## Logic Block Diagram



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## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>max</sub>							
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY621472E30LL	Automotive-A	2.2	3.0	3.6	45	2	2.5	15	20	1	7

## Pin Configuration

Figure 1. 44-pin TSOP II pinout

A <sub>4</sub>	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	OE
A <sub>0</sub>	5	40	BHE
CE <sub>1</sub>	6	39	BLE
I/O <sub>0</sub>	7	38	I/O <sub>15</sub>
I/O <sub>1</sub>	8	37	I/O <sub>14</sub>
I/O <sub>2</sub>	9	36	I/O <sub>13</sub>
I/O <sub>3</sub>	10	35	I/O <sub>12</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>4</sub>	13	32	I/O <sub>11</sub>
I/O <sub>5</sub>	14	31	I/O <sub>10</sub>
I/O <sub>6</sub>	15	30	I/O <sub>9</sub>
I/O <sub>7</sub>	16	29	I/O <sub>8</sub>
WE	17	28	CE <sub>2</sub>
A <sub>17</sub>	18	27	A <sub>8</sub>
A <sub>16</sub>	19	26	A <sub>9</sub>
A <sub>15</sub>	20	25	A <sub>10</sub>
A <sub>14</sub>	21	24	A <sub>11</sub>
A <sub>13</sub>	22	23	A <sub>12</sub>

### Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ), T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
to ground potential ..... -0.3 V to +3.9 V ( $V_{CCmax} + 0.3$  V)

DC voltage applied to outputs  
in High Z State <sup>[2, 3]</sup> ..... -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$  V)

DC input voltage <sup>[2, 3]</sup> ..... -0.3 V to 3.9 V ( $V_{CCmax} + 0.3$  V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[4]</sup>
CY621472E30LL	Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V

## Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ <sup>[5]</sup>	Max	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -0.1$ mA	2.0	—	—	V
		$I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70$ V	2.4	—	—	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 0.1$ mA	—	—	0.4	V
		$I_{OL} = 2.1$ mA, $V_{CC} = 2.70$ V	—	—	0.4	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 2.2$ V to 2.7 V	1.8	—	$V_{CC} + 0.3$	V
		$V_{CC} = 2.7$ V to 3.6 V	2.2	—	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 2.2$ V to 2.7 V	-0.3	—	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V	-0.3	—	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	—	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , Output disabled	-1	—	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$	—	15	20	mA
		$f = 1$ MHz $I_{OUT} = 0$ mA CMOS levels	—	2	2.5	
$I_{SB1}$ <sup>[6]</sup>	Automatic CE power-down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (address and data only), $f = 0$ (OE, BHE, BLE and WE), $V_{CC} = 3.60$ V	—	1	7	μA
$I_{SB2}$ <sup>[6]</sup>	Automatic CE power-down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or (BHE and BLE) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 3.60$ V	—	1	7	μA

### Notes

- $V_{IL}$  (min) = -2.0 V for pulse durations less than 20 ns.
- $V_{IH}$  (max) =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100-μs ramp time from 0 to  $V_{CC}$ (min) and 200 μs wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}$  (typ),  $T_A = 25$  °C.
- Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) need to be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

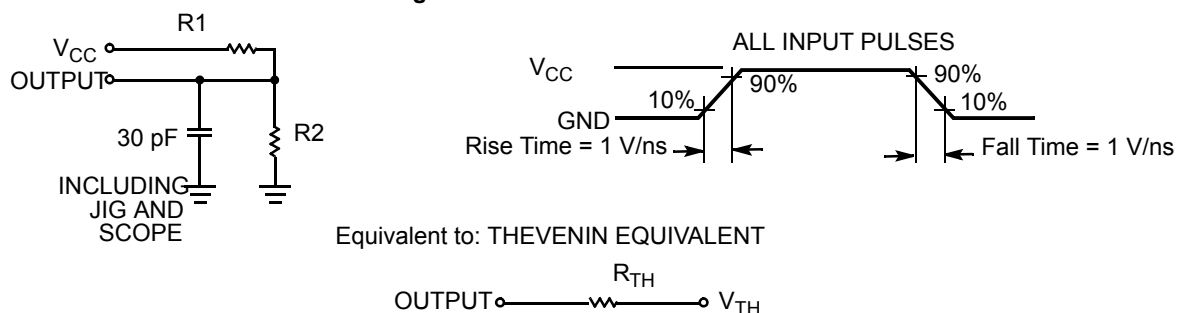
Parameter <sup>[7]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC}(\text{typ})$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[7]</sup>	Description	Test Conditions	44-pin TSOP II Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still Air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	55.52	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		16.03	$^{\circ}\text{C/W}$

## AC Test Load and Waveforms

Figure 2. AC Test Load and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

### Note

7. Tested initially and after any design or process changes that may affect these parameters.

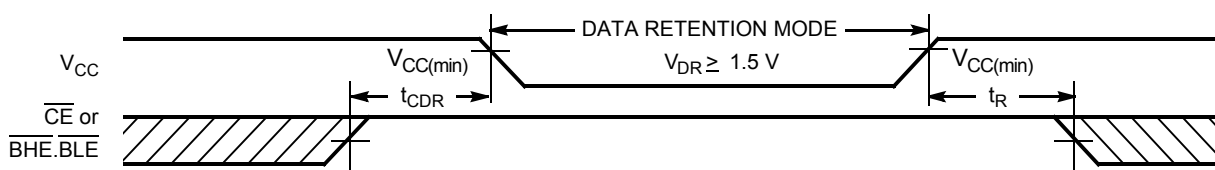
## Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ <sup>[8]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}$ <sup>[9]</sup>	Data retention current	$V_{CC} = 1.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	0.8	7	$\mu\text{A}$
$t_{CDR}$ <sup>[10]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[11]</sup>	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform<sup>[12, 13]</sup>



### Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}(\text{typ})$ ,  $T_A = 25^\circ\text{C}$ .
9. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) need to be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$ .
12.  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH.
13.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

Parameter <sup>[14]</sup>	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	45	–	ns
t <sub>AA</sub>	Address to data valid	–	45	ns
t <sub>OHA</sub>	Data hold from address change	10	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to data valid	–	45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[15]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[15, 16]</sup>	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Low-Z <sup>[15]</sup>	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to High-Z <sup>[15, 16]</sup>	–	18	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Power-up	0	–	ns
t <sub>PD</sub>	$CE_1$ HIGH/ $CE_2$ LOW to Power-down	–	45	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z <sup>[15, 17]</sup>	5	–	ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z <sup>[15, 16]</sup>	–	18	ns
Write Cycle <sup>[18]</sup>				
t <sub>WC</sub>	Write cycle time	45	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Write End	35	–	ns
t <sub>AW</sub>	Address setup to write end	35	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35	–	ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[15, 16]</sup>	–	18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[15]</sup>	10	–	ns

### Notes

14. Test conditions for all parameters other than tristate parameters assume a signal transition time of 3 ns (1 V/ns) or less, timing reference levels of  $V_{CC}(typ)/2$ , input pulse levels of 0 to  $V_{CC}(typ)$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 2 on page 5](#).

15. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

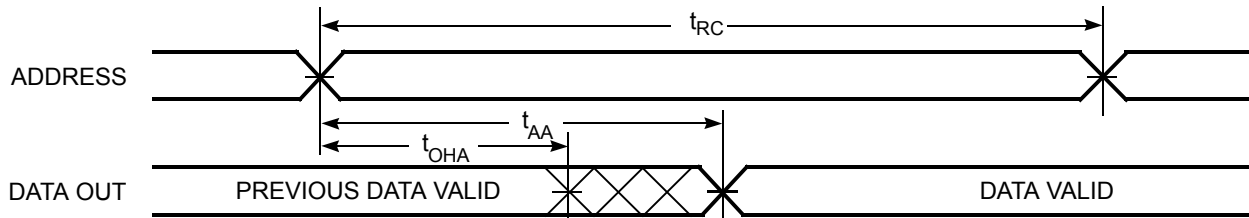
16.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

17. If both byte enables are together, this value is 10 ns.

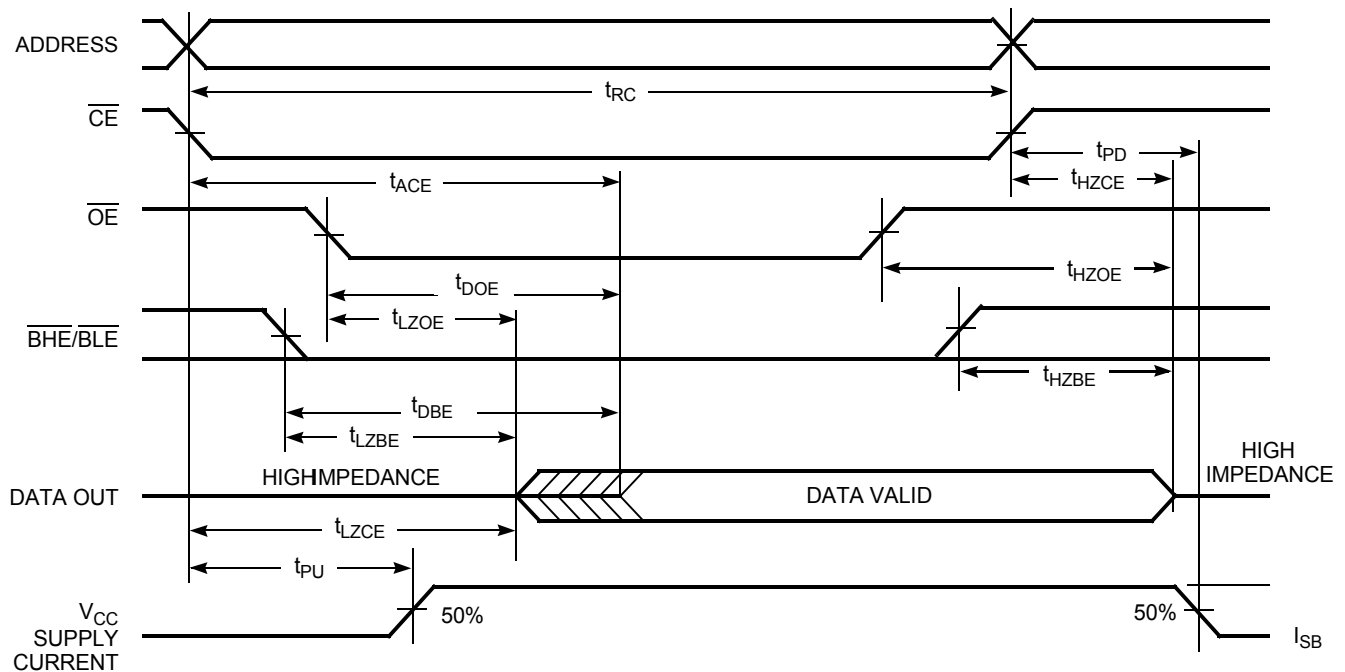
18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [19, 20]



**Figure 5. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [20, 21, 22]



### Notes

19. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$  =  $V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ .

20.  $\overline{\text{WE}}$  is HIGH for read cycle.

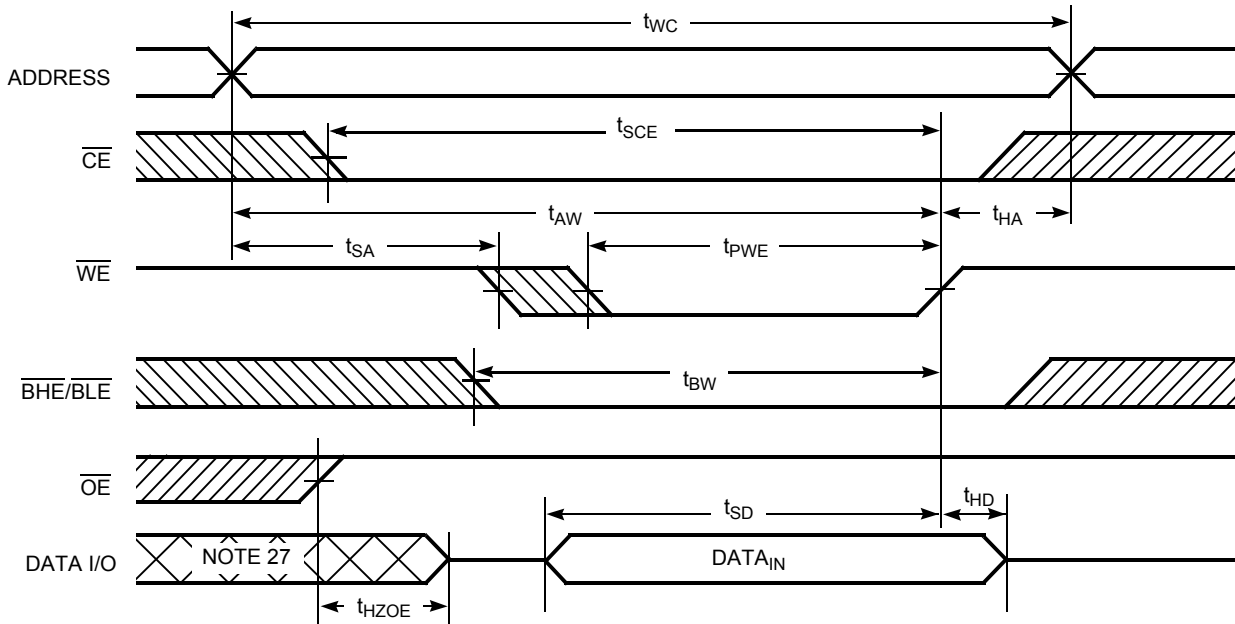
21.  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH.

22. Address valid before or similar to  $\overline{\text{CE}}$  and  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW.

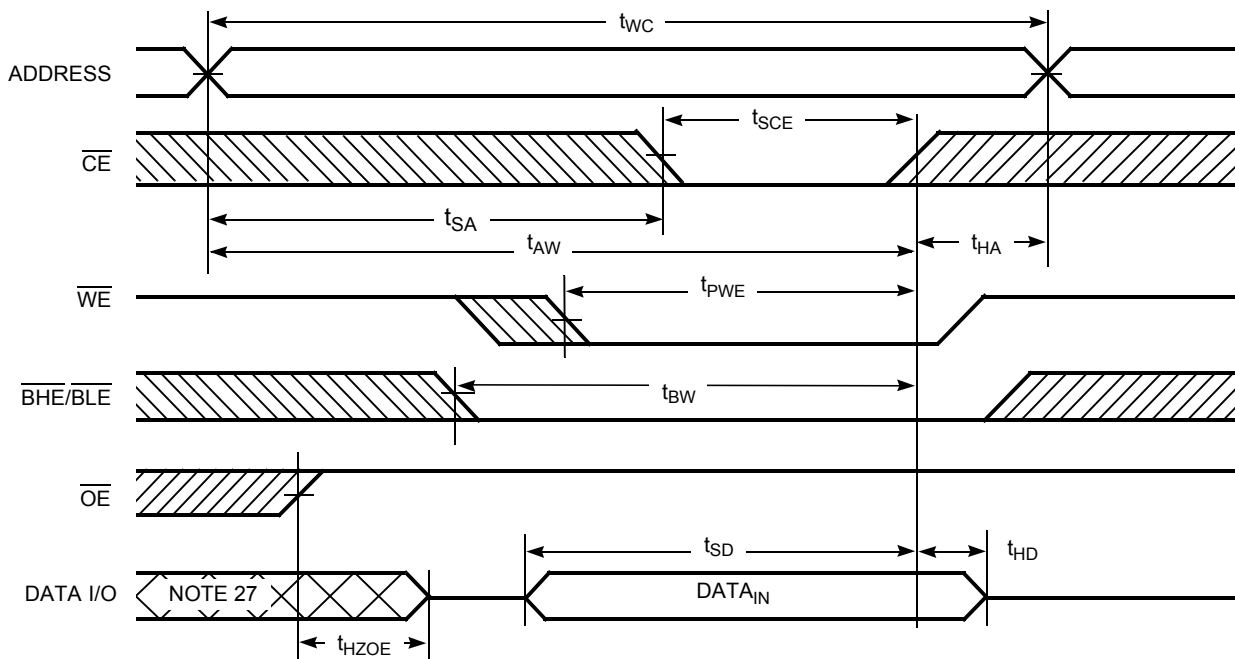


## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** [23, 24, 25, 26]



**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [23, 24, 25, 26]

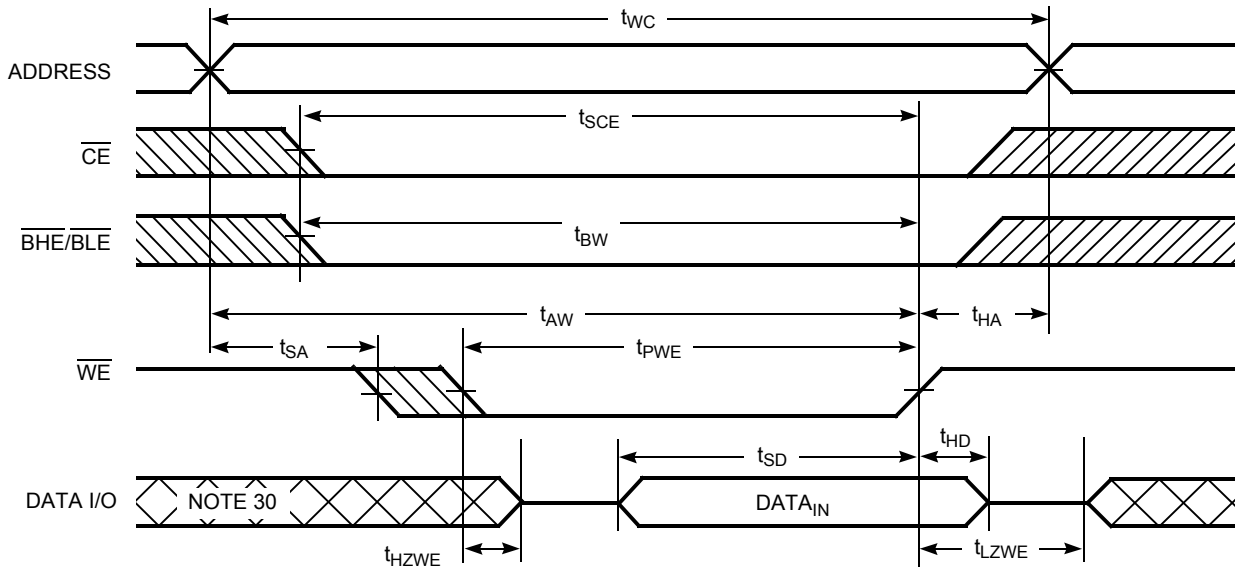


### Notes

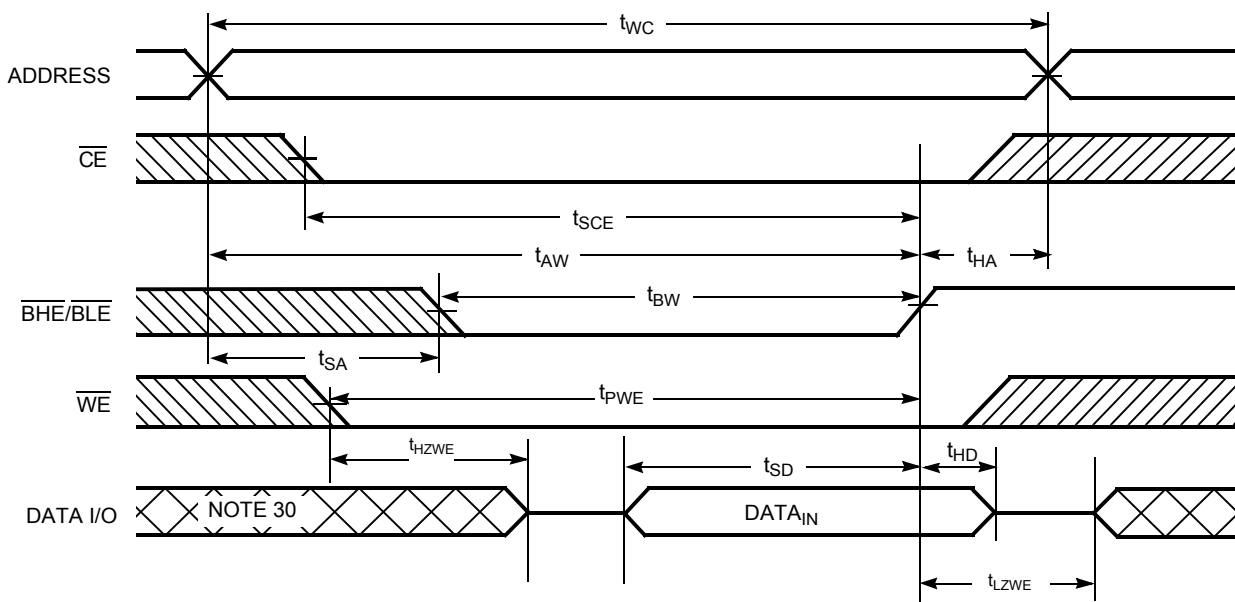
23.  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. For all other cases  $\overline{\text{CE}}$  is HIGH.
24. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
25. Data I/O is high-impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
26. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high-impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [28, 29]**



**Figure 9. Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW) [28, 29]**



### Notes

28.  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH.

29. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.

30. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	I/Os	Mode	Power
H	X <sup>[31]</sup>	X	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[31]</sup>	L	X	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X <sup>[31]</sup>	X <sup>[31]</sup>	X	X	H	H	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	H	L	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	L	H	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data in ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data in ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High-Z	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data in ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High-Z	Write	Active ( $I_{CC}$ )

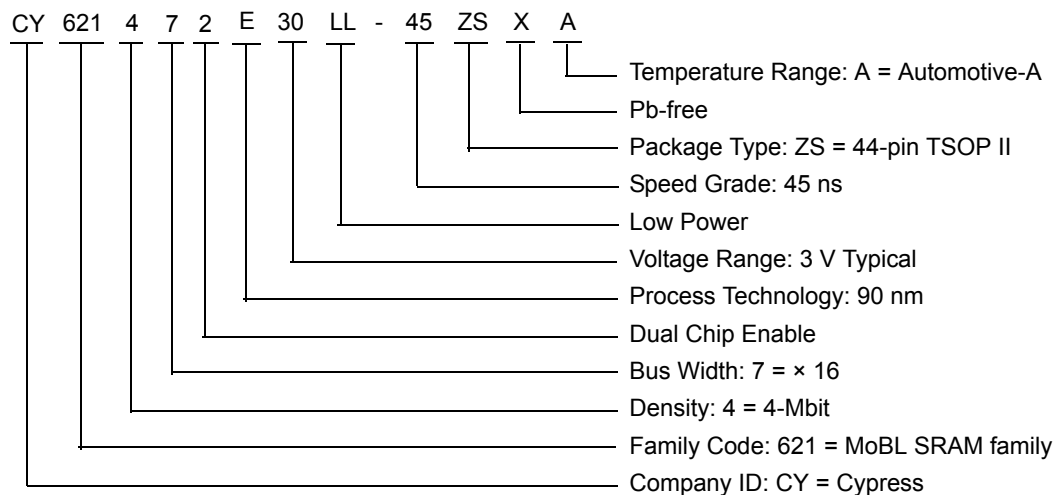
### Note

31. The 'X' (Don't care) state for the chip enables ( $\overline{CE}_1$  and  $CE_2$ ) in the Truth Table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

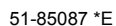
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY621472E30LL-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A

## Ordering Code Definitions



**Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087**



## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY621472E30 MoBL® Automotive, 4-Mbit (256K × 16) Static RAM Document Number: 001-89978				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*A	4316520	VINI	03/21/2014	Changed status from Preliminary to Final.
*B	5545167	VINI	12/07/2016	Updated <a href="#">Thermal Resistance</a> : Replaced “two-layer” with “four-layer” in “Test Conditions” column. Changed value of $\Theta_{JA}$ parameter corresponding to 44-pin TSOP II Package from 77 °C/W to 55.52 °C/W. Changed value of $\Theta_{JC}$ parameter corresponding to 44-pin TSOP II Package from 13 °C/W to 16.03 °C/W. Updated to new template. Completing Sunset Review.

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