

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 7 μ A
- Ultra low active power
 - Typical active current: 2 mA at $f = 1$ MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

Functional Description

The CY62136ESL is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that reduces power consumption when addresses are

not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

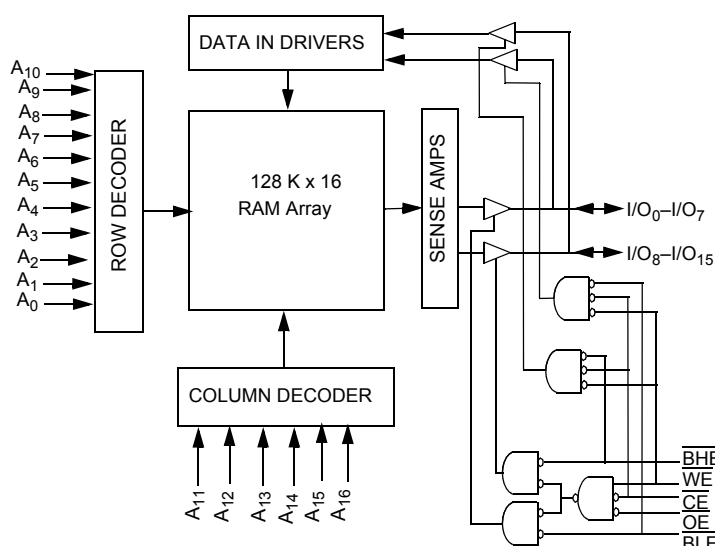
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the [Truth Table on page 11](#) for a complete description of read and write modes.

The device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

Logic Block Diagram

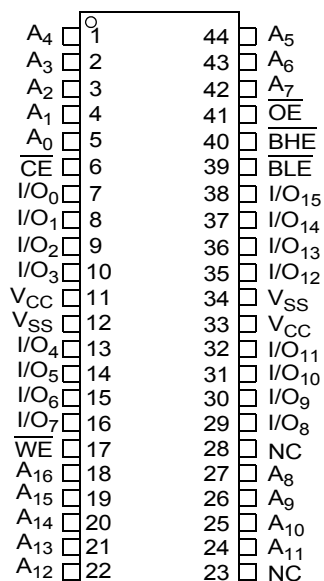


Contents

Pin Configuration	3	Ordering Information	12
Product Portfolio	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagram	13
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	17
Data Retention Characteristics	6	Worldwide Sales and Design Support	17
Data Retention Waveform	6	Products	17
Switching Characteristics	7	PSoC® Solutions	17
Switching Waveforms	8	Cypress Developer Community	17
Truth Table	11	Technical Support	17

Pin Configuration

Figure 1. 44-pin TSOP II pinout (Top View) ^[1]



Product Portfolio

Product	Range	V _{CC} Range (V) ^[2]	Speed (ns)	Power Dissipation					
				Operating I _{CC} , (mA)				Standby, I _{SB2} (μA)	
				f = 1MHz		f = f _{max} = 1/TRC			
				Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY62136ESL	Industrial	2.2 V to 3.6 V and 4.5 V to 5.5 V	45	2	2.5	15	20	1	7

Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage
to ground potential [4, 5] -0.5 V to 6.0 V

DC voltage applied to outputs
in High Z State [4, 5] -0.5 V to 6.0 V

DC input voltage [4, 5] -0.5 V to 6.0 V

Output current into outputs (LOW) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) >2001 V

Latch up current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62136ESL	Industrial	-40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ ^[7]	Max	
V _{OH}	Output HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OH} = -0.1 mA	2.0	—	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OH} = -1.0 mA	2.4	—	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OH} = -1.0 mA	2.4	—	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OH} = -0.1 mA	—	3.4 ^[8]	
V _{OL}	Output LOW voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA	—	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1 mA	—	0.4	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OL} = 2.1 mA	—	0.4	
V _{IH}	Input HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7	—	—	V _{CC} + 0.3	V
		2.7 ≤ V _{CC} ≤ 3.6	—	—	V _{CC} + 0.3	
		4.5 ≤ V _{CC} ≤ 5.5	—	—	V _{CC} + 0.5	
V _{IL}	Input LOW voltage	2.2 ≤ V _{CC} ≤ 2.7	—0.3	—	0.6	V
		2.7 ≤ V _{CC} ≤ 3.6	—0.3	—	0.8	
		4.5 ≤ V _{CC} ≤ 5.5	—0.5	—	0.8	
I _{IX}	Input leakage current	GND ≤ V _{in} ≤ V _{CC}	-1	—	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} ; Output disabled	-1	—	+1	μA
I _{CC}	V _{CC} Operating supply current	f = f _{max} = 1/t _{RC}	—	15	20	mA
		f = 1 MHz	—	2	2.5	
I _{SB1} ^[9]	Automatic CE power-down current — CMOS inputs	CE ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = f _{max} (Address and data only), f = 0 (OE, BHE, BLE and WE), V _{CC} = V _{CC(max)}	—	1	7	μA
I _{SB2} ^[9]	Automatic CE power-down current — CMOS inputs	CE ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = V _{CC(max)}	—	1	7	μA

Notes

- V_{IL}(min) = -2.0 V for pulse durations less than 20 ns.
- V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C.
- Please note that, the maximum V_{OH} limit for this device may not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider. This maximum limit is not 100% tested.
- Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

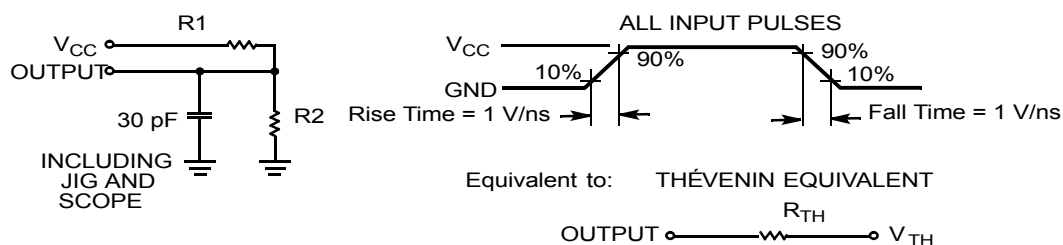
Parameter ^[10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		17	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Note

10. Tested initially and after any design or process changes that may affect these parameters.

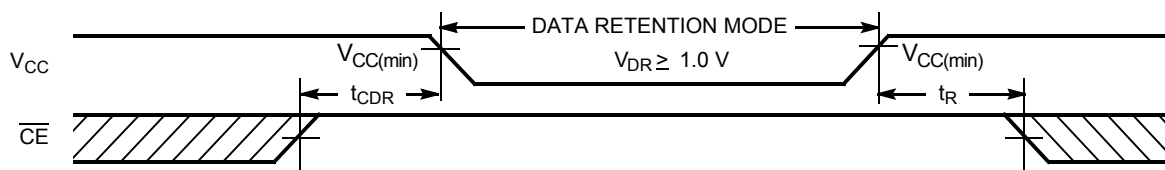
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
$I_{CCDR}^{[12]}$	Data retention current	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	$V_{CC} = 1.0 \text{ V}$	–	0.8	3 μA
$t_{CDR}^{[13]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[14]}$	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.
12. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu\text{s}$ or stable at $V_{CC(min)} \geq 100 \mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[15, 16]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	45	–	ns
t _{AA}	Address to data valid	–	45	ns
t _{OHA}	Data hold from address change	10	–	ns
t _{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t _{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[17]	5	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[17, 18]	–	18	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[17]	10	–	ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[17, 18]	–	18	ns
t _{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t _{PD}	$\overline{CE}$ HIGH to ower-down	–	45	ns
t _{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	22	ns
t _{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[17]	5	–	ns
t _{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[17, 18]	–	18	ns
Write Cycle ^[19, 20]				
t _{WC}	Write cycle time	45	–	ns
t _{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t _{AW}	Address setup to write end	35	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{WE}$ pulse width	35	–	ns
t _{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t _{SD}	Data setup to write end	25	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[17, 18]	–	18	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[17]	10	–	ns

Notes

15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 2 on page 5](#).
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
20. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ Controlled) should be equal to sum of t_{SD} and t_{HZWE} .

Figure 4. Read Cycle No.1 (Address Transition Controlled) [21, 22]

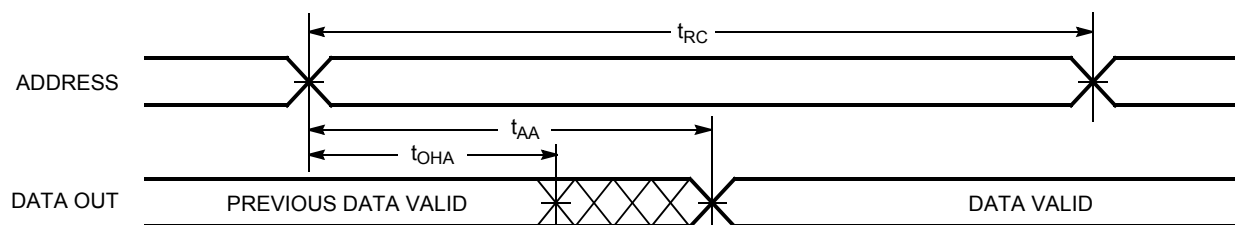
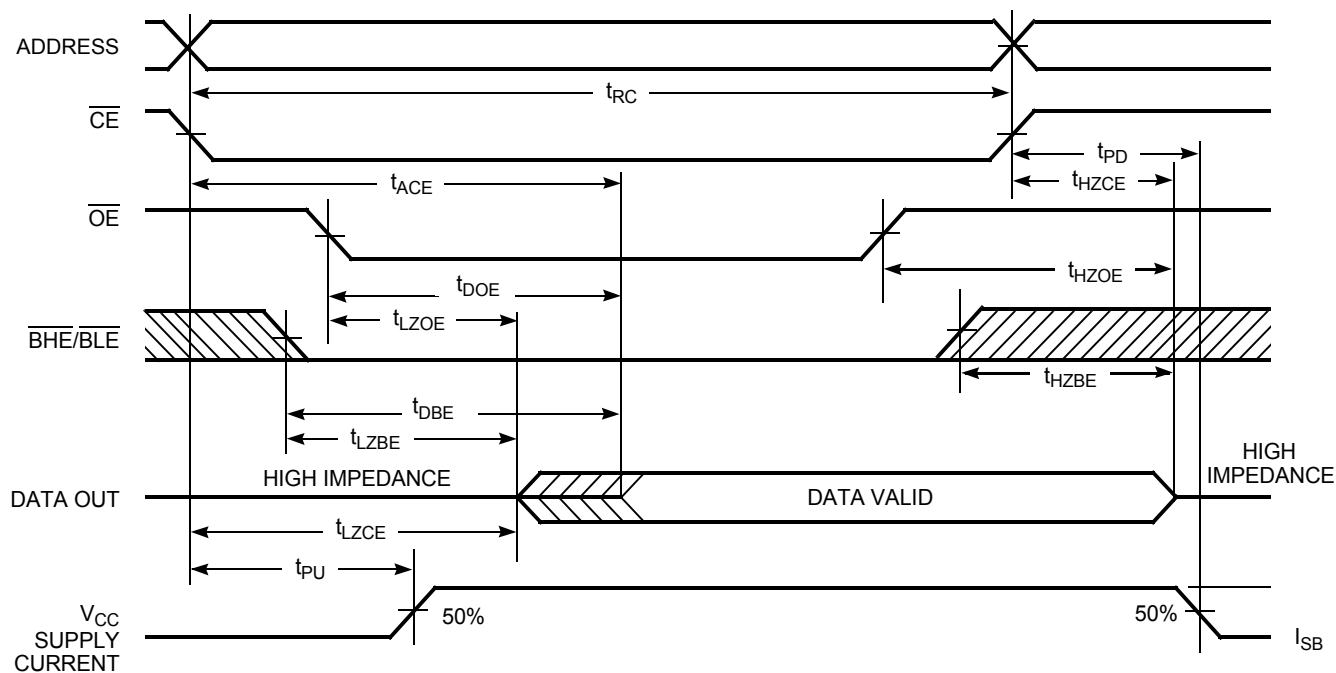


Figure 5. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [22, 23]



21. $\overline{\text{OE}}$, $\overline{\text{CE}}$ = V_{IL} , $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, or both = V_{IL} .
 22. $\overline{\text{WE}}$ is HIGH for read cycle.
 23. Address valid before or similar to $\overline{\text{CE}}$. $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) [24, 25, 26]

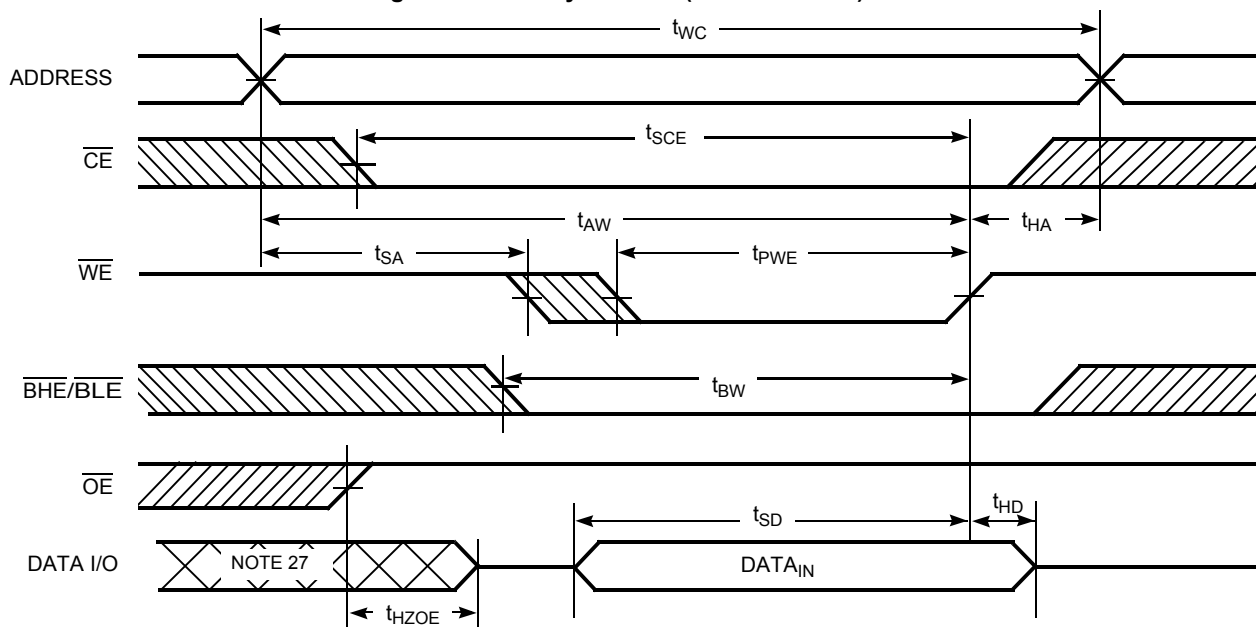
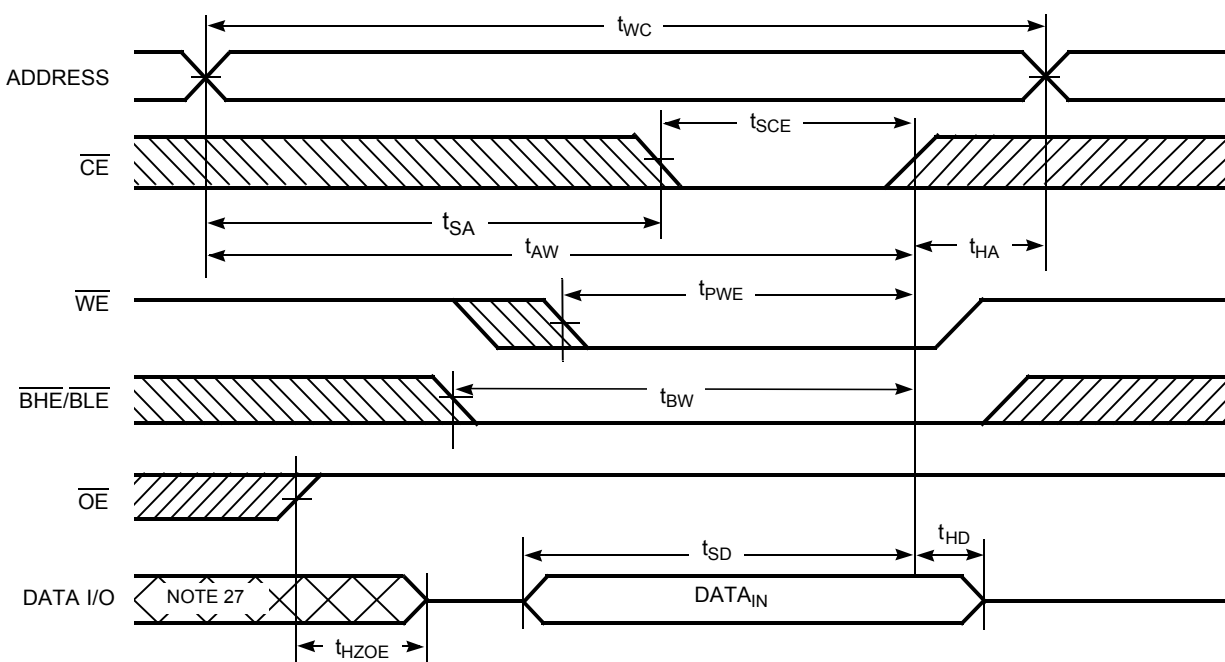


Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [24, 25, 26]



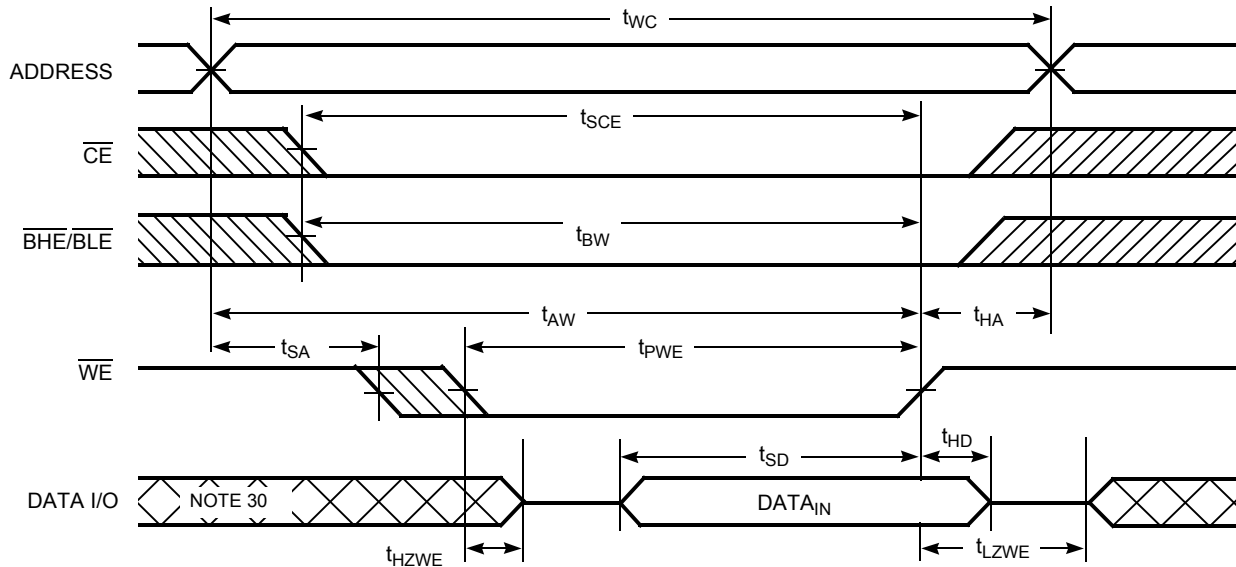
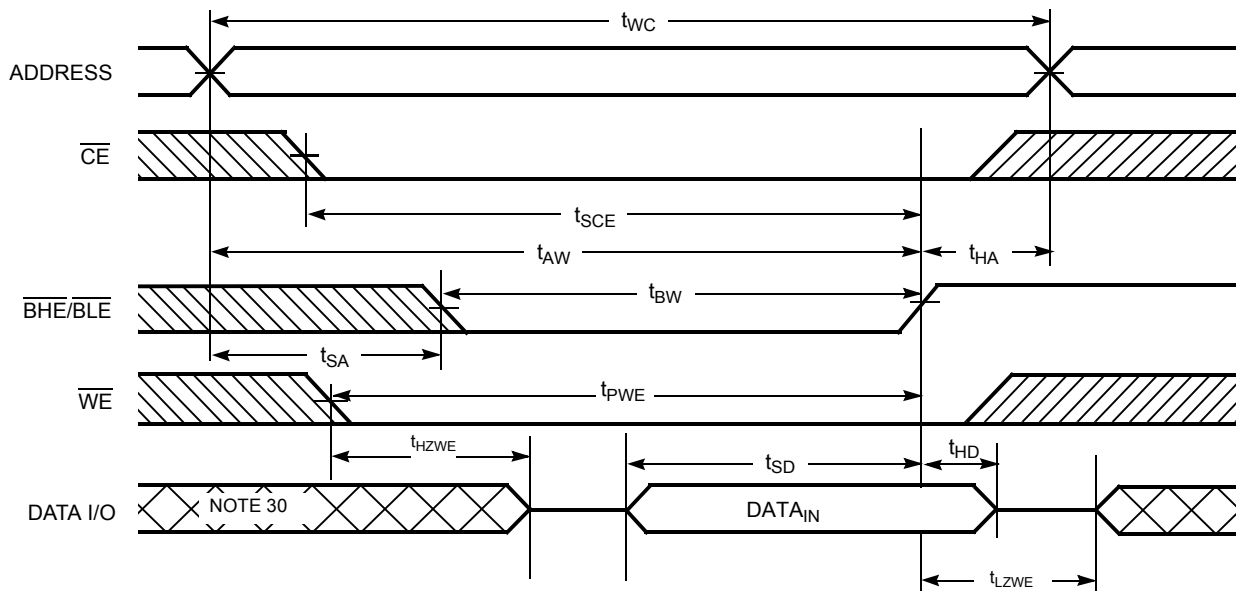
Notes

24. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IL}}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

25. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.

26. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}} = V_{\text{IH}}$, the output remains in a high impedance state.

27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)
Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [28, 29]

Figure 9. Write Cycle No. 4 ($\overline{BHE/BLE}$ Controlled, $\overline{OE}$ LOW) [28]

Notes

28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
 29. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD} .
 30. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}^{[31]}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X ^[31]	X ^[31]	High Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

Note

31. The 'X' (Don't care) state for the Chip enable ($\overline{CE}$) and Byte enables ($\overline{BHE}$ and $\overline{BLE}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

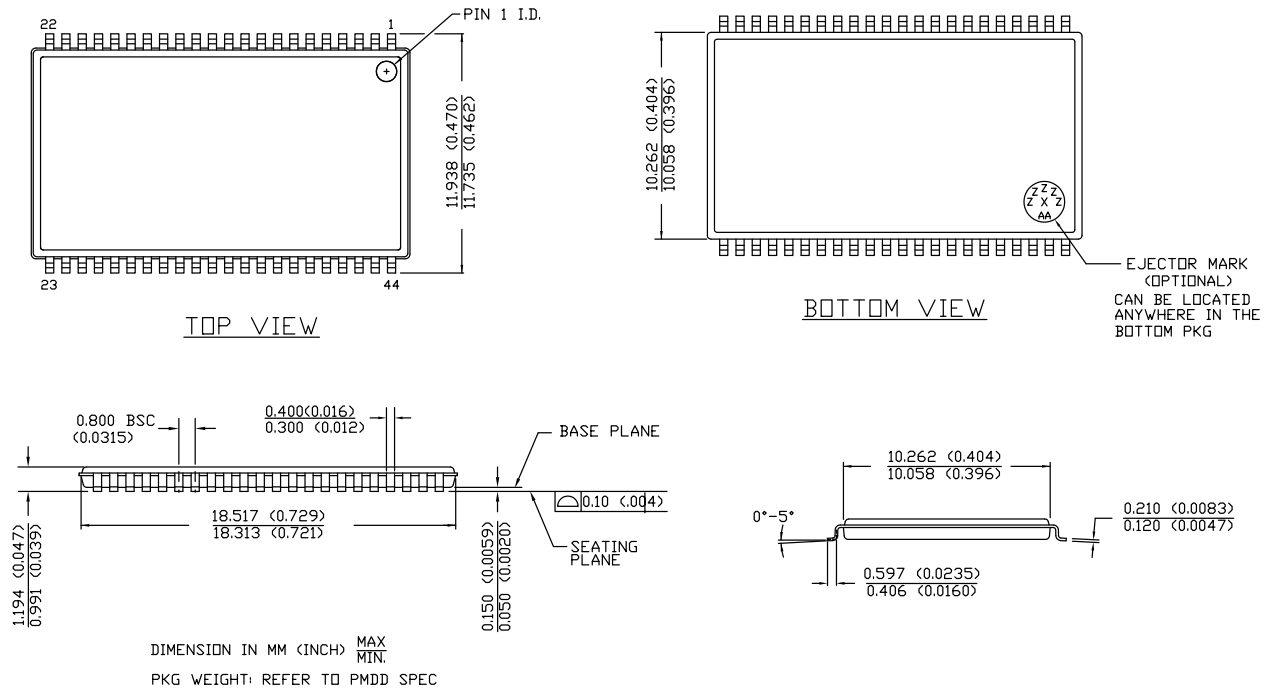
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136ESL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial

Ordering Code Definitions

CY	621	3	6	E	SL	-	45	ZS	X	I	
											Temperature Grade: I = Industrial
											Pb-free
											Package Type: ZS = 44-pin TSOP II
											Speed Grade: 45 ns
											Wide Voltage Range (3 V and 5 V)
											Process Technology: E = 90 nm Technology
											Bus width: 6 = × 16
											Density: 3 = 2-Mbit
											Family Code: 621 = MoBL SRAM family
											Company ID: CY = Cypress

Package Diagram

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62136ESL MoBL [®] , 2-Mbit (128 K × 16) Static RAM Document Number: 001-48147				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2615537	VKN / PYRS	12/03/08	New data sheet.
*A	2718906	VKN	06/15/2009	Post to external web.
*B	2944332	VKN	06/04/2010	Added Contents . Updated Electrical Characteristics : Added Note 9 and referred the same note in I _{SB2} parameter. Updated Switching Characteristics : Added Note 16 and referred the same note in "Parameter" column. Updated Truth Table : Added Note 31 and referred the same note in "CE", "BHE" and "BLE" columns. Updated Package Diagram . Updated links in Sales, Solutions, and Legal Information .
*C	3126445	RAME	01/03/2011	Changed all table notes to footnotes in all instances across the document. Added Acronyms and Units of Measure . Added Ordering Code Definitions . Updated to new template.
*D	3283711	RAME	06/15/2011	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated to new template.
*E	3499186	TAVA	01/17/2012	Updated Product Portfolio . Updated Package Diagram .
*F	3874351	NILE	01/18/2013	Updated Package Diagram : spec 51-85087 – Changed revision from *D to *E.
*G	4019657	MEMJ	06/04/2013	Updated Functional Description . Updated Electrical Characteristics : Added one more Test Condition "4.5 ≤ V _{CC} ≤ 5.5, I _{OH} = -0.1 mA" for V _{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 8 and referred the same note in maximum value for V _{OH} parameter corresponding to Test Condition "4.5 ≤ V _{CC} ≤ 5.5, I _{OH} = -0.1 mA".
*H	4100920	VINI	08/21/2013	Updated Switching Characteristics : Added Note 15 and referred the same note in "Parameter" column. Updated to new template.
*I	4540548	VINI	10/28/2014	Updated Maximum Ratings : Referred Notes 4, 5 in "Supply voltage to ground potential". Updated Electrical Characteristics : Updated Note 8. Updated Switching Characteristics : Added Note 20 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Note 29 and referred the same note in Figure 8 .
*J	4575393	VINI	11/20/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Switching Waveforms : Updated Figure 5 (Added shading to BHE/BLE in the waveform).

Document History Page (continued)

Document Title: CY62136ESL MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 001-48147				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*K	5059123	NILE	12/21/2015	Update Thermal Resistance : Changed value of Θ_{JA} parameter corresponding to 44-pin TSOP II package from 77 °C/W to 57 °C/W. Changed value of Θ_{JC} parameter corresponding to 44-pin TSOP II package from 13 °C/W to 17 °C/W. Updated to new template. Completing Sunset Review.
*L	5978618	AESATMP9	11/29/2017	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2008-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.