CY3688

MoBL-USB™ TX2UL Development Kit Guide

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Contents

1. Introduction

The CY3688 MoBL-USB™ TX2UL Development Kit (DVK) is a combination of hardware and documentation, which can be used to evaluate the MoBL-USB TX2UL device and to integrate it to existing development platforms with ULPI interface.

The Cypress MoBL-USB TX2UL is a low-voltage high-speed and full-speed compatible USB 2.0 ULPI Transceiver. The TX2UL is specifically designed for mobile handset applications by offering tiny package options and low power consumption.

Due to the requirement for backward compatibility in the USB 2.0 specification, the USB 2.0 ULPI PHY functions with either a Full-Speed (12 Mbits/sec) USB host or a High-Speed (480 Mbits/sec) USB host.

1.1 Kit Components

- Development board
- Quick start guide
- CD ROM
- Power supply
- USB A to B cable

1.2 Development Board

The board can be used to interconnect to a development platform with ULPI Link. After the TX2UL device is configured, the link enumerates to the USB host PC and runs traffic. USB signal quality testing is done to confirm the quality of TX2UL eye diagram. Board schematic and layout are included in the CD ROM.

1.2.1 Connector and Jumper Definition on the Development Board

J1:100-pin T&MT connector

D3, D6, D8: Power indication

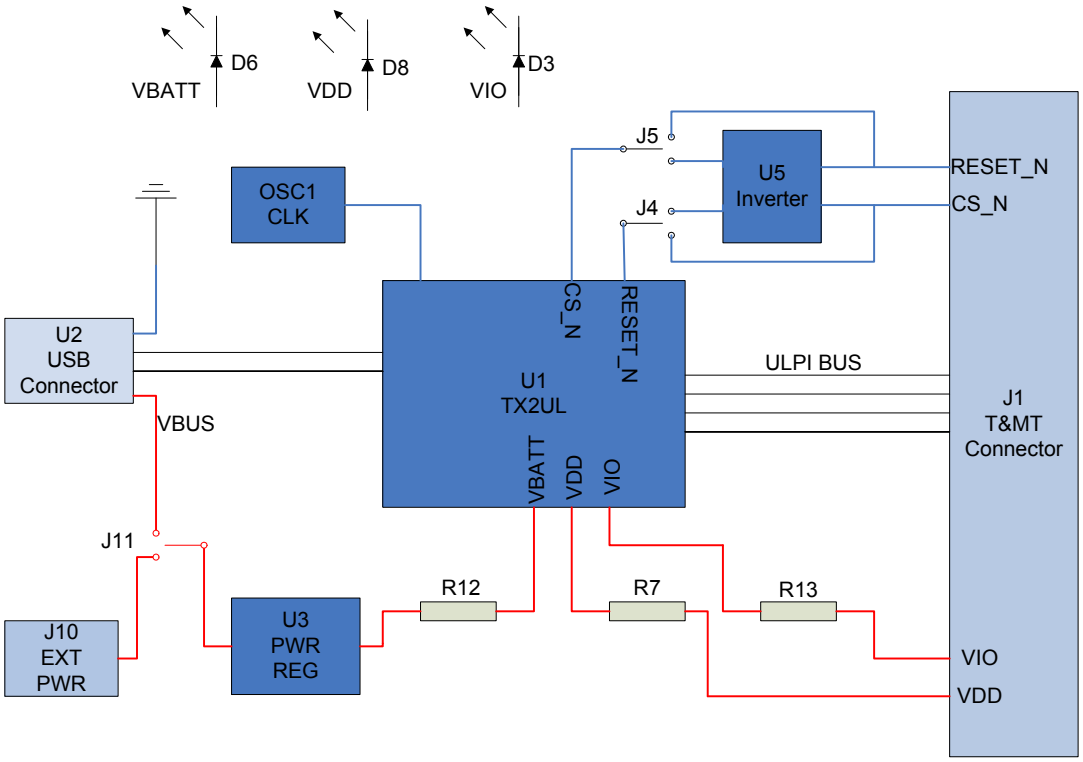
U2: USB Type B connector

J11: VBATT power supply selector

J4: Jumper for CS_N inversion for links with active high operation

J5: Jumper for RESET_N inversion for links with active high operation

Figure 1-1. Block Diagram



1.2.2 Power Supply

The TX2UL device VDD and VIO power supplies are expected to be supplied from the ULPI connector. VBATT power supply can be supplied from VBUS or the external power supply included with the kit. To power the board using VBUS, connect pin 2 and 3 of J11. Make sure the USB cable is connected to a host USB port. The other option is to use the included power supply and connect 1 and 2 of J11 (default configuration).

The system is equipped with a method to check the power consumption of the TX2UL device. Measure the voltage drop across R7, R13, and R12, this is the current consumed by VDD, VIO, and VBATT consecutively.

1.2.3 ULPI Interface

UTMI+ Low Pin Interface (ULPI) is a standard interface developed to interface a link to a USB 2.0 PHY. It supports an 8-bit wide SDR data path. The primary I/Os of this block support multirange LVCMOS signaling from 1.8 V to 3.3 V. The level used is automatically selected by the voltage applied to VIO and can be set at any voltage between 1.8 V and 3.3 V.

The ULPI interface is mapped to J1 for interconnection to development platforms. The connector pinout is as specified by the ULPI specification, page 92. Use the schematic attached in the CD/DVD ROM as a reference.

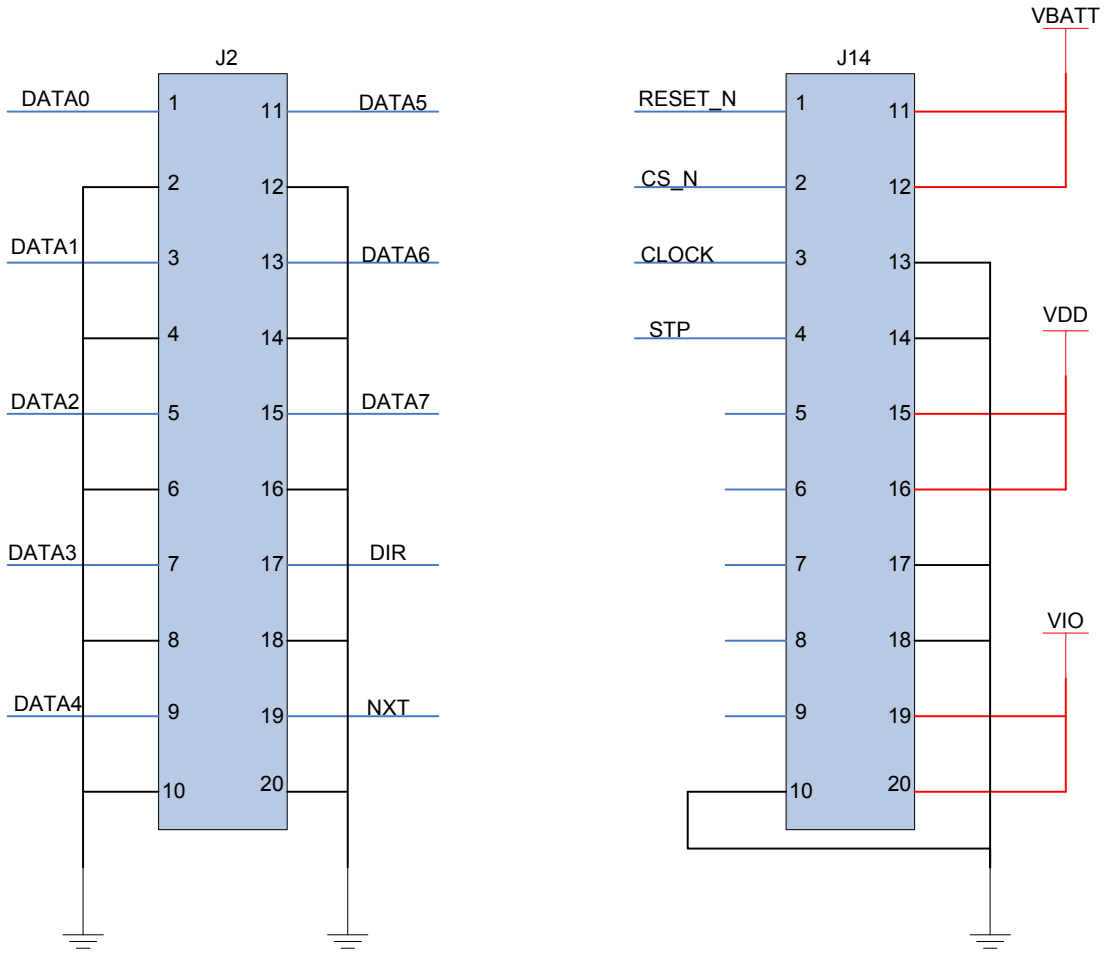
1.2.4 CS_N and RESET

The TX2UL device uses CS_N and RESET_N as active low inputs. In case this system is used with a link with active high GPIO operation, an option is available to invert these signals. The default is J4 and J5; connect 1 and 2 for direct connection from link. Connecting 2 and 3 will invert these signals.

1.2.5 Testing and Accessibility

J2 and J14 shown in the following figure are test points for debugging purposes. It can be used to connect a logic analyzer to observe the ULPI bus timing.

Figure 2. Testing and Accessibility



1.2.6 Specification

The following specifications are useful when developing with the TX2UL USB 2.0 ULPI PHY. These specifications are also found at http://www.usb.org.

- UTMI+ Low Pin Interface (ULPI) Specification, V1.1
- USB 2.0 Specification, USB Implementers Forum (USB-IF)

1.3 Document Revision History

Rev.	PDF Creation Date	Origin of Change	Description of Change
**	05/20/2008	AESA	New Guide.
*A	09/15/2009	AESA	Changed Part Number to TX2UL.
*B	05/05/2011	EYZ	Added schematic
*C	03/29/2012	HBM	Updated Chapter Title in Cover page as “CY3688 MoBL-USB™ TX2UL Development Kit Guide”. Updated Chapter Title in Chapter 1 as “Introduction”.

1.4 Documentation Conventions

Table 1. Documentation Conventions for User Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: $2 + 2 = 4$
No text, gray table cell	Represents a reserved bit in register tables.

A. Appendix

A.1 TX3 DVK Board Schematic