CY2XP12

Low RMS Phase Jitter Programmable LVPECL Clock Generator

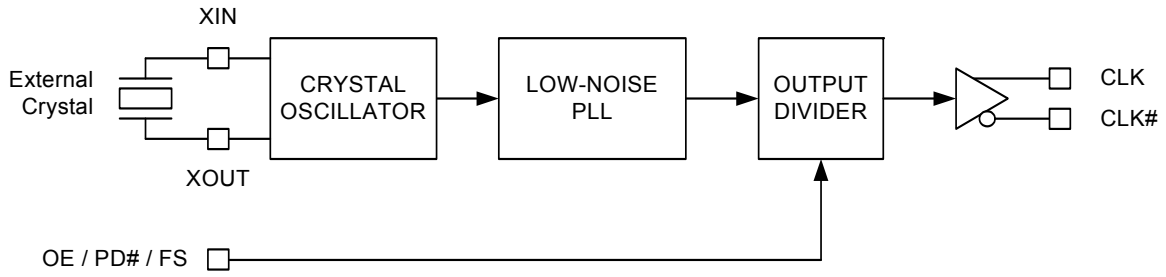
Features

- Programmable LVPECL clock generator
- Low RMS phase jitter
- Available output frequencies: 50 MHz to 700 MHz
- Pb-free 8-Pin TSSOP package
- Supply voltage: 3.3 V or 2.5 V
- Industrial temperature ranges

Functional Description

The CY2XP12 is a PLL (Phase Locked Loop) based high performance clock generator. It is optimized to generate 10 Gb Ethernet, SONET, and other high performance clock frequencies. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter, which meets both 10 Gb Ethernet and SONET jitter requirements. The CY2XP12 device has a crystal oscillator interface input and one LVPECL output pair. CY2XP12 can be programmed as Output Enable (OE), or Power Down (PD#), or Frequency Select (FS) device by configuring the pin 5. The output frequency and drive-strength of this device are also programmable.The device can be programmed either to operate at 3.3 V or at 2.5 V.

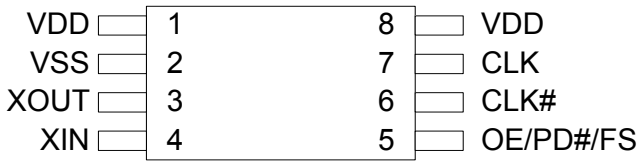
Logic Block Diagram



Contents

Pinouts

Figure 1. 8-pin TSSOP pinout



Pin Definitions

8-pin TSSOP

Pin Number	Pin Name	I/O Type	Description
1, 8	VDD	Power	3.3 V or 2.5 V power supply. All supply current flows through pin 1
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL Output and Input	Parallel resonant crystal interface
5	OE/PD#/FS	CMOS Input	Output enable pin: Active HIGH. If OE=1, CLK is enabled. When LOW, the output is high impedance. Power-down pin: Active LOW. If PD# = 0, the device is powered down and the clock is disabled. Frequency Select pin: One of the two stored frequencies can be selected.
6,7	CLK#, CLK	LVPECL Output	Differential clock output

Frequency Table

Part Number	Crystal Frequency (MHz)	Output Frequency (MHz)	Functionality of Pin 5	VDD	RMS Phase Jitter	
					Offset Range	Jitter (typical)
CY2XP12ZXI01	25	312.5	OE	3.3 V	1.875 to 20 MHz	0.3 ps
CY2XP12ZXI02	25	50	PD#	3.3 V	12 kHz to 20 MHz	1.0 ps

Functional Overview

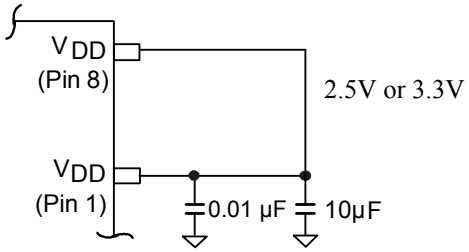
This device with external crystal option has OE or PD# or FS feature of Pin 5. The OE function is used to enable or disable CLK output. PD# function can quickly put the device in low-power state, but it takes longer time to wake-up because of reacquire of PLL lock. FS feature is used to select two different output frequencies for multirate serializer application.

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 2 illustrates a typical filtering scheme. Because all of the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 µF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 µF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

Figure 2. Power Supply Filtering



Termination for LVPECL Output

The CY2XP12 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm dc termination on each of the two output signals. For 3.3 V operation, this data sheet specifies output levels for termination to V_{DD}–2.0 V. This same termination voltage can also be used for V_{DD} = 2.5 V operation, or it can be terminated to V_{DD}-1.5 V. Note that it is also possible to terminate with 50 ohms to ground (V_{SS}), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance (Z_0) should match the termination impedance. Figure 3 and Figure 4 shows a standard termination scheme.

Figure 3. LVPECL Output Termination for 3.3V Supply

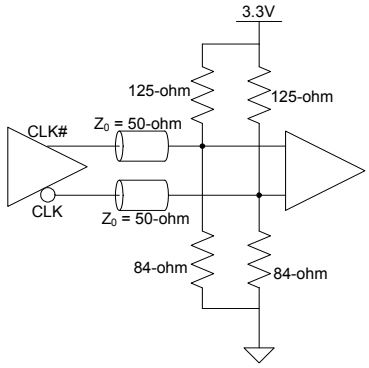
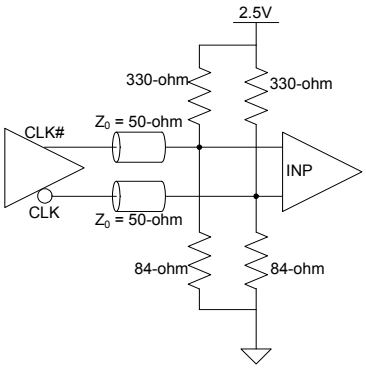


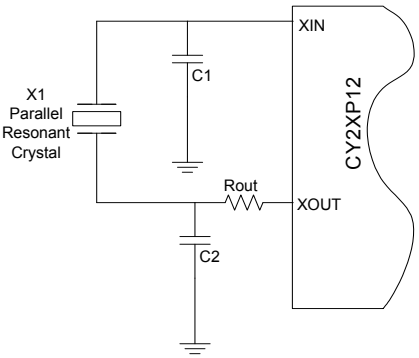
Figure 4. LVPECL Output Termination for 2.5V Supply



Crystal Input Reference

CY2XP12 should have minimum 8 pF load capacitor parallel to the resonant crystal. The capacitors C1 and C2 as shown in Figure 5 are chosen to minimize the ppm error. These values can be derived based on the parasitic trace capacitance (Cp), and capacitance of the CY2XP12 device pins (XIN and XOUT). Values of C1 and C2 are layout dependant and can be calculated as C1=C2=2*CL - Cp. When the drive level of the crystal is low and the drive level of CY2XP12 is high, the application may need an additional resistor Rout. When Rout is added, C2 is also required to be readjusted for the precise frequency calculation.

Figure 5. Crystal Input Interface



Termination Circuits

Figure 6. 3.3 V Output Load AC Test Circuit

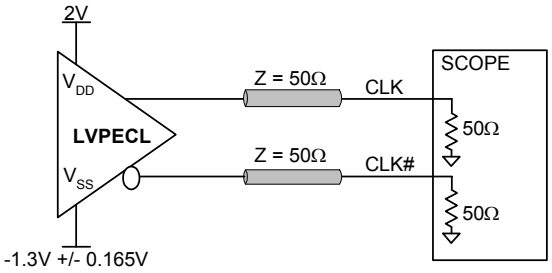
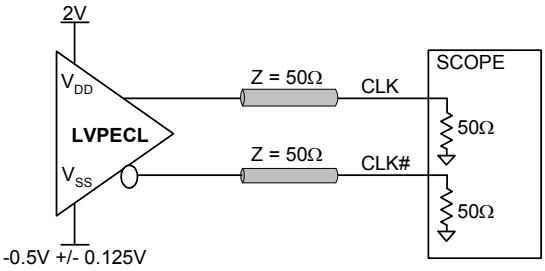


Figure 7. 2.5 V Output Load AC Test Circuit



Absolute Maximum Conditions

Parameter	Description	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non operating	–65	150	°C
T_J	Temperature, Junction		–	135	°C
ESD_{HBM}	ESD Protection, Human Body Model	JEDEC STD 22-A114-B	2000	–	V
UL–94	Flammability Rating	At 1/8 in.	V–0		
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	3.3 V Supply Voltage	3.135	3.465	V
	2.5 V Supply Voltage	2.375	2.625	V
T_A	Ambient Temperature, Industrial	–40	85	°C
T_{PU}	Power-up time for all V_{DD} to reach minimum specified voltage (ensure power ramps is monotonic)	0.05	500	ms

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current with Output Unterminated	V_{DD} = 3.465 V, OE = V_{DD}, output unterminated	–	–	125	mA
		V_{DD} = 2.625 V, OE = V_{DD}, output unterminated	–	–	120	mA
I_{DDT}	Operating Supply Current with Output Terminated	V_{DD} = 3.465 V, OE = V_{DD}, output terminated	–	–	150	mA
		V_{DD} = 2.625 V, OE = V_{DD}, output terminated	–	–	145	mA
I_{SB}	Standby supply current.	PD# = Vss			200	µA
V_{OH}	LVPECL Output High Voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} –1.15	–	V_{DD} – 0.75	V
V_{OL}	LVPECL Output Low Voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} – 2.0	–	V_{DD} – 1.625	V
V_{OD1}	LVPECL Peak-to-Peak Output Voltage Swing	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	600	–	1000	mV
V_{OD2}	LVPECL Output Voltage Swing (V_{OH} – V_{OL})	V_{DD} = 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 1.5 V	500	–	1000	mV
V_{OCM}	LVPECL Output Common Mode Voltage (V_{OH} + V_{OL})/2	V_{DD} = 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 1.5 V	1.2	–	–	V
I_{OZ}	LVPECL Output Leakage Current	Output off, OE = V_{SS}	–35	–	35	µA
V_{IH}	Input High Voltage, OE Pin		0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage, OE Pin		–0.3	–	0.3 × V_{DD}	V
I_{IH}	Input High Current, OE Pin	OE = V_{DD}	–	–	115	µA
I_{IL}	Input Low Current, OE Pin	OE = V_{SS}	–50	–	–	µA
C_{IN}[5]	Input Capacitance, OE Pin		–	15	–	pF
C_{INX}[5]	Pin Capacitance, XIN & XOUT		–	4.5	–	pF

Note
3. Refer to Figure 9 on page 9.

AC Electrical Characteristics

Parameter [5]	Description	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		Refer Frequency Table			
T_R, T_F [3]	Output Rise or Fall Time	20% to 80% of full output swing	–	0.5	1.0	ns
$T_{Jitter(\phi)}$ [6]	RMS Phase Jitter (Random)	312.5 MHz, (1.875 to 20 MHz)	Refer Frequency Table			
T_{DC} [7]	Output Duty Cycle	Measured at zero crossing point	45	–	55	%
T_{OHZ}	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T_{OE}	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time $V_{DD} = V_{DD}$(min.)	–	–	5	ms

Recommended Crystal Specifications

For SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
F_{IN}	Crystal frequency	8–14	14–28	28–48	MHz
R1	Maximum motional resistance (ESR)	135	50	30	Ω
CL	Parallel load capacitance (see Note 4 below)	8–18	8–14	8–12	pF
DL(max)	Maximum crystal drive level	300	300	300	µW

Notes
4. Guaranteed by design but not 100% tested.
5. Not 100% tested, guaranteed by design and characterization.
6. Refer to Figure 10 on page 9.
7. Refer to Figure 11 on page 9.

Switching Waveforms

Figure 8. Output DC Parameters

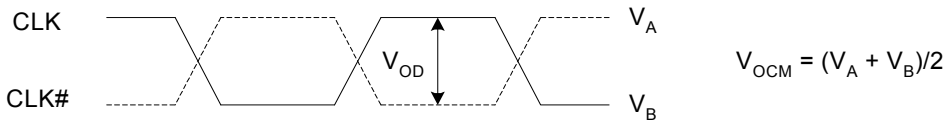


Figure 9. Output Rise and Fall Time

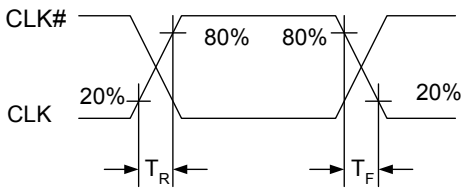


Figure 10. RMS Phase Jitter

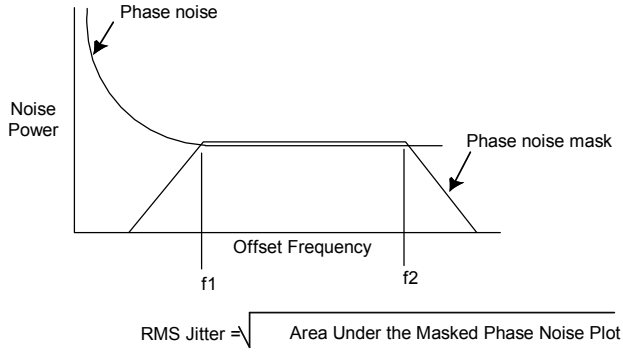


Figure 11. Output Duty Cycle

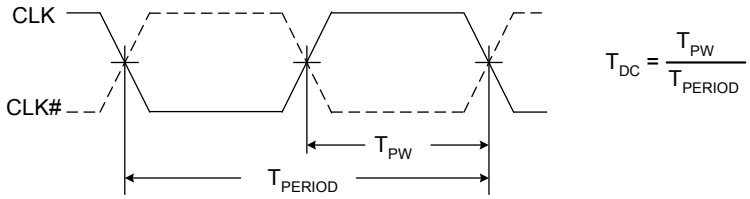
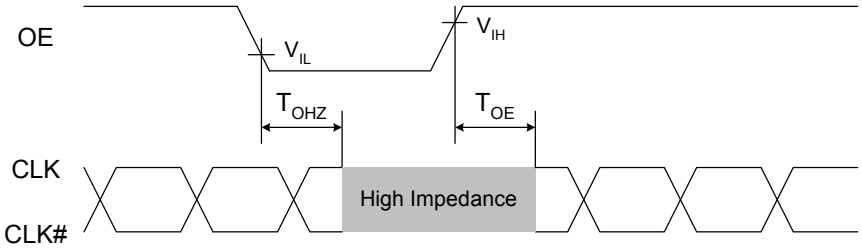


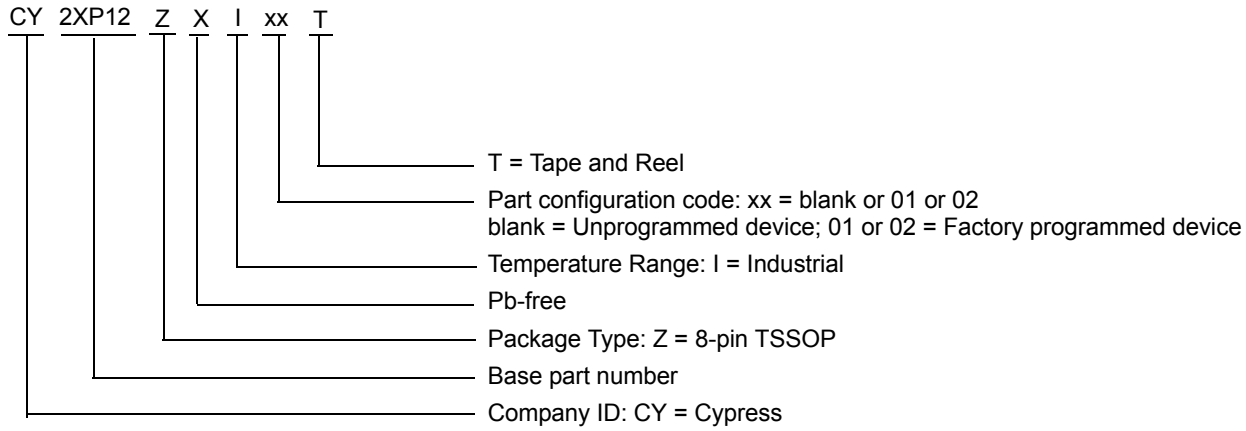
Figure 12. Output Enable Timing



Ordering Information

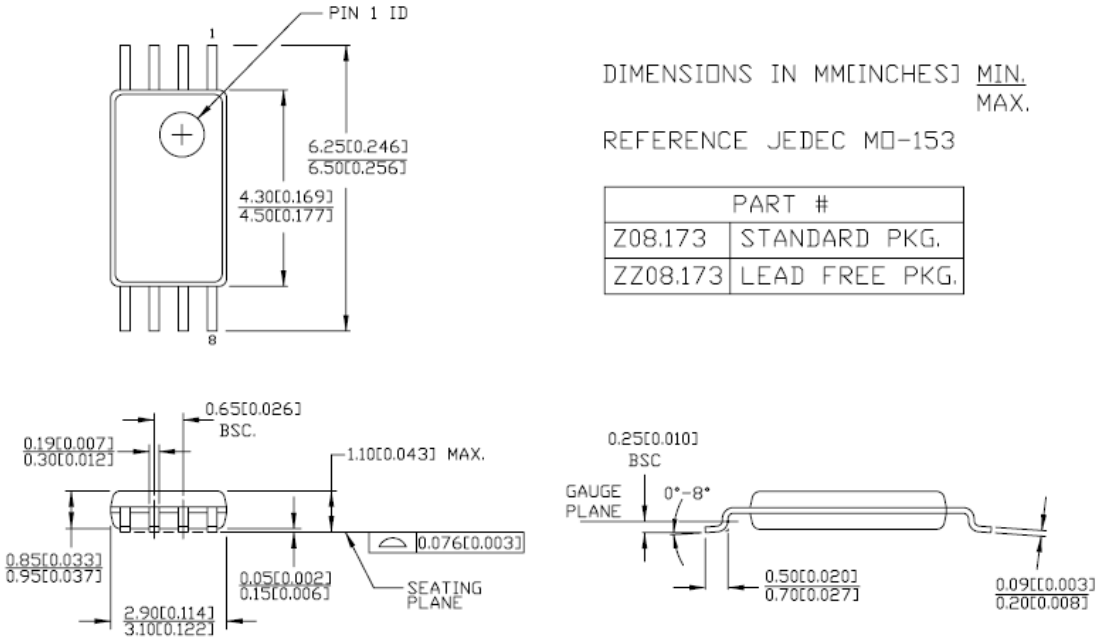
Part Number	Package Type	Product Flow
CY2XP12ZXI	8-pin TSSOP (Unprogrammed device)	Industrial, -40°C to 85°C
CY2XP12ZXIT	8-pin TSSOP – Tape and Reel (Unprogrammed device)	Industrial, -40°C to 85°C
CY2XP12ZX01	8-pin TSSOP (Factory Programmed device)	Industrial, -40°C to 85°C
CY2XP12ZX01T	8-pin TSSOP – Tape and Reel (Factory Programmed device)	Industrial, -40°C to 85°C
CY2XP12ZX02	8-pin TSSOP (Factory Programmed device)	Industrial, -40°C to 85°C
CY2XP12ZX02T	8-pin TSSOP – Tape and Reel (Factory Programmed device)	Industrial, -40°C to 85°C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 13. 8-pin TSSOP (4.40 mm Body) Z08.173/ZZ08.173 Package Outline, 51-85093



51-85093 *E

Acronyms

Table 1. Acronyms Used

Acronym	Description
CLKOUT	Clock Output
CMOS	Complementary Metal Oxide Semiconductor
DPM	Die Pick Map
EPROM	Erasable Programmable Read Only Memory
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
NTSC	National Television System Committee
OE	Output Enable
PAL	Phase Alternate Line
PD	Power-Down
PLL	Phase Locked Loop
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2XP12, Low RMS Phase Jitter Programmable LVPECL Clock Generator Document Number: 001-96954				
Revision	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	4700590	03/25/2015	TAVA	New data sheet.

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