CY241V8A-11

MPEG Clock Generator with VCXO

Features

- Integrated phase locked loop (PLL)
- Low jitter, high accuracy outputs
- VCXO with analog adjust
- 3.3 V operation

Benefits

- Highest performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Application compatibility for a wide variety of designs

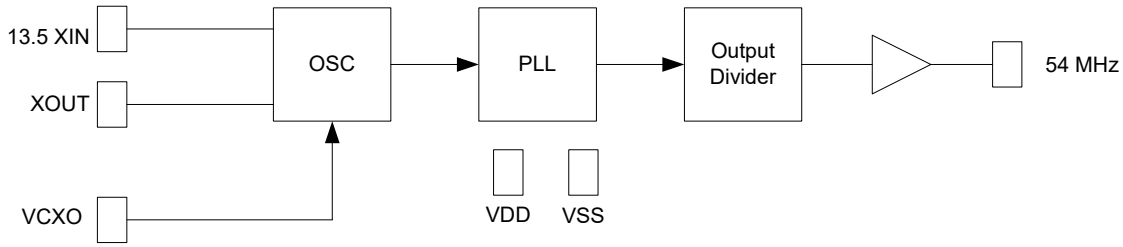
Functional Description

For a complete list of related documentation, click here.

Frequency Table

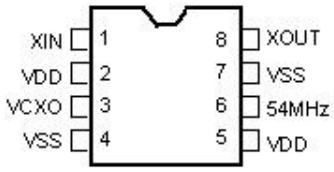
Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Control Curve	Other Features
CY241V8A-11	1	13.5 MHz pullable crystal input per Cypress specification	One copy of 54 MHz	linear	Pinout-compatible with CY2411

Block Diagram



Pin Configuration

Figure 1. 8-pin SOIC pinout



Pin Descriptions

Name	Pin Number	Description
XIN	1	Reference crystal input
VDD	2, 5	Voltage supply
VCXO	3	Input analog control for VCXO
VSS	4, 7	Ground
54 MHz	6	54 MHz clock output
XOUT	8	Reference crystal output

Absolute Maximum Conditions

Supply voltage (V_{DD}) ..... –0.5 to +7.0 V
DC input voltage ..... –0.5 V to V_{DD} + 0.5 V
Storage temperature (Non-condensing) ..... –55 °C to +125 °C
Junction temperature ..... –40 °C to +125 °C
Data retention at Tj = 125 °C ..... > 10 years
Package power dissipation ..... 350 mW
ESD (human body model) MIL-STD-883 ..... > 2000 V

Pullable Crystal Specifications

Parameter [1]	Description	Comments	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	13.5	–	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	–
DL	Crystal drive level	No external series resistor assumed	150	–	–	µW
F_{3SEPHI}	Third overtone separation from 3 × F_{NOM}	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from 3 × F_{NOM}	Low side	–	–	–150	ppm
C_0	Crystal shunt capacitance		–	–	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	–	250	–
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VDD	Operating voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	0	–	70	°C
C_{LOAD}	Max load capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD} pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Name	Description	Min	Typ	Max	Unit
I_{OH}	Output HIGH current	V_{OH} = V_{DD} – 0.5 V, V_{DD} = 3.3 V	12	24	–	mA
I_{OL}	Output LOW current	V_{OL} = 0.5 V, V_{DD} = 3.3 V	12	24	–	mA
C_{IN}	Input capacitance	Except XIN, XOUT pins	–	–	7	pF
V_{VCXO}	VCXO input range		0	–	V_{DD}	V
$f_{\Delta XO}$ [2]	VCXO pullability range	Low side	–	–	–115	ppm
		High side	115	–	–	ppm
I_{VDD}	Supply current		–	30	35	mA

Notes
1. Crystals that meet this specification include: Ecliptek ECX-5788-13.500M,Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL,PDI HA13500XFSA14XC.
2. –115/+115 ppm assumes 2.5 pF of additional board level load capacitance. This range will be shifted down with more board capacitance or shifted up with less board capacitance.

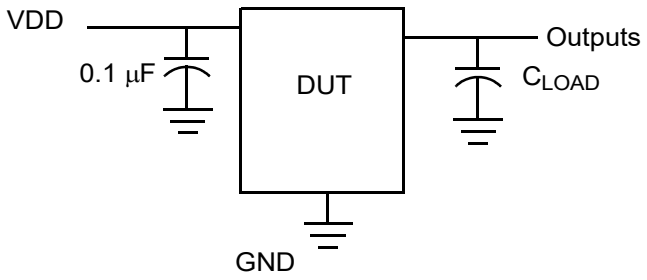
AC Electrical Specifications

(V_{DD} = 3.3 V)

Parameter [3]	Name	Description	Min	Typ	Max	Unit
DC	Output duty cycle	Duty cycle is defined in Figure 3 on page 4, 50% of V_{DD}	45	50	55	%
ER	Rising edge rate	Output clock edge rate, measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF. See Figure 4 on page 4.	0.8	1.4	–	V/ns
EF	Falling edge rate	Output clock edge rate, measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF. See Figure 4 on page 4.	0.8	1.4	–	V/ns
t_9	Clock jitter	Peak-to-peak period jitter	–	–	100	ps
t_{10}	PLL lock time		–	–	3	ms

Test and Measurement Setup

Figure 2. Test and Measurement Setup



Note
3. Not 100% tested.

Voltage and Timing Definitions

Figure 3. Duty Cycle Definition

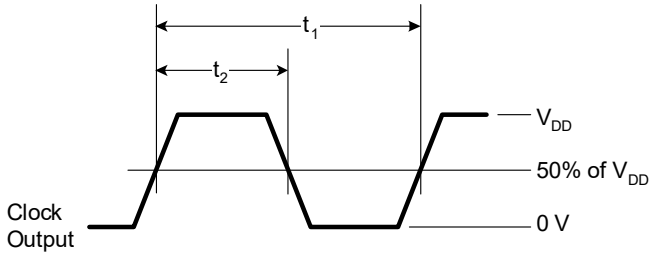
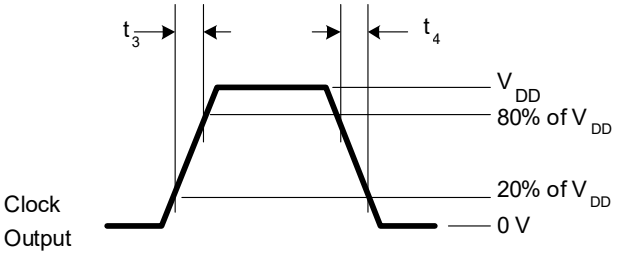


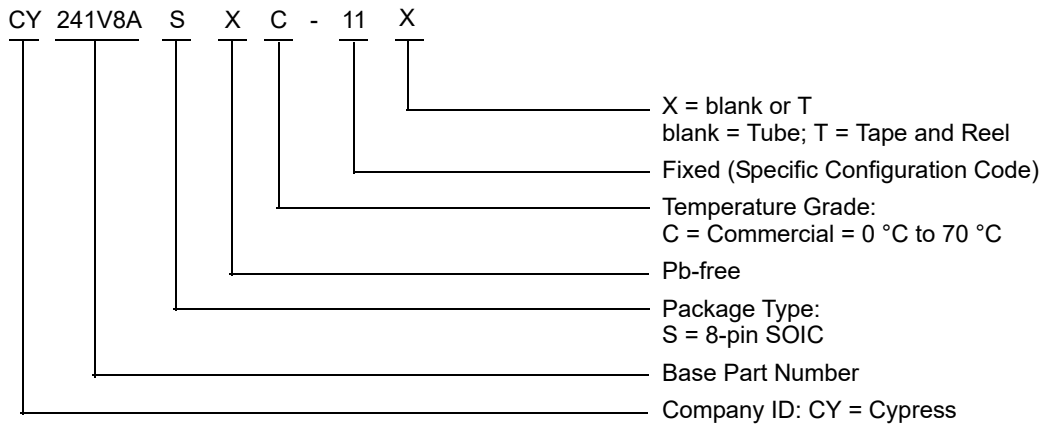
Figure 4. ER = (0.6 × V_{DD}) / t_3, EF = (0.6 × V_{DD}) / t_4



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage	Features
CY241V8ASXC-11	S8	8-pin SOIC	Commercial	3.3 V	Linear VCXO control curve
CY241V8ASXC-11T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3 V	Linear VCXO control curve

Ordering Code Definitions

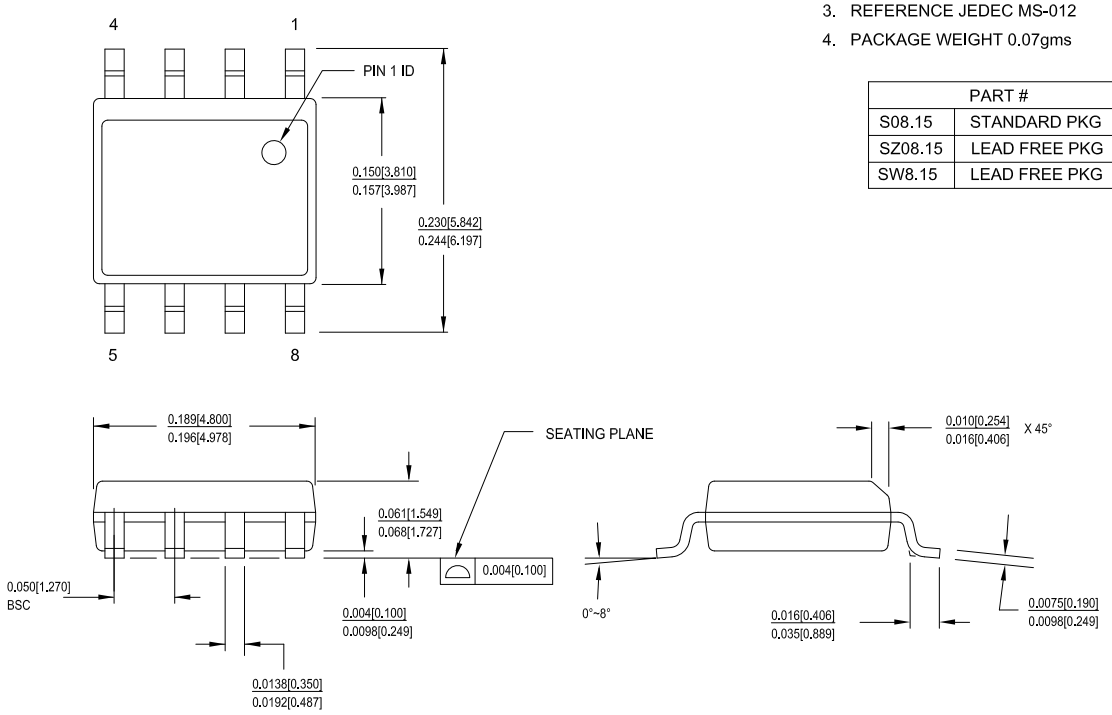


Package Drawing and Dimensions

Figure 5. 8-pin SOIC (150 Mils) S08.15/SZ08.15 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *I

Acronyms

Acronym	Description
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
PLL	Phase Locked Loop
SOIC	Small Outline Integrated Circuit
VCXO	Voltage Controlled Crystal Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
fF	femtofarad
MHz	megahertz
µF	microfarad
µW	microwatt
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt

Document History Page

Document Title: CY241V8A-11, MPEG Clock Generator with VCXO Document Number: 38-07654				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	214071	RGL	03/26/2004	New data sheet.
*A	220461	RGL	04/22/2004	Minor Change (Post to external web).
*B	2896017	CXQ	03/18/2010	Obsolete document.
*C	3000820	CXQ	08/06/2010	Reinstatement of data sheet (Activate document). Updated Ordering Information (Updated part numbers).
*D	3557456	PURU	03/21/2012	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *D to *E. Added Acronyms and Units of Measure. Removed from web (Post to internal spec system only since the part is not available on web, hence removing the data sheet from Cypress web). Completing Sunset Review.
*E	4581659	AJU	11/28/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *E to *F.
*F	4724115	TAVA	04/14/2015	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*G	6011722	PAWK	01/03/2018	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *G to *I. Updated to new template.

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