CY23FS08-06

FailSafe™ 1.8 V Zero Delay Buffer

Features

- Internal digitally compensated crystal oscillator (DCXO) for continuous glitch free operation
- Zero I/O propagation delay
- Low output cycle-to-cycle jitter (< 46 ps RMS)
- 3.84 MHz reference input
- Supports industry standard input crystals
- 122.88 MHz outputs
- Dual reference inputs
- 28-pin shrunk small outline package (SSOP)
- 1.8 V output power supplies
- 3.3 V core power supply
- Industrial temperature range

Functional Description

The CY23FS08-06 is a FailSafe zero delay buffer with two reference clock inputs and eight phase aligned outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure.

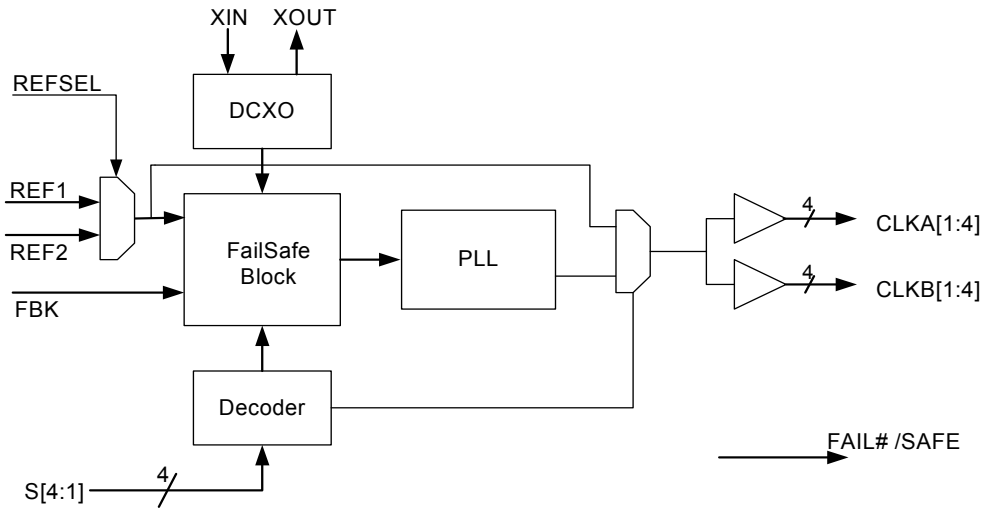
Continuous, glitch-free operation is achieved by using a DCXO that serves as a redundant clock source in the event of a reference clock failure by maintaining the last frequency and phase information of the reference clock.

The unique feature of the CY23FS08-06 is that the DCXO is in fact, the primary clocking source, that is synchronized (phase aligned) to the external reference clock. When this external clock is restored, the DCXO automatically resynchronizes to the external clock.

The frequency of the crystal that is connected to the DCXO is chosen as an integer factor of the frequency of the reference clock. This factor is set by four select lines: S[4:1]. For more information, see Configuration Table on page 4. The CY23FS08-06 has three split power supplies; one for core, another for Bank A outputs, and the third for Bank B outputs. Each output power supply, except VDDC is connected to 1.8 V. VDDC is the power supply pin for internal circuits and is connected to 3.3 V.

The CY23FS08-06 is identical to the CY23FS08-05, except that the following parameters have been removed: output-output and intrabank skew, static and dynamic phase offsets. Also, Fail#/Safe timing (Figure 3 on page 5) has been relaxed, and conditions were added to $t_{J(CC)}$ spec.

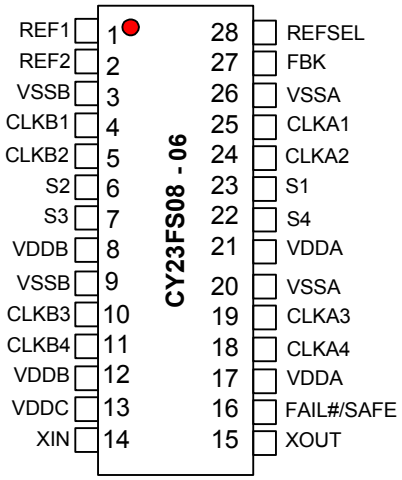
Logic Block Diagram



Contents

Pinouts

Figure 1. 28-pin SSOP pinout



Pin Definitions

28-pin SSOP

Pin Number	Pin Name	Description
1, 2	REF1, REF2	Reference clock inputs.[1] 5 V tolerant
4, 5, 10, 11	CLKB[1:4]	Bank B clock outputs.[2] CLKB3 and CLKB4 are differential signals when terminated as shown in Figure 7 on page 8. CLKB3 is negative output, CLKB4 is positive output
25, 24, 19, 18	CLKA[1:4]	Bank A clock outputs[2]
27	FBK	No connect, internal feedback
23, 6, 7, 22	S[1:4]	Frequency select pins[3]
14	XIN	Reference crystal input
15	XOUT	Reference crystal output
16	FAIL#/SAFE	Valid reference indicator. A high level indicates a valid reference input
13	VDDC	3.3 V power supply for the internal circuitry
8, 12	VDDB	1.8 V power supply for Bank B outputs
3, 9	VSSB	Ground
17, 21	VDDA	1.8 V power supply for Bank A outputs
20, 26	VSSA	Ground
28	REFSEL	Reference select. Selects the active reference clock from either REF1 or REF2. When REFSEL = 1, REF1 is selected. When REFSEL = 0, REF2 is selected[3]

Configuration Table

S[4:1]	XTAL (MHz)		REF (MHz)		Xtal/REF Ratio	OUT/REF Ratio							
	Min	Max	Min	Max		CLKA1	CLKA2	CLKA3	CLKA4	CLKB1	CLKB2	CLKB3	CLKB4
0000	15.36	16.384	3.84	4.096	4	32	32	32	32	32	32	32	32
0001	15.36	16.384	3.84	4.096	4	Off	Off	32	32	32	32	32	32
0010	15.36	16.384	3.84	4.096	4	Off	Off	Off	Off	32	32	32	32
0011	15.36	16.384	3.84	4.096	4	Off	Off	16	16	32	32	32	32
0100	15.36	16.384	3.84	4.096	4	Off	Off	Off	Off	Off	Off	32	32
0101	15.36	16.384	3.84	4.096	4	8	8	16	16	32	32	32	32
0110	15.36	16.384	3.84	4.096	4	8	8	8	8	16	16	16	16
0111	15.36	16.384	3.84	4.096	4	1	1	10	10	20	20	20	20
1xxx	-	-	-	-	-	Off	Off	Off	Off	Off	Off	Off	Off

Notes
1. Weak pull downs on these inputs.
2. Weak pull downs on all CLK outputs.
3. Weak pull ups on these inputs.

FailSafe Function

The CY23FS08-06 is targeted at clock distribution applications that can or currently require continued operation, if the main reference clock fail. Existing approaches to this requirement have used multiple reference clocks with either internal or external methods for switching between references. The problem with this technique is that it leads to interruptions (or glitches) when transitioning from one reference to another. This often requires complex external circuitry or software to maintain system stability. The technique implemented in this design completely eliminates any switching of references to the phase locked loop (PLL) that greatly simplifies the system design.

The CY23FS08-06 PLL is driven by the crystal oscillator that is phase aligned to an external reference clock. It is aligned in a way that the output of the device is effectively phase aligned to reference through the external feedback loop. This is accomplished by using a digitally controlled capacitor array to pull the crystal frequency over an approximate range of ±100 ppm from its nominal frequency.

In this mode, if the reference frequency fails (that is, stop or disappear), the DCXO maintains its last setting. Then a flag signal (FAIL#/SAFE) is set to indicate failure of the reference clock.

The CY23FS08-06 provides four select bits, S1 through S4 to control the reference to crystal frequency ratio. The DCXO is internally tuned to the phase and frequency of the external reference only when the reference frequency divided by this ratio is within the DCXO capture range. If the frequency is out of range, a flag is set on the FAIL#/SAFE pin notifying the system that the selected reference is not valid. If the reference moves in range, then the flag is cleared indicating to the system that the selected reference is valid.

Figure 2. Fail#/Safe Timing for Input Reference Failing Catastrophically

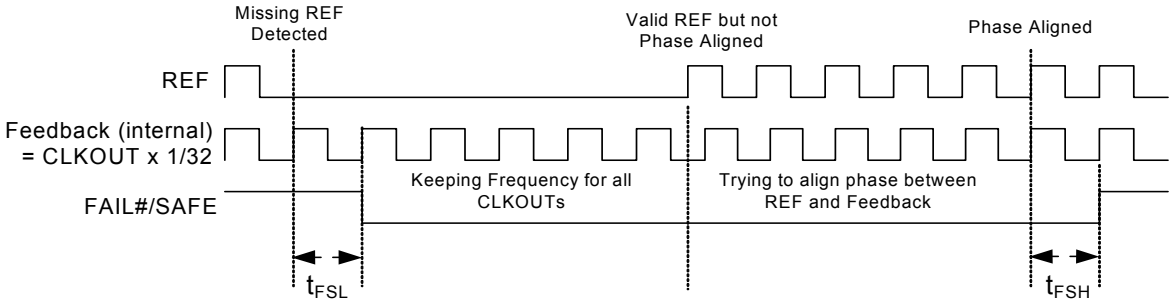


Figure 3. Fail#/Safe Timing Formula

$$t_{FSL(max)} = t_{REF} + 50\ ns$$

$$t_{FSH(min)} = t_{REF} + 50\ ns$$

Table 1. FailSafe Timing Table

Parameter	Description	Conditions	Min	Max	Unit
t_{FSL}	Fail#/Safe assert delay	Measured at 80% to 20%, Load = 15 pF	–	See Figure 3 on page 5	ns
t_{FSH}	Fail#/Safe deassert delay	Measured at 80% to 20%, Load = 15 pF	See Figure 3 on page 5	–	ns

DCXO and Capture Range

FailSafe uses a DCXO for tracking the incoming reference clock. The CY23FS08-06 is configured for a capture range of approximately +/- 100 ppm when using a pullable crystal as specified in Pullable Crystal Specifications on page 10.

Figure 4. FailSafe Timing Diagram: Input Reference Slowly Drifting Out of FailSafe Capture Range

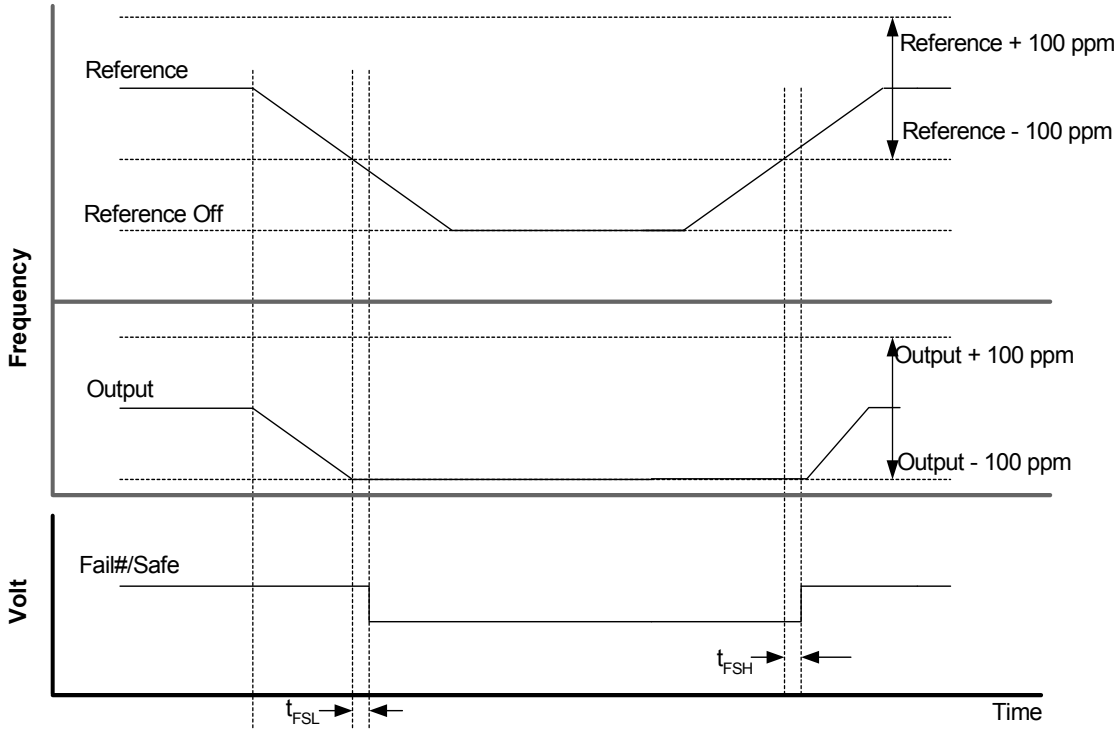


Figure 5. FailSafe Reference Switching Behavior

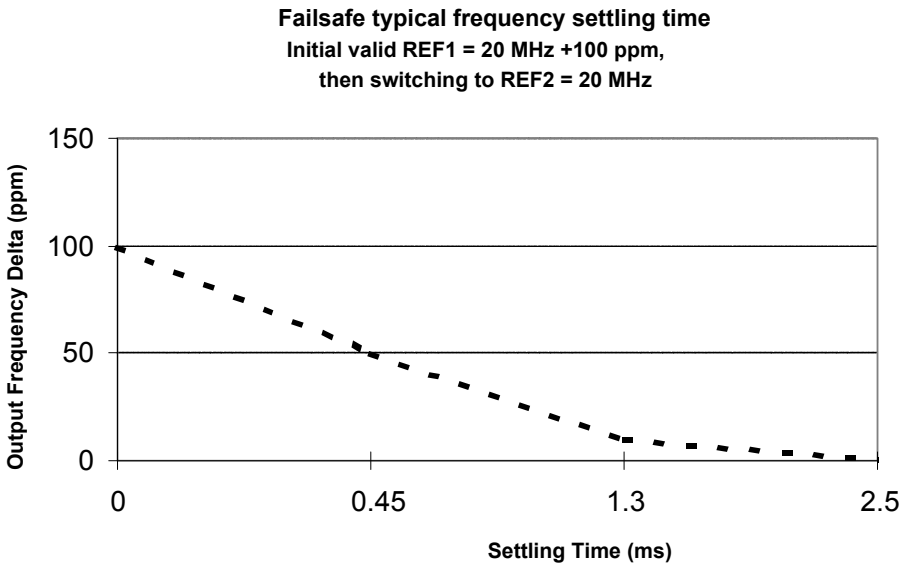


Figure 6. FailSafe Effective Loop Bandwidth (Min)

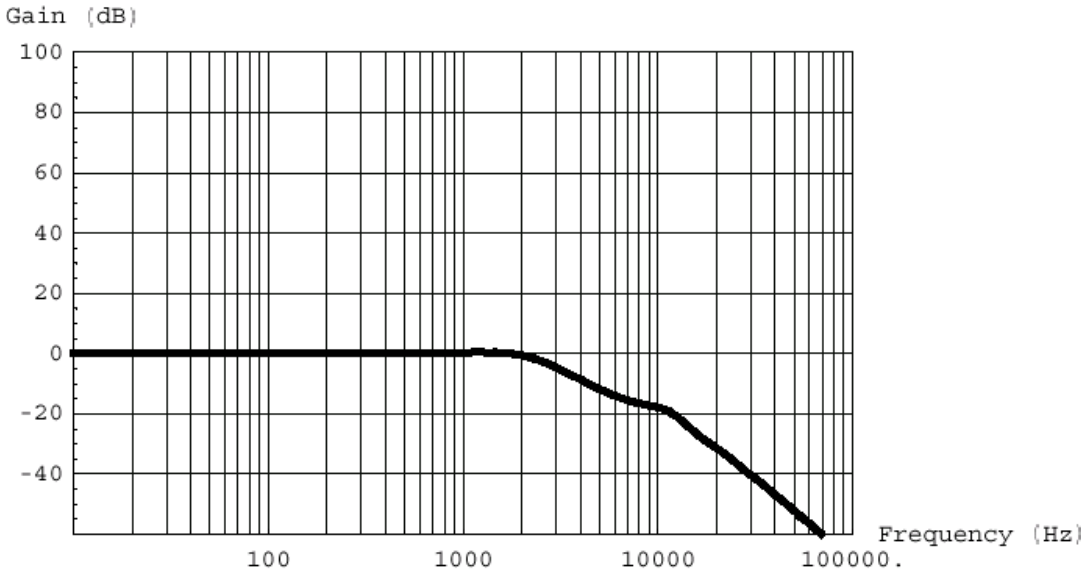
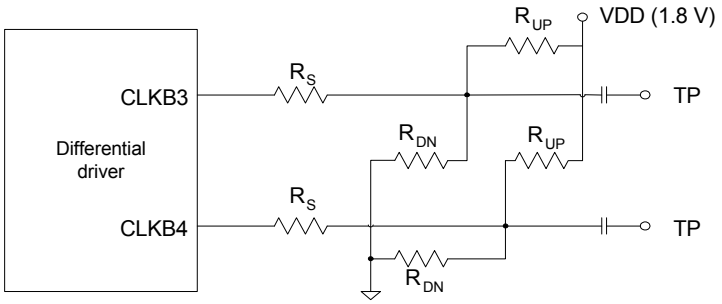
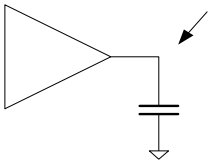


Figure 7. Output Termination for Differential Output and Measurement Setup for Single-Ended Outputs



Differential Output Termination Network for CLKB3 and CLKB4



Measurement point for single-ended clocks

Figure 8. Duty Cycle

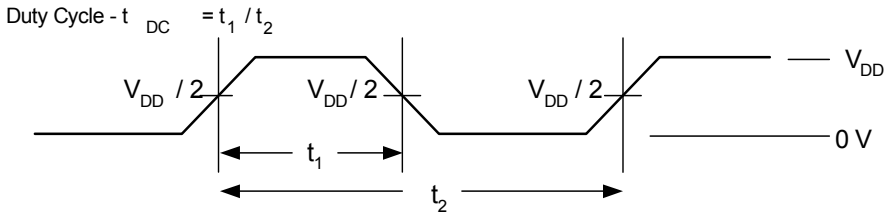


Figure 9. Input Slew Rate

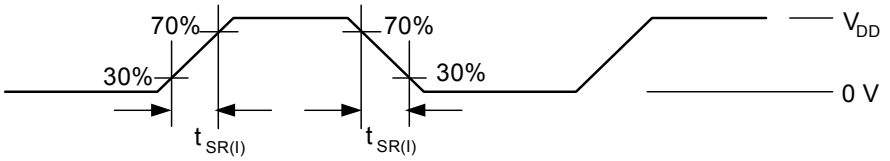
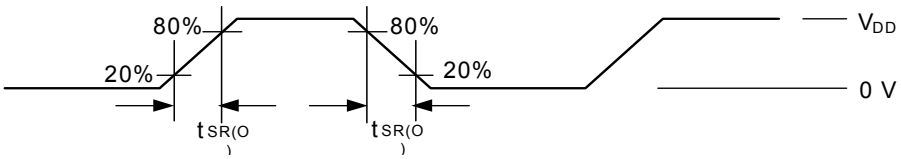


Figure 10. Output Slew Rate



Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	–	–0.5	4.6	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, storage	Non-functional	–65	150	°C
T_J	Temperature, junction	Functional	–	125	°C
ESD_{HBM}	ESD protection (human body model)	MIL-STD-883, Method 3015	2000	–	V
$Ø_{JC}$	Dissipation, junction to case	Mil-Specification 883E Method 1012.1	36.17		°C/W
$Ø_{JA}$	Dissipation, junction to ambient	JEDEC (JESD 51)	100.6		°C/W
UL–94	Flammability rating	At 1/8 in	V–0		–
MSL	Moisture sensitivity level	–	1		–

Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DDC}	3.3 V supply voltage	3.135	3.465	V
V_{DDA}, V_{DDB}	1.8 V supply voltage range	1.70	1.90	V
T_A	Ambient operating temperature, industrial	–40	85	°C
C_L	Output load capacitance	–	15	pF
C_{IN}	Input capacitance (except XIN)	–	7	pF
C_{XIN}	Crystal input capacitance (all internal caps off)	10	13	pF
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps are monotonic)	0.05	500	ms

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage	CMOS Levels, 30% of V_{DD}	–	–	0.3 × V_{DD}	V
V_{IH}	Input high voltage	CMOS Levels, 70% of V_{DD}	0.7 × V_{DD}	–	–	V
I_{IL}	Input low current	V_{IN} = V_{SS} (100 k pull-up only)	–	–	50	µA
I_{IH}	Input high current	V_{IN} = V_{DD} (100 k pull-down only)	–	–	50	µA
I_{OL}	Output low current	V_{OL} = 0.5 V, V_{DD} = 1.8 V	14	–	–	mA
I_{OH}	Output high current	V_{OH} = V_{DD} – 0.5 V, V_{DD} = 1.8 V	–	–	–12	mA
I_{DD}	Dynamic current	V_{DDA}, V_{DDB}, and V_{DDC} are all at the maximum values, I_{OUT} = 0mA, output frequency = maximum	–	–	75	mA
I_{DDQ}	Quiescent current	All inputs are grounded, PLL and DCXO are in bypass mode, reference input = 0	–	–	250	µA

Switching Characteristics

Parameter [4]	Description	Test Conditions	Min	Typ	Max	Unit
f_{REF}	Reference frequency	Industrial grade	3.8	–	4.1	MHz
f_{OUT}	Output frequency	15 pF load	3.8	–	133	MHz
f_{XIN}	DCXO frequency	–	15	–	25	MHz
t_{DC}	Duty cycle	Measured at $V_{DD}/2$	40	–	60	%
$t_{SR(I)}$	Input slew rate	Measured on REF1 Input, 30% to 70% of V_{DD}	0.5	–	4.0	V/ns
$t_{SR(O)}$	Output slew rate	Measured from 20% to 80% of V_{DD} = 1.8 V, 15 pF Load	0.3	–	3.0	V/ns
$t_{J(CC)}$	Cycle-to-cycle jitter	Load = 15 pF, $f_{OUT} \geq 62.5$ MHz, S[4:1] = 0100	–	200	250	ps
			–	18	46	ps_{RMS}

Pullable Crystal Specifications

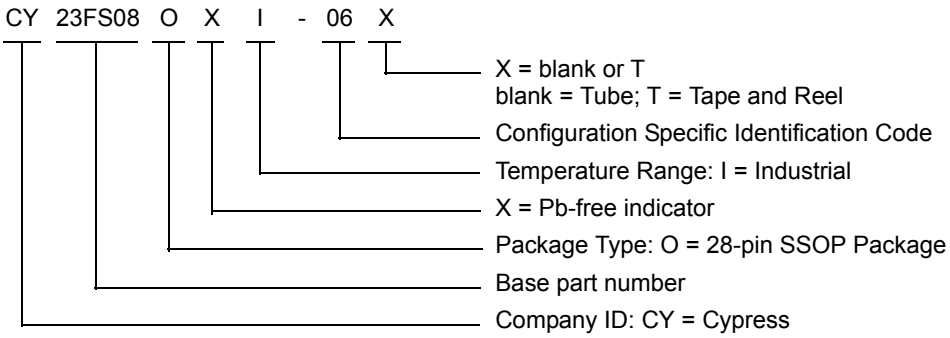
Parameter	Description	Min	Typ	Max	Unit
CR load	Crystal load capacitance	–	16	–	pF
C0/C1	C0/C1 ratio	–	240	–	–
ESR	Equivalent series resistance	–	–	50	Ω

Note
4. Parameters are guaranteed by design and characterization. Not 100% tested in production.

Ordering Information

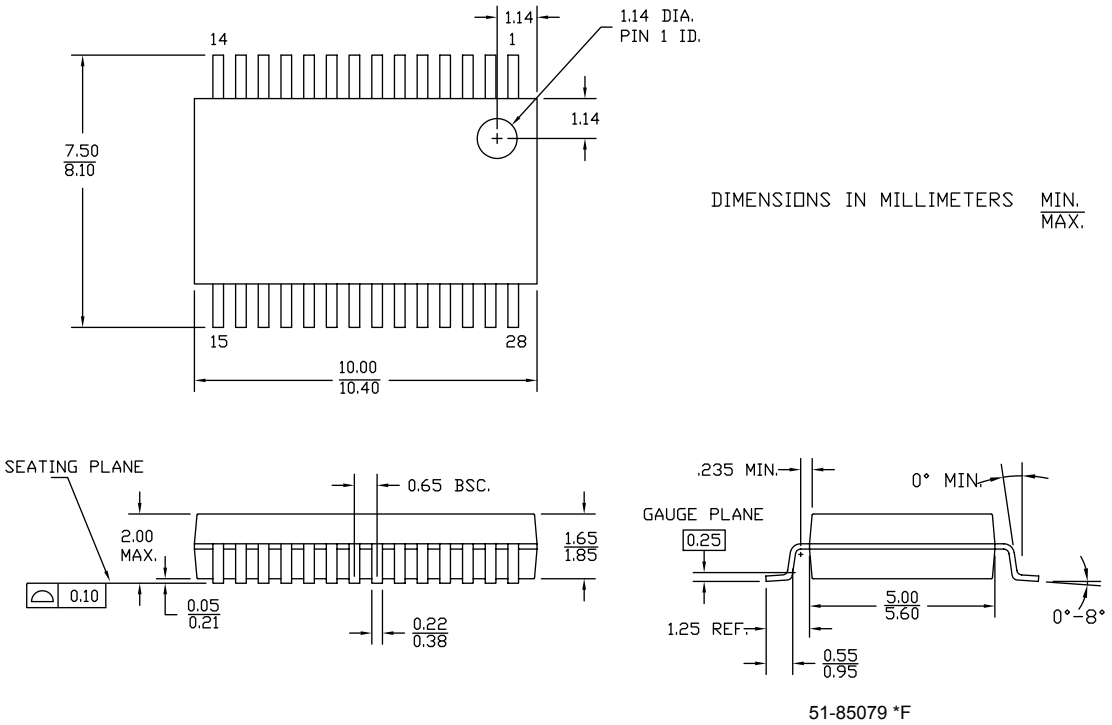
Part Number	Package Type	Product Flow
Pb-free		
CY23FS08OXI-06	28-pin SSOP	Industrial, –40 °C to 85 °C
CY23FS08OXI-06T	28-pin SSOP – Tape and Reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 11. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079



51-85079 *F

Acronyms

Acronym	Description
DCXO	Digitally Controlled Crystal Oscillator
ESD	Electrostatic Discharge
PLL	Phase Locked Loop
RMS	Root Mean Square
SSOP	Shrunk Small Outline Package
XTAL	Crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
ppm	parts per million
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY23FS08-06, FailSafe™ 1.8 V Zero Delay Buffer Document Number: 001-63589				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3007393	XHT	08/13/2010	New data sheet.
*A	3102695	BASH	12/13/2010	Changed status from Preliminary to Final.
*B	3169093	BASH	02/10/2011	Updated Electrical Characteristics: Removed typical value of I_{OL} parameter. Removed typical value of I_{OH} parameter.
*C	4149503	CINM	10/07/2013	Updated Package Drawing and Dimensions: spec 51-85079 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*D	5484823	TAVA	10/20/2016	Updated Package Drawing and Dimensions: spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*E	5975808	AESATMP9	11/24/2017	Updated logo and copyright.

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