CY2313ANZ

13 Output, 3.3 V Clock Buffer

Features

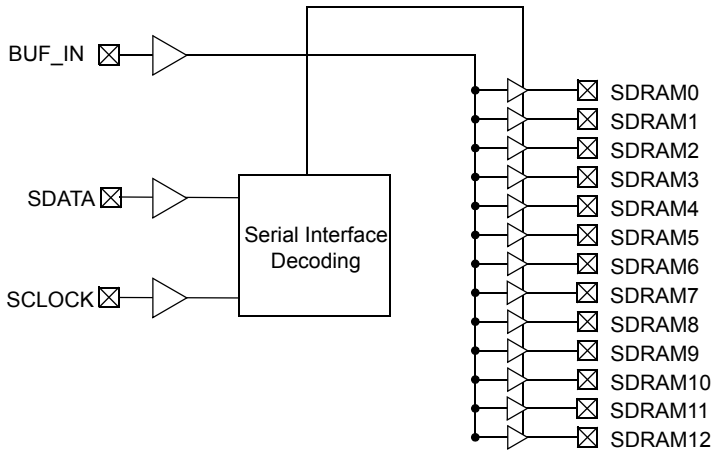
- One input to 13 output buffer/driver
- Supply voltage: 3.3 V
- Supports up to three SDRAM DIMMs
- SMBus serial interface for output control
- Low skew outputs
- Up to 100-MHz operation
- Multiple V_{DD} and V_{SS} pins for noise reduction
- Low EMI outputs
- Package: 28-pin small-outline integrated circuit (SOIC)

Functional Description

The CY2313ANZ is a 3.3 V clock buffer. While originally designed to distribute clocks in desktop PC applications - hence the signal names - it is a general purpose device suitable to a wide variety of clock buffering applications. The part has thirteen outputs. In a PC application, twelve of which can be used to drive up to three SDRAM DIMMs, and the remaining output can be used for external feedback to a PLL. The device operates at 3.3 V and outputs can run up to 100 MHz.

The CY2313ANZ also includes an SMBus serial interface which can enable or disable each output clock. On power-up, all output clocks are enabled.

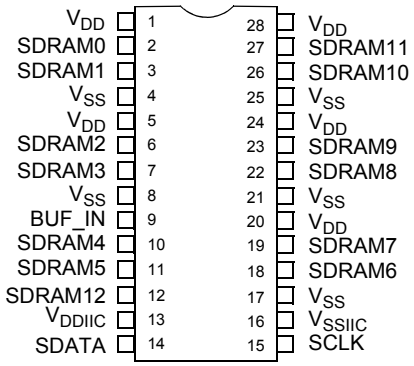
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 28-pin SOIC pinout (Top View)



Pin Summary

Name	Pins	Description
V_{DD}	1, 5, 20, 24, 28	3.3 V digital voltage supply
V_{SS}	4, 8, 17, 21, 25	Ground
V_{DDIIC}	13	Serial interface voltage supply
V_{SSIIC}	16	Ground for serial interface
BUF_IN	9	Input clock
SDATA	14	SMBus data input/output, internal pull-up to V_{DD}
SCLK	15	SMBus clock input, internal pull-up to V_{DD}
SDRAM [0-12]	2, 3, 6, 7, 10, 11, 12, 18, 19, 22, 23, 26, 27	Clock outputs

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  .

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to “0”
- Serial interface address for the CY2313ANZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	–

Byte 0:SDRAM Active/Inactive Register

(1 = Enable, 0 = Disable), Default = Enabled

Bit	Pin #	Description
Bit 7	11	SDRAM5 (active/inactive)
Bit 6	10	SDRAM4 (active/inactive)
Bit 5	–	Reserved, drive to 0
Bit 4	–	Reserved, drive to 0
Bit 3	7	SDRAM3 (active/inactive)
Bit 2	6	SDRAM2 (active/inactive)
Bit 1	3	SDRAM1 (active/inactive)
Bit 0	2	SDRAM0 (active/inactive)

Byte 1: SDRAM Active/Inactive Register

(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	27	SDRAM11 (active/inactive)
Bit 6	26	SDRAM10 (active/inactive)
Bit 5	23	SDRAM9 (active/inactive)
Bit 4	22	SDRAM8 (active/inactive)
Bit 3	–	Reserved, drive to 0
Bit 2	–	Reserved, drive to 0
Bit 1	19	SDRAM7 (active/inactive)
Bit 0	18	SDRAM6 (active/inactive)

Byte 2: SDRAM Active/Inactive Register

(1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	–	Reserved, drive to 0
Bit 6	12	SDRAM12 (active/inactive)
Bit 5	–	Reserved, drive to 0
Bit 4	–	Reserved, drive to 0
Bit 3	–	Reserved, drive to 0
Bit 2	–	Reserved, drive to 0
Bit 1	–	Reserved, drive to 0
Bit 0	–	Reserved, drive to 0

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage to ground potential .....–0.5 V to +7.0 V

DC input voltage (Except BUF_IN) .....–0.5 V to V_{DD} + 0.5 V

DC input voltage (BUF_IN) .....–0.5 V to +7.0 V

Storage temperature ..... –65 °C to +150 °C

Junction temperature ..... 150 °C

Static discharge voltage
(per MIL-STD-883, method 3015) ..... > 2000 V

Operating Conditions

Parameter [1]	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.135	3.465	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance	–	30	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage [2]	Except serial interface pins	–	0.8	V
V_{ILiic}	Input LOW voltage	For serial interface pins only	–	0.7	V
V_{IH}	Input HIGH voltage [2]		2.0	–	V
I_{IL}	Input LOW current (BUF_IN input)	V_{IN} = 0 V	–10	10	µA
I_{IL}	Input LOW current (Except BUF_IN pin)	V_{IN} = 0 V	–	100	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–10	10	µA
V_{OL}	Output LOW voltage [3]	I_{OL} = 25 mA	–	0.4	V
V_{OH}	Output HIGH voltage [3]	I_{OH} = –36 mA	2.4	–	V
I_{DD}	Supply current [3]	Unloaded outputs, 100 MHz	–	200	mA
I_{DD}	Supply current [3]	Loaded outputs, 100 MHz	–	290	mA
I_{DD}	Supply current [3]	Unloaded outputs, 66.67 MHz	–	150	mA
I_{DD}	Supply current [3]	Loaded outputs, 66.67 MHz	–	185	mA
I_{DDS}	Supply current	BUF_IN = V_{DD} or V_{SS} All other inputs at V_{DD}	–	500	µA

Notes
1. Electrical parameters are guaranteed under the operating conditions specified.
2. BUF_IN input has a threshold voltage of V_{DD}/2.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics

Over the Operating Range

Parameter [4]	Description	Test Conditions	Min	Typ	Max	Unit
	Maximum operating frequency		–	–	100	MHz
	Duty cycle [5, 6] = $t_2 \div t_1$	Measured at 1.5 V	45	50	55	%
t_3	Rising edge rate [5]	Measured between 0.4 V and 2.4 V	0.9	1.5	4.0	V/ns
t_4	Falling edge rate [5]	Measured between 2.4 V and 0.4 V	0.9	1.5	4.0	V/ns
t_5	Output to output skew[5]	All outputs equally loaded	–250	–	250	ps
t_6	SDRAM buffer LH propagation delay [5]	Input edge greater than 1 V/ns	1.0	3.5	5.0	ns
t_7	SDRAM buffer HL propagation delay [5]	Input edge greater than 1 V/ns	1.0	3.5	5.0	ns

Notes
4. All parameters specified with loaded outputs.
5. Parameter is guaranteed by design and characterization. Not 100 percent tested in production.
6. Duty cycle of input clock is 50 percent. Rising and falling edge rate of the input clock is greater than 1 V/ns.

Switching Waveforms

Figure 2. Duty Cycle Timing

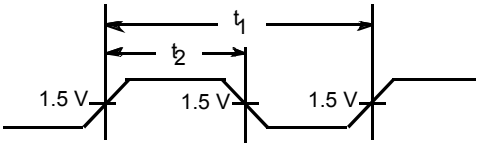


Figure 3. All Outputs Rise/Fall Time

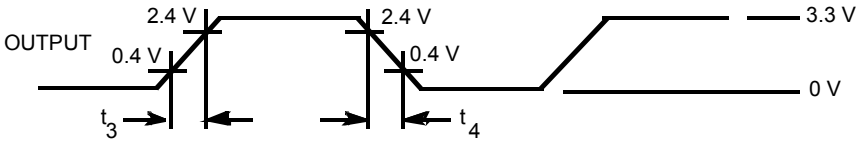


Figure 4. Output-Output Skew

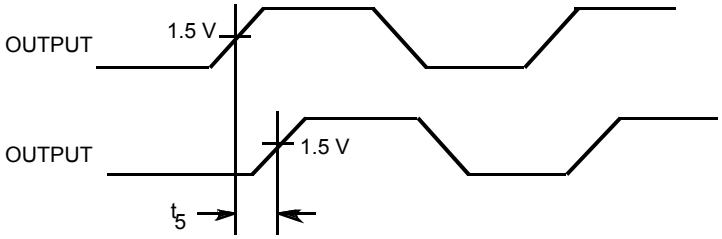
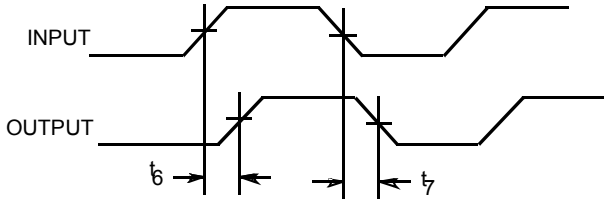
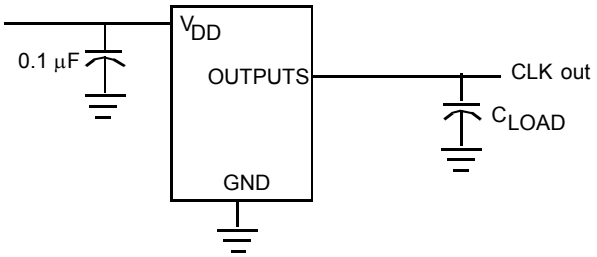


Figure 5. SDRAM Buffer LH and HL Propagation Delay



Test Circuit



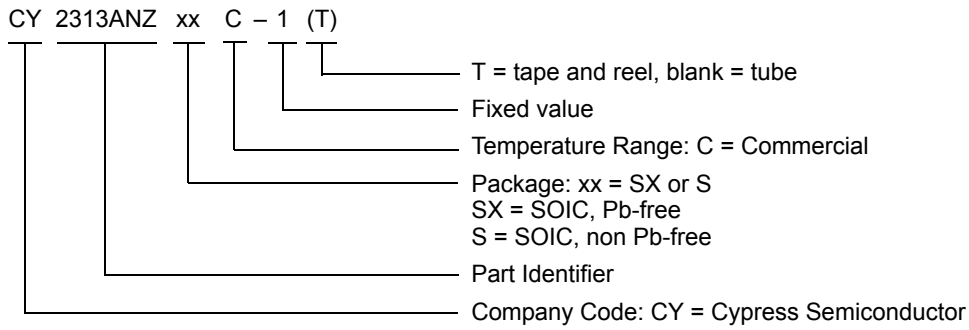
Application Information

- Clock traces may require either series or parallel termination. An IBIS model is available for simulation.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the buffer (typically 25 Ω), and Rseries is the series terminating resistor.
  Rseries > Rtrace – Rout
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A ferrite bead may be used to isolate the board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50 Ω impedance at the clock frequency, under loaded DC conditions. Refer to the application note Layout and Termination Techniques for Cypress Clock Generators for more details.
- If a Ferrite Bead is used, a 10 µF to 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Ordering Information

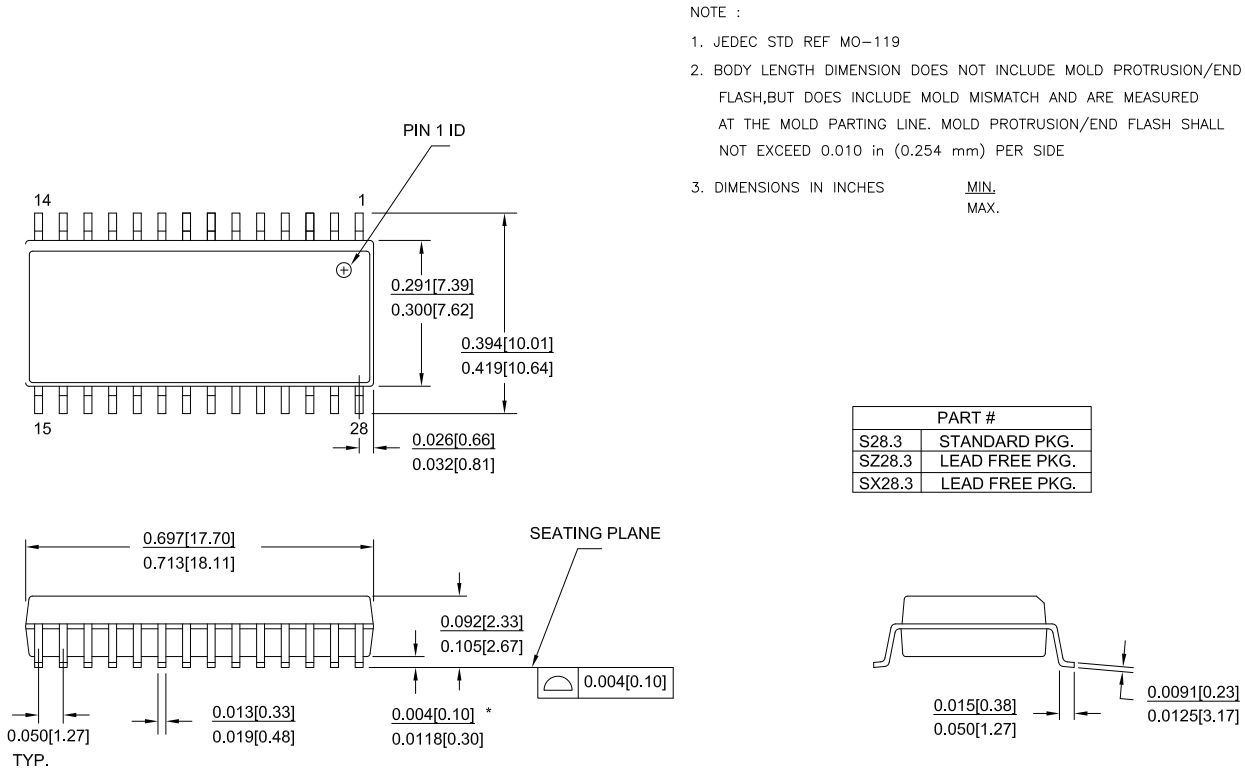
Ordering Code	Package Type	Operating Range
CY2313ANZSC–1	28-pin SOIC	Commercial, 0 °C to 70 °C
Pb-free		
CY2313ANZSXC–1	28-pin SOIC	Commercial, 0 °C to 70 °C
CY2313ANZSXC–1T	28-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Diagram

Figure 6. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026



Acronyms

Acronym	Description
DIMM	Dual In-line Memory Module
PC	Personal Computer
PLL	Phase-Locked Loop
SDRAM	Synchronous Dynamic Random Access Memory
SOIC	Small-Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt

Document History Page

Document Title: CY2313ANZ, 13 Output, 3.3 V Clock Buffer Document Number: 38-07144				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110253	11/18/01	DSG	Change from Spec number: 38-00692 to 38-07144
*A	121831	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*B	1244583	See ECN	DPF	Added Pb-free part numbers in the Ordering Information
*C	3022355	09/14/2010	KVM	Changed title from “13 Output, 3.3 V SDRAM Buffer for Desktop PCs with Three DIMMs” to “13 Output, 3.3 V Clock Buffer” Clarified that the serial interface is SMBus Removed timing parameters and waveforms that were not applicable Added Ordering Code Definitions. Updated Package Diagram. Added Acronyms and Units of Measure. Minor edits and updated in new template
*D	4141810	09/30/2013	CINM	Updated Package Diagram: spec 51-85026 – Changed revision from *E to *G. Updated in new template. Completing Sunset Review.

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