SUMMARY

CY15B256Q

256-Kbit (32K × 8) Automotive-E Serial (SPI) F-RAM

Features

- 256-Kbit ferroelectric random access memory (F-RAM) logically organized as 32K × 8
  - High-endurance 10 trillion (10^{13}) read/writes
  - 121-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Very fast serial peripheral interface (SPI)
  - Up to 33-MHz frequency
  - Direct hardware replacement for serial flash and EEPROM
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Sophisticated write-protection scheme
  - Hardware protection using the Write Protect ($\overline{WP}$) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4, 1/2, or entire array
- Device ID
  - Manufacturer ID and Product ID
- Low power consumption
  - 5-mA active current at 33 MHz
  - 500-µA standby current
  - 12-µA sleep mode current
- Low-voltage operation: V_{DD} = 2.7 V to 3.6 V
- Automotive-E temperature: –40 °C to +125 °C
- 8-pin small outline integrated circuit (SOIC) package
- AEC Q100 Grade 1 compliant
- Restriction of hazardous substances (RoHS) compliant

Functional Overview

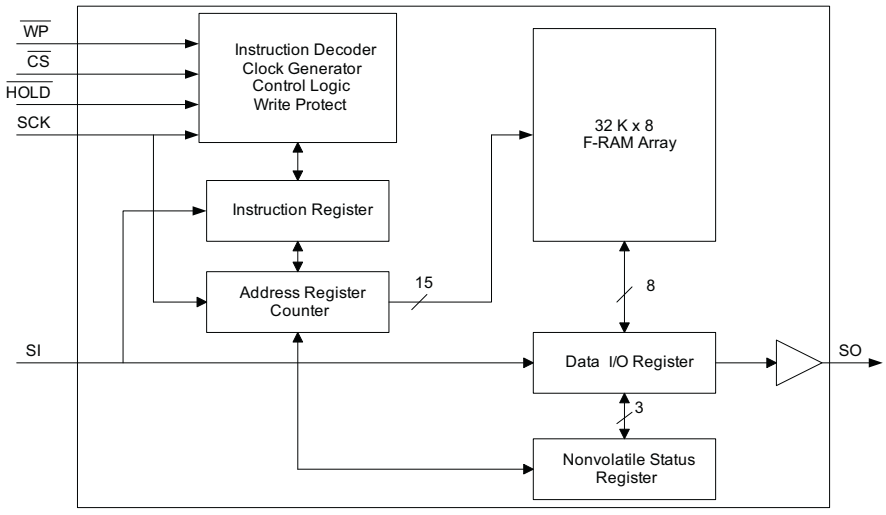
The CY15B256Q is a 256-Kbit nonvolatile memory employing an advanced ferroelectric process. An F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 121 years while eliminating the complexities, overhead, and system-level reliability problems caused by serial flash, EEPROM, and other nonvolatile memories.

Unlike serial flash and EEPROM, the CY15B256Q performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. The CY15B256Q is capable of supporting 10^{13} read/write cycles, or 10 million times more write cycles than EEPROM.

These capabilities make the CY15B256Q ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data logging, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash or EEPROM can cause data loss.

The CY15B256Q provides substantial benefits to users of serial EEPROM or flash as a hardware drop-in replacement. The CY15B256Q uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The device incorporates a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The device specifications are guaranteed over an automotive-e range of –40 °C to +125 °C.

Logic Block Diagram



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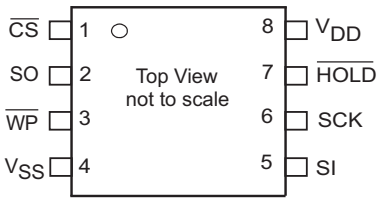
Pinout

Figure 1. 8-pin SOIC Pinout



Pin Definitions

Pin Name	I/O Type	Description
SCK	Input	**Serial Clock**. All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Because the device is synchronous, the clock frequency may be any value between 0 and 33 MHz and may be interrupted at any time.
$\overline{CS}$	Input	**Chip Select**. This active LOW input activates the device. When HIGH, the device enters the low-power standby mode, ignores other inputs, and the output is tristated. When LOW, the device internally activates the SCK signal. A falling edge on $\overline{CS}$ must occur before every opcode.
SI[1]	Input	**Serial Input**. All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet I_{DD} specifications.
SO[1]	Output	**Serial Output**. This is the data output pin. It is driven during a read and remains tristated at all other times including when $\overline{HOLD}$ is LOW. Data transitions are driven on the falling edge of the serial clock.
$\overline{WP}$	Input	**Write Protect**. This active LOW pin prevents write operation to the Status Register when WPEN is set to '1'. This is critical because other write protection features are controlled through the Status Register. A complete explanation of write protection is provided on Status Register and Write Protection on page 7. This pin must be tied to V_{DD} if not used.
$\overline{HOLD}$	Input	**HOLD Pin**. The $\overline{HOLD}$ pin is used when the host CPU must interrupt a memory operation for another task. When $\overline{HOLD}$ is LOW, the current operation is suspended. The device ignores any transition on SCK or $\overline{CS}$. All transitions on $\overline{HOLD}$ must occur while SCK is LOW. This pin has a weak internal pull-up (refer to the R_{IN} spec in DC Electrical Characteristics).
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Note
1. SI may be connected to SO for a single pin data interface.

Overview

The CY15B256Q is a serial F-RAM memory. The memory array is logically organized as 32,768 × 8 bits and is accessed using an industry-standard serial peripheral interface (SPI) bus. The functional operation of the F-RAM is similar to serial flash and serial EEPROMs. The major difference between the CY15B256Q and a serial flash or EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing the CY15B256Q, the user addresses 32K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an opcode, and a two-byte address. The upper bit of the address range is 'don't care' value. The complete address of 15 bits specifies each byte address uniquely.

Most functions of the CY15B256Q are either controlled by the SPI interface or are handled by on-board circuitry. The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike a serial flash or EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in Memory Operation on page 8.

Serial Peripheral Interface - SPI Bus

The CY15B256Q is a SPI slave device and operates at speeds up to 33 MHz. This high-speed serial bus provides high-performance serial communication to a SPI master. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The CY15B256Q operates in SPI Mode 0 and 3.

SPI Overview

The SPI is a four-pin interface with Chip Select ($\overline{CS}$), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

The SPI is a synchronous serial interface, which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on the SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both of these modes, data is clocked into the F-RAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated, the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms in the SPI protocol are as follows:

SPI Master

The SPI master device controls the operations on a SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All of the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. An SPI slave never initiates a communication on the SPI bus and acts only on the instruction from the master.

The CY15B256Q operates as an SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{CS}$)

To select any slave device, the master needs to pull down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active Chip Select cycle.

Serial Clock (SCK)

The Serial Clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

The CY15B256Q enables SPI modes 0 and 3 for data communication. In both of these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of a SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission (SI/SO)

The SPI data bus consists of two lines, SI and SO, for serial data communication. SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

The CY15B256Q has two separate pins for SI and SO, which can be connected with the master as shown in Figure 2.

For a microcontroller that has no dedicated SPI bus, a general-purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together and tie off (HIGH) the $\overline{HOLD}$ and $\overline{WP}$ pins. Figure 3 shows such a configuration, which uses only three pins.

Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the Most Significant Bit (MSB). This is valid for both address and data transmission.

The 256-Kbit serial F-RAM requires a 2-byte address for any read or write operation. Because the address is only 15 bits, the upper bit which is fed in is ignored by the device. Although the upper bit is 'don't care', Cypress recommends that these bits be set to 0s to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY15B256Q uses the standard opcodes for memory accesses.

Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin until the next falling edge of $\overline{CS}$, and the SO pin remains tristated.

Status Register

CY15B256Q has an 8-bit Status Register. The bits in the Status Register are used to configure the device. These bits are described in Table 3 on page 7.

Figure 2. System Configuration with SPI Port

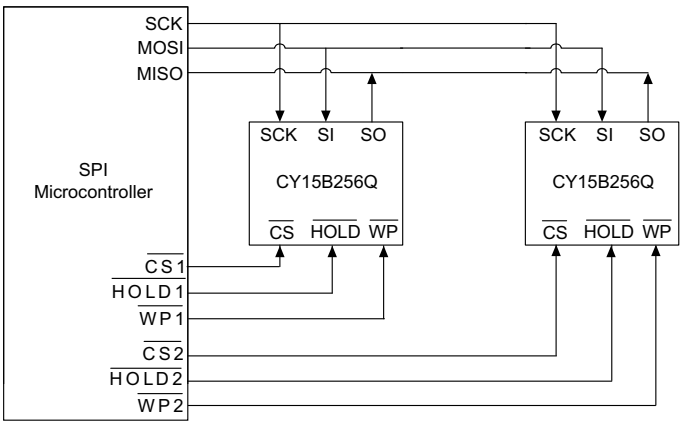
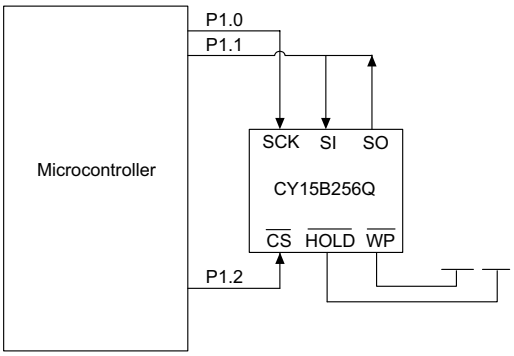


Figure 3. System Configuration without SPI Port



SPI Modes

CY15B256Q may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK.The two SPI modes are shown in Figure 4 on page 6 and Figure 5 on page 6. The status of the clock when the bus master is not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

The device detects the SPI mode from the status of the SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If the SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if the SCK pin is HIGH, it works in SPI Mode 3.

Figure 4. SPI Mode 0

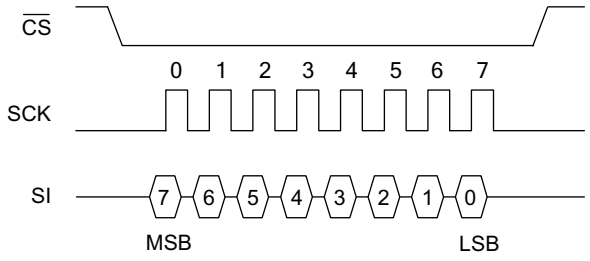
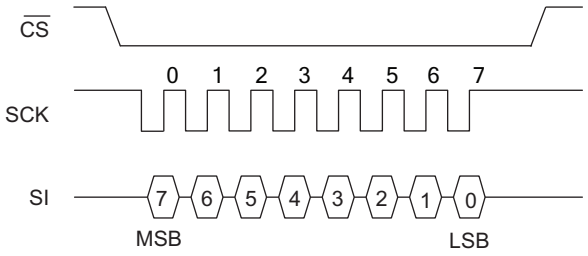


Figure 5. SPI Mode 3



Power Up to First Access

The CY15B256Q is not accessible for a t_{PU} time after power-up. Users must comply with the timing parameter t_{PU}, which is the minimum time from V_{DD}(min) to the first $\overline{CS}$ LOW.

Command Structure

There are nine commands, called opcodes, that can be issued by the bus master to the CY15B256Q. They are listed in Table 1. These opcodes control the functions performed by the memory.

Table 1. Opcode Commands

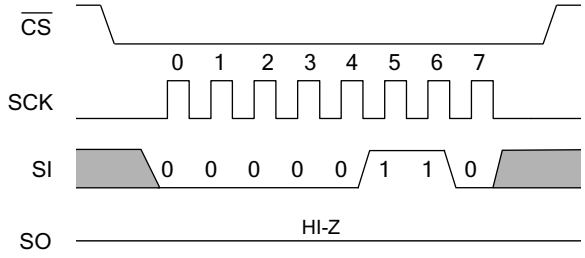
Name	Description	Opcode
WREN	Set write enable latch	0000 0110b
WRDI	Reset write enable latch	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read memory data	0000 0011b
FSTRD	Fast read memory data	0000 1011b
WRITE	Write memory data	0000 0010b
SLEEP	Enter sleep mode	1011 1001b
RDID	Read device ID	1001 1111b
Reserved	Reserved	1100 0011b
		1100 0010b
		0101 1010b
		0101 1011b

WREN - Set Write Enable Latch

The CY15B256Q will power up with writes disabled. The WREN command must be issued before any write operation. Sending the WREN opcode allows the user to issue subsequent opcodes for write operations. These include writing the Status Register (WRSR) and writing the memory (WRITE).

Sending the WREN opcode causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL = '1' indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit - only the WREN opcode can set this bit. The WEL bit will be automatically cleared on the rising edge of $\overline{CS}$ following a WRDI, a WRSR, or a WRITE operation. This prevents further writes to the Status Register or the F-RAM array without another WREN command. Figure 6 illustrates the WREN command bus configuration.

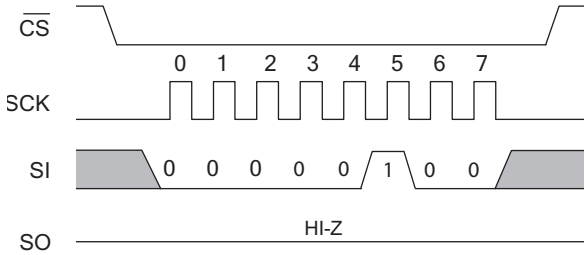
Figure 6. WREN Bus Configuration



WRDI - Reset Write Enable Latch

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the Status Register and verifying that WEL is equal to '0'. Figure 7 illustrates the WRDI command bus configuration.

Figure 7. WRDI Bus Configuration



Status Register and Write Protection

The write protection features of the CY15B256Q are multi-tiered and are enabled through the status register. The status register is organized as follows (the default value shipped from the factory for bits in the status register is ‘0’):

Table 2. Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	X (0)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEL (0)	X (0)

Table 3. Status Register Bit Definition

Bit	Definition	Description
Bit 0	Don’t care	This bit is non-writable and always returns ‘0’ upon read.
Bit 1 (WEL)	Write Enable	WEL indicates if the device is write enabled. This bit defaults to ‘0’ (disabled) on power-up. WEL = '1' --> Write enabled WEL = '0' --> Write disabled
Bit 2 (BP0)	Block Protect bit ‘0’	Used for block protection. For details, see Table 4 on page 7.
Bit 3 (BP1)	Block Protect bit ‘1’	Used for block protection. For details, see Table 4 on page 7.
Bit 4-6	Don’t care	These bits are non-writable and always return ‘0’ upon read.
Bit 7 (WPEN)	Write Protect Enable bit	Used to enable the function of Write Protect Pin ($\overline{WP}$). For details, see Table 5 on page 7.

Bits 0 and 4-6 are fixed at ‘0’; none of these bits can be modified. Note that bit 0 ("Ready or Write in progress” bit in serial flash and EEPROM) is unnecessary, as the F-RAM writes in real-time and is never busy, so it reads out as a ‘0’. An exception to this is when the device is waking up from sleep mode, which is described in Sleep Mode on page 10. The BP1 and BP0 control the software write-protection features and are nonvolatile bits. The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in Table 4.

Table 4. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	6000h to 7FFFh (upper 1/4)
1	0	4000h to 7FFFh (upper 1/2)
1	1	0000h to 7FFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The write protect enable bit (WPEN) in the Status Register controls the effect of the hardware write protect ($\overline{WP}$) pin. When the WPEN bit is set to '0', the status of the $\overline{WP}$ pin is ignored. When the WPEN bit is set to '1', a LOW on the $\overline{WP}$ pin inhibits a write to the Status Register. Thus the Status Register is write-protected only when WPEN = '1' and $\overline{WP}$ = '0'.

Table 5 summarizes the write protection conditions.

Table 5. Write Protection

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading the status register provides information about the current state of the write-protection features. Following the RDSR opcode, the CY15B256Q will return one byte with the contents of the Status Register.

WRSR - Write Status Register

The WRSR command allows the SPI bus master to write into the Status Register and change the write protect configuration by setting the WPEN, BP0, and BP1 bits as required. Before issuing a WRSR command, the $\overline{WP}$ pin must be HIGH or inactive. Note that on the CY15B256Q, $\overline{WP}$ only prevents writing to the Status Register, not the memory array. Before sending the WRSR command, the user must send a WREN command to enable writes. Executing a WRSR command is a write operation and therefore, clears the Write Enable Latch.

Figure 8. RDSR Bus Configuration

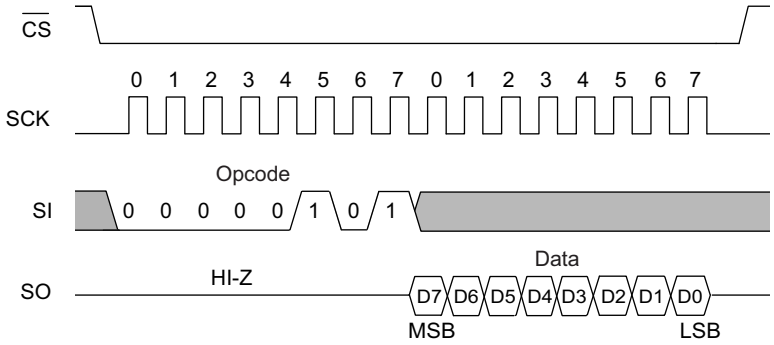
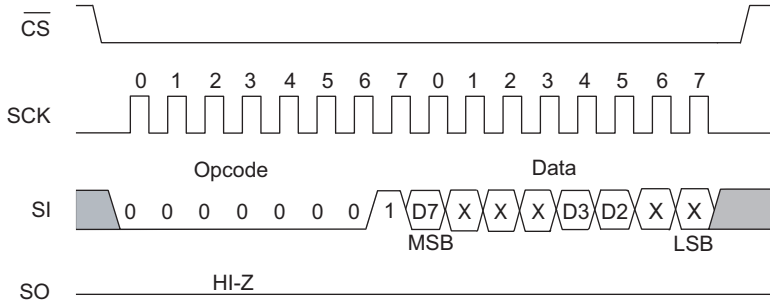


Figure 9. WRSR Bus Configuration (WREN not shown)



Memory Operation

The SPI interface, which is capable of a high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike serial flash and EEPROMs, the CY15B256Q can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory begin with a WREN opcode with $\overline{CS}$ being asserted and deasserted. The next opcode is WRITE. The WRITE opcode is followed by a two-byte address containing the 15-bit address (A14-A0) of the first data byte to be written into the memory. The upper bit of the two-byte address is ignored. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps $\overline{CS}$ LOW. If the last address of 7FFFh is reached, the counter will roll over to 0000h. Data is written to MSB first. The rising edge of $\overline{CS}$ terminates a write operation. A write operation is shown in Figure 10.

Note When a burst write reaches a protected block address, the automatic address increment stops and all the subsequent data bytes received for write will be ignored by the device.

EEPROMs use page buffers to increase their write throughput. This compensates for the technology's inherently slow write operations. F-RAM memories do not have page buffers because each byte is written to the F-RAM array immediately after it is clocked in (after the eighth clock). This allows any number of bytes to be written without page buffer delays.

Note If the power is lost in the middle of the write operation, only the last completed byte will be written.

Read Operation

After the falling edge of $\overline{CS}$, the bus master can issue a READ opcode. Following the READ command is a two-byte address containing the 15-bit address (A14-A0) of the first byte of the read operation. The upper bit of the address is ignored. After the opcode and address are issued, the device drives out the read data on the next eight clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and $\overline{CS}$ is LOW. If the last address of 7FFFh is reached, the counter will roll over to 0000h. Data is read MSB first. The rising edge of $\overline{CS}$ terminates a read operation and tristates the SO pin. A read operation is shown in Figure 11.

Fast Read Operation

The CY15B256Q supports a FAST READ opcode (0Bh) that is provided for code compatibility with serial flash devices. The FAST READ opcode is followed by a two-byte address containing the 15-bit address (A14-A0) of the first byte of the read operation and then a dummy byte. The dummy byte inserts a read latency of an 8-clock cycle. The fast read operation is otherwise the same as an ordinary read operation except that it

requires an additional dummy byte. After receiving opcode, address, and a dummy byte, the CY15B256Q starts driving its SO line with data bytes, with MSB first, and continues transmitting as long as the device is selected and the clock is available. In case of bulk read, the internal address counter is incremented automatically, and after the last address 7FFFh is reached, the counter rolls over to 0000h. When the device is driving data on its SO line, any transition on its SI line is ignored. The rising edge of $\overline{CS}$ terminates a fast read operation and tristates the SO pin. A Fast Read operation is shown in Figure 12.

Figure 10. Memory Write (WREN not shown) Operation

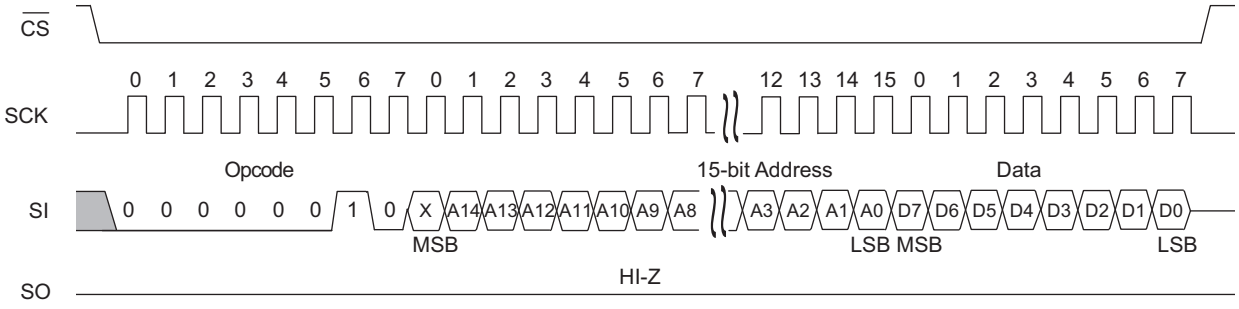


Figure 11. Memory Read Operation

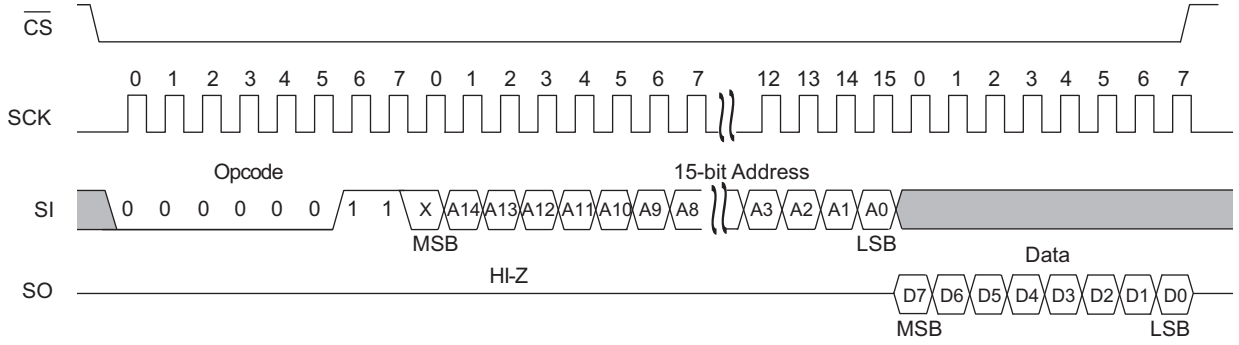
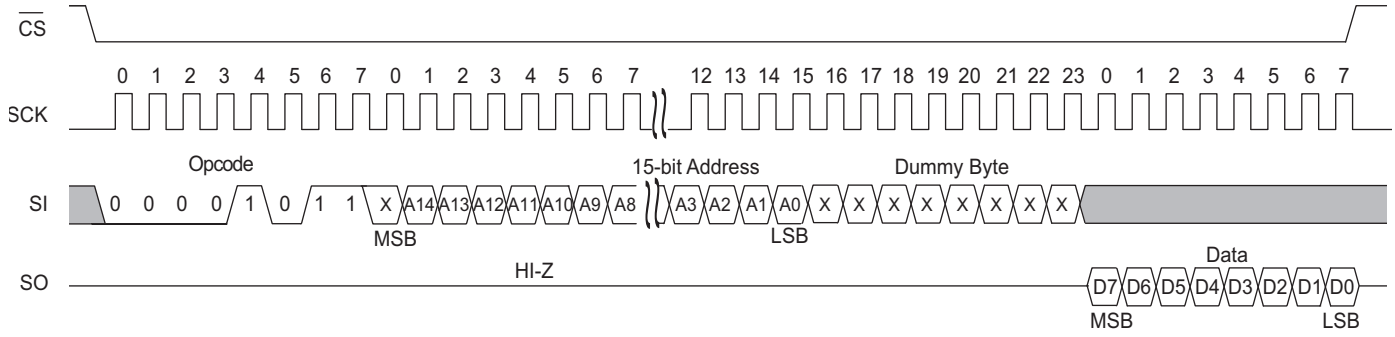


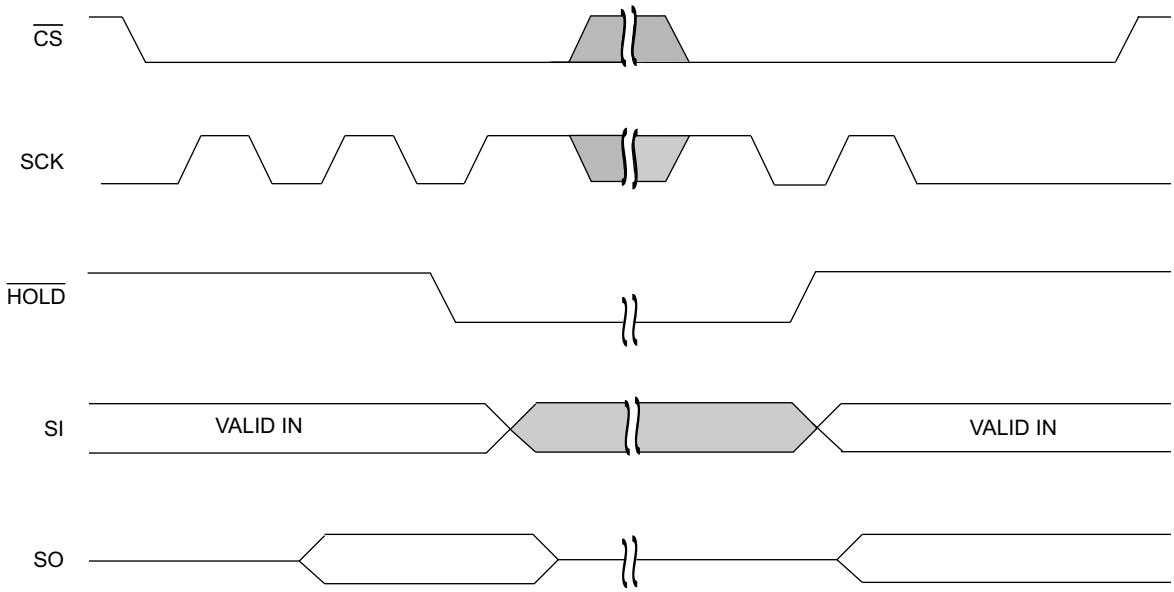
Figure 12. Fast Read Operation



HOLD Pin Operation

The HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master pulls the HOLD pin LOW while SCK is LOW, the current operation will pause. Taking the HOLD pin HIGH while SCK is LOW will resume an operation. The transitions of HOLD must occur while SCK is LOW, but the SCK and CS pin can toggle during a hold state.

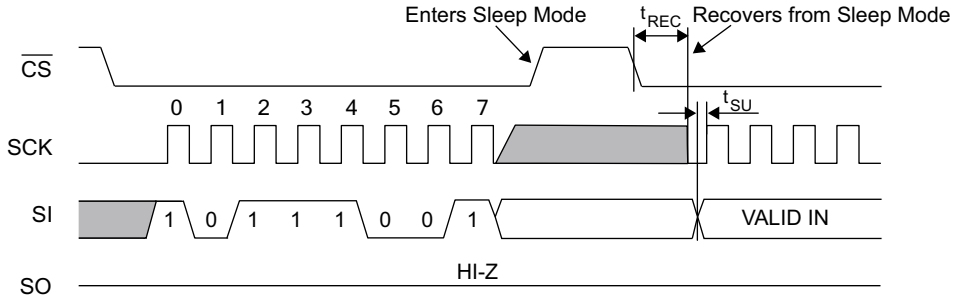
Figure 13. HOLD Operation [2]



Sleep Mode

A low-power sleep mode is implemented on the CY15B256Q device. The device will enter the low-power state when the SLEEP opcode B9h is clocked-in and a rising edge of CS is applied. When in sleep mode, the SCK and SI pins are ignored and SO will be HI-Z, but the device continues to monitor the CS pin. On the next falling edge of CS, the device will return to normal operation within t_{REC} time. The SO pin remains in a HI-Z state during the wakeup period. The device does not necessarily respond to an opcode within the wakeup period. To start the wakeup procedure, the controller may send a “dummy” read, for example, and wait the remaining t_{REC} time.

Figure 14. Sleep Mode Operation



Note
2. Figure 13 shows the HOLD operation for input mode and output mode.

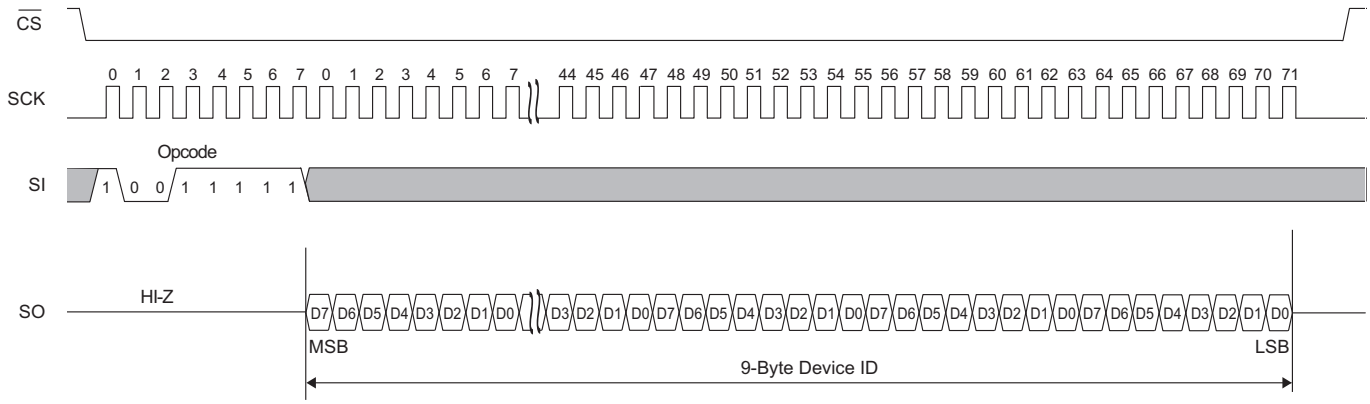
Device ID

The CY15B256Q device can be interrogated for its manufacturer, product identification, and die revision. The RDID opcode 9Fh allows the user to read the manufacturer ID and product ID, both of which are read-only bytes. The JEDEC-assigned manufacturer ID places the Cypress (Ramtron) identifier in bank 7; therefore, there are six bytes of the continuation code 7Fh followed by the single byte C2h. There are two bytes of product ID, which includes a family code, a density code, a sub code, and the product revision code.

Table 6. Device ID

Device ID (9 bytes)	Device ID Description					
	71–16 (56 bits)	15–13 (3 bits)	12–8 (5 bits)	7–6 (2 bits)	5–3 (3 bits)	2–0 (3 bits)
	Manufacturer ID	Product ID				
		Family	Density	Sub	Rev	Rsvd
7F7F7F7F7F7FC222C8h	01111111011111110111111110111 11110111111101111111111000010	001	00010	11	001	000

Figure 15. Read Device ID



Endurance

The CY15B256Q devices are capable of being accessed at least 10^{13} times, reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis for each access (read or write) to the memory array. The F-RAM architecture is based on an array of rows and columns of 4K rows of 64-bits each. The entire row is internally accessed once whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation. Table 7 shows endurance calculations for a 64-byte repeating loop, which includes an opcode, a starting address, and a sequential 64-byte data stream. This causes each byte to experience one endurance cycle through the loop.

Table 7. Time to Reach Endurance Limit for Repeating 64-byte Loop

SCK Freq (MHz)	Endurance Cycles/sec	Endurance Cycles/year	Years to Reach Limit
33	61,570	1.94×10^{12}	5.2
25	46,645	1.47×10^{12}	6.8
10	18,660	5.88×10^{11}	17.0
5	9,330	2.94×10^{11}	34.0

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +150 °C

Maximum accumulated storage time
At 150 °C ambient temperature ..... 1000 h
At 125 °C ambient temperature ..... 11000 h
At 85 °C ambient temperature ..... 121 Years

Ambient temperature
with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to + 4.5 V

Input voltage ..... –1.0 V to +4.5 V and $V_{IN} < V_{DD} + 1.0$ V

DC voltage applied to outputs
in HI-Z state ..... –0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on
any pin to ground potential ..... –2.0 V to V_{DD} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering
temperature (3 seconds) ..... + 260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Electrostatic discharge voltage
Human Body Model (JEDEC Std JESD22-A114-B) ..... 2 kV

Charged Device Model (JEDEC Std JESD22-C101-A) ..... 500 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Automotive-E	–40 °C to +125 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [3]	Max	Unit
V_{DD}	Power supply			2.7	3.3	3.6	V
I_{DD}	V_{DD} supply current	SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open.	f_{SCK} = 33 MHz	–	–	5	mA
			f_{SCK} = 1 MHz	–	–	0.5	mA
I_{SB}	V_{DD} standby current	$\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.		–	90	500	µA
I_{ZZ}	Sleep mode current	$\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.		–	5	12	µA
I_{LI}	Input leakage current (Except $\overline{HOLD}$)	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+1	µA
	Input leakage current (for $\overline{HOLD}$)			–100	–	+1	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$		–1	–	+1	µA
V_{IH}	Input HIGH voltage			0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage			– 0.3	–	0.3 × V_{DD}	V
V_{OH1}	Output HIGH voltage	I_{OH} = –1 mA, V_{DD} = 2.7 V.		2.4	–	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA		V_{DD} – 0.2	–	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} = 2.7 V		–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA		–	–	0.2	V
R_{in} [4]	Input resistance ($\overline{HOLD}$)	For V_{IN} = V_{IL}(max)		800	–	–	kΩ
		For V_{IN} = V_{IH}(min)		30	–	–	kΩ

Notes
3. Typical values are at 25 °C, V_{DD} = V_{DD}(typ). Not 100% tested.
4. The input pull-up circuit is strong (30 kΩ) when the input voltage is above V_{IH} and weak (800 kΩ) when the input voltage is below V_{IL}.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 125 °C	11000	–	Hours
		T_A = 105 °C	38	–	Years
		T_A = 85 °C	121	–	Years
NV_C	Endurance	Over operating temperature	10^{13}	–	Cycles

Example of an F-RAM Life Time in an AEC-Q100 Automotive Application

An application does not operate under a steady temperature for the entire usage life time of the application. Instead, it is often expected to operate in multiple temperature environments throughout the application's usage life time. Accordingly, the retention specification for F-RAM in applications often needs to be calculated cumulatively. An example calculation for a multi-temperature thermal profile is given in the following table.

Temperature T	Time Factor t	Acceleration Factor with respect to Tmax A [5]	Profile Factor P	Profile Life Time L (P)
		$A = \frac{L(T)}{L(Tmax)} = e^{\frac{Ea}{k}\left(\frac{1}{T}-\frac{1}{Tmax}\right)}$	$P = \frac{1}{\left(\frac{t1}{A1}+\frac{t2}{A2}+\frac{t3}{A3}+\frac{t4}{A4}\right)}$	$L(P) = P \times L(Tmax)$
T1 = 125 °C	t1 = 0.1	A1 = 1	8.33	> 10.46 Years
T2 = 105 °C	t2 = 0.15	A2 = 8.67		
T3 = 85 °C	t3 = 0.25	A3 = 95.68		
T4 = 55 °C	t4 = 0.50	A4 = 6074.80		

Capacitance

Parameter [6]	Description	Test Conditions	Max	Unit
C_O	Output pin capacitance (SO)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	8	pF
C_I	Input pin capacitance		6	pF

Thermal Resistance

Parameter	Description	Test Conditions	8-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	146	°C/W
Θ_{JC}	Thermal resistance (junction to case)		48	°C/W

AC Test Conditions

Input pulse levels .....10% and 90% of V_{DD}
Input rise and fall times .....3 ns
Input and output timing reference levels .....0.5 × V_{DD}
Output load capacitance ..... 30 pF

Note
5. Where k is the Boltzmann constant 8.617 × 10^{-5} eV/K, Tmax is the highest temperature specified for the product, and T is any temperature within the F-RAM product specification. All temperatures are in Kelvin in the equation.
6. This parameter is periodically sampled and not 100% tested.

AC Switching Characteristics

Over the Operating Range

Parameters [7]		Description	V_{DD} = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt. Parameter		Min	Max	
f_{SCK}	–	SCK clock frequency	0	33	MHz
t_{CH}	–	Clock HIGH time	11	–	ns
t_{CL}	–	Clock LOW time	11	–	ns
t_{CSU}	t_{CSS}	Chip select setup	10	–	ns
t_{CSH}	t_{CSH}	Chip select hold	10	–	ns
t_{OD} [8, 9]	t_{HZCS}	Output disable time	–	12	ns
t_{ODV}	t_{CO}	Output data valid time	–	9	ns
t_{OH}	–	Output hold time	0	–	ns
t_D	–	Deselect time	40	–	ns
t_R [10, 11]	–	Data in rise time	–	50	ns
t_F [10, 11]	–	Data in fall time	–	50	ns
t_{SU}	t_{SD}	Data setup time	5	–	ns
t_H	t_{HD}	Data hold time	5	–	ns
t_{HS}	t_{SH}	$\overline{\text{HOLD}}$ setup time	10	–	ns
t_{HH}	t_{HH}	$\overline{\text{HOLD}}$ hold time	10	–	ns
t_{HZ} [8, 9]	t_{HHZ}	$\overline{\text{HOLD}}$ LOW to output HI-Z	–	20	ns
t_{LZ} [9]	t_{HLZ}	$\overline{\text{HOLD}}$ HIGH to data active	–	20	ns

Notes

7. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance shown in AC Test Conditions.
8. t_{OD} and t_{HZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
9. Characterized but not 100% tested in production.
10. Rise and fall times measured between 10% and 90% of waveform.
11. These parameters are guaranteed by design and are not tested.

Figure 16. Synchronous Data Timing (Mode 0)

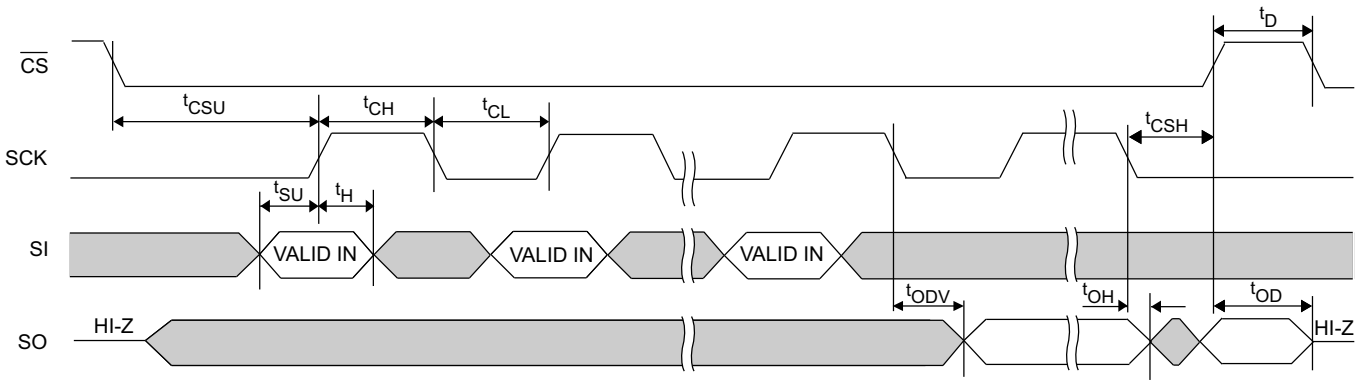
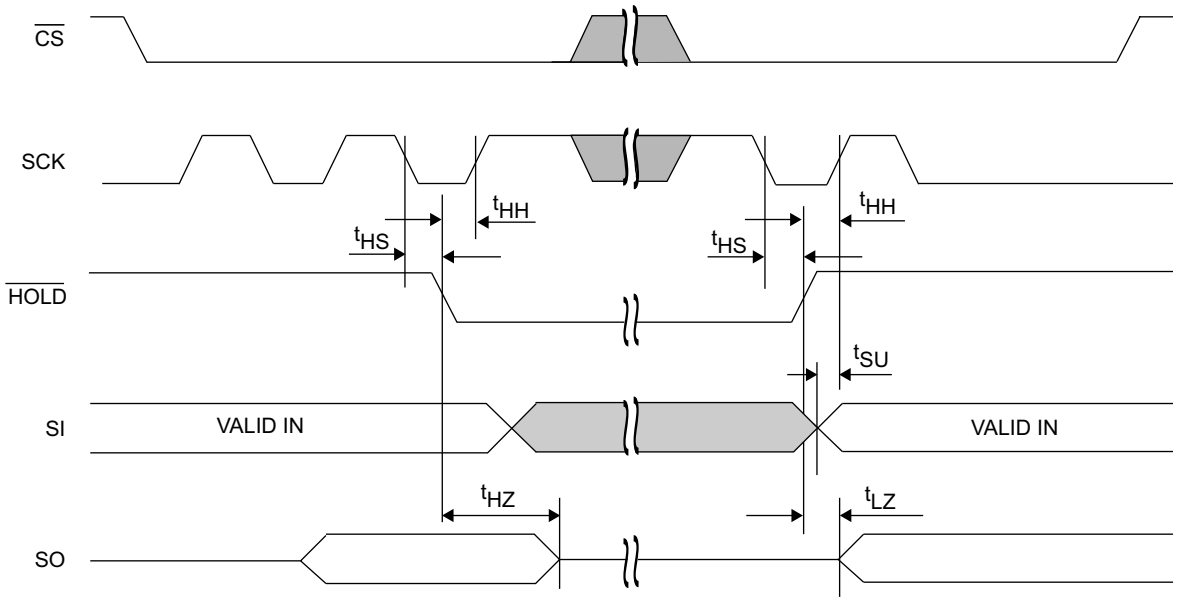


Figure 17. $\overline{\text{HOLD}}$ Timing

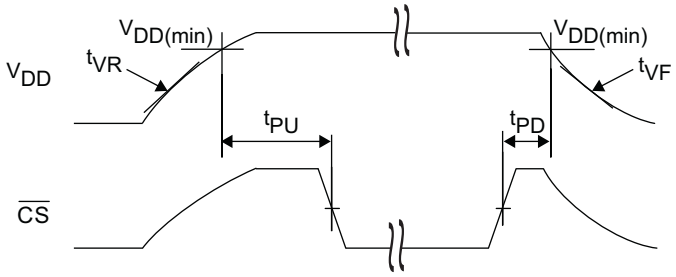


Power Cycle Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up V_{DD} (min) to first access ($\overline{CS}$ LOW)	250	–	µs
t_{PD}	Last access ($\overline{CS}$ HIGH) to power-down (V_{DD}(min))	0	–	µs
t_{VR} [12, 13]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF} [12, 13]	V_{DD} power-down ramp rate	100	–	µs/V
t_{REC} [14]	Recovery time from sleep mode	–	400	µs

Figure 18. Power Cycle Timing



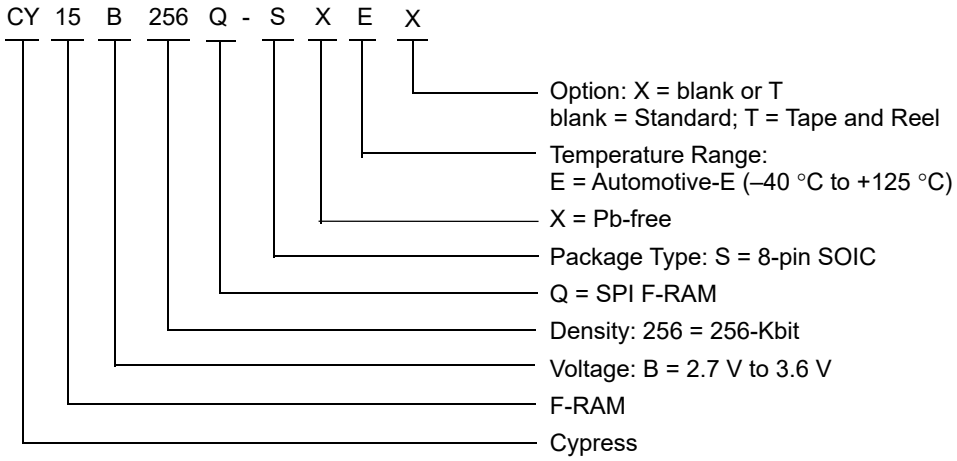
Notes
12. Slope measured at any point on V_{DD} waveform.
13. These parameters are guaranteed by design and are not tested.
14. Refer to Figure 14 for sleep mode recovery timing.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY15B256Q-SXE	51-85066	8-pin SOIC	–40 °C to +125 °C

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

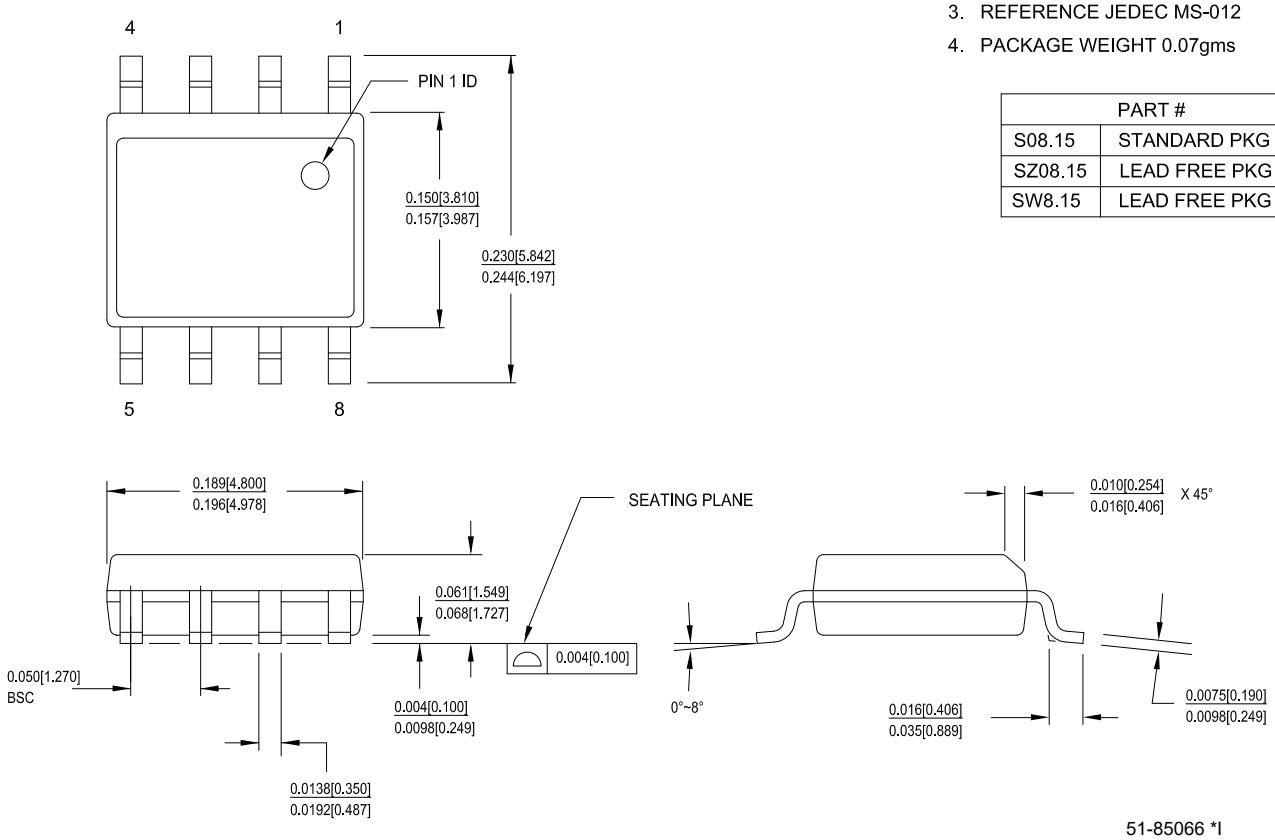


Package Diagram

Figure 19. 8-pin SOIC (150 Mils) Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *I

Acronyms

Acronym	Description
CPHA	Clock Phase
CPOL	Clock Polarity
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
LSB	Least Significant Bit
MSB	Most Significant Bit
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Kbit	Kilobit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY15B256Q, 256-Kbit (32K × 8) Automotive-E Serial (SPI) F-RAM Document Number: 001-97632			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	4765469	05/19/2015	New data sheet.
*A	4884691	08/14/2015	Updated Maximum Ratings: Updated ratings of “Storage temperature” (Replaced “+125 °C” with “+150 °C”). Removed “Maximum junction temperature”. Added “Maximum accumulated storage time”. Added “Ambient temperature with power applied”.
*B	5451057	09/27/2016	Updated Power Cycle Timing: Changed minimum value of t_{PU} parameter from 1 ms to 250 µs. Updated Package Diagram: spec 51-85066 – Changed revision from *G to *H. Updated to new template.
*C	6868371	04/26/2020	Updated to template. Updated Spec 51-85066 *H to *I in Package Diagram.

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