Control integrated power system (CIPOS™)

CIPOS™ Mini PFC-integrated IPM technical description

About this document

Scope and Purpose

The scope of this application note is to describe the product of CIPOS™ Mini power factor correction (PFC) integrated intelligent power module (IPM) and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as IGBT or gate drive IC, as well as to the design of the necessary external circuitry, such as bootstrap or interfacing.

Intended Audience

Power electronics engineers who want to design reliable and efficient CIPOS™ Mini PFC-integrated IPM applications.

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1 Scope

The scope of this application note is to describe the CIPOS™ Mini PFC-integrated IPM and the basic requirements for operating the product in recommended conditions. This is related to the integrated components, such as IGBT or gate drive IC, as well as to the design of the necessary external circuitry, such as bootstrap or interfacing. Integrating discrete power semiconductors and drivers into one package allows the reduction of time and effort spent on design. To meet the strong demand for small size and higher power density, Infineon Technologies has developed a new family of highly integrated intelligent power modules that contain nearly all of the semiconductor components required to drive electronically controlled variable-speed electric motors. They incorporate a three-phase inverter and PFC power stage with a silicon-on-insulator (SOI) gate driver and Infineon's leading-edge TRENCHSTOP™ IGBTs and anti-parallel diodes for inverter part and 650V TRENCHSTOP™ / TRENCHSTOP™ 5 IGBT and rapid switching emitter-controlled diode for single boost PFC part.

The application note concerns the following products.

IFCM10P60GD

IFCM10S60GD

IFCM15P60GD

IFCM15S60GD

Note: IvCMxxy60zu
*v = **F**(PFC)*
*xx = **nominal current***
*y = **PFC switching speed**(P(40 kHz), S(20 kHz))*
*z = **G**(Temp., Itrip, Fault)*
*u = **D**(DCB)*

CIPOS™ Mini PFC-integrated IPM is a family of intelligent power modules with single phase boost PFC which are designed for low power motor drives in household appliances, such as air conditioners(1 ~ 1.5 kW).

1.1 Product line-up

Table 1 Line-up of CIPOS™ Mini PFC-integrated IPM product

Part number	Rating		Inverter circuit	PFC topology	Package	Isolation voltage [V_{rms}]	Main applications
	Current [A]	Voltage [V]					
IFCM10P60zD	10	600	Closed emitter	Single phase boost	DCB DIL module	2000 V_{rms} sinusoidal, 1min.	Air conditioner
IFCM10S60zD							
IFCM15P60zD	15						
IFCM15S60zD							

1.2 Nomenclature

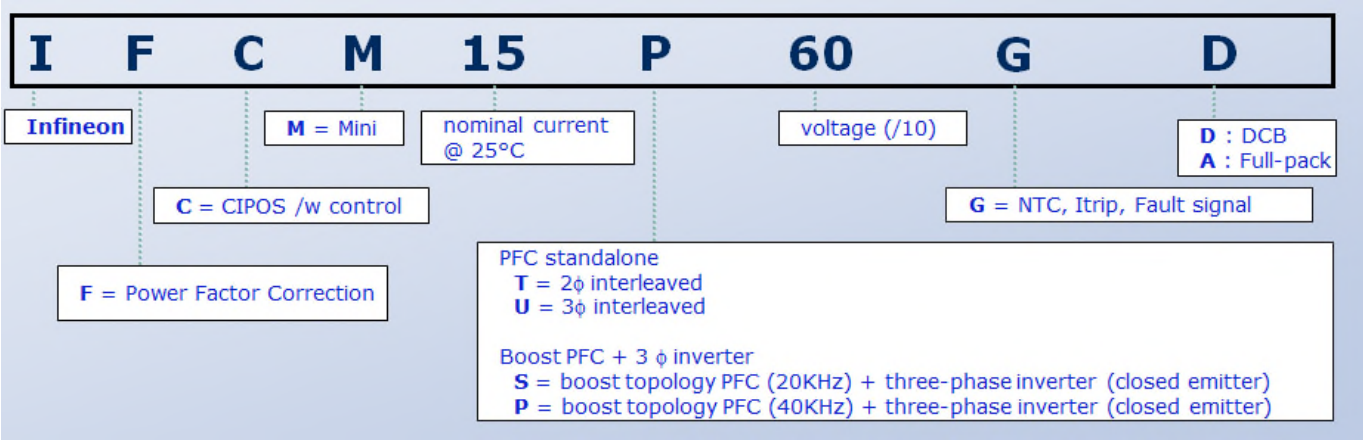


Figure 1 CIPOS™ Mini PFC-integrated IPM products nomenclature

2 Internal components and package technology

2.1 Power transistor technology for inverter – TRENCHSTOP™ IGBT

Infineon Technologies introduced their TRENCHSTOP™ IGBT technology in 2004. This technology continues the well-known properties of robustness of Infineon IGBT, such as short circuit withstand capability and maximum junction temperature. On the other hand all advantages of these technologies remain in order to achieve highest efficiency and enable for highest power density. This refers to very low static parameters such as saturation voltage of IGBT as well as to the excellent dynamic parameter such as turn-off energy of the IGBT [1].

2.2 Power diode technology for inverter – emitter-controlled diode

Emitter-controlled diode is Infineon's unique fast recovery diode technology. The ultrathin wafer and Fieldstop technology makes the emitter-controlled diode ideally suited for consumer and industry applications as it lowers the turn-on losses of the IGBT with soft recovery. The emitter-controlled diode is optimized for Infineon IGBT technology.

2.3 Power transistor technology for PFC – 650V TRENCHSTOP™ IGBT

The trench-field-stop technology is the most common concept for modern IGBTs with blocking voltages in the range of 600 V to 1200 V. Within this technology, the device performance is mainly controlled by design parameters like cell geometry, chip thickness, and doping profile. These parameters determine the carrier distribution in the device and, hence, influence the static and dynamic characteristics of the IGBT significantly. Infineon Technologies has developed two kinds of products according to their PFC IGBT characteristics. High Speed 3 (H3) for 20 kHz switching frequency is included in IFCMxxS60GD and TRENCHSTOP™ 5 (H5) for 40 kHz switching frequency is included in IFCMxxP60GD.

2.3.1 High Speed 3 (H3) IGBT

The performance of an IGBT is determined by a trade-off curve which describes the correlation between the turn-off energy (Eoff) and the collector-emitter saturation voltage ($V_{CE(sat)}$). Therefore, the performance of an IGBT can be either optimized for high-frequency applications which need devices with low dynamic losses, or for low-frequency applications which benefit from low static losses. The High Speed 3 IGBT is optimized for high-frequency applications compared with IGBT 3 due to its low Eoff = 0.6 mJ. The IGBT3 provides a more than two times larger Eoff = 1.4 mJ, whereas the $V_{CE(sat)}$ is low as 1.45 V [2].

2.3.2 TRENCHSTOP™ 5 (H5) IGBT

The TRENCHSTOP™ 5 device is a forceful advancement of Infineon’s field stop technology to gain lowest switch off losses due to drift zone reduction to < 50 µm. This results in a considerable reduction of charge carriers during device-on operation which need to be removed from the device at switch off. Furthermore, the device is characterized by a significantly increased channel width compared to Infineon’s TRENCHSTOP™ series in order to reduce simultaneously $V_{CE(sat)}$ and switch off losses [3].

2.4 Power diode technology for PFC – rapid emitter-controlled diode

The rapid emitter-controlled diode of Infineon is optimized to operate with 650 V TRENCHSTOP™ IGBT as a boost diode in PFC topology when the switching frequency is less than 40 kHz because conduction losses dominate switching losses at lower switching frequency operation. The rapid diode advancement in thin wafer technology helps to maintain a stable V_F over temperature. The rapid diode combines low V_F for lower conduction losses and low I_{rr} to reduce Eon of the TRENCHSTOP™ IGBT. Increased efficiency, with the additional benefit of having a 650 V breakthrough voltage can be achieved [4].

2.5 Control IC – 6 channel gate driver IC

The basic feature of this technology is the separation of the active silicon from the base material by means of a buried silicon oxide layer. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices. This also prevents the latch-up effect even in case of high dv/dt switching under elevated temperature and hence provides improved robustness. Besides the thin-film SOI technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays [5]. A monolithic single control IC for all 6 IGBTs provides further advantages, such as bootstrap circuitry, matched propagation delay times, built-in deadtime, cross conduction prevention and all 6 IGBTs turn-off under fault situations like undervoltage lockout (UVLO) or overcurrent.

2.6 Thermistor

In CIPOS™ Mini family, the thermistor is integrated optionally on the internal PCB. It is connected between V_{FO} and V_{SS} pins. A circuit proposal using the thermistor for over temperature protection is discussed in Section 5.4.

Table 2 Raw data of the thermistor used in CIPOS™ Mini

T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]	T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]
-40	2662.292	2962.540	3262.789	10.1	45	34.520	36.508	38.496	5.4
-35	1925.308	2133.692	2342.076	9.8	50	28.400	29.972	31.545	5.2
-30	1407.191	1553.414	1699.637	9.4	55	23.485	24.735	25.985	5.1
-25	1038.949	1142.63	1246.312	9.1	60	19.517	20.515	21.514	4.9
-20	774.497	848.747	922.997	8.7	65	16.296	17.097	17.898	4.7
-15	582.690	636.369	690.048	8.4	70	13.670	14.315	14.960	4.5
-10	442.252	481.410	520.568	8.1	75	11.517	12.039	12.561	4.3
-5	338.491	367.303	396.114	7.8	80	9.745	10.169	10.593	4.2
0	261.164	282.537	303.910	7.6	85	8.279	8.625	8.971	4.0
5	203.056	219.036	235.016	7.3	90	7.062	7.345	7.628	3.9
10	159.044	171.081	183.118	7.0	95	6.046	6.279	6.511	3.7
15	125.454	134.586	143.717	6.8	100	5.199	5.388	5.576	3.5
20	99.630	106.605	113.580	6.5	105	4.468	4.640	4.811	3.7
25	79.638	85.000	90.362	6.3	110	3.856	4.009	4.163	3.8
30	64.055	68.203	72.352	6.1	115	3.338	3.477	3.615	4.0
35	51.831	55.059	58.287	5.9	120	2.900	3.024	3.149	4.1
40	42.182	44.708	47.235	5.7	125	2.527	2.639	2.751	4.2

2.7 Package technology

The CIPOS™ Mini DCB package offers the smallest size while providing high power density up to 600 V, 15 A by employing TRENCHSTOP™ IGBT and anti-parallel diode for inverter with 6 channel gate drive IC and TRENCHSTOP™ 5 IGBT and rapid switching emitter-controlled diode for PFC. It contains all the power components such as the IGBTs and isolates them from each other and from the heatsink. All low power components such as the gate drive IC and thermistor are assembled on a PCB.

The electric insulation is given by ceramic layer of the DCB itself, which is simultaneously the thermal contact to the heat sink. In order to further decrease the thermal impedance, the internal lead frame design is optimized [6]. Figure 2 shows the external view of CIPOS™ Mini DCB package.

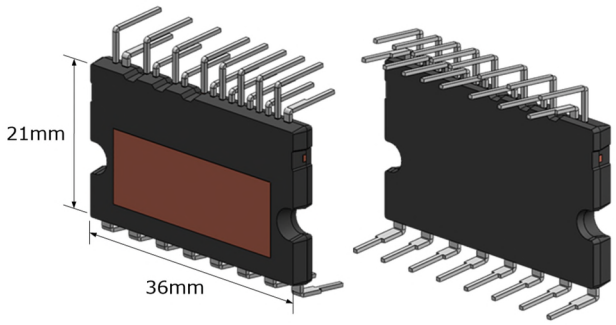


Figure 2 External view of CIPOS™ Mini DCB package

3 Product overview

3.1 Internal circuit and features

Figure 3 illustrates the internal block diagram of the CIPOS™ Mini PFC-integrated IPM. It consists of a three-phase IGBT inverter circuit, single phase boost PFC circuit, and a driver IC with control functions. The detailed features and integrated functions of this IPM are described as follows.

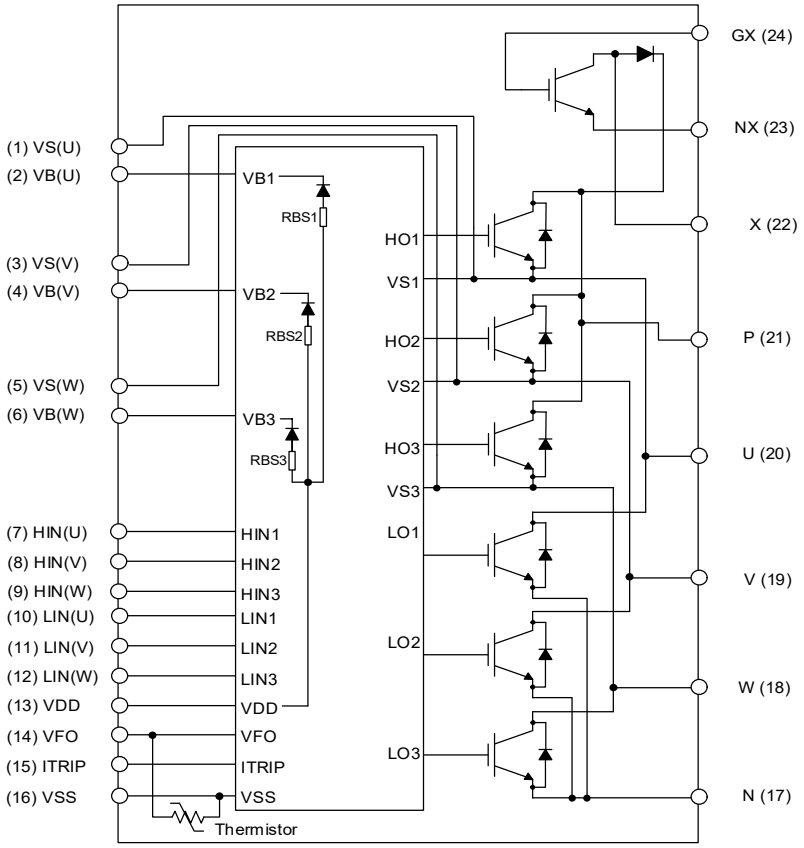


Figure 3 Internal circuit

Features

- Package
  - 600 V 10 A / 15 A rating in one physical package size (mechanical layouts are identical)
  - Fully isolated dual in-line (DIL) molded module
  - Lead-free terminal plating; RoHS compliant
  - Very low thermal resistance due to DCB

- Inverter
  - TRENCHSTOP™ IGBTs with separate body diode
  - Rugged SOI gate driver technology with stability against transient and negative voltage
  - Integrated bootstrap functionality
  - Matched delay times of all channels / Built in deadtime

- PFC
  - TRENCHSTOP™ IGBT / 650 V TRENCHSTOP™ 5 IGBT
  - 650 V rapid switching emitter-controlled diode

- Functions
  - Overcurrent shutdown
  - Temperature monitor
  - Undervoltage lockout at all channels
  - Low-side closed emitter
  - Anti cross-conduction
  - All 6 switches turn off during protection
  - Active-high input signal logic

3.2 Maximum electrical ratings

Table 3 Detail description of absolute maximum ratings (Inverter Section of IFCM10P60GD)

Item	Symbol	Rating	Description
Max. blocking voltage	V_{CES}	600 V	The sustained collector-emitter voltage of internal IGBTs
Output current	I_C	±10 A	The allowable continuous IGBT collector current at T_C = 25°C.
Junction temperature	T_J	-40 ~ 150°C	Considering temperature ripple on the power chips, the maximum junction temperature rating of CIPOS™ Mini is 150°C.
Operating case temperature range	T_C	-40 ~ 100°C	T_C (case temperature) is defined as a temperature of the package surface underneath the specified power chip. Please mount a temperature sensor on a heat-sink surface at the defined position in Figure 4 so as to get accurate temperature information.

Table 4 Detail description of absolute maximum ratings (PFC Section of IFCM10P60GD)

Item	Symbol	Rating	Description
Max. blocking voltage	V_{CES}	650 V	The sustained collector-emitter voltage of IGBTs
Gate-emitter peak voltage	V_{GES}	±20 V	The allowable peak IGBT gate-emitter voltage at T_J = 25°C.
Input RMS current	I_i	30 A	The allowable Input RMS current at T_J = 25°C.
Junction temperature	T_J	-40 ~ 150°C	Considering temperature ripple on the power chips, the maximum junction temperature rating of CIPOS™ Mini is 150°C.

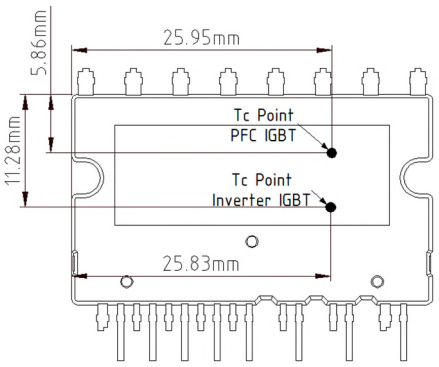


Figure 4 T_C measurement point

3.3 Description of the input and output pins

Table 5 defines the CIPOS™ Mini PFC-integrated IPM input and output pins. The detailed functional descriptions are as follows:

Table 5 Pin descriptions of CIPOS™ Mini PFC-integrated IPM

Pin Number	Pin Name	Pin Description
1	VS(U)	U-phase high-side floating IC supply offset voltage
2	VB(U)	U-phase high-side floating IC supply voltage
3	VS(V)	V-phase high-side floating IC supply offset voltage
4	VB(V)	V-phase high-side floating IC supply voltage
5	VS(W)	W-phase high-side floating IC supply offset voltage
6	VB(W)	W-phase high-side floating IC supply voltage
7	HIN(U)	U-phase high-side gate driver input
8	HIN(V)	V-phase high-side gate driver input
9	HIN(W)	W-phase high-side gate driver input
10	LIN(U)	U-phase low-side gate driver input
11	LIN(V)	V-phase low-side gate driver input
12	LIN(W)	W-phase low-side gate driver input
13	V_{DD}	Low-side control supply
14	V_{FO}	Fault output / Temperature monitor
15	ITRIP	Overcurrent shutdown input
16	V_{SS}	Low-side control negative supply
17	N	Inverter low-side emitter
18	W	Motor W-phase output
19	V	Motor V-phase output
20	U	Motor U-phase output
21	P	Positive PFC output voltage / Positive inverter bus input voltage
22	X	PFC IGBT collector
23	NX	PFC IGBT emitter
24	GX	PFC IGBT gate

High-side bias voltage pins for driving the IGBT

Pins: VB(U) – VS(U) , VB(V) – VS(V), VB(W) – VS(W)

- These pins provide the gate drive power to the high-side IGBTs.
- The ability to utilize a boot-strap circuit scheme for the high-side IGBTs eliminates the need of external power supplies.
- Each boot-strap capacitor is charged from the V_{DD} supply during the ON-state of the corresponding low-side IGBT or the freewheeling state of the low-side freewheeling diode.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low-side bias voltage pin

Pin: V_{DD}

- This is the control supply pin for the internal IC.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to this pin.

Low-side common supply ground pin

Pin: V_{SS}

- This pin connects the control ground for the internal IC.

Signal input pins

Pins: HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)

- These are pins to control the operation of the internal IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active-high. The IGBT associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the CIPOS™ Mini against noise influences
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 6.

Overcurrent detection pin

Pin: ITRIP

- The current sensing shunt resistor should be connected between the pin N (emitter of low-side IGBT) and the power ground to detect short-circuit current (refer to Figure 8). A RC filter should be connected between the shunt resistor and the pin ITRIP to eliminate noise.
- The integrated comparator is triggered, if the voltage V_{ITRIP} is higher than 0.47 V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at pin V_{FO} is pulled down to LOW.
- The connection length between the shunt resistor and ITRIP pin should be minimized.

Fault output and temperature monitoring pin

Pin: V_{FO}

- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the CIPOS™ Mini. The alarm conditions are overcurrent detection and low-side bias under voltage operation.
- The V_{FO} output is open-drain configured. The V_{FO} signal line should be pulled up to the logic power supply (5 V / 3.3 V) with proper resistance considering temperature monitoring with the parallel connected thermistor between V_{FO} and V_{SS} pins optional.

Positive DC-link pin

Pin: P

- This is the DC-link positive power supply pin of the CIPOS™ Mini PFC-integrated IPM.
- It is internally connected to the collectors of the high-side IGBTs.
- In order to suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically metal film capacitors are used.)

Negative DC-link pin

Pin: N

- This is the DC-link negative power supply pin (power ground) of the inverter.
- These pin is connected to the low-side IGBT emitters of the each phase.

Inverter power output pins

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e. g. motor).

Single boost PFC pins

Pins: X, NX, GX

- These pins are emitter, collector and gate of IGBT for single phase boost PFC.

3.4 Outline drawings

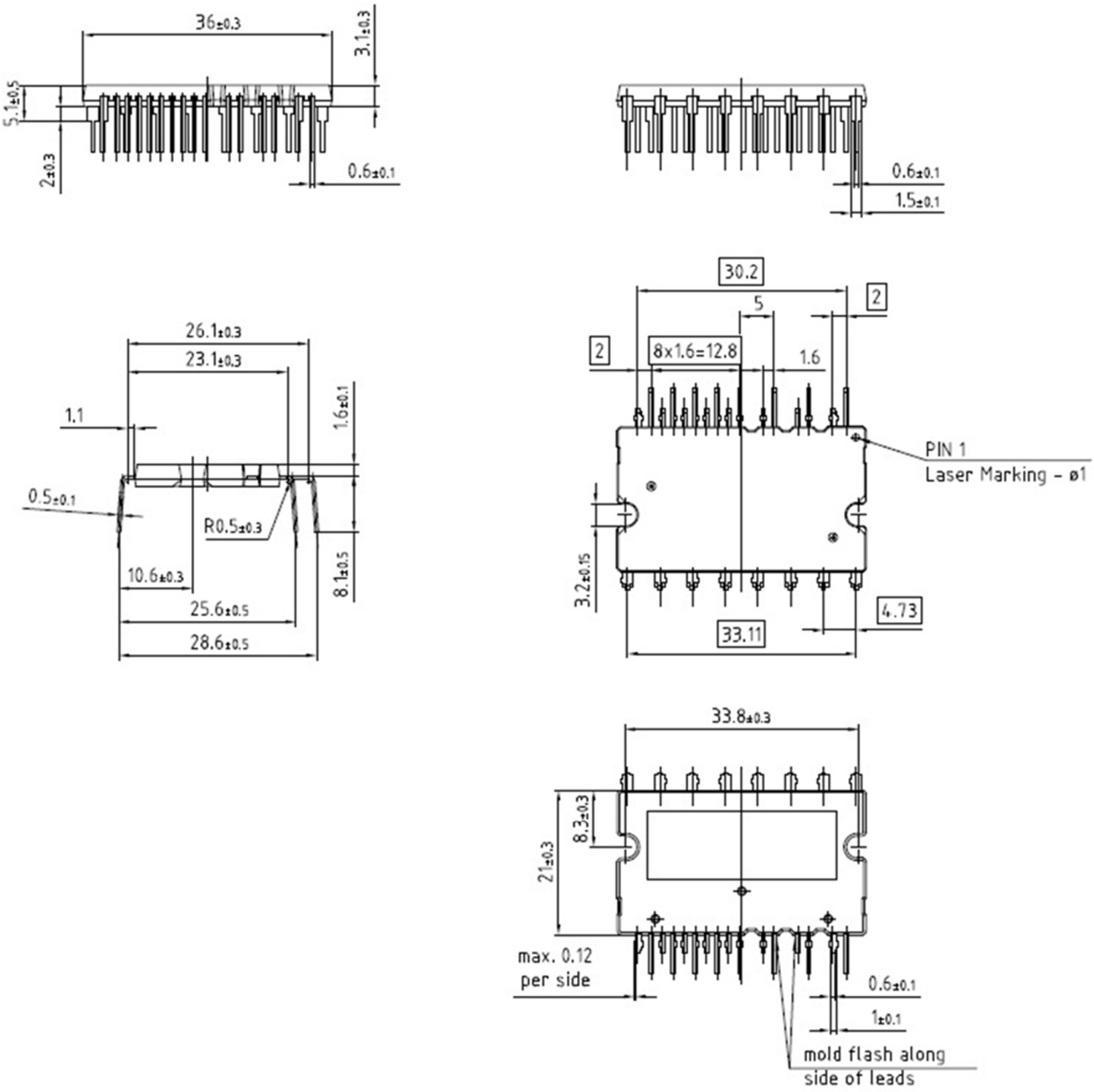


Figure 5 Package outline dimensions (Unit: [mm])

4 Interface circuit and layout guide

4.1 Input/output signal connection

Figure 6 shows the I/O interface circuit between microcontroller and the CIPOS™ Mini. The CIPOS™ Mini input logic is active-high with internal pull-down resistors. External pull-down resistors are not needed. V_{FO} output is open-drain configured. This signal should be pulled up to the positive side of 5 V or 3.3 V external logic power supply with a pull-up resistor. The pull-up resistor value should be properly selected, e.g. 3.6 kΩ with a parallel connected thermistor between V_{FO} and V_{SS} pins.

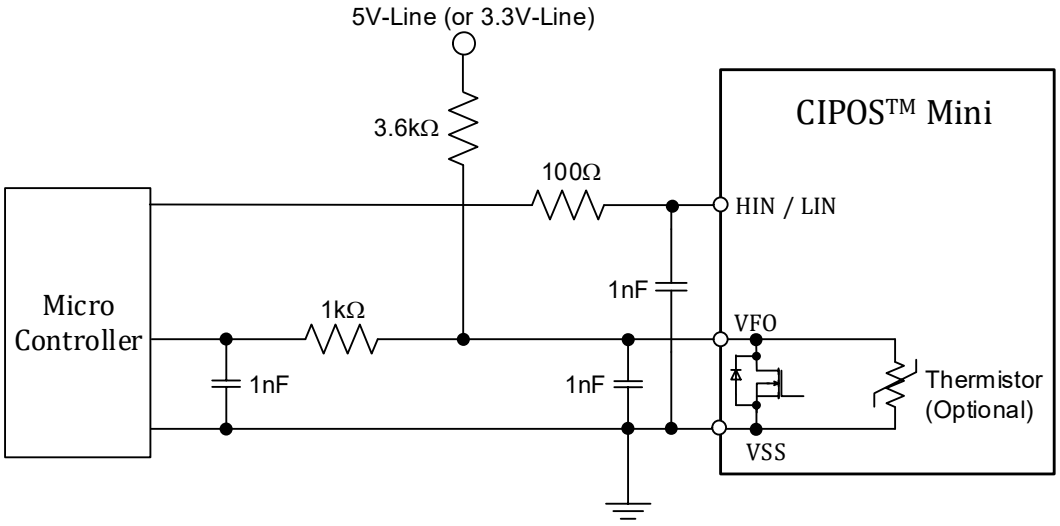


Figure 6 Recommended microcontroller I/O interface circuit

Table 6 Maximum ratings of input and V_{FO} pins

Item	Symbol	Condition	Rating	Unit
Module supply voltage	V_{DD}	Applied between V_{DD} – V_{SS}	20	V
Input voltage	VIN	Applied between HIN(U), HIN(V), HIN(W) – V_{SS} LIN(U), LIN(V), LIN(W) – V_{SS}	-1 ~ 10	V
Fault output supply voltage	V_{FO}	Applied between V_{FO} – V_{SS}	-0.5 ~ V_{DD}+0.5	V

The input and fault output maximum rating voltages are listed in Table 6. Since the fault output is open-drain configured and its rating is V_{DD}+0.5 V, a 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supply, which is the same as the input signals. It is also recommended placing bypass capacitors as close as possible to the V_{FO} and signal lines from the microcontroller as well as the CIPOS™ Mini.

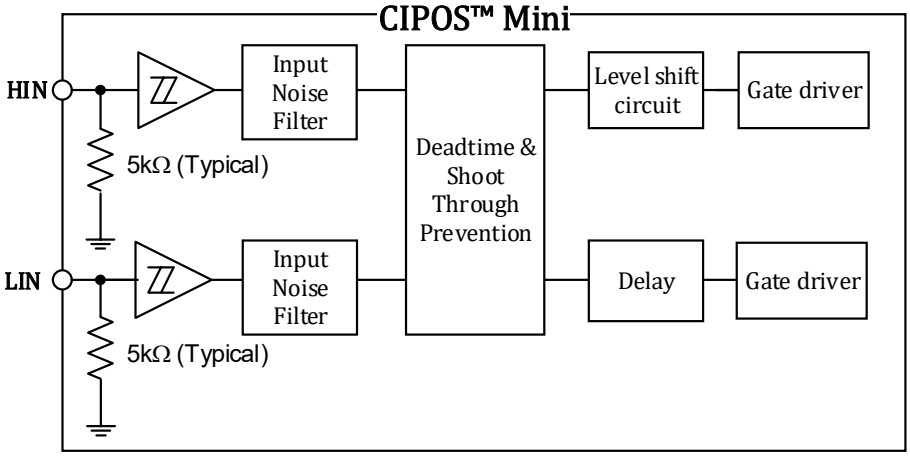


Figure 7 Simplified block diagram of CIPOS™ Mini control IC

Because CIPOS™ Mini family employs active-high input logic, the power sequence restriction between the control supply and the input signal during start-up or shut down operation does not exist. Therefore it makes the system fail-safe. In addition, pull-down resistors are built in to each input circuit. Thus, external pull-down resistors are not needed. This reduces the required external component count. Input Schmitt-trigger, noise filter, deadtime and shoot through prevention functions provide beneficial noise rejection to short input pulses. Furthermore, by lowering the turn on and turn off threshold voltage of input signal as shown in Table 7, a direct connection to 3.3 V-class microcontroller or DSP is possible.

Table 7 Input threshold voltage (at V_{DD} = 15 V, T_J = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (LIN, HIN)	V_{IH_TH}	HIN – V_{SS} LIN – V_{SS}	-	2.1	2.5	V
Logic "0" input voltage (LIN, HIN)	V_{IL_TH}		0.7	0.9	-	V

As shown in Figure 7, the CIPOS™ Mini input signal section integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between microcontroller output and CIPOS™ Mini input, pay attention to the signal voltage drop at the CIPOS™ Mini input terminals. It should fulfill the logic "1" input voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown in Figure 6.

4.2 General interface circuit example

Figure 8 shows typical application circuit of CIPOS™ Mini PFC-integrated IPM for interface schematic with control signals connected directly to a microcontroller.

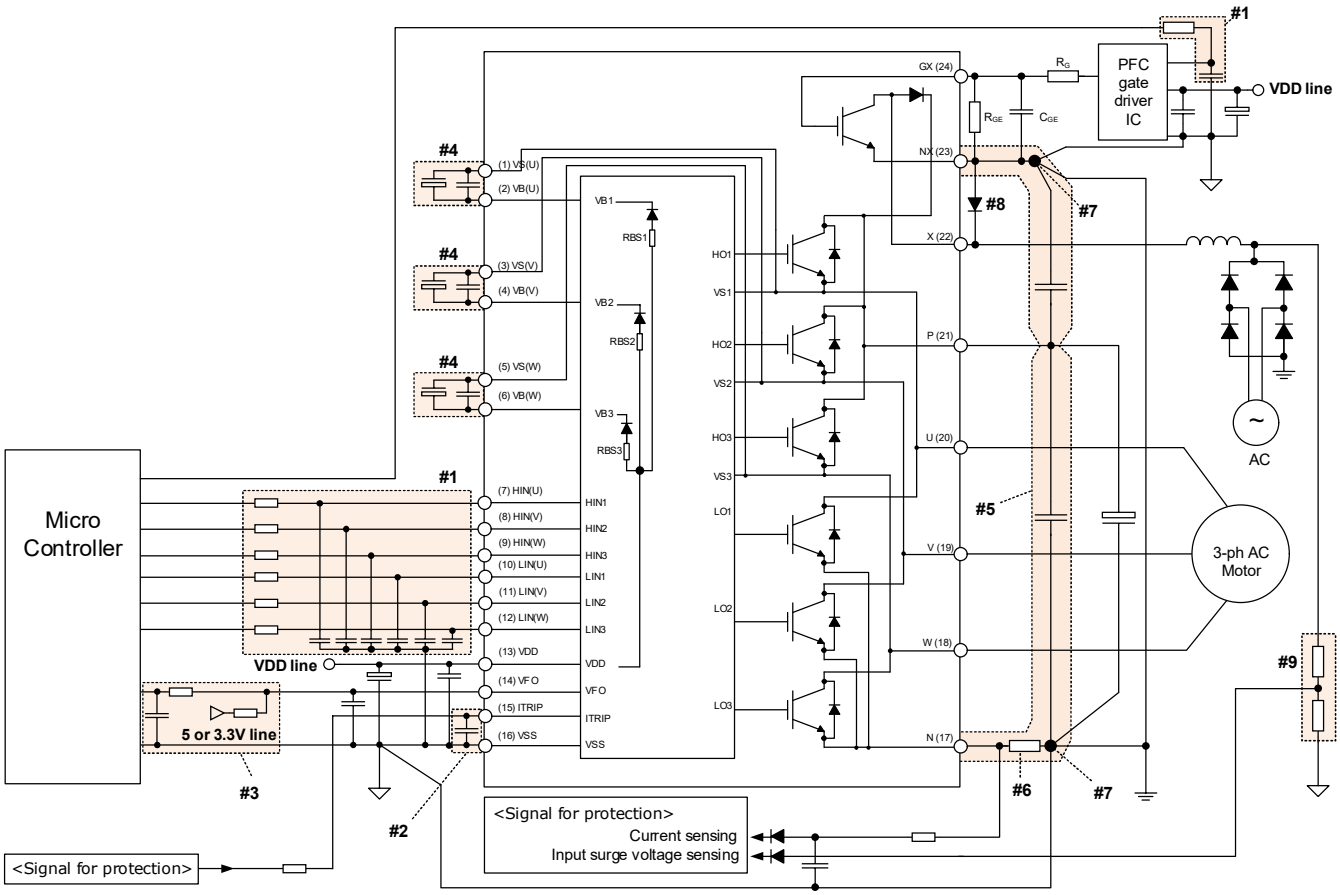


Figure 8 Application circuit example

Because the PFC IGBT inside this product has very high speed switching characteristics, considerable large surge voltage between P and NX terminals and switching noise on signaling path are generated easily. Please pay attention to the below items for optimized application circuit design

Note:

1. *Input Circuit*
   - *To reduce input signal noise by high speed switching, the RIN and CIN filter circuit should be mounted.(100 Ω, 1 nF)*
   - *CIN should be placed as close to V_{SS} pin as possible.*
2. *ITRIP circuit*
   - *To prevent protection function errors, CITRIP should be placed as close to ITRIP and V_{SS} pins as possible.*
3. *V_{FO} circuit*
   - *V_{FO} output is an open-drain output. This signal line should be pulled up to the positive side of the 5 V/3.3 V logic power supply with a proper resistor RPU. It is recommended that RC filter be placed as close to the controller as possible.*

4. *VB-VS Circuit*
   - *Capacitor for high-side floating supply voltage should be placed as close to VB and VS pins as possible.*
5. *Snubber capacitor*
   - *The wiring between CIPOS™ Mini and snubber capacitor including shunt resistor should be as short as possible.*
6. *Shunt resistor*
   - *Each shunt resistor of SMD type should be used for reducing its stray inductance.*
7. *Ground pattern*
   - *Each ground pattern should be separated at only one point of shunt resistor as short as possible.*
   - *Power ground pattern between PFC and Inverter should be connected as short as possible.*
8. *Anti parallel diode*
   - *It is mandatory to connect anti-parallel diode (2 A, voltage rating higher than 650 V) to PFC IGBT.*
9. *Input surge voltage protection circuit*
   - *This protection circuit is necessary for PFC IGBT to be protected from excessive surge voltage*

4.3 Recommended rated output current of power supply

Control and gate drive power for the CIPOS™ Mini is normally provided by a single 15 V supply that is connected to the module V_{DD} and V_{SS} terminal. Also, we have to consider PFC IGBT power consumption. The circuit current of V_{DD} control supply of IFCM15P60GD is shown in below Table 8 (a), (b).

Table 8 The circuit current of control power supply of IFCM15P60GD

(a) Inverter Section

Item		Static (Typ.) [mA]	Dynamic (Typ.) [mA]	Total (Typ.) [mA]
$V_{DD} = 15$ [V]	$f_{SW} = 5$ [kHz]	1.3	1.9	3.2
	$f_{SW} = 20$ [kHz]	1.3	7.4	8.7

(b) PFC section with gate drive IC(IR44272L)

Item		Static (Typ.) [mA]	Dynamic (Typ.) [mA]	Total (Typ.) [mA]
$V_{DD} = 15$ [V]	$f_{SW} = 40$ [kHz]	0.4	3.2	3.6

And, the circuit current of the 5 V logic power supply (V_{FO} & input terminals) is about 20 mA

Finally, the recommended minimum circuit currents of power supply are shown in Table 9 which is considered ripple current and enough margins at the worst conditions, e.g. 5 times higher than the calculated value.

Table 9 The recommended minimum circuit current of power supply (Unit: [mA])

Item	The circuit current of +15 V control supply	The circuit current of +5 V logic supply
$V_{DD} \leq 15$ [V], $f_{SW} \leq 20$ [kHz]	62	45

4.4 Recommended layout pattern for OCP & SCP function

It is recommended that the ITRIP filter capacitor connections to the CIPOS™ Mini pins be as short as possible. The ITRIP filter capacitor should be connected to V_{SS} pin directly without overlapped ground pattern. The signal ground and power ground should be as short as possible and connected at only one point via the filter capacitor of V_{DD} line.

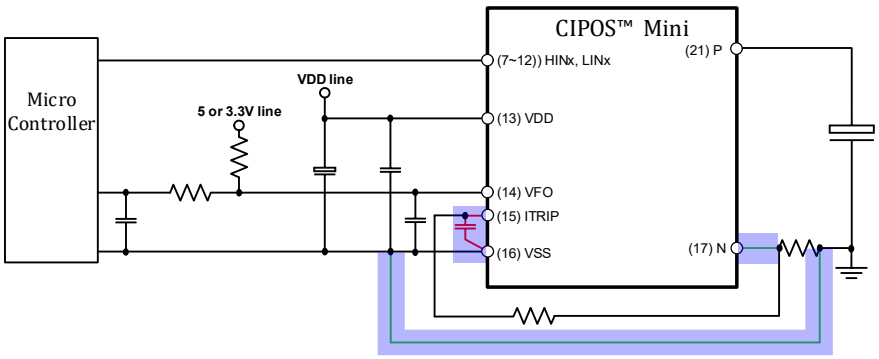


Figure 9 Recommended layout pattern for OCP & SCP function

4.5 Recommended wiring of shunt resistor and snubber capacitor

An external current sensing resistor is applied to detect overcurrent of phase currents. A long wiring pattern between the shunt resistor and CIPOS™ Mini will cause excessive surges that might damage the CIPOS™ Mini's internal IC and current detection components. This may also distort the sensing signal. To decrease the pattern inductance, the wiring between the shunt resistor and CIPOS™ Mini should be as short as possible. As shown in Figure 10, a snubber capacitor should be installed in the right location so as to suppress surge voltages effectively. Generally a high frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location '1' as shown in Figure 10, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location '2', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be a little lower than the calculated design value. The "2" position surge suppression effect is greater than the location '1' or '3'. The '3' position is a reasonable compromise with better suppression than in location '1' without impacting the current sensing signal accuracy. For this reason, the location '3' is generally used.

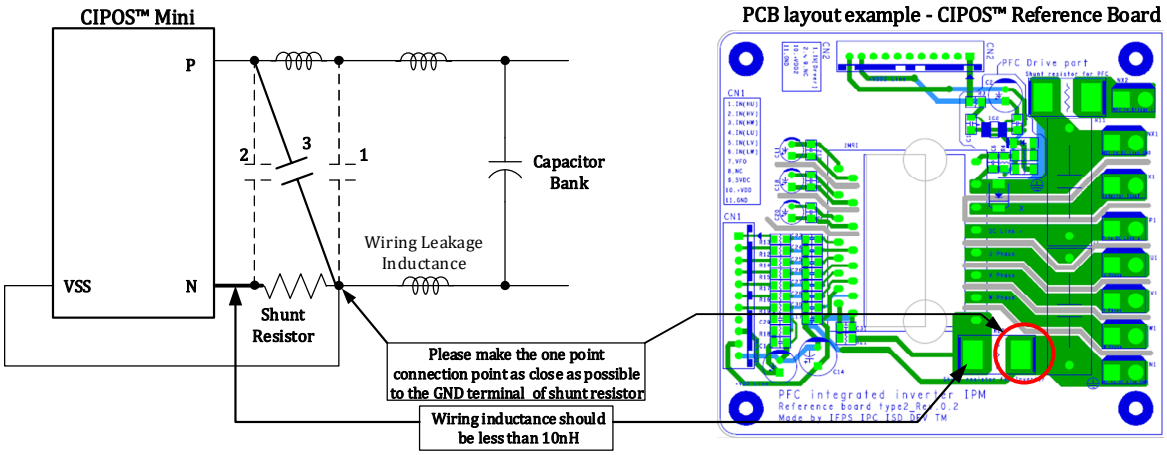


Figure 10 Recommended wiring of shunt resistor and snubber capacitor

4.6 Recommended layout for gate driving of PFC

We should consider PCB pattern layout carefully when drawing the layout for the PFC gate drive cicuit. Because PFC IGBT is operated with fast switching frequency, stable PFC IGBT operation is related to the pattern layout of the gate drive circuit. Especially, ground pattern design is more important.

In order to prevent interference of PFC gate signal by IGBT switching, we recommend pattern design as “2” and “4” in Figure 11. It needs one point connection between the ground of gate driver and the power ground as showin in the red circle in Figure 11. If PCB pattern is desgined as “1” and “3”, PFC IGBT might be operated improperly due to gate voltage oscillation. Also, we recommend adding RC filter for gate singal of PFC for stable IGBT operation.

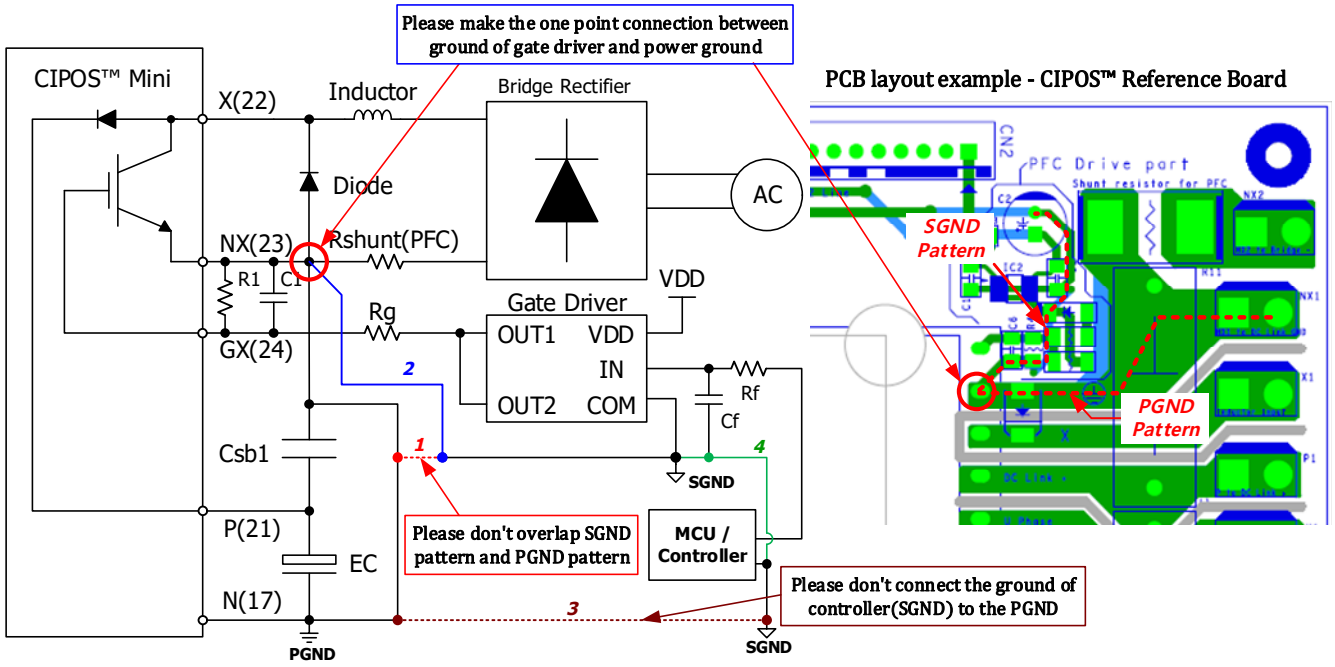


Figure 11 Recommended pattern layout between signa ground(SGND) and power ground(PGND)

4.7 Pin and screw holes coordinates for CIPOS™ Mini package footprint

Figure 12 shows CIPOS™ Mini package position on PCB to indicate center coordinates of each pin and screw hole in Table 10.

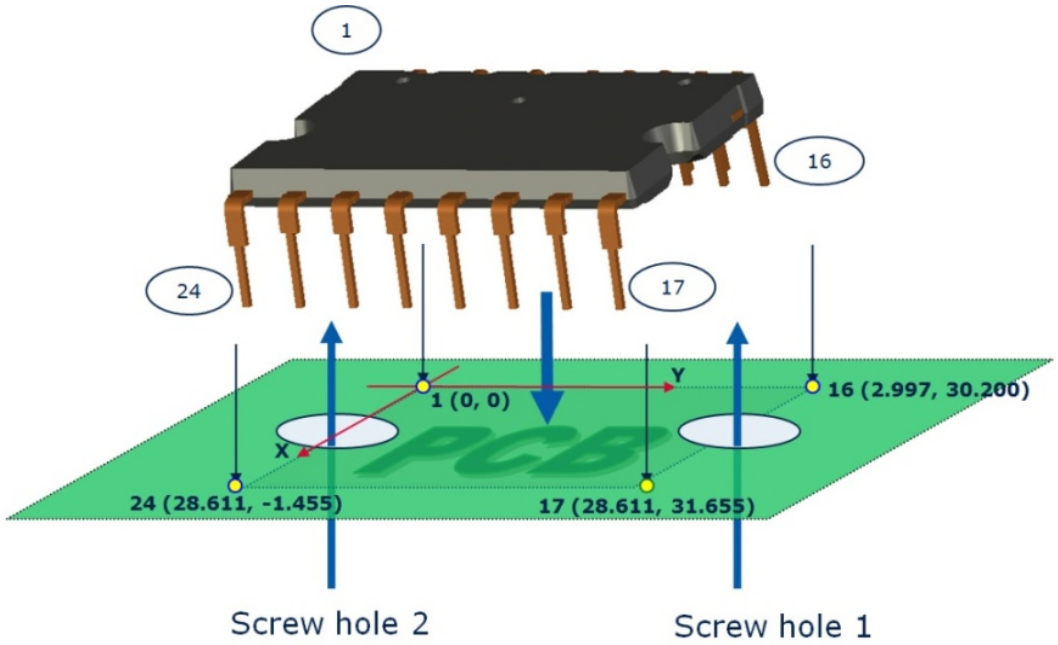


Figure 12 CIPOS™ Mini package position on PCB (Unit: [mm])

Table 10 Pin & screw holes coordinates for CIPOS™ Mini package footprint (Unit: [mm])

Pin number		X	Y	Pin number		X	Y
Signal pins	1	0.000	0.000	Signal pins	14	2.997	26.600
	2	2.997	2.000		15	0.000	28.200
	3	0.000	5.400		16	2.997	30.200
	4	2.997	7.000	Power pins	17	28.611	31.655
	5	0.000	10.400		18	28.611	26.925
	6	2.997	12.000		19	28.611	22.195
	7	0.000	15.400		20	28.611	17.465
	8	2.997	17.000		21	28.611	12.735
	9	0.000	18.600		22	28.611	8.005
	10	2.997	20.200		23	28.611	3.275
	11	0.000	21.800		24	28.611	-1.455
	12	2.997	23.400	Screw hole	25	17.950	32.000
	13	0.000	25.000		26	17.950	-1.800

5 Protection features

5.1 Undervoltage protection

Control and gate drive power for the CIPOS™ Mini is normally provided by a single 15 V supply that is connected to the module V_{DD} and V_{SS} terminals. For proper operation this voltage should be regulated to 15 V ± 10%. Table 11 describes the behavior of the CIPOS™ Mini for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected at the CIPOS™ Mini's pins.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1 V/µs.

The potential at the module's V_{SS} terminal is different from that at the N power terminal by the voltage drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (V_{SS}) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits to generate the floating supplies for the high-side gate drives.

When control supply voltage (V_{DD} and V_{BS}) falls down under UVLO level, IGBT will turn off while ignoring the input signal.

Table 11 CIPOS™ Mini functions versus control power supply voltage

Control Voltage Range [V]	CIPOS™ Mini Function Operations
0 ~ 4	Control IC does not operate. UVLO and fault output does not operate.
4 ~ 13	As the UVLO function is activated, control input signals are blocked and a fault signal V_{FO} is generated.
13 ~ 14	IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range so the $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition. And high-side IGBTs can't operate after V_{BS} initial charging because V_{BS} can't reach to V_{BSUV+}.
14 ~ 18.5 for V_{DD} 13.5 ~ 18.5 for V_{BS}	Normal operation. This is the recommended operating condition. V_{DD} of 16 V is recommended when only integrated bootstrap circuitry is used. (14.5 ~ 18.5 V V_{DD} is recommended for IFCMxx60Gy)
18.5 ~ 20 for V_{DD} 18.5 ~ 20 for V_{BS}	IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the CIPOS™ Mini might be damaged.

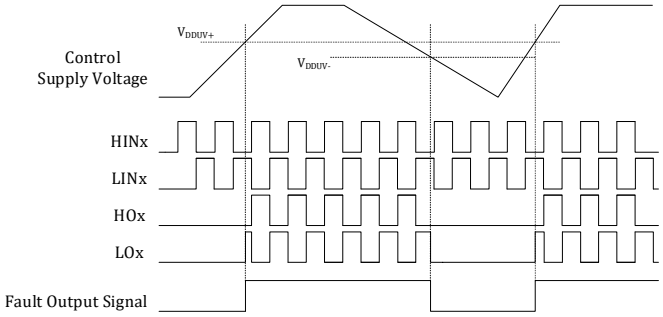


Figure 13 Timing chart of low-side undervoltage protection function

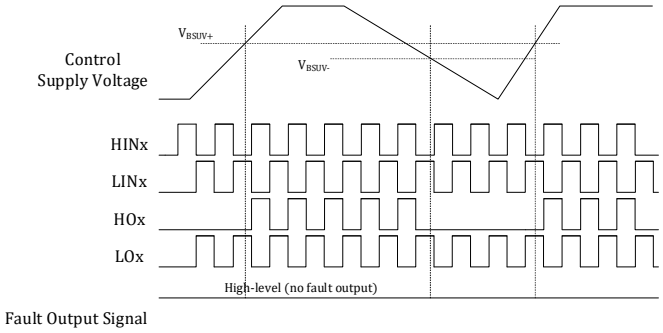


Figure 14 Timing chart of high-side undervoltage protection function

5.2 Overcurrent protection

5.2.1 Timing chart of overcurrent (OC) protection

The CIPOS™ Mini has an overcurrent shutdown function. Its internal IC monitors the voltage of the ITRIP pin and if this voltage exceeds the $V_{IT,TH+}$, which is specified in the devices datasheets, a fault signal is activated and all IGBTs are turned off. Typically the maximum short circuit current magnitude is gate voltage dependant. A higher gate voltage results in a larger short circuit current. In order to avoid this potential problem, the maximum overcurrent trip level is generally set to below 2 times the nominal rated collector current. The overcurrent protection-timing chart is shown in Figure 15.

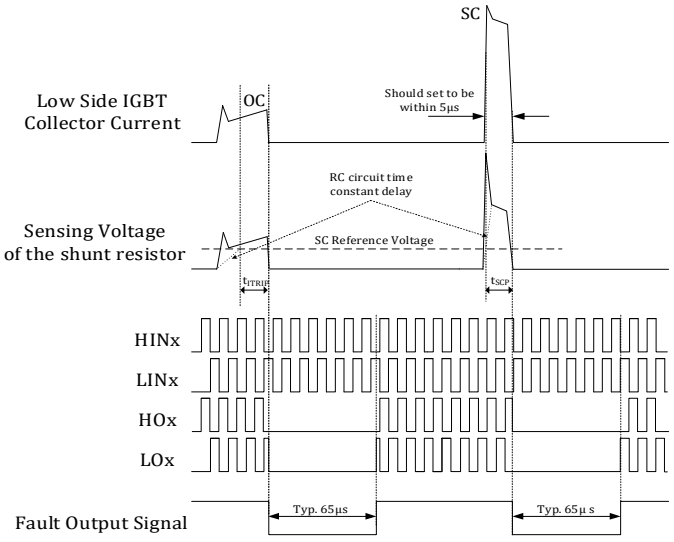


Figure 15 Timing chart of overcurrent protection function

5.2.2 Selecting current sensing shunt resistor

The value of the current sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive going threshold voltage of CIPOS™ Mini. It is typically 0.47 V. I_{OC} is the current of OC detection level.

The maximum value of OC protection level should be set lower than the repetitive peak collector current in the datasheet considering the tolerance of shunt resistor.

For example, the maximum peak collector current of IFCM10P60GD is 20 A_{peak}, and thus, the recommended value of the shunt resistor is calculated as

$$R_{SH(min)} = \frac{0.47}{20} = 0.024\Omega$$

For the power rating of the shunt resistor, the below list should be considered:

- Maximum load current of inverter (I_{rms})
- Shunt resistor value at $T_C = 25°C$ (R_{SH})
- Power derating ratio of shunt resistor at $T_{SH} = 100°C$ according to the manufacturer's datasheet
- Safety margin

The shunt resistor power rating is calculated by the following equation.

$$P_{SH} = \frac{I_{rms}^2 \times R_{SH} \times margin}{deratingratio} \quad (2)$$

For example, in case of IFCM10P60GD and $R_{SH} = 24\ m\Omega$:

- Max. load current of the inverter: 6 A_{rms}
- Power derating ratio of shunt resistor at $T_{SH} = 100°C$: 80%
- Safety margin : 30%

$$P_{SH} = \frac{6^2 \times 0.024 \times 1.3}{0.8} = 1.40W$$

A proper power rating of shunt resistor is over than 1.4 W, e.g. 2 W.

Based on the previous equations, conditions, and calculation method, the minimum shunt resistance and resistor power according to CIPOS™ Mini products are introduced as listed in Table 12.

It's noted that a proper resistance and power rating higher than the minimum value should be chosen considering the overcurrent protection level required in the application.

Table 12 Minimum R_{SH} and P_{SH}

Product	Maximum peak current	Minimum shunt resistance, R_{SH}	Minimum shunt resistor power, P_{SH}
IFCM10P60zD	20 A	24 mΩ	1.5 W
IFCM10S60zD	20 A	24 mΩ	1.5 W
IFCM15P60zD	30 A	16 mΩ	3 W
IFCM15S60zD	30 A	16 mΩ	3 W

5.2.3 Delay time

The RC filter is necessary in the overcurrent sensing circuit to prevent malfunction of OC protection caused by noise. The RC time constant is determined by considering the noise duration and the short-circuit withstand time capability of the IGBT.

When the sensing voltage on shunt resistor exceeds the ITRIP positive going threshold ($V_{IT,TH+}$), this voltage is applied to the ITRIP pin of CIPOS™ Mini via the RC filter. Table 13 shows the specification of the OC protection reference level. The filter delay time (t_{FILTER}) that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is caused by below equation (3), (4).

$$V_{IT,TH+} = R_{SH} \cdot I_C \cdot \left(1 - \frac{1}{e^{\frac{t_{Filter}}{\tau}}}\right) \quad (3)$$

$$t_{Filter} = -\tau \cdot \ln\left(1 - \frac{V_{IT,TH+}}{R_{SH} \cdot I_C}\right) \quad (4)$$

Where, $V_{IT,TH+}$ is the ITRIP pin input voltage, I_C is the peak current, R_{SH} is the shunt resistor value and τ is the RC time constant. In addition there is a shutdown propagation delay of Itrip (t_{ITRIP}). Please refer to Table 14.

Table 13 Specification of OC protection reference level ' $V_{IT,TH+}$'

Item	Min.	Typ.	Max.	Unit
ITRIP positive going threshold $V_{IT,TH+}$	0.40	0.47	0.54	V

Table 14 Internal delay time of OC protection circuit

Item		Condition	Min.	Typ.	Max.	Unit
Shut down propagation delay (t_{ITRIP})	IFCM10P60zD	I_{out} = 6 A, from $V_{IT,TH+}$ to 10% I_{out}	-	1290	-	ns
	IFCM10S60zD					
	IFCM15P60zD	I_{out} = 10 A, from $V_{IT,TH+}$ to 10% I_{out}	-	1330	-	
	IFCM15S60zD					

Therefore the total time from ITRIP positive going threshold ($V_{IT,TH+}$) to the shut down of the IGBT becomes:

$$t_{TOTAL} = t_{FILTER} + t_{ITRIP} \quad (5)$$

The total delay must be less than the 5 µs of short circuit withstand time (t_{SC}) in the datasheet. Thus, the RC time constant should be set in the range of 1~2 µs. Recommended values for the filter components are R = 1.8 kΩ and C = 1 nF.

5.3 Fault output circuit

Table 15 Fault-output maximum ratings

Item	Symbol	Condition	Rating	Unit
Fault output supply voltage	V_{FO}	Applied between V_{FO}-V_{SS}	-0.5~ V_{DD}+0.5	V
Fault output current	I_{FO}	Sink current at V_{FO} pin	10	mA

Table 16

Table 17 Electric characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output current	I_{FO}	V_{ITRIP} = 0 V, V_{FO} = 5 V	-	2	-	nA
Fault output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.5	-	V

Because V_{FO} terminal is an open-drain type, it must be pulled up to the high level via a pull-up resistor. The resistor has to be calculated according to the above specifications.

5.4 Over temperature protection

CIPOS™ Mini with optional temperature sensing function has one pin for both fault-output and temperature sensing. Figure 16 shows the internal thermistor resistance characteristics as a function of the thermistor temperature. A circuitry is introduced in this section for over temperature protection. As shown in Figure 17, V_{FO} pin is connected directly to the ADC and fault detection terminals of the microcontroller. This circuit is very simple and allows the IGBTs have to be shut down by the microcontroller. For example, when R1 is 3.6 kΩ, then V_{FO} at about 100°C of thermistor temperature is 2.95 V_{typ} at V_{ctr} = 5 V and 1.95 V at V_{ctr} = 3.3 V, as shown in Figure 18. It's noted that V_{FO} for over temperature protection should be not less than microcontroller fault trip level.

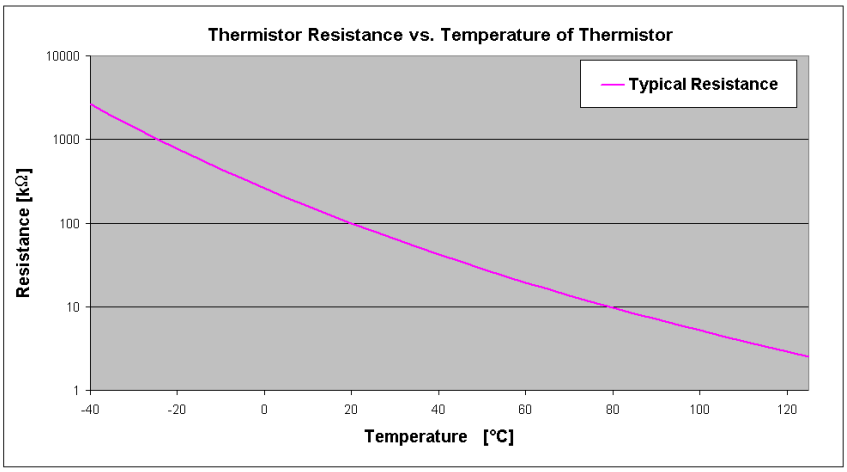


Figure 16 Internal thermistor resistance characteristics as a function of thermistor temperature

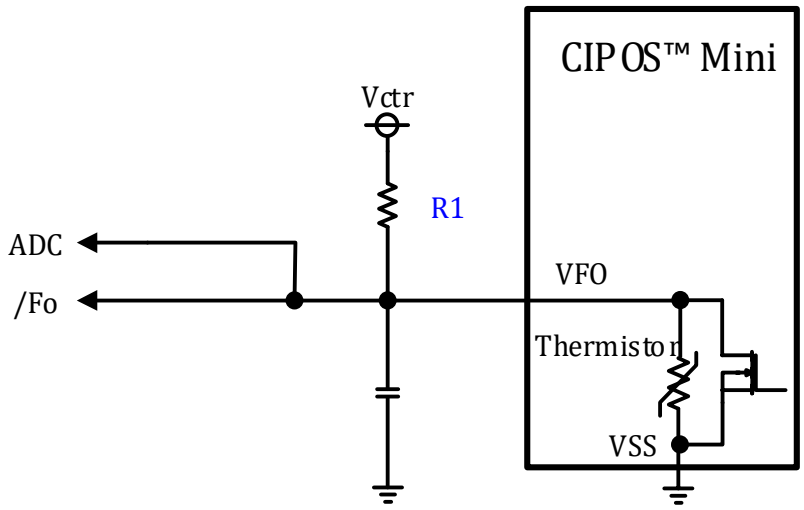


Figure 17 Circuit proposals for over temperature protection

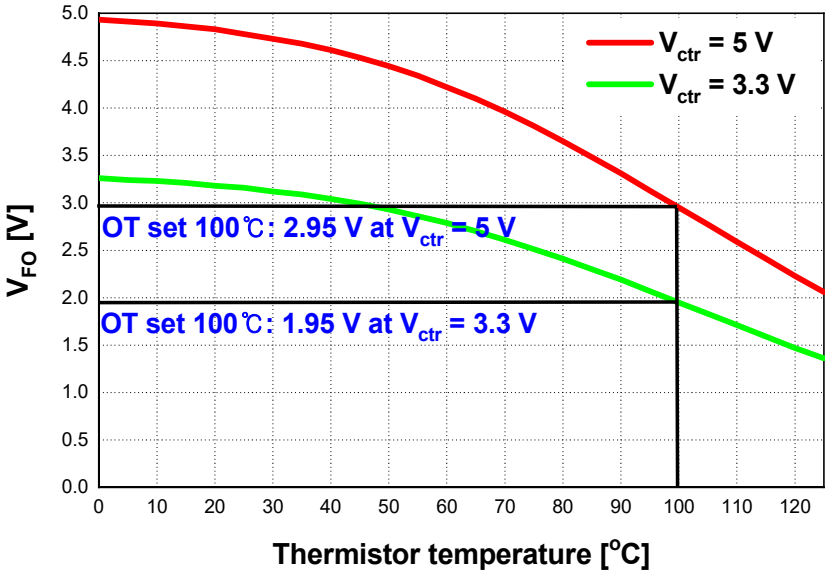


Figure 18 Voltage of V_{FO} pin according to thermistor temperature

6 Bootstrap Circuit

6.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,V,W)}$ and $V_{S\,(U,V,W)}$, provides the supply to the IC within the CIPOS™ Mini. This supply voltage must be in the range of 13.0~18.5V to ensure that the IC can fully drive the high-side IGBT. The CIPOS™ Mini includes an undervoltage detection function for the V_{BS} to ensure that the IC does not drive the high-side IGBT if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note that the UVLO function of any high-side section acts only on the triggered channel without any feedback to the control level.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and cheap. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a diode, resistor and capacitor as shown in Figure 19. The current flow path of the bootstrap circuit is shown in Figure 19. When V_S is pulled down to ground (either through the low-side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

6.2 Internal bootstrap functionality characteristics

CIPOS™ Mini includes three bootstrap functionalities in the internal driver IC, which consist of three diodes and three resistors, as shown in Figure 3. A typical value of the internal bootstrap resistor is 40 Ω at room temperature. For more information, please refer to Table 18. R_{BS2} and R_{BS3} have the same value with R_{BS1}.

V_{DD} of 16 V is recommended when only the integrated bootstrap circuitry is used.

Table 18 Electrical characteristics of internal bootstrap parameters

Description	Condition	Symbol	Min.	Typ.	Max.	Unit
Repetitive peak reverse voltage		V_{RRM}	600	-	-	V
Bootstrap resistance of U-phase	VS2 or VS3 = 300 V, T_J = 25°C VS2 and VS3 = 0 V, T_J = 25°C VS2 or VS3 = 300 V, T_J = 125°C VS2 and VS3 = 0 V, T_J = 125°C	R_{BS1}	-	35 40 50 65	-	Ω
Reverse recovery	I_F = 0.6 A, di/dt = 80 A/µs	t_{rr_BS}	-	50	-	ns
Forward voltage drop	I_F = 20 mA, VS2 and VS3 = 0 V	V_{F_BS}	-	2.6	-	V

High voltage supply to gate driver between VSx and V_{SS} is limited to dynamic operation.

If it is necessary to reduce the bootstrap resistance, an external bootstrap circuitry is recommended. For example, when 39 Ω of bootstrap resistor and 1N4937 of bootstrap diode are connected externally to CIPOS™ Mini, the bootstrap resistance becomes around 25 Ω, as shown in Table 19.

Table 19 Bootstrap resistance with external bootstrap circuitry (39 Ω and 1N4937)

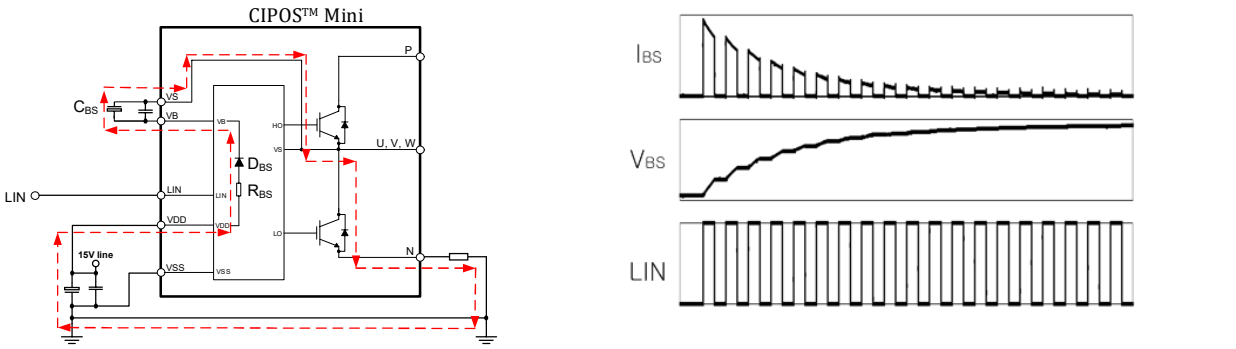
Description	Condition	Symbol	Min.	Typ.	Max.	Unit
Bootstrap resistance of U-phase	T_J = 25°C T_J = 125°C	R_{BS1}	-	24 28	-	Ω

6.3 Initial charging of bootstrap capacitor

Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_{FD} - V_{LS}}\right) \quad (6)$$

- V_{FD} = Forward voltage drop across the bootstrap diode
- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor voltage
- V_{LS} = Voltage drop across the low-side IGBT
- δ = Duty ratio of PWM



(a) Bootstrap circuit (b) Timing chart of initial bootstrap charging

Figure 19 Bootstrap circuit operation and initial changing

6.4 Bootstrap capacitor selection

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V} \quad (7)$$

- Where,
- Δt = maximum ON pulse width of high-side IGBT
- ΔV = the allowable discharge voltage of the C_{BS}.
- I_{leak}= maximum discharge current of the C_{BS} mainly via the following mechanisms:
  - Gate charge for turning the high-side IGBT on
  - Quiescent current to the high-side circuit in the IC
  - Level-shift charge required by level-shifters in the IC
  - Leakage current in the bootstrap diode
  - C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
  - Bootstrap diode reverse recovery charge

In practice a leakage current of 1 mA is recommended as a calculation basis for CIPOS™ Mini. By taking in consideration dispersion and reliability, the capacitance is generally selected to be 2~3 times higher than the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the VS voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the pins of the CIPOS™ Mini as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the CIPOS™ Mini is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

6.5 Charging and discharging of the bootstrap capacitor during PWM-inverter operation

The bootstrap capacitor C_{BS} charges through the bootstrap diode D_{BS} and resistor R_{BS} according to Figure 19 from the V_{DD} supply when the high-side IGBT is off, and the V_S voltage is pulled down to ground. It discharges when the high-side IGBT or diode are on.

Example 1: Selection of the initial charging time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (6).

Conditions:

- $C_{BS} = 4.7\ \mu F$, $R_{BS} = 40\ \Omega$, Duty ratio (δ) = 0.5, D_{BS} = internal bootstrap diode, $V_{DD} = 15\ V$, $V_{FD} = 0.9\ V$
- $V_{BS\ (min)} = 13.5\ V$, $V_{LS} = 0.1\ V$

$$t_{charge} \geq 4.7\mu F \times 40\Omega \times \frac{1}{0.5} \times \ln\left(\frac{15V}{15V-13.5V-0.9V-0.1V}\right) \cong 1.1ms$$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

Example 2: The minimum value of the bootstrap capacitor

Conditions:

- $\Delta V = 0.1\ V$, $I_{leak} = 1\ mA$

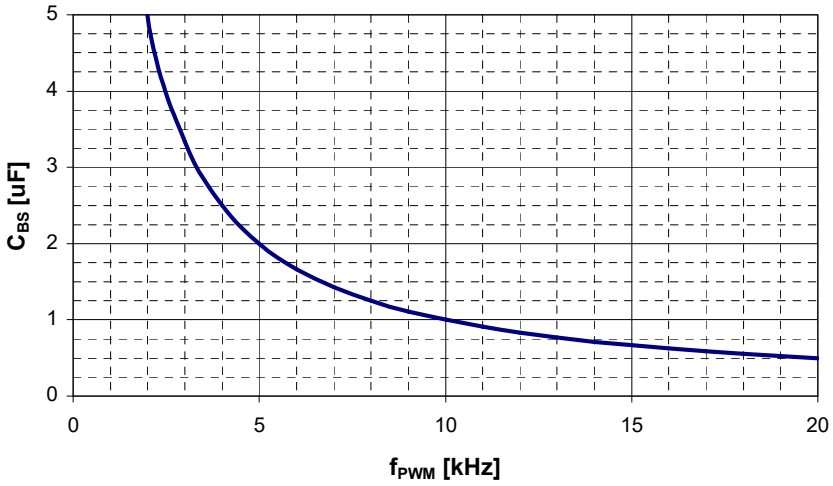


Figure 20 Bootstrap capacitance as a function of the switching frequency

Figure 20 shows the curve corresponding to equation (7) for a continuous sinusoidal modulation, if the voltage ripple ΔV_{BS} is 0.1 V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range of up to 4.7 µF for most switching frequencies. In other PWM method case like a discontinuous sinusoidal modulation, the t_{charge} must be set the longest period of the low-side IGBT off.

Note that this result is only an example. It is recommended that the system design considers the actual control pattern and lifetime of the used components.

7 Single-phase boost PFC

7.1 Basic introduction

The PFC section of the CIPOS™ Mini PFC-integrated IPM consists of IGBT and Diode. 650 V TRENCHSTOP™ IGBT or TRENCHSTOP™ 5 IGBT and 650 V rapid switching emitter-controlled diode are selected in order to deliver lower switching loss and better ruggedness for PFC application. IFCMxxS60GD utilizes TRENCHSTOP™ IGBT which is optimized for medium speed switching frequency (up to 40 kHz) and IFCMxxP60GD utilizes TRENCHSTOP™ 5 IGBT which is optimized for high speed switching frequency (up to 60 kHz).

On the other hand, the PFC section of this IPM doesn't include the gate drive IC part. So, we need more consideration for driving the PFC IGBT than for the 3-phase inverter section.

7.2 General application example

Figure 21 shows general application example for PFC section on the CIPOS™ Mini PFC-integrated IPM.

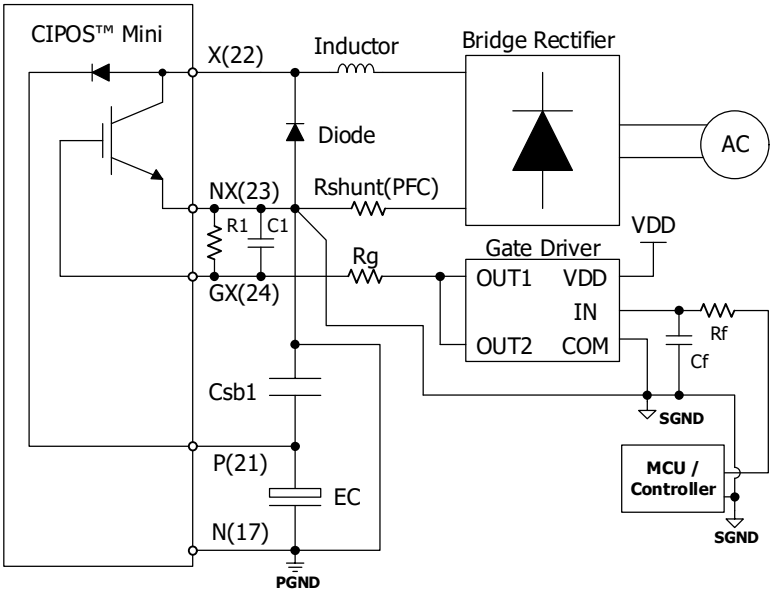


Figure 21 Application example

7.2.1 Gate drive IC

In order to drive the PFC IGBT, we strongly recommend using a gate driver IC such as IRS44273L which is a single low-side driver IC. Features of IRS44273L are as below,

Features

- CMOS Schmitt-triggered input
- Undervoltage lockout
- 3.3 V logic compatible
- 1.5 A sinking / sourcing current (typical)
- 50 nsec turn-on/off propagation delay (typical)

7.2.2 Gate resistor selection

For the gate resistance and capacitance for PFC IGBT, we suggest R_G = 10 Ohm, C_{GE} = 4.7 nF as Table 20 in order to have stable operation. However, it can be changed depending on user's conditions.

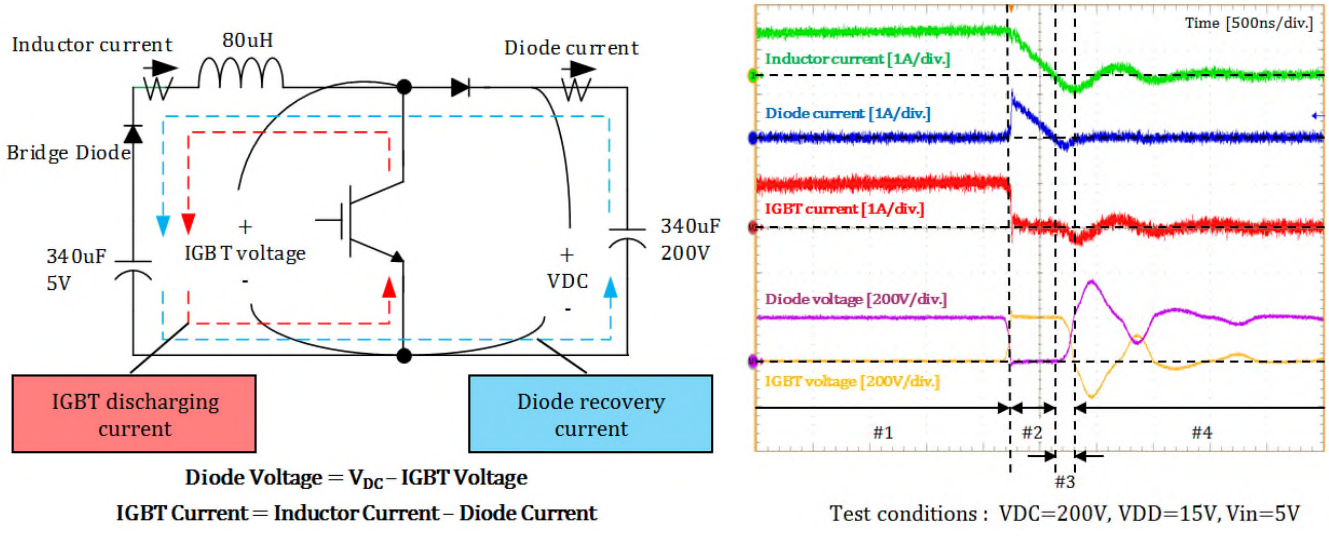
Table 20 Switching characteristics at recommended gate drive parameters(V_{DC} = 400 V, V_{GE} = 15 V, I_C = 15 A, T_J = 25°C)

Product	R_G [Ω]	C_{GE} [nF]	E_{ON} [µJ]	On dv/dt [kV/µs]	On di/dt [A/µs]	E_{OFF} [µJ]	Off dv/dt [kV/µs]	Off di/dt [A/µs]
IFCM15P60zD	10	4.7	368	8.1	368	99	17.9	664
IFCM15S60zD	10	4.7	570	5.7	249	212	8.9	525

7.2.3 Anti-parallel diode between collector and emitter

During startup, shutdown and under fault conditions power circuits often pass through operating modes that are not readily apparent from normal operation analysis. And example is the standard boost PFC circuit. A PFC circuit may be designed to operate its boost inductor in the continuous current mode (CCM) during mormal load operation. However, under light load, the boost inductor may go into discontinuous current mode (DCM) conduction. Discontinous operation may also occur near the AC mains zero voltage crossing even under full load conditions. Operation in DCM may require the PFC switching device to conduct in the reverse direction. If an alternate current path is not provided for this switch current reversal, the IGBT may be reverse avalanched. In most cases low energy reverse avalanche is not harmful to IGBTs but it will cause additional heating. However, under specific circumstances gradual degradation and failure is possible. If the energy associated with this current reversal is minimal the failure mode may not be immediate but appear as gradual device degradation and random device failures. For detailed information, please refer to [7].

Figure 22 explain circuit operation about negative voltage generation at IGBT during DCM mode operation at low AC input conditions. When IGBT status was changed from turn-on (#1) to turn-off (#2), diode reverse recovery current flow via circuit path (#3) when inductor current was became zero. At this time, IGBT voltage goes down negative value (#4).



(a) Circuit operation during IGBT On/Off (b) Waveform at each component

Figure 22 Circuit operation and operating waveform during DCM mode operation at low AC input condition

So, in order to prevent random failure problem by reverse avalanched, anti-parallel diode should be added between collector and emitter to bypass reverse current. For anti-parallel diode, voltage rating is same with boost IGBT rating and current rating is 1~2 [A]. We recommend 800 V, 2 A rating fast recovery diode. Figure 23 shows effect of anti-parallel diode.

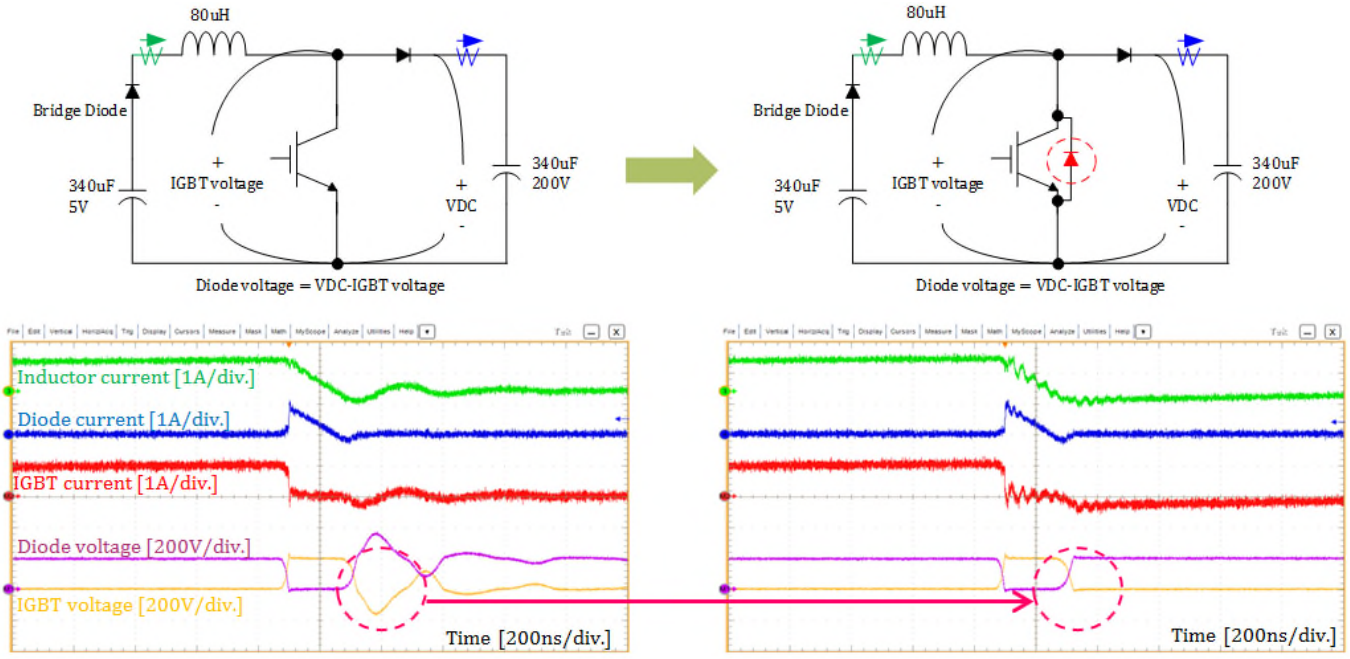


Figure 23 Correction of negative voltage at IGBT by using anti-parallel diode

8 Thermal system design

8.1 Introduction

The thermal design of a system is a key issue of CIPOS™ Mini PFC-integrated IPM in electronic systems such as drives. In order to avoid overheating and / or to increase reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing CIPOS™ Mini family as intelligent power module for the application. To get the most out of the system a proper heat sink choice is necessary. A good thermal design either allows to maximize the power or to increase the reliability of the system (by reducing the maximum temperature). This application note will give a short introduction to power losses and heat sinks, helping to understand the mode of operation and to find the right heat sink for a specific application.

For the thermal design, one needs:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,max}$ of the power semiconductors
- The junction to ambient thermal resistance impedance $Z_{th,J-A}$. For stationary considerations the static thermal resistance $R_{th,J-A}$ is sufficient. This thermal resistance comprises the junction to case thermal resistance $R_{th,J-C}$ as provided in datasheets, the case to heat sink thermal resistance $R_{th,C-HS}$ accounting for the heat flow through the thermal interface material between heat sink and the power module and the heat sink to ambient thermal resistance $R_{th,HS-A}$. Each thermal resistance can be extended to its corresponding thermal impedance by adding the thermal capacitances.
- The maximum allowable ambient temperature $T_{A,max}$

Furthermore all heat flow paths need to be identified. Figure 24 presents a typical simplified equivalent circuit for the thermal network of CIPOS™ Mini PFC-integrated IPM. This circuit is simplified as it omits thermal capacitances and typically negligible heat paths such as the heat transfer from the module surface directly to the ambient via convection and radiation.

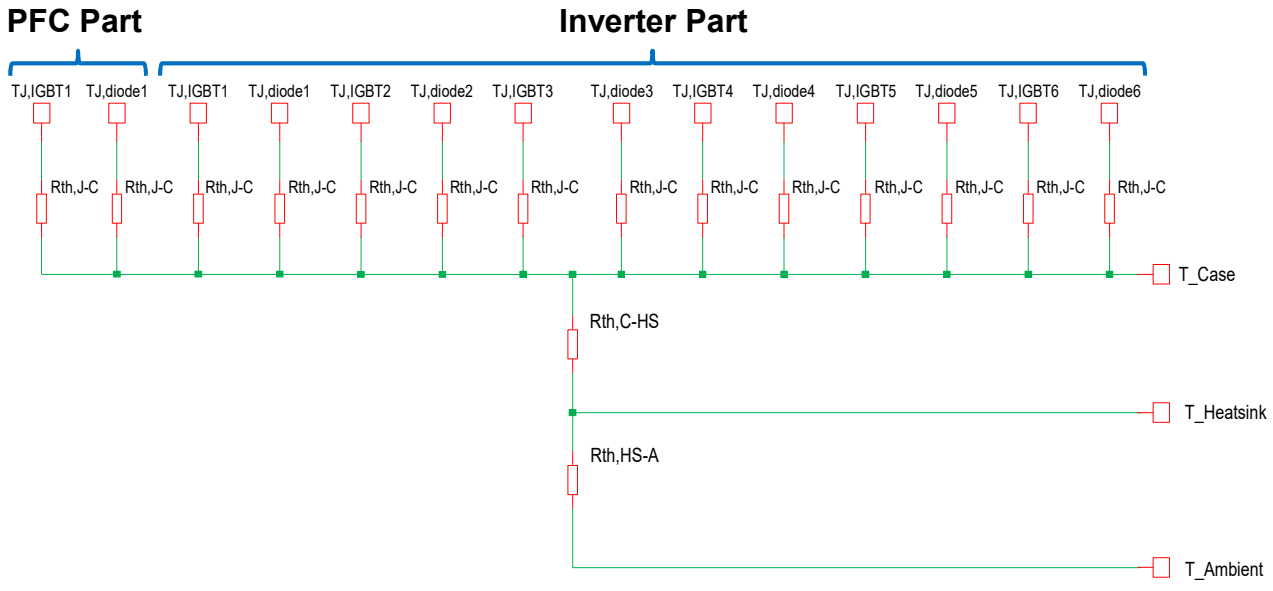


Figure 24 Simplified thermal equivalent circuit

8.2 Power loss (inverter section)

The power losses of inverter section in the CIPOS™ Mini PFC-integrated IPM are composed of conduction and switching losses in the IGBTs and diodes. The loss during the turn-off steady state can be ignored because it is very small amount and has little effect on increasing the temperature in the device. The conduction loss depends on the dc electrical characteristics of the device i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand the switching loss is determined by the dynamic characteristics like turn-on/off time and over-voltage/current. Hence, in order to obtain the accurate switching loss, the DC-link voltage of the system, the applied switching frequency and the power circuit layout in addition to the current and temperature should be considered.

In this chapter, based on a PWM-inverter system for motor control applications, detailed equations are shown to calculate both losses of the CIPOS™ Mini for a 3-phase continuous sinusoidal PWM. For other cases like 3-phase discontinuous PWMs, please refer to [8].

8.2.1 Conduction losses

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$V_{IGBT} = V_I + R_I \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i \qquad (8)$$

- V_I = Threshold voltage of IGBT
- V_D = Threshold voltage of Diode
- R_I = on-state slope resistance of IGBT
- R_D = on-state slope resistance of Diode

Assuming that the switching frequency is high, the output current of the PWM-inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak}\cos(\theta - \varphi) \qquad (9)$$

Where, ϕ is the phase-angle difference between output voltage and current. Using equations (8) and (9), the conduction loss of one IGBT and its monolithic body diode can be obtained as follows.

$$P_{con.I} = \frac{1}{2\pi}\int_0^{\pi} \xi(V_{IGBT} \times i)d\theta = \frac{I_{peak}}{2\pi}V_I + \frac{I_{peak}}{8}V_I M I\cos\varphi + \frac{I_{peak}^2}{8}R_I + \frac{I_{peak}^2}{3\pi}R_I M I\cos\varphi \qquad (10)$$

$$P_{con.D} = \frac{1}{2\pi}\int_0^{\pi} (1-\xi)(V_{DIODE} \times i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D M I\cos\varphi + \frac{I_{peak}^2}{8}R_D - \frac{I_{peak}^2}{3\pi}R_D M I\cos\varphi \qquad (11)$$

$$P_{con} = P_{con.I} + P_{con.D} \qquad (12)$$

Where ξ is the duty cycle in the given PWM method.

$$\xi = \frac{1 + MI\cos\theta}{2} \qquad (13)$$

Where, MI is the PWM modulation index (MI, defined as the peak phase voltage divided by the half of dc link voltage).

It should be noted that the total inverter conduction losses are six times of the P_{con}.

8.2.2 Switching losses

Different devices have different switching characteristics and they also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (Joule) can be experimentally measured indirectly by multiplying the current and voltage and integrating over time, under a given circumstance. Therefore the linear dependency of the switching energy loss on the switched-current is expressed during one switching period as follows.

Switching energy loss $= (E_I + E_D) \times i\ [J]$ (14)

$$E_I = E_{I.ON} + E_{I.OFF} \quad (15)$$

$$E_D = E_{D.ON} + E_{D.OFF} \quad (16)$$

Where, E_I i is the switching loss energy of the IGBT and E_D i is for the diode. E_I and E_D can be considered a constant approximately.

As mentioned in the equation (9), the output current can be considered a sinusoidal waveform and the switching loss occurs every PWM period for the continuous PWM schemes. Therefore, depending on the switching frequency f_{SW}, the switching loss of one device is the following equation (17).

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi}(E_I + E_D)\ i\ f_{sw}\,d\varphi = \frac{(E_I + E_D)f_{sw}I_{peak}}{\pi} \quad (17)$$

Where, E_I is a unique constant of IGBT related to the switching energy and different IGBT have different E_I value. E_D is the constant for the diode. Those should be derived by experimental measurement. From the equation (17), it should be noted that the switching losses are a linear function of current and directly proportional to the switching frequency.

8.3 Power loss (PFC section)

PFC shapes the input current of the power supply to be synchronized with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics. In order to proper design, we need to consider several factors. However, in this chapter, we introduce the equation for power losses estimation of IGBT and diode. For other design infromation like bridge rectifier, gate drive circuit, boost inductor, AC line current filter, and etc, please refer to [9]

8.3.1 Conduction losses

Following is the theory for the simplified power loss calculation.

For simplicity input waveforms are full periodic sinusoidal signals:

$V_{in}(t) = V_{in,peak} * sin(\omega * t)$

The first half wave (T/2) current for the controlled and uncontrolled switch:

$I_{in}(t) = I_{in} * sin(\omega * t)$

$I_{IGBT}(t) = PWM(t) * I_{in}(t)$

$I_{Diode}(t) = (1 - PWM(t)) * I_{in}(t)$

Input voltage peak to output voltage ratio is taken as variable($0 \leq \frac{V_{in,peak}}{V_{out}} \leq 1$).

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$V_{IGBT} = V_I + R_I \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i$$

- V_I = Threshold voltage of IGBT
- V_D = Threshold voltage of diode
- R_I = on-state slope resistance of IGBT
- R_D = on-state slope resistance of diode

The average conduction loss of the IGBT for the first half wave is:

$$P_{cond,IGBT} = \frac{2}{T} * \int_0^{\frac{T}{2}} V_{IGBT}(I_C(t)) * I_C(t) dt$$

Therefore it is possible to describe the V_{IGBT} characteristics with two prameters (V_I, R_I) and use them for the calculation of conduction losses.

$$P_{cond,IGBT} = \frac{2}{T} * \int_0^{\frac{T}{2}} (V_I + PWM(t) * I_{in}(t) * R_I) * PWM(t) * I_{in}(t) dt$$

Using:

$$PWM^2(t) = PWM(t)$$

and using D as average model IGBT duty cycle:

$$D(t_i) = \frac{1}{T_{SW}} * \int_{t_i}^{t_i + T_{SW}} PWM(t) dt$$

$$P_{cond,IGBT} = \frac{2}{T} * (V_I * \int_0^{\frac{T}{2}} PWM(t) * I_{in}(t) dt + R_I * \int_0^{\frac{T}{2}} PWM(t) * I_{in}^2(t) dt)$$

For contiuous conduction mode operation:

$$D(t) = 1 - \frac{V_{in,peak}}{V_{out}} * sin(\omega * t)$$

Therefore, the result:

$$P_{cond,IGBT} = \frac{2}{T} * (V_I * I_{in} * \sqrt{2} * \int_0^{\frac{T}{2}} sin(\omega * t) - \frac{V_{in,peak}}{V_{out}} * sin^2(\omega * t) dt + R_I * I_{in}^2 * \int_0^{\frac{T}{2}} sin^2(\omega * t) - \frac{V_{in,peak}}{V_{out}} * sin^3(\omega * t) dt)$$

$$P_{cond,IGBT} = V_I * I_{in} * \left(\frac{2 * \sqrt{2}}{\pi} - \frac{V_{in,peak}}{V_{out}} * \frac{1}{\sqrt{2}}\right) + R_I * I_{in}^2 * (1 - \frac{V_{in,peak}}{V_{out}} * \frac{8}{3 * \pi})$$

The same way for the boost diode:

$$P_{cond,diode} = \frac{V_{in,peak}}{V_{out}} * (V_D * I_{in} * \frac{1}{\sqrt{2}} + R_D * I_{in}^2 * \frac{8}{3 * \pi})$$

8.3.2 Switching losses

The influence of the diode for the switch on losses of the IGBT makes it necessary to characterize the IGBT and diode pair together.

$$P_{swi,IGBT} = F_{SW} * \frac{2}{T} * \int_0^{\frac{T}{2}} E_{off}(I_{IGBT}(t)) + E_{on}(I_{IGBT}(t))dt$$

Assuming linear switching characteristics, it is possible to describe the switching characteristics with 4 parameters ($E_{off,0}$, $E_{off,n}$, $E_{on,0}$, $E_{on,n}$) and use them for calculation of the switching loesses:

$$E_{off}(I_{IGBT}) = E_{off,0} + \frac{E_{off,n} - E_{off,0}}{I_n} * I_{IGBT}$$

$$E_{on}(I_{IGBT}) = E_{on,0} + \frac{E_{on,n} - E_{on,0}}{I_n} * I_{IGBT}$$

With I_n and V_n are the nominal current and output voltage where switching losses were measured and F_{SW} is a constant switching frequency:

$$P_{swi,IGBT} = \frac{V_{out}}{V_n} * F_{SW} * \frac{2}{T} * \int_0^{\frac{T}{2}} E_{off,0} + E_{on,0} + \frac{(E_{off,n} - E_{off,n} + E_{on,n} - E_{on,0})}{I_n} * I_{IGBT}(t)dt$$

The switching losses are calculated to:

$$P_{swi,IGBT} = \frac{V_{out}}{V_n} * F_{SW} * (E_{off,0} + E_{on,0} + \frac{I_{in}}{I_n} * \sqrt{2} * \frac{2}{\pi} * (E_{off,n} - E_{on,0} + E_{on,n} - E_{on,0})$$

Same for the Diode:

$$P_{swi,Diode} = \frac{V_{out}}{V_n} * F_{SW} * (E_{rec,0} + \frac{I_{in}}{I_n} * \sqrt{2} * \frac{2}{\pi} * (E_{rec,n} - E_{rec,0}))$$

8.4 Thermal impedance

In practical operation, the power loss P_D is cyclic and therefore the transient impedance needs to be considered. The thermal impedance is typically represented by a RC equivalent circuit as shown in Figure 25. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the CIPOS™ Mini. Figure 26 and Figure 27 shows thermal impedance of IGBT and co-pack diode from junction to case curves of IFCM15P60GD. The thermal resistance goes into saturation in about 10 seconds.

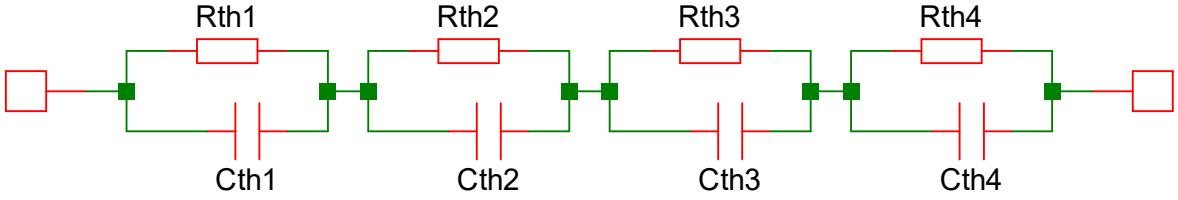


Figure 25 Thermal impedance RC equivalent circuit

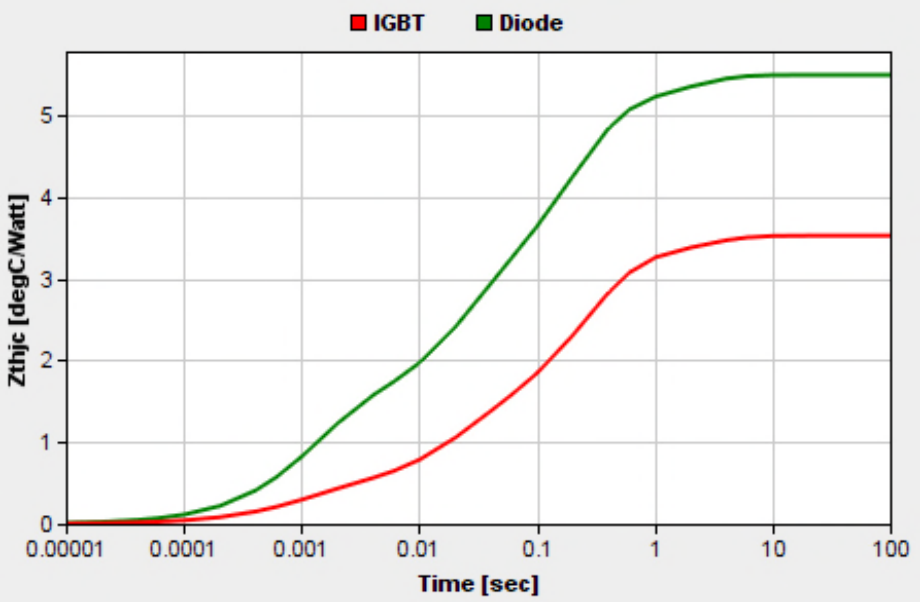


Figure 26 Thermal impedance curves (IFCM15P60GD, inverter part based on multi-chip heating)

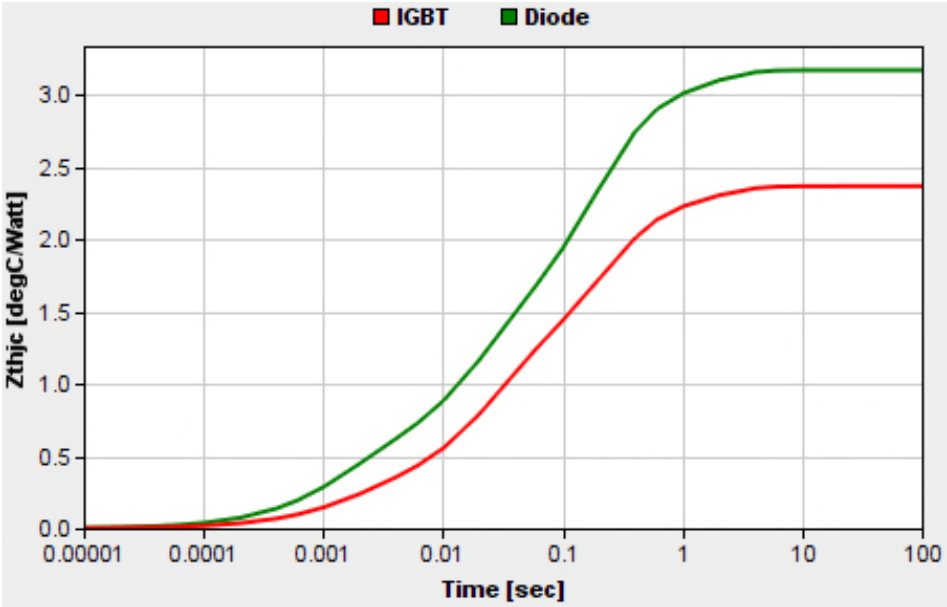


Figure 27 Thermal impedance curves (IFCM15P60GD, PFC part based on multi-chip heating)

8.5 Temperature rise considerations and calculation examples

The simulator CIPOSIM allows calculating power losses and temperature profiles for a constant case temperature. The result of loss calculation using the typical characteristics is shown in Figure 28 as "Effective current versus carrier frequency characteristics" (for V_{PN} = 400 V, V_{DD} = 15 V, $V_{CE(sat)}$ = typical, Switching losses = typical, T_J = 150°C, T_C = 100°C, $R_{th(j-c)}$ = max., MI = 0.8, PF = 0.8, 3-phase continuous PWM modulation, 60 Hz sine waveform output).

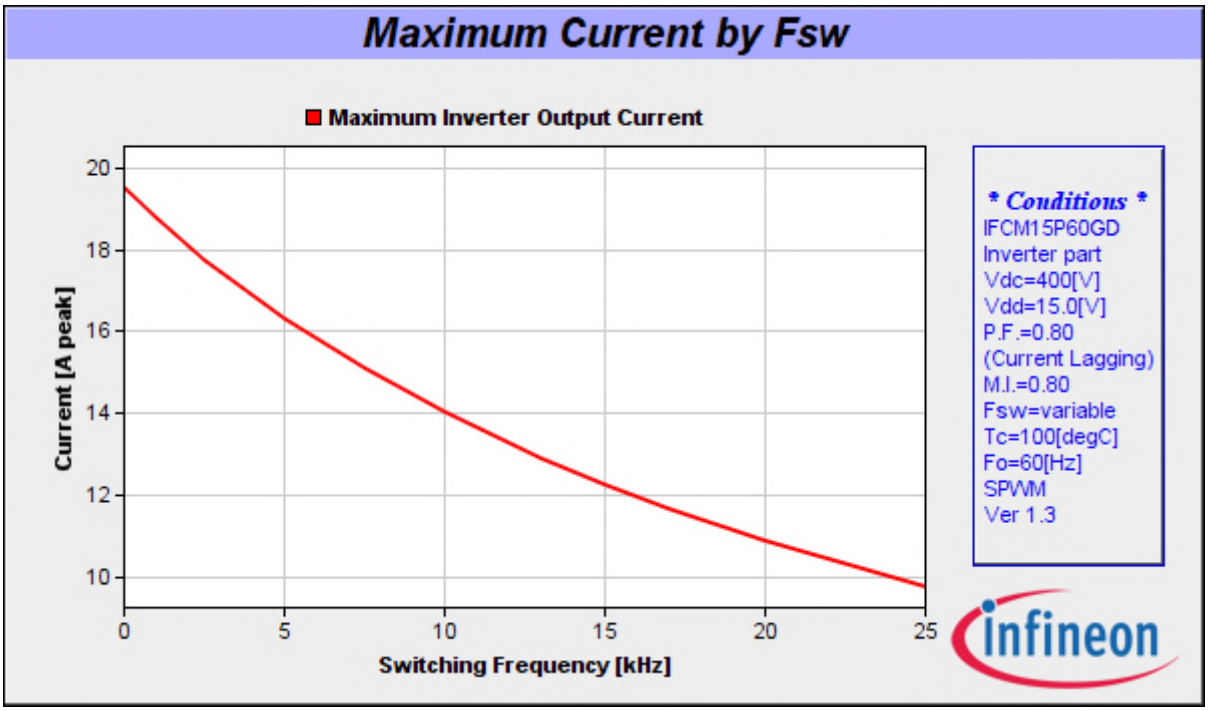


Figure 28 Effective current – carrier frequency characteristics of IFCM15P60GD [10]

CIPOSIM provides the power loss simulation of PFC section as well. Figure 29 shows "Maximum current (power) versus carrier frequency characteristics" (for V_{AC} = 220 V/60 Hz, V_{PN} = 400 V, V_{DD} = 15 V, R_g = 10 Ω, C_{ge} = 4.7 nF, $V_{CE(sat)}$ = typical, Switching losses = typical, T_J = 150°C, T_C = 100°C, $R_{th(j-c)}$ = max., CCM mode PFC, PF = 1.0). *CIPOSIM can be updated without any notice for improvement.

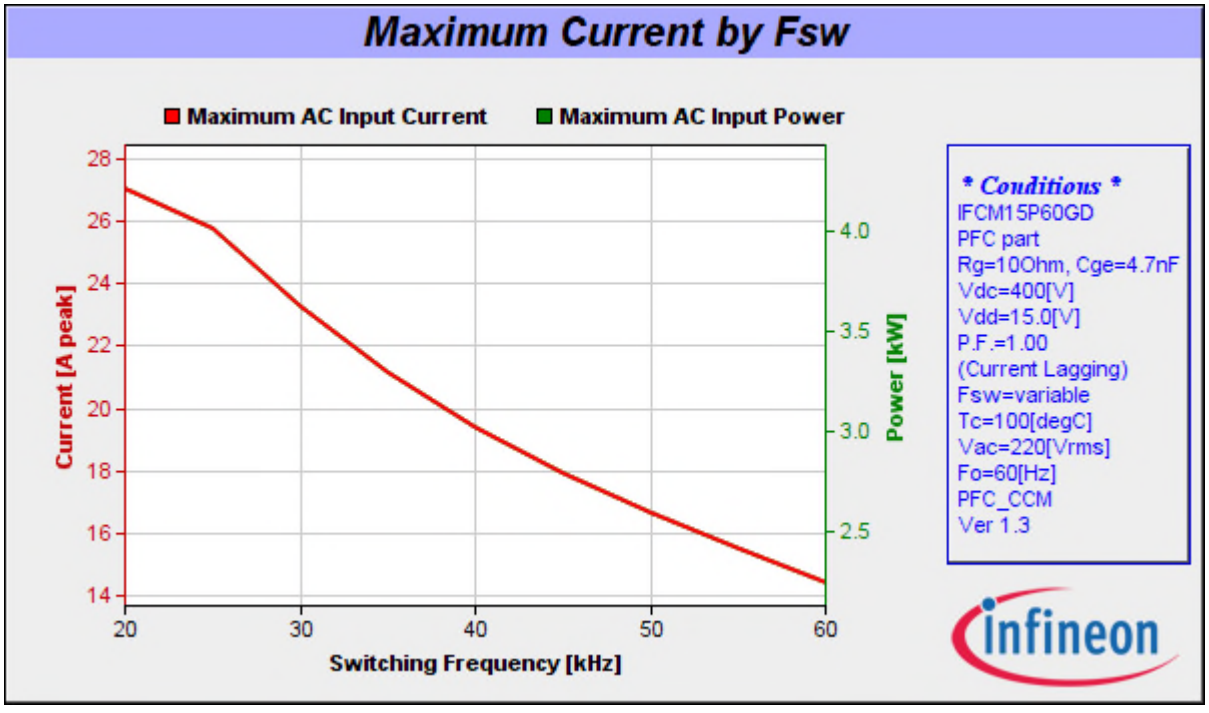


Figure 29 Effective power – carrier frequency characteristics of IFCM15P60GD [10]

Figure 28 and Figure 29 shows an example of an IPM operated under the condition of Tc = 100°C. It indicates the effective current which can be output when the junction temperature T_J rises to the maximum junction temperature of 150°C (up to which the CIPOS™ Mini operates safely). The CIPOSIM can be updated without any notice for improvement.

8.6 Heat sink selection guide

8.6.1 Required heat sink performance

If the power losses $P_{sw,i}$, $R_{th,J-C}$ and the maximum ambient temperature are known, the required thermal resistance of the heat sink and the thermal interface material can be calculated according to Figure 25 from,

$$T_{J,max} = T_{A,max} + \sum_i P_{sw,i} \cdot R_{th,HS-A} + \sum_i P_{sw,i} \cdot R_{th,C-HS} + Max(P_{sw,i} \cdot R_{th,JC,i}) \quad (18)$$

For three phase bridges one can simply assume that all power switches dissipate the same power and they all have the same $R_{th,J-C}$. This leads to the required thermal resistance from case to ambient.

$$R_{th,C-A} = R_{th,C-HS} + R_{th,HS-A} = \frac{T_{J,max} - P_{sw} \cdot R_{th,JC} - T_{A,max}}{\sum P_{sw}} \quad (19)$$

For example, the power switches of a washing machine drive dissipate 3.5W maximum each, the maximum ambient temperature is 50°C, the maximum junction temperature is 150°C and $R_{th,jC}$ is 3K/W. It results in,

$$R_{th,C-A} \le \frac{150°C - 3.5W \cdot 3\frac{K}{W} - 50°C}{6 \cdot 3.5W} = 4.3\frac{K}{W}$$

If the heat sink temperature shall be limited to 100°C, an even lower thermal resistance is required:

$$R_{th,C-A} \le \frac{100°C - 50°C}{6 \cdot 3.5W} = 2.4\frac{K}{W}$$

Smaller heat sinks with higher thermal resistances may be acceptable if the maximum power is only required for a short time (times below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heat sink the larger it's thermal capacitance the longer does it take to heat up the heat sink.

8.6.2 Heat sink characteristics

Heat sinks are characterized by three parameters:

- Heat transfer from the power source to heat sink
- Heat transfer within the heat sink (to all the surfaces of the heat sink)
- Heat transfer from heat sink surfaces to ambient

8.6.2.1 Heat transfer from heat source to heat sink

There are two factors which need to be considered in order to provide a good thermal contact between power source and heat sink:

- **Flatness of the contact area**
  - Due to the unevenness of surfaces, a thermal interface material needs to be applied between heat source and heat sink. However, such materials have a rather low thermal conductivity (<10 K/W).

Hence these materials should be as thin as possible. On the other hand, they need to fill out the space between heat source and heat sink. Therefore, the unevenness of the heat sink should be as low as possible. In addition, the particle size of the interface material must fit to the roughness of the module and the heat sink surfaces. Too large particle will unnecessarily increase the thickness of the interface layer and hence will increase the thermal resistance. Too small particles will not provide a good contact between the two surfaces and will lead to a higher thermal resistance as well.

- **Mounting pressure**
  - The higher the mounting pressure the better the interface material disperses and excessive interface material squeezes out resulting in a thinner interface layer with a lower thermal resistance.

8.6.2.2 Heat transfer within the heat sink

The heat transfer within the heat sink is mainly determined by:

- **Heat sink material**
  - The material needs to be a good thermal conductor. Most heat sinks are made of aluminum ($\lambda \approx 200$ W/(m*K)). Copper is heavier and more expensive but also nearly twice as efficient ($\lambda \approx 400$ W/(m*K)).
- **Fin thickness**
  - If the fins are too thin, the thermal resistance from heat source to fin is too high and the efficiency of the fin decreases. Hence it does not make sense to make the fins as thin as possible in order to have more fins and therefore to increase the surface area.

8.6.2.3 Heat transfer from heat sink surface to ambient

The heat transfers to the ambient mainly by convection. The corresponding thermal resistance is defined as

$$R_{th,conv} = \frac{1}{\alpha \cdot A} \qquad (20)$$

Where α is the heat transfer coefficient and A is the surface area.

Hence there are two important parameters:

- **Surface area:** Heat sinks require a huge surface area in order to easily transfer the heat to the ambient. However, as the heat source is assumed to be concentrated at a point and not uniformly distributed, the total thermal resistance of a heat sink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in section 8.6.2.2.
- **Heat transfer coefficient (aerodynamics):** This coefficient is strongly depending on the air flow velocity as shown in Figure 30. If there is no externally induced flow one speaks of natural convection, otherwise it's forced convection. Heat sinks with very small fin spacing do not allow a good air flow. If a fan is used, the fin gap may be lower than for natural convection as the fan forces the air through the space between the fins.

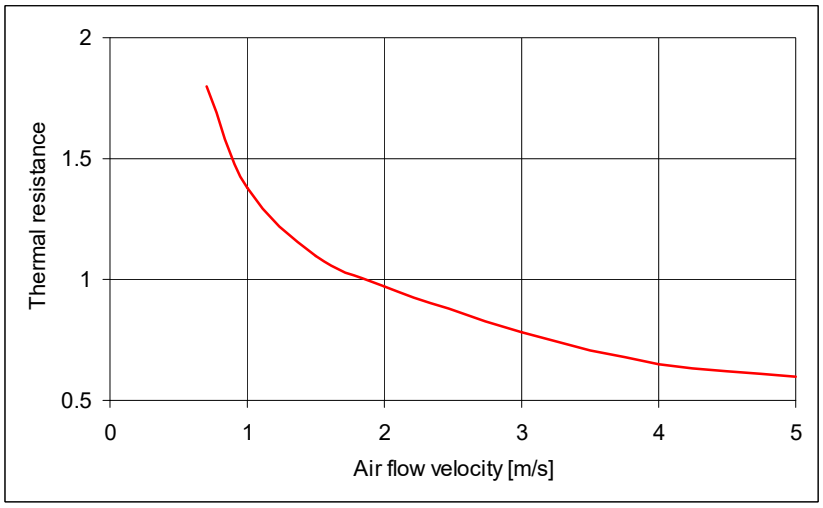


Figure 30 Thermal resistance as a function of the air flow velocity

Furthermore, in case of natural convection the heat sink efficiency depends on the temperature difference of heat sink and ambient (i.e. on the dissipated power). Some manufacturers, like Aavid thermalloy, provide a correction table which allows calculating the thermal resistance depending on the temperature difference. Figure 31 shows the heat sink efficiency degradation for natural convection as provided in [11]. Please note that the thermal resistance is 25% higher at 30 W than at 75 W.

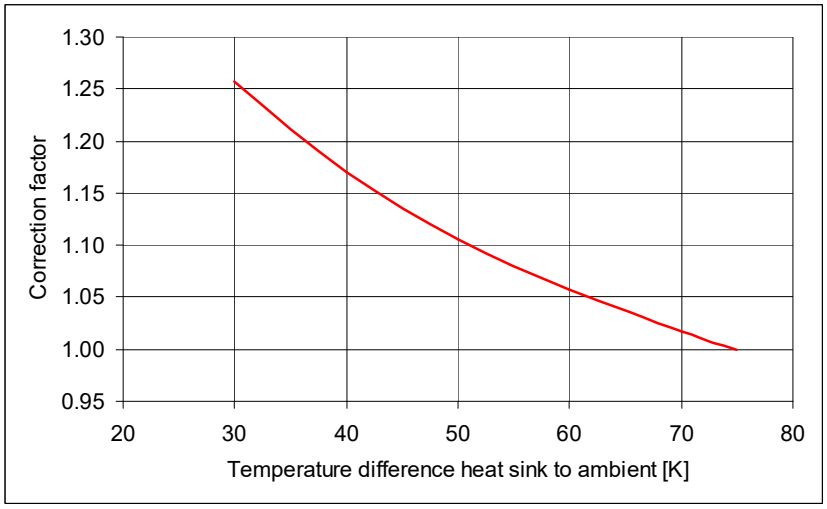


Figure 31 Correction factors for temperature

The positioning of the heat sink plays also an important role for the aerodynamics. In case of natural convection the best mounting attitude is with vertical fins as the heated air tends to move upwards due to buoyancy. Furthermore, one should make sure that there are no significant obstructions impeding the air flow.

Radiation occurs as well, supporting the heat transfer from heat sink to ambient. In order to the increase radiated heat one can use anodized heat sinks with a black surface. However, this decreases the thermal resistance of the heat sink only by a few percent in case of natural convection. Radiated heat is negligible in case of forced convection. Hence blank heat sinks can be used if there isn't a fan used with the heat sink.

The discussions in this section clearly show that there cannot be a single thermal resistance value assigned to a certain heat sink.

8.6.3 Selecting a heat sink

Unfortunately there are no straightforward recipes for selecting heat sinks. Finding a sufficient heat sink will include an iterative process of choosing and testing heat sinks. In order to get a first rough estimation of the required volume of the heat sink, one can start with estimated volumetric thermal resistances as given in Table 21 (Taken from [12]). This table gives only a first clue as the actual resistance may vary depending on many parameters like actual dimensions, type and orientation etc.

Table 21 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric Resistance [cm^3 °C/W]
Natural convection	500 ~ 800
1.0	150 ~ 250
2.5	80 ~ 150
5.0	50 ~ 80

One can roughly assume that the volume of a heat sink needs to be quadrupled in order to half it's thermal resistance. This gives a hint whether natural convection is sufficient for the available space or forced convection is required.

In order to get an optimized heat sink for a given application, one needs to contact heat sink manufacturers or consultants. Further hints and references can be found in [12].

When contacting heat sink manufacturers in order to find a suitable heat sink, please take care under which conditions the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heat sink. Also take care that the fin spacing is optimized for the corresponding airflow conditions.

9 Heat sink mounting and handling guidelines

9.1 Heat sink mounting

9.1.1 General guidelines

An adequate heat sinking capability of the CIPOS™ Mini is only achievable if it is suitably mounted. This is the fundamental requirement in order to meet the electrical and thermal performance of the module. The following general points should be observed when mounting CIPOS™ Mini on a heat sink. Verify the following points related to the heat sink:

a) There must be no burrs on aluminum or copper heat sinks.
b) Screw holes must be countersunk.
c) There must be no unevenness or scratches in the heat sink.
d) The surface of the module must be completely in contact with the heat sink.
e) There must be no oxidation nor stain or burrs on the heat sink surface.

To improve the thermal conductivity, apply silicone grease to the contact surface between the CIPOS™ Mini and heat sink. Spread a homogenous layer of silicone grease with a thickness of 100µm over the CIPOS™ Mini substrate surface. Non-planar surfaces of the heat sink may require a thicker layer of thermal grease. Please refer here to the specifications of the heat sink manufacturer. It is important to note here, that the heat sink covers the complete backside of the module. There may be different functional behavior, if there is a portion of the backside of the module, which is not in contact with the heat sink.

To prevent a loss of heat dissipation effect due to warping of the substrate, tighten down the mounting screws gradually and sequentially while maintaining a left/right balance in pressure applied.

It must be assured by design of the application PCB, that the plane of the back side of the module and the plane of the heat sink are parallel in order to achieve minimal tensions of the package and an optimal contact of the module with the heat sink. Please refer to the mechanical specifications of the module given in the datasheets.

It is basics of good engineering to verify the function and thermal conditions by means of detailed measurements. It is best to use a final application inverter system, which is assembled with the final production process. This helps to achieve high quality applications.

9.1.1.1 Recommended tightening torque

As shown in Table 22, the tightening torque of M3 screws is specified for minimum MS = 0.49 [N·m] and maximum MS = 0.78 [N·m]. The screw holes must be centered to the screw openings of the mold compound, so that the screws do not contact the mold compound. If an insulating sheet is used, use a sheet larger than the CIPOS™ Mini, and it should be aligned accurately when attached. It is important to ensure, that no air is enclosed by the insulating sheet. Generally speaking, insulating sheets are used in the following cases:

- When the ability of withstanding primary and secondary voltages is required, to achieve required safety standard against a hazardous situation.
- When the CIPOS™ Mini must be insulated from the heat sink.
- When measuring the module, to reduce radiated noise or eliminate other signal related problems.

Table 22 Mechanical characteristics and ratings

Item	Condition	Package type	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	DCB	0.49	-	0.78	[N·m]
Device flatness	(Note Figure 32)		-50	-	+100	[µm]
Heat sink flatness	(Note Figure 33)		-50	-	+100	[µm]
Weight		DCB	-	6.83	-	[g]

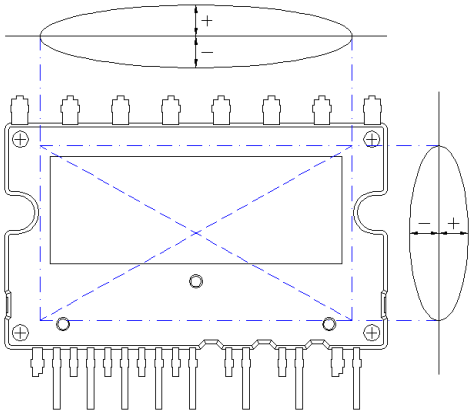


Figure 32 Device flatness measurement position

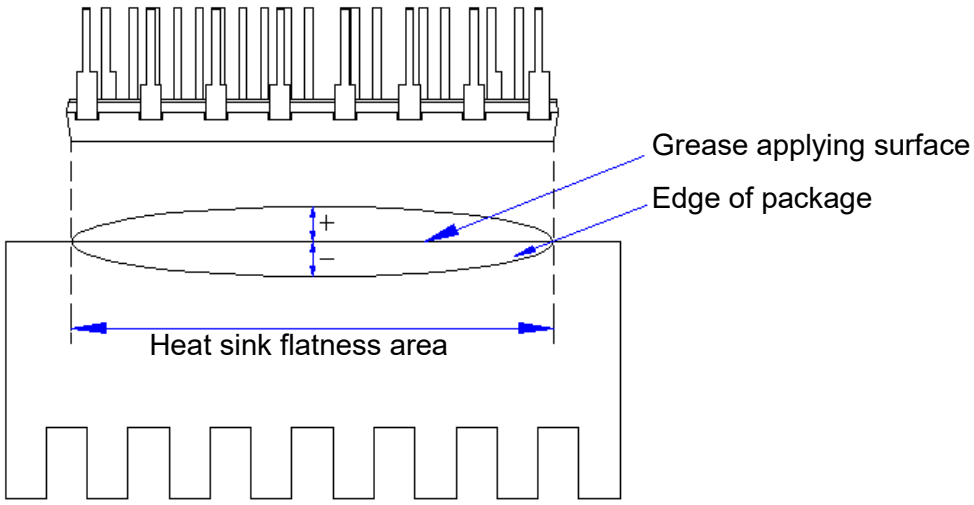


Figure 33 Heat sink flatness measurement position

9.1.1.2 Screw tightening to heat sink

The tightening of the screws is the main process of attaching the module to the heat sink. It is assumed that an interface pad is attached to the heat sink surface, which extends to the edge of the module and is located for the fixing holes. It is recommended that M3 fixing screws are used in conjunction with a spring washer and a plain washer. The spring washer must be assembled between the plain washer and the screw head. The screw torque must be monitored by the fixing tool.

Tightening Process:

- Align module with the fixing holes.
- Insert screw A with washers to touch only position (pre-screwing).
- Insert screw B with washers (pre-screwing).
- Tighten screw A to final torque.
- Tighten screw B to final torque.

Note: The pre-screwing torque is set to 20~30% of maximum torque rating.

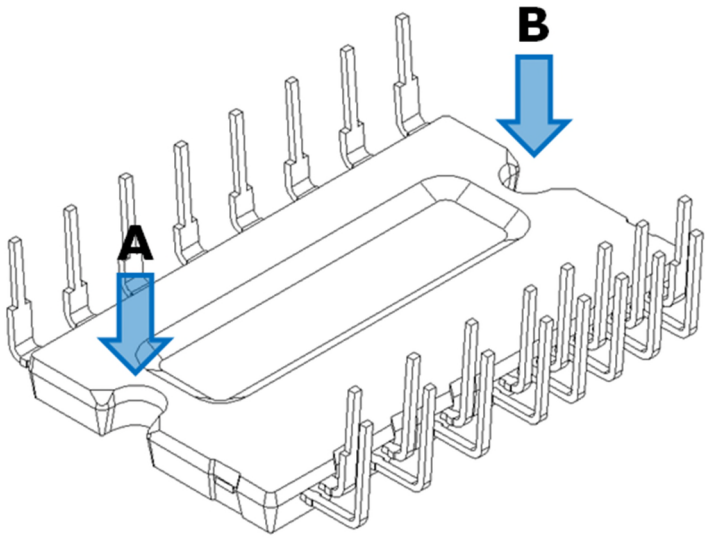


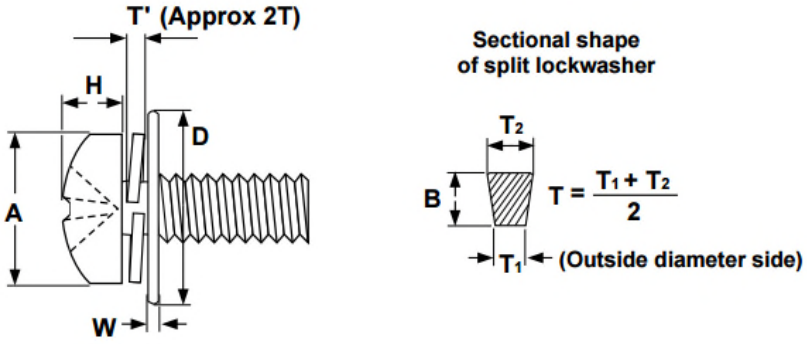
Figure 34 Reommended screw tightening order : Pre-screwing A → B, final screwing A → B

9.1.1.3 Mounting screw

When we attach module to heat sink, we recommend M3 SEMS screw (JIS B1256/JIS B1188) as Table 23.

Table 23 Recommended screw specification (Typical)

Screw dimensions				Flat washer		Spring washer	
Size	Thread pitch	A	H	D	W	D1	B x T
		Head diameter	Head height	Outer diameter	Thickness	Outside diameter	
M3	0.5	5.2	2.0	7.8	0.58	5	1.1 x 0.7



9.1.2 Recommended heat sink shape and system mechanical structure

A shock or vibration through PCB or heat sink might cause the crack of the package mounted on the heat sink. To avoid a broken or cracked package and to endure shock or vibration through PCB or heat sink, a heat sink shape is recommended as shown in Figure 35. The heat sink needs to be fixed to the PCB with screws or eyelets. In mass production stage, the process sequence for system assembly in terms of device soldering on PCB, heat sink mounting and casing etc., should be taken into account to avoid mechanical stress on the device pins, package mold compound, heat sink and system enclosure etc.

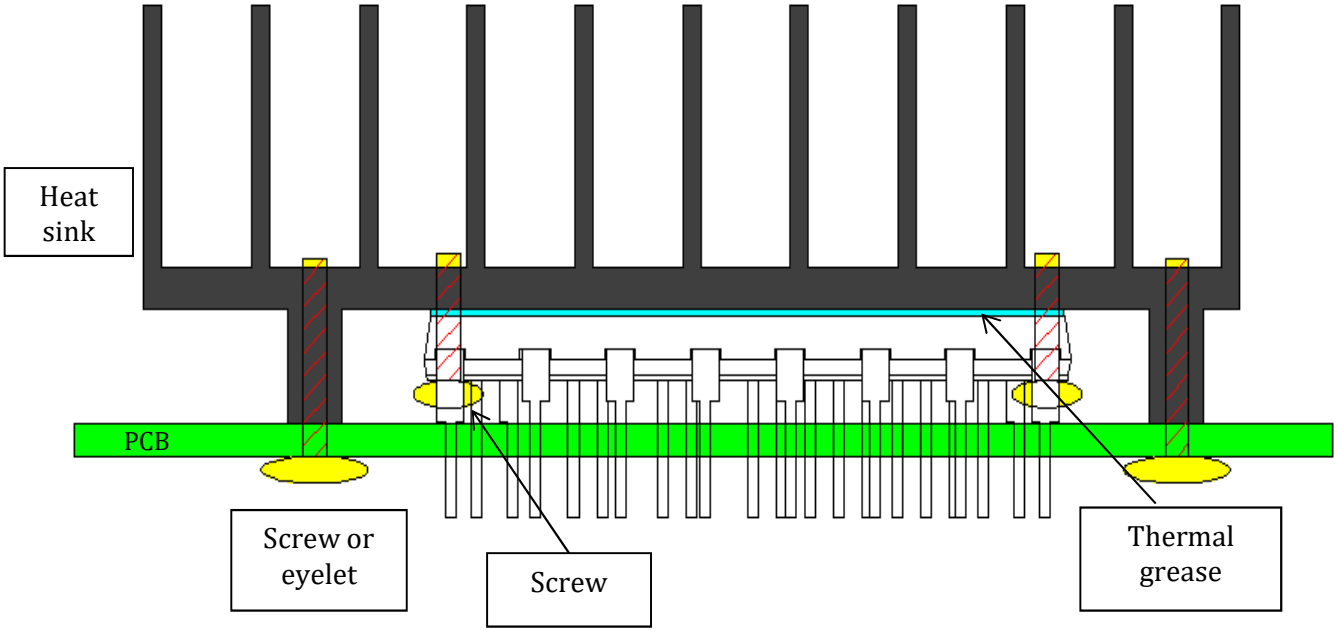


Figure 35 Recommended heat sink shape

9.2 Handling guide line

When installing a module to a heat sink, excessive uneven tightening force might apply stress to inside chips, which will lead to a broken or degradation of the device. An example of recommended fastening order is shown in Figure 34.

- Do not over torque when mounting the screws. Excessive mounting torque may cause damage to module hole as well as damage to the screw and heat sink.
- Avoid one-side tightening stress. Uneven mounting can cause the module hole to be damaged.

To get effective heat dissipation, it is necessary to enlarge the contact area as much as possible, which minimizes the contact thermal resistance.

Properly apply thermal conductive grease over the contact surface between the module and the heat sink, which is also useful for preventing the contact surface from corrosion. Furthermore the grease should be of stable quality and long term endurance within wide operating temperature range. Use a torque wrench to tighten to the specified torque rating. Exceeding the maximum torque limitation might cause a module to be damaged or degraded. Pay attention not to have any dirt remaining on the contact surface between the module and the heat sink. All equipment, which is used to handle or mount CIPOS™ Mini must comply with the relevant ESD standards. This includes e.g. transportation, storage and assembly. The module itself is an ESD sensitive device. It may therefore be damaged in case of ESD shocks.

Don’t shake and handle by grabbing only the heat sink, and especially don’t stress the PCB by grabbing only the heat sink. That might cause package cracking or a broken package.

9.3 Storage guideline

9.3.1 Recommended storage conditions

Temperature: 5 ~ 35°C

Relative humidity: 45 ~ 75%

- Avoid leaving the CIPOS™ Mini family exposed to moisture or direct sunlight. Especially, be careful during periods of rain or snow.
- Use storage areas where there is minimal temperature fluctuation.

Rapid temperature changes can cause moisture condensation on the stored CIPOS™ Mini, resulting in lead oxidation or corrosion as a result, and leading to degraded solderability.

- Do not allow the CIPOS™ Mini family to be exposed to corrosive gasses or dusty conditions.
- Do not allow excessive external forces or loads to be applied to the CIPOS™ Mini family while they are in storage.

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Revision History

Major changes since the last revision

Page or Reference	Description of change
V 1.0	Initial release
V 1.1	Removed products which are without NTC thermistor, corrected unit in Figure 15 (65ms → 65µs), added equation (3),(4) in section 5.2.3
V 1.2	Corrected unit in Figure 15 “5ms → 5us”
V 1.3	Updated Table 23

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