Control Integrated POwer System (CIPOS™)
Inverter IPM Reference Board Type 1 for 1-Shunt Resistor

About this document

Scope and Purpose

The scope of this application note is to describe the product reference board of the CIPOS™ Mini inverter IPM and the basic requirements for operating the product in a recommended mode. Environmental conditions were considered in the design of the reference board. The design was tested as described in this document but not qualified regarding safety requirements or manufacturing and operation over the whole operating temperature range or lifetime. The boards provided by Infineon are subject to functional testing only.

Reference boards are not subject to the same procedures as regular products regarding Returned Material Analysis (RMA), Process Change notification (PCN) and Product Discontinuation (PD). Reference boards are intended to be used under laboratory conditions by specialists only.

Intended Audience

Power electronics engineers who want to evaluate the CIPOS™ Mini inverter IPM.

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Introduction

1 Introduction

This reference board is composed of the IGCM10F60GA, minimum peripheral components and single current sensing resistor. It is designed for customers to evaluate the performance of the CIPOS™ Mini inverter IPM with simple connections of control signals and power wires. Figure 1 shows the external view of the reference board.

This application note also describes how to design key parameters and PCB layout.

Figure 1  Reference board pictures

Figure 2  Application example
2 Schematic

Figure 3 shows a circuitry of the reference board.

The reference board consists of interface circuit, bootstrap circuit, snubber capacitor, Short Circuit (SC) protection circuit, fault output circuit, current sensing resistor and passive parts etc.

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**Figure 3** Circuit of the reference board

*Note:* The "Vct" on the J1 pin 9 denotes the control signal supply voltage such as 5V or 3.3V.

*Note:* It is optional to use external bootstrap circuit together with the internal one as shown in the dotted line, in case that a smaller bootstrap resistor is necessary.
3 External Connection

3.1 Signal Connector

Table 1 Pin description of the signal connector (J1 HEADER 11, 11-pin, 2.5mm pin pitch)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HIN(U)</td>
<td>Control signal input for phase U upper side IGBT</td>
</tr>
<tr>
<td>2</td>
<td>HIN(V)</td>
<td>Control signal input for phase V upper side IGBT</td>
</tr>
<tr>
<td>3</td>
<td>HIN(W)</td>
<td>Control signal input for phase W upper side IGBT</td>
</tr>
<tr>
<td>4</td>
<td>LIN(U)</td>
<td>Control signal input for phase U lower side IGBT</td>
</tr>
<tr>
<td>5</td>
<td>LIN(V)</td>
<td>Control signal input for phase V lower side IGBT</td>
</tr>
<tr>
<td>6</td>
<td>LIN(W)</td>
<td>Control signal input for phase W lower side IGBT</td>
</tr>
<tr>
<td>7</td>
<td>/Fo</td>
<td>Fault output signal /Temperature monitor (Optional)</td>
</tr>
<tr>
<td>8</td>
<td>Vsh</td>
<td>Sensing signal for voltage of current sensing resistor</td>
</tr>
<tr>
<td>9</td>
<td>Vctr</td>
<td>External 5V or 3.3V supply for control signal</td>
</tr>
<tr>
<td>10</td>
<td>VDD</td>
<td>External 15V supply for module</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

3.2 Power Terminals

Table 2 Pin description of power terminals

<table>
<thead>
<tr>
<th>Terminal Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td>Output node of U phase</td>
</tr>
<tr>
<td>V</td>
<td>Output node of V phase</td>
</tr>
<tr>
<td>W</td>
<td>Output node of W phase</td>
</tr>
<tr>
<td>P</td>
<td>Positive node of DC link voltage</td>
</tr>
<tr>
<td>N</td>
<td>Negative node of DC link voltage</td>
</tr>
</tbody>
</table>
Control Integrated POwer System (CIPOS™)
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Key Parameters Setting

4 Key Parameters Setting

4.1 Circuit of Input Signals (LIN(X), HIN(X))

The input signals are compatible with either TTL or CMOS levels. The logic level can go down to 3.3V. The maximum input voltage of the input signal pin is clamped to 10.5V by the internal Zener diode. However the recommended voltage range of input voltage is up to 5V. The input signals LIN(X) and HIN(X) are active high.

These pins have an internal pull-down structure with a pull-down resistor, which is nominal 5kΩ. The input noise filter inside the CIPOS™ Mini inverter IPM suppresses short pulses and prevents a false IGBT driving from an unintentional operation. The input noise filter time (t_{FLIN}) is typically 270ns. This means that the input signal must stay on more than 270ns so that the driver IC detects the normal PWM input for a correct IGBT driving. CIPOS™ Mini inverter IPM can be connected directly to the controller without an external input RC filter due to the internal pull down resistor and input noise filter, as shown in Figure 4.

![Internal pull-down resistor and input noise filter on input signal pin](image)

**Figure 4** Internal pull-down resistor and input noise filter on input signal pin

4.2 Bootstrap Capacitor

Bootstrapping is a common method for charge pumping from a low potential to a higher one. With this technique a supply voltage can be easily established for a floating high side section of the gate driver. Figure 5 below shows a simple bootstrap circuit diagram. It represents only one-phase effective circuit from a three-phase half bridge inverter. The bootstrap functionality is implemented internally to limit current. Please refer to the datasheet and application note for the bootstrapping method in detail.

![Bootstrap circuit for the supply of the high side gate drive](image)

**Figure 5** Bootstrap circuit for the supply of the high side gate drive
Key Parameters Setting

A low leakage current of the high side section is very important in order to keep the bootstrap capacitor small. The bootstrap capacitor \( C_{BS} \) is discharged mainly by the following mechanisms:

- Quiescent current to the high side circuit in IC
- Gate charge for turning high side IGBT on
- Level-shift charge required by level shifters in IC
- Bootstrap capacitor leakage current (can be ignored for a non-electrolytic capacitor)
- Bootstrap diode leakage current
- Bootstrap diode reverse recovery charge

The calculation of the bootstrap capacitor results in the following equation.

\[
C_{BS} = \frac{I_{\text{leak}} \times t_p}{\Delta V_{BS}}
\]

Where,

- \( C_{BS} \): bootstrap capacitor value
- \( I_{\text{leak}} \): maximum discharge current of the \( C_{BS} \)
- \( t_p \): maximum on pulse width of the high side IGBT
- \( \Delta V_{BS} \): voltage drop at the bootstrap capacitor within a switching period

A practical leakage current level \( I_{\text{leak}} \) of the CIPOS™ Mini inverter IPM is max. 1mA for 1 cycle turn on of the HS IGBT.

Figure 6 shows the curve corresponding to the \( C_{BS} \) equation above for a continuous sinusoidal modulation when the voltage ripple \( \Delta V_{BS} \) is 0.1V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range up to 4.7\( \mu \)F for 2~20kHz switching frequencies. In other PWM method case like a discontinuous sinusoidal modulation, the \( t_p \) must be set to the longest period of the low side IGBT off.

![Figure 6](image_url)
### Key Parameters Setting

#### 4.3 Internal Bootstrap Circuit Characteristics

CIPOS™ Mini inverter IPM includes three bootstrap circuits in the internal drive IC, which consist of three diodes and three resistors, as shown in Figure 5. A typical value of the internal bootstrap resistor is 40Ω. For more information, please refer to the below Table 3. Note that R_{BS2} and R_{BS3} have the same value with the R_{BS1}.

<table>
<thead>
<tr>
<th>Description</th>
<th>Condition</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Repetitive peak reverse voltage</td>
<td>V_{RRM}</td>
<td>600</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
| Bootstrap resistance of U-phase | &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &nbsp; &n...
Key Parameters Setting

4.4.1 Current Sensing Resistor Selection

The value of the current sensing resistor can be calculated with the following equation.

\[ R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \]

Where,

- \( R_{SH} \): current sensing resistor value
- \( V_{IT,TH+} \): ITRIP positive going threshold voltage, typ. 0.47V
- \( I_{OC} \): over current level

A maximum value of the OC protection level should be set less than the maximum peak output current in the datasheet absolute maximum ratings while taking into consideration the tolerance of the current sensing resistor.

For example, the maximum peak output current of the IGCM10F60GA is 20A_{peak},

\[ R_{SH(min)} = \frac{0.47}{20} = 0.024\Omega \]

So the recommended value of the current sensing resistor should be higher than 24m\( \Omega \) for IGCM10F60GA.

In order to calculate the power rating of the current sensing resistor, the below items has to be taken into account.

- Maximum load current of the inverter module (I_{RMS})
- Current sensing resistor value at Tc=25°C (R_{SH})
- Power derating ratio of the current sensing resistor at T_{SH}=100°C
- Safety margin

And the power rating can be calculated with the equation below.

\[ P_{SH} = \frac{I_{RMS}^2 \times R_{SH} \times \text{Safety margin}}{\text{Derating ratio}} \]

For example, in case of IGCM10F60GA and R_{SH}=24m\( \Omega \)

- Max. load current of the inverter module (I_{RMS}) : 6A_{RMS}
- Current sensing resistor value at Tc=25°C (R_{SH}) : 0.024\( \Omega \)
- Power derating ratio of the current sensing resistor at T_{SH}=100°C : 80%
- Safety margin : 30%

\[ P_{SH} = \frac{6A^2 \times 0.024\Omega \times 130\%}{80\%} = 1.4W \]

So the proper power rating of the current sensing resistor is recommended as more than 1.4W.

Based on the equation, condition and calculation method above, some example values of minimum current sensing resistance and required resistor power rating are introduced as shown in below Table 4 for CIPOS™ Mini inverter module products. When choosing a proper current sensing resistance and its power rating, an accurate OC protection level in the application setting should be taken into account for a correct over current detection.

Table 4 Maximum peak current, shunt resistor value and required power rating
4.4.2 Delay Time

An RC filter should be necessary in the OC sensing circuit to prevent a false OC protection caused by noise interference. The time constant of the RC filter should be determined while considering the noise period and the IGBT withstand time against the OC event. When the current flows through the current sensing resistor, the induced voltage drop on the current sensing resistor is supplied to the ITRIP pin of the CIPOS™ Mini inverter IPM through the RC filter. While the ITRIP pin voltage is rising to the ITRIP positive threshold voltage (typ. 0.47V), the filter delay time (t\text{\text{filter}}) is created by the RC filter time constant. In addition there is a shutdown propagation delay on ITRIP (t\text{\text{TRIP}}) as shown in the Table 5 below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shut down propagation delay (t\text{\text{TRIP}})</td>
<td>I\text{\text{out}} = 20A, from V\text{\text{IT,TH+}} to 10% I\text{\text{out}}</td>
<td>-</td>
<td>1420</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>I\text{\text{out}} = 15A, from V\text{\text{IT,TH+}} to 10% I\text{\text{out}}</td>
<td>-</td>
<td>1540</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I\text{\text{out}} = 10A, from V\text{\text{IT,TH+}} to 10% I\text{\text{out}}</td>
<td>-</td>
<td>1340</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I\text{\text{out}} = 6A, from V\text{\text{IT,TH+}} to 10% I\text{\text{out}}</td>
<td>-</td>
<td>1260</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I\text{\text{out}} = 4A, from V\text{\text{IT,TH+}} to 10% I\text{\text{out}}</td>
<td>-</td>
<td>1300</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I\text{\text{out}} = 2.5A, from V\text{\text{IT,TH+}} to 10% I\text{\text{out}}</td>
<td>-</td>
<td>1320</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

Therefore, the total delay time from occurrence of the OC event to the shutdown of the IGBT gate becomes:

\[ t\text{\text{\text{total}}} = t\text{\text{\text{\text{filter}}} + t\text{\text{\text{TRIP}}}} \]

The shutdown propagation delay is in inverse proportion to the current range. Therefore the t\text{\text{\text{TRIP}} will be shorter with a higher current condition, comparing to the current condition in the Table 5. The total delay must be less than 5\mu{s of the short circuit withstand time (t\text{\text{s}}} which is specified in the datasheet. Thus, the RC time constant should be set in the range of 1~2\mu{s. A recommended RC filter values are 1.8k\Omega R10 and 1nF C17.

4.5 Temperature Monitor and Thermal Protection

In case of the CIPOS™ Mini inverter IPM, a built-in thermistor (85k\Omega at 25°C) is connected between VFO and VSS pins. The typical application circuit looks like Figure 8 where the VFO pin is used for both thermistor temperature sensing and fault flag. The voltage of the VFO pin decreases as the thermistor temperature increases because the thermistor is a NTC (Negative Temperature Coefficient) type and it is connected to the external pull-up resistor. Note that the voltage variation of the VFO pin, which is generated by the thermistor temperature change, should be always higher than the fault detection level of the micro controller. In this reference board, the pull-up resistor is set to 3.6k\Omega so that the VFO voltage becomes 2.95V and 1.95V respectively for 5V and 3.3V control voltage (V\text{\text{ct}}) when the thermistor temperature is 100°C, as shown in Figure 9.
Control Integrated P0wer System (CIPOS™)
Inverter IPM Reference Board Type 1 for 1-Shunt Resistor

Key Parameters Setting

![Diagram of CIPOS™ IxFMxxF60GA with Drive IC, Micro Controller, Input to AD Converter, and Input to Fault Detection]

**Figure 8** Temperature monitor with built in thermistor and pull up resistor

![Graph showing voltage variation of the VFO along with the NTC thermistor temperature change]

**Figure 9** Voltage variation of the VFO along with the NTC thermistor temperature change

OT set 100 °C: 1.95V at Vctr=3.3V
OT set 100 °C: 2.95V at Vctr=5V
# Control Integrated P0wer System (CIPOS™)
## Inverter IPM Reference Board Type 1 for 1-Shunt Resistor

### Part List

#### Table 6

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Components</th>
<th>Description</th>
<th>Supplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1 ~ R6</td>
<td>100Ω, 1/8W, 5%</td>
<td>Series resistors for input voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>R7 ~ R9</td>
<td>No Connection</td>
<td>See note below</td>
<td>-</td>
</tr>
<tr>
<td>R10</td>
<td>1.8kΩ, 1/8W, 1%</td>
<td>Series resistor for current sensing voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>R11</td>
<td>3.6kΩ, 1/8W, 1%</td>
<td>Pull-up resistor for fault output voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>R12</td>
<td>1kΩ, 1/8W, 5%</td>
<td>Series resistor for fault output voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>R13</td>
<td>Content 4.4.1</td>
<td>Current sensing resistor</td>
<td>Vishay</td>
</tr>
<tr>
<td>C1 ~ C6</td>
<td>1nF, 25V</td>
<td>Bypass capacitors for input voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>C7 ~ C9</td>
<td>0.1uF, 25V</td>
<td>Bypass capacitors for high side bias voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>C10 ~ C12</td>
<td>22uF, 35V</td>
<td>Bootstrap capacitors</td>
<td>Samyoung</td>
</tr>
<tr>
<td>C13</td>
<td>100uF, 35V</td>
<td>Source capacitor for 5 or 3.3V supply voltage</td>
<td>Samyoung</td>
</tr>
<tr>
<td>C14</td>
<td>0.1uF, 35V</td>
<td>Bypass capacitor for 5 or 3.3V supply voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>C15</td>
<td>220uF, 35V</td>
<td>Source capacitor for VDD supply voltage</td>
<td>Samyoung</td>
</tr>
<tr>
<td>C16</td>
<td>0.1uF, 35V</td>
<td>Bypass capacitor for VDD supply voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>C17</td>
<td>1nF, 25V</td>
<td>Bypass capacitor for current sensing voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>C18</td>
<td>1nF, 16V</td>
<td>Bypass capacitor for fault output voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>C19</td>
<td>1nF, 16V</td>
<td>Bypass capacitor for fault output voltage</td>
<td>Walsin</td>
</tr>
<tr>
<td>C20</td>
<td>0.1uF, 630V</td>
<td>Snubber capacitor</td>
<td>Pilkor</td>
</tr>
<tr>
<td>D1 ~ D3</td>
<td>No Connection</td>
<td>See note below</td>
<td>-</td>
</tr>
<tr>
<td>J1</td>
<td>SMW250-11P</td>
<td>Signal &amp; Power supply connector</td>
<td>Yeonho</td>
</tr>
<tr>
<td>U, V, W, P, N</td>
<td>Fasten Tap</td>
<td>Power terminals</td>
<td>KET</td>
</tr>
</tbody>
</table>

**Note:** It is optional to use external bootstrap circuit together with internal one, in case that smaller bootstrap resistor is necessary.
6 PCB Design Guide

In general, there are several issues to be considered when designing a switching power supply application.

- Low stray inductive connection
- Isolation distance
- Component placement

This chapter will explain about the items above and come up with the solutions for the better layout design.

6.1 Layout of Reference Board

![Top view](image1)

![Bottom view](image2)

**Figure 10** Layout of reference board type 1 for 1-shunt resistor

1. The connection between emitters of CIPOS™ Mini inverter IPM (N) and current sensing resistor should be as short and as wide as possible.
2. It is recommended that the ground pin of the micro-controller should be directly connected to the VSS pin. Signal ground and power ground should be as short as possible and connected at only one point via the VDD capacitor (C16).
3. All of the bypass capacitors should be placed as close to the pins of CIPOS™ Mini inverter IPM as possible.
4. The capacitor (C17) for voltage sensing of the current sensing resistor should be placed as close to ITRIP and VSS pins as possible.
5. In order to accurately detect the voltage of the current sensing resistor, both sensing and ground patterns should be connected at the pins of the current sensing resistor and should not be overlapped with any patterns for the load current, as shown in Figure 10.
PCB Design Guide

6. The snubber capacitor (C20) should be placed as close to the power terminals as possible.

7. The PCB routings for power pins such as P, U, V, W and N should be placed on both top and bottom layers with vias to allow high current flowing. They have to keep the minimum isolation distance among the power patterns. The distance should be at least over than 2.54mm.

8. Note that there are milling profiles in blue lines on the board to keep the isolation distance.

9. All components except the CIPOS™ Mini inverter IPM are placed on the top layer.
7 Reference

[1] Infineon Power Semitech: CIPOS™ Mini IGCM10F60GA; Datasheet Ver. 1.6; Infineon Power Semitech, 2014

Revision History

Major changes since the last revision

<table>
<thead>
<tr>
<th>Page or Reference</th>
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