Control integrated power system (CIPOS™)

CIPOS™ Mini interleaved PFC IPM technical description

About this document

Scope and Purpose

The scope of this application note is to describe the product family of CIPOS™ Mini interleaved power factor correction (PFC) intelligent power module (IPM) and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as IGBT or gate drive IC, as well as to the design of the necessary external circuitry, such as interfacing.

Intended audience

Power electronics engineers who want to design reliable and efficient CIPOS™ Mini interleaved PFC IPM applications.

Table of Contents

Table of Contents

1 Scope

The scope of this application note is to describe the product family of CIPOS™ Mini interleaved PFC IPM and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as IGBT or gate drive IC, as well as to the design of the necessary external circuitry, such as interfacing. Integrating power semiconductors and drivers into one package allows them to reduce the time and effort spent on design. To meet the strong demand for small size and higher power density, Infineon has developed a new family of highly integrated interleaved PFC IPMs that contain nearly the entire semiconductor components required to drive interleaved PFC applications. They incorporate two or three phase interleaved PFC power stage with a silicon-on-insulator (SOI) gate driver and Infineon's leading-edge TRENCHSTOP™ 5 IGBT & rapid switching emitter-controlled diode for IFCMxxT65zu & IFCMxxU65zu.

The application note concerns the following products.

IFCM20T65GD

IFCM20U65GD

IFCM30T65GD

IFCM30U65GD

Note: IvCMxxy65zu
v = F(PFC IGBT+Diode)
xx = nominal current
y = topology(T, U)
z = G(Temp., Itrip, Fault)
u = D(DCB)

CIPOS™ Mini interleaved PFC IPM is a family of intelligent power modules which are designed for PFC circuit in household appliances, such as air conditioners applications.

1.1 Product line-up

Table 1 Line-up of CIPOS™ Mini interleaved PFC IPM

Part Number	Rating		PFC circuit	Package	Isolation voltage	Main applications
	Current [A]	Voltage [V]				
IFCM30U65GD	30	650	3-phase interleaved	Molded DIL module with DCB	2000 V_{rms} sinusoidal, 1min.	Home appliance applications such as air conditioner
IFCM30T65GD			2-phase interleaved			
IFCM20U65GD	20		3-phase interleaved			
IFCM20T65GD			2-phase interleaved			

1.2 Nomenclature

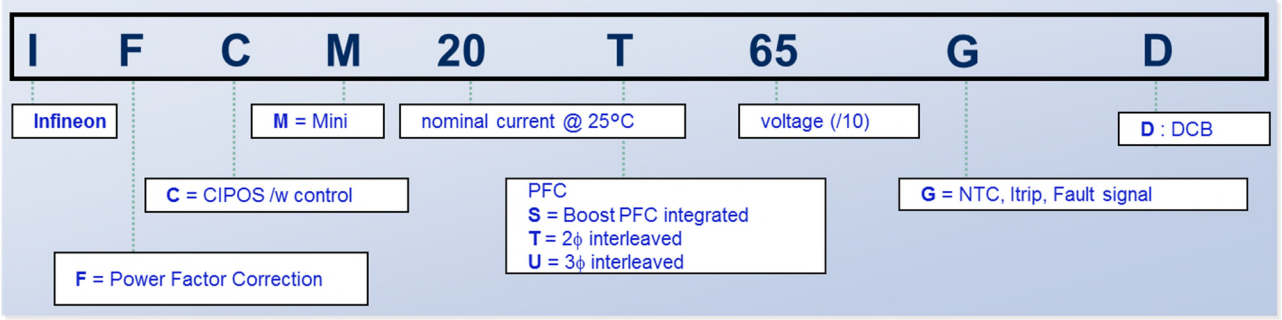


Figure 1 CIPOS™ Mini interleaved PFC IPM product nomenclature

2 Internal components and package technology

2.1 Power transistor technology – 650V TRENCHSTOP™ 5 IGBT

Infineon's 650 V TRENCHSTOP™ 5 IGBT technology redefines "best-in-class" IGBT by providing unmatched performance in terms of efficiency for hard switching applications. When high efficiency, lower system costs and increased reliability are demanded, TRENCHSTOP™ 5 is the only option. TRENCHSTOP™ 5 IGBTs deliver a dramatic reduction in switching and conduction losses [1].

2.2 Power diode technology – rapid emitter-controlled diode

The rapid diode of Infineon is optimized to operate with 650 V TRENCHSTOP™ 5 IGBT as a boost diode in PFC topology when the switching frequency is less than 40 kHz because conduction losses dominate switching losses at lower switching frequency operation. Rapid diode advancement in thin wafer technology helps to maintain a stable V_F over temperature. The rapid diode combines low V_F for lower conduction losses and low I_{rr} to reduce Eon of the TRENCHSTOP™ 5 IGBT. Increased efficiency, with the additional benefit of having a 650 V breakthrough voltage can be achieved [2].

2.3 Control IC – 3 channel gate driver IC

The basic feature of this technology is the separation of the active silicon from the base material by means of a buried silicon oxide layer. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices. This also prevents the latch-up effect even in case of high dv/dt switching under elevated temperature and hence provides improved robustness. Besides the thin-film SOI technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays [3]. A monolithic single control IC for all IGBTs provides further advantages, such as matched propagation delay times and all IGBTs turn-off under fault situations like undervoltage lockout (UVLO) or overcurrent.

2.4 Thermistor

In CIPOS™ Mini interleaved PFC IPM, the thermistor is integrated on the internal PCB. It is connected between NTC and V_{SS} pins. A circuit proposal using the thermistor for over temperature protection is discussed in Section 5.4.

Table 2 Raw data of the thermistor used in CIPOS™ Mini interleaved PFC IPM

T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]	T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]
-40	2662.292	2962.540	3262.789	10.1	45	34.520	36.508	38.496	5.4
-35	1925.308	2133.692	2342.076	9.8	50	28.400	29.972	31.545	5.2
-30	1407.191	1553.414	1699.637	9.4	55	23.485	24.735	25.985	5.1
-25	1038.949	1142.63	1246.312	9.1	60	19.517	20.515	21.514	4.9
-20	774.497	848.747	922.997	8.7	65	16.296	17.097	17.898	4.7
-15	582.690	636.369	690.048	8.4	70	13.670	14.315	14.960	4.5
-10	442.252	481.410	520.568	8.1	75	11.517	12.039	12.561	4.3
-5	338.491	367.303	396.114	7.8	80	9.745	10.169	10.593	4.2
0	261.164	282.537	303.910	7.6	85	8.279	8.625	8.971	4.0
5	203.056	219.036	235.016	7.3	90	7.062	7.345	7.628	3.9
10	159.044	171.081	183.118	7.0	95	6.046	6.279	6.511	3.7

15	125.454	134.586	143.717	6.8	100	5.199	5.388	5.576	3.5
20	99.630	106.605	113.580	6.5	105	4.468	4.640	4.811	3.7
25	79.638	85.000	90.362	6.3	110	3.856	4.009	4.163	3.8
30	64.055	68.203	72.352	6.1	115	3.338	3.477	3.615	4.0
35	51.831	55.059	58.287	5.9	120	2.900	3.024	3.149	4.1
40	42.182	44.708	47.235	5.7	125	2.527	2.639	2.751	4.2

2.5 Package technology

The CIPOS™ Mini interleaved PFC IPM offers the smallest size while providing high power density up to 650 V, 30 A by employing TRENCHSTOP™ 5 IGBT and rapid diode with 3 channel gate drive IC. It contains all the power components such as the IGBTs and isolates them from each other and from the heat sink. All low power components such as the gate drive IC and thermistor are assembled on a PCB.

The electric insulation is given by the mold compound and DCB, which are simultaneously the thermal contact to the heat sink. In order to further decrease the thermal impedance, the internal lead frame design is optimized [4]. Figure 2 shows the external view of CIPOS™ Mini interleaved PFC IPM package.

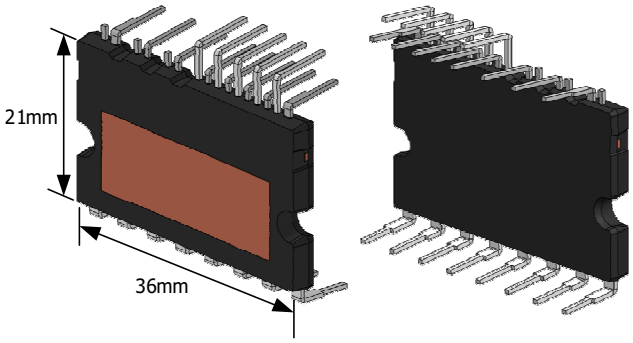
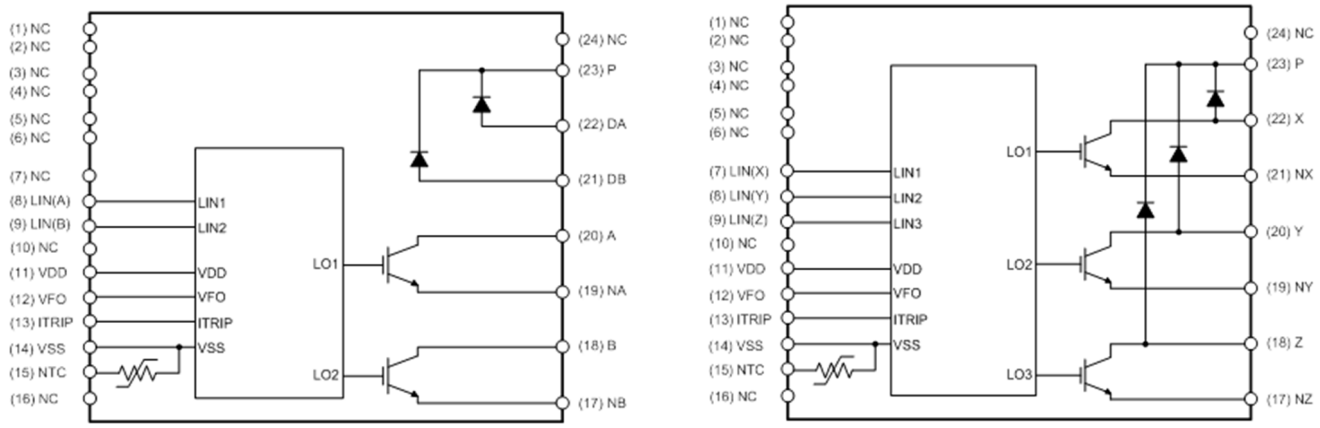


Figure 2 External view of CIPOS™ Mini interleaved PFC IPM

3 Product overview

3.1 Internal circuit and features

Figure 3 illustrates the internal block diagram of the CIPOS™ Mini interleaved PFC IPM. It consists of a two or three phase PFC IGBT plus diode circuit and a driver IC with control functions. The detailed features and integrated functions of CIPOS™ Mini interleaved PFC IPM are described as follows.



(a) Two phase interleaved PFC IPM (b) Three phase interleaved PFC IPM

Figure 3 Internal circuit

Features

- 650 V, 20 A to 30 A rating in one physical package size (mechanical layouts are identical)
- Fully isolated dual in-line (DIL) molded module
- Infineon TRENCHSTOP™ 5 IGBTs
- Rapid emitter-controlled diodes
- Rugged SOI gate driver technology with stability against transient
- Lead-free terminal plating; RoHS compliant
- Very low thermal resistance due to DCB

- **Functions**
- Overcurrent shutdown
- Temperature sense
- Undervoltage lockout
- Emitter pins accessible for all phase current monitoring (open emitter)
- All switches turn off during protection
- Active-high input signal logic

3.2 Maximum electrical ratings

Table 3 Detail description of absolute maximum ratings (IFCM20T65GD case)

Item	Symbol	Rating	Description
Max. blocking voltage	V_{CES}	650 V	The sustained collector-emitter voltage of internal IGBTs
Output current	I_C	±20 A	The allowable continuous IGBT collector current at T_C = 25°C.
Junction temperature	T_J	-40 ~ 150°C	Considering temperature ripple on the power chips, the maximum junction temperature rating of CIPOS™ Mini interleaved PFC IPM is 150°C.
Operating case temperature range	T_C	-40 ~ 125°C	T_C (case temperature) is defined as a temperature of the package surface underneath the specified power chip. Please mount a temperature sensor on a heat sink surface at the defined position in Figure 4 so as to get accurate temperature information.

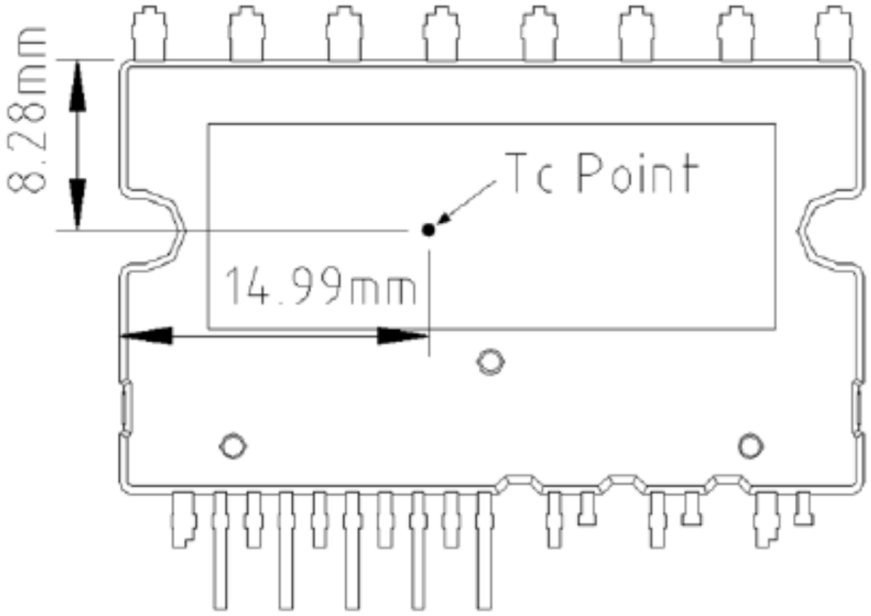


Figure 4 T_C measurement point

3.3 Description of the input and output pins

Table 4 and Table 5 define the CIPOS™ Mini interleaved PFC IPM input and output pins. The detailed functional descriptions are as follows:

Table 4 Pin descriptions of CIPOS™ Mini interleaved PFC IPM for 2 phase interleaved PFC topology

Pin Number	Pin Name	Pin Description
1	NC	No Connection
2	NC	No Connection
3	NC	No Connection
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	LIN(A)	A phase IGBT gate driver input
9	LIN(B)	B phase IGBT gate driver input
10	NC	No Connection
11	V_{DD}	Control supply
12	V_{FO}	Fault output
13	ITRIP	Overcurrent shutdown input
14	V_{SS}	Control negative supply
15	NTC	Thermistor
16	NC	No Connection
17	NB	B phase IGBT emitter
18	B	B phase IGBT collector
19	NA	A phase IGBT emitter
20	A	A phase IGBT collector
21	DB	B phase diode anode
22	DA	A phase diode anode
23	P	Positive output voltage
24	NC	No Connection

Table 5 Pin descriptions of CIPOS™ Mini interleaved PFC IPM for 3 phase interleaved PFC topology

Pin Number	Pin Name	Pin Description
1	NC	No Connection
2	NC	No Connection
3	NC	No Connection
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	LIN(X)	X phase IGBT gate driver input
8	LIN(Y)	Y phase IGBT gate driver input
9	LIN(Z)	Z phase IGBT gate driver input
10	NC	No Connection
11	V_{DD}	Control supply
12	V_{FO}	Fault output
13	ITRIP	Overcurrent shutdown input
14	V_{SS}	Control negative supply
15	NTC	Thermistor
16	NC	No Connection
17	NZ	Z phase IGBT emitter
18	Z	Z phase IGBT collector
19	NY	Y phase IGBT emitter
20	Y	Y phase IGBT collector
21	NX	X phase IGBT emitter
22	X	X phase IGBT collector
23	P	Positive output voltage
24	NC	No Connection

IGBT bias voltage pin

Pin: V_{DD}

- This is the control supply pin for the internal IC.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to this pin.

IGBT common supply ground pin

Pin: V_{SS}

- This pin connects the control ground for the internal IC.

Signal input pins

Pins: LIN(A), LIN(B) for 2-phase, LIN(X), LIN(Y), LIN(Z) for 3-phase

- These are pins to control the operation of the internal IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active-high. The IGBT associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the CIPOS™ Mini interleaved PFC IPM against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 6.

Overcurrent detection pin

Pin: ITRIP

- The current sensing shunt resistor should be connected between the pin N (emitter of IGBT) and the power ground to detect short-circuit current (refer to Figure 8). An RC filter should be connected between the shunt resistor and the pin ITRIP to eliminate noise.
- The integrated comparator is triggered, if the voltage V_{ITRIP} is higher than 0.47 V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at pin V_{FO} is pulled down to LOW.
- The connection length between the shunt resistor and ITRIP pin should be minimized.

Fault output pin

Pin: V_{FO}

- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the CIPOS™ Mini interleaved PFC IPM. The alarm conditions are overcurrent detection and IGBT bias undervoltage operation.
- The V_{FO} output is open-drain configured. The V_{FO} signal line should be pulled up to the logic power supply (5 V / 3.3 V) with proper resistance.

Temperature monitoring pin

Pin: NTC

- The NTC pin provides direct access to the thermistor, which is referenced to V_{SS}.
- An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

Positive output pin

Pin: P

- This is the positive output pin of the CIPOS™ Mini interleaved PFC IPM.
- It is internally connected to the cathods of the PFC diodes.
- In order to suppress the surge voltage caused by the positive output wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically metal film capacitors are used.)

Negative output pins

Pins: NA, NB for 2-phase, NX, NY, NZ for 3-phase

- These are the negative output pins (power ground) of the PFC.
- These pins are connected to the PFC IGBT emitters of the each phase.

PFC power input pins

Pins: A, B for 2-phase

- These pins are IGBT collector. It is mandatory to connect anti-parallel diode between IGBT collector and emitter. PFC input pins for connecting to the PFC inductor.

Pins: DA, DB for 2-phase

- The diode anode should be externally connected with IGBT collector of each phase.

Pins: X, Y, Z for 3-phase

- These pins are IGBT collector. It is mandatory to connect anti-parallel diode between IGBT collector and emitter. PFC input pins for connecting to the PFC inductor. These are internally connected to the PFC diode anode of the each phase.

3.4 Outline drawings

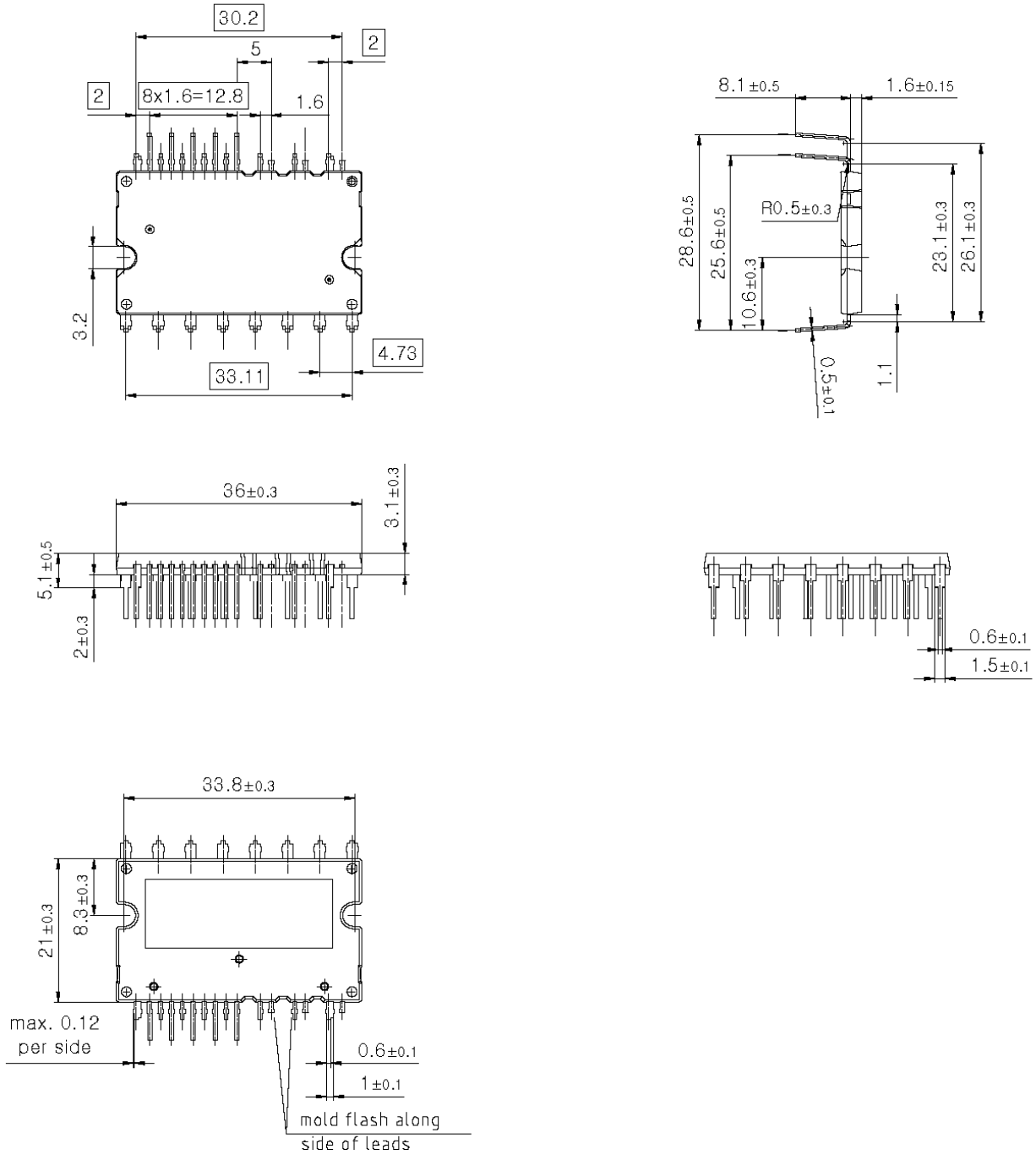


Figure 5 Package outline dimensions (Unit: [mm])

4 Interface circuit and layout guide

4.1 Input/output signal connection

Figure 6 shows the I/O interface circuit between microcontroller and CIPOS™ Mini interleaved PFC IPM. The input logic is active-high with internal pull-down resistors. External pull-down resistors are not needed. V_{FO} output is open-drain configured. This signal should be pulled up to the positive side of 5 V or 3.3 V external logic power supply with a pull-up resistor. The pull-up resistor value should be properly selected, e.g. 3.6 kΩ.

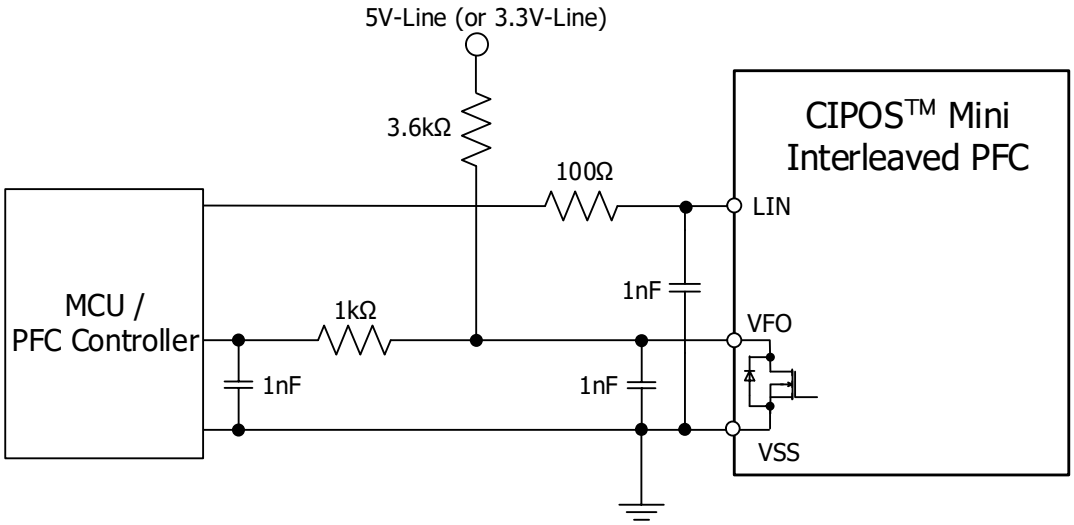


Figure 6 Recommended microcontroller I/O interface circuit

Table 6 Maximum ratings of input and V_{FO} pins

Item	Symbol	Condition	Rating	Unit
Module supply voltage	V_{DD}	Applied between V_{DD} – V_{SS}	20	V
Input voltage	VIN	Applied between LIN(A), LIN(B), LIN(X), LIN(Y), LIN(Z) – V_{SS}	-1 ~ 10	V
Fault output supply soltage	V_{FO}	Applied between V_{FO} – V_{SS}	-0.5 ~ V_{DD}+0.5	V

The input and fault output maximum rating voltages are listed in Table 6. Since the fault output is open-drain configured and its rating is V_{DD}+0.5 V, a 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supply, which is the same as the input signals. It is also recommended placing bypass capacitors as close as possible to the V_{FO} and signal lines from the microcontroller as well as the CIPOS™ Mini interleaved PFC IPM.

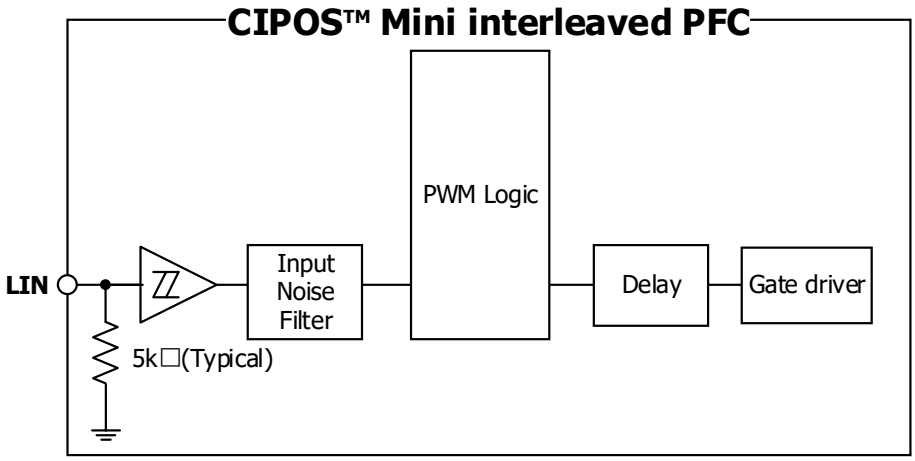


Figure 7 Simplified block diagram of CIPOS™ Mini interleaved PFC IPM control IC

Because CIPOS™ Mini interleaved PFC IPM family employs active-high input logic, the power sequence restriction between the control supply and the input signal during start-up or shut down operation does not exist. Therefore it makes the system fail-safe. In addition, pull-down resistors are built in to each input circuit. Thus, external pull-down resistors are not needed. This reduces the required external component count. Input Schmitt-trigger and noise filter functions provide beneficial noise rejection to short input pulses. Furthermore, by lowering the turn on and turn off threshold voltage of input signal as shown in Table 7, a direct connection to 3.3 V-class microcontroller or DSP is possible.

Table 7 Input threshold voltage (at V_{DD} = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (LIN)	V_{IH_TH}	LIN – V_{SS}	-	2.1	2.5	V
Logic "0" input voltage (LIN)	V_{IL_TH}		0.7	0.9	-	V

As shown in Figure 7, the CIPOS™ Mini interleaved PFC IPM input signal section integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between microcontroller output and CIPOS™ Mini interleaved PFC IPM input, pay attention to the signal voltage drop at the CIPOS™ Mini interleaved PFC IPM input terminals. It should fulfill the logic "1" input voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown in Figure 6.

4.2 General interface circuit example

Figure 8 and Figure 9 show typical application circuit of CIPOS™ Mini interleaved PFC IPM for interface schematic with control signals connected directly to a microcontroller.

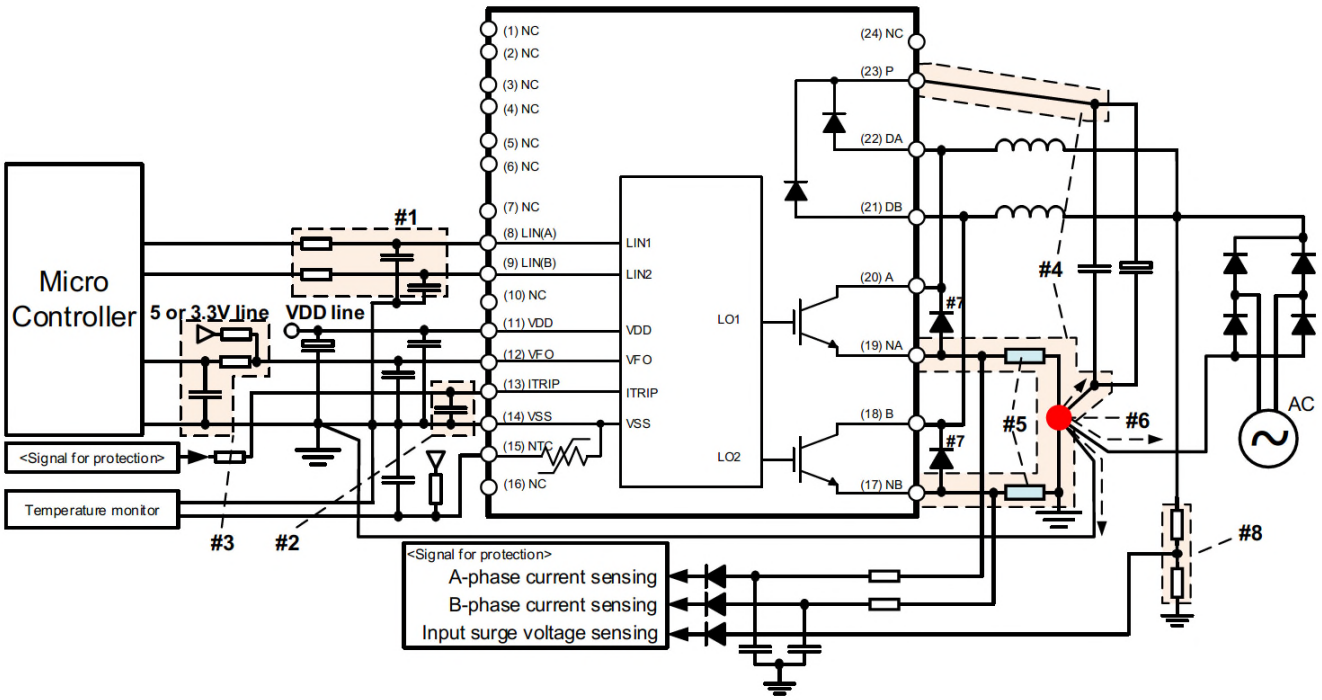


Figure 8 Application circuit example of CIPOS™ Mini 2-phase interleaved PFC IPM (IFCMxxT65zu)

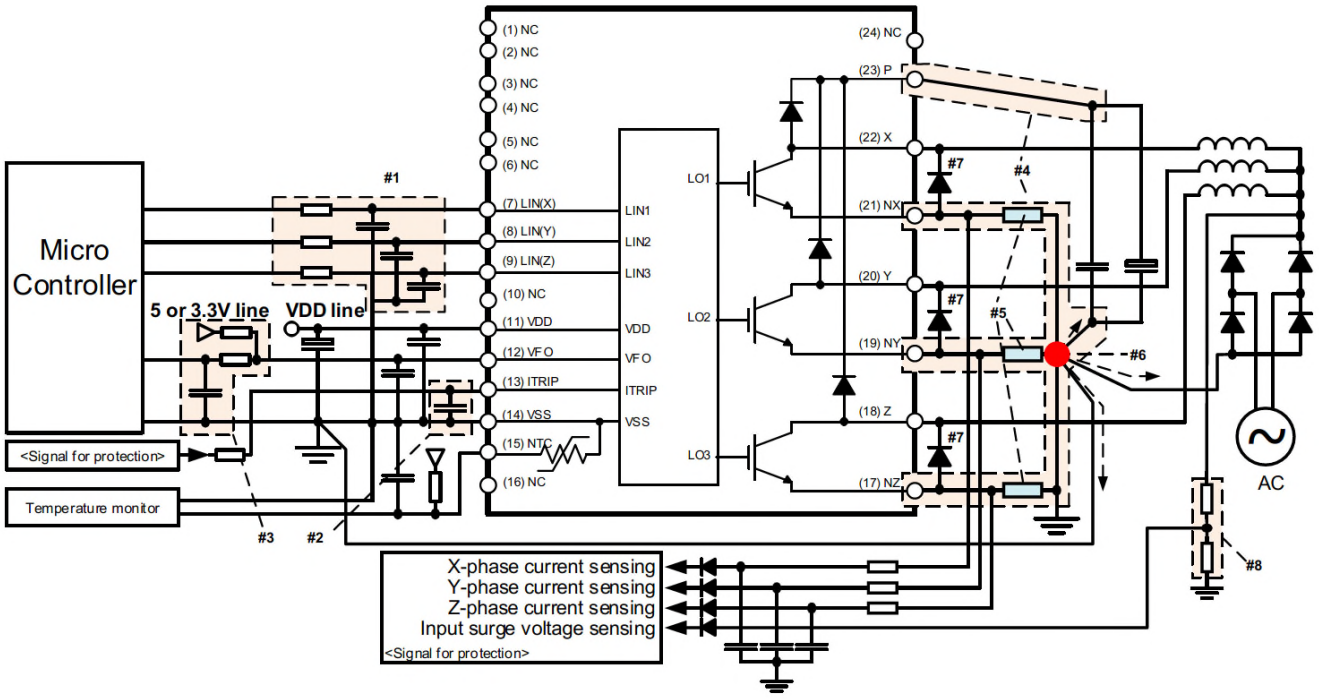


Figure 9 Application circuit example of CIPOS™ Mini 3-phase interleaved PFC IPM (IFCMxxU65zu)

Note:

1. *The input signals are active-high configured. There is an internal 5 kΩ pull-down resistor from each input signal line to V_{SS}. When employing RC coupling circuits between microcontroller and CIPOS™Mini interleaved PFC IPM, the RC values should be properly selected so that the input signals are compatible with the CIPOS™ Mini interleaved PFC IPM logic "1"/logic "0" input voltages.*
2. *To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3 cm)*
3. *The merit of integrating an application specific type IC inside CIPOS™Mini interleaved PFC IPM is to achieve the direct coupling to microcontroller terminals without any opto-coupler or transformer isolation.*
4. *V_{FO} output is an open-drain output. This signal line should be pulled up to the positive side of the 5 V/3.3 V logic power supply with a pull up resistor. When placing RC filter between CIPOS™Mini interleaved PFC IPM and microcontroller, close location to the microcontroller is recommended. (Refer to Figure 6)*
5. *To prevent protection function errors, the R_{ITRIP} and C_{ITRIP} wiring between ITRIP and N pins should be as short as possible. C_{ITRIP} wiring should be placed as close to V_{SS} pin as possible.*
6. *The short-circuit protection time constant $\tau_{ITRIP} = R_{ITRIP} * C_{ITRIP}$ should be set in the range of 1~2 µs. The IGBT turning off within 5 µs must be ensured with the overall overcurrent protection reaction time of the control.*
7. *Each capacitor should be mounted as close to the pins of the CIPOS™Mini interleaved PFC IPM as possible.*
8. *V_{DD} of 16 V is recommended when the integrated bootstrap circuitry only is used.*
9. *It is recommended connecting the ground pin of microcontroller directly to the V_{SS} pin.*

4.3 Recommended rated output current of power supply

Control and gate drive power for the CIPOS™ Mini interleaved PFC IPM is normally provided by a single 15 V supply that is connected to the module V_{DD} and V_{SS} terminal. The circuit current of V_{DD} control supply of IFCM30T65GD is shown in below Table 8.

Table 8 The circuit current of control power supply of IFCM30T65GD (Unit: [mA])

Item		Static (typ.)	Dynamic (typ.)	Total (typ.)
V_{DD} = 15 V	f_{SW} = 15 kHz	0.40	1.44	1.84
	f_{SW} = 20 kHz	0.40	1.92	2.32
V_{DD} = 20 V	f_{SW} = 20 kHz	0.85	7.44	8.29

And, the circuit current of the 5 V logic power supply (V_{FO} & input terminals) is about 9 mA.

Finally, the recommended minimum circuit currents of power supply are shown in Table 9 which is considered ripple current and enough margins at the worst conditions, e.g. 5 times higher than the calculated value.

Table 9 The recommended minimum circuit current of power supply (Unit: [mA])

Item	The circuit current of +15 V control supply	The circuit current of +5 V logic supply
$V_{DD} \le 20$ V, $f_{SW} \le 20$ kHz	45	45

4.4 Recommended layout pattern for OCP function

It is recommended that the ITRIP filter capacitor connections to the CIPOS™ Mini interleaved PFC IPM pins be as short as possible. The ITRIP filter capacitor should be connected to V_{SS} pin directly without overlapped ground pattern. The signal ground and power ground should be as short as possible and connected at only one point via the filter capacitor of V_{DD} line.

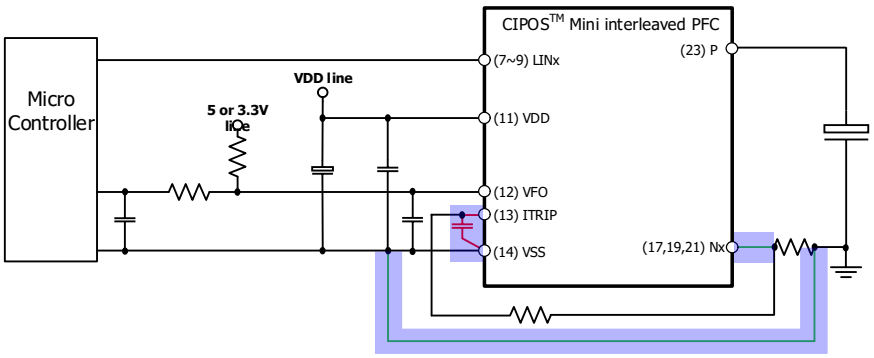


Figure 10 Recommended layout pattern for OCP function

4.5 Recommended wiring of shunt resistor and snubber capacitor

External current sensing resistors are applied to detect overcurrent of phase currents. A long wiring pattern between the shunt resistors and CIPOS™ Mini interleaved PFC IPM will cause excessive surges that might damage internal IC and current detection components. This may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and CIPOS™ Mini interleaved PFC IPM should be as short as possible.

As shown in Figure 11 snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a high frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location ‘1’ as shown in Figure 11Figure 11, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location ‘2’, the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be a little lower than the calculated design value. The “2” position surge suppression effect is greater than the location ‘1’ or ‘3’. The ‘3’ position is a reasonable compromise with better suppression than in location ‘1’ without impacting the current sensing signal accuracy. For this reason, the location ‘3’ is generally used.

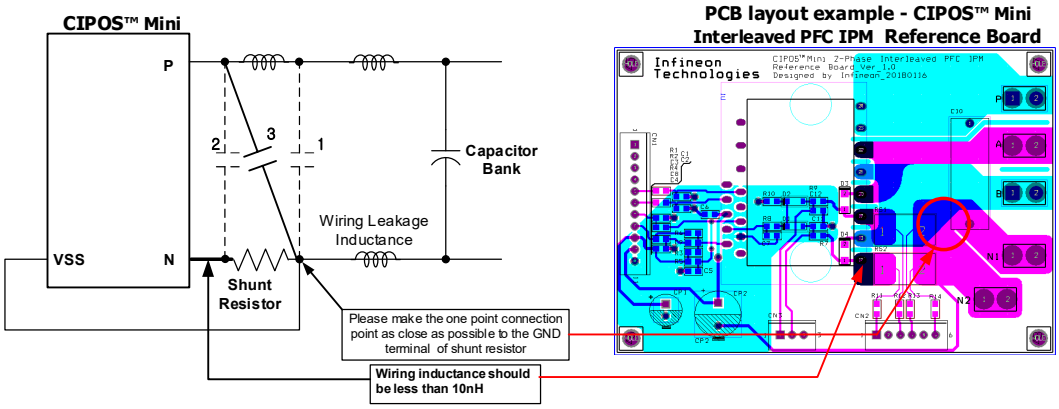


Figure 11 Recommended wiring of shunt resistor and snubber capacitor

4.6 Pin and screw holes coordinates for CIPOS™ Mini interleaved PFC IPM footprint

Figure 12 shows CIPOS™ Mini interleaved PFC IPM position on PCB to indicate center coordinates of each pin and screw hole in Table 10.

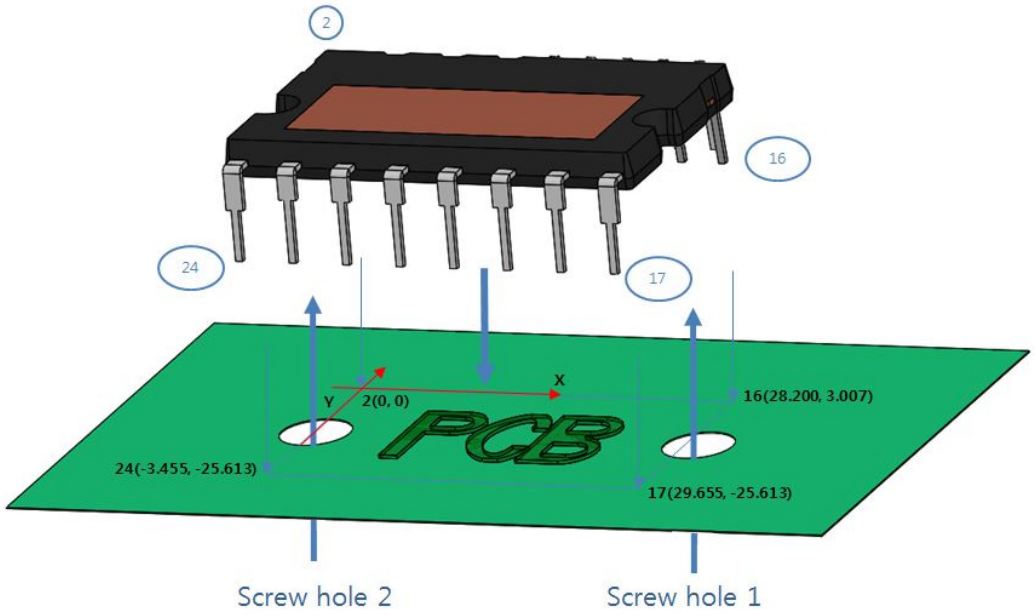


Figure 12 CIPOS™ Mini interleaved PFC IPM position on PCB (Unit: [mm])

Table 10 Pin & screw holes coordinates for CIPOS™ Mini interleaved PFC IPM footprint (Unit: [mm])

Pin Number		X	Y	Pin Number		X	Y
Signal Pin	1	N/A	N/A	Signal Pin	14	24.600	0.000
	2	0.000	0.000		15	26.200	3.007
	3	N/A	N/A		16	28.200	0.000
	4	5.000	0.000	Power Pin	17	29.655	-25.613
	5	N/A	N/A		18	24.925	-25.613
	6	10.000	0.000		19	20.195	-25.613
	7	13.400	3.007		20	15.465	-25.613
	8	15.000	0.000		21	10.735	-25.613
	9	16.600	3.007		22	6.005	-25.613
	10	18.200	0.000		23	1.275	-25.613
	11	19.800	3.007		24	-3.455	-25.613
	12	21.400	0.000	Screw Hole	1	30.000	-14.977
	13	23.000	3.007		2	-3.800	-14.977

5 Protection features

5.1 Undervoltage protection

Control and gate drive power for the CIPOS™ Mini interleaved PFC IPM is normally provided by a single 15 V supply that is connected to the module V_{DD} and V_{SS} terminals. For proper operation this voltage should be regulated to 15 V ± 10%. Table 11 describes the behavior of the CIPOS™ Mini interleaved PFC IPM for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected at the CIPOS™ Mini interleaved PFC IPM's pins.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1 V/µs.

The potential at the module's V_{SS} terminal is different from that at the N power terminal by the voltage drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (V_{SS}) a ground plane in the PCB layout.

When control supply voltage (V_{DD}) falls down under UVLO level, IGBT will turn off while ignoring the input signal.

Table 11 CIPOS™ Mini interleaved PFC IPM functions versus control power supply voltage

Control voltage range [V]	CIPOS™ Mini Interleaved PFC IPM function operations
0 ~ 4	Control IC does not operate. UVLO and fault output does not operate.
4 ~ 13	As the undervoltage lockout function is activated, control input signals are blocked and a fault signal V_{FO} is generated.
13 ~ 14	IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range so the $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
14 ~ 18.5 for V_{DD}	Normal operation. This is the recommended operating condition.
18.5 ~ 20 for V_{DD}	IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. It causes increasing system noise.
Over 20	Control circuit in the CIPOS™ Mini interleaved PFC IPM might be damaged.

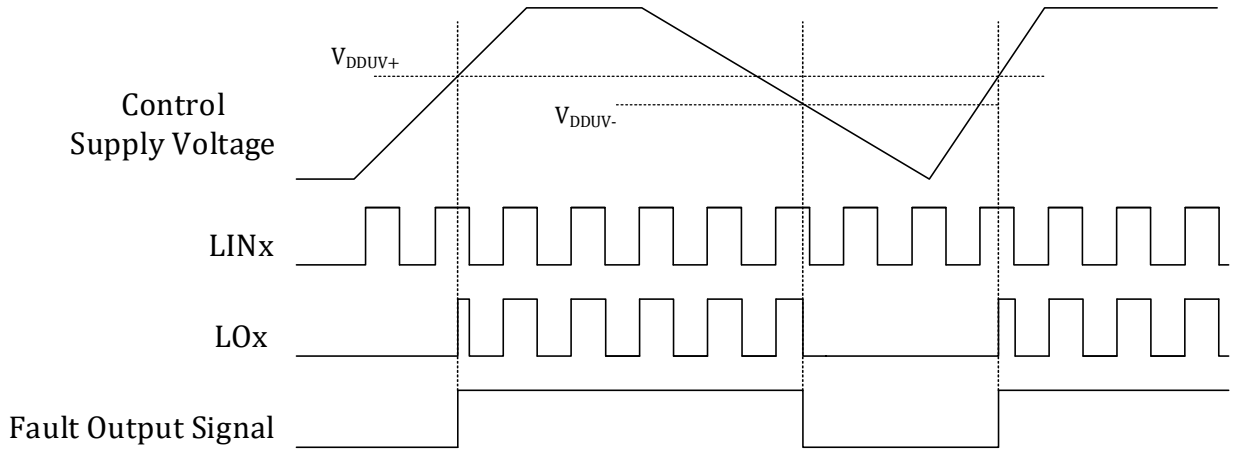


Figure 13 Timing chart of low-side undervoltage protection function

5.2 Overcurrent protection

5.2.1 Timing chart of overcurrent (OC) protection

The CIPOS™ Mini interleaved PFC IPM has an overcurrent shutdown function. Its internal IC monitors the voltage of the ITRIP pin and if this voltage exceeds the $V_{IT,TH+}$, which is specified in the devices datasheets, a fault signal is activated and all IGBTs are turned off. In order to avoid this potential problem, the maximum overcurrent trip level is generally set to below 2 times the nominal rated collector current. The overcurrent protection-timing chart is shown in Figure 14.

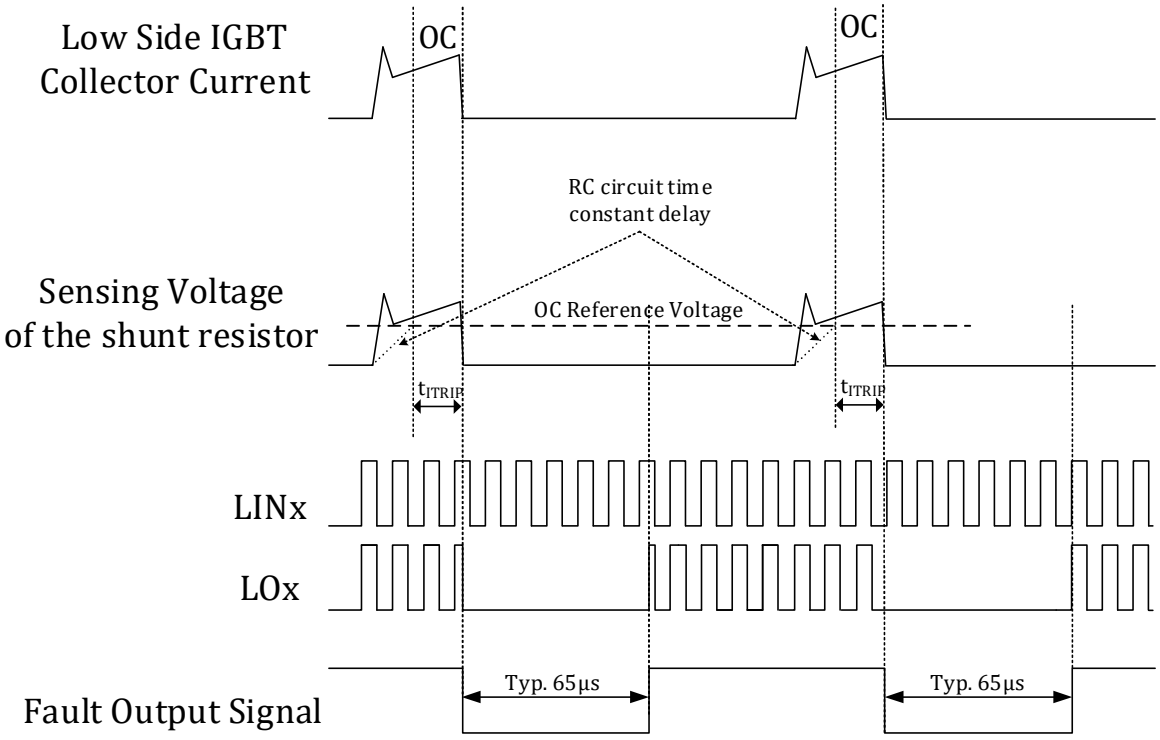


Figure 14 Timing chart of overcurrent protection function

5.2.2 Selecting current sensing shunt resistor

The value of the current sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive going threshold voltage of CIPOS™ Mini interleaved PFC IPM. It is typically 0.47 V. I_{OC} is the current of OC detection level.

The maximum value of OC protection level should be set lower than the repetitive peak collector current in the datasheet considering the tolerance of shunt resistor.

For example, the maximum peak collector current of IFCM20T65GD is 30 A_{peak}, and thus, the recommended value of the shunt resistor is calculated as

$$R_{SH(min)} = \frac{0.47}{30} = 0.016\Omega$$

For the power rating of the shunt resistor, the below list should be considered:

- Maximum load current of PFC (I_{rms})
- Shunt resistor value at T_C = 25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH} = 100°C according to the manufacturer's datasheet
- Safety margin

The shunt resistor power rating is calculated by the following equation.

$$P_{SH} = \frac{I_{rms}^2 \times R_{SH} \times margin}{derating\,ratio} \quad (2)$$

For example, in case of IFCM20T65GD and R_{SH} = 16 mΩ:

- Max. load current of the inverter: 7 A_{rms}
- Power derating ratio of shunt resistor at T_{SH} = 100°C: 80%
- Safety margin : 30%

$$P_{SH} = \frac{7^2 \times 0.017 \times 1.3}{0.8} = 1.35W$$

A proper power rating of shunt resistor is over than 1.35 W, e.g. 2.0 W.

Based on the previous equations, conditions, and calculation method, the minimum shunt resistance and resistor power according to CIPOS™ Mini interleaved PFC IPM products are introduced as listed in Table 12.

It's noted that a proper resistance and power rating higher than the minimum value should be chosen considering the overcurrent protection level required in the application.

Table 12 Examples of minimum R_{SH} and P_{SH}

Product	Maximum peak current	Minimum shunt resistance, R_{SH}	Minimum shunt resistor power, P_{SH}
IFCM30U65GD	40 A	12 mΩ	3 W
IFCM30T65GD	40 A	12 mΩ	3 W
IFCM20U65GD	30 A	17 mΩ	2 W
IFCM20T65GD	30 A	17 mΩ	2 W

5.2.3 Delay time

The RC filter is necessary in the overcurrent sensing circuit to prevent malfunction of OC protection caused by noise. The RC time constant is determined by considering the noise duration and safety operation capability of the IGBT.

When the sensing voltage on shunt resistor exceeds the ITRIP positive going threshold ($V_{IT,TH+}$), this voltage is applied to the ITRIP pin of CIPOS™ Mini via the RC filter. Table 13 shows the specification of the OC protection reference level. The filter delay time (t_{FILTER}) that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is caused by below equation (3), (4).

$$V_{IT,TH+} = R_{SH} \cdot I_C \cdot \left(1 - \frac{1}{e^{\frac{t_{Filter}}{\tau}}}\right) \quad (3)$$

$$t_{Filter} = -\tau \cdot \ln\left(1 - \frac{V_{IT,TH+}}{R_{SH} \cdot I_C}\right) \quad (4)$$

Where, $V_{IT,TH+}$ is the ITRIP pin input voltage, I_C is the peak current, R_{SH} is the shunt resistor value and τ is the RC time constant. In addition there is a shutdown propagation delay of Itrip (t_{ITRIP}). In addition there is a shutdown propagation delay of Itrip (t_{ITRIP}). Please refer to Table 14.

Table 13 Specification of OC protection reference level ' $V_{IT,TH+}$'

Item	Min.	Typ.	Max.	Unit
ITRIP positive going threshold $V_{IT,TH+}$	0.40	0.47	0.54	V

Table 14 Internal delay time of OC protection circuit

Item		Condition	Min.	Typ.	Max.	Unit
Shut down propagation delay (t_{ITRIP})	IFCM30U65GD	I_{out} =20A, from $V_{IT,TH+}$ to 10% I_{out}		1420		ns
	IFCM30T65GD	I_{out} =20A, from $V_{IT,TH+}$ to 10% I_{out}		1420		
	IFCM20U65GD	I_{out} =15A, from $V_{IT,TH+}$ to 10% I_{out}		1350		
	IFCM20T65GD	I_{out} =15A, from $V_{IT,TH+}$ to 10% I_{out}		1350		

Therefore the total time from ITRIP positive going threshold ($V_{IT,TH+}$) to the shut down of the IGBT becomes:

$$t_{Total} = t_{Filter} + t_{ITRIP} \quad (3)$$

The recommended total delay is less than the 5 µs of safety operation. Thus, the RC time constant should be set in the range of 1~2 µs. Recommended values for the filter components are R = 1.8 kΩ and C = 1 nF.

5.3 Fault output circuit

Table 15 Fault-output maximum ratings

Item	Symbol	Condition	Rating	Unit
Fault output supply voltage	V_{FO}	Applied between V_{FO}-V_{SS}	-0.5~ V_{DD}+0.5	V
Fault output current	I_{FO}	Sink current at V_{FO} pin	10	mA

Table 16 Electric characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output current	I_{FO}	V_{ITRIP} = 0 V, V_{FO} = 5 V	-	2	-	nA
Fault output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.5	-	V

Because V_{FO} terminal is an open-drain type, it must be pulled up to the high level via a pull-up resistor. The resistor has to be calculated according to the above specifications.

5.4 Over temperature protection

CIPOS™ Mini interleaved PFC IPM has independent NTC pins for temperature sensing functions. Figure 15 shows the internal thermistor resistance characteristics as a function of the thermistor temperature. As shown in Figure 16, NTC pin is connected directly to ADC terminals of the microcontroller. This circuit is very simple and allows the IGBTs have to be shut down by NTC temperature. For example, when R1 is 3.6 kΩ, then NTC at about 100°C of thermistor temperature is 2.95 V_{typ} at V_{ctr} = 5 V and 1.95 V at V_{ctr} = 3.3 V, as shown in Figure 17.

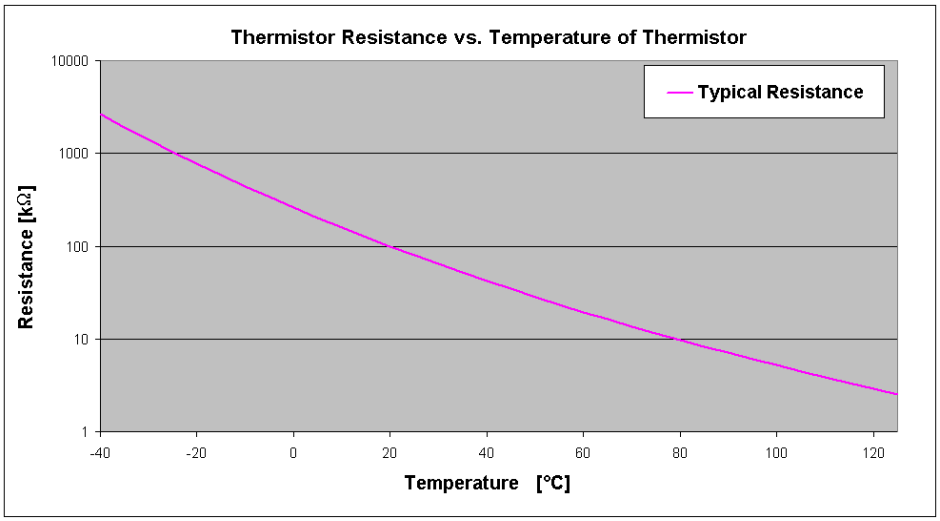


Figure 15 Internal thermistor resistance characteristics as a function of thermistor temperature

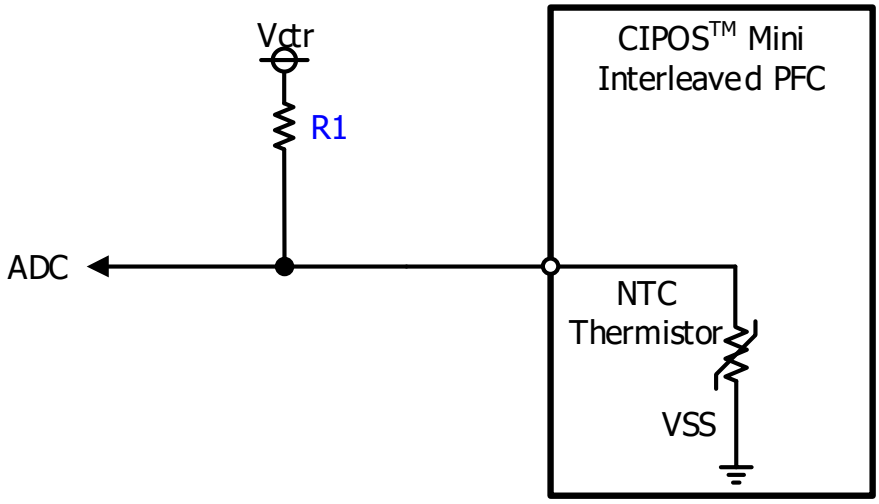


Figure 16 Circuit proposals for over temperature protection

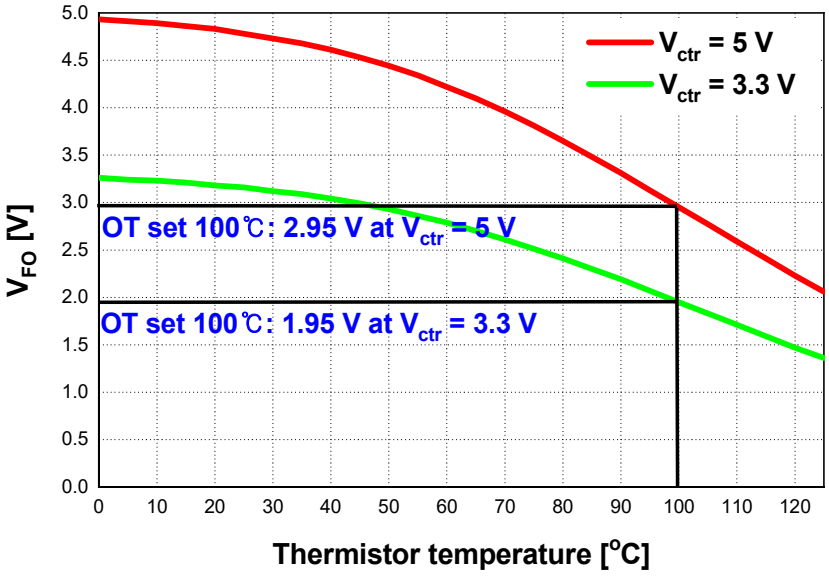


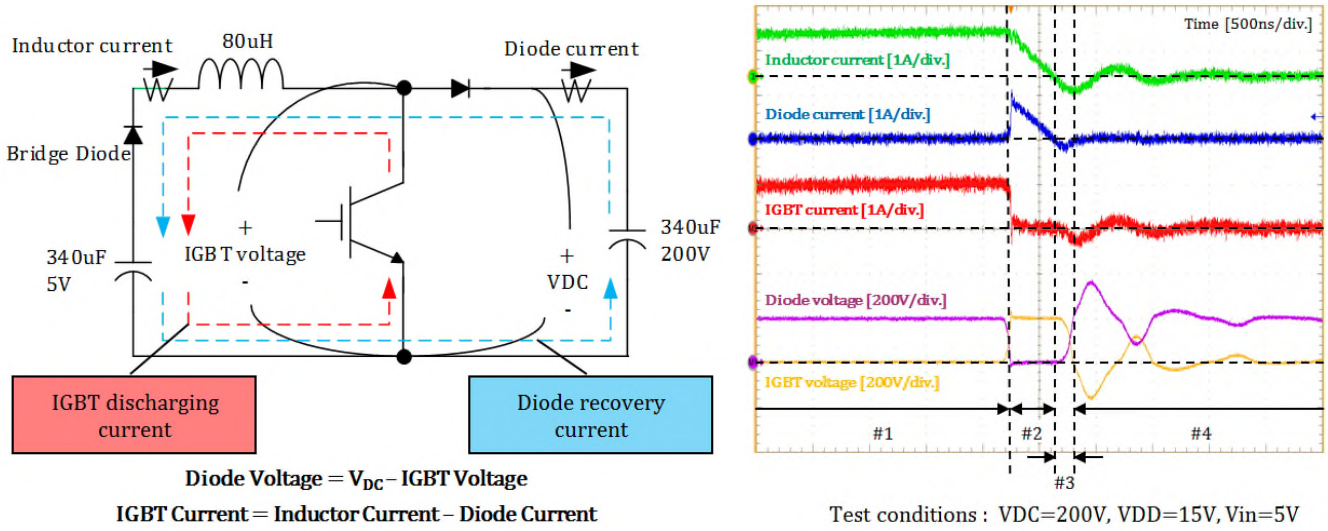
Figure 17 Voltage of NTC pin according to thermistor temperature when R1 is 3.6kΩ

6 Peripheral PFC Circuit

6.1 Anti-parallel diode between collector and emitter

During startup, shutdown and under fault conditions power circuits often pass through operating modes that are not readily apparent from normal operation analysis. And example is the standard boost PFC circuit. A PFC circuit may be designed to operate its boost inductor in the continuous current mode (CCM) during normal load operation. However, under light load, the boost inductor may go into discontinuous current mode (DCM) conduction. Discontinous operation may also occur near the AC mains zero voltage crossing even under full load conditions. Operation in DCM may require the PFC powerswitching device to conduct in the reverse direction. If an alternate current path is not provided for this switch current reversal, the IGBT may be reverse avalanched. In most cases low energy reverse avalanche is not harmful to IGBTs but it will cause additional heating. However, under specific circumstances gradual degradation and failure is possible. If the energy associated with this current reversal is minimal the failure mode may not be immediate but appear as gradual device degradation and random device failures. For detailed information, please refer to [7].

Figure 18 explain circuit operation about negative voltage generation at IGBT during DCM mode operation at low AC input conditions. When IGBT status was changed from turn-on (#1) to turn-off (#2), diode reverse recovery current flow via circuit path (#3) when inductor current was became zero. At this time, IGBT voltage goes down negative value (#4).



(a) Circuit Operation during IGBT On/Off (b) Waveform at each component

Figure 18 Circuit operation and operating waveform during DCM mode operation at low AC input condition

So, in order to prevent random failure problem by reverse avalanched, anti-parallel diode should be added between collector and emitter to bypass reverse current. For anti-parallel diode, voltage rating is same with boost IGBT rating and current rating is 1~2 A. We recommend 800 V, 2 A rating fast recovery diode. Figure 19 shows effect of anti-parallel diode.

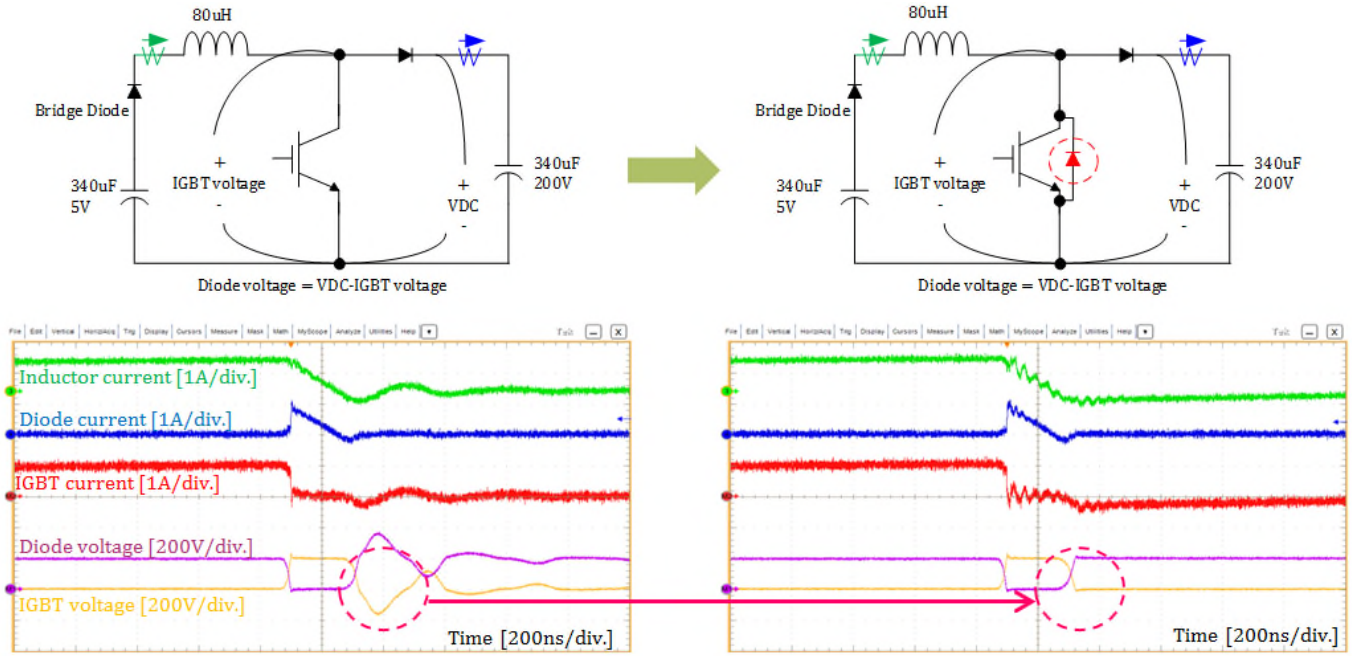


Figure 19 Correction of negative voltage at IGBT by using anti-parallel diode

7 Thermal system design

7.1 Introduction

The thermal design of a system is a key issue of CIPOS™ Mini interleaved PFC IPM included in electronic systems such as motor drives. In order to avoid overheating and / or to increase the reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing CIPOS™ Mini interleaved PFC IPM as intelligent power module for the application. To get the most power out of the system a proper heat sink choice is necessary. A good thermal design either allows to maximize the power or to increase the reliability of the system (by reducing the maximum temperature). This application note will give a short introduction to power losses and heat sinks, helping to understand the mode of operation and to find the right heat sink for a specific application.

For the thermal design, one needs:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,max}$ of the power semiconductors
- The junction to ambient thermal resistance impedance $Z_{th,J-A}$. For stationary considerations the static thermal resistance $R_{th,J-A}$ is sufficient. This thermal resistance comprises the junction to case thermal resistance $R_{th,J-C}$ as provided in datasheets, the case to heat sink thermal resistance $R_{th,C-HS}$ accounting for the heat flow through the thermal interface material between heat sink and the power module and the heat sink to ambient thermal resistance $R_{th,HS-A}$. Each thermal resistance can be extended to its corresponding thermal impedance by adding the thermal capacitances.
- The maximum allowable ambient temperature $T_{A,max}$

Furthermore all heat flow paths need to be identified. Figure 20 presents a typical simplified equivalent circuit for the thermal network. This circuit is simplified as it omits thermal capacitances and typically negligible heat paths such as the heat transfer from the module surface directly to the ambient via convection and radiation.

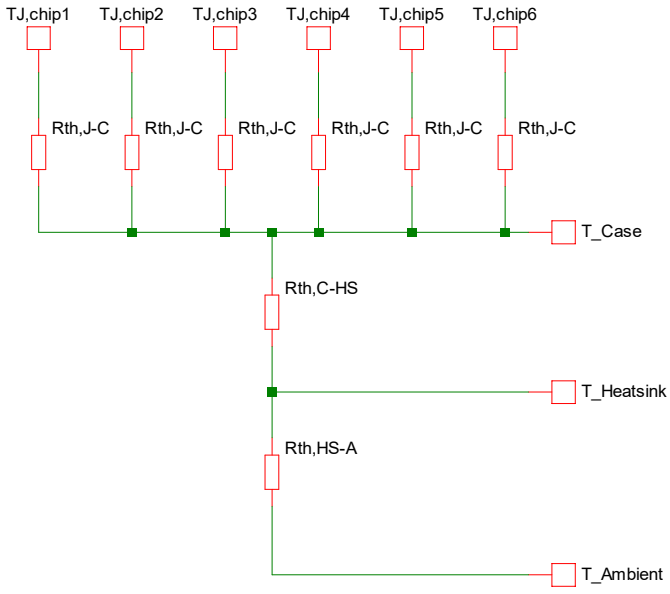


Figure 20 Simplified thermal equivalent circuit

7.2 Power loss

PFC shapes the input current of the power supply to be synchronized with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics. In order to proper design, we need to consider several factors. However, in this chapter, we introduce the equation for power losses estimation of IGBT & diode. For other design infromation like bridge rectifier, gate drive circuit, boost inductor, AC line current filter, and etc, please refer to [8].

7.2.1 Conduction losses

Following is the theory for the simplified power loss calculation.

For simplicity input waveforms are full periodic sinusoidal signals:

$V_{in}(t) = V_{in,peak} * sin(\omega * t)$

The first half wave (T/2) current for the controlled and uncontrolled switch:

$I_{in}(t) = I_{in} * sin(\omega * t)$

$I_{IGBT}(t) = PWM(t) * I_{in}(t)$

$I_{Diode}(t) = (1 - PWM(t)) * I_{in}(t)$

Input voltage peak to output voltage ratio is taken as variable($0 \leq \frac{V_{in,peak}}{V_{out}} \leq 1$). The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$V_{IGBT} = V_I + R_I \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i$$

- V_I = Threshold voltage of IGBT
- V_D = Threshold voltage of diode
- R_I = on-state slope resistance of IGBT
- R_D = on-state slope resistance of diode

The average conduction loss of the IGBT for the first half wave is:

$$P_{cond,IGBT} = \frac{2}{T} * \int_0^{\frac{T}{2}} V_{IGBT}(I_C(t)) * I_C(t) dt$$

Therefore it is possible to describe the V_{IGBT} characteristics with two prameters (V_I, R_I) and use them for the calculation of conduction losses.

$$P_{cond,IGBT} = \frac{2}{T} * \int_0^{\frac{T}{2}} (V_I + PWM(t) * I_{in}(t) * R_I) * PWM(t) * I_{in}(t) dt$$

Using:

$$PWM^2(t) = PWM(t)$$

and using D as average model IGBT duty cycle:

$$D(t_i) = \frac{1}{T_{SW}} * \int_{t_i}^{t_i + T_{SW}} PWM(t) dt$$

$$P_{cond,IGBT} = \frac{2}{T} * (V_I * \int_0^{\frac{T}{2}} PWM(t) * I_{in}(t)dt + R_I * \int_0^{\frac{T}{2}} PWM(t) * I_{in}^2(t)dt)$$

For CCM operation:

$$D(t) = 1 - \frac{V_{in,peak}}{V_{out}} * sin(\omega * t)$$

Therefore, the result:

$$P_{cond,IGBT} = \frac{2}{T} * (V_I * I_{in} * \sqrt{2} * \int_0^{\frac{T}{2}} sin(\omega * t) - \frac{V_{in,peak}}{V_{out}} * sin^2(\omega * t)dt + R_I * I_{in}^2 * \int_0^{\frac{T}{2}} sin^2(\omega * t) - \frac{V_{in,peak}}{V_{out}} * sin^3(\omega * t)dt)$$

$$P_{cond,IGBT} = V_I * I_{in} * \left(\frac{2 * \sqrt{2}}{\pi} - \frac{V_{in,peak}}{V_{out}} * \frac{1}{\sqrt{2}}\right) + R_I * I_{in}^2 * (1 - \frac{V_{in,peak}}{V_{out}} * \frac{8}{3 * \pi})$$

The same way for the boost diode:

$$P_{cond,diode} = \frac{V_{in,peak}}{V_{out}} * (V_D * I_{in} * \frac{1}{\sqrt{2}} + R_D * I_{in}^2 * \frac{8}{3 * \pi})$$

7.2.2 Switching losses

The influence of the diode for the switch on losses of the IGBT makes it necessary to characterize the IGBT and diode pair together.

$$P_{swi,IGBT} = F_{SW} * \frac{2}{T} * \int_0^{\frac{T}{2}} E_{off}\big(I_{IGBT}(t)\big) + E_{on}\big(I_{IGBT}(t)\big)dt$$

Assuming linear switching characteristics, it is possible to describe the switching characteristics with 4 parameters ($E_{off,0}$, $E_{off,n}$, $E_{on,0}$, $E_{on,n}$) and use them for calculation of the switching loesses:

$$E_{off}(I_{IGBT}) = E_{off,0} + \frac{E_{off,n} - E_{off,0}}{I_n} * I_{IGBT}$$

$$E_{on}(I_{IGBT}) = E_{on,0} + \frac{E_{on,n} - E_{on,0}}{I_n} * I_{IGBT}$$

With I_n and V_n are the nominal current and output voltage where switching losses were measured and F_{SW} is a constant switching frequency:

$$P_{swi,IGBT} = \frac{V_{out}}{V_n} * F_{SW} * \frac{2}{T} * \int_0^{\frac{T}{2}} E_{off,0} + E_{on,0} + \frac{(E_{off,n} - E_{off,n} + E_{on,n} - E_{on,0})}{I_n} * I_{IGBT}(t)dt$$

The switching losses are calculated to:

$$P_{swi,IGBT} = \frac{V_{out}}{V_n} * F_{SW} * (E_{off,0} + E_{on,0} + \frac{I_{in}}{I_n} * \sqrt{2} * \frac{2}{\pi} * (E_{off,n} - E_{on,0} + E_{on,n} - E_{on,0})$$

Same for the Diode:

$$P_{swi,Diode} = \frac{V_{out}}{V_n} * F_{SW} * (E_{rec,0} + \frac{I_{in}}{I_n} * \sqrt{2} * \frac{2}{\pi} * \big(E_{rec,n} - E_{rec,0}\big)).$$

7.3 Thermal impedance

In practical operation, the power loss P_D is cyclic and therefore the transient impedance needs to be considered. The thermal impedance is typically represented by a RC equivalent circuit (foster type chain) as shown in Figure 21. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the CIPOS™ Mini interleaved PFC IPM. Figure 22 shows thermal impedance from junction to case curves of IFCM20T65GD. The thermal resistance goes into saturation in about 10 seconds. Other kinds of CIPOS™ Mini interleaved PFC IPM also show similar characteristics.

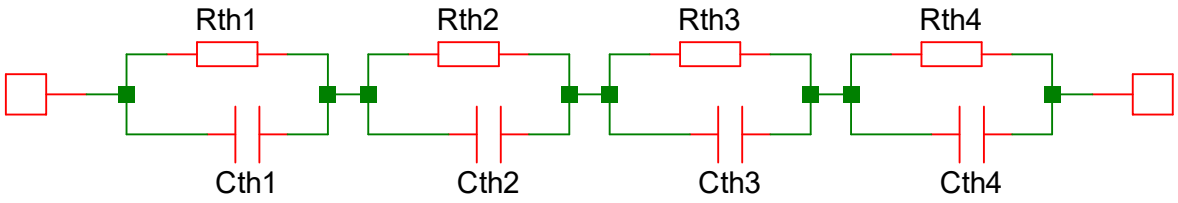


Figure 21 Thermal impedance RC equivalent circuit

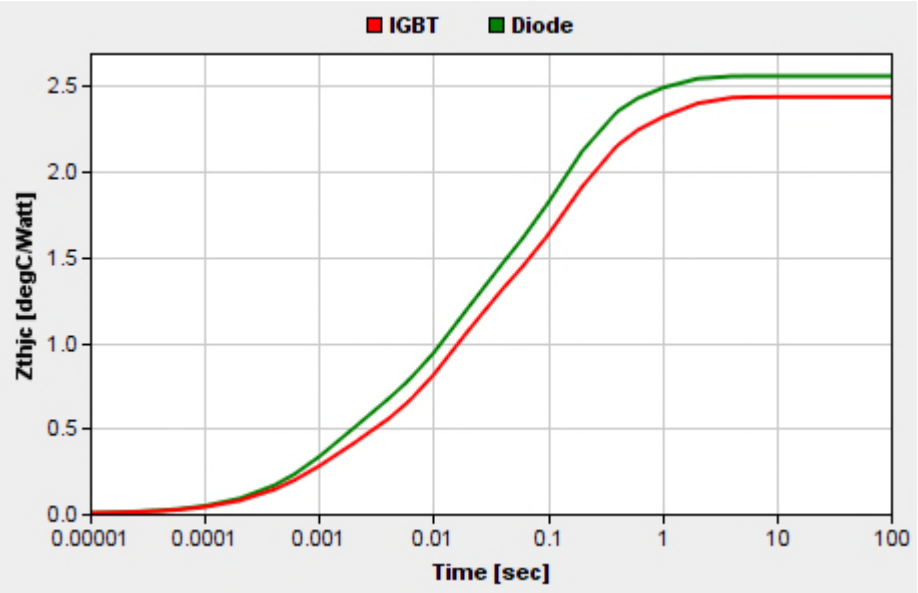


Figure 22 Thermal impedance curves (IFCM20T65GD)

7.4 Temperature rise considerations and calculation example

The simulator CIPOSIM allows calculating power losses and temperature profiles for a constant case temperature. The result of loss calculation using the typical characteristics is shown in Figure 23 as “Effective current versus carrier frequency characteristics” (for V_{PN} = 390 V, V_{DD} = 15 V, $V_{CE(sat)}$ = typical, Switching loss = typical, T_J = 150°C, T_C = 100°C, Rth(j-c) = Max., PF = 1.0, V_{AC} = 180 V, f_{AC} = 60 Hz, CCM PFC).

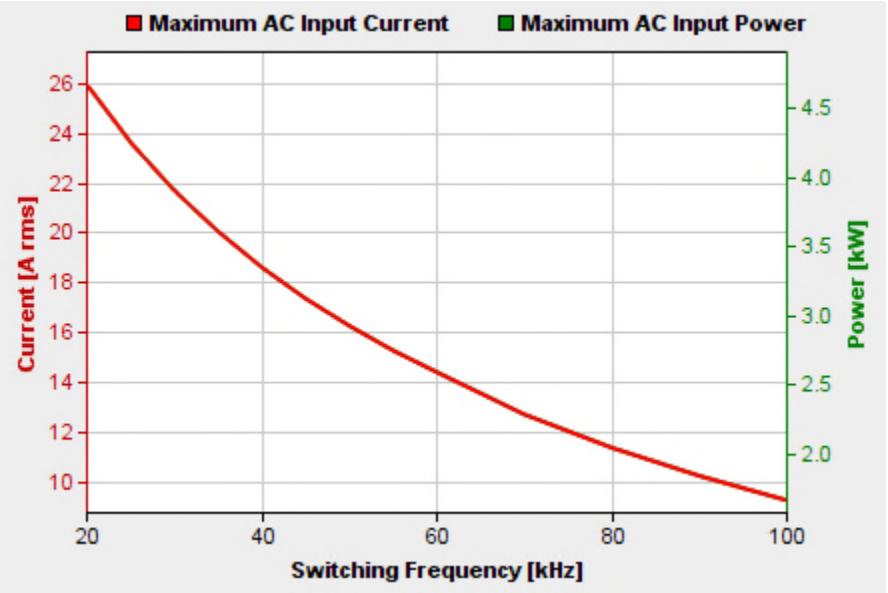


Figure 23 Effective current versus carrier frequency characteristics of IFCM20T60GD [9]

7.5 Heat sink selection guide

7.5.1 Required heat sink performance

If the power losses $P_{sw,i}$, $R_{th,J-C}$ and the maximum ambient temperature are known, the required thermal resistance of the heat sink and the thermal interface material can be calculated according to Figure 21 from,

$$T_{J,max} = T_{A,max} + \sum_i P_{sw,i} \cdot R_{th,HS-A} + \sum_i P_{sw,i} \cdot R_{th,C-HS} + Max(P_{sw,i} \cdot R_{th,JC,i}) \quad (16)$$

For three phase bridges one can simply assume that all power switches dissipate the same power and they all have the same $R_{th,J-C}$. This leads to the required thermal resistance from case to ambient.

$$R_{th,C-A} = R_{th,C-HS} + R_{th,HS-A} = \frac{T_{J,max} - P_{sw} \cdot R_{th,JC} - T_{A,max}}{\sum P_{sw}} \quad (17)$$

For example, the power switches of a washing machine drive dissipate 3.5 W maximum each, the maximum ambient temperature is 50°C, the maximum junction temperature is 150°C and $R_{th,jC}$ is 3 K/W. It results in,

$$R_{th,C-A} \le \frac{150°C - 3.5W \cdot 3\frac{K}{W} - 50°C}{6 \cdot 3.5W} = 4.3\frac{K}{W}$$

If the heat sink temperature shall be limited to 100°C, an even lower thermal resistance is required:

$$R_{th,C-A} \le \frac{100°C - 50°C}{6 \cdot 3.5W} = 2.4\frac{K}{W}$$

Smaller heat sinks with higher thermal resistances may be acceptable if the maximum power is only required for a short time (times below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heat sink the larger it's thermal capacitance the longer does it take to heat up the heat sink.

7.5.2 Heat sink characteristics

Heat sinks are characterized by three parameters:

- Heat transfer from the power source to heat sink
- Heat transfer within the heat sink (to all the surfaces of the heat sink)
- Heat transfer from heat sink surfaces to ambient

7.5.2.1 Heat transfer from heat source to heat sink

There are two factors which need to be considered in order to provide a good thermal contact between power source and heat sink:

- **Flatness of the contact area**
  - Due to the unevenness of surfaces, a thermal interface material needs to be supplied between heat source and heat sink. However, such materials have a rather low thermal conductivity (<10 K/W). Hence these materials should be as thin as possible. On the other hand, they need to fill out the space between heat source and heat sink. Therefore, the unevenness of the heat sink should be as low as possible. In addition, the particle size of the interface material must fit to the roughness of the module and the heat sink surfaces. Too large particle will unnecessarily increase the thickness of the interface layer and hence will increase the thermal resistance. Too small particles will not provide a good contact between the two surfaces and will lead to a higher thermal resistance as well.
- **Mounting pressure**
  - The higher the mounting pressure the better the interface material disperses and excessive interface material squeezes out resulting in a thinner interface layer with a lower thermal resistance.

7.5.2.2 Heat transfer within the heat sink

The heat transfer within the heat sink is mainly determined by:

- **Heat sink material**
  - The material needs to be a good thermal conductor. Most heat sinks are made of aluminum ($\lambda \approx 200$ W/ (m*K)). Copper is heavier and more expensive but also nearly twice as efficient ($\lambda \approx 400$ W/ (m*K)).
- **Fin thickness**
  - If the fins are too thin, the thermal resistance from heat source to fin is too high and the efficiency of the fin decreases. Hence it does not make sense to make the fins as thin as possible in order to spent more fins and therefore to increase the surface area.

7.5.2.3 Heat transfer from heat sink surface to ambient

The heat transfers to the ambient mainly by convection. The corresponding thermal resistance is defined as

$$R_{th,conv} = \frac{1}{\alpha \cdot A} \qquad (18)$$

Where α is the heat transfer coefficient and A is the surface area.

Hence there are two important parameters:

- **Surface area:** Heat sinks require a huge surface area in order to easily transfer the heat to the ambient. However, as the heat source is assumed to be concentrated at a point and not uniformly distributed, the total thermal resistance of a heat sink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in section 7.5.2.2.

- **Heat transfer coefficient (aerodynamics):** This coefficient is strongly depending on the air flow velocity as shown in Figure 24. If there is no externally induced flow one speaks of natural convection, otherwise it's forced convection. Heat sinks with very small fin spacing do not allow a good air flow. If a fan is used, the fin gap may be lower than for natural convection as the fan forces the air through the space between the fins.

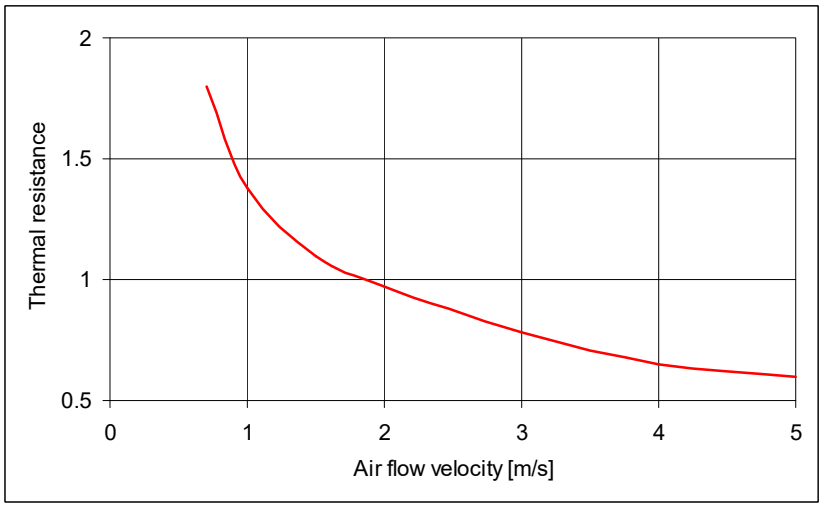


Figure 24 Thermal resistance as a function of the air flow velocity

Furthermore, in case of natural convection the heat sink efficiency depends on the temperature difference of heat sink and ambient (i.e. on the dissipated power). Some manufacturers, like Aavid thermalloy, provide a correction table which allows calculating the thermal resistance depending on the temperature difference. Figure 25 shows the heat sink efficiency degradation for natural convection as provided in [6]. Please note that the thermal resistance is 25% higher at 30 W than at 75 W.

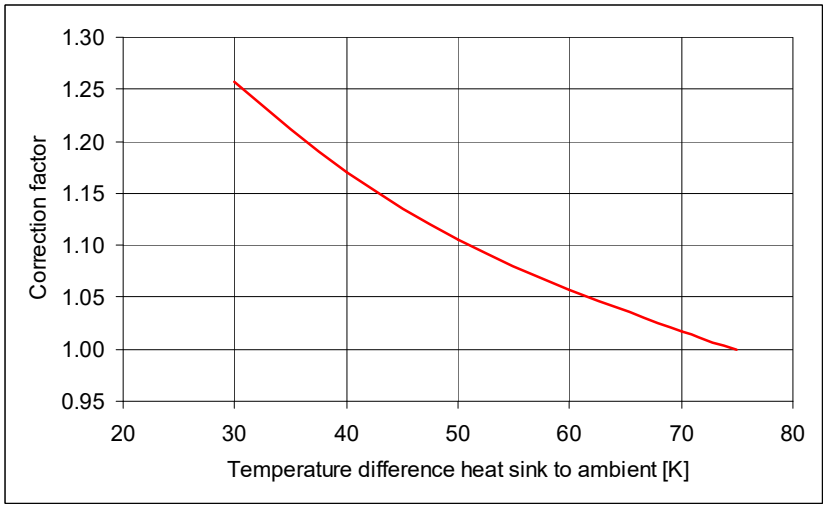


Figure 25 Correction factors for temperature

The positioning of the heat sink plays also an important role for the aerodynamics. In case of natural convection the best mounting attitude is with vertical fins as the heated air tends to move upwards due to buoyancy. Furthermore, one should make sure that there are no significant obstructions impeding the air flow.

Radiation occurs as well supporting the heat transfer from heat sink to ambient. In order to the increase radiated heat one can use anodized heat sinks with a black surface. However, this decreases the thermal

resistance of the heat sink only by a few percent in case of natural convection. Radiated heat is negligible in case of forced convection. Hence blank heat sinks can be used if there isn't a fan used with the heat sink.

The discussions in this section clearly show that there cannot be a single thermal resistance value assigned to a certain heat sink.

7.5.3 Selecting a heat sink

Unfortunately there are no straightforward recipes for selecting heat sinks. Finding a sufficient heat sink will include an iterative process of choosing and testing heat sinks. In order to get a first rough estimation of the required volume of the heat sink, one can start with estimated volumetric thermal resistances as given in Table 17 (Taken from [5]). This table gives only a first clue as the actual resistance may vary depending on many parameters like actual dimensions, type and orientation etc.

Table 17 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric resistance [cm^3 °C/W]
Natural convection	500 ~ 800
1.0	150 ~ 250
2.5	80 ~ 150
5.0	50 ~ 80

One can roughly assume that the volume of a heat sink needs to be quadrupled in order to half it's thermal resistance. This gives a hint whether natural convection is sufficient for the available space or forced convection is required.

In order to get an optimized heat sink for a given application, one needs to contact heat sink manufacturers or consultants. Further hints and references can be found in [5].

When contacting heat sink manufacturers in order to find a suited heat sink, please take care under which conditions the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heat sink. Also take care that the fin spacing is optimized for the corresponding flow conditions.

8 Heat sink mounting and handling guidelines

8.1 Heat sink mounting

8.1.1 General guidelines

An adequate heat sinking capability of the CIPOS™ Mini interleaved PFC IPM is only achievable, if it is suitably mounted. This is the fundamental requirement in order to meet the electrical and thermal performance of the module. The following general points should be observed when mounting CIPOS™ Mini interleaved PFC IPM on a heat sink. Verify the following points related to the heat sink:

a) There must be no burrs on aluminum or copper heat sinks
b) Screw holes must be countersunk
c) There must be no unevenness or scratches in the heat sink
d) The surface of the module must be completely in contact with the heat sink
e) There must be no oxidation nor stain or burrs on the heat sink surface

To improve the thermal conductivity, apply silicone grease to the contact surface between the CIPOS™ Mini interleaved PFC IPM and heat sink. Spread a homogenous layer of silicone grease with a thickness of 100 µm over the CIPOS™ Mini interleaved PFC IPM substrate surface. Non-planar surfaces of the heat sink may require a thicker layer of thermal grease. Please refer here to the specifications of the heat sink manufacturer. It is important to note here, that the heat sink covers the complete backside of the module. There may be different functional behavior, if there is a portion of the backside of the module, which is not in contact with the heat sink.

To prevent a loss of heat dissipation effect due to warping of the substrate, tighten down the mounting screws gradually and sequentially while maintaining a left/right balance in pressure applied.

It must be assured by design of the application PCB, that the plane of the back side of the module and the plane of the heat sink are parallel in order to achieve minimal tensions of the package and an optimal contact of the module with the heat sink. Please refer to the mechanical specifications of the module given in the datasheets.

It is basics of good engineering to verify the function and thermal conditions by means of detailed measurements. It is best to use a final application inverter system, which is assembled with the final production process. This helps to achieve high quality applications.

8.1.1.1 Recommended tightening torque

As shown in Table 18, the tightening torque of M3 screws is specified for typically 0.69 N·m and maximum 0.78 N·m. The screw holes must be centered to the screw openings of the mold compound, so that the screws do not contact the mold compound. If an insulating sheet is used, use a sheet larger than the CIPOS™ Mini interleaved PFC IPM, and it should be aligned accurately when attached. It is important to ensure, that no air is enclosed by the insulating sheet. Generally speaking, insulating sheets are used in the following cases:

- When the ability of withstanding primary and secondary voltages is required, to achieve required safety standard against a hazardous situation
- When the CIPOS™ Mini interleaved PFC IPM must be insulated from the heat sink
- When measuring the module, to reduce radiated noise or eliminate other signal related problems

Table 18 Mechanical characteristics and ratings

Item	Condition	Package type	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	DCB	0.49	-	0.78	N·m
Device flatness	(Note Figure 26)		-50	-	+100	µm
Heat sink flatness	(Note Figure 27)		0	-	+100	µm
Weight		DCB	-	6.58	-	g

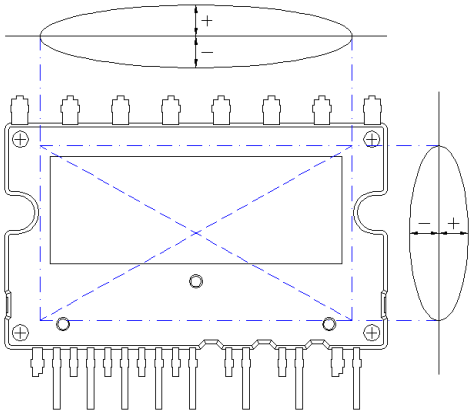


Figure 26 Device flatness measurement position

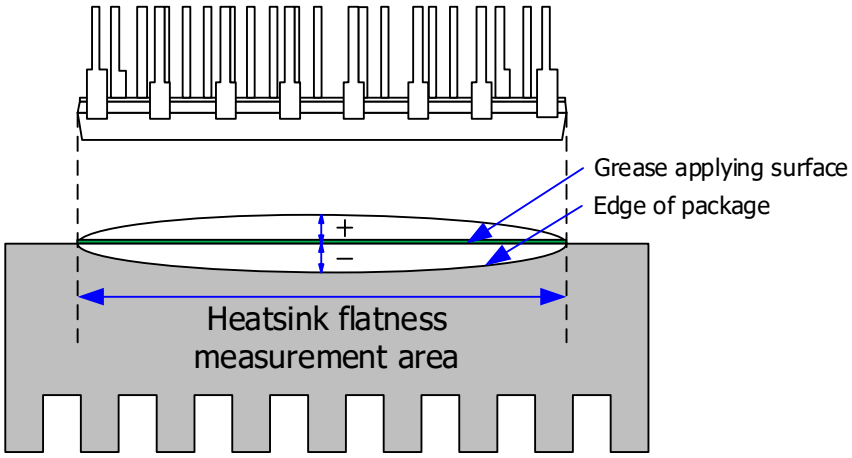


Figure 27 Heat sink flatness measurement position

8.1.1.2 Screw tightening to heat sink

The tightening of the screws is the main process of attaching the module to the heat sink. It is assumed that an interface pad is attached to the heat sink surface, which extends to the edge of the module and is located for the fixing holes. It is recommended that M3 fixing screws are used in conjunction with a spring washer and a plain washer. The spring washer must be assembled between the plain washer and the screw head. The screw torque must be monitored by the fixing tool.

Tightening process:

- Align module with the fixing holes
- Insert screw A with washers to touch only position (pre-screwing)
- Insert screw B with washers (pre-screwing)
- Tighten screw A to final torque
- Tighten screw B to final torque

Note: The pre-screwing torque is set to 20~30% of maximum torque rating.

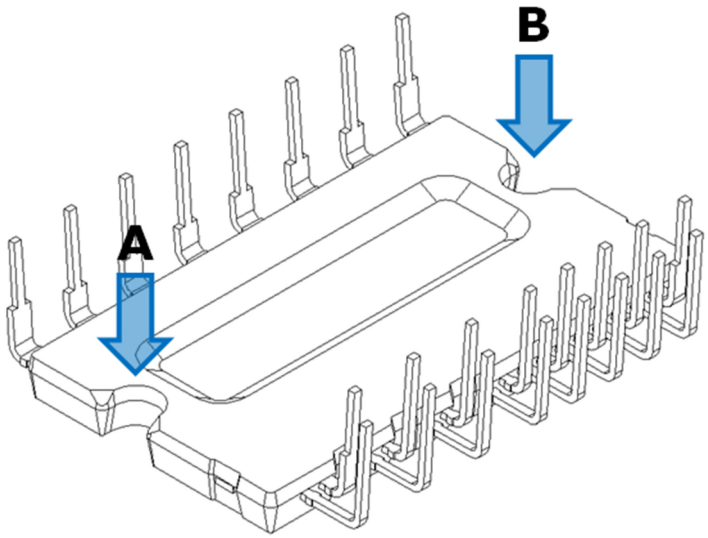


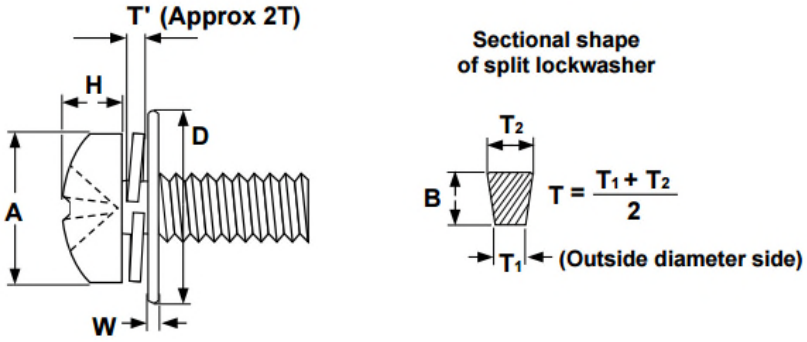
Figure 28 Reommended screw tightening order : Pre-screwing A → B, Final screwing A → B

8.1.1.3 Mounting screw

When we attach module to heat sink, we recommend M3 SEMS screw (JIS B1256/JIS B1188) as Table 19.

Table 19 Recommended screw specification (Typical)

Screw dimensions				Flat washer		Spring washer	
Size	Thread pitch	A Head diameter	H Head height	D Outer diameter	W Thickness	D1 Outside diameter	B x T
M3	0.5	5.2	2.0	7.8	0.58	5	1.1 x 0.7



8.1.2 Recommended heat sink shape and system mechanical structure

A shock or vibration through PCB or heat sink might cause the crack of the package mounted on the heat sink. To avoid a broken or cracked package and to endure shock or vibration through PCB or heat sink, a heat sink shape is recommended as shown in Figure 29. The heat sink needs to be fixed to the PCB with screws or eyelets. In mass production stage, the process sequence for system assembly in terms of device soldering on PCB, heat sink mounting and casing etc., should be taken into account to avoid mechanical stress on the device pins, package mold compound, heat sink and system enclosure etc.

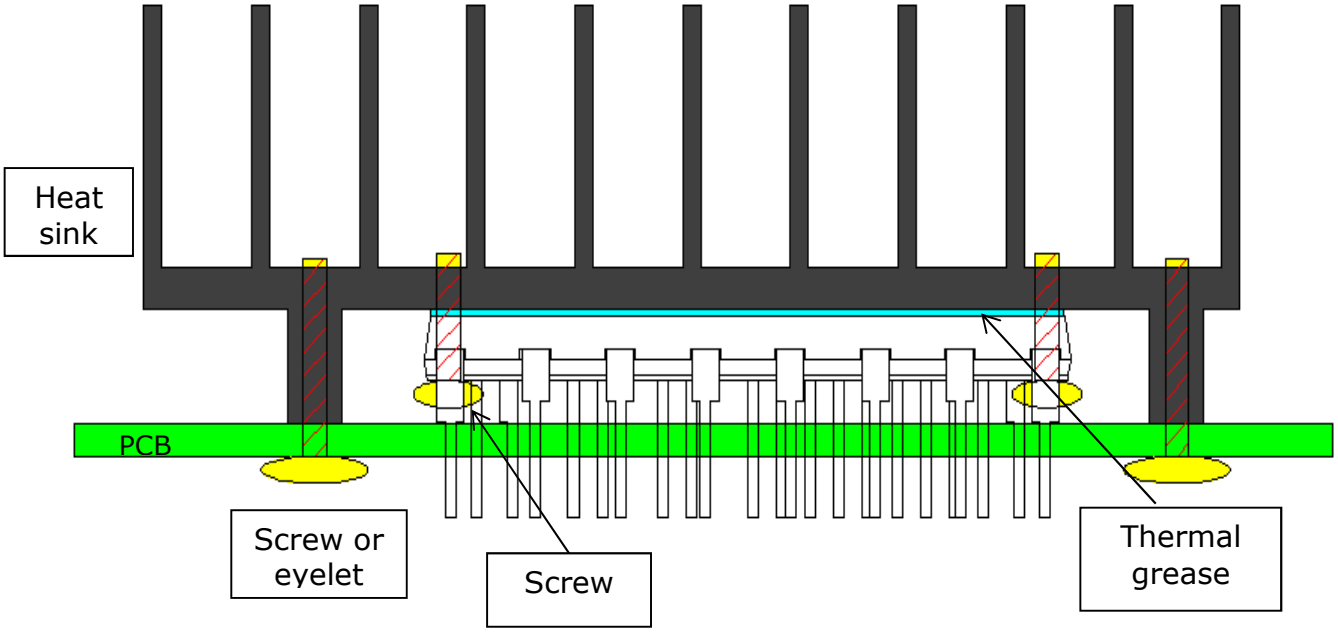


Figure 29 Recommended heat sink shape

8.2 Handling guide line

When installing a module to a heat sink, excessive uneven tightening force might apply stress to inside chips, which will lead to a broken or degradation of the device. An example of recommended fastening order is shown in Figure 28.

- Do not over torque when mounting the screws. Excessive mounting torque may cause damage to module hole as well as damage to the screw and heat sink.
- Avoid one-side tightening stress. Uneven mounting can cause the module hole to be damaged.

To get effective heat dissipation, it is necessary to enlarge the contact area as much as possible, which minimizes the contact thermal resistance.

Properly, apply thermal conductive grease over the contact surface between the module and the heat sink, which is also useful for preventing the contact surface from corrosion. Furthermore the grease should be with stable quality and long term endurance within wide operating temperature range. Use a torque wrench to tighten to the specified torque rating. Exceeding the maximum torque limitation might cause a module to be damaged or degraded. Pay attention not to have any dirt remaining on the contact surface between the module and the heat sink. All equipment, which is used to handle or mount CIPOS™ Mini interleaved PFC IPM must comply with the relevant ESD standards. This includes e.g. transportation, storage and assembly. The module itself is an ESD sensitive device. It may therefore be damaged in case of ESD shocks.

Don’t shake and handle by grabbing only the heat sink, and especially don’t shock to PCB by grabbing only the heat sink. That might cause package cracking or a broken package.

8.3 Storage guideline

8.3.1 Recommended storage conditions

Temperature: 5 ~ 35℃

Relative humidity: 45 ~ 75%

- Avoid leaving the CIPOS™ Mini interleaved PFC IPM exposed to moisture or direct sunlight. Especially, be careful during periods of rain or snow.
- Use storage areas where there is minimal temperature fluctuation.

Rapid temperature changes can cause moisture condensation on the stored CIPOS™ Mini interleaved PFC IPM, resulting in lead oxidation or corrosion as a result, leading to degraded solderability.

- Do not allow the CIPOS™ Mini interleaved PFC IPM to be exposed to corrosive gasses or dusty conditions.
- Do not allow excessive external forces or loads to be applied to the CIPOS™ Mini interleaved PFC IPM while they are in storage.

9 References

1. [1] Thomas Kimmer, Erich Griebl: “TRENCHSTOP™ 5: A new application specific IGBT series”, PCIM Europe 2012, Nuremberg, Germany.
2. [2] “650V Rapid Diode for Industrial Applications”, Application note, Infineon Technologies AG V2.0, Jul. 2014
3. [3] R. Keggenhoff, Z.Liang, Andre Arens, P. Kanschat, R. Rudolf. ‘Novel SOI Driver for Low Power Drive Applications’, Power Systems Design Europe Nov. 2005
4. [4] S Park, J Cho, H Kwon, J Lee, D Chung: “A Compact Intelligent Power Module with High Thermal Performance for up to 4kW Power Motor Drives”, PCIM Europe 2014, Nuremberg, Germany.
5. [5] S. Lee, “How to select a heat sink”, Electronics Coolings, Vol.1, No.1, June 1995
6. [6] Aavid Thermalloy, **http://www.aavidthermalloy.com/technical/correct.shtml**
7. [7] Alexander H.Craig, Ronald H Randall, Joe Yedinak: “Ghost Failures in boost topology circuits explained through third quadrant operation”, APEC, 2000. Fifteenth Annual IEEE
8. [8] Infineon Power Semitech: Design Guide for Boost Type CCM PFC with ICE2PCSxx, 2008
9. [9] CIPOSIM - CIPOS™ Mini Simulator, Infineon Technologies Power Semitech, 2009

Revision History

Major changes since the last revision

Page or Reference	Description of change
V 1.0	First release
V 1.1	Updated Table 19

Other Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-11-11
Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

AN2016-25 Application Note

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

Please note that this product is not qualified according to the AEC Q100 or AEC Q101 documents of the Automotive Electronics Council.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.