Control Integrated POwer System (CIPOS™)

2-Phase Interleaved PFC IPM (IFCMxxT65yz) Reference Board

About this document

Scope and Purpose

The scope of this application note is to describe the product reference board of the CIPOS™ Mini 2-phase interleaved PFC IPM and the basic requirements for operating the product in a recommended mode. Environmental conditions were considered in the design of the reference board. The design was tested as described in this document but not qualified regarding safety requirements or manufacturing and operation over the whole operating temperature range or lifetime. The boards provided by Infineon are subject to functional testing only.

Reference boards are not subject to the same procedures as regular products regarding Returned Material Analysis (RMA), Process Change notification (PCN) and Product Discontinuation (PD). Reference boards are intended to be used under laboratory conditions by specialists only.

Intended Audience

Power electronics engineers who want to evaluate the CIPOS™ Mini 2-phase interleaved PFC IPM.

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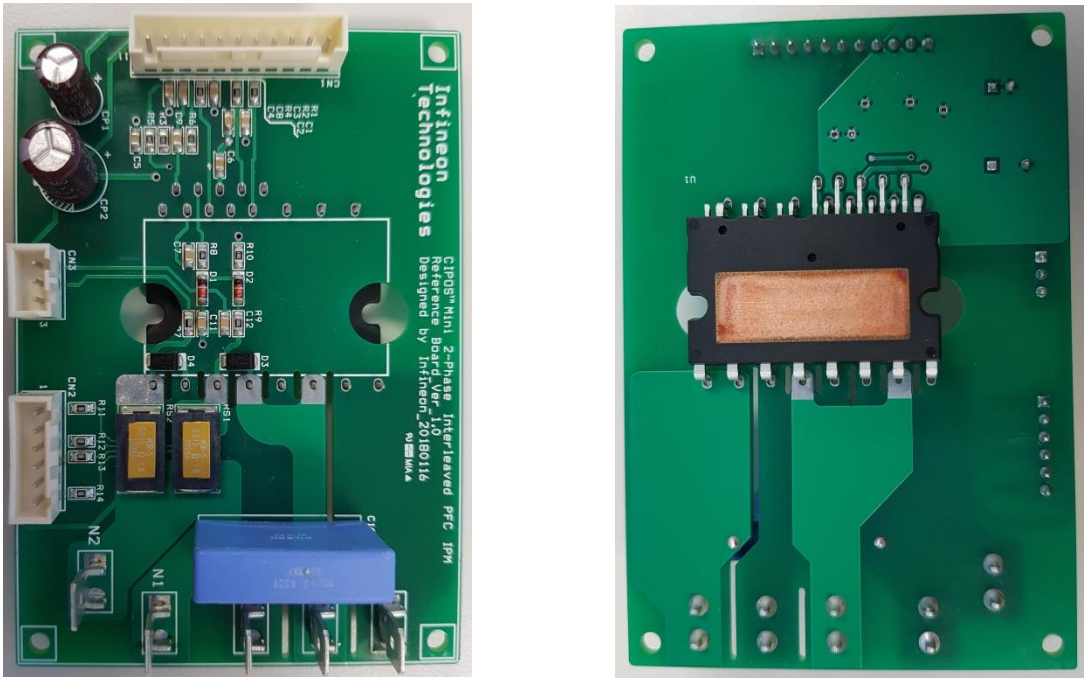
1 Introduction

This reference board is composed of IFCM20T65GD, minimum peripheral components and two current sensing resistors. It is designed for customers to evaluate the performance of the CIPOS™ Mini 2-phase interleaved PFC IPM with simple connections of control signals and power wires. Figure 1 shows the external view of the reference board.

This application note also describes how to design key parameters and PCB layout.



Top view Bottom view

Figure 1 Reference board pictures

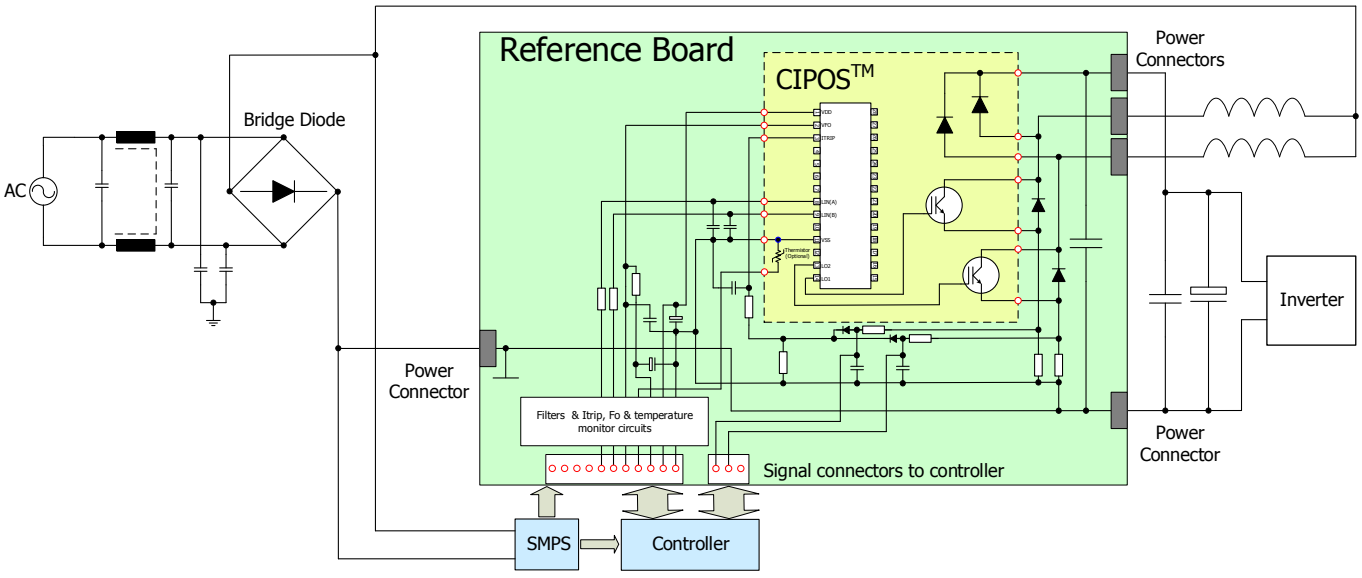


Figure 2 Application example

2 Schematic

Figure 3 shows a circuitry of the reference board.

The reference board consists of interface circuit, snubber capacitor, Over Current (OC) protection circuit, fault output circuit, current sensing resistors and passive parts etc.

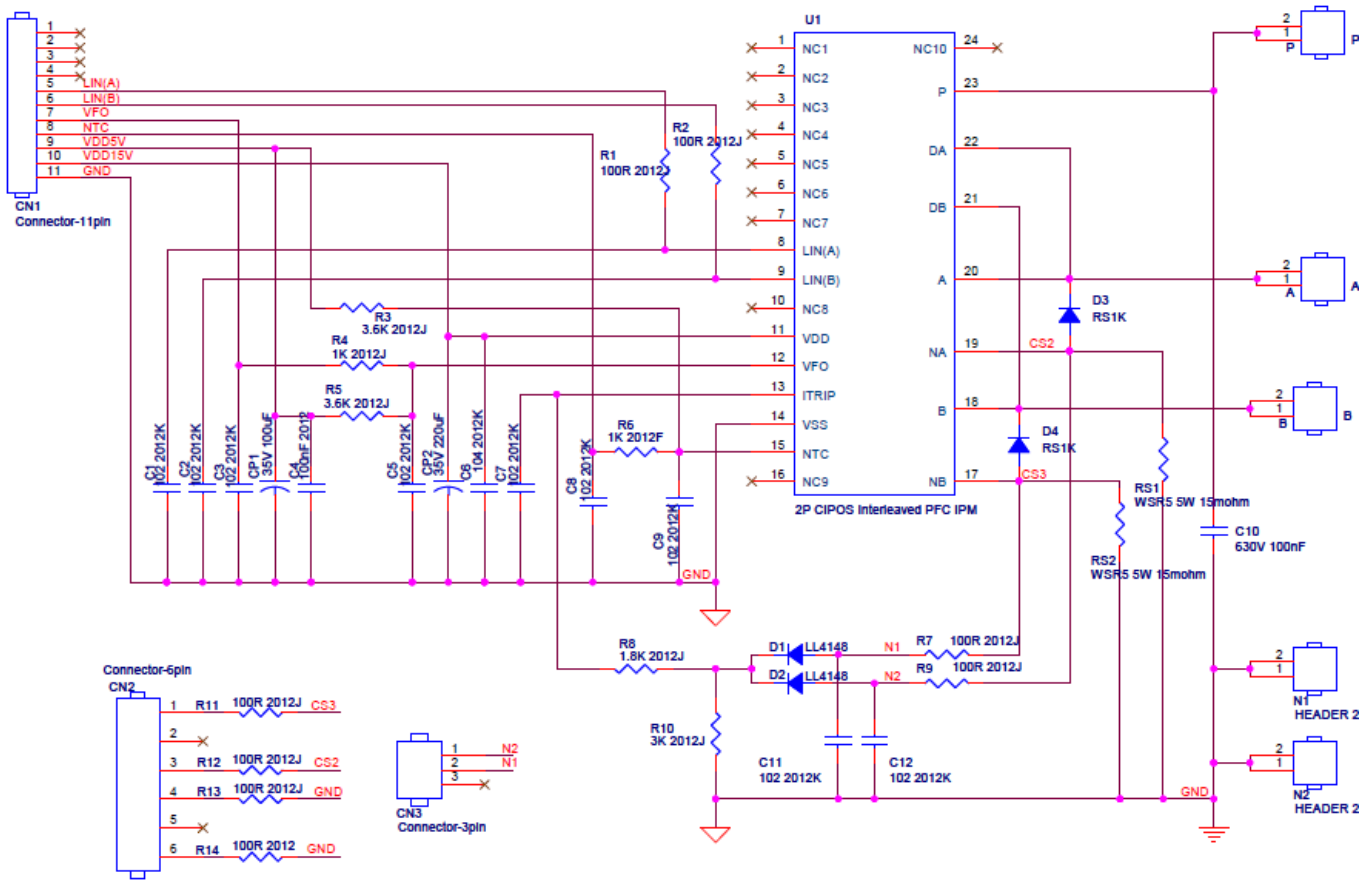


Figure 3 Circuit of the reference board

Note: The “VDD5V” on the CN1 Connector 11 pin 9 denotes the control signal supply voltage such as 5V or 3.3V

3 External Connection

3.1 Signal Connector

Table 1 Pin description of the signal connector (CN1, 11-pin, 2.5mm pin pitch)

Pin No.	Name	Description
1 ~ 4	NC	No connection
5	LIN(A)	Control signal input for phase A IGBT
6	LIN(B)	Control signal input for phase B IGBT
7	VFO	Fault output signal
8	NTC	Temperature monitor output signal
9	VDD5V	External 5V or 3.3V supply for control signal
10	VDD15V	External 15V supply for module power
11	GND	Ground

3.2 Current Sensing Connector

Table 2 Pin description of the current sensing connector (CN2, 6-pin, 2.5mm pin pitch)

Pin No.	Name	Description
1	CS3	Current sensing signal of phase B IGBT
3	CS2	Current sensing signal of phase A IGBT
4, 6	GND	Differential ground of phase A & B for current sensing
2, 5	NC	No connection

3.3 ITRIP Connector

Table 3 Pin description of the ITRIP connector (CN3, 3-pin, 2.5mm pin pitch)

Pin No.	Name	Description
1	N2	Current sensing signal of phase A
2	N1	Current sensing signal of phase B
3	NC	No connection

3.4 Power Terminals

Table 4 Pin description of power terminals

Terminal No.	Name	Desctiption
P	P	Cathode of PFC diode
A	A	Collector of phase A IGBT
B	B	Collector of phase B IGBT
N1, N2	GND	Ground

4 Key Parameter Setting

4.1 Circuit of Input Signals (LINx)

The input signals are compatible with either TTL or CMOS levels. The logic level can go down to 3.3V. The maximum input voltage of the input signal pin is clamped to 10.5V by the internal Zener diode. However the recommended voltage range of input voltage is up to 5V. The input signals LINx are active high.

These pins have an internal pull-down structure with a pull-down resistor, which is nominal 5kΩ. The input noise filter inside the CIPOS™ Mini interleaved PFC IPM suppresses short pulses and prevents a false IGBT driving from an unintentional operation. The input noise filter time (t_{FLIN}) is typically 270ns. This means that the input signal must stay on more than 270ns so that the driver IC detects the normal PWM input for a correct IGBT driving. CIPOS™ Mini interleaved PFC IPM can be connected directly to the controller without an external input RC filter due to the internal pull down resistor and input noise filter, as shown in Figure 4.

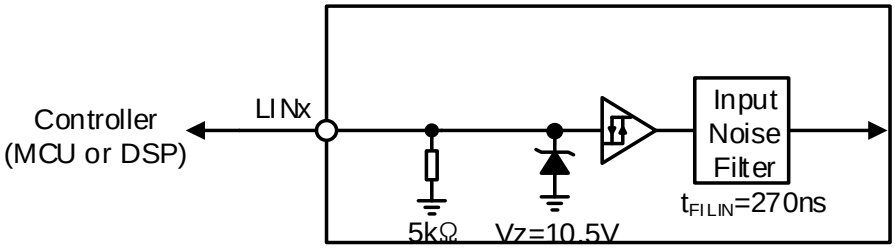


Figure 4 Internal pull-down resistor and input noise filter on input signal pin

4.2 Over Current Protection

Over Current (OC) protection level is decided by ITRIP positive going threshold voltage ($V_{IT,TH+}$) and current sensing resistance. When the ITRIP voltage exceeds $V_{IT,TH+}$, the module turns off all 2 IGBTs and the fault flag is activated during fault-output duration time, typically 65µs.

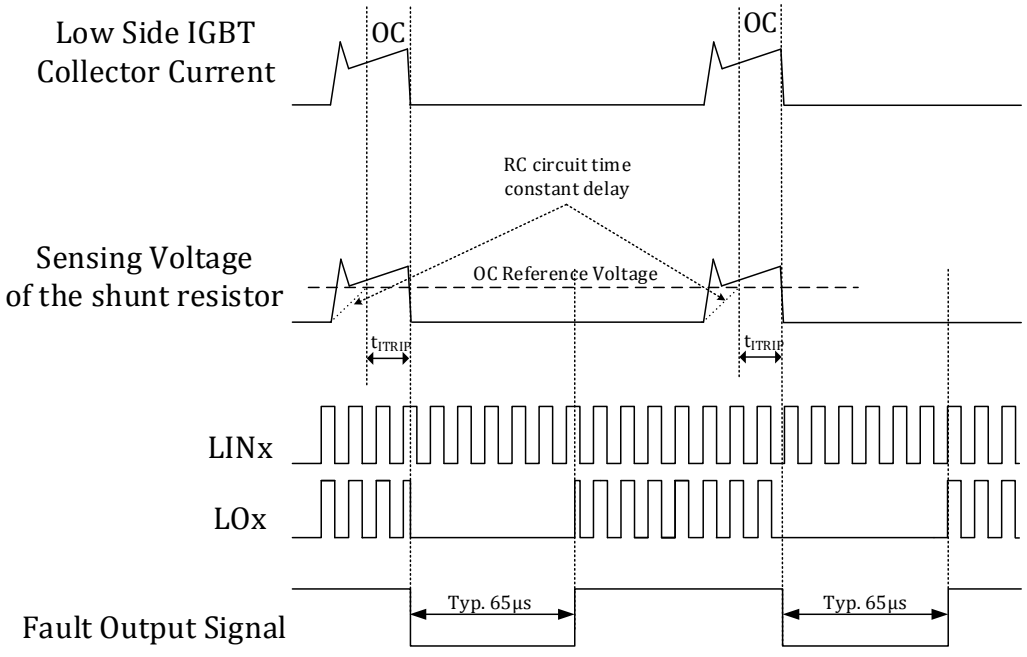


Figure 5 Timing chart of OC protection

4.2.1 Current Sensing Resistor Selection

The value of the current sensing resistor can be calculated with the following equation.

$$R_{SH} = \frac{V_{IT,TH+} + V_{FILTER,DIODE\,DROP}}{I_{OC}}$$

Where,

- R_{SH} : current sensing resistor value
- $V_{IT,TH+}$: ITRIP positive going threshold voltage, typ. 0.47V
- $V_{FILTER,\,DIODEDROP}$: voltage drop from R_{SH} to ITRIP by ORing diode, typ. 0.62V (LL4148, I_F=5mA, T_J=25°C)
- I_{OC} : over current level

A maximum value of the OC protection level should be set less than the maximum peak output current in the datasheet absolute maximum ratings while taking into consideration the tolerance of the current sensing resistor.

For example, the maximum peak output current of the IFCM20T65GD is $30A_{peak}$,

$$R_{SH(min)} = \frac{0.47V + 0.62V}{30A} = \frac{1.09V}{30A} = 0.036\Omega$$

So the recommended value of the current sensing resistor should be higher than 36mΩ for IFCM20T65GD.

In order to calculate the power rating of the current sensing resistor, the below items has to be taken into account.

- Maximum load current of the 2-phase interleaved PFC IPM (I_{RMS})
- Current sensing resistor value at T_C=25°C (R_{SH})
- Power derating ratio of the current sensing resistor at T_{SH}=100°C
- Safety margin

And the power rating can be calculated with the equation below.

$$P_{SH} = \frac{I_{RMS}^{\,2} \times R_{SH} \times \text{Safety margin}}{\text{Derating ratio}}$$

For example, in case of IFCM20T65GD and R_{SH}=36mΩ,

- Max. load current of the 2-phase interleaved PFC IPM (I_{RMS}) : $7A_{RMS}$
- Current sensing resistor value at Tc=25°C (R_{SH}) : 0.036Ω
- Power derating ratio of the current sensing resistor at T_{SH}=100°C : 80%
- Safety margin : 30%

$$P_{SH} = \frac{7A^2 \times 0.036\Omega \times 130\%}{80\%} = 2.87W$$

So the proper power rating of the current sensing resistor is recommended as more than 3W.

Based on the equation, condition and calculation method above, some example values of minimum current sensing resistance and required resistor power rating are introduced as shown in below Table 5 for CIPOS™ Mini 2-phase interleaved PFC IPM products. When choosing a proper current sensing resistance and its power rating, an accurate OC protection level in the application setting should be taken into account for a correct over current detection.

Table 5 Maximum peak current, shunt resistor value and required power rating

Product	Maximum Peak Current	Minimum Shunt Resistance, R_{SH}	Minimum Shunt Resistor Power, P_{SH}
IFCM20T65GD	30A	36mΩ	3.0W
IFCM30T65GD	40A	27mΩ	4.5W

4.2.2 Delay Time

The RC filter is necessary in the over current sensing circuit to prevent malfunction of OC protection caused by noise. The RC time constant is determined by considering the noise duration and safety operation capability of the IGBT.

When the sensing voltage on shunt resistor exceeds the ITRIP positive going threshold ($V_{IT,TH+}$), this voltage is applied to the ITRIP pin of CIPOS™ Mini via the RC filter. Table 6 shows the specification of the OC protection reference level. The filter delay time (t_{FILTER}) that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is caused by below equation (1), (2).

$$V_{IT,TH+} = R_{SH} \cdot I_C \cdot \left(1 - \frac{1}{e^{\frac{t_{Filter}}{\tau}}}\right) \quad (1)$$

$$t_{Filter} = -\tau \cdot ln\left(1 - \frac{V_{IT,TH+}}{R_{SH} \cdot I_C}\right) \quad (2)$$

Where, $V_{IT,TH+}$ is the ITRIP pin input voltage, I_C is the peak current, R_{SH} is the shunt resistor value and τ is the RC time constant. In addition there is a shutdown propagation delay of Itrip (t_{ITRIP}). In addition there is a shutdown propagation delay of Itrip (t_{ITRIP}). Please refer to Table 7.

Table 6 Specification of OC protection reference level '$V_{IT,TH+}$'

Item	Min.	Typ.	Max.	Unit
ITRIP positive going threshold $V_{IT,TH+}$	0.40	0.47	0.54	V

Table 7 Shut down propagation delay

Item		Condition	Min.	Typ.	Max.	Unit
Shut down propagation delay (t_{ITRIP})	IFCM30T65GD	I_{out} =20A, from $V_{IT,TH+}$to 10% I_{out}	-	1420	-	ns
	IFCM20T65GD	I_{out} =15A, from $V_{IT,TH+}$to 10% I_{out}	-	1350	-	

Therefore, the total delay time from the occurrence of the OC event to the shut down of the IGBT gate becomes:

$$t_{Total} = t_{Filter} + t_{ITRIP}$$

The shut down propagation delay is in inverse proportion to the current range. Therefore the t_{ITRIP} will be shorter with a higher current condition, comparing to the current condition in the Table 7. The total delay must be less than 5µs of the short circuit withstand time (t_{SC}), which is specified in the datasheet. Thus, the RC time constant should be set in the range of 1~2µs. A recommended RC filter values are 1.8kΩ R8, 100Ω R7 & R9, 1nF C7 and 1nF C11 & C12.

4.3 Temperature Monitor and Thermal Protection

In case of the CIPOS™ Mini 2-phase interleaved PFC IPM, a built-in thermistor (85kΩ at 25°C) is connected between NTC and VSS pins. The typical application circuit looks like Figure 6 where the NTC pin is used for thermistor temperature sensing and the VFO pin is used for fault flag. The voltage of the NTC pin decreases as the thermistor temperature increases because the thermistor is an NTC (Negative Temperature Coefficient) type and it is connected to the external pull-up resistor. Note that the voltage variation of the NTC pin, which is generated by the thermistor temperature change, should be always inside the A/D converter input range of the micro controller. In this reference board, the pull-up resistor is set to 3.6kΩ so that the NTC voltage becomes 2.95V and 1.95V respectively for 5V and 3.3V control voltage (VDD5V) when the thermistor temperature is 100°C, as shown in Figure 7.

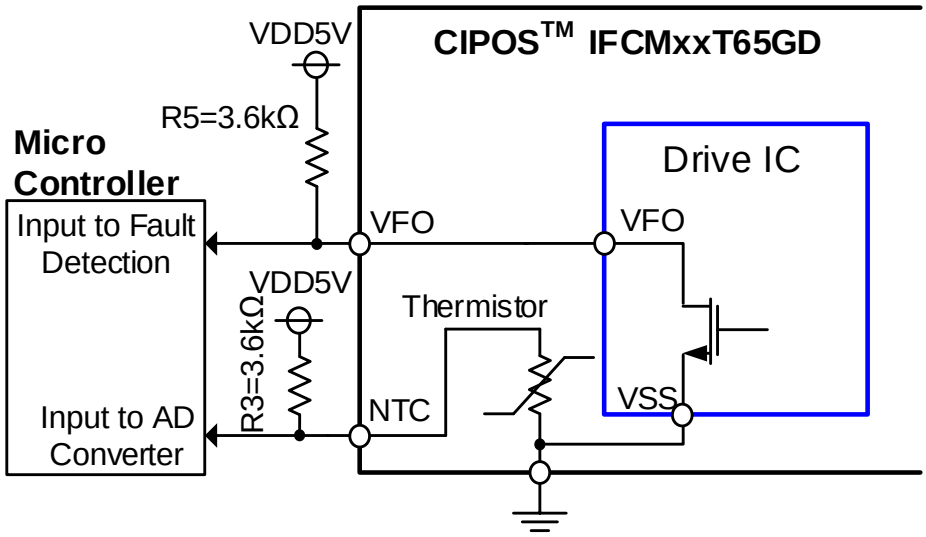


Figure 6 Temperature monitor with built in thermistor and pull up resistor

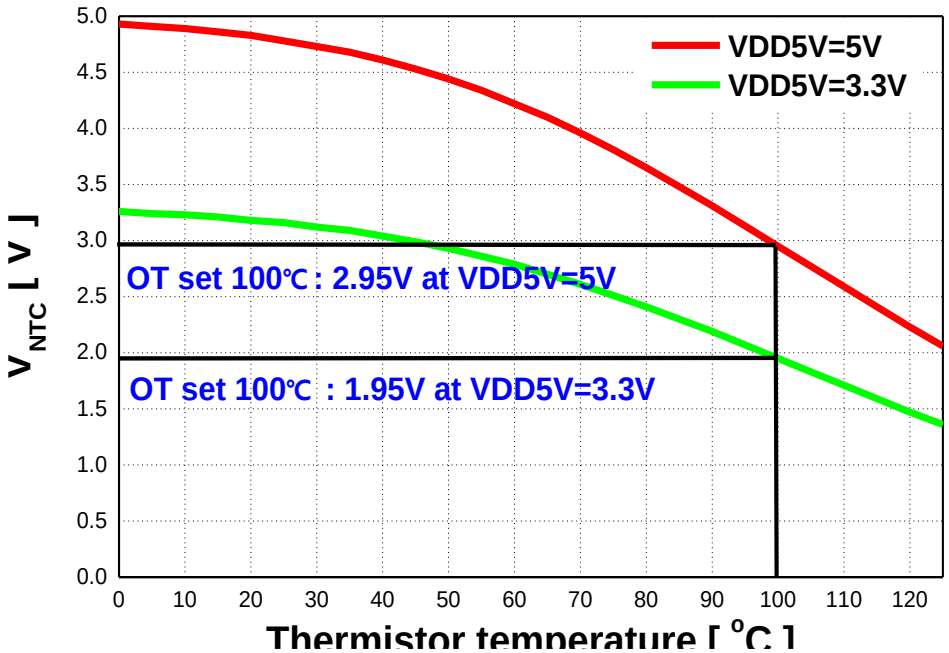


Figure 7 Voltage variation of the NTC pin along with the NTC thermistor temperature change

5 Boost PFC Circuit Setting

5.1 Target Specification

Table 8 below shows a target specification example for the CIPOS™ Mini 2-phase interleaved PFC IPM reference board.

Table 8 Design parameters for the proposed target specification

Design parameter	Parameter name	Value
Minimum input voltage	Vin_min	85VAC
Maximum input voltage	Vin_max	265VAC
Line frequency	f_L	50Hz
Output voltage	Vout	390VDC
Minimum output voltage	Vout_min	250VDC
Output current	Iout	10.26A
Output power	Pout	4000W
Efficiency	η	>90% at full load
PFC switching frequency	f_{SW}	40kHz
Maximum ambient temperature around PFC	T_{Amax}	70°C

5.2 Boost Inductor

The maximum input RMS current, I_{in_RMS}, is needed to obtain 4000W output power P_{out} with 85V minimum AC input voltage V_{in_min}. The equation below shows the calculation example for a maximum input RMS current.

$$I_{in\_RMS} = \frac{P_{out}}{V_{in\_min} \times \eta} = \frac{4000W}{85V \times 90\%} = 52.29A$$

The sinusoidal peak value of AC current, I_{in_pk}, is calculated as below.

$$I_{in\_pk} = \sqrt{2} \times I_{in\_RMS} = \sqrt{2} \times 52.29A = 73.95A$$

The I_{HF} represents a high frequency ripple current peak to peak on the boost inductor. It is related to maximum input power and minimum input voltage as below.

$$I_{HF} = k \times \sqrt{2} \times \frac{P_{in\_max\_PH}}{V_{in\_min}}$$

$$P_{in\_max\_PH} = \frac{P_{out\_max}}{\eta \times No\_of\_phase}$$

The “k” is a ratio of inductor ripple current based on the inductor average current. It must be kept reasonably small, and it is usually optimized in the range of 15% to 25% for cost effective design based on the current magnetic component status. For example, if k=22%, then,

$$I_{HF} = k \times \sqrt{2} \times \frac{P_{in\_max\_PH}}{V_{in\_min}} = 22\% \times \sqrt{2} \times \frac{4000W}{90\% \times 2} \times \frac{1}{85V} = 8.13A$$

The peak current passing through the inductor is,

$$I_{in\_peak\_PH} = \frac{I_{in\_peak}}{No\_of\_phase} = \frac{73.95A}{2} = 36.98A$$

$$I_{L\_pk} = I_{in\_peak\_PH} + \frac{I_{HF}}{2} = 36.98A + \frac{8.13A}{2} = 41.05A$$

The on-duty of the transistor switch in a boost converter operating under CCM at minimum AC input RMS voltage is,

$$D_{on} = 1 - \frac{\sqrt{2} \times V_{in\_min}}{V_{out}} = 1 - \frac{\sqrt{2} \times 85V}{390V} = 0.692$$

The boost choke inductor value is,

$$L_{boost} = \frac{D_{on} \times (1 - D_{on}) \times V_{out}}{I_{HF} \times f_{SW}} = \frac{D_{on} \times V_{in\_min} \times \sqrt{2}}{I_{HF} \times f_{SW}}$$

Calculating the equation above with the value of D_{on}=0.692 will generate the L_{boost} value as below.

$$L_{boost} = \frac{D_{on} \times V_{in\_min} \times \sqrt{2}}{I_{HF} \times f_{SW}} = \frac{0.692 \times 85V \times \sqrt{2}}{8.13A \times 40kHz} = 256\mu H$$

The core material of the boost inductor can be either magnetic powder or ferrite. For further detailed design of boost inductor, please refer to the PFC controller related document or appropriate application note.

5.3 Output Capacitor

An output bulk capacitor has to meet the requirement for output double line frequency ripple limit as the equation below. The Vout_ripple is normally defined as lower than 10% of Vout. For example, 3% of 390VDC Vout is around 12V of Vout_ripple. The equation below shows a calculation example of minimum output capacitance.

$$C_{OUT} \geq \frac{I_{OUT}}{2\pi \times f_L \times V_{out\_ripple}} = \frac{10.26A}{2\pi \times 50Hz \times 12V} = 2722\mu F$$

The output capacitor of PFC circuit also has to supply enough energy to the next stage during hold-up time. The 20ms hold-up time is based on the line frequency of 50Hz. The output capacitor value should be higher than the result of the equation below for hold-up time requirement.

$$C_{OUT} \geq \frac{2 \times P_{OUT} \times t_{holdup}}{V_{out}^2 - V_{out\_min}^2} = \frac{2 \times 4000W \times 20ms}{390V^2 - 250V^2} = 1786\mu F$$

Comparing with two output capacitor calculation values above, the 2722µF capacitor can be chosen, but a max. 20% capacitance tolerance should be considered. So around 3300µF capacitor is finally recommended for the output capacitor.

6 Part List

Table 9 Part list (Only for reference. Supplier can be changed.)

Symbol	Components	Description	Supplier
R1, R2	100Ω, 5%, 2012	Filter resistors for LIN(A) and LIN(B) signal input	Walsin
R3	3.6kΩ, 1%, 2012	Pull-up resistor to VDD5V for NTC supply voltage	Walsin
R4	1kΩ, 5%, 2012	Filter resistor for VFO signal output	Walsin
R5	3.6kΩ, 1%, 2012	Pull-up resistor to VDD5V for VFO supply voltage	Walsin
R6	1kΩ, 5%, 2012	Filter resistor for NTC signal output	Walsin
R7, R9	100Ω, 1%, 2012	Filter resistors for current sensing signal input	Walsin
R8	1.8kΩ, 1%, 2012	Filter resistor for current sensing signal input	Walsin
R10	3kΩ, 1%, 2012	Pull-down resistor for current sensing signal input	Walsin
R11 ~ R14	100Ω, 1%, 2012	Series resistors for current sensing signal interface	Walsin
RS1, RS2	Refer to 4.2.1	Shunt resistors for current sensing	Vishay
C1, C2	1nF, 50V, X7R, 10%	Filter capacitors for LIN(A) and LIN(B) signal input	Walsin
C3	1nF, 50V, X7R, 10%	Filter capacitor for VFO signal output	Walsin
CP1	100uF, 35V	Bulk capacitor for VDD5V supply voltage	Samyoung
C4	100nF, 50V, X7R, 10%	Bypass capacitor for VDD5V supply voltage	Walsin
C5	1nF, 50V, X7R, 10%	Bypass capacitor for VFO supply voltage	Walsin
CP2	220uF, 35V	Bulk capacitor for VDD15V supply voltage	Samyoung
C6	100nF, 50V, X7R, 10%	Bypass capacitor for VDD15V supply voltage	Walsin
C7	1nF, 50V, X7R, 10%	Filter capacitor for current sensing signal input	Walsin
C8	1nF, 50V, X7R, 10%	Filter capacitor for NTC signal output	Walsin
C9	1nF, 50V, X7R, 10%	Bypass capacitor for NTC supply voltage	Walsin
C10	0.1uF, 630V	Snubber capacitor to reduce switching noise	Pilkor
C11, C12	1nF, 50V, X7R, 10%	Filter capacitor for current sensing signal input	Walsin
D1, D2	LL4148	ORing diodes for current sensing signal input	Vishay
D3, D4	RS1K	Freewheeling diodes for boost PFC	Vishay
CN1	SMW250-11P	11-pin connector for signal and power supply	Yeonho
CN2	SMW250-6P	6-pin connector for current sensing signal	Yeonho
CN3	SMW250-3P	3-pin connector for current sensing signal	Yeonho
J1 ~ J5	Fasten Tap	Power terminals	KET
U1	IFCM20T65GD	CIPOS™ Mini 2-phase interleaved PFC IPM	Infineon Technologies

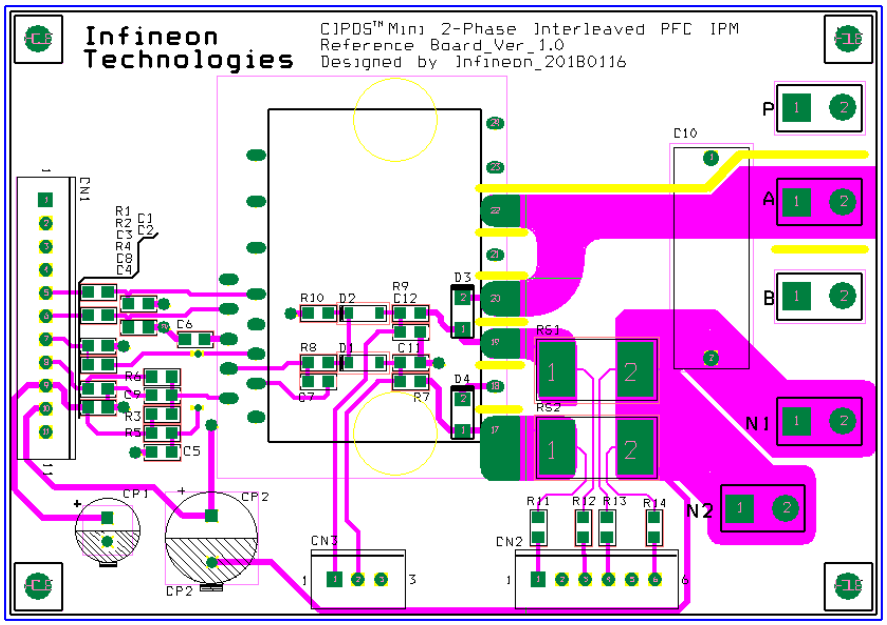
7 PCB Design Guide

In general, there are several issues to be considered when designing a switching power supply application.

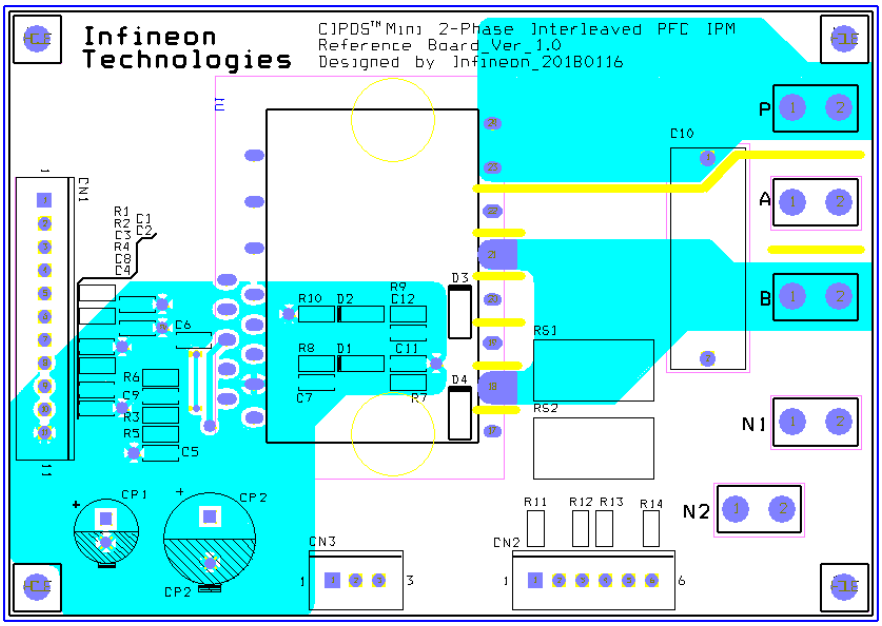
- Low stray inductive connection
- Isolation distance
- Component placement

This chapter will explain about the items above and come up with the solutions for the better layout design.

7.1 Layout of Reference Board



Top view



Bottom view

Figure 8 Layout of reference board for 2-shunt resistors

1. *The connection between emitters of CIPOS™ Mini 2-phase interleaved PFC IPM (NA and NB) and current sensing resistors should be as short and as wide as possible.*
2. *It is recommended that the ground pin of the micro-controller should be directly connected to the VSS pin. Signal ground and power ground should be as short as possible and connected at only one point via the VDD capacitor (C6).*
3. *All of the bypass capacitors should be placed as close to the pins of CIPOS™ Mini 2-phase interleaved PFC IPM as possible.*
4. *The capacitor (C7) for voltage sensing of the current sensing resistor should be placed as close to ITRIP and VSS pins as possible.*
5. *In order to accurately detect the voltage of the current sensing resistor, both sensing and ground patterns should be connected at the pins of the current sensing resistor and should not be overlapped with any patterns for the load current, as shown in Figure 8.*
6. *The snubber capacitor (C10) should be placed as close to the power terminals as possible.*
7. *The PCB routings for power pins such as P, DA, DB, A, NA, B and NB should be placed on both top and bottom layers with vias to allow high current flowing. They have to keep the minimum isolation distance among the power patterns. The distance should be at least over than 2.54mm.*
8. *Note that there are milling profiles in gray lines on the board to keep the isolation distance.*
9. *All components except the CIPOS™ Mini 2-phase interleaved PFC IPM are placed on the top layer.*

8 Peripheral Components Connection

This reference board is composed of IFCM20T65GD, minimum peripheral components and two current sensing resistors. So, in order to operate the reference board by 2-phase interleaved PFC topology, users need to set up additional external system and components such as bridge rectifier, boost inductor, main DC link capacitor, power supply, PFC control system, and resistive load.

Figure 9 is example of system setup for evaluation of the 2-phase interleaved PFC IPM reference board.

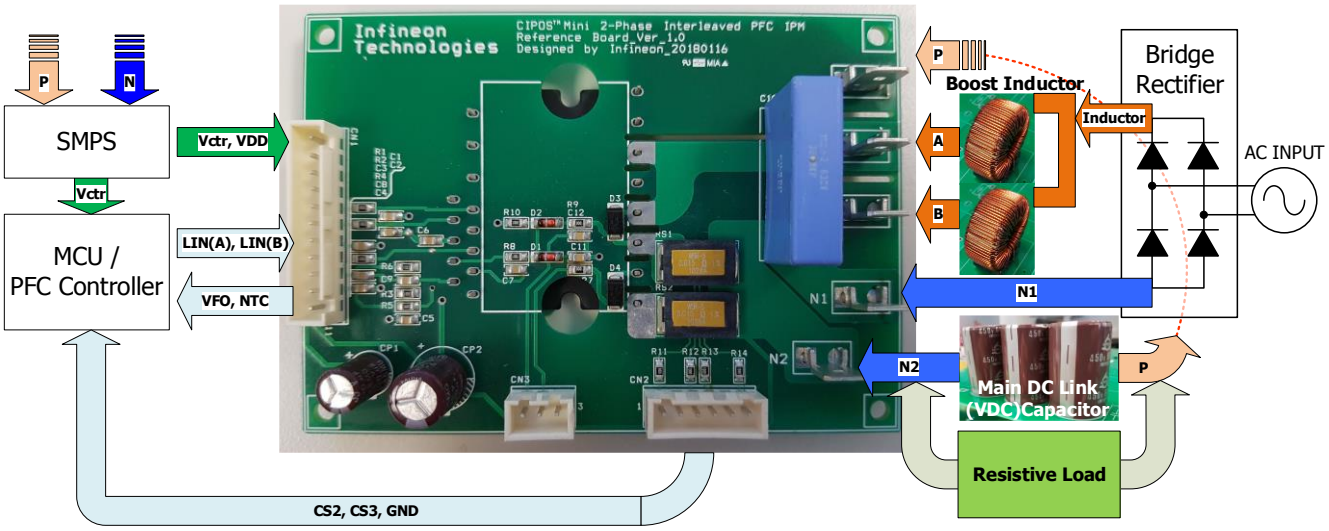


Figure 9 System setup with reference board

9 Evaluation Example of Reference Board

9.1 Evaluation Results

Table 1 Evaluation Setup [DUT: IFCM20T65GD]

Design parameter	Parameter name	Value
Input voltage	V_{in}	220 [Vac]
Line frequency	f_L	60 [Hz]
Output voltage	V_{out}	400 [VDC]
Output power	P_{out}	3500 [W]
Main boost inductance	L_{boost}	100 [µH]
PFC switching frequency	f_{SW}	40 [kHz]
Cooling Method	-	Convection cooling
Load	-	Resistive load

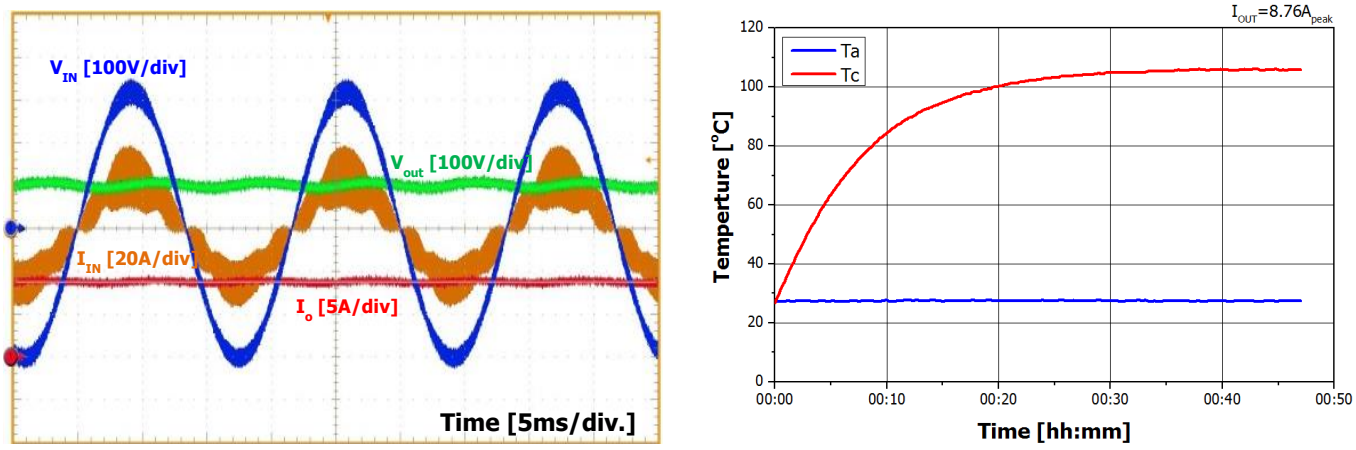


Figure 10 Operating waveform (CH1: Input voltage, CH2: Input current, CH3: Output voltage, CH4: Output current) and Case temperature (T_C)

Input Conditions			Output Conditions			Power Factor	Efficiency [%]	Case Temperature [°C]
Voltage [Vac] / Frequency [Hz]	Current [Arms]	Power [kW]	Voltage [Vrms]	Current [Arms]	Power [kW]			
220/60	17.3	3.8	400	8.76	3.5	0.99	92.1	106.0

10 Reference

[1] Infineon Power Semitech: CIPOS™ IFCM20T65GD; Datasheet Ver1.0; Infineon Power Semitech, 2016

[2] Infineon Power Semitech: Design Guide for Boost Type CCM PFC with ICE2PCSxx, 2008

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